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Heterodyne-based hybrid controller for wide dynamic range optoelectronic frequency synthesis

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Abstract: Chip scale optical frequency combs using microresonators can enable a wide variety of applications from metrology to telecommunications. While tremendous progress has been made in miniaturizing the optical components, sources of variability and drift due to ambient conditions often limit their performance. We describe the design and implementation of a mixed-signal controller for optoelectronic frequency synthesis with notable frequency stability by locking it to an RF reference. A C-band tunable laser is phase-locked using commercial off the shelf components and custom board-level designs. Utilizing several laser inputs, our hybrid control loop enables a 50 nm tuning range with less than 10^{-12} frequency instability for 1 second averaging. A heterodyne receiver overcomes poor SNR of the photonics, and also features a scan-and-lock algorithm to facilitate an extended acquisition range. We report > 500 GHz frequency steps in 4.4 ms. All of the frequency settings and loop stability dynamics are programmable in real-time via a custom Graphical User Interface.

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1.   Introduction

The synthesis and control of the light emitted from a laser with radio frequency precision and agility is a long sought goal. An important advance was the introduction of octave-spanning, self-referenced laser frequency combs [1,2] that provide a direct microwave-to-optical connection. This has opened new opportunities for optical frequency metrology [3], direct frequency comb spectroscopy [4-6], and precision LIDAR [7,8], to name a few. Nonetheless, for many of these applications, the power of a single optical comb tooth is relatively small, and it would be valuable to have a single-frequency tunable output with milliwatt (or greater) power that is ultimately referenced to an absolute microwave reference via a frequency comb. This concept has been successfully implemented in a few laboratory experiments [9-11]. More recently, the introduction of microresonator Kerr frequency combs [12-15] provide a new opportunity for optical frequency synthesis in a compact chip-integrated format. Indeed, Kerr frequency combs have now been self-referenced [16-19], and radio-frequency-referenced optical synthesis with integrated photonic frequency combs and a tunable continuous wave (CW) laser has recently been demonstrated [20].

The basic architecture of such an optical frequency synthesizer includes a self-referenced Kerr frequency comb that provides the absolute frequency grid against which an integrated CW laser is tuned and phase-locked. A critical part of the optoelectronic integration of this architecture is the development and optimization of a phase-locked loop for the CW laser that can accommodate the desired dynamic range of 1 part per 100 trillion. This implies a combination of hertz-level precision and terahertz-wide frequency tunability (e.g. tuning across

the entire telecommunications C-band). While a phase-locked loop (PLL) approach can provide hertz-level stabilization, the single tuning knob of a classical PLL does not provide enough frequency span in the optical spectrum. One method is to employ coupled tuning of heaters and semiconductor optical amplifiers (SOAs), which requires simultaneous minimization of multiple nonlinear variables in the feedback loop. We present a novel optical PLL where the knobs are sequentially tuned in a coarse-to-fine fashion by exploiting the ability to freeze the loop in a hybrid analog-digital control loop. Though prior implementations have achieved similar broadband tunability and dynamic range, they require manual parameter setting through expensive benchtop sources. Our implementation on the other hand has fully integrated components with a tailored software interface and is a true standalone controller.

The paper is organized as follows: We present an overview of the overall frequency synthesis concept, along with brief descriptions of the photonic components utilized. Next, a digitally assisted analog front-end overcoming the limitation of low-Q components while enabling detection of signals with low SNR is discussed. We then discuss the details of a reconfigurable digital signal processor used in the control loop that avoids frequency multiplication. The design of a custom, low-noise tunable laser driver is then described. Results from synthesis experiments in both transient and steady-state situations are reported. Finally, we conclude the paper along with a discussion of future work.

2. System overview

An optical heterodyne detection is a common method for translating optical frequencies to the microwave domain. When used in synthesis applications, emission from a tunable laser (TL) is combined with an optical reference of precisely known wavelength. The difference in their frequencies can be detected on a photodiode and is stabilized to a fixed value in a phase-locked loop. This form of offset-locking , while limited in locking range to offset frequencies that can be detected and handled by the underlying electronics, can provide parts per trillion frequency precision. As mentioned previously, a Kerr frequency comb can be utilized to generate a multitude of optical references with fixed frequency spacing, facilitating manageable offset frequencies over the optical range of the TL. While there is plenty of literature on Kerr frequency comb generation, the corresponding standalone electronic stabilization system has not garnered much attention. While the goal is to eventually have an integrated frequency comb reference, we focus the current paper on the control system used to stabilize the tunable laser and for simplicity we use two commercial lasers to emulate the comb teeth.

2.1. Tunable laser

The tunable laser, fabricated by Aurrion, Inc., emits up to ~4 mW of CW light coupled into a fiber. An SOA provides an on-chip small-signal gain >10 dB. As seen in Fig. 1(b), the TL contains a gain section, a phase section and two micro-rings. The gain section and the SOA consist of InP-based quantum wells heterogeneously integrated on a silicon (Si) waveguide [21].

Current can also be injected in heaters implemented on the phase section. This allows modifying its refractive index and finely tuning the laser emission wavelength. The two microring resonators are designed with a high quality factor and slightly different radii [22,23]. This so-called Vernier effect provides a narrow-band optical filter, which allows for a large side-mode suppression ratio in the laser emission spectrum. The center of this filter can be thermally tuned by changing the current in heaters implemented on top of each ring. These heaters were designed with small thermal impedance to minimize the electric power required for thermal tuning. With a careful adjustment of the current injected through the phase section and the ring heaters, the emission wavelength of this PIC can be tuned over 50 nm centered around 1540 nm.

The major caveat to heater control is the long time constant associated with thermal settling, an unsuitable trait for the wide loop bandwidth and fast settling times desired in this system.
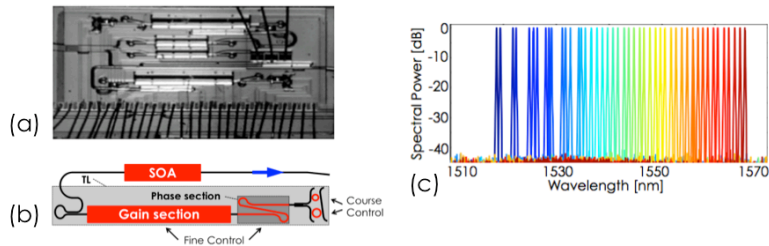
Fig. 1. (a) Die photograph of the PIC. The top half contains components for generating the optical comb reference. The bottom half of the die features the tunable laser. (b) Schematic of the TL. Black segments represent Si waveguides, and the blue arrow indicates laser light is emitted to the right. (c) OSA measurements demonstrating the spectral range of the TL.

Adjusting the current in the laser's gain section provides another tuning knob where the underlying physics allow ~GHz modulation bandwidth. We therefore use this as our high bandwidth control point, with the ring and phase heaters providing coarse tuning.

2.2. Controller architecture

Frequency synthesis is achieved with the feedback loop shown in Fig. 2. The two reference lasers imitate comb teeth spaced several modes apart for the following stability and switching measurements. Light from the tunable laser output is coupled and the resulting beatnote is detected on a benchtop photodiode and transimpedance amplifier, the Agilent 11982A.

Early synthesis experiments showed that the unlocked tunable laser periodically exhibits a frequency jitter larger than our acquisition range and faster than our loop bandwidth. To prevent us from losing lock when this occurs, we divide the beatnote frequency by 16 with two high-speed dividers. Low noise amplifiers are also inserted to amplify the input and output signals to suit the full-scale range of each commercial component.

The digitally assisted analog front-end, later described in detail, utilizes down conversion to limit the noise bandwidth and improve the beatnote's SNR. In-phase and Quadrature (I/Q) signals
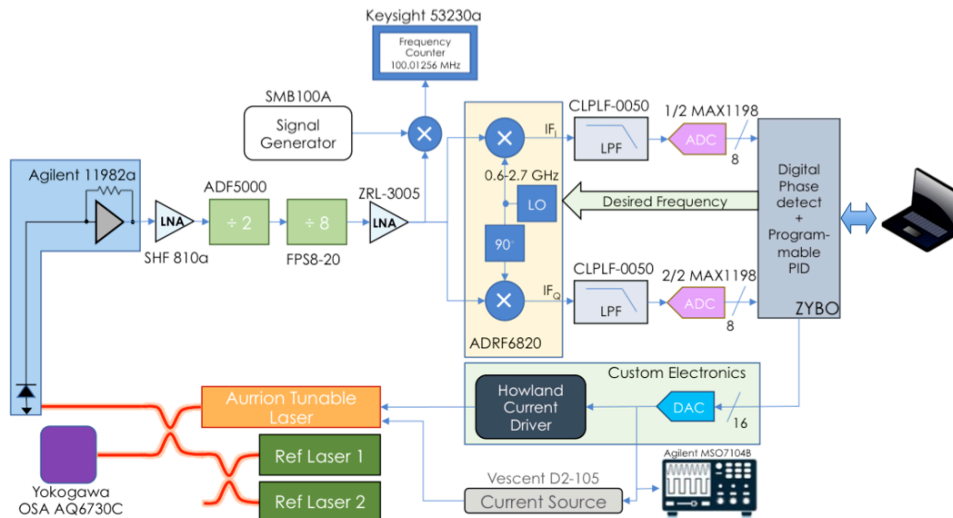

Fig. 2. Overview of the optical frequency synthesizer.

allow us to implement a digital image rejection [24], which will be crucial in the integrated system when the optical comb teeth can produce multiple undesired beatnotes that appear as images. The I/Q signals are converted to the digital domain through a dual-channel, high-speed ADC (MAX1198). In addition to image rejection, moving to the digital domain facilitates the complex control of the TL's multiple tuning knobs. This is performed on a Xilinx Zybo FPGA/ARM SoC.

The FPGA implements a multiplierless digital signal processor for phase error detection and correction, while the ARM processor manages user requests. The error correction — implemented as a programmable PID loop filter — outputs a feedback signal, which is summed with the laser DC operating point bias currents. Our custom PCB implements all of the tunable laser's current drivers through 16-bit voltage DACs and voltage-to-current converter circuits.

Stability of the PLL is achieved through proper selection of coefficients in the programmable loop filter. This is currently configured for lead-lag compensation to provide the highest loop bandwidth with ample stability (>60° phase margin). While this particular tunable laser has a high frequency conversion gain (K_{VCO} = 300 MHz/mA), the loop filter provides the ability to shift the overall gain of the loop up or down to accommodate a variety of lasers. In the current implementation, the dominant latency in the path comes from the 1 Msps update rate of the voltage DACs. Therefore, a 20 kHz bandwidth is chosen to avoid any significant phase degradation associated with this latency. Closed loop results presented in Section 6.2 show that the transient rise times correspond to this set bandwidth.

2.3. Digital interfacing

The complexity of the loop is hidden from the end-user by seamless integration with a software interface. However, the large number of disparate components with vendor specific interfacing requirements makes this quite challenging. We solved this issue by utilizing a central processing unit (the ARM Cortex-A9), which communicates with the reconfigurable digital logic and the data converters.

Several layers of abstraction are crossed in designing a synthesizer from a Graphical-User-Interface (GUI) down to the IC level. Detailed in Fig. 3, each of these layers required us to develop a protocol for real-time communication up and down the hierarchy.

Our top-level GUI is a standalone executable created in Microsoft Visual Basic. Commands from the user, such as *Turn Lock On* or *Change Wavelength*, are translated in the software and sent over USB to the FPGA's JTAG port. The FPGA features a hardwired ARM Cortex-A9
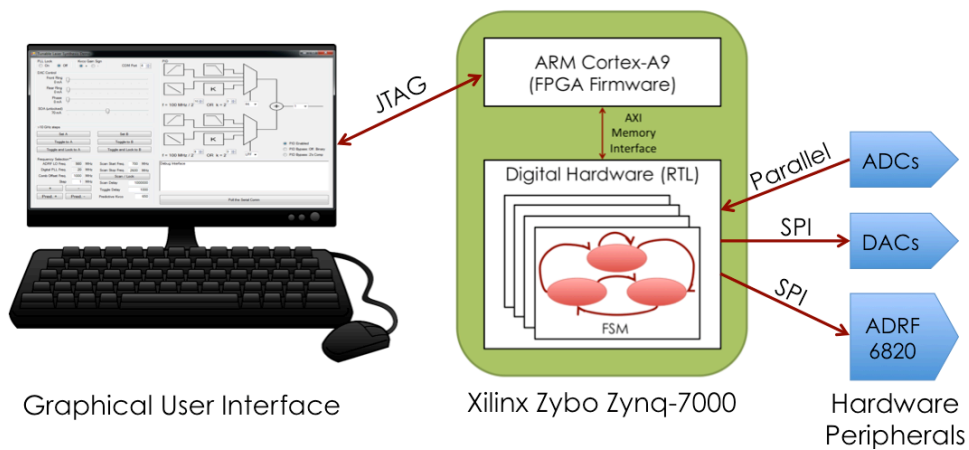

Fig. 3. Various digital standards utilized to interface from the hardware to the GUI.

processor that runs a custom firmware.

When a GUI command is received, the firmware deciphers it and sends lower level requests via a Xilinx AXI Memory Interface [25]. This built-in protocol allows the processor to write to allocated memory blocks that custom HDL can read from, and vice-versa. Our Verilog is composed of several finite state machines (FSMs) where each handles processor requests for a major component in the system. The FSMs controlling the evaluation modules (DACs, ADCs, and ADRF6820) utilize a SPI or Parallel Bus to communicate between the FPGA and IC.

3. Digitally Assisted Analog Front-End

The other comb lines of the optical comb reference (second reference laser in the current configuration) contribute a significant amount of stray power relative to the single beatnote we are trying to detect and phase-lock. In the electrical domain this translates to a poor SNR, further exacerbated by the large frequency range of the beatnote (DC - 7.5 GHz). While high-Q RF filters could be used to reduce the noise bandwidth, the Q's required are excessively large and hard to implement, especially when the center frequency is high. One way to relax the Q constraint is to translate the center frequency so that the same noise bandwidth can be achieved with a lower Q filter. We utilized a heterodyne receiver to implement the down conversion and a low-pass filter as a moderate Q filter to improve the SNR.

The ADRF6820 evaluation board from Analog Devices was chosen to mix the incoming signal down to an intermediate frequency. The ADRF6820 features a tunable local oscillator (LO) that spans 675-2700 MHz. With a desired intermediate frequency between 20-25 MHz, this allows us to phase-lock the incoming signal within 695-2725 MHz ($\omega_{IF} = \omega_{IN} - \omega_{LO}$). The local oscillator frequency is locked via its own on-board PLL, with the frequency programmed via a SPI bus.

One key challenge is to find the beatnote before initial lock is acquired or after switching to a far-off wavelength due to the finite loop bandwidth and acquisition range. Predefined set points for the heaters allow us to reliably move the tunable laser to the correct comb tooth, though the absolute offset frequency can vary several hundred megahertz due to thermal fluctuations. With our 100 Msps ADC, the front-end is limited by a +/- 25 MHz acquisition range to find the beatnote and acquire lock. To alleviate this we sweep the LO across its full range and detect when the mixed down signal is within our ADC bandwidth. Figure 4 animates how this sweep is performed. In the top row (a), the LO is far from the RF input and the outputs do not fall within the ADC bandwidth. Eventually the LO is brought close enough to the input (b), and the
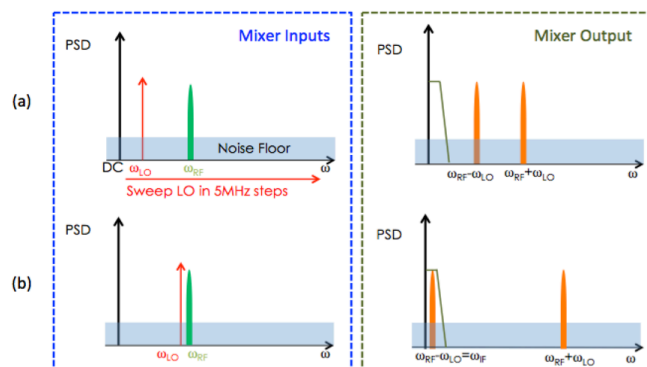

Fig. 4. Power spectral densities for the mixer inputs (left) and mixer output (right). Cases are illustrated for when the LO is far from the incoming signal (a) and when the LO is brought close (b).

down-converted signal is detected on our ADC. Following the sweep, we acquire lock at that frequency and subsequently track thermal drift or synthesize any desired offset frequency.

This sweep algorithm is the largest factor in our frequency switching timing. We reduced the scan time by performing a coarse-fine sweep, which requires less LO steps to find the signal. By default, the ADRF6820 performs a calibration of its VCO's internal settings each time the LO is stepped, requiring 2 ms per step. Figure 5 demonstrates how overriding the calibration and providing our own VCO internal settings made the sweep 256 times faster. The slower sweep is done once at startup, and the ADRF6820's calibration results are stored in a lookup table (LUT) in the FPGA which is used for the remainder of operation.

The ADRF6820 outputs in-phase and quadrature (I/Q) signals, which allow for image rejection and phase unwrapping in the digital domain. Commercial 5th order low-pass filters provide anti-aliasing before the MAX1198EVKIT samples I and Q simultaneously. This dual-channel, 100 Msps ADC transmits the 8-bit conversion of both signals to the FPGA over a parallel bus.
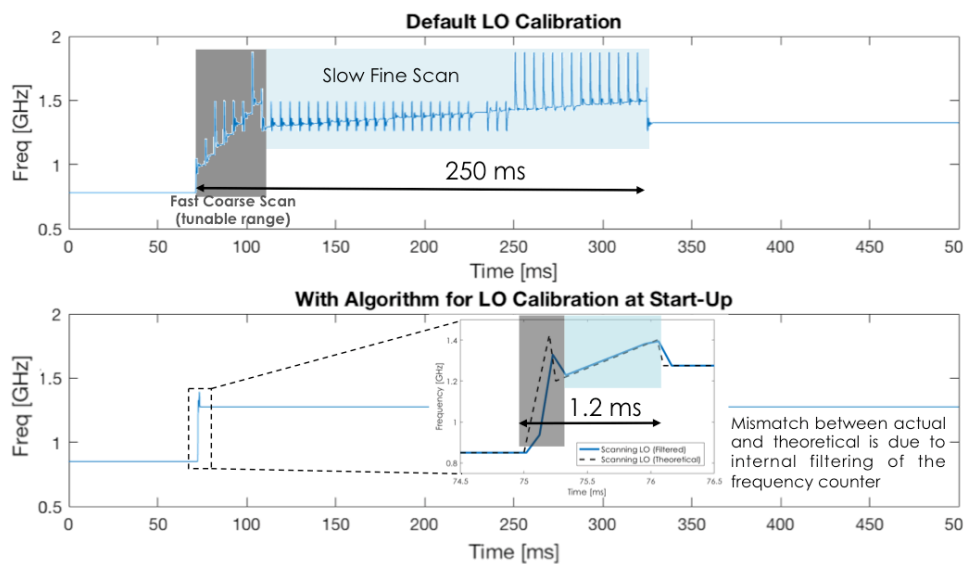

Fig. 5. Transient measurement of the LO's frequency during the coarse-fine scan used to detect the beatnote (located at 1.35 GHz). Implementation of the LO calibration algorithm at start-up improves the speed of this scan significantly. Once the scan is complete, the LO frequency is properly set and the phase-locked loop can be closed.

4. Multiplierless digital signal processor

Due to the complexity of controlling several non-linear inputs to the tunable laser, we chose to handle error detection and correction in the digital domain. Multiplierless implementations were specifically chosen to minimize power and area consumption on the FPGA.

Once the I/Q signals are digitized, the instantaneous phase is computed using a Coordinate Rotation Digital Computer (CORDIC) computation block. The instantaneous phase from this block is then compared to an ideal reference phase inside the phase comparator block, which gives us the phase difference (error signal). The phase difference is fed into the programmable loop filter, which generates the control signal for the gain section of the laser.

4.1. Arctangent

To compute the instantaneous phase of the IF signal, we use the I and Q signals as two arguments for the CORDIC. This block, used in the vectoring mode, is a slight variation of the architecture used in the seminal work done by Volder et al. [26]. Instead of using expensive multiplication and division operations to compute the arctangent, the algorithm in Fig. 6 formulates the problem in such a way that it can be computed iteratively with the use of simultaneous shift and add blocks, thereby substantially reducing area and power consumption. The traditional implementation of the
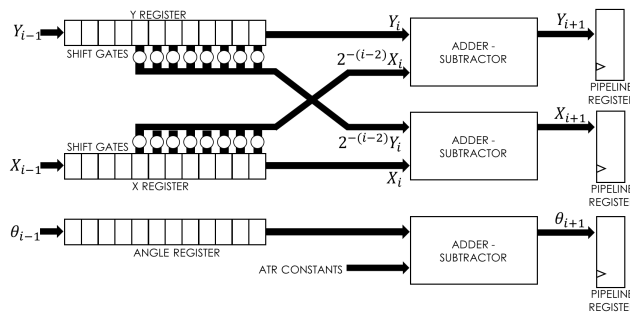
Fig. 6. CORDIC Arctangent computes the phase of the beatnote in a multiplierless configuration.

CORDIC algorithm has a latency of 16 cycles and a throughput of 1 output (instantaneous phase) every 16 cycles. This implementation can further be improved by pipelining the computation. The pipelined architecture still has a latency of 16 clock cycles but has an improved throughput of 1 output (instantaneous phase) every clock cycle.

4.2. Phase comparator

The instantaneous phase of the IF signal is then compared to an ideal phase, which is generated with respect to our reference clock. The ideal phase is constructed as a 14-bit accumulation of an expected rate of change and is compared to the instantaneous phase computed by the arc tangent block. The comparator output has two extra bits to allow an overflow and underflow of $\pm 2\pi$ respectively.

4.3. Programmable loop filter

The 16-bit output from the phase comparator is then fed into the programmable loop filter that generates the control signal for the gain section of the laser.
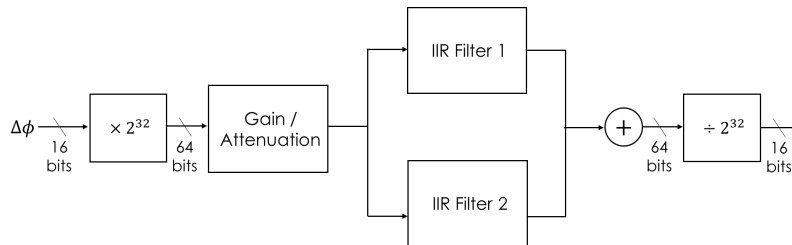

Fig. 7. Programmable Loop Filter

The two IIR filters in the figure can be configured to be integrators, low-pass filters, differentiators, or proportional gain blocks. The parameters for these blocks are dynamically updated by the user via the GUI, which allows them to adapt to the laser's bandwidth requirements in real-time.

A peculiar characteristic of the implementation in Fig. 7 is that all the IIR filter coefficients and gain parameters are restricted to be powers of 2. This enables the implementation to carry out the computation using simultaneous shift and add operations and does not use any multiplication or division operations, resulting in lower area and power consumption.

5. Tunable laser driver PCB

This PCB was designed with the goal of creating many low-noise and high resolution drivers, with minimal interfacing to the FPGA. The AD5676R was chosen as an 8 channel, 16-bit voltage DAC. In order to properly drive the diode sections of the laser, each DAC voltage is converted to a current through the Improved Howland Current Pump shown in Fig. 8(a). Detailed in the following equations, the feedback loop governs $I_{OUT} = V_{DAC} / R_5$. This lets us change the full-scale range of drivers individually, despite them sharing an octal DAC with a fixed full-scale range.
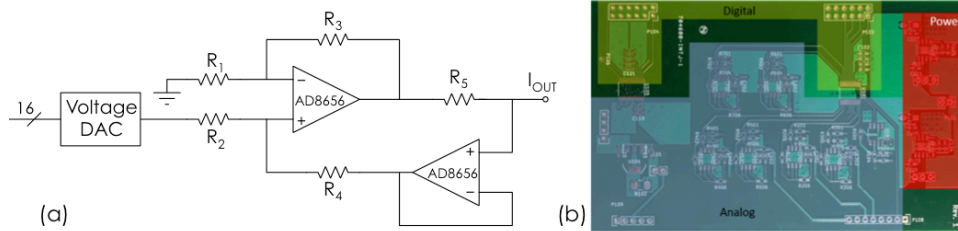

Fig. 8. (a) Schematic for the Improved Howland Current Pump. An unbuffered voltage DAC input is translated to a low-noise current output with flexible full-scale range. (b) PCB design which implements several Improved Howland Current Pumps to control the tunable laser.

$$V_+ = \left(\frac{R_4}{R_1 + R_4} \right) [V_{DAC} - V_{OUT}]$$

$$V_o = \left(1 + \frac{R_3}{R_2} \right) V_+$$

$$I_{OUT} = \frac{V_o - V_{OUT}}{R_5}$$

Set $R_1 = R_2 = R_3 = R_4$

$$\therefore \quad I_{OUT} = \frac{V_{DAC}}{R_5} \qquad (1)$$

The laser gain section is our frequency-tuning knob and requires fine resolution to reach our Hz tuning specification. We selected a full-scale range of 2 mA for our Improved Howland Current Pump output — corresponding to 30 μA LSB steps from the DAC — and summed that current with a DC bias of 65 mA. The phase section and ring heaters each require a 20 mA full scale range in order to span all wavelengths, and a smaller value for R_5 can accomplish this. The AD8656 op-amp was carefully chosen to meet the demands of our system (high bandwidth, low noise, >20 mA output current). The current driver exhibits 15.2 μA_{RMS} noise, limited by the output noise voltage DAC.

The PCB layout in Fig. 8(b) prioritizes the isolation of analog traces and power supplies, to prevent digital signals from coupling to the outputs. The digital SPI bus plugs directly into the FPGA evaluation board, which minimizes trace length and allows us to reach the maximum clock rate and update rate of the DACs. These design techniques helped us realize low-noise drivers with minimal coupling.

6.   Results

The measurement equipment used in the system is present in Fig. 2. A Yokogawa AQ6730C Optical Spectrum Analyzer (OSA) allows us to record the optical spectra with 20 pm resolution but we rely on RF analysis to report synthesizer performance. The divided beat note is down converted to a frequency that can be tracked by a Keysight 53230A Frequency Counter. This is used to measure Allan Deviation (ADEV) and switching times for larger frequency steps. The Keysight 53230A is known to perform internal filtering that makes it unsuitable for measuring fast frequency steps such as <1 GHz changes offset of the the same comb tooth. We therefore report the settling time of our DAC measured on an oscilloscope.

6.1.   Frequency stability

The RF beatnote frequency is plotted as a transient in Fig. 9(a). While most of the data are contained within the frequency counter's noise floor, it is clear that a non-white noise source causes significant frequency deviations with a tendency to occur in the upward direction. We believe that poor SNR going into the frequency dividers causes extra toggles, manifesting as these large glitches.
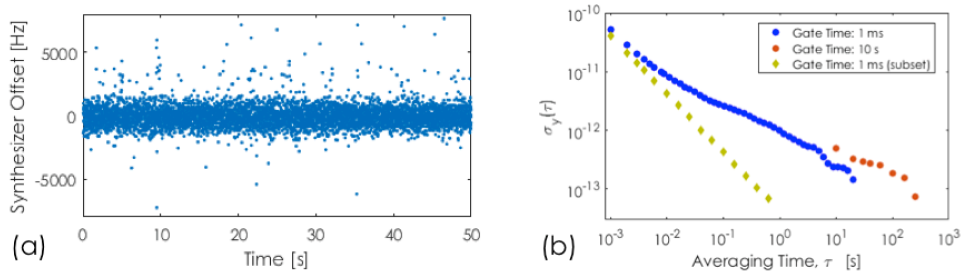

Fig. 9. (a) Transient frequency counter data for the synthesizer's beatnote. (b) Overlapped Allan Deviation of the synthesizer's beatnote.

Long-term frequency stability is shown as an overlapped ADEV in Fig. 9(b). 1 millisecond gate time is used for short averaging values though the noise floor becomes a limitation far out. A 10 second gate time measurement is also analyzed to expand the trend for longer averaging. The glitches described above prevent the deviation from averaging at the rate of $1/\tau$. A subset of the data which contained no frequency glitches is also plotted (green diamonds). We believe the synthesis can approach this long-term stability once the glitches are removed. Our future implementation will move the frequency division after the down-conversion and low pass filter, which will decrease the noise bandwidth and improve SNR several orders of magnitude.

6.2.   Switching speeds

Frequency steps <10 GHz are requested from the GUI and executed in several actions. With the tuning of the gain section known (units MHz/mA), we first break the feedback loop and change the DAC to the current that we predict sets our desired frequency. We then program a new LO frequency so the anticipated beatnote is within our IF bandwidth, and finally re-close the feedback loop.

Several different sized steps are shown in Fig. 10. The settling time in a linear regime is inversely proportional to the PLL's bandwidth, in our case 20 kHz. This is limited by the dominant latency in our system, the 1 Msps update rate of our DAC. It would be expected that all three steps have the same settling times if we were purely limited by the PLL bandwidth. Our commercial DAC also introduces a slew rate limitation, causing the larger steps to have longer settling times.
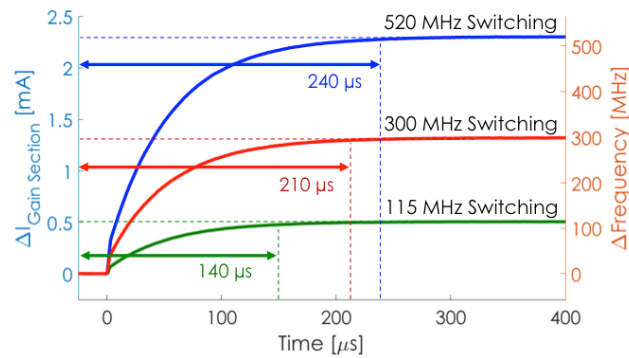
Fig. 10. Transient response of the change of current (left axis) in order to step the output frequency (right axis).

These results show that our future efforts need to focus on a higher bandwidth DAC with a faster slew rate.

Frequency switching times >100 GHz are also reported, outside the linear range of our gain section tuning knob. A LUT adjusts the ring heaters to bring the tunable laser wavelength to the desired comb tooth. Thermal drift after changing the heaters powers can cause significant output drift (14 GHz/°C), so our current algorithm waits for the PIC to reach thermal stability before attempting lock. We then perform our scan-and-lock algorithm to pull the beatnote within our IF bandwidth and reacquire lock.

The optical spectra in Fig. 11 show the tunable laser moving from an offset of one comb tooth to another. This is also captured in a transient measurement of the RF beatnote frequency in Fig. 12(a,b,c). The laser moves wavelengths in <100 μs though the thermal equilibrium is reached over 4 ms. The scan finds the new beatnote frequency and lock is achieved in 400 μs. We envision the future system controlling the heaters with pre-emphasis drive in order to accelerate the thermal settling and eliminate the dead-time delay for the worst case scenario [27].
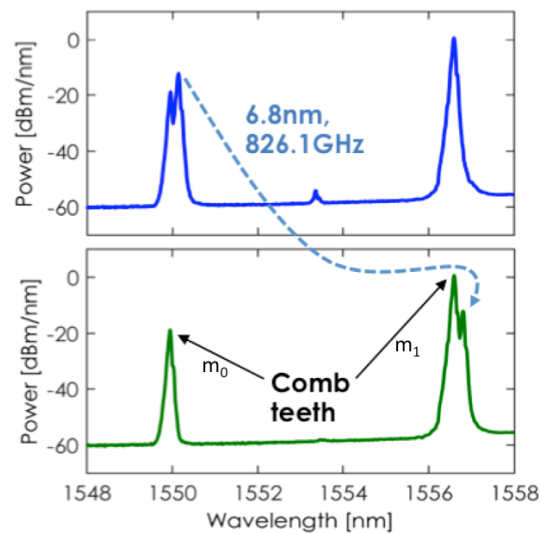

Fig. 11. OSA spectra showing the tunable laser move from an offset of one comb tooth to another. The jump is measured as 6.8 nm, corresponding to 826.1 GHz.
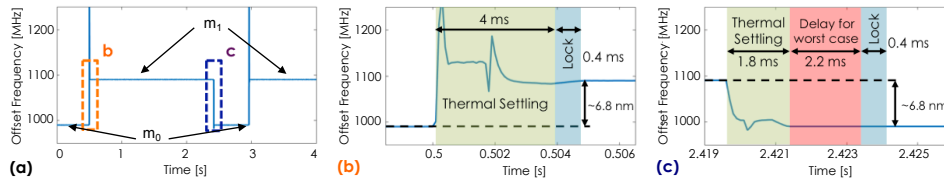
Fig. 12. Transient response of the tunable laser beatnote switching between states shown in Fig. 11, captured on the frequency counter.

7. Conclusion

In summary, we have presented a comprehensive system that enables optoelectronic frequency synthesis. Custom design implementations from the board level up to the GUI allow the user real-time control over our fully configurable frequency synthesizer. Spanning 50 nm of range required multiple tuning knobs, while achieving 10^{-12} stability also necessitated a high bandwidth knob for noise suppression. The optical design constraints also presented an SNR limitation and challenges for lock acquisition, both of which were addressed by a heterodyne receiver featuring a coarse-fine scan-and-lock algorithm. Ultimately, this architecture enabled wavelength switching >5 nm in less than 5 ms.

Moving forward, this research will be focused on designing an ASIC that performs all of this functionality, while improving upon the limitations of current commercially available board-level components. A custom analog front-end with an integrated .1-15 GHz downconversion will allow us to lock the beatnote across the full range between optical comb teeth, compared to the .675-2.7 GHz input range of the current evaluation module. While the commercial DAC limited our 20 kHz bandwidth and switching speeds, the ASIC laser drivers will target a faster update rate with slew considerations, to allow >1 MHz bandwidth with greater noise suppression and faster switching. We envision cointegration of this ASIC and the PICs will enable new fields for metrology with a low-cost, minimal SWaP optical frequency synthesizer.