

Received January 26, 2022, accepted February 8, 2022, date of publication March 8, 2022, date of current version March 16, 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3157332

Levelized Cost of Energy-Oriented Modular String Inverter Design Optimization for PV Generation System Using Geometric Programming

YEONGRACK SON¹, (Member, IEEE), SATYAKI MUKHERJEE^{2,3}, (Member, IEEE),
RAHUL MALLIK⁴, (Graduate Student Member, IEEE),
BRANKO MAJMUNOVIĆ², (Graduate Student Member, IEEE),
SOHAM DUTTA⁴, (Graduate Student Member, IEEE),
BRIAN JOHNSON⁴, (Member, IEEE), DRAGAN MAKSIMOVIĆ², (Fellow, IEEE),
AND GAB-SU SEO¹, (Senior Member, IEEE)

¹National Renewable Energy Laboratory, Power Systems Engineering Center, Golden, CO 80401, USA

²Department of Electrical, Computer, and Energy Engineering, University of Colorado at Boulder, Boulder, CO 80309, USA

³Milan M. Jovanović Power Electronics Laboratory, Delta Electronics (Americas), Durham, NC 27709, USA

⁴Department of Electrical and Computer Engineering, University of Washington, Seattle, WA 98195, USA

Corresponding author: Gab-Su Seo (gabsu.seo@nrel.gov)

This work was authored in part by Alliance for Sustainable Energy, LLC, the manager and operator of the National Renewable Energy Laboratory for the U.S. Department of Energy (DOE) under Contract No. DE-AC36-08GO28308. Funding provided by U. S. Department of Energy Office of Energy Efficiency and Renewable Energy Solar Energy Technologies Office, and Laboratory Directed Research and Development program of National Renewable Energy Laboratory.

ABSTRACT Levelized cost of energy (LCOE) is a commonly used metric to assess the cost-to-benefit ratio over the lifetime of an energy resource, such as photovoltaics (PV); however, power electronics engineers tend to rely on metrics such as efficiency and power density, which do not guarantee lifetime cost optimality. Recent work has shown that an LCOE-focused optimization approach can yield improved system designs, leading to improved lifetime performance with balanced lifetime cost and energy generation. This paper outlines an LCOE optimization framework for PV power electronics that uses geometric programming. The large number of circuit parameters and nonlinear nature of the system equations pose significant barriers. Our approach allows for decoupling the design variables, which, in turn, enables superior computational efficiency and a near-optimal solution. By incorporating the power electronics design process and magnetic loss mechanism into the convex design framework, the optimization engine yields practically implementable parameters for a PV converter that minimizes LCOE. An optimization example for a cascaded modular PV inverter architecture is presented that suggests 3.35% LCOE improvement can be achieved by the new power electronics and the advanced optimization. The proposed optimization framework can be applied to other power generation systems to evaluate the effect of the power electronics design on system lifetime costs and efficiency.

INDEX TERMS Convex optimization, geometric programming, levelized cost of energy, lifetime energy cost, magnetic loss modeling, solar inverters, modular multilevel converter.

I. INTRODUCTION

Demand and the importance of renewable energy have been rapidly increasing because of recent technology advancements that are leading to significant improvements in cost-effectiveness, comparable to conventional generation [1]. Among renewable energy resources, photovoltaics (PV) are

becoming increasingly common in all sectors, i.e., at the utility, commercial, and residential scales. Recent reports show that new installations of PV have increased by an order of magnitude during the last decade, and the generation cost of a PV system is even lower than conventional energy sources in some regions [2].

To improve PV system performance and displace retiring conventional generation, recent research and development efforts have focused on cost reduction with balanced

The associate editor coordinating the review of this manuscript and approving it for publication was Lorenzo Ciani ^{id}.

performance [3]. The levelized cost of energy (LCOE) is a widely accepted metric used to evaluate a technology's performance [4]. The LCOE measures the energy cost required to generate a unit amount of energy for a system's lifetime, e.g., \$/kWh. To estimate the lifetime cost and energy yield, it factors in comprehensive system-level characteristics, such as cost for procurement and installation, PV panel efficiency and degradation, cost for maintenance and downtime, and financial factors for investment. By reflecting and balancing multiple aspects, the LCOE-oriented system design can be used to maximize system performance.

Prior LCOE-oriented works on PV generation systems have analyzed the cost share of the system components and their impacts on the LCOE in the scope of the entire system [5], [6]. Moving the scope inside the system, several studies have been conducted to compare the technologies or different conditions in a region [7]–[10]. Most prior work using the LCOE has not considered the PV inverter, which is an essential element for dc-to-ac power conversion and the grid interface; in general, parameters in the power conversion (e.g., efficiency and cost) are assumed to be given or negligible. In power electronics designs, on the other hand, power conversion efficiency and component cost are common design metrics, but, in general, their impact on the system-level performance metrics has not been a high priority. The inverter performance, however, has been found to be not negligible; moreover, inverter performance can significantly impact the entire system's performance, including its LCOE [11]. An LCOE optimization methodology for a PV inverter system incorporating the reliability of the components, reported in [12], demonstrated how component design optimization leads to LCOE reduction. In [13], Saridakis *et al.* presented a design optimization approach to evaluate the impact of using Silicon Carbide (SiC) power switches in PV inverters. By balancing the switching frequency and output filter structure, they showed the potential of the SiC PV inverters with device cost reduction compared to Silicon-based ones. A recent work reported in [14] studied the impact of different PV power conversion system architectures on LCOE, including conventional central and string inverters and multiport dc transformers, with battery storage at the utility scale. Reference [15] discussed PV inverter LCOE improvement by employing absolute active power control to contribute to extending the inverter lifetime with thermal stress on power switches controlled. Because the LCOE of a generation system can be designed to represent the detailed impact of the design parameters of interest, an LCOE-oriented design methodology can derive improved design by balancing both efficiency and cost with proper system modeling [11], [12], [14]. In addition, it can be used to evaluate the relative value of a new technology compared to the baseline state-of-the-art solutions [13]–[15].

This paper presents an LCOE-oriented PV inverter design optimization. Distinguished from prior works that used exhaustive search [11], [15] or genetic algorithms [12], [13], geometric programming (GP) is employed in this

optimization work for its superior computation efficiency. In addition, GP can guarantee the global optimal point obtained with detailed models, if the optimization problem is well constructed to have a specific form that is compatible with the method [16]. Section II presents an introduction to the GP optimization. Component-level modeling for the power conversion loss and the cost to model the LCOE improvement from a new technology are introduced in Section III. Section IV presents an optimization case study of a cascaded modular PV inverter system design with the GP algorithm, rated for a 200-kW commercial-scale PV generation. The proposed LCOE-oriented design optimization is validated by comparing its results with ones from the physics model-based method. Section V concludes the paper with final remarks.

II. GEOMETRIC PROGRAMMING

GP is an optimization problem-solving algorithm that has a special form of objective and constraint functions, called posynomial. The posynomial function can be defined as:

$$f_{posy}(x) = \sum_{k=1}^K (c_k x_1^{a_{k1}} x_2^{a_{k2}} \dots x_n^{a_{kn}}), \quad (1)$$

where x_1, x_2, \dots, x_n are optimization variables; and the coefficients, c_k , and exponents, $a_{k1}, a_{k2}, \dots, a_{kn}$, are the model parameters, which are determined by the model characteristics. Here, the optimization variables and the coefficients are positive real, and the exponents are real values. This is why this form is called “posynomial,” which is “positive,” and “polynomial.” K is the number of terms in the posynomial function, and it is in monomial form when $K = 1$. The standard form of GP is expressed as:

$$\begin{aligned} \text{minimize } f_o(x) &= \sum_{k=1}^K (c_{ok} x_1^{a_{ok1}} x_2^{a_{ok2}} \dots x_n^{a_{okn}}) \\ \text{subject to } f_i(x) &= \sum_{l=1}^L (c_{il} x_1^{a_{il1}} x_2^{a_{il2}} \dots x_n^{a_{iln}}) \\ &\leq 1, i = 1, \dots, m \\ h_j(x) &= c_j x_1^{a_{j1}} x_2^{a_{j2}} \dots x_n^{a_{jn}} = 1, j = 1, \dots, p, \quad (2) \end{aligned}$$

where f_o is the objective function, which should be minimized in the optimization problem; and f_i and h_j are the inequality and the equality constraint functions, respectively, which should be satisfied in the optimal point.

GP retains benefits in the convex optimization since it is a special expansion of the convex [16]. The convex optimization is mathematically proven to find the global optimal point if it exists. It is also known to have polynomial time complexity [17]; it can solve an optimization problem in a computationally efficient manner. The improvement in the computational performance of the convex optimization (and GP) has been attributed to the advancements in solvers, e.g., MOSEK [18]. Moreover, it has been recently found that many practical optimization problems, especially in electrical

circuit design and system optimization problems, have model functions that are equivalent or well approximated to the posynomial form; therefore, GP has been widely applied in practical electrical circuit/system design optimization problems [19]–[24].

The first step to solving the practical optimization problem with GP is to model the target system in a posynomial form. In case the system cannot be modeled, by nature, in posynomial, approximation or fitting is required. Provided that the original non-posynomial model is $f(x)$, with data points $(x, f(x))$ and its posynomially fitted form, $f_{fit}(x)$, the set of unknowns in $f_{fit}(x)$, with the coefficients and exponents in (1), is found by fitting functions to minimize the deviation of $f_{fit}(x)$ from $f(x)$. In the fitting process, the sum of the square of the relative errors:

$$\sum_{i=1}^N r_i^2 = \sum_{i=1}^N \left(\frac{f^{(i)}(x) - f_{fit}^{(i)}(x)}{f^{(i)}(x)} \right)^2 \quad (3)$$

or the maximum relative error:

$$\max \left(\left| \frac{f^{(i)}(x) - f_{fit}^{(i)}(x)}{f^{(i)}(x)} \right| \right), \quad i = 1, \dots, N \quad (4)$$

is commonly used as the error term, where N is the number of data points of $(x, f(x))$. The fitting process is a nonlinear optimization problem, and general nonlinear least-square methods—such as Gauss-Newton [25] or Levenberg-Marquardt [26]—can be used to find the unknowns that minimize the error. These methods are not guaranteed to converge to the global optimum, and the solution depends on the initial values of the unknowns. So the accuracy of the solution can be enhanced by repeated trials with changing initial values. There are several techniques to reduce the error in the posynomial fitting [27], [28]. In these works, the fitting error is reduced by applying a larger number of monomial terms or by breaking the data set into clusters and performing the fitting with each cluster.

The GP problem with optimization variables that are contained within a certain discrete set, such as an integer, is called mixed-integer geometric programming (MIGP) [16], [29]. It cannot be solved with the same method as the ordinary GP, and methods for solving the MIGP have some drawbacks compared to those for the GP solver. The methods to solve the MIGP can be classified into two types. The first is the heuristic method. To obtain a solution, the heuristic method first relaxes the integer constraints and solves the relaxed noninteger GP problem. After solving, the relaxed values of the variables are rounded to integer variables, and the optimization process is completed by solving the reduced-order optimization problem, with integer variables fixed to the rounded values. Once formulated, it can calculate the optimum in a computationally efficient manner; however, because the process of relaxation and rounding is an approximation of the originals, it may find a design point that deviates from the global optimum. The second is the global method. In this method, the GP optimization runs multiple cases with

different sets of fixed integer variables to find the global optimal. Since it explores the entire design space, it can find the global optimum at the cost of additional computation. One should consider the trade-offs (computation and accuracy) when choosing the method for an MIGP problem.

III. OPTIMIZATION MODEL

LCOE presents the lifetime energy cost of a generation system. This value incorporates system performance metrics, including the system efficiency, cost, degradation of the equipment, and interest rate; therefore, an LCOE-oriented optimization can identify the optimal system design for the minimum lifetime cost. LCOE for a generation system can be defined as:

$$LCOE = \frac{C_{life}}{E_{life}} = \frac{C_0 + \sum_{t=1}^T \frac{C_t}{(1+i)^t}}{8760 \cdot P_{rated} \cdot \gamma \cdot (\sum_{t=1}^T (1-\delta)^{t-1})}, \quad (5)$$

where C_{life} and E_{life} are the lifetime cost and energy generated, respectively. C_0 is the initial investment cost, including installation cost; C_t is the yearly dispensed cost; and P_{rated} is the rated power of the system; $\gamma = c_t \eta$ is the ratio of actual power per year considering the system efficiency (η) and capacity factor (c_t), considering irradiance and temperature for a geographic region; δ is the degradation factor, such as PV module degradation; and i is the interest rate.

By comparing the LCOE value to baselines, the effectiveness and performance of a new technology can be evaluated. In case of evaluating a new power electronics technology, i.e., replacement of the PV-to-grid power conversion architecture, the parameters related to the power conversion would vary, including the installation cost (inverter and transformer cost), C_t , and the power conversion efficiency, η . On the other hand, the rest of the parameters in (5) would remain unchanged, such as the cost and degradation factor for the PV modules. Based on this rationale, the LCOE of the system with a new topology can be rewritten and simplified, focusing on the changes, as:

$$\begin{aligned} LCOE_{new} &= \frac{(\bar{C}_0 - \Delta C_0) + \sum_{t=1}^T \frac{C_t}{(1+i)^t}}{8760 \cdot P_{rated} \cdot c_t(\bar{\eta} + \Delta\eta) \cdot (\sum_{t=1}^T (1-\delta)^{t-1})} \\ &\approx \overline{LCOE} - \frac{\Delta C_0}{\bar{E}_{life}} - \overline{LCOE} \frac{\Delta\eta}{\bar{\eta}} \end{aligned} \quad (6)$$

where ΔC_0 and $\Delta\eta$ are the cost and efficiency change by applying the new topology, respectively. \bar{C}_0 , $\bar{\eta}$, \overline{LCOE} , \bar{E}_{life} are the initial cost, efficiency, LCOE, and lifetime energy generation of the baseline topology, respectively. The LCOE improvement resulting from replacing the power conversion architecture in the new topology can be expressed as follows:

$$\frac{\Delta LCOE}{\overline{LCOE}} = \frac{\overline{LCOE} - LCOE_{new}}{\overline{LCOE}} = \frac{\Delta C_0}{\bar{E}_{life} \overline{LCOE}} + \frac{\Delta\eta}{\bar{\eta}}. \quad (7)$$

Since lower LCOE translates into a lower cost required to generate the same amount of energy, the greater the

LCOE improvement factor (7) is, the better (lower) LCOE is expected. Based on this, (7) is used as the objective function for the optimization in the study.

To compute the improvement factor for a new power conversion technology, its cost and loss are required to derive ΔC_0 and $\Delta \eta$, as shown in (7). To abstract the two differentials, the major components in the power conversion that determine the two key metrics should be properly modeled. Since the power semiconductor devices and magnetic components, i.e., transformers and inductors, are the major drivers for the power electronics cost and loss, the modeling of the two is explained in the subsections.

A. SWITCH LOSS MODELING

The loss of the power semiconductor switch is represented by the conduction loss and the switching loss, which can be expressed as:

$$P_{cond} = i_{rms}^2 R_{ds(on)}, \quad (8)$$

$$P_{sw} = 2C_{oss} v_{sw}^2 f_{sw}, \quad (9)$$

respectively, where $R_{ds(on)}$, C_{oss} are the on-state resistance and the output capacitance of a switch device. i_{rms} , v_{sw} , f_{sw} are the root-mean-square (RMS) current, drain-source voltage, and switching frequency of the switch, respectively. Here, the relationship between $R_{ds(on)}$ and C_{oss} can be modeled considering the bare die area and height of the switch. The output capacitance, C_{oss} , can be modeled as the capacitance of the parallel plate capacitor as:

$$C_{oss} = \epsilon \frac{A_{die}}{W_d} + C_{fixed} \quad (10)$$

where W_d , A_{die} are the width and height of the bare switch die, and C_{fixed} is the offset capacitance. In case of a vertical SiC MOSFET, W_d and A_{die} can be modeled as:

$$W_d = \frac{2v_{BD}}{E_{C,SiC}},$$

$$A_{die} = K_{SiC} \frac{v_{BD}^\kappa}{R_{ds(on)}}, \quad (11)$$

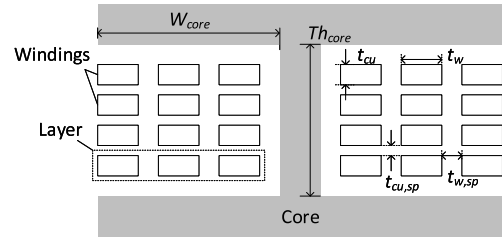
where v_{BD} is the blocking voltage of the switch. Coefficients of the switch characteristics, C_{fixed} , $E_{C,SiC}$, K_{SiC} and κ , can be extracted from the device data sheet. Substituting (10) and (11) into (9), the switching loss can be expressed in the posynomial form of $R_{ds(on)}$ and f_{sw} as:

$$P_{sw} = 2 \left(\epsilon \frac{K_{SiC} E_{C,SiC} v_{BD}^{\kappa-1}}{2R_{ds(on)}} + C_{fixed} \right) v_{sw}^2 f_{sw}. \quad (12)$$

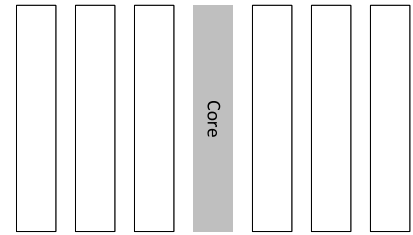
B. TRANSFORMER AND INDUCTOR LOSS MODELING

The loss of magnetic components can be modeled by the core loss and the copper loss. The core loss of the unit volume core can be expressed by the iGSE method [30] as:

$$P_{core} = \frac{1}{T_s} \frac{K_{fe}}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos \theta|^\alpha 2^{\beta-\alpha} d\theta}$$



(a) Front view



(b) Top view

FIGURE 1. Winding geometry for copper loss modeling of magnetic components.

$$\times \int_0^{T_s} (B_{pk-pk})^{\beta-\alpha} \left| \frac{dB}{dt} \right|^\alpha dt \quad (13)$$

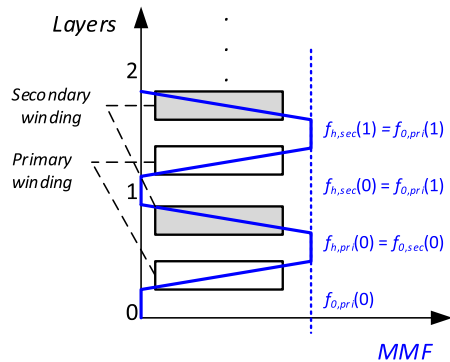
where α , β , and K_{fe} are parameters related to the core material and geometry and can be found in the core data sheet. T_s and B_{pk-pk} are the unit period of the ac excitation and the peak-to-peak value of the flux density of the core section, $B(t)$, within a single excitation period, respectively. In this model equation, the core loss can be expressed as a posynomial if $B(t)$ is properly modeled. Since $B(t)$ is based on the voltage profile applied to the component, its modeling and approximation process needed would depend on the circuit topology and operation. Section IV will provide an example modeling process of the core loss to formulate a posynomial form for the case study.

For the magnetic copper loss, Dowell's equation can be used [31]. This model function is derived by considering the dc resistance, skin effect, and proximity effect of the winding. Fig. 1 shows the design concept of the winding. In this figure, the shape of the winding is assumed to be rectangular, and t_{cu} , t_w are the thickness and width of a winding. W_{core} and Th_{core} are the width and thickness of the winding area in the core, respectively. Assuming that the current waveform at the winding is sinusoidal, the copper loss of a single layer winding in Fig. 1 can be expressed as:

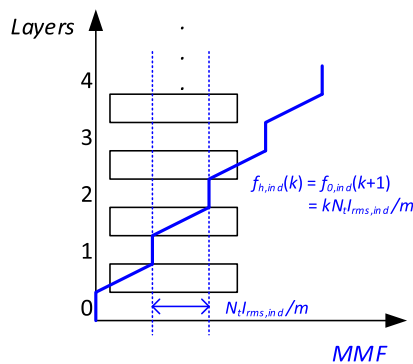
$$P_{layer} = \frac{\phi R_{dc}}{(N_t/m)^2} \left((f_h^2 + f_0^2) \left(\frac{\sinh(2\phi) + \sin(2\phi)}{\cosh(2\phi) - \cos(2\phi)} \right) - 4f_h f_0 \frac{\sinh(\phi) \cos(\phi) + \cosh(\phi) \sin(\phi)}{\cosh(2\phi) - \cos(2\phi)} \right)$$

$$= \frac{\phi R_{dc}}{(N_t/m)^2} \left((f_h^2 + f_0^2) G_1(\phi) - 4f_h f_0 G_2(\phi) \right), \quad (14)$$

where N_t, m, f_h, f_0 are the total winding turns, the number of layers, and the magneto-motive forces (MMF) on both sides of the winding, respectively. R_{dc} is the dc resistance of the single-layer winding, expressed as $R_{dc} = \rho \frac{N_t \cdot MLT}{m i_{rms} t_{cu}}$, where MLT is the mean length per single turn. $\phi = t_{cu} / \delta$ with $\delta = \sqrt{2\pi \mu_0 f_{ac}}$ is the skin depth, where f_{ac} is the frequency of the ac excitation.



(a) Fully interleaved transformer



(b) Inductor

FIGURE 2. MMF profiles in multiple-layer magnetic components.

The total copper loss of the component is calculated by adding the copper loss of every layer, considering f_h and f_0 of each layer. In the case of the transformer, the total copper loss is dependent on the winding structure of the primary winding and the secondary winding; previous work [32] showed that the copper loss is minimized if the primary winding and the secondary winding are alternately placed layer by layer. This placement is called a fully interleaved placement. The MMFs, f_0 and f_h , for the fully interleaved wound transformer can be expressed as shown in Fig. 2a. In Fig. 2a, the MMF values of the primary winding and the secondary winding in a certain layer can be expressed as:

$$\begin{aligned} f_{0,pr} &= f_{h,sec} = 0, \\ f_{h,pr} &= f_{0,sec} = \frac{N_{t,pr} i_{rms,pr}}{m}, \end{aligned} \quad (15)$$

where $N_{t,pr}, i_{rms,pr}$ are the total turns and the RMS current value of the primary-side winding, respectively.

Equation (15) is satisfied if the MMF from the primary winding and the secondary winding are in opposite directions and therefore cancel each other. By substituting (15) into (14), the copper loss of the fully interleaved transformer by a single ac frequency can be presented as:

$$\begin{aligned} P_{layer, XF} &= \frac{\phi R_{dc, pri}}{(N_{t, pri} / m)^2} \left(\frac{N_{t, pri} i_{rms, pri}}{m} \right)^2 G_1(\phi) \\ &+ \frac{\phi R_{dc, sec}}{(N_{t, sec} / m)^2} \left(\frac{N_{t, sec} i_{rms, sec}}{m} \right)^2 G_1(\phi) \\ &= 2 \frac{\phi R_{dc, pri}}{(N_{t, pri} / m)^2} \left(\frac{N_{t, pri} i_{rms, pri}}{m} \right)^2 G_1(\phi), \end{aligned} \quad (16)$$

where $\frac{R_{dc, pri}}{R_{dc, sec}} = \left(\frac{N_{t, pri}}{N_{t, sec}} \right)^2$ is assumed. $N_{t, sec}, i_{rms, sec}$ are the total turns and the RMS current value of the secondary-side winding, respectively. The total copper loss of the transformer considering up to n_{th} harmonic current components can be calculated as:

$$\begin{aligned} P_{copper, XF} &= \sum_{j=1}^m \sum_{k=1}^n P_{layer, XF} \\ &= 2m R_{dc, pri} \sum_{k=1}^n \sqrt{k} \phi i_{rms, kth}^2 G_1(\sqrt{k} \phi) \end{aligned} \quad (17)$$

where $i_{rms, kth}$ is the RMS current value of the k^{th} harmonics component.

Different from the transformer, the MMF of a common inductor accumulates as additional layers are stacked, as illustrated in Fig. 2. The MMF values of the inductor by the j^{th} layer are expressed as:

$$\begin{aligned} f_0(j) &= (j-1) N_t i_{rms} / m \\ f_h(j) &= f_0(j+1) = j N_t i_{rms} / m. \end{aligned} \quad (18)$$

By substituting (18) into (14), the copper loss of the j^{th} layer by the fundamental frequency current can be expressed as follows:

$$\begin{aligned} P_{layer, IND}(j) &= \frac{\phi R_{dc}}{(N_t / m)^2} \left((f_h^2 + f_0^2) G_1(\phi) - 4f_h f_0 G_2(\phi) \right) \\ &= \phi R_{dc} i_{rms}^2 \left((j^2 + (j-1)^2) G_1(\phi) - 4j(j-1) G_2(\phi) \right). \end{aligned} \quad (19)$$

Similar to the transformer modeling, the total copper loss of the inductor, considering up to n_{th} harmonics, can be modeled from (19):

$$\begin{aligned} P_{copper, IND} &= \sum_{j=1}^m \sum_{k=1}^n \sqrt{k} \phi R_{dc} i_{rms, kth}^2 \\ &\times \left((j^2 + (j-1)^2) G_1(\sqrt{k} \phi) - 4j(j-1) G_2(\sqrt{k} \phi) \right) \end{aligned}$$

$$\begin{aligned}
 &= mR_{dc} \sum_{k=1}^n \sqrt{k} \phi i_{rms,kth}^2 \\
 &\times \left(G_1 (\sqrt{k} \phi) + \frac{2}{3} (m^2 - 1) (G_1 (\sqrt{k} \phi) - 2G_2 (\sqrt{k} \phi)) \right). \tag{20}
 \end{aligned}$$

Note that for the GP optimization, since G_1 and G_2 in the copper loss models, (17) and (20), are not posynomials as of function of ϕ , they should be approximated. The RMS harmonic current, i_{rms} , depends on the circuit topology and operation. An example fitting process is presented in Section IV.

C. COST MODELING

The component costs for a power conversion architecture can be abstracted by developing scalable models as functions of key performance metrics. For the power switches, by assuming that the semiconductor switch cost is proportional to the die area, the switch cost can be modeled as:

$$C_{semi} = \frac{k_{semi,cost}}{K_{SiC}} A_{die} = k_{semi,cost} \frac{V_{BD}^k}{R_{ds(on)}}. \tag{21}$$

Using the market data of the switch under consideration, the cost model coefficient, $k_{semi,cost}$, can be calculated.

For the magnetic components, in this study, it is assumed that their cost is determined by the core cost, and, based on this, the cost for the transformers and the inductors is modeled to be proportional to the core volume:

$$C_{core} = k_{core} V_{core} \tag{22}$$

where V_{core} is the relative core volume of the magnetic component, and k_{core} is the cost of the unit volume core.

IV. CASE STUDY: OPTIMIZATION ENGINE DEVELOPMENT USING GEOMETRIC PROGRAMMING FOR DIRECT LOW-VOLTAGE DC TO MEDIUM-VOLTAGE AC PV POWER CONVERSION SYSTEM

In this section, an optimization case study for a cascaded modular PV inverter architecture is presented. Fig. 3 shows the system block diagram under this study using *circuit + control*, (C^2), modules. The C^2 architecture features cascaded modular power conversion with stacked converter modules to directly generate medium-voltage ac output without grid frequency (50/60-Hz) step-up transformers from low-voltage dc input, i.e., < 1500 V. Each C^2 module is connected to a PV string, and the PV dc power is transformed to the three-phase ac driven by a quadruple active bridge (QAB) with high-frequency transformers followed by three full-bridge inverters for individual phases, as illustrated in Fig. 3. The QAB stage operates as a dc transformer (DCX) with a fixed conversion ratio to improve the efficiency. The three-phase outputs of the modules are connected in series with interleaved pulse-width modulation (PWM) signals to synthesize the multilevel medium-voltage output. Further details of the power conversion can be found in [33].

A. SYSTEM MODELING

Based on the circuit and system operation, the LCOE improvement that the C^2 system can achieve, compared to a conventional PV generation architecture, can be modeled as follows. The modeling approach considers major components in power conversion, including the QAB primary switches (4ea/module), QAB secondary switches (12ea/module), inverter switches (12ea/module), high-frequency transformers (3ea/module), and QAB leakage inductor (3ea/module). To represent the system characteristics for the LCOE-oriented optimization, the system modeling should incorporate the loss and cost mechanism of the individual components. As presented in Section III, the loss functions, P , and the cost functions, C , for the C^2 system can be defined as:

$$\begin{aligned}
 P_{QAB,C^2} &= f_1 (N_{module}, N_t, X_F, m_{XF}, R_{ds(on),pri}, \\
 &\quad R_{ds(on),sec}, f_{sw,QAB}) \\
 P_{INV,C^2} &= f_2 (N_{module}, N_t, X_F, m_{XF}, R_{ds(on),INV}, f_{sw,INV}) \\
 P_{XF,C^2} &= f_3 (N_{module}, N_t, X_F, m_{XF}, V_{core,XF}, \\
 &\quad f_{sw,QAB}, t_w, X_F, t_{cu,XF}) \\
 P_{IND,C^2} &= f_4 (N_{module}, V_{core,IND}, f_{sw,QAB}, N_t, IND, \\
 &\quad m_{IND}, t_w, IND, t_{cu,IND}) \\
 C_{semi,QAB} &= f_5 (N_{module}, N_t, X_F, m_{XF}, R_{ds(on),pri}, R_{ds(on),sec}) \\
 C_{semi,INV} &= f_6 (N_{module}, N_t, X_F, m_{XF}, R_{ds(on),INV}) \\
 C_{CORE,C^2} &= f_7 (N_{module}, V_{core,XF}, V_{core,IND}), \tag{23}
 \end{aligned}$$

where N_{module} , $R_{ds(on),pri}$, $R_{ds(on),sec}$, $R_{ds(on),INV}$, $f_{sw,QAB}$, $f_{sw,INV}$, $V_{core,XF}$, and $V_{core,IND}$ are the number of modules, the on-state resistance of the primary-side switch, the secondary-side switch, the inverter switch, the switching frequency of the QAB, the switching frequency of the inverter, and the core volume of the transformer and inductor, respectively. The magnetic component variables, N_t , m , t_w , and t_{cu} , are the geometric parameters of the transformer and inductor, representing the number of turns, number of layers, and the winding width and winding thickness of the transformer and inductor, respectively. Here, in the modeling process, the power and voltage ratings of the cascaded modules in the target system are assumed to be identical. This assumption is based on the common practice found in the field, mostly for controllability, scalability with standardized modules, and cost-effectiveness in commercialization and mass production. Similar approaches in modular power conversion systems are found in [34], [35]. The function models, f_1, \dots, f_7 , in (23) will be represented in posynomial form, with respect to the design variables, to perform the GP optimization.

Fig. 4 shows the relationship of the optimization variables and the model functions of the C^2 system. The system efficiency and the total installation cost are calculated from (23) as:

$$\begin{aligned}
 \eta_{new} &= 1 - \frac{P_{loss,C^2}}{P_{rated}} \\
 &= 1 - \frac{N_{module}}{P_{rated}} (P_{QAB,C^2} + P_{INV,C^2} \\
 &\quad + P_{XF,C^2} + P_{IND,C^2}), \tag{24}
 \end{aligned}$$

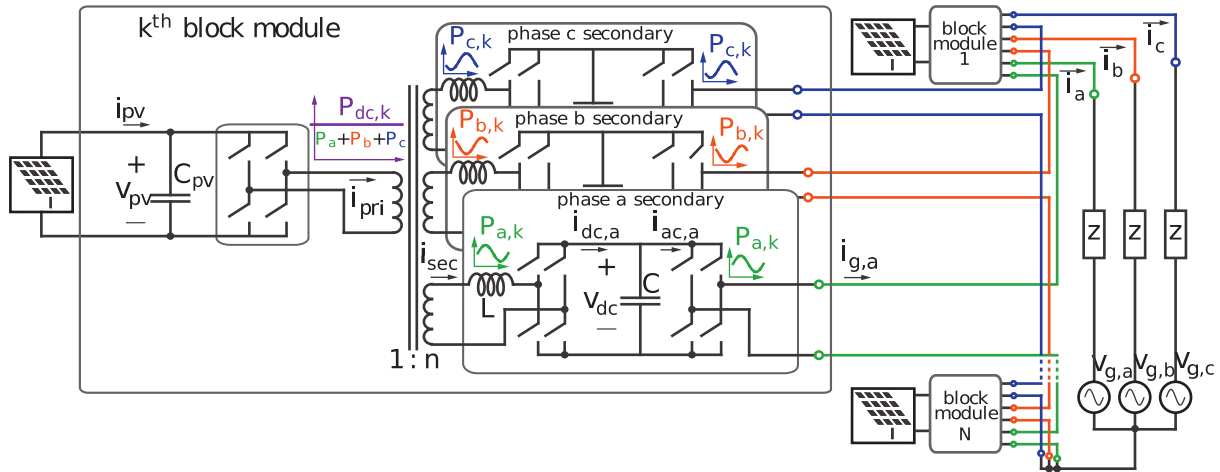


FIGURE 3. Cascaded modular PV inverter architecture for case study using C^2 building blocks [33].

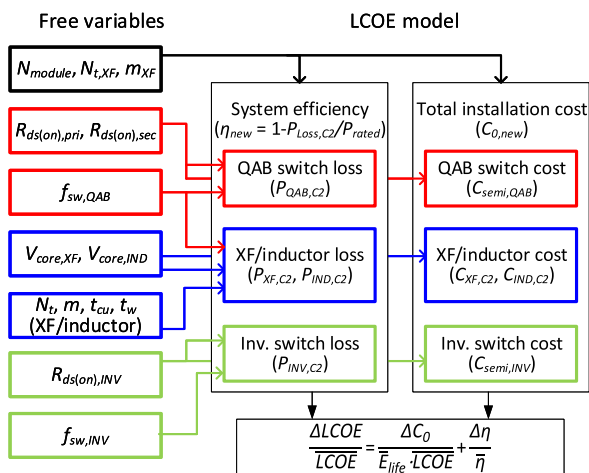


FIGURE 4. Block diagram of C^2 topology LCOE calculation model.

and:

$$C_{0,new} = N_{module}(C_{semi,QAB} + C_{semi,INV} + C_{XF,C2} + C_{IND,C2}). \quad (25)$$

The LCOE improvement factor of the C^2 system can be calculated by substituting the calculated values in (24) and (25) and the LCOE, E_{life} , η , C_0 , values for the conventional one into (7). The modeling process of each loss and the cost model (23) is explained in the following.

1) SWITCH LOSS MODELING

First, the switch loss model for the C^2 system, $P_{QAB,C2}$ and $P_{INV,C2}$, are presented. The power loss of the QAB switches, $P_{QAB,C2}$, can be expressed as:

$$\begin{aligned} P_{QAB,C2} &= P_{cond,QAB} + P_{sw,QAB} \\ &= \left(4i_{rms,pri}^2 R_{ds(on),pri} + 12i_{rms,sec}^2 R_{ds(on),sec} \right) \\ &\quad + 12 \left(2kV_{dc}^2 C_{oss,sec} f_{sw,QAB} \right), \end{aligned} \quad (26)$$

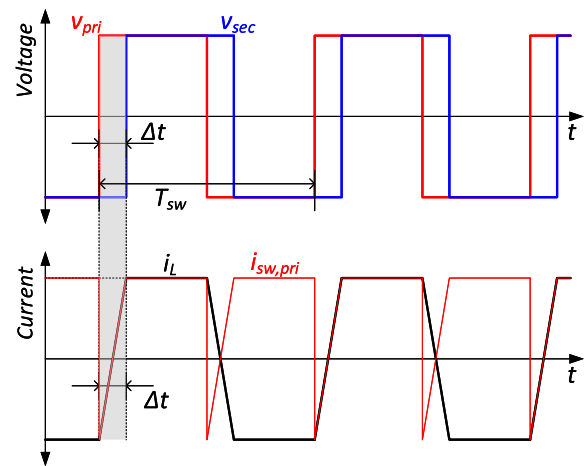


FIGURE 5. Voltage and current waveforms of QAB in C^2 module.

where $i_{rms,pri}$ and $i_{rms,sec}$ are the RMS current of the primary-side switches and secondary-side switches of the QAB, respectively. Fig. 5 shows the voltage and current waveform of the QAB in the C^2 topology. Variables, v_{pri} , v_{sec} , i_L , $i_{sw,pri}$, Δt , T_{sw} are the primary-side voltage, secondary-side voltage, inductor current, primary-side switch current, time delay between the primary and secondary voltage, and the switching period of the QAB, respectively. In the QAB, a phase difference between v_{pri} and v_{sec} allows the electrical power to be delivered to the secondary side. The RMS value of $i_{sw,pri}$ is represented as follows [33]:

$$\begin{aligned} i_{rms,pri} &\approx \frac{i_{pv}}{1 - \frac{\phi_{max}}{\pi}} \sqrt{\frac{1}{2} - \frac{\phi_{max}}{3\pi}} \\ &= \frac{P_{rated}}{N_{module} v_{pv}} \frac{1}{1 - \frac{\phi_{max}}{\pi}} \sqrt{\frac{1}{2} - \frac{\phi_{max}}{3\pi}} \end{aligned} \quad (27)$$

where $\phi_{max} = \Delta t / T_{sw}$ is the phase shift between the primary-side voltage and the secondary-side voltage at the rated

power, which is set as $\pi/6$ for practicality. v_{pv}, i_{pv} are the voltage and current from the PV panel connected to the QAB primary side. As discussed, the QAB has three secondary-side bridges to output three-phase ac, and the secondary-side current, $i_{sw,sec}$, contains the line frequency component. The RMS value of $i_{sw,sec}$ considering the line frequency component can be expressed as:

$$i_{rms,sec} \approx \frac{v_{dc}\phi_{max}}{2\pi f_{sw,QAB}L_{lk}} \sqrt{\frac{1}{4} - \frac{4\phi_{max}}{9\pi^2}}, \quad (28)$$

where L_{lk} is the designed leakage inductance of the QAB for the rated power at $\phi = \phi_{max}$. v_{dc} is the dc-link voltage at the QAB secondary side and the inverter input, which can be calculated as:

$$v_{dc} = m_{INV} \frac{v_{g,pk}}{N_{module}} = n_{TR} v_{pv} \quad (29)$$

where m_{INV} is the output voltage margin of the inverter, $v_{g,pk}$ is the peak phase voltage of the grid, and $n_{TR} = N_{l,pri}/N_{l,sec}$ is the turns ratio of the QAB transformer. Substituting (27), (28), and (29) into (26), the QAB switch loss model can be represented as the posynomial function form with respect to variables N_{module} , $R_{ds(on),pri}$, $R_{ds(on),sec}$, and $f_{sw,QAB}$.

The switching loss of the QAB switches can be modeled by incorporating the degree of soft switching achieved over an ac line cycle and the other switching losses. Using a current source(s), e.g., leakage inductance or magnetizing inductance, the QAB can be designed to achieve zero-voltage switching (ZVS) to mitigate the turn-on switching loss, which is the major loss component of majority carrier switches, such as SiC MOSFETs under this study. Since the QAB delivers ac power, fluctuating at double-line frequency (100 or 120 Hz), the ZVS condition may depend on the line cycle and the source of soft switching. The QAB primary-side switches can straightforwardly obtain the full ZVS, independent of the line cycle, since the sum of the three individual ac phase currents flowing through the primary side is kept constant. The secondary-side switches can also achieve the ZVS by securing enough inductive current and PWM dead time over the entire line cycle, e.g., having moderate magnetizing inductance current that remains constant to discharge parasitic device capacitances, independent of line cycle. Further discussion on the soft switching techniques for the QAB can be found in [36].

With the QAB designed to achieve the full ZVS, the other switching losses remaining should be incorporated into the switch model to result in a reasonable design optimization. To represent the inevitable switching losses, including MOSFET gate drive loss and turn-off loss, the switching-loss factor, k , in (26), is set to 0.1 in this study.

The loss model of the inverters is expressed as:

$$\begin{aligned} P_{INV,C2} &= P_{cond,INV} + P_{sw,INV} \\ &= 12i_{rms,INV}^2 R_{ds(on),INV} \\ &\quad + 12 \left(2v_{dc}^2 C_{oss,sec} f_{sw,INV} \right). \end{aligned} \quad (30)$$

Here, the single-phase inverters of the C^2 architecture are implemented with full-bridge inverters operating in the bipolar modulation and hard switching; no soft-switching technique is employed. In this case, the RMS current of the inverter switches, $i_{rms,INV}$, considering the switching ripple can be expressed as follows [37]:

$$\begin{aligned} i_{rms,INV} &= \sqrt{i_{rms,g}^2 + i_{rms,ripple}^2} \\ &= \sqrt{\left(\frac{P_{rated}}{3v_{g,rms}} \right)^2 + \frac{1}{3} \left(1 - m_a^2 + \frac{3}{8}m_a^4 \right)} \\ &\quad \times \sqrt{\left(\frac{v_{dc}}{2(N_{module}f_{sw,INV})(N_{module}L_{INV})} \right)^2} \end{aligned} \quad (31)$$

As in the QAB case, the inverter switch loss model can also be expressed in posynomial form with respect to N_{module} , $f_{sw,INV}$, and $R_{ds(on),INV}$ by substituting (29) and (31) into (30). Here, an additional constraint is required to ensure that the switching ripple current of the inverter stays below the limit. Equation (32) shows the inequality constraint regarding this limit. It is a posynomial form with respect to variables N_{module} and $f_{sw,INV}$.

$$i_{ripple,pk} = \frac{v_{dc}}{2(N_{module}f_{sw,INV})(L_{INV})} \leq i_{ripple,lim} \quad (32)$$

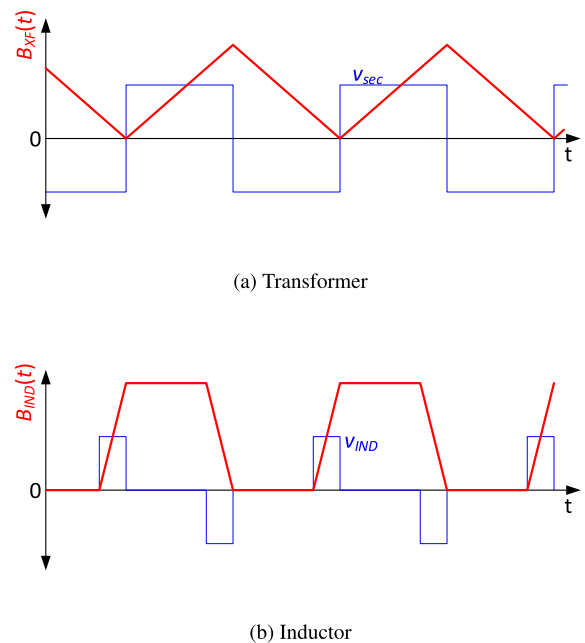


FIGURE 6. Flux density, $B(t)$, for magnetic components in the QAB.

2) MAGNETIC COMPONENT LOSS MODELING

The loss of the magnetic components in the C^2 system occurs at the inductors and transformers in the QAB. In general, the magnetic loss can be divided into core loss and copper loss. The core loss can be presented in posynomial forms as

functions of the design variables, $V_{core, XF}$, $V_{core, IND}$, $N_{t, XF}$, $N_{t, IND}$, and $f_{sw, QAB}$. Fig. 6 shows the flux density waveforms, $B(t)$, for the transformers and the inductors in the QAB, which can be expressed as:

$$B_{XF}(t) = \frac{v_{XF}}{N_t A_w} = \begin{cases} \frac{v_{pv} t}{N_{t, XF} A_{Base} V_{core, XF}^{2/3}} & (0 \leq t \leq 0.5T_{sw, QAB}) \\ \frac{v_{pv} (T_{sw, QAB} - t)}{N_{t, XF} A_{Base} V_{core, XF}^{2/3}} & (0.5T_{sw, QAB} \leq t \leq T_{sw, QAB}) \end{cases} \quad (33)$$

$$B_{IND}(t) = \frac{v_{IND}}{N_t A_w} = \begin{cases} \frac{v_{pv} t}{N_{t, IND} A_{Base} V_{core, IND}^{2/3}} & (0 \leq t \leq \Delta t) \\ \frac{v_{pv} \Delta t}{N_{t, IND} A_{Base} V_{core, IND}^{2/3}} & (\Delta t \leq t \leq 0.5T_{sw, QAB}) \\ \frac{v_{pv} (0.5T_{sw, QAB} + \Delta t - t)}{N_{t, IND} A_{Base} V_{core, IND}^{2/3}} & (0.5T_{sw, QAB} \leq t \leq 0.5T_{sw, QAB} + \Delta t) \\ 0 & (otherwise) \end{cases} \quad (34)$$

where $T_{sw, QAB} = 1/f_{sw, QAB}$ is the switching period of the QAB; v_{XF} and v_{IND} are the voltages applied to the transformer and the inductor; N_t and A_w are the number of turns and the cross-sectional area of the surroundings by turns; v_{pv} is the panel voltage; and A_{Base} is the cross-sectional area of the unit volume core. By substituting (33) and (34) into (13), the core loss of the components in the QAB can be presented as:

$$P_{core, XF} = V_{core, XF} \frac{1}{T_{sw}} \frac{K_{fe}}{2\pi^\alpha 2^{\beta-\alpha}} \times 2 \left(\frac{v_{pv}}{N_{t, XF} A_{Base} V_{core, XF}^{2/3}} \right)^\beta \frac{(T_{sw}/2)^{\beta-\alpha+1}}{\beta-\alpha+1}$$

$$P_{core, IND} = V_{core, IND} \frac{1}{T_{sw}} \frac{K_{fe}}{2\pi^\alpha 2^{\beta-\alpha}} \times 2 \left(\frac{v_{pv}}{N_{t, IND} A_{Base} V_{core, IND}^{2/3}} \right)^\beta \frac{(\Delta t)^{\beta-\alpha+1}}{\beta-\alpha+1}. \quad (35)$$

In addition, the saturation of the core should be considered. Here, the peak value of the flux density should be kept under the limit, B_{max} , to avoid the core saturation. Constraints related to the saturation can be expressed as:

$$B_{XF, pk} = \frac{0.5v_{pv} T_{sw, QAB}}{N_{t, XF} A_{Base} V_{core, XF}^{2/3}} \leq B_{max}$$

$$B_{IND, pk} = \frac{v_{pv} \Delta t}{N_{t, IND} A_{Base} V_{core, IND}^{2/3}} \leq B_{max} \quad (36)$$

where $B_{XF, pk}$ and $B_{IND, pk}$ are the peak values of flux density, $B_{XF}(t)$ and $B_{IND}(t)$, respectively. As shown, these constraints are in monomial form to the design variables; they can be applied to the GP optimization without modification.

In contrast to the core loss model, the native copper loss model is not in posynomial form to the variables $V_{core, XF}$, $V_{core, IND}$, and $f_{sw, QAB}$; therefore, the posynomial fitting to the total copper loss is required so that the loss model can be applied to the GP optimization.

To derive the copper losses of the QAB inductors and transformers, the RMS values of the harmonic current components can be expressed, referring to the illustration in Fig. 5, by using the Taylor series:

$$i_{rms, pri} = i_{L, pk} \sum_{k=1}^n \frac{2\sqrt{2} \sin(k\alpha\pi)}{\alpha(k\pi)^2}. \quad (37)$$

Substituting (37) into (17), the total copper loss of the transformer can be expressed as:

$$P_{copper, XF} = 2mR_{dc, pri} i_{L, pk}^2 \sum_{k=1}^n \sqrt{k} \phi \left(\frac{2\sqrt{2} \sin(k\alpha\pi)}{\alpha(k\pi)^2} \right)^2 \times \left(\frac{\sinh(2\sqrt{k}\phi) + \sin(2\sqrt{k}\phi)}{\cosh(2\sqrt{k}\phi) - \cos(2\sqrt{k}\phi)} \right) = 2mR_{dc, pri} i_{L, pk}^2 F_{ac, XF}(\phi). \quad (38)$$

By fitting $F_{ac, XF}$ to posynomial form with respect to $\phi = t_{cu}/\delta$, the total copper loss can be modeled as posynomial with respect to t_{cu} and $f_{sw, QAB}$. In the same manner, the total copper loss of the inductor is:

$$P_{copper, IND} = R_{dc} i_{L, pk}^2 \sum_{k=1}^n m \sqrt{k} \phi \left(\frac{2\sqrt{2} \sin(k\alpha\pi)}{\alpha(k\pi)^2} \right)^2 \times \left(G_1 \sqrt{k} \phi + \frac{2}{3} (m^2 - 1) (G_1(\sqrt{k}\phi) - 2G_2(\sqrt{k}\phi)) \right) = R_{dc} i_{L, pk}^2 F_{ac, IND}(m, \phi). \quad (39)$$

Fig. 7a and 7b show the plots of the non-posynomial terms, $F_{ac, XF}$ and $F_{ac, IND}$, with respect to ϕ .

Next, the posynomial fitting process of $F_{ac, XF}$ and $F_{ac, IND}$ is presented. Posynomial functions should have convex or affine characteristics; however, as shown in Figs. 7a and 7b, $F_{ac, XF}$ and $F_{ac, IND}$ have a concave shape starting from $\phi \approx 2.2$, and this area aggravates the fitting error. In this case, higher fitting accuracy can be obtained by dividing the original function into several clusters and performing fitting to each cluster. In this case study, $F_{ac, XF}$ is divided into two clusters at $\phi = 2.2$, and $F_{ac, IND}$ is divided into three clusters at $\phi = 1$ and $\phi = 2$. Figs. 8 and 9 show the fitting result to $F_{ac, XF}$ and $F_{ac, IND}$, with and without clustering. The posynomial functions for the copper loss factors

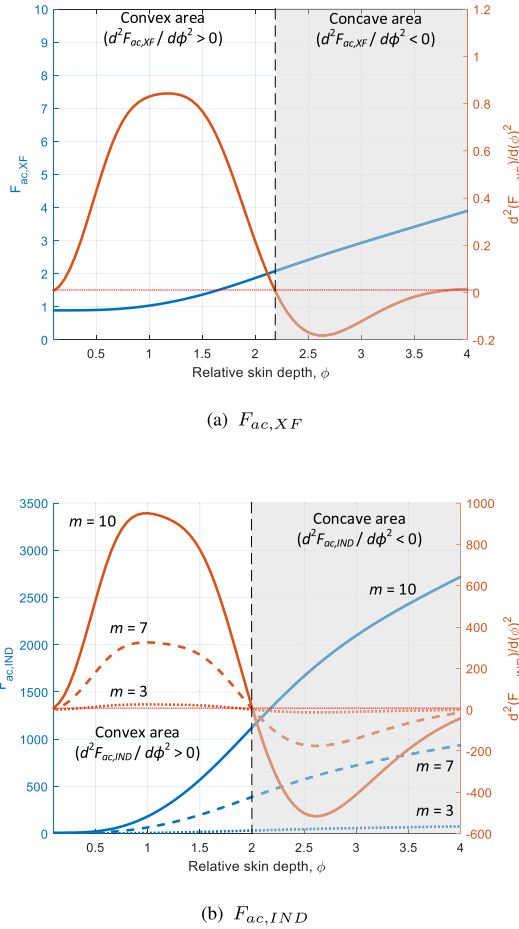


FIGURE 7. Copper loss factors for posynomial fitting as functions of ϕ .

from the fitting are:

$$F_{ac, XF}(\phi) = \begin{cases} 0.2698\phi^{-0.3268} + 0.9901\phi^{-0.0403} \\ + 0.5965\phi^{0.3398} + 0.6940\phi^{2.486} \\ + 0.3732\phi^{-0.0293} + 1.2633 & (0 < \phi \leq 2.2) \\ 0.2368\phi^{0.8182} + 0.7054\phi^{-0.6689} \\ + 0.9176\phi^{0.9266} + 1.1906\phi^{0.9569} \\ + 1.2674\phi^{1.1699} + 0.0591 & (\phi \geq 2.2) \end{cases} \quad (40)$$

$$F_{ac, IND}(m, \phi) = \begin{cases} 0.8725m^{0.9837}\phi^{-0.0186} \\ + 0.1851m^{2.9890}\phi^{3.5105} \\ 0.1933m^{2.988}\phi^{2.6327} & (0 < \phi \leq 1) \\ + 0.8516m^{0.9192}\phi^{-0.1813} \\ + 0.0011m^{-64.8504}\phi^{-4.0907} \\ 0.5351m^{2.9854}\phi^{1.229} & (1 < \phi \leq 2) \\ + 0.8312m^{-30.4309}\phi^{-26.4924} \\ + 0.3447m^{0.9749}\phi^{0.6964} + 0.0441 & (\phi \geq 2) \end{cases} \quad (41)$$

This clustering technique is distinguished from the commonly used max-monomial fitting method [27] or the softmax-posynomial fitting method [38]. Fig. 10 illustrates the difference between the methods. The conventional clustering method reported in [27] and [38] combines the fitting results of each cluster into a single fitting function. It is proven to work well when fitting into a convex function but not in a concave function case. The proposed clustering separates the original functions into several convex functions and solves each optimization problem with separate functions. This technique, as a result, has an optimization performance trade-off between model accuracy and computation time since more clusters require additional computation for solving subproblems.

There are constraints for the transformer/inductor practical design. First, the number of layers, m_{XF} and m_{IND} , and the number of turns per layer, $N_{t, XF}/m_{XF}$ and $N_{t, IND}/m_{IND}$, should be integer. The entire width and thickness of the winding should also be less than the width and thickness of the winding area of the core so that all windings can be placed within the core. Equation (42) shows the expressions of the geometric constraints:

$$\begin{aligned} W_{winding, XF} &= \frac{N_{t, XF}}{m_{XF}} (T_{w, XF} + T_{w, sp, XF}) \\ &\leq W_{core, XF} = W_{Base} V_{core, XF}^{1/3} \\ W_{winding, IND} &= \frac{N_{t, IND}}{m_{IND}} (T_{w, IND} + T_{w, sp, IND}) \\ &\leq W_{core, IND} = W_{Base} V_{core, IND}^{1/3} \\ Th_{winding, XF} &= m_{XF} (T_{cu, XF} + T_{cu, sp, XF}) \\ &\leq W_{core, XF} = Th_{Base} V_{core, XF}^{1/3} \\ Th_{winding, IND} &= m_{IND} (T_{cu, IND} + T_{cu, sp, IND}) \\ &\leq W_{core, IND} = Th_{Base} V_{core, IND}^{1/3}, \end{aligned} \quad (42)$$

where $W_{winding, XF}$ and $W_{winding, IND}$ are the width of the transformer and inductor winding; $Th_{winding, XF}$ and $Th_{winding, IND}$ are the thickness of the transformer and inductor winding; and W_{Base} and Th_{Base} are the width and thickness of the unit volume core, respectively. The spaces between the windings, $T_{w, sp}$ and $T_{cu, sp}$, are predetermined by considering the isolation voltage level and size limit. In this case study, It is assumed that $T_{w, sp} = 1$ mm and $T_{cu, sp} = 0.254$ mm.

3) COST MODELING

The cost models of the C^2 system components, $C_{semi, QAB}$, $C_{semi, INV}$, $C_{core, XF}$, and $C_{core, IND}$ can be expressed as:

$$\begin{aligned} C_{semi, QAB} &= 4C_{semi, pri} + 12C_{semi, sec} \\ &= k_{semi, cost} \left(4 \frac{V_{BD, pri}^k}{R_{ds(on), pri}} + 12 \frac{V_{BD, sec}^k}{R_{ds(on), sec}} \right) \\ C_{semi, INV} &= 12C_{semi, INV} \\ &= 12k_{semi, cost} \left(\frac{V_{BD, sec}^k}{R_{ds(on), INV}} \right) \end{aligned}$$

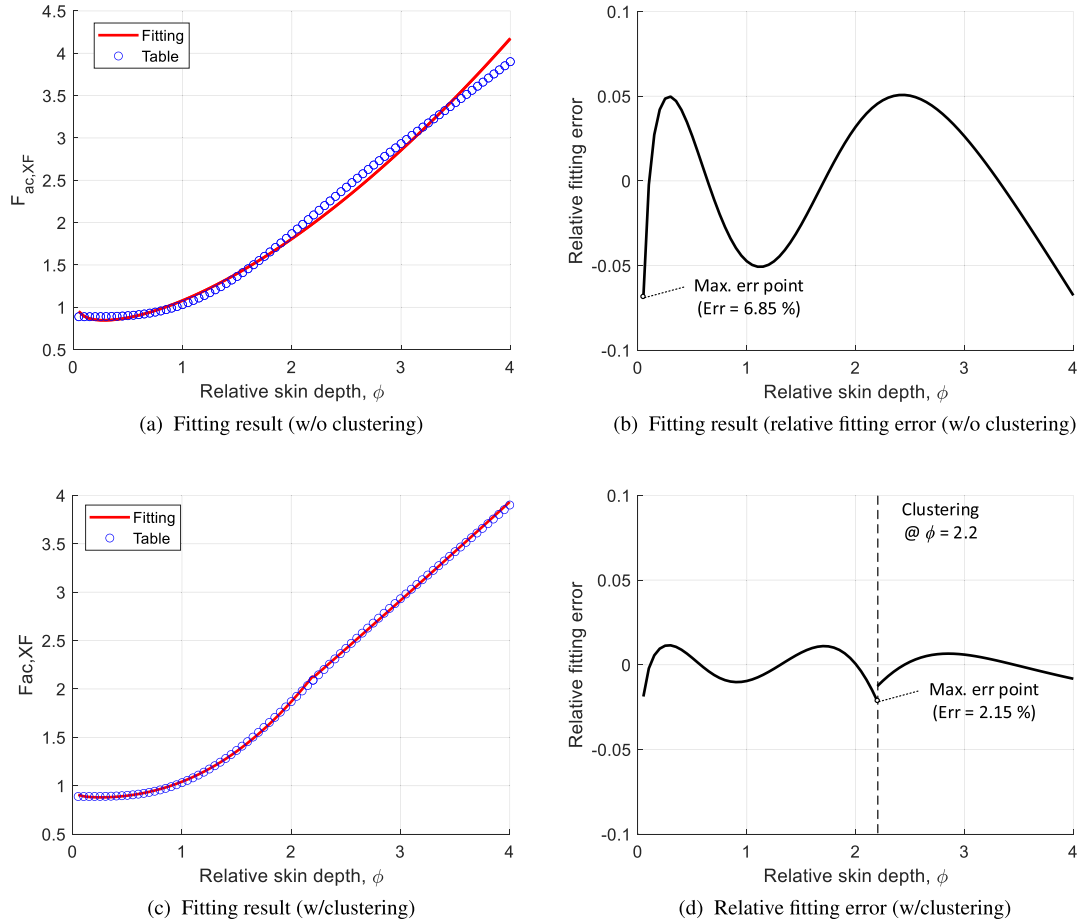


FIGURE 8. Posynomial fitting for transformer copper loss factor, $F_{ac, XF}$, with and without clustering.

$$\begin{aligned} C_{core, XF} &= 3k_{core}V_{core, XF} \\ C_{core, IND} &= 3k_{core}V_{core, IND}. \end{aligned} \quad (43)$$

As shown, the cost model functions have posynomial forms with respect to the design variables, $R_{ds(on)}$ and V_{core} , directly applicable for the GP optimization. The model equations are based on two assumptions: i) The same SiC switch technology (latest CREE SiC devices in this study) is used for the QAB and the inverters, scalable with the key parameters, i.e., voltage rating and on-resistance; and ii) the same magnetic core material in the same geometry (EE cores from TDK in this study) is used in the transformers and the inductors, scalable with core volume. It makes the optimization problem more tractable and provide system-level insights. In case different types of semiconductor switches or cores are used, they can be reflected by modifying coefficients $k_{semi, cost}$ and k_{core} in the cost model.

4) GP OPTIMIZATION MODEL

The final GP optimization form for the C^2 system design is expressed as follows:

$$\text{maximize } \frac{\Delta LCOE}{LCOE}$$

$$\begin{aligned} \text{subject to } & B_{XF, pk} \leq B_{max} \\ & B_{IND, pk} \leq B_{max} \\ & i_{ripple, INV} \leq i_{ripple, max} \\ & W_{winding, XF} \leq W_{core, XF} \\ & W_{winding, IND} \leq W_{core, IND} \\ & Th_{winding, XF} \leq Th_{core, XF} \\ & Th_{winding, IND} \leq Th_{core, IND}. \end{aligned} \quad (44)$$

In the optimization model (44), five design variables, N_{module} , $N_{t, XF}$, m_{XF} , $N_{t, IND}$, and m_{IND} , are integer values in practice. As a result, it is an MIGP problem, requiring a certain algorithm for optimization. In this case study, a heuristic method is chosen to obtain a lower computation time. Fig. 11 shows the flowchart of the heuristic algorithm used. In Step I, the five integer variables in (44) are relaxed as noninteger, and we obtain the temporary optimal points by solving the relaxed GP problems. As shown in (40) and (41), ϕ is clustered in a copper loss model fitting. The number of optimization problems generated is equal to the number of clusters in the copper loss fitting, and the solution can be obtained by solving each problem and selecting the solution that maximizes the LCOE improvement factor among them. In this case study, there are

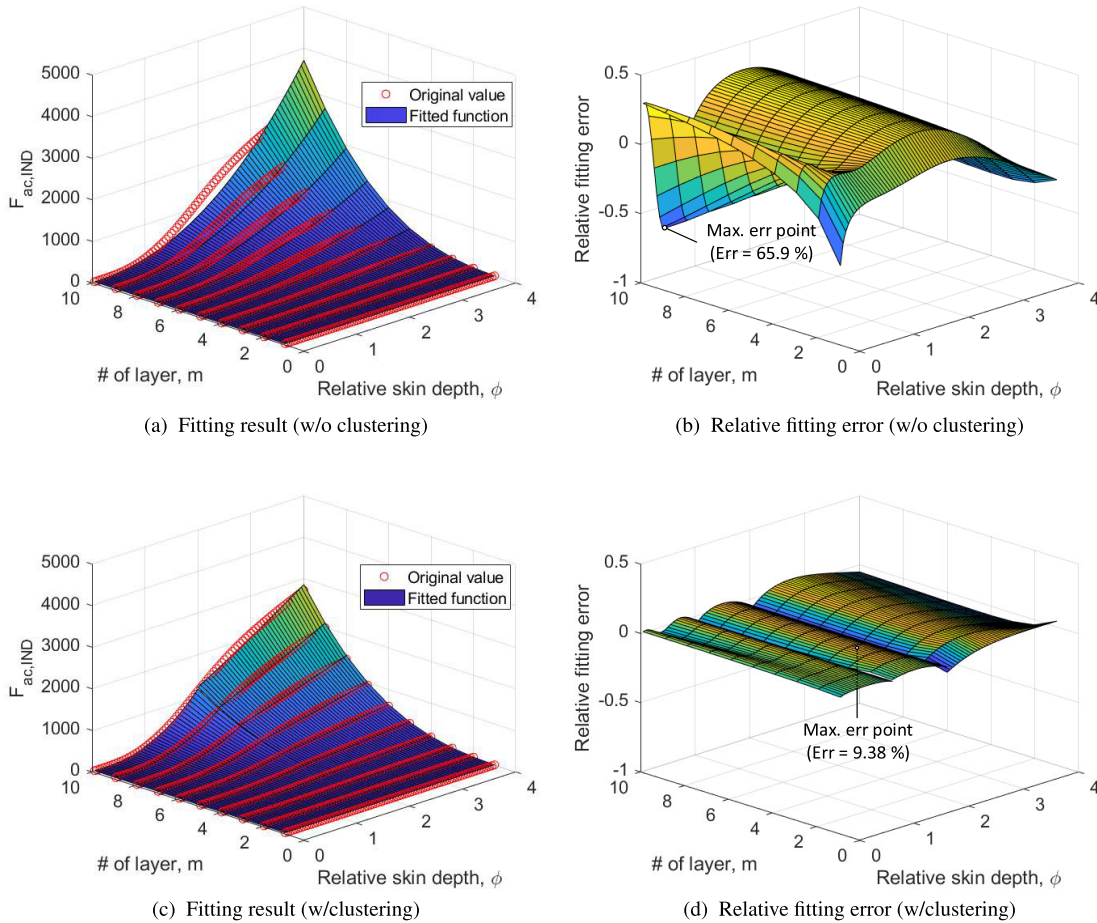


FIGURE 9. Posynomial fitting for inductor copper loss factor, $F_{ac,IND}$, with and without clustering.

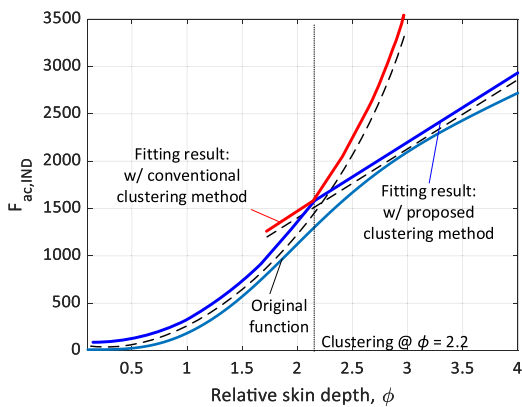


FIGURE 10. Comparison of posynomial fitting methods.

six subproblems from the clustering, $2 \cdot 3$, two options in the transformer loss fitting, three options in the inductor fitting.

In the next steps, as shown in Fig. 11, relaxed variables are fixed to certain integer values to satisfy the practical design limitation. In Step II, the number of modules, N_{module} , and the number of turns per layer, $N_{t, XF}/m_{XF}$, are rounded to

the integer values. First, two candidates of integer N_{module} are selected, which are the floor and ceiling values of the value from Step I. Next, $N_{t, XF}/m_{XF}$ is rounded to maintain the turns ratio of the transformer $n_{TR} = N_{t, sec}/N_{t, XF}$ at its optimal value from Step I. As shown in (29), the transformer turns ratio determines the dc-link voltage and thus the switch voltage ratings required. Consequently, it would determine the switching loss and cost of the switches. According to (21), the cost of the switches exponentially scale with the dc-link voltage, so the design with a low dc-link voltage in a certain range tends to outperform in the LCOE; therefore, with the deviation of n_{TR} from the value in Step I limited, the degradation in the iterated LCOE improvement in Step II can be minimized. In addition, the number of turns per layer of the transformer should be integer values—both the primary side, $N_{t, XF}/m_{XF}$, and the secondary side, $N_{t, sec}/m_{XF}$. Fig. 12 shows the potential design choices of the number of primary and secondary turns per layer of the transformer. As shown, $N_{t, XF}/m_{XF}$ and $N_{t, sec}/m_{XF}$ are selected under the three design criteria:

- $n_{TR, min} \leq N_{t, sec}/N_{t, pri} \leq n_{TR, max}$
- $|N_{t, sec}/N_{t, pri} - n_{TR, StepI}|$ should be minimized.

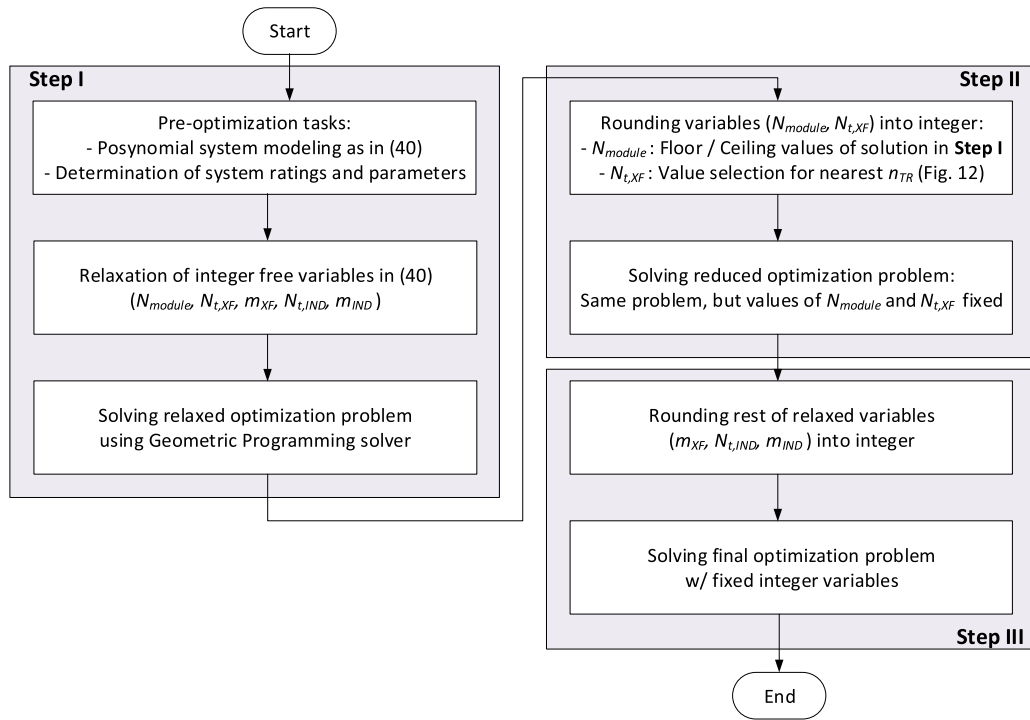
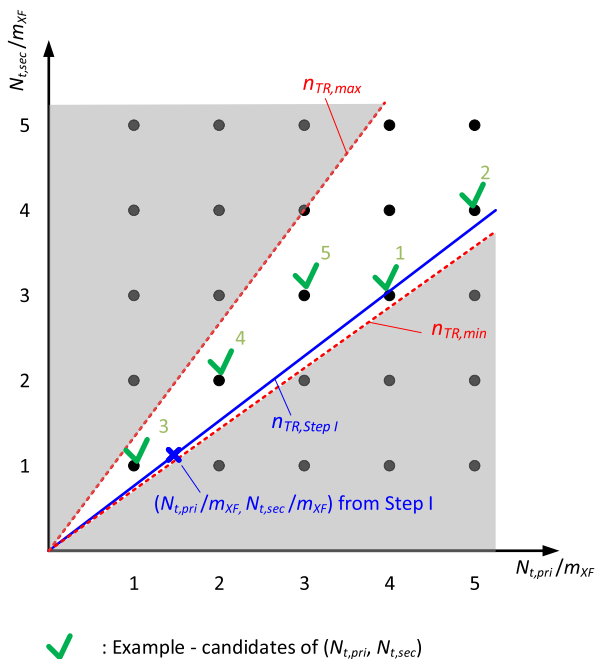


FIGURE 11. Flowchart of the proposed optimization method with two integer variable iteration processes to identify practical optimal design values.



✓ : Example - candidates of $(N_{t,pri}, N_{t,sec})$

FIGURE 12. Rounding of $N_{t,XF}$ into integers: selection of candidates.

- Among the $(N_{t,XF}/m_{XF}, N_{t,sec}/m_{XF})$ pairs with same $N_{t,sec}/N_{t,pri}$, the pairs with a smaller number of turns should be selected for less copper loss.

The maximum and the minimum of the turns ratio, $n_{TR,min}$ and $n_{TR,max}$, can be expressed as:

$$n_{TR,max} = \frac{v_{BV,max}}{m_{BV} v_{pv}},$$

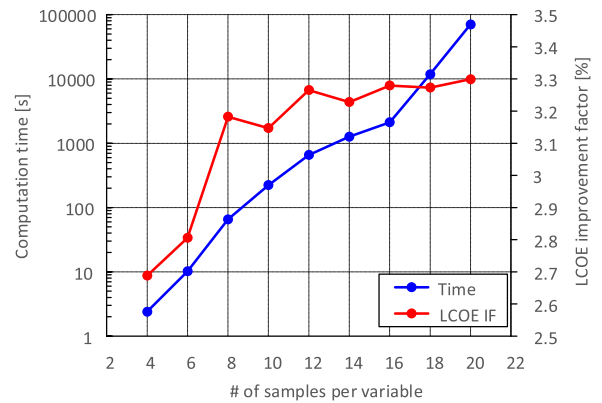


FIGURE 13. Computation time and maximum LCOE improvement factor found as a function of the number of samples per variable by using the exhaustive algorithm. Computation time exponentially increases with improvement saturation.

$$n_{TR,min} = \frac{v_{g,pk}}{N_{module} m_{INV} v_{pv}}, \quad (45)$$

where $v_{BV,max}$, m_{BV} , and m_{INV} are the maximum switch voltage rating available, the boundary voltage margin for the semiconductor switch, and the output voltage margin of the inverter. Having boundaries avoids significant variation of the turns ratio iterated in Step II that may result from rounding of $N_{t,XF}/m_{XF}$ and $N_{t,sec}/m_{XF}$. Five design candidates selected from the criteria, as an example, are illustrated in Fig. 12. At the final stage of Step II, the optimization engine reruns the selected cases; as a result, it runs multiple times but with reduced free variables; the two design variables, N_{module} and $N_{t,XF}/m_{t,XF}$, are predetermined. Among multiple

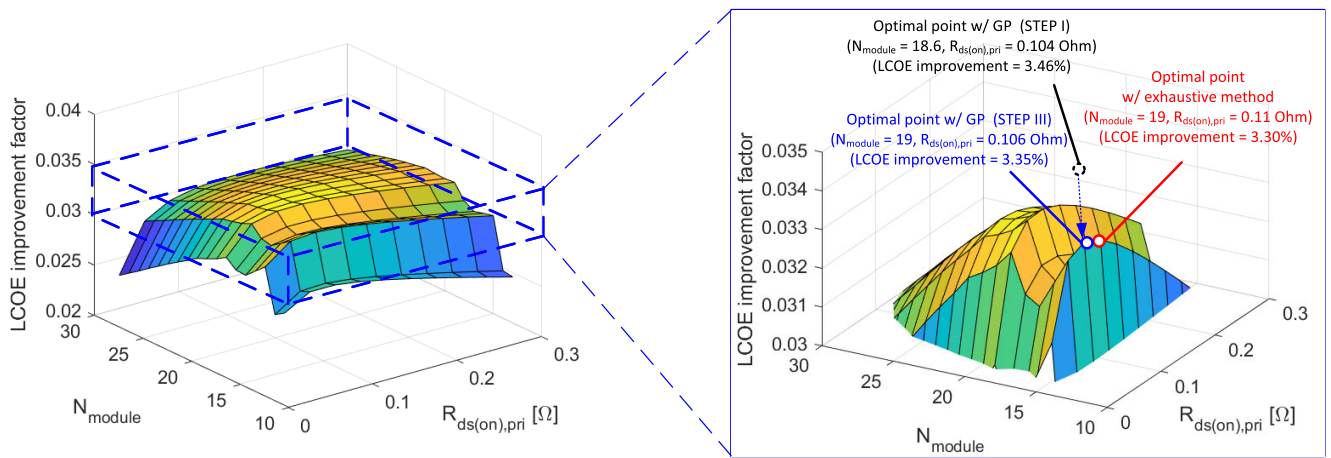


FIGURE 14. Final design point from the GP optimization overlaid on the design surface generated from the original models. The initial result (Step I) is iterated to the final design (Step III) with practical design values.

TABLE 1. System parameters used in optimization.

System ratings	
Parameter	Rated value
P_{rated}	200 kW
V_{grid}	13.2 kV
V_{pv}	1000 V
Parameters of benchmark system	
Parameter	Value
$LCOE$	6 Cents/kWh
η_{bench}	0.97
c_t	0.24
\bar{C}_0	16,536 US Dollars

optimal designs identified in Step II, the one with the maximum LCOE improvement is selected.

In Step III, first, the other integer variables are finalized; m_{XF} , N_{IND} , and m_{IND} are rounded from the noninteger values identified in Step II. These variables are rounded to the nearest integer values. The last integer variable left, N_{XF} , is determined, as m_{XF} is rounded accordingly. With optimal design values practical for the integer variables identified and fixed, the final optimal design is derived from the GP optimization to finalize the other design variables for the maximum LCOE improvement.

The system parameter values given for the optimization are listed in Table 1. The core characteristics for the magnetic component losses and costs in this case study are based on EELP 102 set with N87 from TDK [39]. For the semiconductor power switches, electrical characteristics and market data for commercial SiC power devices from Cree are used.

B. OPTIMIZATION RESULTS

In this section, the performance of the GP optimization is validated with the design values derived for the example system. To serve as a reliable reference for the performance evaluation, results from an exhaustive search algorithm using the original system models, without approximations for

convexity, are used. The algorithm searches the entire design space formed with a range of free variables. The reference data sets generated from the algorithm are reliable since the original models are based on common approaches that are widely accepted in the literature, and also they have been validated for the modular multilevel architecture for the case study in the prior works. Reference [33] validated topological feasibility, [40] substantiated control, and [36] provided loss and efficiency models. They include experimental results for the architecture as well as experimental validation of the loss models.

TABLE 2. Performance comparison of GP optimization compared to exhaustive search.

Test case	Time [s]	$\frac{\Delta LCOE}{LCOE}$ [%]
Step I	6.01	3.46
Step II	9.76	3.36
Step III	13.23	3.35
Exhaustive	70,448	3.30

Based on the discussion, the performance of the GP optimization is evaluated by comparison with the exhaustive search. Fig. 13 presents two performance metrics of the brute-force method, the computation time and the LCOE improvement achieved, as a function of the number of data points per variable. As expected, the computation time exponentially increases with increasing data points since the total number of cases searched is proportional to $n_d^{n_f}$, where n_d and n_f are the number of data points per variable and the number of free variables. On the other hand, notably, the LCOE improvement factor saturates approaching 3.3%, following the initial steady increase beyond a certain point, which implies that it approaches a design point near the optimal, but it is not guaranteed to be the definite solution. Fig. 13 also clearly shows the heavy computation required to derive a near-optimal point. In this case, it takes 2000 seconds to find a design to approach 3.3% of LCOE improvement.

TABLE 3. Key designs values from the GP optimization and exhaustive search. Variables adjusted to practical values are highlighted in bold at the step of iteration.

Methods	N_{module}	$R_{ds,pri}$ [mΩ]	$R_{ds,sec}$ [mΩ]	$R_{ds,INV}$ [mΩ]	$f_{sw,QAB}$ [kHz]	$f_{sw,INV}$ [kHz]	$V_{core,XF}$ [cm ³]	$V_{core,IND}$ [cm ³]	$N_{t,XF,pri}$ [turns]	$N_{t,XF,sec}$ [turns]	$N_{t,IND}$ [turns]
Step I	18.7	104	149	106	237	7.31	195	91.4	38.3	28.7	15.5
Step II	19	106	146	105	126	7.07	135	92.9	51.8	38.9	19.6
Step III	19	106	146	105	123	7.07	136	91.2	52	39	20
Exhaustive	19	110	140	110	89	8.86	155	89.4	64	48	22

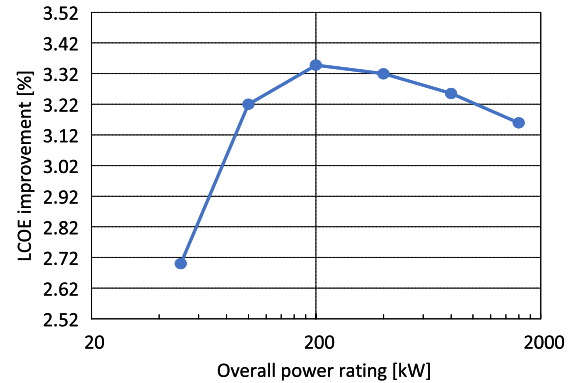
TABLE 4. LCOE improvement factor error from curve fitting of transformer and inductor copper loss models.

Methods	Copper loss, XF [W]	Copper loss, IND [W]	$\frac{\Delta LCOE}{LCOE}$ [%]
Step III (w/ fitting)	32.48	16.37	3.33
Step III (w/o fitting)	32.17	15.29	3.35
Error [%]	0.96	7.05	0.41

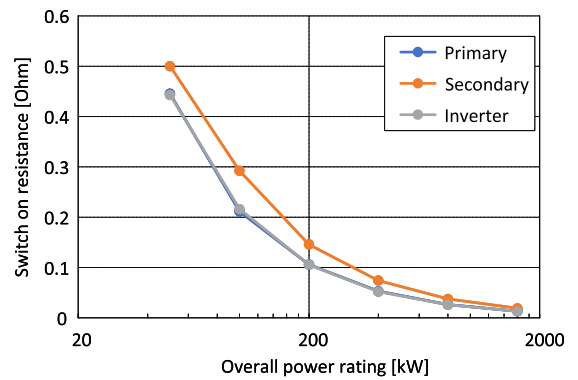
Table 2 compares the computation time taken for each step of the proposed GP optimization and the LCOE improvement estimates to the exhaustive search. The reference data from the exhaustive search are taken from the case with 20 samples per variable. For the proposed GP optimization, the result of Step I, direct from the convex optimization, indicates an LCOE improvement of 3.46% with impractical design values. Following, Step II iterates to a new optimization point with two variables adjusted to practical values, N_{module} and $N_{t,XF}$. Based on that, Step III achieves the final design with the other three integer variables rounded (refer to Figs. 11 and 12 for details). Fig. 14 locates the initial (Step I) and final design (Step III) values on the design surface generated from the exhaustive search with respect to N_{module} and $R_{ds(on),pri}$. As illustrated, the final result is in good agreement with the one from the original models, which validates the proposed optimization method. As tabulated in Table 2, the GP optimization outperforms the exhaustive search by three orders of magnitude in computation time (13.23 s versus 70,448 s), with the final design point of higher LCOE improvement (3.35% versus 3.30%). For reference, the design values from the GP and exhaustive search are listed in Table 3.

Table 4 shows the error resulting from the curve fitting of the copper loss model functions. The final fitting errors for the transformers and inductors are below the maximum discussed in Section IV-A (refer to Figs. 8d and 9d). The $\frac{\Delta LCOE}{LCOE}$ error caused by the function fitting is approximately 0.4%. The acceptable error and superior computation time confirm the value of the GP-based optimization.

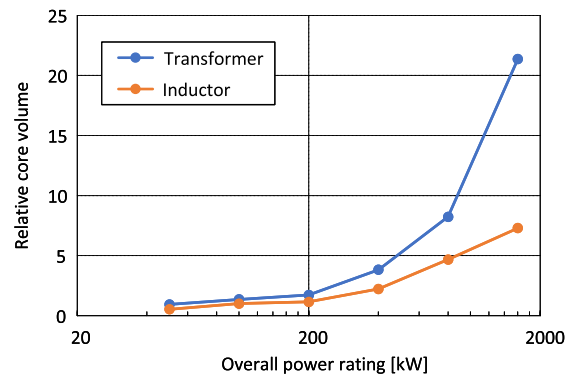
In addition, to provide insights for system scaling, optimization results with varying system power ratings are presented. The system power scales from 50 kW to 1.6 MW, with intervals of power of 2, with the other non-free variables fixed for the optimizations, yielding five additional data points, as displayed in Fig. 15. Fig. 15a shows that the LCOE improvement varies with changing power ratings. It implies that the power rating can be set as a design variable. It is, however, unclear that the final form of optimization would yield acceptable results. It may need to



(a) LCOE improvement



(b) Switch On-resistance



(c) Relative core volume

FIGURE 15. Optimization results as functions of system power rates.

compromise accuracy to incorporate the involving variable to maintain the tractable optimization; the system rating is closely coupled with other design variables, thus hindering the straightforward formation of posynomials with acceptable model accuracy. Regarding the optimal design parameters for

different power ratings, results for the switch on-resistances and core volumes are noticeable. As illustrated in Fig. 15b and 15c, the higher the power ratings, the larger switches and core volumes are favorable. It is matched with the common practice because higher power ratings (i.e., higher currents at the same voltage), in general, require lower switch on-resistance and larger core volume with thicker windings to avoid excessive conduction and copper loss, resulting in reduced optimal switching frequency to suppress the switching and core loss. In addition, note that the results may be valid only within a certain boundary since the non-free variables that were fixed at the optimizations should be properly scaled for changes, e.g., PV array voltage and grid interconnection voltage.

V. CONCLUSION

In this paper, an LCOE-oriented convex optimization of a grid-tied PV inverter system to derive power electronics design parameters has been presented. By formulating the objective function for the lifetime cost of energy generation that allows for decoupling design variables to enable superior computational efficiency, the GP optimization can find near-optimal design parameters that maximize the LCOE improvement for a new power electronics technology. Based on the framework, an optimization example for a cascaded modular PV inverter system was presented that suggests 3.35% LCOE improvement by the new power electronics and the advanced optimization. The GP-based design optimization example also validated its superior performance over the exhaustive search; it demonstrated it can find practical design values that obtain better LCOE in significantly reduced computation time, about 2,400 times shorter in the example. Using its superior performance, the proposed GP optimization framework can be applied to other power generation systems to evaluate the effect of the power electronics design on system efficiency and lifetime costs and to efficiently find practical optimal design values for implementation.

ACKNOWLEDGMENT

The U.S. Government retains and the publisher, by accepting the article for publication, acknowledges that the U.S. Government retains a nonexclusive, paid-up, irrevocable, worldwide license to publish or reproduce the published form of this work, or allow others to do so, for U.S. Government purposes. The views expressed in the article do not necessarily represent the views of the DOE or the U.S. Government. The authors would like to thank Dr. Hugo Nestor Villegas Pico for his assistance in the initial LCOE modeling effort and Dr. Jinia Roy for her assistance in the initial stage of the convex optimization framework development during their time at the National Renewable Energy Laboratory.

REFERENCES

[1] R. Fu, D. J. Feldman, and R. M. Margolis, "U.S. Solar photovoltaic system cost benchmark: Q1 2018," Nat. Renew. Energy Lab. (NREL), Golden, CO, USA, Tech. Rep. NREL/TP-6A20-72399, 2018. [Online]. Available: <https://www.nrel.gov/docs/fy19osti/72399.pdf>

[2] N. M. Haegel et al., "Terawatt-scale photovoltaics: Transform global energy," *Science*, vol. 364, no. 6443, pp. 836–838, 2019.

[3] T. J. Silverman and H. Huang, "Solar energy technologies office multi-year program plan," U.S. Dept. Energy Sol. Energy Technol. Office, Washington, DC, USA, Tech. Rep. DOE/EE-2346, May 2021. [Online]. Available: <https://www.energy.gov/sites/default/files/2021-06/Solar%20Energy%20Technologies%20Office%202021%20Multi-Year%20Program%20Plan%2006-21.pdf> and <https://www.osti.gov/biblio/1783207-solar-energy-technologies-office-multi-year-program-plan>

[4] W. Short, D. J. Packey, and T. Holt, "A manual for the economic evaluation of energy efficiency and renewable energy technologies," Nat. Renew. Energy Lab., Golden, CO, USA, Tech. Rep. NREL/TP-462-5173, 1995. [Online]. Available: <https://www.nrel.gov/docs/legosti/old/5173.pdf>

[5] R. Jones-Albertus, D. Feldman, R. Fu, K. Horowitz, and M. Woodhouse, "Technology advances needed for photovoltaics to achieve widespread grid price parity," *Prog. Photovolt., Res. Appl.*, vol. 24, no. 9, pp. 1272–1283, Sep. 2016.

[6] T. Kerekes, E. Koutroulis, D. Sera, R. Teodorescu, and M. Katsanevakis, "An optimization method for designing large PV plants," *IEEE J. Photovolt.*, vol. 3, no. 2, pp. 814–822, Apr. 2013.

[7] S. Rehman, H. U. R. Habib, S. Wang, M. S. Buker, L. M. Alhems, and H. Z. Al Garni, "Optimal design and model predictive control of standalone HRES: A real case study for residential demand side management," *IEEE Access*, vol. 8, pp. 29767–29814, 2020.

[8] K. Branker, M. J. M. Pathak, and J. M. Pearce, "A review of solar photovoltaic levelized cost of electricity," *Renew. Sustain. Energy Rev.*, vol. 15, no. 9, pp. 4470–4482, Dec. 2011.

[9] M. Kharrich, S. Kamel, M. Abdeen, O. H. Mohammed, M. Akherraz, T. Khurshaid, and S.-B. Rhee, "Developed approach based on equilibrium optimizer for optimal design of hybrid PV/wind/diesel/battery microgrid in Dakhla, Morocco," *IEEE Access*, vol. 9, pp. 13655–13670, 2021.

[10] C. Breyer and A. Gerlach, "Global overview on grid-parity: Global overview on grid-parity," *Prog. Photovolt., Res. Appl.*, vol. 21, no. 1, pp. 121–136, Jan. 2013.

[11] G.-S. Seo, S. Mukherjee, J. Roy, K. Goodrick, R. Mallik, B. Majmunovic, S. Dutta, D. Maksimovic, and B. Johnson, "Levelized-cost-of-electricity-driven design optimization for medium-voltage transformerless photovoltaic converters," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2019, pp. 6973–6980.

[12] S. Saridakis, E. Koutroulis, and F. Blaabjerg, "Optimal design of modern transformerless PV inverter topologies," *IEEE Trans. Energy Convers.*, vol. 28, no. 2, pp. 394–404, Jun. 2013.

[13] S. Saridakis, E. Koutroulis, and F. Blaabjerg, "Optimization of SiC-based H5 and conergy-NPC transformerless PV inverters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 2, pp. 555–567, Jun. 2015.

[14] Z. An, R. P. Kandula, and D. Divan, "Comparative investigation of system-level optimized power conversion system architectures to reduce LCOE for large-scale PV-plus-storage farms," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Oct. 2021, pp. 719–726.

[15] Y. Yang, E. Koutroulis, A. Sangwongwanich, and F. Blaabjerg, "Minimizing the levelized cost of energy in single-phase photovoltaic systems with an absolute active power control," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2015, pp. 28–34.

[16] S. Boyd, S.-J. Kim, L. Vandenbergh, and A. Hassibi, "A tutorial on geometric programming," *Optim. Eng.*, vol. 8, no. 1, p. 67, Mar. 2007.

[17] Y. Nesterov and A. Nemirovskii, *Interior-Point Polynomial Algorithms in Convex Programming* (Studies in Applied Mathematics). Philadelphia, PA, USA: Society for Industrial and Applied Mathematics, 1994.

[18] *MOSEK Optimization Toolbox for MATLAB*, User's Guide Reference Manual, Version 4, MOSEK ApS, Copenhagen, Denmark, 2019.

[19] S. P. Boyd and S. J. Kim, "Geometric programming for circuit optimization," in *Proc. Int. Symp. Phys. Design (ISPD)*, 2005, pp. 44–46.

[20] R. A. Jabr, "Application of geometric programming to transformer design," *IEEE Trans. Magn.*, vol. 41, no. 11, pp. 4261–4269, Nov. 2005.

[21] I. Jang, Y. Lee, S. Kim, and J. Kim, "Power-performance tradeoff analysis of CML-based high-speed transmitter designs using circuit-level optimization," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 4, pp. 540–550, Apr. 2016.

[22] A. Sayed, A. N. Mohieldin, and M. Mahroos, "A fast and accurate geometric programming technique for analog circuits sizing," in *Proc. 31st Int. Conf. Microelectron. (ICM)*, Dec. 2019, pp. 316–319.

- [23] A. Stupar, M. Halamicck, T. Moianou, A. Prodic, and J. A. Taylor, "Efficiency optimization of a 7-switch flying capacitor buck converter power stage IC using simulation and geometric programming," in *Proc. IEEE 19th Workshop Control Modeling Power Electron. (COMPEL)*, Jun. 2018, pp. 1–8.
- [24] A. Stupar, T. McRae, N. Vukadinovic, A. Prodic, and J. A. Taylor, "Multi-objective optimization of multi-level DC–DC converters using geometric programming," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 11912–11939, Dec. 2019.
- [25] H. O. Hartley, "The modified Gauss–Newton method for the fitting of nonlinear regression functions by least squares," *Technometrics*, vol. 3, no. 2, pp. 269–280, May 1961.
- [26] J. J. Moré, "The Levenberg–Marquardt algorithm: Implementation and theory," in *Numerical Analysis*. Berlin, Germany: Springer, 1978, pp. 105–116.
- [27] A. Magnani and S. P. Boyd, "Convex piecewise-linear fitting," *Optim. Eng.*, vol. 10, no. 3, pp. 1–17, 2009.
- [28] J. Kim, L. Vandenberghe, and C.-K. K. Yang, "Convex piecewise-linear modeling method for circuit optimization via geometric programming," *IEEE Trans. Comput. Aided Design Integr. Circuits Syst.*, vol. 29, no. 11, pp. 1823–1827, Nov. 2010.
- [29] J. Le Ny and G. J. Pappas, "Geometric programming and mechanism design for air traffic conflict resolution," in *Proc. Amer. Control Conf.*, Jun. 2010, pp. 3069–3074.
- [30] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters," in *Proc. IEEE Workshop Comput. Power Electron.*, Jun. 2002, pp. 36–41.
- [31] P. L. Dowell, "Effects of eddy currents in transformer windings," *Proc. Inst. Elect. Eng.*, vol. 113, no. 8, pp. 1387–1394, Jun. 1966.
- [32] K. Iyer, "Transformer winding losses with round conductors and foil windings for duty-cycle regulated square waveform followed by winding design and comparison for sinusoidal excitation," Ph.D. dissertation, Univ. Minnesota, Minneapolis, MN, USA, 2013.
- [33] P. K. Achanta, B. B. Johnson, G.-S. Seo, and D. Maksimovic, "A multilevel DC to three-phase AC architecture for photovoltaic power plants," *IEEE Trans. Energy Convers.*, vol. 34, no. 1, pp. 181–190, Mar. 2019.
- [34] D. Karwatzki and A. Mertens, "Generalized control approach for a class of modular multilevel converter topologies," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 2888–2900, Apr. 2018.
- [35] P. Hu, R. Teodorescu, S. Wang, S. Li, and J. M. Guerrero, "A currentless sorting and selection-based capacitor-voltage-balancing method for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1022–1025, Feb. 2019.
- [36] B. Majmunovic, S. Mukherjee, R. Mallik, S. Dutta, G.-S. Seo, B. Johnson, and D. Maksimovic, "Soft switching over the entire line cycle for a quadruple active bridge DCX in a DC to three-phase AC module," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2020, pp. 3464–3471.
- [37] H. Kim and K.-H. Kim, "Filter design for grid connected PV inverters," in *Proc. IEEE Int. Conf. Sustain. Energy Technol.*, Nov. 2008, pp. 1070–1075.
- [38] W. Hoburg, P. Kirschen, and P. Abbeel, "Data fitting with geometric-programming-compatible softmax functions," *Optim. Eng.*, vol. 17, no. 4, pp. 897–918, 2016.
- [39] *TDK EELP 102 Core Datasheet*, TDK, Tokyo, Japan, May 2017.
- [40] S. Dutta, M. Lu, B. Majmunovic, R. Mallik, G.-S. Seo, D. Maksimovic, and B. Johnson, "Grid-connected self-synchronizing cascaded H-bridge inverters with autonomous power sharing," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Oct. 2021, pp. 2806–2813.



YEONGRACK SON (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Seoul National University, South Korea, in 2011, 2013, and 2017, respectively.

From 2017 to 2019, he was a Staff Engineer at Samsung Electronics Company, South Korea. He is currently with the National Renewable Energy Laboratory (NREL), working as a Post-doctoral Researcher. His research interests include

power electronics and control systems for renewable energy systems and microgrids.



SATYAKI MUKHERJEE (Member, IEEE) received the integrated B.Tech. and M.Tech. degrees in electrical engineering from the Indian Institute of Technology, Kharagpur, in 2018, and the Ph.D. degree from the Colorado Power Electronics Center (CoPEC), University of Colorado at Boulder, in June 2021.

He was a member of Research and Development Staff with the Milan M. Jovanović Power Electronics Laboratory (MPEL), Delta Electronics (Americas) Ltd., Research Triangle Park. He held a graduate student intern position with the Kilby Laboratories, Texas Instruments Inc., Santa Clara, in 2019. His current research interests include power electronics for transportation electrification and renewable energy sources, high-frequency power conversion using wide bandgap semiconductors, high frequency magnetics design, automotive lighting, and digital control of switched-mode power converters.



RAHUL MALLIK (Graduate Student Member, IEEE) received the B.E. degree in electrical engineering from Jadavpur University, in 2015, and the M.E. degree in electrical engineering from the Indian Institute of Science, in 2017. He is currently pursuing the Ph.D. degree with the University of Washington, Seattle.

He has worked as an Associate Scientist at Hitachi ABB Power Grids, from 2017 to 2018, and interned at Enphase Energy, TX, USA, in 2021.

Since 2018, he has been a Research Assistant with the Washington Power Electronics Laboratory, University of Washington. His research interests include design, modeling and control of high-power/high-frequency DC-DC converters, nonlinear control of grid forming inverters, and electromechanical systems.



BRANKO MAJMUHOVIĆ (Graduate Student Member, IEEE) received the B.S. degree in electrical engineering from the University of Belgrade, Belgrade, Serbia, in 2016, and the M.S. degree in power electronics and drives from Aalborg University, Aalborg, Denmark, in 2018. He is currently pursuing the Ph.D. degree with the Colorado Power Electronics Center (CoPEC), University of Colorado at Boulder, Boulder, CO, USA.

His current research interest includes optimization of active-bridge-based modular power converters.



SOHAM DUTTA (Graduate Student Member, IEEE) received the B.E. degree in electrical engineering from Jadavpur University, India, in 2015, and the M.E. degree in electrical engineering from the Indian Institute of Science, in 2017. He is currently pursuing the Ph.D. degree in power electronics with the University of Washington, Seattle, USA.

His research interests include design and control of cascaded DC–AC converters for medium voltage applications. His master's thesis was on the emulation of AC transmission lines using back-to-back power electronic converters.



BRIAN JOHNSON (Member, IEEE) received the M.S. and Ph.D. degrees in electrical and computer engineering from the University of Illinois at Urbana–Champaign, Urbana, in 2010 and 2013, respectively.

He is currently a Washington Research Foundation Innovation Assistant Professor with the Department of Electrical and Computer Engineering, University of Washington. Prior to joining the University of Washington, in 2018, he was an

Engineer with the National Renewable Energy Laboratory, Golden, CO, USA. His research interests include renewable energy systems, power electronics, and control systems. He is currently serving as an Associate Editor for the IEEE TRANSACTIONS ON ENERGY CONVERSION.



DRAGAN MAKSIMOVIĆ (Fellow, IEEE) received the B.S. and M.S. degrees in electrical engineering from the University of Belgrade, Belgrade, Serbia, in 1984 and 1986, respectively, and the Ph.D. degree from the California Institute of Technology, Pasadena, CA, USA, in 1989.

From 1989 to 1992, he was with the University of Belgrade. Since 1992, he has been with the Department of Electrical, Computer and Energy Engineering, University of Colorado at Boulder,

where he is currently a Professor and the Co-Director of the Colorado Power Electronics Center. He has coauthored more than 350 publications and the textbooks *Fundamentals of Power Electronics* (3rd edition, Springer 2020) and *Digital Control of High-Frequency Switched-Mode Power Converters* (Wiley IEEE Press 2015). His current research interests include power electronics for renewable energy sources and energy efficiency, high-frequency power conversion using wide bandgap semiconductors, and digital control of switched-mode power converters.

Prof. Maksimović received the 1997 NSF Career Award, the *IEEE PELS Transactions Prize Paper Award*, in 1997, the IEEE PELS prize letter awards, in 2009 and 2010, the University of Colorado at Boulder Inventor of the Year Award, in 2006, the IEEE PELS Modeling and Control Technical Achievement Award for 2012, the Holland Excellence in teaching awards, in 2004, 2011, and 2018, the Charles Hutchinson Memorial Teaching Award for 2012, and the 2013 Boulder Faculty Assembly Excellence in Teaching Award.



GAB-SU SEO (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from Seoul National University, Seoul, South Korea, in 2015.

From 2016 to 2017, he was a Research Associate with the Colorado Power Electronics Center, University of Colorado at Boulder, Boulder, CO, USA. Since 2018, he has been with the National Renewable Energy Laboratory (NREL), Power Systems Engineering Center, Golden, CO, USA,

where he is currently a Senior Electrical Engineer and leads research projects focused on power electronics and power systems applications for electric grids with high penetrations of inverter-based resources. He has coauthored more than 60 IEEE journals and conference papers with one best paper award. He coauthored the Research Roadmap on Grid-Forming Inverters (NREL), in 2020. His current research interests include power electronics for renewable energy systems and microgrids and power systems engineering for grid modernization, including grid-forming inverter control and inverter-driven power system black start for low- or zero-inertia grids to improve grid resilience and stability.

Dr. Seo is the IEEE Roadmap Working Group Chair of the International Technology Roadmap of Power Electronics for Distributed Energy Resources (ITRD)–WG3 Integration and Control of DER. He is an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS, the IEEE ACCESS, the IEEE OPEN JOURNAL OF POWER ELECTRONICS, and the *Journal of Power Electronics*.

• • •