48 V to 1 V Active-Clamp Stacked Direct Forward Converter

by

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Thesis directed by Prof. Dr. Dragan Maksimovic

Abstract

This thesis presents a 48 V-to-1 V stacked direct forward (SDF) dc-dc converter consisting of four 12 V-to-1 V direct forward (DF) modules connected in input-series output-parallel (ISOP) configuration. In each DF module, there is no secondary-side inductance, and a single-ended forward transformer is driven at a high duty cycle to reduce the switch root-mean-square currents. An active clamp is employed on the primary side to reset the transformer, limit the switch voltage stress, and facilitate zero voltage switching. The approach is verified by simulation results on a 12 V-to-1 V, 50 A, 200 kHz prototype module using GaN devices and a planar transformer, and having a peak efficiency of 93.9% and the full-load efficiency of 91.8%. In this thesis, experimental results are presented for a 12 V-to-1 V DF prototype.

Dedication

To my beloved family and in the memory of my late grandfather.

Acknowledgements

I would like to thank my thesis advisor, Dr. Dragan Maksimovic, for giving me the opportunity to do my master's thesis under his guidance. Thanks to his guidance and encouragement, I was able to gain a lot of valuable knowledge in the field of power electronics and keep myself motivated throughout the completion of my thesis. Additionally, I would like to thank Dr. Luca Corradini and Dr. Robert W. Erickson, who have helped me learn and better understand analysis, modeling, design and control techniques in power electronics. I would like to thank my peers who supported and encouraged me during the completion of my thesis. Finally, I would like to thank my parents for their support as well as inspiration throughout my graduate studies.

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Chapter 1

Introduction

With the development in wireless technology, Internet of Things, cloud computing, etc., there has been an increase in power demand. To meet this increasing demand in data center server applications, there has been a shift toward using 48 V bus voltage, which leads to a reduction in distribution losses. For a given power level, distribution losses are inversely proportional to voltage square:

$$P_{loss} \propto \frac{1}{V^2} \tag{1.1}$$

Thus, with increase in the voltage from 12 V to 48 V the distribution losses are reduced 16 times. Figure 1.1 shows block diagram of a 48 V server board used in data centers today.

The shift to 48 V distribution has caused an increase in the demand for intermediate 48 V to 12 V power converters and 48 V to 1 V Point of Load (PoL) converters. Thus, there is a need for DC-DC converters that provide high step-down ratio of 48 V-to-1 V with high efficiency. Typical DC-DC converters, such as the buck-converter, have much lower efficiency at high conversion ratios because of the presence of indirect power, which is a function of the conversion ratio. The indirect power, $P_{indirect}$, is the power transferred through the input to the output through the switching action of power semiconductor devices, which converts dc power from the input to the power and then rectifies the ac power back to the dc power at

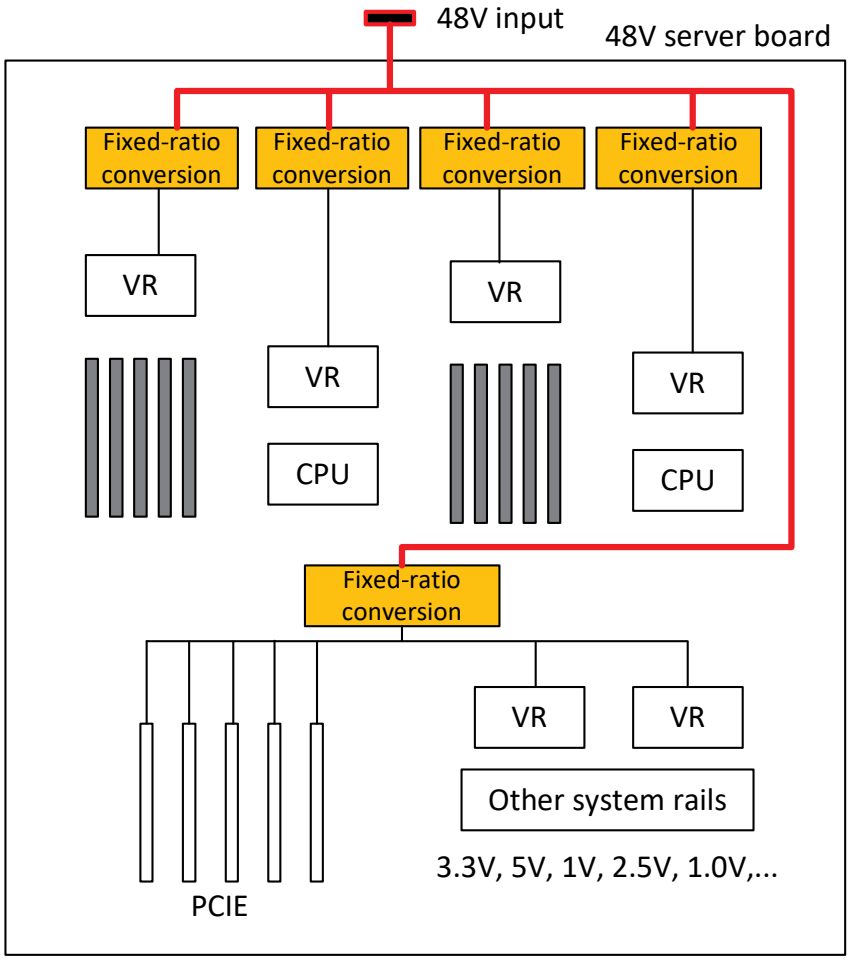


Figure 1.1: 48 V data center server board.

the output. For example, for a buck converter, the direct power is given by:

$$P_{direct} = DP_{out} \tag{1.2}$$

and the indirect power is given by:

$$P_{indirect} = D'P_{out} \tag{1.3}$$

where D, which is the duty-cycle of the top power FET, is equal to the conversion ratio V_{out}/V_g, assuming losses are small.

Recent advances in 48-to-1 V conversion include, for example, hybrid switched capacitor [1–4], switched resonant tank [3], transformer-isolated [5], and composite "sigma"

converters [6]. Figure 1.2 summarizes the designs proposed in recent literature. As can be seen in this figure, the full load efficiency of most of the proposed designs is less than 90%. In

			APEC 2023			
Parameter	Transformer less Stacked Active Bridge Converter with Merged Regulation Stage [10]	Vertical Stacked LEGO-PoL CPU Voltage Regulator [4]	Mini-LEGO based 48-V-to-1-V CPU VRM for Vertical Power Delivery [2]	Hybrid GaN-Si CPU VRM with Multi-stack Switched Capacitor [3]	Hybrid Switched Capacitor Voltage Regulator based 48 V – 1V Converter [1]	48/1V Sigma Converter Voltage Regulator Module [9]
Gain	48	48	48	48	48	48
Architecture	TSAB + Multiphase Buck	2:1 Switched Capacitor + M-phase Buck	2:1 Switched Capacitor + M-phase Buck	Multi-stack Switched Capacitor	2:1 Switched Capacitor + 8:1 Series-Capacitor-Buck	LLC Converter (with matrix transformer)+ Buck Converter
Load	~90 *A*	780 *A*	240 A	220 *A*	500 *A*	80 A
Complexity	Relatively Higher	Relatively Higher	–	–	–	Relatively Higher
Peak System Efficiency	91.5 %	91.1 %	87.1 %	92.9 % (w/ leakage inductor) 91.2 % (w/o leakage inductor)	94.7 %	93.4 %
Full Load System Efficiency	~85 %	79.2 %	84.1 %	86.3 % (w/ leakage inductor) 85.1 % (w/o leakage inductor)	86.4 %	91.6 %

Figure 1.2: Summary of literature review.

addition, the proposed topologies are either two-stage power conversion systems or converter architectures with merged topologies. Both these types of solutions are fairly complicated architectures with the individual converters being either hybrid switched capacitor converter topologies or resonant converters, such as LLC converters.

A different, "direct power conversion" principle was introduced in [7] and demonstrated for 48 V-to-12 V and 12 V-to-1 V applications. Operating as a standard forward converter but without the secondary-side inductor, the direct power converter offers simple and highly efficient open-loop operation with an essentially fixed conversion ratio determined by the transformer turns ratio. However, in very high-step-down applications, such as 48-to-1 V, the switch voltage stress and the transformer design present practical limitations.

These inferences helped motivate the work presented in this thesis, which has the following objectives:

- To achieve a full-load efficiency higher than 90% for the overall conversion ratio of

48 V to 1 V.

- To propose an overall simpler converter architecture.

One way to approach the problem is by designing converters that are more efficient in processing the indirect power at high conversion ratios. Such converters may have the following characteristics:

- Reduced switch voltage and current stress;
- Reduced inductor or transformer volt-seconds;
- Soft-switching such as zero-voltage switching (ZVS) or zero-current switching (ZCS).

This thesis proposes a stacked direct forward (SDF) converter shown in Fig. 1.3, consisting of four 12 V-to-1 V active-clamp direct forward (DF) converter modules shown in Fig. 2.1. The DF modules are connected in input-series output-parallel (ISOP) configuration. This converter offers three features compared to the approach described in [7]:

(1) A very high step-down ratio is achieved using a stacked converter architecture similar to the approach described in [8];

(2) An active clamp is used in each DF module to reset the transformer, limit the voltage stress, and facilitate zero voltage switching

(3) A planar transformer is used to achieve a low profile and simplify the overall converter design.

The thesis presents the design, simulation and experimental results for a highly efficient 12 V-to-1 V, 200 kHz prototype DF module using GaN devices, as well as simulation results for a complete

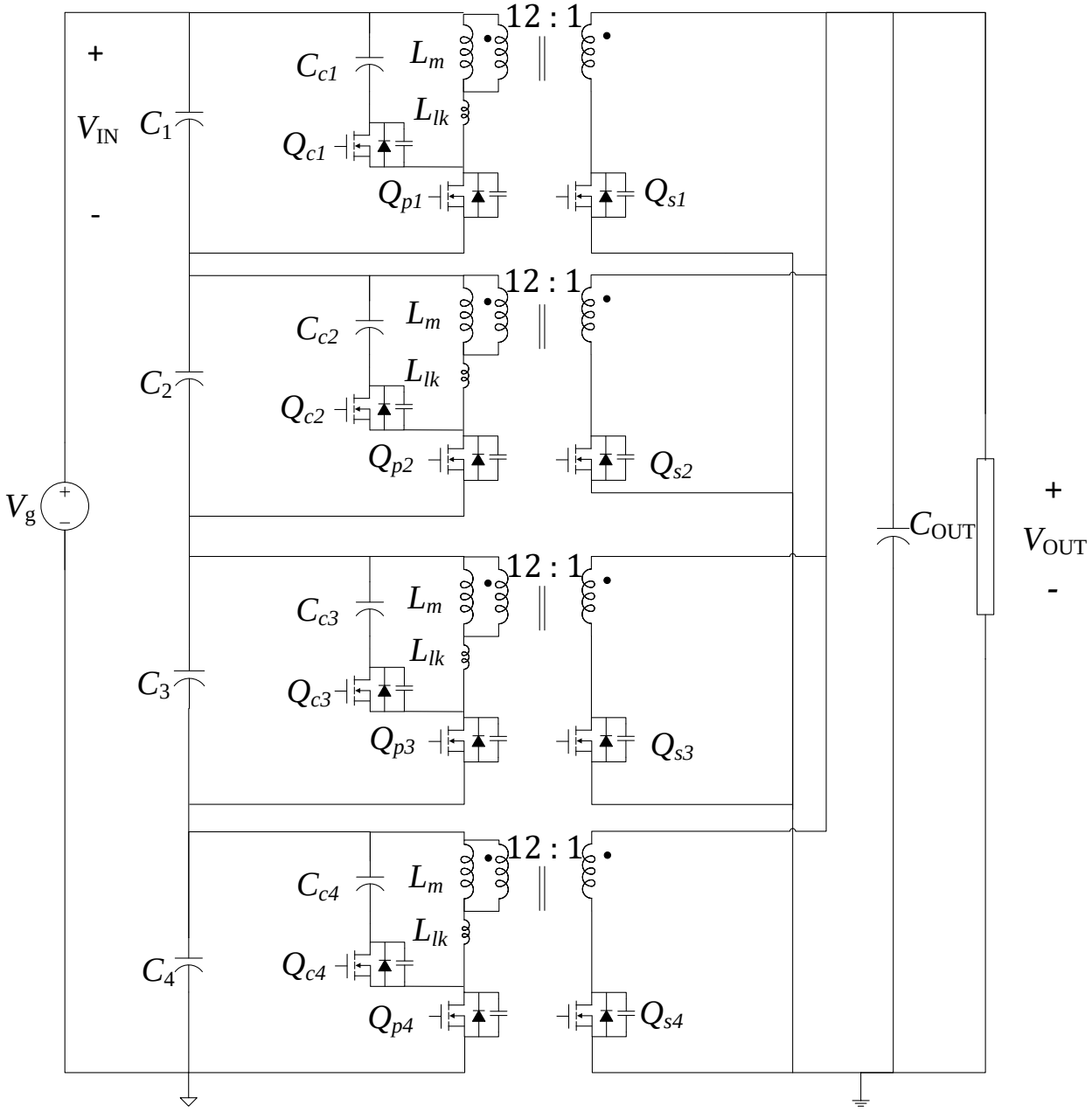


Figure 1.3: Proposed stacked direct forward (SDF) dc-dc converter comprising four active-clamp direct forward (DF) modules in input-series, output-parallel configuration, $V_{IN} = V_g/4$.

Chapter 2

Active-Clamp Direct Forward Converter Module

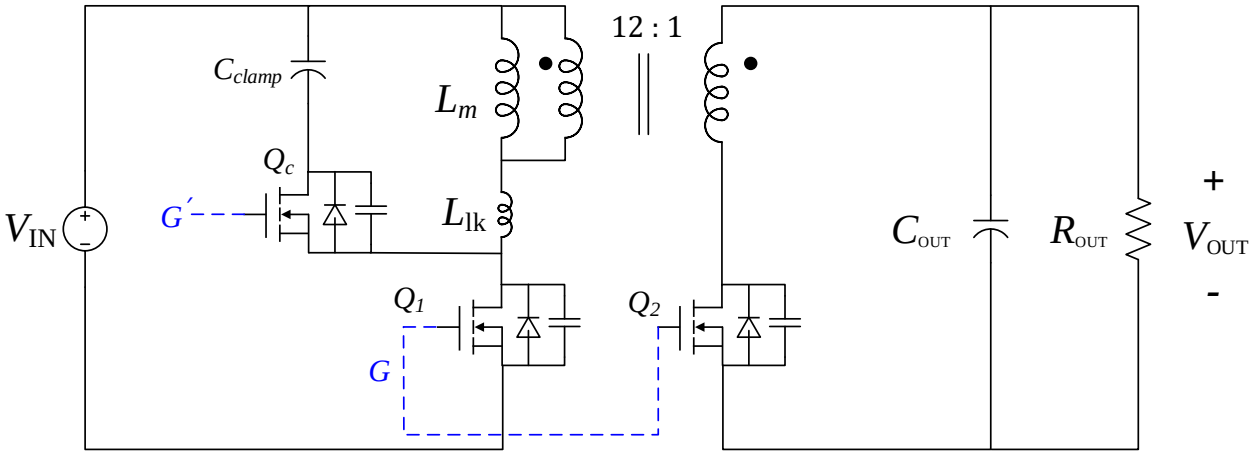


Figure 2.1: 12 V-to-1 V active-clamp direct forward (DF) converter module.

The 12 V-to-1 V active-clamp DF converter is shown in Fig. 2.1. This converter has a 12:1 transformer and excludes the secondary-side inductor. Both the primary switch Q_1 and the secondary switch Q_2 are turned on and off simultaneously at high duty cycle D. When Q_1 and Q_2 are both on, a scaled input voltage $V_{IN}/12$ is impressed across the secondary, and the current charging the output filter capacitor is limited only by the transformer leakage inductance and the series resistances of the switches and the windings. When Q_1 and Q_2 are turned off, the magnetizing inductance forms a resonant circuit with the output capacitance

of the devices. Resonance results in high voltage stress and the need to precisely time the switching period [7]. As in a standard forward converter, the active clamp shown in Fig. 2.1 limits the voltage stress to approximately $V_{IN}/(1-D)$, resets the transformer more effectively and allows zero-voltage switching with more flexibility in the timing of switch control signals.

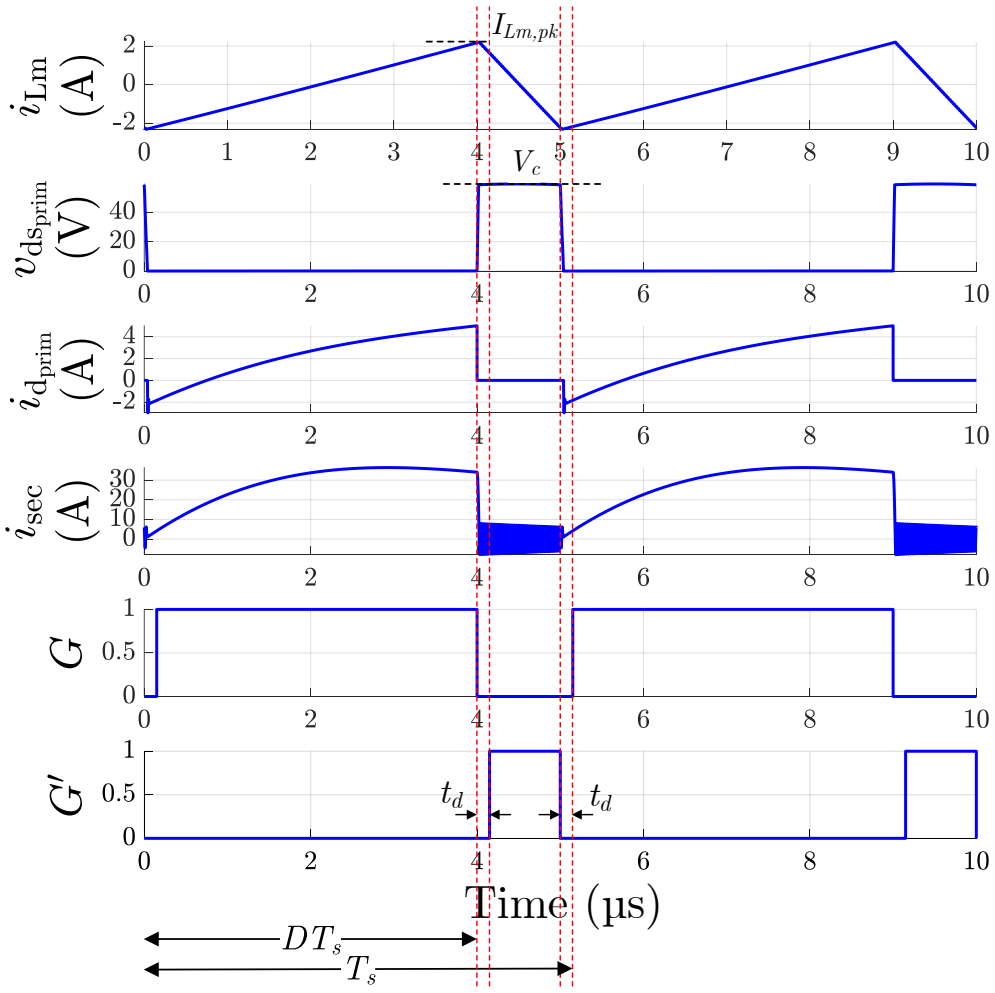


Figure 2.2: Switching waveforms in the direct forward (DF) converter.

2.1 Active-Clamp Direct Forward Converter Operation

Referring to the waveforms in Fig. 2.2, in the DT_s interval, both Q_1 and Q_2 conduct. This causes the power to flow directly from the input to the output and the magnetizing inductance charges to its peak value, $I_{Lm,pk}$. The secondary current, which is limited only by the transformer leakage inductance and the device and winding series resistances, charges the output filter capacitor. In response to an increase in load, the drop in the output voltage results in an automatic increase in the secondary current. The conversion ratio is essentially fixed and determined by the transformer turns ratio.

In the $D^{'}T_s$ interval, Q_1 and Q_2 are both off, and the clamp switch turns on (with short dead times in between). In this interval, the transformer magnetizing inductance of the transformer is discharged through the clamp switch. The voltage stress across Q_1 and Q_2 is approximately equal to $\frac{V_{IN}}{(1-D)}$ and $\frac{V_{IN}}{12(1-D)}$ respectively.

As in a standard active-clamp converter, short dead times t_d are introduced between the switching of Q_1 and Q_2 and Q_c. Resonant transitions during the dead times result in zero voltage switching of all devices.

2.2 State Plane Analysis

Time-domain analysis of resonant and soft-switching circuits can be very tedious due to the presence of a system of differential equations which may need to be solved simultaneously. State-Plane Analysis is a tool that converts the dc-dc converter analysis into a geometrical problem; where the geometry is a circle. This is typically an easier way to perform a design-oriented analysis of the dc-dc converter.

The DF converter is also analyzed using the same approach. First, we consider the normalized current and voltage parameters as follows for the analysis:

$$V_{base} = V_{IN} \tag{2.1}$$

$$R_0 = \sqrt{\frac{L_m}{C_{eq}}} \qquad \text{and} \qquad \omega_0 = \sqrt{\frac{1}{L_m C_{eq}}} \tag{2.2}$$

where

$$C_{eq} = C_{Q_1} + C_{Q_c} + N^2 C_{Q_2} \tag{2.3}$$

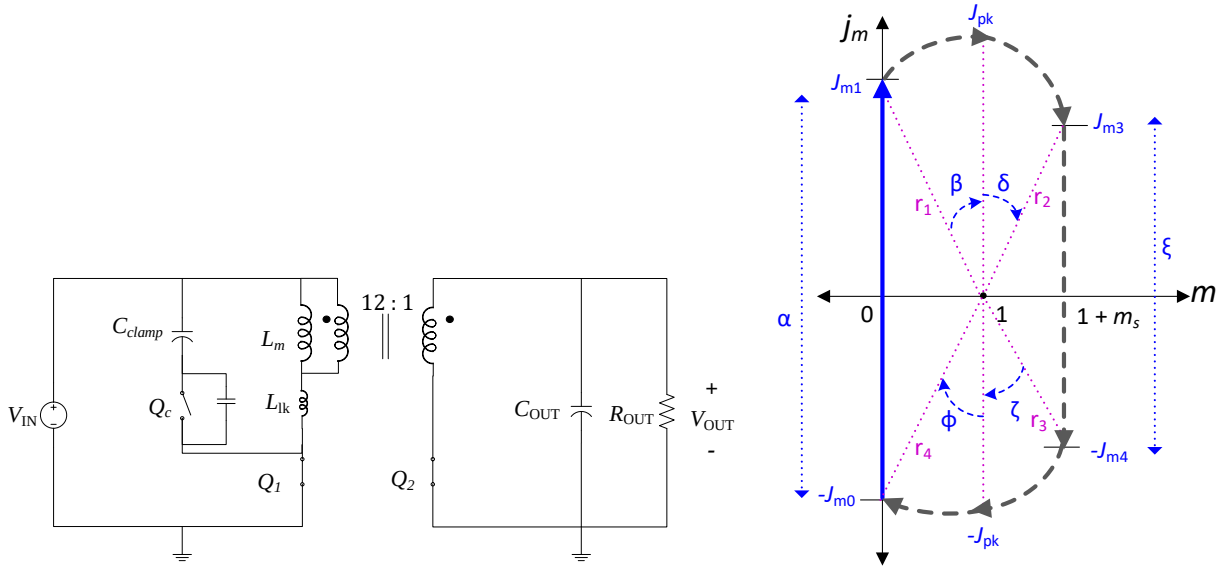
N is the turns ratio of the transformer, $N = 12$, and

$$I_{base} = \frac{V_{base}}{R_0} \tag{2.4}$$

The inductor current and capacitor voltages are normalized using V_{base} and I_{base}. Let the inductor current and the capacitor voltage be denoted by i_{L_m} and v_{ds}. These normalized variables are denoted by:

$$m = \frac{v_{ds}}{V_{base}} \quad \text{and} \quad j_m = \frac{i_{Lm}}{I_{base}} \tag{2.5}$$

2.2.1 Sub-interval 1: Q_1 and Q_2 are on and Q_c is off



(a) (b)

Figure 2.3: Sub-interval - 1: (a) circuit-state (b) state-plane

Referring to Fig. 2.3, the switches Q_1 and Q_2 conduct and the magnetizing inductance,

L_m, charges. The initial condition is given by

$$j_m = -J_{m_0} \quad \text{and} \quad m = 0 \tag{2.6}$$

During this interval, j_m increases to J_{m1} while $m = 0$ since the switches, Q_1 and Q_2 are on. The voltage across the magnetizing inductance is V_{IN} and thus the magnetizing current increases with a slope of $\frac{V_{IN}}{L_m}$.

2.2.2 Sub-interval 2 (dead-time interval): Q_1 and Q_2 are on and Q_c is off

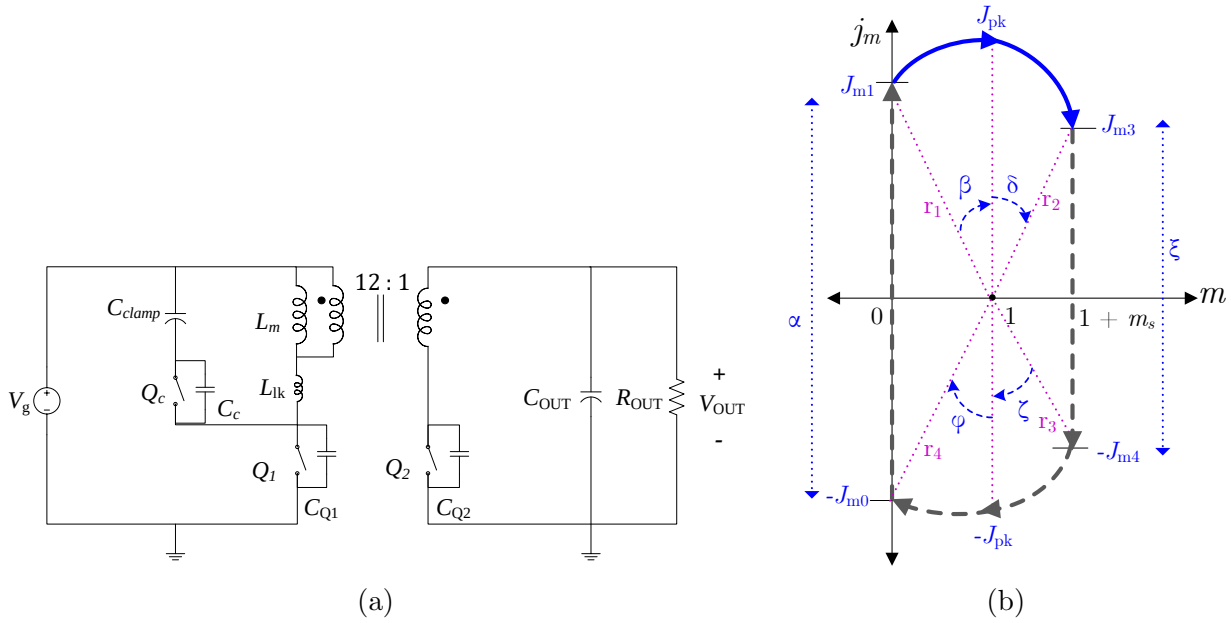


Figure 2.4: Sub-interval - 2: (a) circuit-state (b) state-plane

Initial conditions are:

$$j_m = J_{m_1} \quad \text{and} \quad m = 0 \tag{2.7}$$

As shown in Fig. 2.4, in this interval, the switches Q_1 and Q_2 are off and the magnetizing inductance, L_m, charges until the switch node voltage, v_{ds} reaches V_{IN}. At this point, the magnetizing current i_{L_m} reaches its peak value.

During this interval, there is resonance between the equivalent capacitance, C_{eq} and L_m. Once the switch-node voltage reaches V_g, the magnetizing inductor starts to discharge and v_{ds} now increases further to $\frac{V_{IN}}{1-D}$.

Dead time can be calculated as:

$$t_{d_1} = \frac{\beta}{\omega_0} + \frac{\delta}{\omega_0} \tag{2.8}$$

The final condition is

$$j_m = J_{m_3} \quad \text{and} \quad m = 0 \tag{2.9}$$

2.2.3 Sub-interval 3: Q_1 and Q_2 are on and Q_c is off

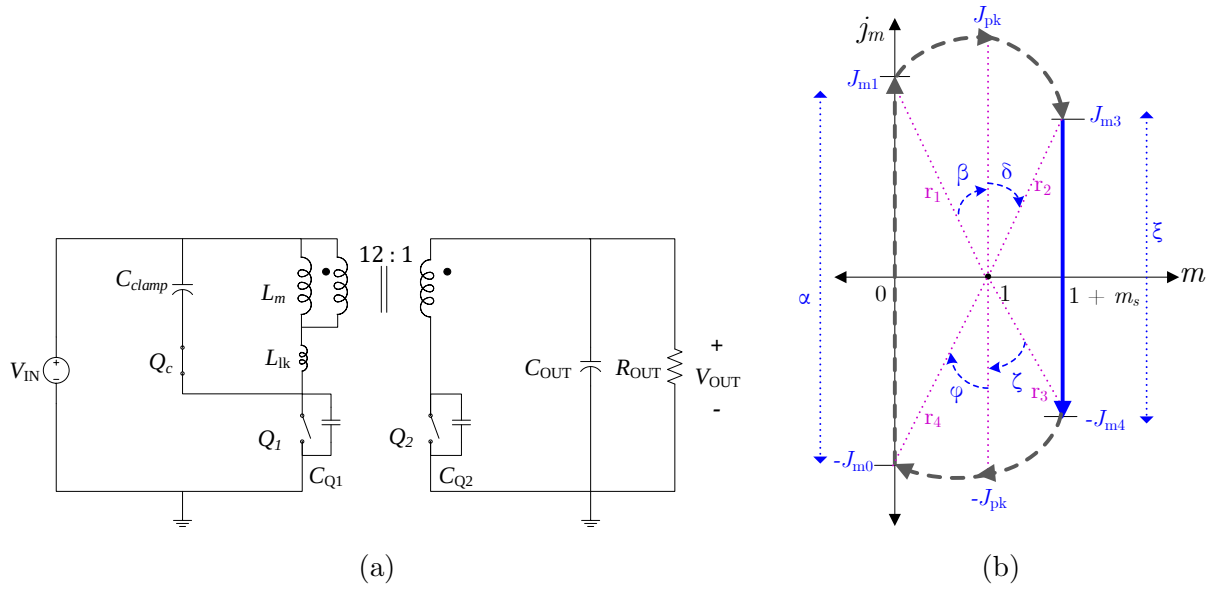


Figure 2.5: Sub-interval - 3: (a) circuit-state (b) state-plane

Initial conditions are:

$$j_m = J_{m_3} \quad \text{and} \quad m = 0 \tag{2.10}$$

Referring to Fig. 2.5, in this interval, the switches Q_1 and Q_2 are off and now the clamp switch, Q_c is turned on with ZVS. Magnetizing inductance, L_m, discharges linearly from J_{m_3}

to $-J_{m_4}$ and the switch node voltage, v_{ds} remains constant at $\frac{V_{IN}}{1-D}$. This corresponds to $m = (1 + m_s)$.

2.2.4 Sub-interval 4 (dead-time interval): Q_1 and Q_2 are on and Q_c is off

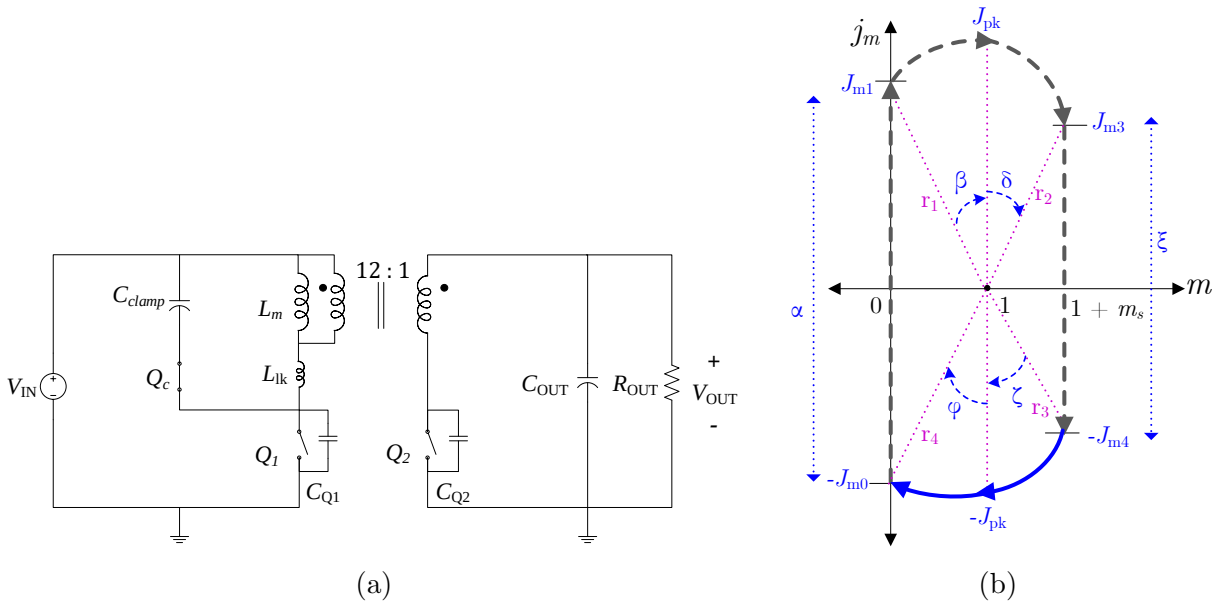


Figure 2.6: Sub-interval - 4: (a) circuit-state (b) state-plane

Initial conditions are:

$$j_m = -J_{m_4} \quad \text{and} \quad m = 1 + m_s \tag{2.11}$$

According to Fig. 2.6, in this interval, the switches Q_1 and Q_2 are off and Q_c is turned off. The magnetizing inductance, L_m, reaches its negative peak in the ζ interval when the switch node voltage, v_{ds} reaches V_g.

Once the switch-node voltage reaches V_g, the magnetizing inductor starts to charge to $-J_{m_0}$ as v_{ds} further decreases to zero in the φ interval. During this entire interval, there is resonance between the equivalent capacitance, C_{eq} and L_m. Dead time is calculated as:

$$t_{d_2} = \frac{\zeta}{\omega_0} + \frac{\varphi}{\omega_0} \tag{2.12}$$

The ZVS turn on window for Q_1 and Q_2 is from the instant when $m = 0$ from $j_m = -J_{m0}$ to until it is negative. Solving the state-plane at the boundary condition gives the minimum required L_m to satisfy the ZVS conditions for all the switches.

2.3 Gate Driver and FET Loss calculations

Since ZVS is achieved on all the switches, the primary sources of switch loss and gate-driver loss are as follows:

(1) Conduction Loss

(2) Turn-off Loss

(3) Gate-driver Loss

Referring to Fig. 2.1, these loss calculations are documented below.

2.3.1 Conduction Loss Calculation:

$$P_{Q_i} = I_{rms}^2 R_{ds_{on_{125_i}}} \tag{2.13}$$

where Q_i represents the primary, clamp, or secondary GaN FET and $R_{ds_{on_{125_i}}}$ represents the corresponding on-resistance of the switches at 125 °C.

2.3.2 Turn-off Loss Calculation:

$$P_{Q_{i_{turn-off}}} = \frac{\left(I_{Q_i} t_{off}\right)^2 f_{sw}}{24 C_{oss_i}} \tag{2.14}$$

where C_{oss_i} is the corresponding C_{oss} and t_{off} is the turn-off time of the corresponding switch. This value is assumed to be 5 ns.

2.3.3 Gate Driver Loss Calculation:

Half-Bridge Gate Driver Loss (Primary Side):

$$P_{HB} = (Q_{Q_1} + Q_{Q_c}) f_{sw} V_{dd} \tag{2.15}$$

Low Side Gate Driver Loss (Secondary Side):

$$P_{LS} = Q_{Q_2} f_{sw} V_{dd} \tag{2.16}$$

where V_{dd} is the gate driver supply voltage and Q_{Q_i} is the corresponding total gate charge of the switches.

2.4 Power Stage Design

A 12 V-to-1 V DF prototype of Fig. 2.1 is constructed for hardware validation with the following parameters: $V_g = 12\,\text{V}$ input voltage, $V_{\text{out}} \approx 1\,\text{V}$ output voltage , $i_o = 50\,\text{A}$ output current, $f_s = 200\,\text{kHz}$ switching frequency, $L_m = 10\,\mu\text{H}$, $C_{\text{out}} = 400\,\mu\text{F}$ and $C_{\text{clamp}} = 1\,\mu\text{F}$. The primary side devices, Q_1 and Q_{c} respectively, are implemented using a single EPC2033 GaN FET, rated for 150 V and having $r_{\text{ds,on}} \approx 7\,\text{m}\Omega$. The primary switches are driven using a half-bridge gate driver, LM5113SD. The secondary switch, Q_2, is implemented by paralleling 2-4 EPC2066 GaN FETs. These switches are rated for 40 V with a $r_{\text{ds,on}} \approx 1.1\,\text{m}\Omega$ each. A low-side gate driver, UCC27611DRVR, is used to drive the secondary-side switches.

Chapter 3

Planar Transformer Design and Analysis

3.1 Planar Transformer Design

The 12 : 1 planar transformer is designed with a magnetizing inductance of 10 µH using TDK EILP14 core having N87 material with an air gap of 0.262 mm. The transformer is designed on a separate 12-layer, 1 oz printed circuit board, which has an overall size of 25.32 mm × 19.68 mm, as shown in Fig. 3.1 with the winding configuration as follows: 6 layers of primary winding connected in series, each having 2 turns and 6 layers of secondary winding all connected in parallel with 1 turn per layer.

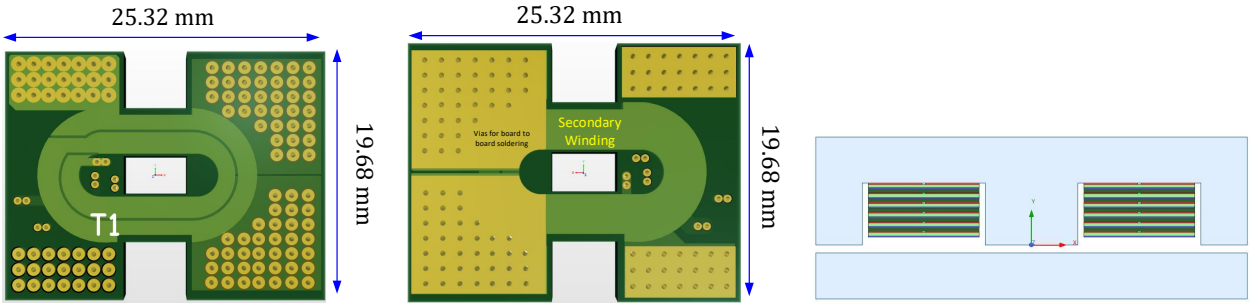


Figure 3.1: Transformer layout: (a) top view of PCB, (b) bottom view of PCB, (c) cross-sectional view of the transformer

The primary and secondary layers are completely interleaved to minimize proximity effects. A 2-D finite element analysis (FEA) is performed to estimate ac resistances and

more accurately predict winding losses. Figs. 3.1a and 3.1b show the layout of the transformer board, and the cross-sectional view of the transformer can be seen in Fig. 3.1c. The transformer has been fabricated and characterized using an impedance analyzer as shown in Fig. 4.2. A large number of vias are used for board-to-board soldering to ensure that the current has multiple parallel paths and that conduction losses through these vias are minimized.

3.2 Modelling and Finite Element Analysis of the Planar Transformer

Detailed loss modeling is performed on the transformer design candidates by calculating core loss using Improved Generalized Steinmetz Equation (iGSE) method and winding losses using Dowel's equations taking into account skin-depth and proximity effect-based losses. The geometrical parameters of the core are calculated from the core datasheet.

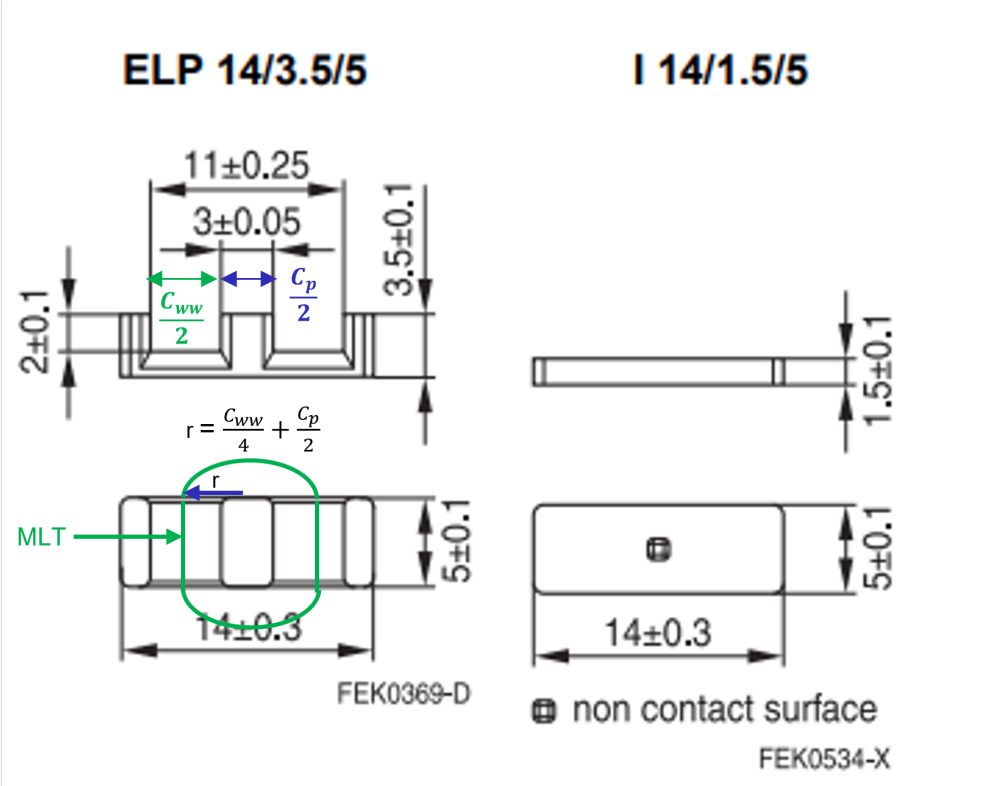


Figure 3.2: Core Dimension Calculations.

Using Fig. 3.2, the mean length per turn (MLT), window width (W), effective core area, (A_w) and effective core volume, (V) can be calculated as:

$$C_{ww} = 11\,\text{mm} - 3\,\text{mm} = 8\,\text{mm} \tag{3.1}$$

$$W = \frac{C_{ww}}{2} = 4\,\text{mm} \tag{3.2}$$

$$MLT = 2\left[5 + \pi\left(\frac{C_{ww}}{4} + \frac{3\,\text{mm}}{2}\right)\right] = 31.99\,\text{mm} \tag{3.3}$$

$$A_w = 14.5\,\text{mm}^2 and V = 242\,\text{mm}^3 \tag{3.4}$$

3.2.1 Core Loss Calculation

The Steinmetz parameters K_{fe} , α and β are found for 100 °C rise in temperature from the manufacturer's website. The flux linkage, λ is calculated based on the converter simulation, which is also used to calculate the magnetic flux density B as:

$$B = \frac{\lambda}{NA_w} \qquad N \text{ is the transformer turns ratio} \tag{3.5}$$

The core loss calculation is performed using Improved Generalized Steinmetz Equation (iGSE) given by Eq. (3.6).

$$P_{fe} = \frac{k_i\,(\Delta B)^{\beta-\alpha}}{T_s}\sum_m \left|\frac{B_{m+1} - B_m}{t_{m+1} - t_m}\right|^{\alpha}(t_{m+1} - t_m) \tag{3.6}$$

where

$$k_i = \frac{K_{fe}}{2^{\beta+1}\pi^{\alpha-1}\left(0.2761 + \frac{1.7061}{\alpha+1.354}\right)} \tag{3.7}$$

Here, B_m is the flux density at time t_m, and ΔB is the peak-to-peak flux density.

3.2.2 Winding Loss

To estimate the winding loss, dc and ac winding resistances are found as follows:

$$A_{cu,pri} = t_{cu}w_{pri} \qquad \text{and} \qquad A_{cu,sec} = t_{cu}w_{sec} \tag{3.8}$$

$$R_{dc,pri} = \frac{\rho MLTn_l}{A_{cu,pri}} \qquad \text{and} \qquad R_{dc,sec} = \frac{\rho MLTn_l}{A_{cu,sec}} \tag{3.9}$$

where, t_{cu} is the thickness of the copper trace, A_w cross-sectional area of the copper trace, trace width of individual turn of primary winding, w_{pri} and secondary winding, w_{sec} is calculated as:

$$w_i = \frac{\left[\frac{C_{ww}}{2} - (n_l + 1)\, s\right]}{n_l} \tag{3.10}$$

Here, n_l is the number of turns per layer of the winding and$i$ corresponds to either primary or secondary winding.

The overall winding loss is then calculated as shown in Eq. (3.11). All winding losses are calculated at 100 °C.

$$.P_{winding_i} = R_{dc_i} \left(\frac{\varphi_k}{n_l^2}\right) \left[\left(F_i^2\,(h) + F_i^2\,(0)\right) G_1\,(\varphi_k) - 4F_i\,(h)\, F_i\,(0)\, G_2\,(\varphi_k)\right] \tag{3.11}$$

Here, k is the harmonic number, and

$$\varphi_k = \frac{t_{cu}}{\delta_k} \qquad \text{and} \qquad \delta_k = \sqrt{\frac{\rho}{2\pi\mu_0 f_k}} \tag{3.12}$$

$$G_1\,(\varphi_k) = \frac{\sinh\,(2\varphi_k) + sin(2\varphi_k)}{\cosh\,(2\varphi_k) - cos(2\varphi_k)}$$

$$G_2\,(\varphi_k) = \frac{\sinh\,(\varphi_k)cos(\varphi_k) + cosh(\varphi_k)sin(\varphi_k)}{\cosh\,(2\varphi_k) - cos(2\varphi_k)} \tag{3.13}$$

The results are shown in Table 3.1. Due to the simplicity of the 12 - layer design with only 2 turns per layer and fewer losses in the 10 µH design, the 12 - layer 10 µH design is selected.

The above loss analysis is performed in MATLAB. The air-gap and fit are verified in ANSYS PEMag by characterization of the transformer for some of the designs shown in Table 3.1. The vertical and horizontal fits of these designs are shown in Fig. 3.3 with a detailed calculation of the stack-up for different copper thicknesses.

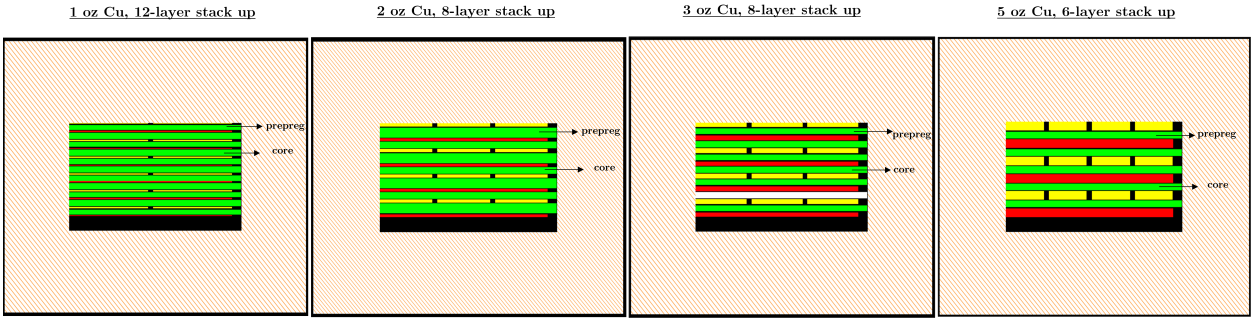
2-D finite element analysis is performed on the 12 - layer design with an air-gap of 0.262 mm. The losses obtained at $f_{sw} = 200$ kHz through the finite element analysis are tabulated in Table 3.2 and fringing observed due to the introduced air-gap is illustrated in Fig. 3.4.

Table 3.1: Predicted transformer total loss for different types of cores and a magnetising inductance of 10 µH and 4 µH.

Design	$L_m = 4\,\mu H$ (W)	$L_m = 10\,\mu H$ (W)
2-layer, 1 oz	15.256	3.782
2-layer, 2 oz	7.768	1.996
2-layer, 3 oz	5.342	1.419
2-layer, 4 oz	4.226	1.154
2-layer, 5 oz	3.666	1.02
4-layer, 1 oz	6.931	1.793
4-layer, 2 oz	3.585	0.995
4-layer, 3 oz	2.501	0.738
4-layer, 4 oz	2.003	0.619
4-layer, 5 oz	1.752	0.559
6-layer, 1 oz	4.553	1.225
6-layer, 2 oz	2.39	0.71
6-layer, 3 oz	1.69	0.543
6-layer, 4 oz	1.367	0.466
6-layer, 5 oz	1.206	0.428
8-layer, 1 oz	3.419	0.767
8-layer, 2 oz	1.821	0.573
8-layer, 3 oz	1.303	0.45
12-layer, 1 oz	2.319	0.692

Table 3.2: Predicted losses for the 12 - layer planar transformer design through 2 - D analysis in ANSYS Maxwell.

f_{sw} (kHz)	Core Loss (W)	Copper Loss (W)	Total Loss (W)
200	0.110	0.732	0.842



(a)

ELP14/3.5/5 + I14/1.5/5					
detailed thickness calculations based on multi-layer stackup					
thickness per trace (oz)	1oz	2oz	3oz	5oz	
thickness per trace (mm)	0.03556	0.07112	0.10668	0.17780	
window height (mm)	1.748	1.748	1.748	1.748	*considering 8% tolerance in window height*
no of layers	12	8	8	6	
total Cu thickness	0.42672	0.56896	0.85344	1.0668	
total insulation thickness (core + prepeg)	1.32128	1.17904	0.89456	0.6812	
prepeg layers	6	4	4	3	
cores	5	3	3	2	
core thickness (for 1.6 mm thick PCB)	0.13	0.13	0.13	0.13	*since window height is 1.9 mm, we can only chose 1.6 mm pcb thickness*
total core thickness	0.65	0.39	0.39	0.26	
total prepeg thickness	0.67128	0.78904	0.50456	0.4212	
per layer prepeg thickness	0.11188	0.19726	0.12614	0.1404	

(b)

Figure 3.3: Vertical and horizontal planar transformer cross-section for different designs (a) ANSYS PEMag (b) Calculations

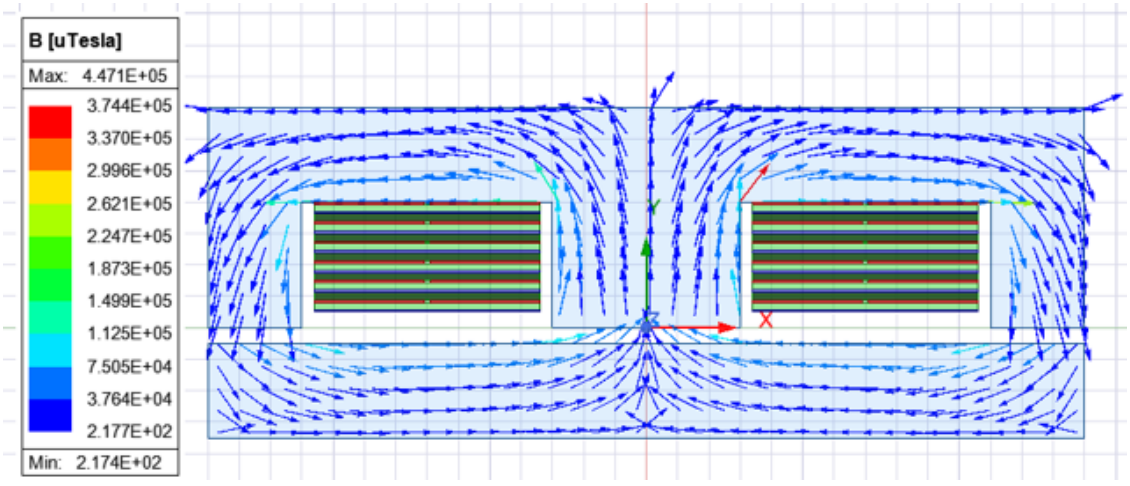


Figure 3.4: Fringing of magnetic flux density observed due tot air-gap of 0.262 mm.

Chapter 4

Simulation and Experimental Validation

4.1 12 V to 1 V direct forward converter efficiency

The loss-budget analysis is performed by varying load from 0.1 A to 50 A with different numbers of parallel secondary side switches. Figure 4.1 provides a comparison of predicted efficiency as a function of load for two, three, or four secondary switches connected in parallel. For the four-switch case, a loss budget and the predicted efficiency are shown in Table 4.1 for the peak-efficiency point and the full-load point. For the 48-to-1 V, 200 A SDF converter of Fig. 1.3 efficiency remains the same as in Fig. 4.1 except that the load is multiplied by a factor of 4.

Table 4.1: Predicted loss budget for the peak-efficiency point and the full-load point, for the case when four switches are connected in parallel on the secondary side.

f_{sw} (kHz)	Load (A)	Switches Loss (W)	Gate Drivers Loss (W)	Core Loss (W)	Winding Loss (W)	Total Loss (W)	η (%)
200	21	0.25	0.12	0.19	0.75	1.17	93.9
200	50	1.20	0.12	0.19	2.14	3.36	91.8

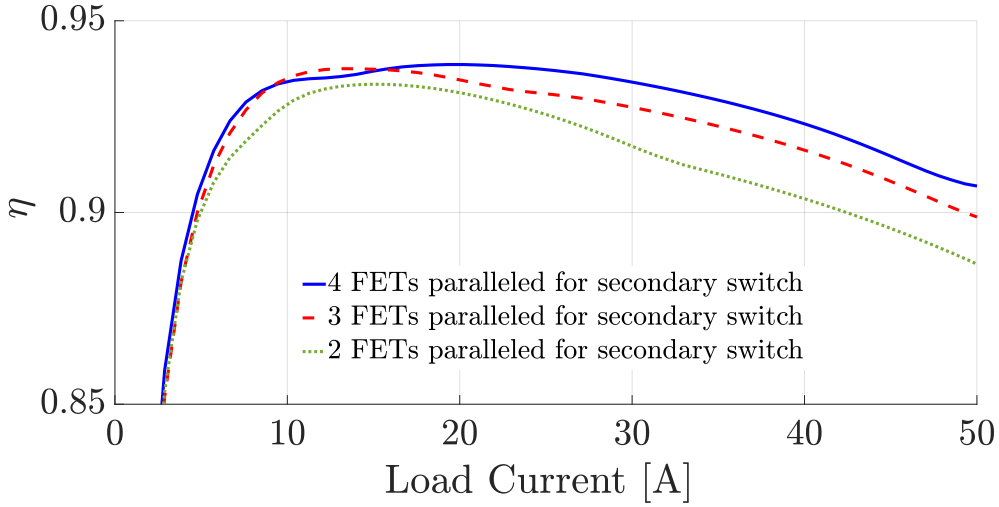


Figure 4.1: Predicted efficiency as a function of load current for the 12 −to-1 V active-clamp direct forward (DF) converter module, for different parallel combinations of the secondary switch.

4.2 Experimental characterization of the 12-layer planar transformer

Characterization of the 12 - layer planar transformer is performed on the Bode-100 analyzer using an impedance box 2-port measurement.

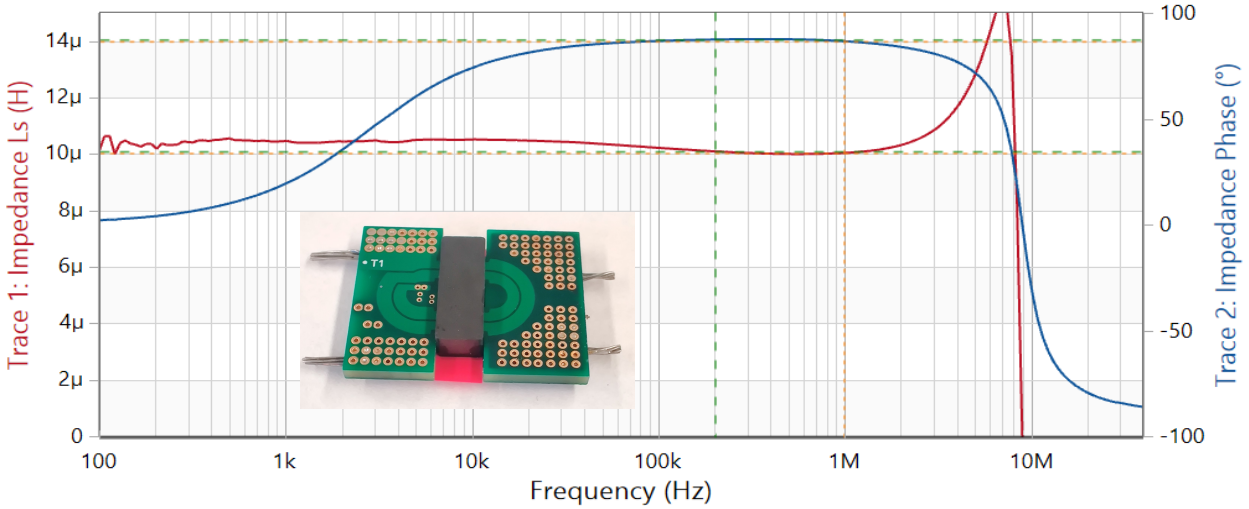


Figure 4.2: Impedance measurement of the planar transformer using Bode 100 network analyzer: $L_{\mathrm{m}} = 10.1\,\mu\mathrm{H}$ and $L_{\mathrm{lk}} = 349\,\mathrm{nH}$ (short-circuited secondary).

The magnetizing inductance is measured by connecting the primary side terminals to

the impedance box, with the secondary terminals left open after calibration is completed. This measurement is shown in Fig. 4.2. A magnetizing inductance of $L_m = 10.1\,\mu\text{H}$ is observed in the measurement. The leakage inductance, $L_{lk} \approx 349\,\text{nH}$, is measured in the same setup with the secondary terminal short-circuited. This measurement also includes some minimal leakage associated with the soldered multi-strand wire terminals to facilitate measurement.

4.3 Hardware Testing of 12 V to 1 V direct forward converter prototype

Experimental testing is performed on a 12 V to 1 V. The prototype is shown in Fig. 4.3. A Texas Instruments TMDSCNCD28379D Delfino control card is used to provide the required control signals to the gate drivers for PWM generation. A dead time of 80 ns is programmed to ensure that the reverse conduction period of the GaN FETs are minimized and zero-voltage switching is achieved on both the primary side switches. This converter is operated in open loop as the steady state of the direct forward converter is majorly dependent on the turns ratio of the transformer.

The equivalent circuit that was tested is shown in Fig. 4.4a and Fig. 4.4b shows V_{sec} and V_{sw} are observed against the control signals G and G'. There is complementary switching performed between the clamp FET Q_c and the primary-side main FET Q_{p1}. Zero-voltage switching is obtained for both the primary side FETs at no load, as shown in 4.5. As can be seen in this figure, the $V_{sw} = \dfrac{V_{IN}}{D'} \approx 64\,\text{V}$ and the $V_{sec} = \dfrac{V_{sw}}{12} \approx 4.5\,\text{V}$.

From Figs. 4.5a and 4.5b, it can be seen that the control signal G used to turn on the primary side FET, Q_{p1} is enabled after the switch node voltage, V_{sw}, drops to zero. The programmed dead time of 80 ns is seen at the turn-on and turn-off instant of these switching waveforms.

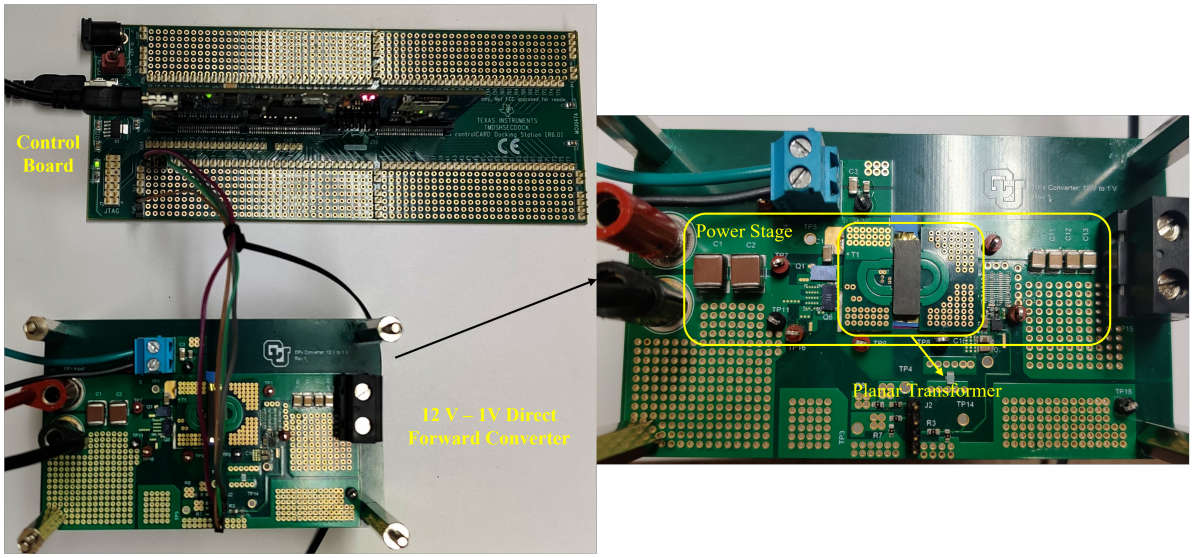


Figure 4.3: 12 V to 1 V PCB Prototype.

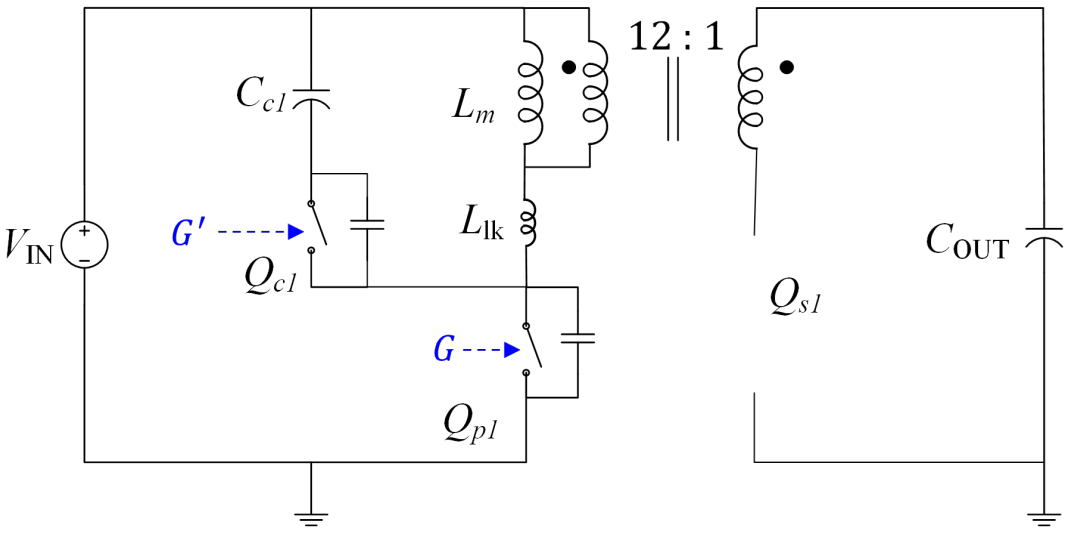
4.3.1 Challenges faced during experimental validation

Hand soldering of secondary-side GaN FETs turned out to be very challenging due to their very small footprint, which is shown in Fig. 4.6. The pad-to-pad clearance is $\approx 200\,\mu m$. Thus. only the primary side circuit was tested in this hardware testing.

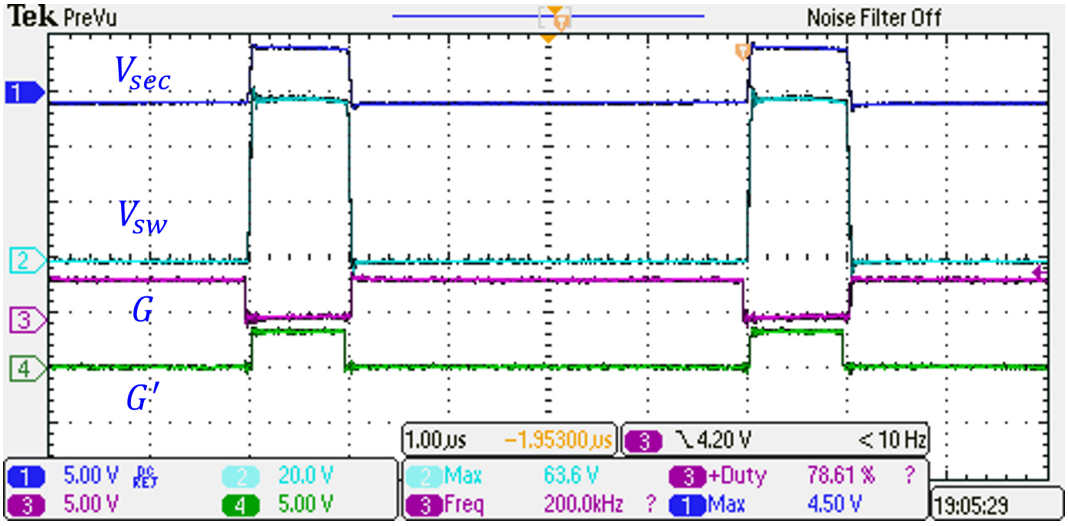
In the next revision, the secondary-side GaN FET will be replaced with a Silicon MOSFET having similar current and voltage ratings and a closer distribution of $r_{ds_{on}}$ and C_{oss} when compared with the current EPC2066 GaN FET. Further testing will be performed on the board later, as the secondary GaN FET is soldered, with different load conditions to characterize efficiency by experiments.

4.4 Simulation of 48 V to 1 V Stacked Direct Forward Converter

A phase-shifted 48 V to 1 V system simulation is performed to validate the stacked converter approach for a load of 200 A. In this system, four direct forward converter modules are connected in input-series output-parallel configuration, as shown in Fig. 1.3. In this simulation, the output capacitor is $C_{out} = 1500\,\mu F$ and a resistive load is $5\,m\Omega$.



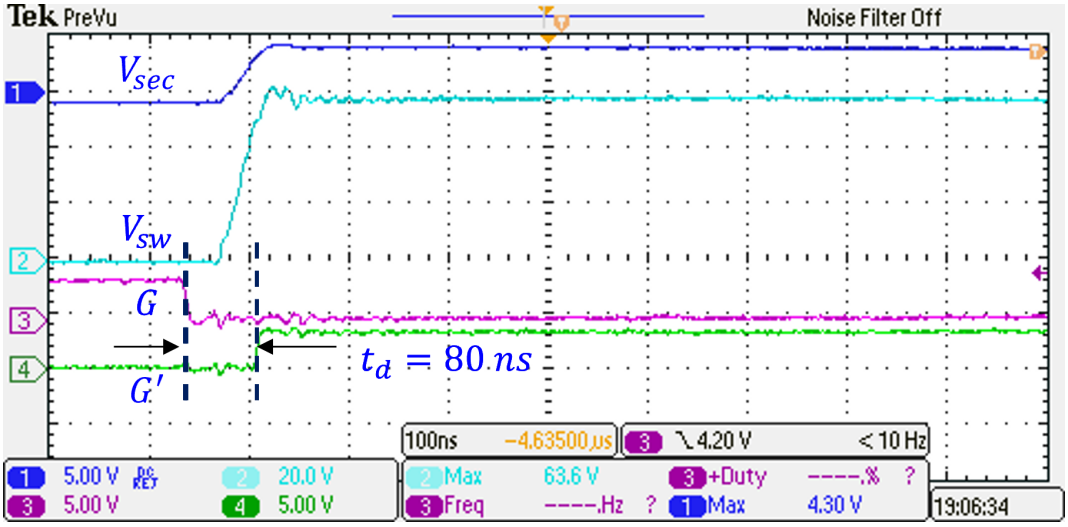
(a)



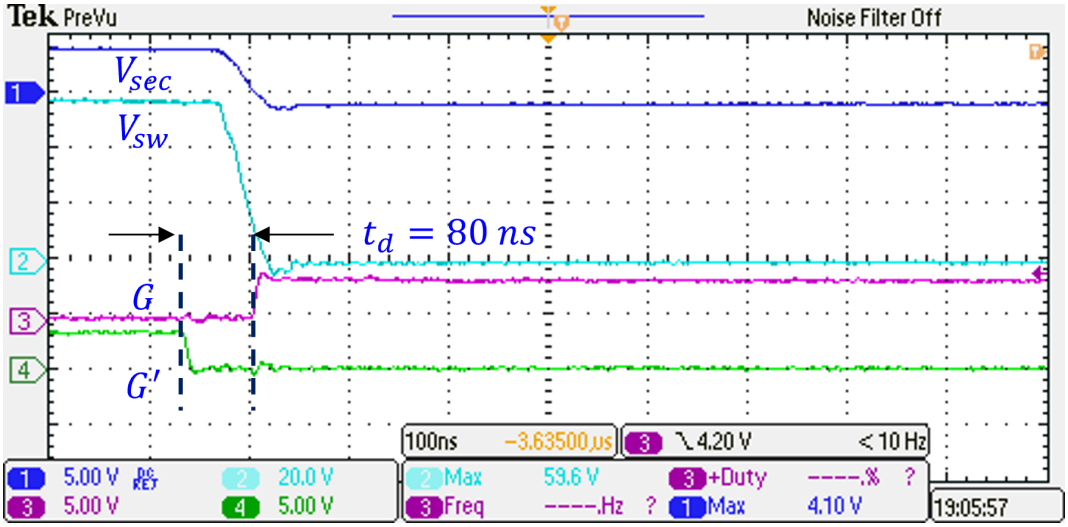
(b)

Figure 4.4: Experimental Validation: (a) Test circuit used for experimental validation (b) V_{sw} and V_{sec} waveforms

The steady-state waveforms obtained by simulation are shown in Fig. 4.7. The same dead time, t_d, of 80 ns is sufficient to achieve zero-voltage switching. Due to the use of four phases, the frequency of the switching ripple seen in the output current and voltage is $4f_{sw}$. The amplitude of the ripple is reduced four times making this ripple very small. The predicted $V_{sw} = \dfrac{V_g}{4D'}$ just as per analytical calculations, and the secondary side voltage



(a)



(b)

Figure 4.5: Experimental validation V_{sw} and V_{sec} waveforms: (a) Primary main FET turn off instant, (b) Primary main FET turn on instant

V_{sec} is the switch-node voltage scaled by the turns ratio, as expected. The high-frequency ringing observed in the D' interval is due to the resonance between L_{lk} and C_{eq}, as explained in Chapter 2, Section 2.2.

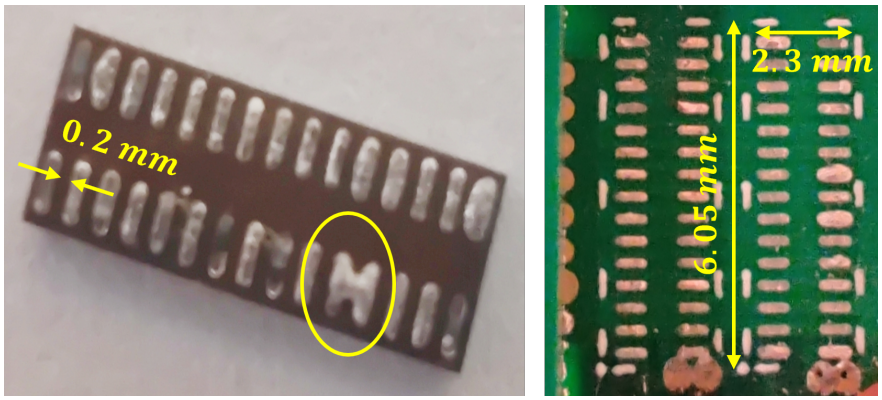


Figure 4.6: EPC2066 GaN FET Footprint.

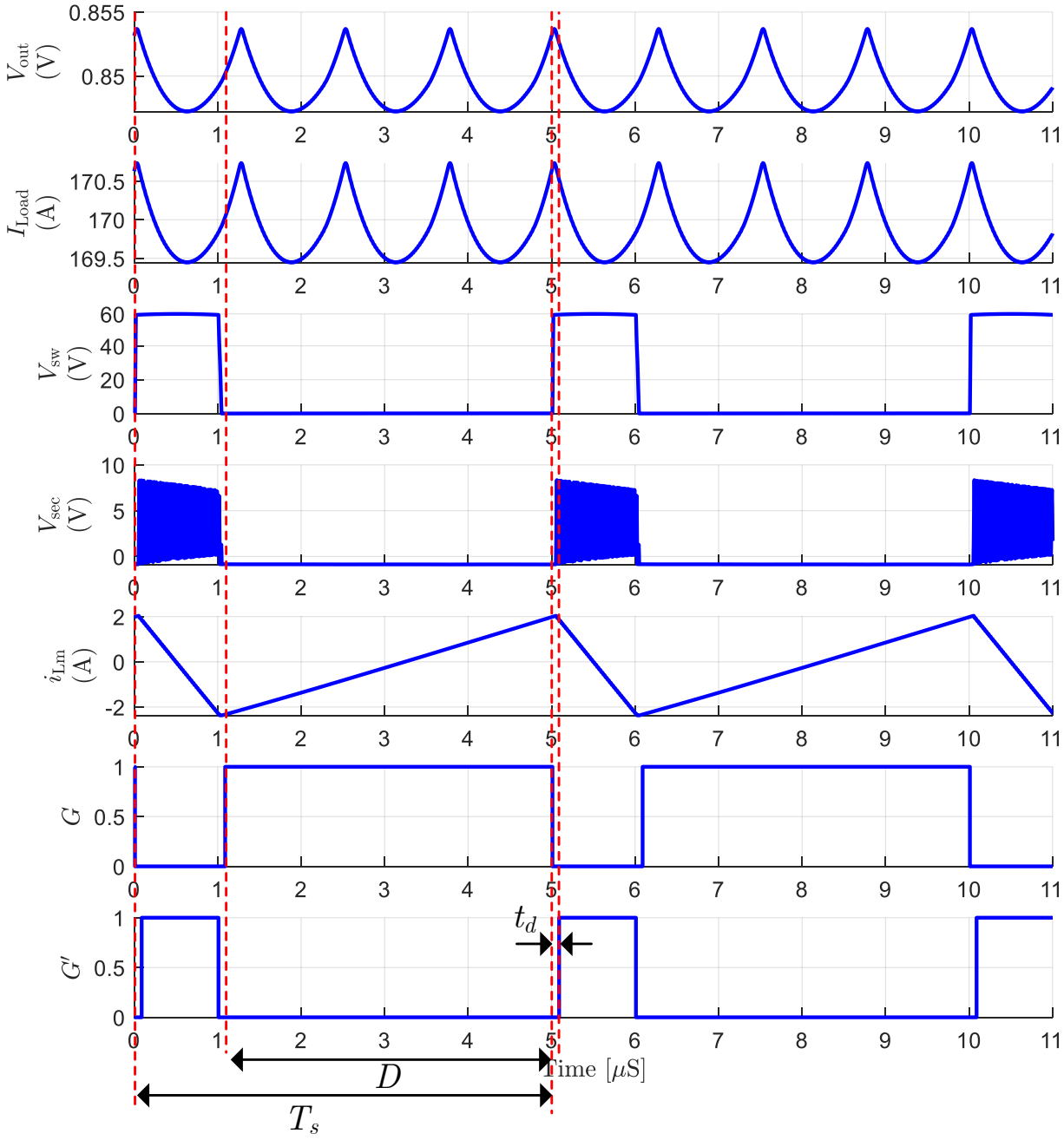


Figure 4.7: Simulation of a phase shifted 48 V to 1 V stacked direct forward converter.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

In this thesis, the design, modeling and loss analysis of 48 V to 1 V Stacked Direct Forward (SDF) converter is performed and validated by simulation. A detailed loss model is developed and analyzed for low-voltage planar transformers and the 12 : 1 transformer design is selected. This design is experimentally validated through characterization using the Bode 100 analyzer. This planar transformer is used in the 12 V to 1 V Direct Forward (DF) converter module. Finally, an experimental validation of 12 V to 1 V module is performed and ZVS operation of the primary side switches is validated with the programmed dead time, $t_d = 80$ ns, at no load condition. It is also verified that the active clamp successfully clamps the switch voltage to $\frac{V_{IN}}{D'}$, thus reducing the switch voltage stress.

5.2 Future Work

From the results and challenges faced in the implementation of the 12 V to 1 V direct forward converter, the following changes will need to be addressed in future revisions of the converter:

(1) **Changing the transformer design from the 12−layer implementation to the 8−layer design.**

As can be seen in Table 3.1, the 8 - layer 3 oz design has less loss by ≈ 0.39 W. With negligible switching losses and minimized conduction losses, the converter efficiency is mostly dictated by the efficiency of the transformer. Thus, minimizing losses in the transformer design can give a better efficiency advantage at the light and full load.

(2) **Replacing the secondary side EPC2066 GaN FETs with Si-based MOSFETs with relatively closer distribution of $r_{ds_{on}}$ and C_{oss}.**

EPC2066 switches have a very small footprint with very small pad-to-pad clearance. This causes difficulty in soldering the GaN FETs without possible drain-source shorts. Thus, there is a need to choose a FET with a footprint that would make assembly easier. The primary criterion for this switch selection is the lower value of $r_{ds_{on}}$. A trade off of selecting a small $r_{ds_{on}}$ is a higher C_{oss}. However, this capacitance for Si-based MOSFETs is much higher than for EPC2066. A larger parasitic capacitance results in needing a larger magnetizing inductance or higher dead time to ensure soft switching. It also leads to relatively larger gate driver loss, as the gate charge of the MOSFET is relatively larger than that of the GaN FET.

(3) **Minimising the leakage of the planar transformer to under 1%.**

Minimizing the leakage is critical when the 48 V - 1 V transformer is designed, as the output ripple has some lower frequency harmonics caused by the resonance of the leakage inductance and the equivalent parasitic capacitance. While a larger leakage inductance facilitates ZVS, it also causes additional losses in the transformer, which leads to lower efficiency. Thus, there is a need to better control the leakage inductance of the planar transformer.

This concludes the anticipated design and analysis steps based on the first revision of the 12 V to 1 V direct forward converter. The next steps following this analysis include:

(1) **Design and experimental validation of a second revision of the** 12 V **to** 1 V **direct forward converter** with reduced leakage inductance and secondary side FET changed to a Si-MOSFET with relatively low $r_{ds_{on}}$.

(2) **Developing an electro-thermal finite-element simulation model of the planar transformer.**

This analysis model can help us to understand the transformer parameters such as dc resistance and leakage inductance as functions of different design and layout parameters including air gap and winding layout. In addition, the model can also help us understand the transformer loss as a function of the rise in temperature and the thermal management used.

(3) 48 V **to** 1 V **Stacked Direct Forward Converter design and its experimental validation.**

(4) **Investigation of control strategies for the** 48 V **to** 1 V **stacked direct forward converter** to address load regulation and input bus voltage variation, which can be as wide as 30 V to 60 V.

Bibliography

[1] Z. Yicheng, G. Ting, E. Nathan, H. Logan, and P.-P. Robert, "A 500-A/48-to-1-V switching bus converter: A hybrid switched-capacitor voltage regulator with 94.7% peak efficiency and 464-W/in^3 power density," in **IEEE APEC 2023**.

[2] E. Youssef, B. Jaeil, R. Kaladhar, G. Houle, D. Jonathan, D. Vivek, J. Shuai, K. Harish, L. Xin, S. C. R., and C. Minjie, "Mini-LEGO: a 1.5-MHz 240-A 48-V-to-1-V CPU VRM with 8.4-mm height for vertical power delivery," in **IEEE APEC 2023**.

[3] W. Ping, G. David, A. Stephen, and C. Minjie, "Msc-pol: An ultra-thin 220-A/48-to-1-V hybrid GaN-Si CPU VRM with multistack switched capacitor architecture and coupled magnetics," in **IEEE APEC 2023**.

[4] J. Baek, Y. Elasser, K. Radhakrishnan, H. Gan, J. P. Douglas, H. K. Krishnamurthy, X. Li, S. Jiang, C. R. Sullivan, and M. Chen, "Vertical stacked lego-pol cpu voltage regulator," vol. 37, no. 6, 2022, pp. 6305–6322.

[5] L. Xin and L. Qiang, "Multiphase half-bridge current-doubler rectifier: A 93.1%-efficiency single-stage 48v voltage regulator with 1.04 kw/in^3 power density," in **IEEE APEC 2023**.

[6] M. Ahmed, C. Fei, F. C. Lee, and Q. Li, "High-efficiency high-power-density 48/1V sigma converter voltage regulator module," in **IEEE APEC 2017**, pp. 2207–2212.

[7] J. Cobos, A. Castro, García-Lorenz, J. Cruz, and Cobos, "Direct power converter -DPx- for high gain and high current applications," in **IEEE APEC 2022**, pp. 1016–1022.

[8] B. Majmunović and D. Maksimović, "400–48-V stacked active bridge converter," **IEEE Transactions on Power Electronics**, vol. 37, no. 10, pp. 12 017–12 029, 2022.

[9] G. Ting, Z. Yicheng, and P.-P. Robert, "A regulated cascaded hybrid switched-capacitor converter with soft-charging and zero voltage switching for 48-to-12-V applications," in **IEEE APEC 2023**.

[10] V. Li, M. H. Ahmed, Q. Li, and F. C. Lee, "Modeling and control of sigma converter for 48v voltage regulator application," in **IEEE APEC 2018**, pp. 1199–1204.

[11] J. Zhu and D. Maksimovic, "48 V-to-1 V transformerless stacked active bridge converters with merged regulation stage," in **2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL)**, 2020, pp. 1–6.

[12] D. Costinett, D. Maksimovic, and R. Zane, "Design and control for high efficiency in high step-down dual active bridge converters operating at high switching frequency," **IEEE Transactions on Power Electronics**, vol. 28, no. 8, pp. 3931–3940, 2013.