Analysis and Design of High Efficiency, High Conversion Ratio, DC-DC Power Converters

by

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Analysis and Design of High Efficiency, High Conversion Ratio, DC-DC Power Converters

Thesis directed by Prof. Regan Zane and Prof. Dragan Maksimović

In 2010, more than 2% of all electricity generated in the United States was used to power data centers. Estimates indicate that as many as 85% of data centers constructed prior to 2006 expend more than three times as much electric power on cooling and inefficient conversion than on powering the server hardware itself. One key contributor to the poor energy efficiency in these data centers is power distribution architecures characterized by many cascaded and inefficient power converters. Though the architectures in these data centers vary greatly, they each stand to benefit significantly from a well-designed, highly efficient power converter capable of stepping down the high DC voltages generated in AC rectification to the low DC voltages capable of being distributed across the server motherboard. The design of this converter has unique requirements for the power electronics designer, including constraints on form factor, efficiency, and control. This thesis considers the requirements imposed by the data center application to motivate the analysis and design of high efficiency, high step-down, high frequency DC-DC converters for data centers and other applications.

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Power Converters in Data Centers

In 2011, mankind created 1.2 trillion gigabytes of new electronic data [1]. All of this content made use of large, centralized data centers at some point for its creation, storage, transmission, or distribution. The increasing integration of personal computing into society has spurred the rapid expansion of data centers, with its growing importance reflected by the increased electronic power consumed by data centers in the United States and worldwide. From Fig. 1.1, nearly 80 TWh, or 2.2% of all electricity generated in the US in 2010, was consumed in data centers [2]. In recent years, continued advancements in energy-efficient computing hardware and algorithms, data center facility design, and air conditioning efficiency, among others, have been spurred by public and government interest in the area. However, these advancements are often outpaced by growing demand for online services; future projections predicting as much as 20% annual growth in data center energy consumption in future years.

1.1 Power Consumption in Data Centers

The magnitude of energy consumption associated with these computing operations becomes particularly problematic when the end use of power within the data center is considered. Though most data centers are constructed individually and according to custom specifications, the average data center in the US uses less than half of the facility input power to perform the computations intended in its application. The remaining power is dissipated on infrastructure components required to operate the computational hardware; cooling, humidity regulation, and power conversion

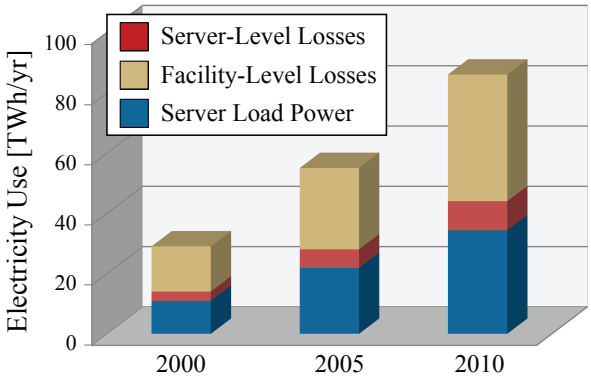


Figure 1.1: Data center electricity use in the United States

and conditioning are the principle components. The relative proportion of energy consumed in infrastructure in a given data center is often addressed with an equivalent figure-of-merit (FOM) known as the power-usage effectiveness (PUE)

$$\text{PUE} = \frac{\text{Total Facility Power}}{\text{IT Equipment Power}} \ . \tag{1.1}$$

For the average data center currently operating in the US, PUE > 2, and PUE > 3 for a majority of data centers built prior to 2006, many of which remain in operation today [3–5].

Unfortunately, this FOM does not provide a full picture of energy use, as there are additional power conversion and cooling stages integrated into the IT equipment itself. This fact is occasionally addressed with a second FOM, the server power-usage effectiveness (SPUE),

$$\text{SPUE} = \frac{\text{Total Server Input Power}}{\text{Computation Hardware Power}} \ . \tag{1.2}$$

Most modern servers have SPUE ≈ 1.6 with state-of-the-art servers as low as SPUE $= 1.2$ [6]. Taking both FOMs into account, the relative proportion of power use for different purposes is shown in Figure 1.3 for an average data center [7].

The presence of this large degree of power consumption prior to load delivery is better understood by considering the power distribution architecture within a standard data center, as shown in Fig. 1.4. It can immediately be seen that the distribution architecture contains many, cascaded power conversion stages. These stages are necessary to convert the high voltage AC power sup-

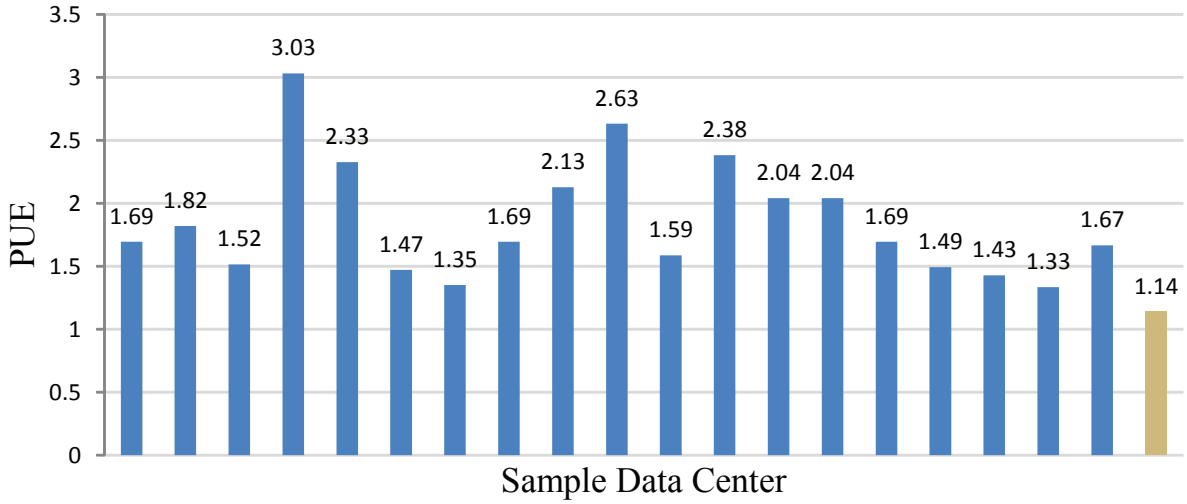


Figure 1.2: PUE values of various data centers included in [5]. The rightmost bar represents Google's current best-in-class data center.

plied to the building by the external transmission systems to the low-voltage DC power required by the server hardware, including processors, memory, and disk drives (CPU, RAM, and HDD, respectively). Additionally, to maintain reliability of the data center in the presence of minor fluctuations in power supplied from the grid, nearly all data centers require uninterruptable power supply (UPS) systems, which are often DC voltage buses with attached battery or flywheel energy storage. The UPS unit allows the data center to continue operation even in the presence of temporary loss-of-power instances, but require that the distribution architecture contain additional conversion stages to convert from the input AC-to-DC at the batteries, back to AC at traditional levels for local distribution. This AC distribution is then rectified by an AC-to-DC converter at the server rack level, and subsequently stepped down by a DC-to-DC converter to a low-voltage intermediate bus, often 48 V. This DC bus is stepped down again on the server itself to 12 V used by the motherboard, and further dropped to the tightly regulated voltage required by each component through voltage regulation modules (VRMs) and point-of-load (POL) converters at the location of the computational hardware.

The high number of power conversion stages present an issue which must be addressed in the

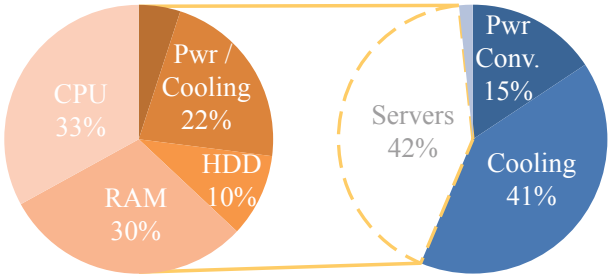


Figure 1.3: Breakdown of approximate usage of electricity in data centers

design of the distribution scheme. Because so many power conversion stages operate in series, even highly efficient individual converters will result in poor overall end-to-end system efficiency where the efficiency of each stage is multiplied. However, this same issue presents great opportunity for benefit from small decreases in power loss at points close to the server load. The resulting cascade of reduced losses is diagrammed in Fig. 1.5. For a representative data center as described in [8], a savings of 1 W at the final DC-DC converter level results in additional savings at each of the previous conversion and cooling stages due to the reduced power provided, eventually resulting in 2.38 W of energy savings for the facility. Thus great benefit can be gained from reduced power consumption or power loss at latter stages in the distribution.

1.2 Data Center Distribution Architectures

Though large benefits may be accrued from small increases in efficiency in the power distribution architecture of Fig. 1.4 due to the redundant conversion stages, even greater benefit is obtainable from the elimination of conversion stages. Such a task can be accomplished through several unique modifications to the distribution architecture, many of which focus on the inefficiencies inherent in the UPS system; a few such modifications are addressed in the following sections

1.2.1 Partial Conversion UPS

Reliable and instantaneous UPS functionality is necessary for commercial data centers, which generate profit only through reliable and continuous operation and availability. Average downtime

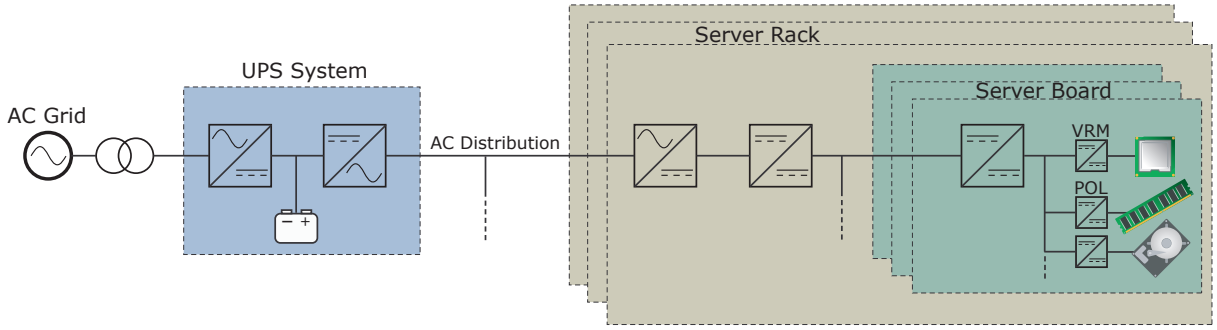


Figure 1.4: Intermediate bus architecture for power distribution in data centers

costs for data centers have been calculated as high as $11,000 per minute of downtime [9], motivating the inclusion of backup and redundancy wherever possible. From an efficiency standpoint, however, the inclusion of a UPS which must process 100% of facility power through two conversion stages constitutes a significant detriment for a system which only operates during relatively uncommon line voltage transient events.

Alternate UPS architectures, known as ECO-mode or line-interactive UPS devices offer one alternative to traditional double-conversion modules. These devices work by processing little or no power during normal operation of the data center, but remain active in order to minimize response time in the event of a power transient. A system using a delta converter is shown in Fig. 1.6. However, such converters are more difficult to parallel for necessary redundancy in the system, and have a higher initial investment and slower response time than traditional double-conversion stages.

1.2.2 On-Board UPS

A second strategy, made popular by Google, employs low-voltage, distributed battery backups rather than a single high-voltage facility-level battery bank. The architecture, shown in Fig. 1.7 prevents the need for second conversion to return to an AC distribution by including a small, 12 V battery on each server board directly, with UPS functionality incorporated at the same level. The approach has the added benefit of producing extremely high PUE figures for data centers which

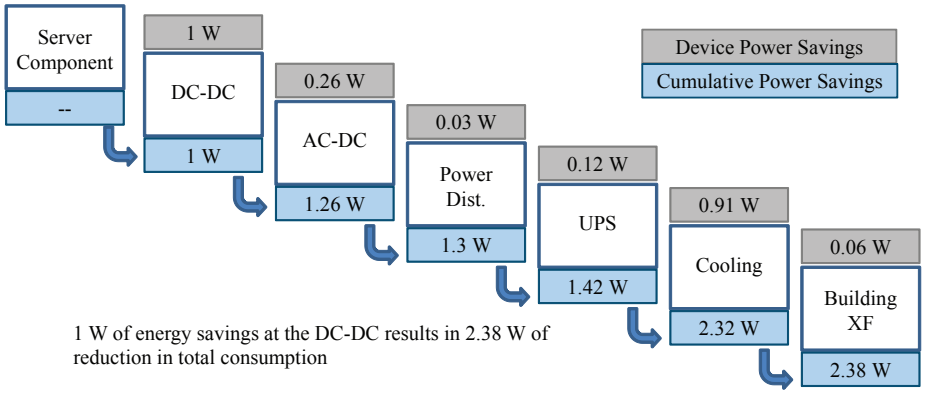


Figure 1.5: The cascading effect of reduced losses near the load in a server power distribution [8].

employ this approach, as nearly all power conversion happens at the server rack level or below, which is not taken into account unless SPUE is also considered, resulting in the extremely low PUE figure for google data centers as demonstrated in Fig. 1.2.

The system is difficult to implement, however, as the capital investment is increased due to the added cost of the distributed batteries, and the added cost and complexity associated with implementing a custom solution for the server motherboards themselves may be prohibitive for smaller data centers and companies.

1.2.3 High Voltage DC Distribution

Finally, the proposed high-voltage DC distribution (HVDC) architecture of Fig. 1.8 has generated considerable interest in recent years [10, 11]. The HVDC data center eliminates power conversion stages associated with the local AC distribution by instead wiring the entire data center for the distribution of a high voltage DC bus (commonly in the range of 200-400 V), which can be tied directly to the battery backup at the UPS. Due largely to the elimination of additional power converters, the HVDC approach promises improved efficiency, increased reliability, lower cost, and decreased overall footprint [12–18]. Additionally, the HVDC distribution facilitates the incorporation of renewables, such as local photovoltaic power sources, by permitting their direct connection to the DC bus.

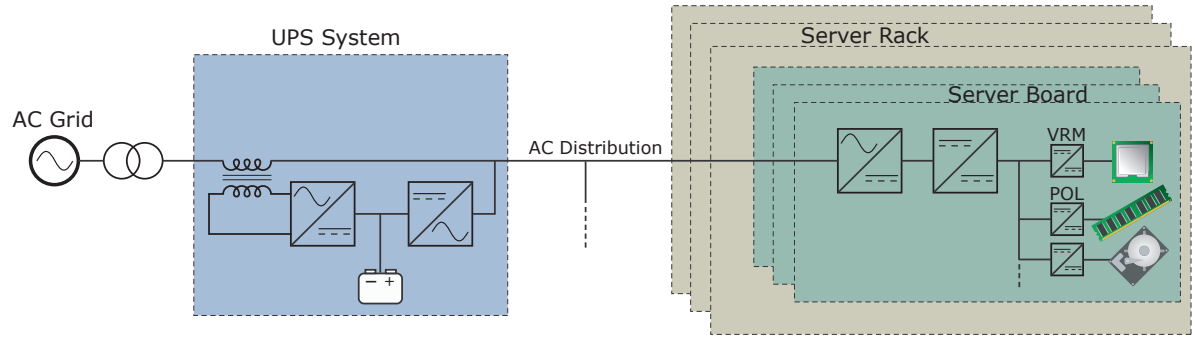


Figure 1.6: Intermediate bus architecture using a delta-conversion (eco-mode) UPS

Issues cited with the adoption of HVDC distribution architectures center largely on the deficiency or absence of established standards and commercial equipment necessary to practically and reliably implement the systems. A subset of these issues are listed in Table 1.1. However, the impact of these issues is increasingly mitigated, as continued interest in the HVDC distribution inevitably leads to the development of appropriate standards, and companies such as Hewlett-Packard and ABB have already begun releasing commercial HVDC-enabled equipment. Stemming from this interest, there have already been a number of DC data centers and office buildings constructed, including most recently a 1 MW, 380 Vdc data center in Zurich Switzerland. This project, completed in May of 2012, is the largest and highest power HVDC data center to date; its constructors claim that the facility operates with 10% higher efficiency, 15% lower investment costs, and a 25% smaller footprint than a comparable AC system.

The final point of contention relating to the adoption of HVDC in data centers concerns the efficiency of the high-to-low voltage step down conversion stage, often referred to as the "Front End" converter. In the DC distribution, this is commonly a DC-to-DC with input in the range of 400 Vdc and output near 12 Vdc, though these voltages have some variation between proposed systems and are potentially the subject of optimization [20]. However, in the AC distribution, the actually step-down can be handled much more simply with a transformer, and a separate rectifying stage converts AC-to-DC. Because the transformer is a passive device, it is capable of

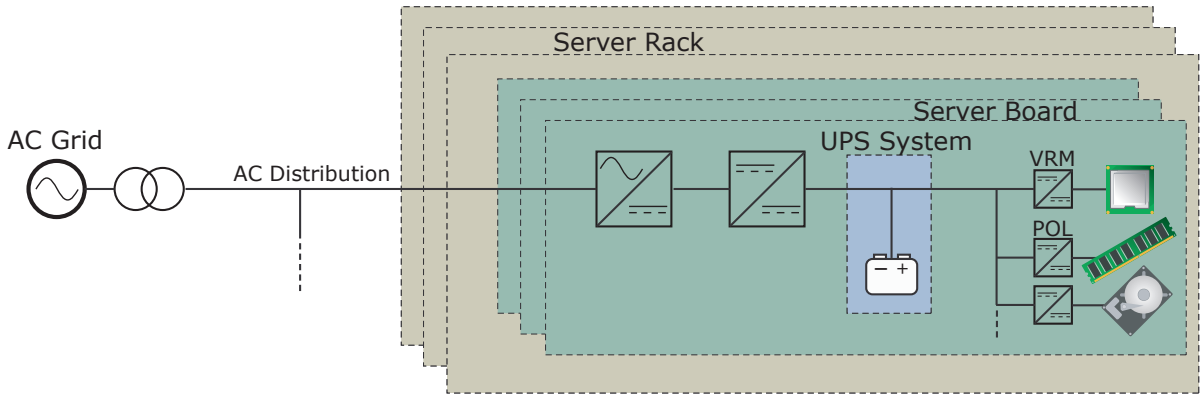


Figure 1.7: On-board UPS architecture used in Google data centers

implementing a large voltage step-down at very high efficiency. Due to saturation limits, however, a transformer alone is not appropriate for the HVDC system. Thus, the high step-down converter highlighted in Fig. 1.8 is the primary element in the distribution chain which is deemed as inferior to the corresponding element in the traditional AC distribution. However, if this converter could be designed to obtain very high efficiency, and be packaged in a form factor much smaller than an equivalent line-frequency AC transformer, even this final point of contention would be overcome.

1.3 Design of Front-End DC-DC Converters in Data Centers

Though the merit of the HVDC distribution is reliant upon the design of a high efficiency, high step-down DC-DC converter, it should be noted that all distribution architectures discussed in the previous section stand to benefit from the inclusion of such a converter. In all cases, there is a need to step down the high DC voltages associated with rectification of AC to the low voltages used by the server equipment at some stage in the distribution.

The remainder of this thesis is dedicated to the careful design and analysis of such a converter. Based on the proposed application, a number of unique characteristics and constraints on converter design are present and must be considered in the converter design. These characteristics are discussed in the remaining sections of this chapter, and summarized in Table 1.2.

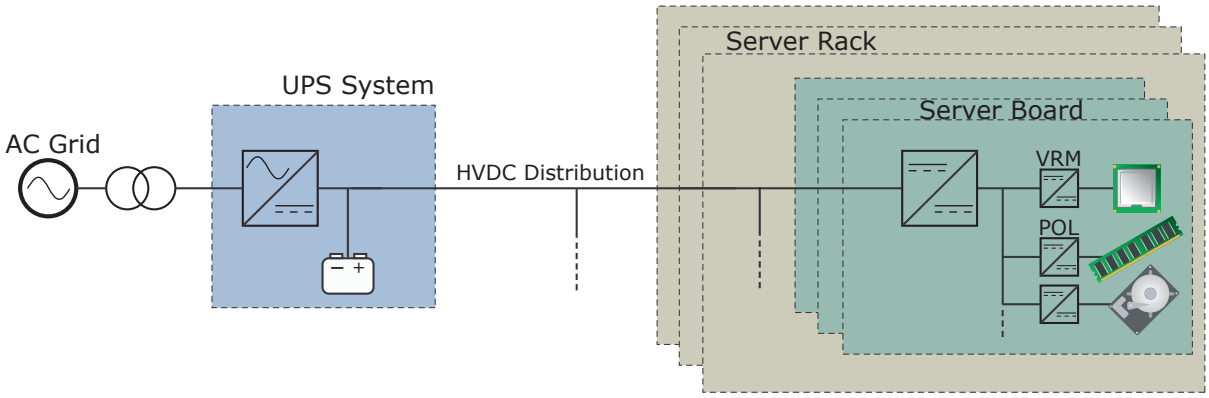


Figure 1.8: HVDC distribution architecture

1.3.1 Voltage Conversion Ratio

The most fundamental issue facing the design of candidate power converter topologies in the data center application is the very high step-down conversion ratio. The large disparity in voltage level between the HVDC bus and the 12 V bus present at the motherboard level should be bridged in a single step, to avoid the issue previously faced by multi-converter topologies. The resulting converter has, necessarily, a wide variety of considerations which must be made due to the presence of both low and high voltages, as well as high and low currents, at the respective ports.

1.3.2 Converter Size

Due to the high infrastructure cost and significant premium on space in the data center, it is desired to construct a converter of appropriate size such that it can be integrated directly onto the motherboard. In addition to reducing the footprint of the overall system, this will reduce the complexity and quantity of wiring and interconnections in the data center, thereby reducing cost and improving reliability.

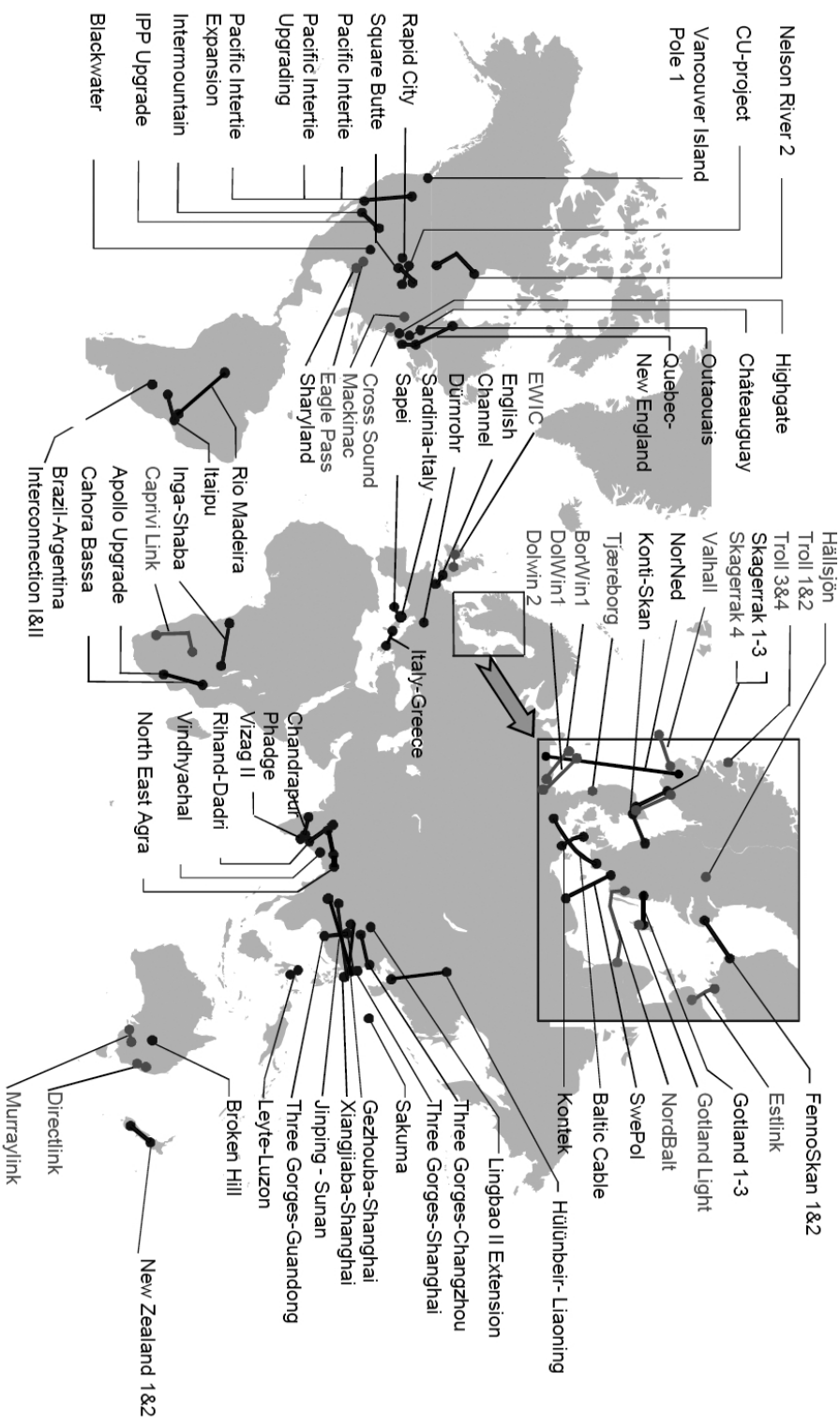


Figure 1.9: Current cites operating with HVDC distribution [19]

1.3.3 Converter Efficiency

In order to address the issues with the current AC, intermediate-bus power distribution architectures, it is necessary that any proposed solution achieve a significantly higher efficiency. In order to achieve this, the efficiency of the front-end converter must be maximized. Initial targets for this research include 98% peak power stage efficiency, and a fairly flat efficiency curve with respect to variations in operating power levels.

1.3.4 Converter Power Level

The output power required in the given application, with the front-end converter residing directly on the server motherboard when successfully constructed with small footprint, is relatively modest. Unlike standard systems in which the front-end converter may supply multiple servers, or even racks of servers, the proposed converter needs supply output power sufficient for only a single motherboard. Thus the application requires only output powers in the hundreds of watts, and initial design will assume an output power near 120 W.

1.3.5 Unregulated Operation

Examining the distribution architectures of Figs. 1.4, 1.6, 1.7, and 1.8 it is apparent that in all cases the low voltage bus which constitutes the proposed converter's output port is loaded only by further DC-DC converters, in the form of VRMs and POLs. It is therefore feasible to design

Table 1.1: Issues relating of the adoption of HVDC in data centers

Standards	Equipment
• Battery attachment method	• Cabling
• Bus voltage range	• Power converters
• Common grounding method	• Breakers
• Safety regulations	• Connectors
• Qualification criteria	

the front-end converter without strict requirements for regulation of the output voltage, as any variations in this bus voltage can be regulated out by the latter conversion stages. This manner of operation will be termed "unregulated", which indicates that the output voltage is not driven to a fixed DC value, though it may still be controlled in some manner; this includes both fixed conversion-ratio converters as well as those which dynamically adjust the output voltage in closed-loop. It is possible to design a converter with greater efficiency in the unregulated case [20,21], and the ability to have a dynamic output voltage reference will be analyzed and taken advantage of in the design of the front-end converter.

Summary

With renewed interest in optimization of power use in recent years, there is significant motivation for the assessment of alternatives to the traditional intermediate bus architecture, with the HVDC distribution at the forefront of potential alternatives. The case for HVDC is made on a number of factors, but is contingent upon the ability to design a highly efficient front-end converter which meets all application requirements. These requirements present a number of unique constraints on the design of traditional power electronic circuits, including constraints on conversion ratio, power levels, efficiency, and physical size of the converter, as well as exhibiting the potential for unregulated converter operation. Given these constraints, the remainder of this thesis will ad-

Table 1.2: Application Characteristics for DC-DC Converter in Data Centers

Requirement	**Justification**
Large voltage conversion ratio	Necessary to transfer power between approximately 400 Vdc input and 12 Vdc output
Small footprint	Necessary to allow the integration of converter directly onto server motherboard, further reduce data center footprint
High efficiency	Needed to maximize system efficiency; ensure HVDC is superior to AC distribution systems
Modest power level	For converter integrated on motherboard, power requirement is that of one server, rather than one or multiple racks
Unregulated output	Low-voltage output is only loaded by further DC-DC VRMs and POLs; bus voltage regulation is not strictly required

dress the analysis, design, control, and implementation of a candidate front-end converter design which meets the application requirements. In order to do so, the nature of high conversion ratio DC-DC conversion is addressed in the following section, and the inherent difficulties are used to motivate the selection of a converter topology to implement the front-end converter.

Chapter 2

High Conversion Ratio DC-to-DC Power Conversion

In general, a DC-to-DC converter may be represented as shown in Fig. 2.1. The converter,

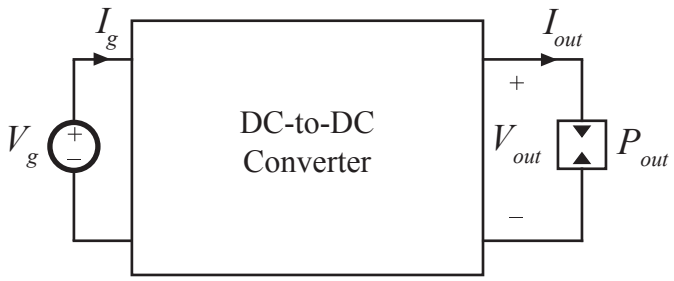


Figure 2.1: Generalized model of a two-port DC-to-DC converter.

included as a "black box" serves the purpose of transferring power from the input port, loaded by the ideal voltage source V_g, to the output port, loaded by the power source P_{out}. In general, both the input voltage and output power sources may be time-varying or nonlinear depending on the application details.

Ideally, the converter is capable of operating with no loss of power, resulting in 100% efficienct power conversion. In any real implementation of a DC-to-DC converter, some losses will exist which decrease the converter efficiency from unity, with the actual operating efficiency defined as

$$\eta = \frac{P_{out}}{P_g} = \frac{V_{out} I_{out}}{V_g I_g} \ . \tag{2.1}$$

Thus, the DC-DC converter design and implementation serve to accomplish two goals in the system defined by Fig. 2.1; because input voltage and power are assumed to be set external to the converter,

the input current (and therefore power) as well as the output voltage (and therefore current) will be set by the converter operation, and its efficiency η. In general, the designer will endeavor to maximize converter efficiency to the extent possible, and will choose to regulate the output voltage and current according to the needs of the load modeled by P_{out}.

The internal construction of the DC-to-DC converter may consist of any of the components shown in Fig. 2.2 [22]. The elements in Fig. 2.2 can be grouped into two sets according to their ideal

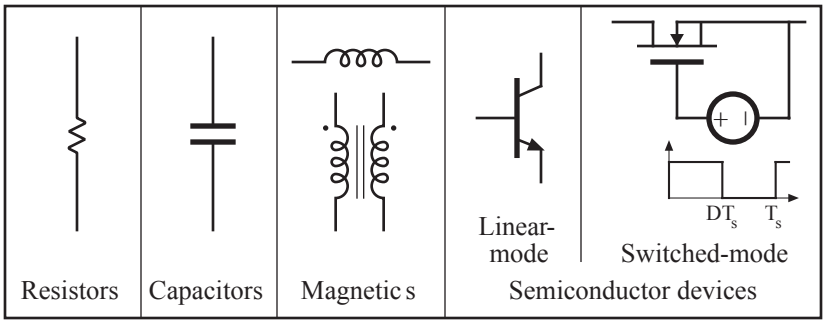


Figure 2.2: Devices available for use in the design of power converter circuits.

power efficiency. In their ideal implementation, neither capacitors, magnetics, nor switched-mode semiconductor devices exhibit any power loss, whereas both resistors and linear-mode semiconductors will have a non-zero minimum loss associated with them when any power is processed through these elements [23].

Where high efficiency is seen as a primary goal in the design of power converters, the use of resistors and linear-mode semiconductors must be limited to reduce the power losses they will exhibit. To this end, DC-to-DC converters are often designed within a subclass of circuits known as switched-mode power supplies (SMPS), so-named because they make use of only magnetics, capacitors, and switched-mode semiconductor devices as power processing elements. Linear-mode semiconductors and resistors are occasionally present in these circuits, but only for the purpose of providing ancillary functions to the core power conversion elements. The basic operational theory and analysis of SMPS is reviewed in the following section.

2.1 Switched-Mode DC-to-DC Converters

The most basic SMPS circuit capable of implementing the DC-to-DC functionality discussed so far is shown in Fig. 2.3. This circuit, known as the Buck converter, consists of a second-order L-C filter and an ideal single-pole, dual-throw (SPDT) switch. The SPDT switch is used to simplify the circuit operational description, but may be considered to consist of two switched-mode semiconductor devices in a realizable circuit implementation.

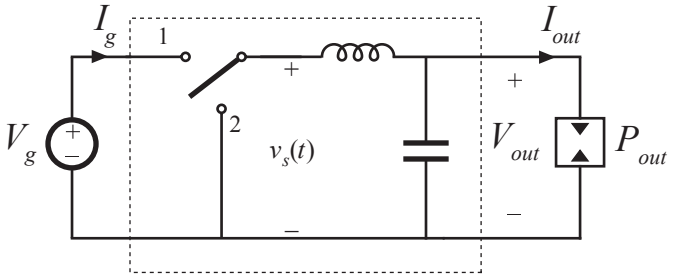


Figure 2.3: The buck converter: a basic SMPS.

The operation of the buck converter of Fig. 2.3 may be well understood by considering the two stages - the SPDT switch and the L-C filter - as independent elements coupled at the voltage $v_s(t)$. Under this approach, $v_s(t)$, often referred to as the switched-node voltage, takes value either V_g or 0 depending on the switch state. To achieve the voltage step-down desired, the SPDT switch is commutated between positions 1 and 2 as shown in Fig 2.4; the commutation occurs periodically with frequency f_s and switching period $T_s = 1/f_s$. Additionally, a duty cycle D is used to define the portion of each switching period in which the switch remains in position 1.

The second-stage L-C circuit then acts as a low pass filter. If the values of inductance L and capacitance C are assumed to be arbitrarily large, the circuit is an ideal low-pass filter, i.e. it will exhibit a transfer function from $v_s(t)$ to V_{out} which passes only the DC component:

$$V_{out} = \langle v_s(t) \rangle \Big|_{T_s} = \frac{1}{T_s} \int_0^{T_s} v_s(t) dt \ , \tag{2.2}$$

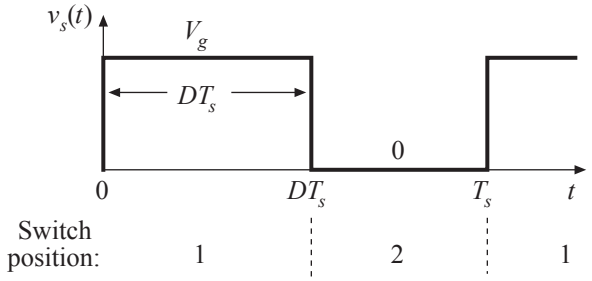


Figure 2.4: Switched-node voltage of the buck converter operated with pulse-width modulation.

where angled brackets indicate the mean value. Because $v_s(t)$ is periodic with value

$$v_s(t) = \begin{cases} V_g & 0 < t < DT_s \ , \\ 0 & DT_s < t < T_s \ , \end{cases} \tag{2.3}$$

the integral in (2.2) can be calculated simply to obtain the output voltage of the buck converter

$$V_{out} = DV_g \ , \tag{2.4}$$

or, as is commonly used, the voltage conversion ratio for the buck

$$M = \frac{V_{out}}{V_g} = D \ . \tag{2.5}$$

This manner of converter operation, in which a constant switching frequency is used and the switch duty cycle is used to control the output voltage, is referred to as Pulse-Width Modulation (PWM).

At this point, it is useful to consider the actual implementation of the SPDT switch used in the buck converter with real semiconductor devices. Though alternate implementations are possible, the circuit of Fig. 2.5 is addressed here, where the SPDT switch is realized with two MOSFETs operating as switched-mode devices. The devices Q_1 and Q_2 are driven with complementary gate-to-source voltages, v_{gs1} and v_{gs2} such that during DT_s only Q_1 conducts current, and during the remainder of the period only Q_2 conducts.

In evaluating the buck converter's usefulness for the proposed, high step-down, high-efficiency converter, it is useful to consider the voltage and current waveforms in each of the semiconductor devices. Though the ideal switched-mode transistor is lossless, any real MOSFET device will exhibit

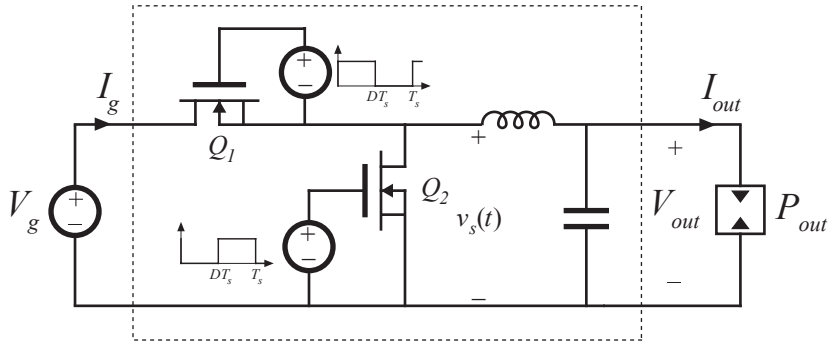


Figure 2.5: Implementation of the ideal SPDT switch in the buck converter with two MOSFET devices.

some loss in-circuit, and these losses will scale with the current and voltage stresses applied to the device. Additionally, for a set performance in-circuit, the cost of the devices used to implement Q_1 and Q_2 will increase as the peak voltage and current they are stressed with increases. In order to evaluate these parameters, steady-state operation of PWM converters is reviewed.

2.1.1 Steady-State Analysis of PWM Converters

For PWM converters operating in steady-state, the principles of inductor volt-second balance and capacitor charge balance may be applied to the circuit [22, 24]. By considering only steady-state operation of the converter, all converter waveforms are periodic; e.g. for inductor currents $i_L(nT_s) = i_L((n+1)T_s)$ and capacitor voltages $v_C(nT_s) = v_C((n+1)T_s)$. If this relation did not hold true, the converter would, by definition, be operating under transient conditions. Keeping in mind that all voltages and currents must take the same value at beginning and end of any switching period, the inductor volt-second balance and capacitor charge balance relations are obtained,

$$\begin{aligned} \int_{nT_s}^{(n+1)T_s} v_L(t)dt &= L\left[i_L((n+1)T_s) - i_L(nT_s)\right] = 0 \ , \\ \int_{nT_s}^{(n+1)T_s} i_C(t)dt &= C\left[v_C((n+1)T_s) - v_C(nT_s)\right] = 0 \ . \end{aligned} \tag{2.6}$$

Further, because the filter components are assumed to be large in value, the small-ripple approximation is applied to state that the actual variation of inductor currents and capacitor voltages

within the switching period is small, and in steady state these parameters are well modeled by their average values,

$$\begin{aligned} i_L(t) &\approx I_L \ , \\ v_C(t) &\approx V_C \ . \end{aligned} \tag{2.7}$$

With these principles applied to the buck converter, the time-domain waveforms of the MOSFET voltages and currents are solved simply, resulting in waveforms as shown in Fig. 2.6. Again applying capacitor charge balance to note that the average capacitor current over one switching period must be zero the inductor current's average value may be solved, $I_L = I_{out} = P_{out}/V_{out}$.

The stresses on the switches in the buck converter are summarized in Table 2.1 for both the general case, and a numerical example application of a 400-to-12 V, 120 W converter. A significant issue can immediately be seen; because the converter is operated with an extremely small duty cycle, $D = 0.03$ as solved from (2.4), Q_1 must pass the entire power flow of the converter during a very small time interval in which it conducts current. This results in peak current stresses which are more than twenty times as large at the average current processed by the device. Despite only conducting an average current of 300 mA, Q_1 must be sized to handle 10 A of current, and will contribute losses associated with 1.73 A of RMS current. Similarly, though the average voltage blocked by Q_2 is only the output voltage of 12 V, the device must be rated to block the full 400 V of the input.

Table 2.1: Voltage and current stresses on buck converter switches.

	Q_1				Q_2			
	v_{peak}	v_{avg}	i_{avg}	i_{rms}	v_{peak}	v_{avg}	i_{avg}	i_{rms}
General:	V_g	$(1-D)V_g$	DI_L	$\sqrt{D}I_L$	V_g	DV_g	$(1-D)I_L$	$\sqrt{1-D}I_L$
Application†:	400 V	388 V	0.3 A	1.73 A	400 V	12 V	9.7 A	9.85 A

† Values given for a 400-to-12 V converter operating at 120 W

2.1.2 Switch Stress and Utilization

The magnitude of the switch stresses in PWM converters is sometimes quantified by considering the "'switch stress"', which is given for the ith switch in the converter by

$$S_i = V_{peak,i} I_{rms,i} \ , \tag{2.8}$$

and the switch utilization, defined as

$$U_i = P_{out}/S_i \ . \tag{2.9}$$

For an individual switch, increased stress S_i correlates strongly with an increase in expected power loss during converter operation. Additionally, for a given application, minimization of total switch stresses $S_{tot} = \sum S_i$, and thus maximization of the total switch utilization $U_{tot} = P_{out}/S_{tot}$, leads to reduction of the total silicon area required to realize the power devices of the converter, thereby curtailing the cost associated with device implementation [22]. In the buck converter, the individual and total switch stresses and utilization are given in Table 2.2, again for both the general case and the 400-to-12 V example application.

For the general case, the switch utilization of the buck converter is plotted as a function of the steady-state duty cycle D in Fig. 2.7. From (2.5), small duty cycles D necessarily result from large converter conversion ratios. This, in turn results in very high switch stresses in the converter. Because it is in series with the input voltage source, all of the power flow of the converter must be processed through transistor Q_1 during its conduction interval, DT_s. During the remainder of the period, $(1 - D)T_s$, no power is flowing from the input source, $I_g = 0$. As the converter operates with a smaller conversion ratio, the period in which power flow is permitted decreases, but the total power flow through the switch remains equal to P_{out}. Thus, for small conversion ratios, all power flow must be accomplished in very small conduction intervals, resulting in very high peak-to-average current in Q_1, and therefore poor switch utilization. Clearly, when switch utilization is of primary concern, the buck converter is not an attractive candidate to implement the high step-down voltage converter; alternate power converter topologies need to be considered if the power conversion is to be accomplished with low cost and high efficiency.

Table 2.2: Device and converter switch stresses and utilization

	S_1	U_1	S_2	U_2	S_{tot}	U_{tot}
General:	$V_g\sqrt{D}I_L$	$\frac{D}{\sqrt{D}}$	$V_g\sqrt{1-D}I_L$	$\frac{D}{\sqrt{1-D}}$	$V_g I_L\left(\sqrt{D}+\sqrt{1-D}\right)$	$\frac{D}{\sqrt{D}+\sqrt{1-D}}$
Application†:	0.69 kVA	0.17	3.94 kVA	0.03	4.63 kVA	0.026

† Values given for a 400-to-12 V converter operating at 120 W

Similar analysis to that detailed for the buck converter can be applied to any other standard SMPS topology. Additional examples are given in Table 2.3, where the converter conversion ratio and switch utilization are given for each power converter. It is clear that the issue facing the buck converter is present in each of these topologies as well; in each case, the switches in the converter are exposed to both the high voltage input and high current output. This causes the switch stresses to be quite large, and the total utilization is therefore very small. Switches must be rated at total kVA ratings well above the actual converter power levels, and converter cost and efficiency are adversely impacted.

To alleviate the issue, topologies must be considered in which the input and output ports of the converter are decoupled. That is, candidate topologies should be separated in such a manner that all switches in the converter circuit are exposed only to the high voltage at the input port *or* the high current at the output port which are inherent in the high step-down application. For this purpose, a transformer is used in circuit to perform the large voltage step-down without requiring small duty cycles and high switch stresses.

2.1.3 Transformer Isolation in PWM Converters

In order to accomplish the decoupling of input and output ports to avoid excessive device stresses, a theoretical circuit element is considered: the DC transformer (DCX) of Fig. 2.8(a). The DCX has behavior equivalent to that of an ideal transformer, where the primary and secondary

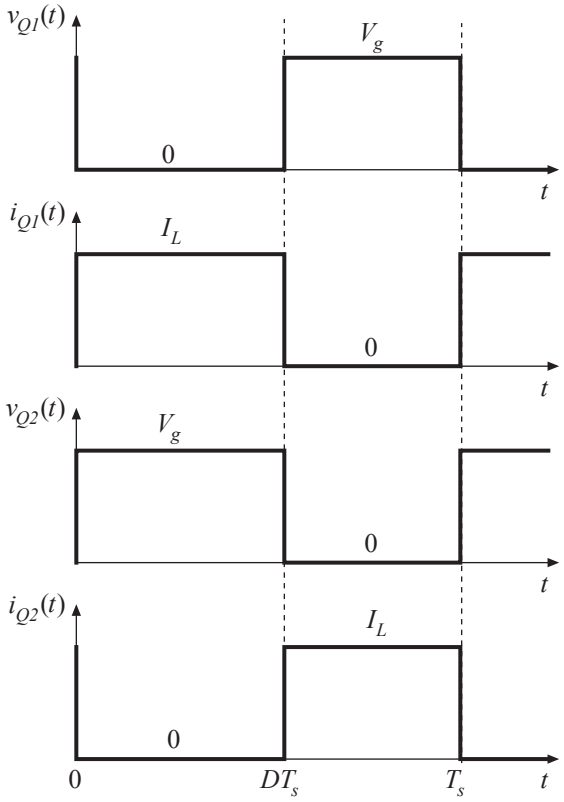


Figure 2.6: Voltage and current stressed of both semiconductor devices in the buck converter.

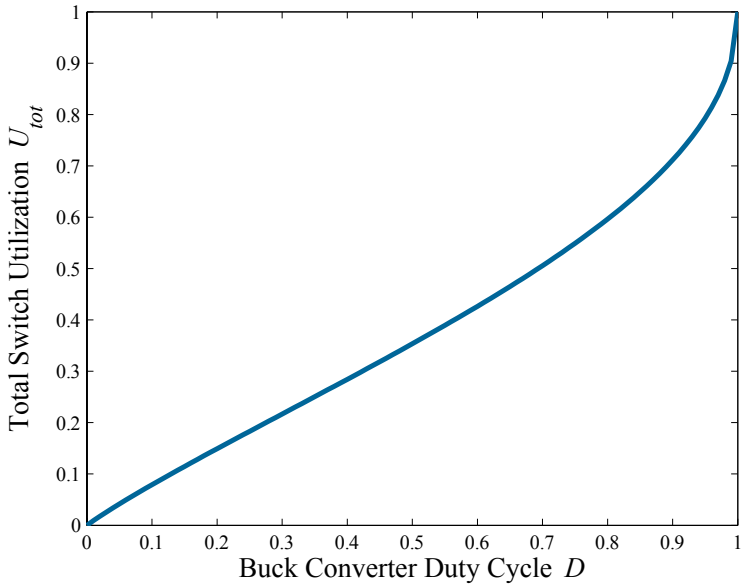
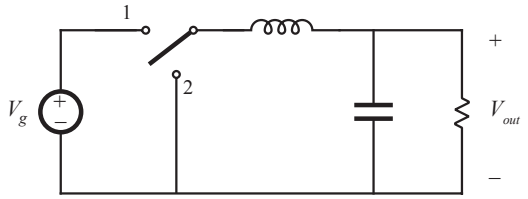
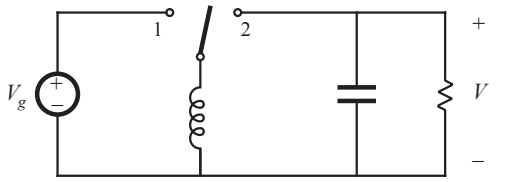
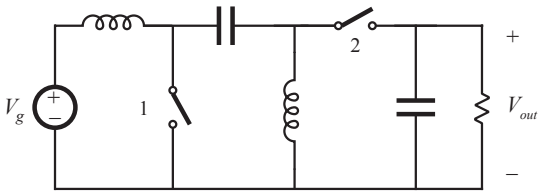
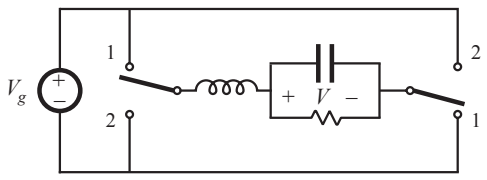
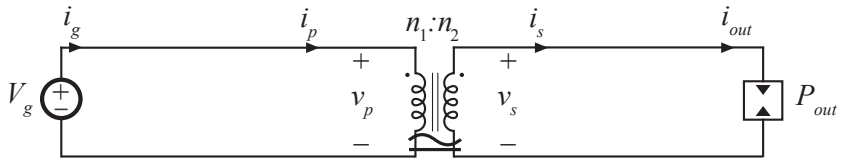


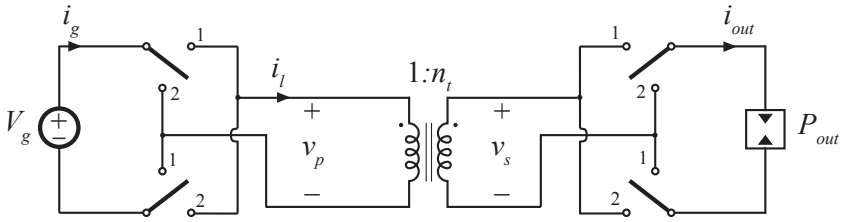
Figure 2.7: Total switch utilization as a function of duty cycle in the buck converter.

Table 2.3: Switch utilization in various converters

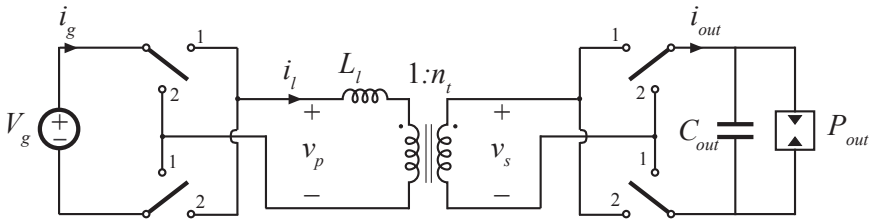
Converter	Duty Cycle D	Total Switch Utilization U_{tot}
Buck 	$\frac{V_{out}}{V_g}$ $= 0.03$	$\frac{D}{\sqrt{D}+\sqrt{1-D}}$ $= 0.026$
Buck-Boost 	$\frac{V_{out}}{V_{out}+V_g}$ $= 0.0291$	$\frac{(1-D)\sqrt{D}}{2}$ $= 0.0828$
SEPIC 	$\frac{V_{out}}{V_{out}+V_g}$ $= 0.0291$	$\frac{(1-D)\sqrt{D}}{2}$ $= 0.0828$
Bridge 	$\frac{V_{out}+V_g}{2V_g}$ $= 0.515$	$\frac{2D-1}{2\sqrt{D}+2\sqrt{1-D}}$ $= 0.0106$



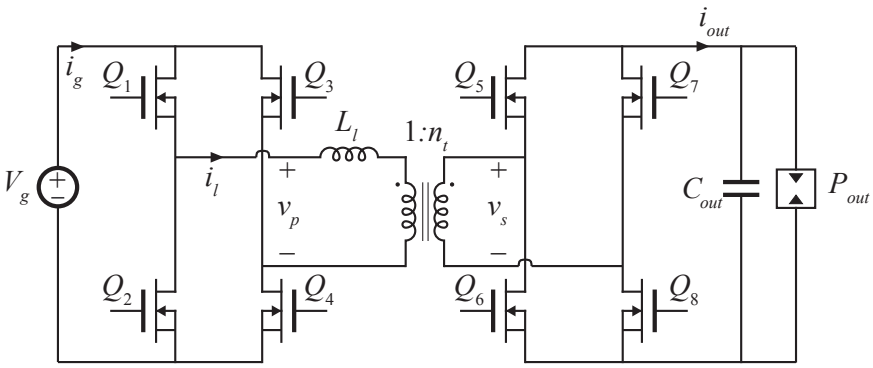
(a) Ideal AC and DC transformer model (DCX).



(b) inclusion of switches to prevent transformer saturation.

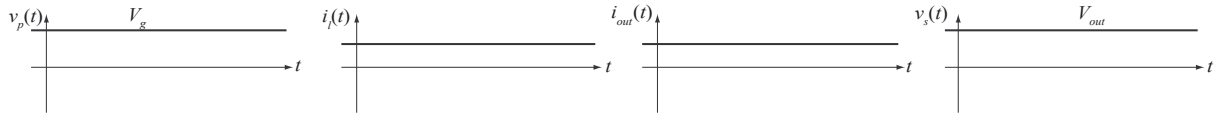


(c) inclusion of transformer leakage inductance.

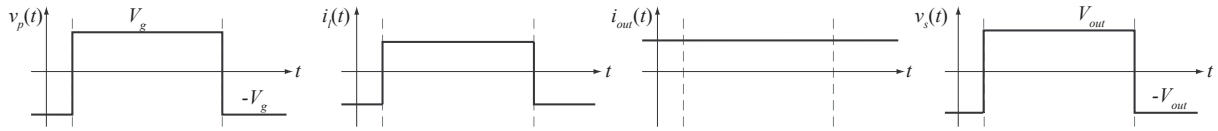


(d) Full dual active bridge converter.

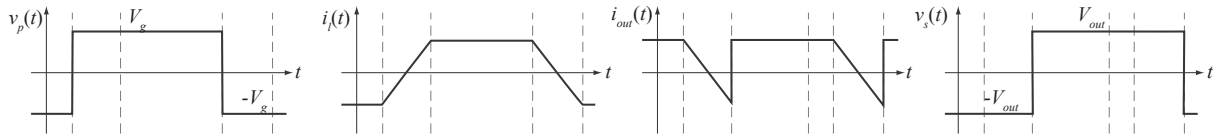
Figure 2.8: Circuits used in the conceptual development of the dual active bridge converter, operating as a DC transformer.



(a) Ideal AC and DC transformer model (DCX).



(b) inclusion of switches to prevent transformer saturation.



(c) inclusion of transformer leakage inductance.

Figure 2.9: Waveforms of the DCX, switched DCX, and DAB converters, where (a)-(c) are given for the corresponding circuit shown in Fig. 2.8.

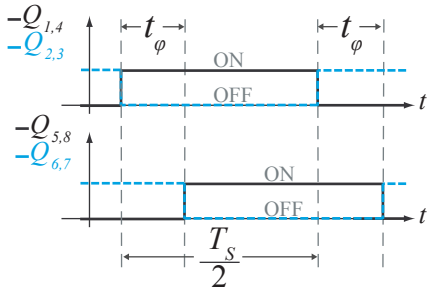


Figure 2.10: Gate drive waveforms for the DAB converter, including phase shift interval time t_φ, which occurs twice per switching period T_s.

winding voltages and currents are related by the number of turns associated with each winding as

$$n_1 i_p(t) + n_2 i_s(t) = 0 \ , \tag{2.10}$$

$$\frac{v_p(t)}{n_1} = \frac{v_s(t)}{n_2} \ . \tag{2.11}$$

These equations hold true for both AC and DC voltages and currents applied to the transformer windings. With V_g being the only source and having no AC-component, all voltages and currents in the ideal DCX are DC, and therefore have unity ratio between average value and either peak or RMS value, as diagrammed in Fig. 2.9(a). The DCX can be used to effectively accomplish the intended voltage step-down by setting the turns ratio equal to the voltage conversion ratio of the converter,

$$\frac{n_2}{n_1} = \frac{V_{out}}{V_g} \ . \tag{2.12}$$

Where the ratio n_2/n_1 is generally termed the turns ratio, n_t. In doing so, two goals are accomplished. First, the power conversion is accomplished, with the transformer effectively passing all power from high voltage input to low voltage output in a lossless manner. Second, the input and output ports are effectively decoupled with the high currents confined to the low voltage output and the high voltages similarly only present at the primary of the DCX. So long as the magnetic isolation barrier between the primary and secondary windings is not traversed, no position in the circuit is simultaneously exposed to voltage and current stresses which caused the poor switch utilization in the non-isolated topologies of the previous section.

2.1.4 Practical DCX implementation

Due to the saturation of magnetic devices when DC voltages are applied, it is not possible to realize the DCX as shown in Fig. 2.8(a). Instead, a minimum extension to the concept is presented in Fig. 2.8(a-d). First, in (b), four SPDT switches are used, all of which are simultaneously and periodically commutated between positions 1 and 2. Each commutation flips the polarity of both the input source and output load. If commutation is carried out with 50% duty cycle, the same

net behavior of the circuit is obtained but the waveforms applied to the transformer are now AC-only, as shown in Fig. 2.9(b). Because all waveforms remain either DC or perfect square-wave AC, it remains true that each waveform has equal peak and RMS value, indicating that at no point in the circuit are the voltage or current stresses greater than the absolute minimum required to achieve the output power of the converter. That is, all circuit elements on the secondary-side of the transformer are stressed at most to the average output values V_{out} and I_{out}, and all circuit elements on the primary are exposed only to V_g and I_g.

The AC transformer, when operated below saturation, will retain behavior well-approximated by the ideal relation in (2.10)-(2.11), so long as the device is constructed with very tight coupling between primary and secondary winding, and very little magnetization of the transformer core is allowed. Unfortunately, any real transformer will exhibit less-than-unity coupling between its two windings. This effect is modeled through the inclusion of a non-zero leakage inductance L_l in series with the transformer, as shown in the further refinement of Fig. 2.8(c). The voltage applied to this inductance at any time is given by the difference of the primary voltage and the secondary voltage, reflected through the transformer

$$v_L(t) = v_p(t) - \frac{v_s(t)}{n_t} \ . \tag{2.13}$$

If no modification is made to the switch commutation scheme, the voltage $v_l(t)$ is zero at all times due to the selection of transformer turns ratio in (2.12). The converter is therefore uncontrollable, as the current in the inductor, and thus the rectified output current, have zero derivative. In order to accommodate this leakage inductance, a small phase shift is therefore inserted between the commutation of the two primary SPDT switches and the two on the secondary. The resulting waveforms are shown in Fig. 2.9(c). During the phase shift interval, the voltage applied the inductor is

$$v_L(t) = \pm \left(V_g - \frac{V_{out}}{n_t} \right) \ . \tag{2.14}$$

which causes a ramping of inductor current. The duration of the phase shift interval can be adjusted in order to control the magnitude of the inductor current, and therefore control the output current

of the converter. In return, the converter is provided some detriment in the fact that the RMS and peak currents in the converter are no longer equal. Examining the output current diagram of Fig. 2.9(c), it is clear that the peak and RMS values of i_{out} will be slightly larger than its average value, I_{out} due to the ramping interval. This increase in RMS currents above the minimum results in additional device stress and additional loss in the converter above the absolute minimums required to achieve the output power. The AC component of the output current additionally necessitates the inclusion of an output capacitance, C_{out} which is assumed large enough such that only the DC component I_{out} is passed to the load. It is desired to operate the converter with a minimum phase shift duration in order to minimize margin by which the RMS currents in the converter exceed the theoretical minimum, and minimize the required output capacitor size necessary to adequately filter the AC component of the output current.

In addition to the leakage inductance L_l, some non-infinite magnetizing inductance will be present in any real transformer implementation. Like the leakage inductance, inclusion of this magnetizing inductance will increase RMS currents present in the converter for the specified operating mode. However, unlike L_l consideration of magnetizing inductance does not necessitate alterations in switch modulation scheme in order to obtain proper operation. Because it is additionally feasible to design a transformer with large enough magnetizing inductance that resulting magnetizing currents are negligible, it is not of crucial importance to include the magnetizing current in this analysis.

Finally, in Fig. 2.8(c), the circuit implementation of the SPDT switches is shown. Each ideal SPDT switch is replaced with two MOSFET devices, resulting in a total of eight active switched-mode elements. In order to achieve the same switching behavior as the SPDT switch circuit, the MOSFETs are driven according to the waveforms of Fig. 2.10. The resulting circuit is now a fully-realizable power converter, and is known as the dual-active bridge (DAB) converter [25].

2.2 The Dual Active Bridge Converter

2.2.1 Switch utilization in the DAB converter

At this point, it is prudent to return to the previous analysis of switch stress and utilization in order to evaluate how successfully this converter is able to accomplish the goal of implementing a high step-down converter without excessive switch stress. As noted previously, the ratio by which the device RMS currents will exceed the average input and output currents depends on the duration of the phase shift interval. In the extreme case, if the phase shift interval is reduced to an absolute minimum (corresponding to a leakage inductance approaching zero), the converter waveforms revert to those shown in Fig. 2.8(b), and switch stresses for primary and secondary devices become

$$S_{1-4} = \sqrt{\frac{1}{2}} I_g V_g \ , \quad S_{5-8} = \sqrt{\frac{1}{2}} I_{out} V_{out} \ . \tag{2.15}$$

This result indicates that the peak voltage and current stresses on each device are the minimum values; no switch is ever subjected to an instantaneous voltage or current greater than the pair of average values present at either the input or output.

Assuming the converter operates with nearly 100% efficiency, $I_g V_g = I_{out} V_{out} = P_{out}$, this means that the individual stresses of all eight switches is identical, which for the intended 400-to-12 V, 120 W application gives

$$S_{1-8} = \frac{\sqrt{2}}{2} P_{out} = 85 \text{ VA} \ , \tag{2.16}$$

which constitutes nearly a 50-fold reduction in the maximum switch stress in the circuit compared to the buck converter case. The individual utilizations are then

$$U_{1-8} = \frac{2}{\sqrt{2}} = 1.414 \ , \tag{2.17}$$

and the total switch utilization of the converter is

$$U_{tot} = \frac{\sqrt{2}}{8} = 0.1768 \ . \tag{2.18}$$

Note that, although the individual switch stresses and utilizations are significantly improved over all non-isolated PWM converters, the total switch utilization is improved only by a factor of two due to

the increased number of switches in circuit. Further alterations to converter topology which reduce the number of active switches present the opportunity to further increase total switch utilization, though this advantage is obtained at the cost of increased complexity or reduced functionality. Additionally, though this thesis will focus on the analysis of the DAB converter with solely inductive tank impedance, resonant converters such as the LLC-converter have also been demonstrated with success for similar applications [26–29].

The exhibition of minimum switch stresses in the presence of a large step-down voltage conversion ratio make the DAB converter an attractive topology for the data center application. However, it should be reiterated that these stress and utilization figures are given under the assumption of zero leakage inductance L_l which is in general not achievable. In order to further examine the merits of the DAB converter in a practical application, the converter operation in the presence of non-zero leakage inductance is reviewed.

2.2.2 Steady State Solution Including Leakage Inductance

In the presence of a non-zero leakage inductance L_l, the converter must operate with a phase shift interval, t_φ as shown in Fig. 2.10 in order to control the value of the output current. Because the inductor current is ramping according to the sum of the input and reflected output voltage applied across it, the presence of this interval necessarily increases the peak and RMS currents in the transformer and inductor (collectively referred to as the "tank") above their corresponding averaged values. A similar increase results in the switch RMS and peak currents relative to their own averaged values, thus reducing the switch utilization. The duration of the phase shift interval is therefore a quantity to be minimized if low stresses are to be achieved during converter operation.

In order to determine the magnitude of reduction in switch utilization, the relation between the DC output current and the time varying currents present throughout the converter must be reviewed [25]. Returning to the waveforms of Fig. 2.8(c), it can be seen that the phase shift is given

by

$$t_\varphi = L_l \frac{I_{pk}}{V_g} \ , \tag{2.19}$$

where I_{pk} is the peak current in the inductor, and the average value of the converter output current is given by [25, 30]

$$I_{out} = \frac{I_{pk}}{n_t} \left(1 - \frac{2t_\varphi}{T_s} \right) \ . \tag{2.20}$$

Combining (2.19) and (2.20)

$$I_{out} = \frac{I_{pk}}{n_t} \left(1 - \frac{2I_{pk}L_l}{V_g T_s} \right) \ . \tag{2.21}$$

Similarly, the RMS output current is given by

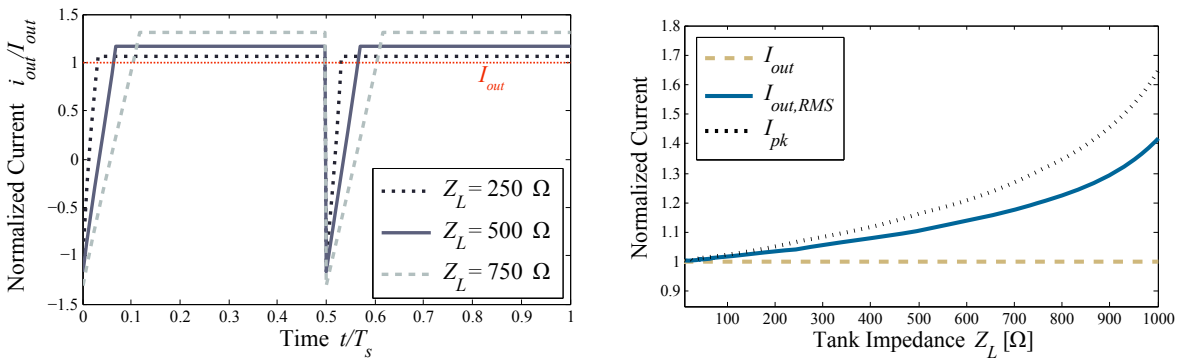
$$I_{out,RMS} = \frac{I_{pk}}{n_t} \sqrt{1 - \frac{4}{3} \frac{I_{pk}L_l}{V_g T_s}} \ . \tag{2.22}$$

Because each switch on the secondary conducts during an identical half-period, the secondary switch RMS currents are simply

$$I_{5-8,RMS} = \frac{I_{pk}}{n_t} \sqrt{\frac{1}{2} - \frac{2}{3} \frac{I_{pk}L_l}{V_g T_s}} \ , \tag{2.23}$$

and the primary switch RMS currents are obtained by reflecting through the transformer turns ratio, $I_{1-4,RMS} = n_t I_{5-8,RMS}$. In (2.20)-(2.23), as argued previously, it is clear that if the inductance L_l is reduced to nearly zero, the resulting converter operates with $n_t I_{pk} = I_{out} = I_{out,RMS}$ and the peak device stresses are minimized. As the inductance increases, the peak and RMS currents throughout the converter increase accordingly. This relationship is diagrammed further in the plots of Fig. 2.11, which show the normalized time-domain output current and the solved peak and RMS current values for varying values of the inductance impedance at the switching frequency $Z_L = 2\pi f_s L_l$, which is also normalized to allow independence from switching frequency selection. Finally, the total switch utilization of the converter is plotted with respect to the size of the tank inductance in Fig. 2.12.

Clearly, there is significant motivation to maintain a minimal leakage inductance magnitude. However, prior to applying this analysis to converter design, additional characteristics of



(a) (b)

Figure 2.11: Time domain output current in (a), normalized by the average output current I_{out}, and for varying values of the inductor impedance at the switching frequency Z_L. In (b), the normalized average, RMS, and peak output current are plotted against this impedance. In all cases the same averaged output voltage and power are assumed.

the converter must be considered. Though current and voltage stresses on the switches have been considered with understanding of their correlation to power loss (and device cost), additional loss mechanisms in the switches must be considered. In order to do so, a basic loss model of switching devices is reviewed in the following section.

2.2.3 Switching Device Loss Model

The DAB Converter of Fig. 2.8(d) is implemented with eight MOSFET transistors which have until now been considered to operate as lossless, ideal switches, with switch state controlled by their respective gate-to-source voltages. However, any implementation of such devices will contain a multitude of parasitic behaviors and characteristics which will cause deviation from ideal behaviors and, in many cases, induce loss in-circuit.

A basic loss model of a MOSFET under switched-mode operation which attempts to include a subset of the most impactful device parasitics is shown in Fig. 2.13(c). The MOSFET is considered to consist of an ideal switch in series with resistance r_{on} which models the resistivity of the conducting channel. The behavior of the intrinsic body diode is included through the addition of an ideal diode between source and drain ports; this diode may be further replaced with its own loss

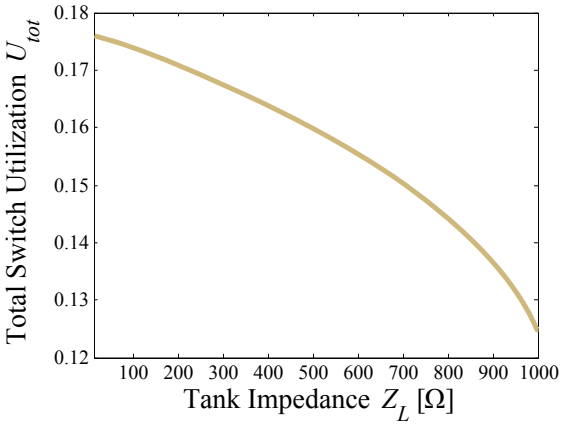


Figure 2.12: Total switch utilization of the DAB converter as it varies with the inductor size (relative to switching frequency).

model if such characteristics are deemed significant to circuit operation. Finally, the stored charges present in the MOSFET device are modeled by three capacitances, C_{gs}, C_{ds}, and C_{gd}. Each of these capacitances is highly nonlinear, and the ramifications of this nonlinearity are addressed in Section 4.1.

Applying the loss model of Fig. 2.13(c) in any SMPS, two types of losses arise. Conduction losses, which arise from the flow of current through the MOSFET on-resistance r_{on} (and diode, is considered non-ideal), and switching losses due to energy loss in the dynamic charging and discharging of device capacitances. Conduction losses due to r_{on} are dependent upon the RMS current applied to the switch, and take the form

$$P_{cond} = {I_{d,RMS}}^2 r_{on} \ . \tag{2.24}$$

Switching losses depend largely on the nature of the application circuit, and may be mitigated or eliminated entirely through soft-switching techniques. Initially, it is sufficient to consider two categories of such losses which may potentially arise. Gate drive losses arise in the circuitry responsible for supplying the pulsating v_{gs} waveforms driving the gate of the device. It a total charge Q_g is needed to charge both C_{gs} and C_{gd} between $v_{gs} = 0$ and its maximum value $V_{GS,max}$, and the device is modulated with switching frequency f_s, the power lost in the gate driver assuming no

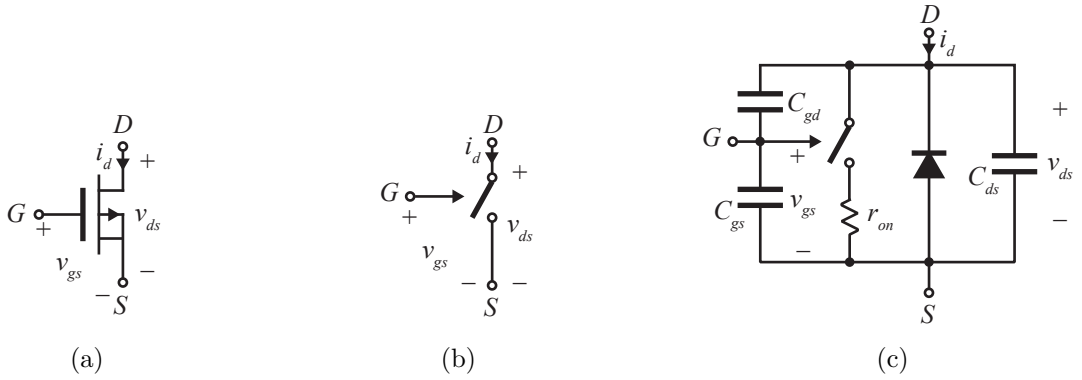


Figure 2.13: The MOSFET circuit symbol of (a) represents a real device which under switched-mode operation may be modeled as ideal (b), or with a subset of parasistics considered (c). In each model the drain, gate, and source ports are indicated as D, G, and S, respectively.

charge recovery is

$$P_{sw,g} = Q_g V_{GS,max} f_s \ . \tag{2.25}$$

Additionally, a second set of losses are incurred anytime the device is turned on with non-zero drain-to-source voltage v_{ds}. In this event, all energy stored in the capacitance C_{ds} is effectively shorted out through the MOSFET channel and associated on-resistance r_{on}. Again assuming a switching frequency f_s and some voltage $V_{DS,sw}$ present on C_{ds} just prior to MOSFET turn-on, the resulting losses are modeled as

$$P_{sw,ds} = \frac{1}{2} C_{ds} {V_{DS,sw}}^2 f_s \ . \tag{2.26}$$

To maximize converter efficiency and minimize energy losses, each of the power losses described in (2.24)-(2.26) should be minimized. The device parameters r_{on}, C_{ds}, and Q_g are subject to optimization through selection of appropriate parts to implement the MOSFETs in-circuit. The tradeoffs inherent in the selection process will be addressed further in the latter sections of this chapter. As derived in the previous section, $I_{d,RMS}$ and thus the incurred conduction losses may be minimized along with the tank inductance L_l. Both $V_{GS,max}$ and $V_{DS,sw}$ may be minimized to reduce the switching losses. A minimum value for $V_{GS,max}$ equal to the device threshold must be met such that the selected device operates in switched-mode. The details of minimizing $V_{DS,sw}$ will be addressed in significant detail in the remainder of this thesis, but for the given description of

operation used thus far, it can be seen that $V_{DS,sw}$ is equal to the input voltage V_g for all primary devices and the output V_{out} for all devices on the transformer secondary. Finally, the two switching loss components are both minimized through the reduction of the switching frequency f_s, which may be subject to design optimization.

In summary, the simple analysis of the DAB converter has found that device stresses – or losses, equivalently – are minimized through two design decisions

- Minimize tank inductance L_l
- Minimize switching frequency f_s
- Minimize parasitic stored charges Q_g and C_{ds}

which result in the respective minimization of conduction and switching losses in the converter. In the following section, the validity of these conclusions is assessed in the presence of increasing detail of converter analysis, and the consideration of design goals beyond converter efficiency.

2.3 Converter Design Tradeoffs

As with most design decision, the enaction of the two design principles from the previous section results in additional ramifications on converter design. In particular, reduction of switching frequency correlates directly with increased converter size, which is not permissible for the data center application considered here. Without the ability to minimize the switching frequency, an alternate means of reducing switching losses must be used. Device parasitic stored charges can be greatly reduced through device selection, though this can only be done at the expense of on-resistance. It is possible, through the increase of tank inductance L_l, to reduce the switched voltage $V_{DS,sw}$ in the converter, with ramifications in terms of conduction losses throughout the converter. The tradeoffs associated with these design decisions are discussed in the following sections.

2.3.1 Selection of Switching Frequency

It is widely known that an inverse relationship exists between the physical size of magnetic components and the switching frequency of any power converter. The details of how this relationship arises, however, are less readily available. In order to understand the genesis of this relation, basic magnetic theory and loss analysis are briefly reviewed.

2.3.1.1 Magnetics Theory

The basic magnetic structure of Fig. 2.14 consists of n turns of a current-conducting wire wrapped around of core material which has permeability as shown in the material B-H characteristic plot of Fig. 2.15. The core geometry is defined as having an equivalent cross-sectional area A_c and transverse length l_m. These equivalent parameters model the aggregate behavior of the actual core area and length, both of which, in general, may vary throughout the core. When a time-varying

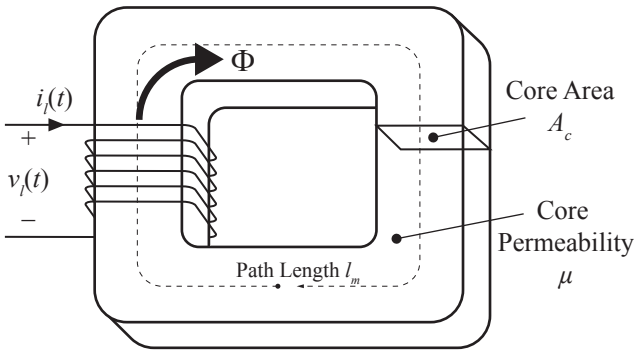


Figure 2.14: General structure of a magnetic device.

voltage $v_l(t)$ is applied to the conductor, a flux $\Phi(t)$ is produced in the core according to Faraday's law

$$v_l(t) = n\frac{d\Phi(t)}{dt} \ , \tag{2.27}$$

which is distributed throughout the core cross-section resulting in a flux density $B(t)$

$$\Phi(t) = \int_{A_c} B(t)dA \ , \tag{2.28}$$

The analysis of such a structure is simplified through three approximations,

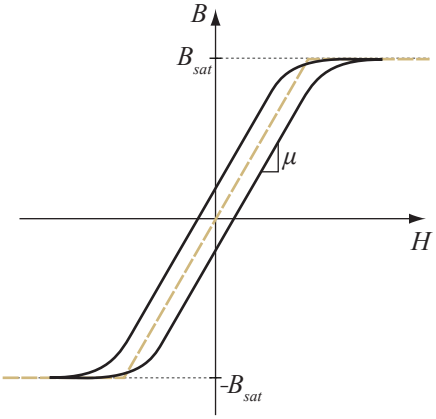


Figure 2.15: General ferrite material characteristic, as well as the simplified relationship which considers the material to be linear within saturation limits.

(1) The flux density is uniformly distributed throughout the core.

(2) The flux is contained entirely within the core material, $\mu \gg \mu_0$.

(3) The magnetic material is linear below the saturation limits, $B = \mu H$.

Applying these assumptions, and combining equations (2.28) and (2.27), the simplified relationship

$$B(t) = \frac{1}{nA_c} \int_0^t v_l(\tau) d\tau \tag{2.29}$$

is obtained. From this equation, the first conception of the relation between magnetic core size and power converter switching frequency can be discerned. In order to prevent saturation of the magnetic material, the peak flux density must be limited such that at all times $|B(t)| < B_{sat}$. Assuming that the implementation of the magnetic device in the power converter results in an applied voltage waveform $v_l(t)$ which is well approximated by a square-wave voltage waveforms with amplitude V_L and duty cycle D, the steady state variation in flux density within one switching period is given by

$$\Delta B = \frac{DT_s V_L}{nA_c} \ . \tag{2.30}$$

Thus, if the magnetic core size is reduced, resulting in the reduction in A_c, an equivalent reduction in the switching period T_s can be made to maintain the flux density variation during converter

operation. However, ΔB may also be reduced through increasing the number of turns of wire n. In order to further investigate the design tradeoffs of doing so, a basic loss analysis of magnetic components is considered.

2.3.1.2 Magnetics Loss Analysis

Standard practice for the loss modeling of magnetic components in power converters considers losses to be classified into either core or copper loss, depending on the location in which they manifest. Copper losses result from non-ideal current conduction in the copper wires making up the n-turn coil, while core losses occur in the magnetic material which constitutes the core.

Copper loss can be further divided into both DC and AC components. DC copper loss is given by the RMS current in the winding and the resistance $R_{L,DC}$ of the wire itself at DC, for example as would be measured by a ohmeter. The DC copper loss is then

$$P_{cu,DC} = {I_{L,RMS}}^2 R_{L,DC} \ . \tag{2.31}$$

For a winding made up of n turns of copper wire with area A_w and for a core geometry in which the mean length of a single turn of copper is MLT, this loss can be further characterized as

$$P_{cu,DC} = {I_{L,RMS}}^2 \rho \frac{nMLT}{A_w} \ , \tag{2.32}$$

where ρ is the resistivity of copper, $1.68 \times 10^{-8}\ \Omega \cdot \mathrm{m}$ at 25°C. In applications where significant steady-state AC currents flow in the conductor, losses will increase above the prediction. This increase may be taken into account through accurate modeling of additional eddy currents present in the conductor, which arise due to fringing of the magnetic flux, proximity effects in multi-layer windings, and the skin effect in solid-core conductors, each of which increases in prevalence with increased frequency of excitation [31]. Methods for the inclusion in analysis and mitigation in design of these AC losses will be presented in further detail in Section 3.6 and Appendix A.1. Though it is possible to model the general behavior of some of these effects, proximity losses and fringing effects in particular are highly geometry-dependent, and are therefore best suited to finite-element simulation techniques, which are presented in Appendix A.1.

Core losses in magnetic components arise fundamentally due to the motion of domain wall boundaries between regions of differing magnetization within the core material [32–35]. Despite knowledge of the physical origin of these losses, simple and useful physical models capable of predicting the magnitude of this loss are not readily available. Instead, empirical models of core loss are used which make use of non-physical curve fit relationships which numerically model the losses based on measured experimental data. The first such model to achieve widespread adoption was the Steinmetz equation [36]

$$P_v = K_V {f_s}^{\alpha} \left(\Delta B\right)^{\beta} \ , \tag{2.33}$$

where P_v is the volumetric core loss of the material, in $\mathrm{mW/cm^3}$, and K_V, α, and β are curve fit parameters. The core loss is then given by

$$P_{core} = P_v V_c \ , \tag{2.34}$$

with $V_c = A_c l_m$ the effective volume of the core.

In general, the Steinmetz equation provides highly accurate matching to experimental data for core loss only for a narrow range of frequencies and flux densities, ignored the effects of DC bias, and is only valid for sinusoidal excitation waveforms [37]. However, because of its simplicity and relative accuracy, the Steinmetz equation was quickly adopted and widely accepted, leading to its use as the standard for reporting core loss data among manufacturers of power magnetic materials. Therefore, more recent models which improve upon the numerical accuracy of this relation often attempt to use the parameters K_V, α, and β [37, 38].

Model improvements have been made across a variety of operating excitations through the inclusion of, for example, the time-history of the flux density derivative, the separation of minor loops of magnetization, or the incorporation of direct modeling of relaxation effects [31, 39–42].

Considering only the Steinmetz-estimated core loss and DC copper loss, it is possible to construct a constrained optimization of the losses in a magnetic component, given a predefined core geometry and set of applied excitation waveforms [22]. To do so, only the original Steinmetz equation for core loss and the DC copper loss are considered. Because the DAB waveforms are

non-sinusoidal and AC, it must be recognized that the use of the standard Steinmetz equation and only including DC resistance terms to predict transformer loss will inherently introduce some error. However, this analysis is sufficient to discern the general constraints on switching frequency in the DAB converter which are the ultimate goal of this analysis.

This optimization makes use of the fact that, for the selected core geometry, a finite area is available in which to fit the turns of coil. This available winding area W_A fits within it the n turns of copper wire with some fill factor

$$K_u = \frac{nA_w}{W_A} \ , \tag{2.35}$$

as shown in Fig. 2.16. This fill factor is less than one due to the portion of the window area which is

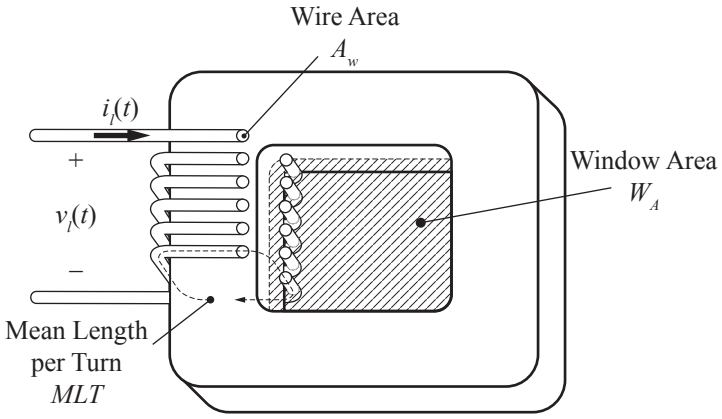


Figure 2.16: Winding area of magnetic core with low fill factor K_u.

taken up by e.g. wire insulation, gaps between conductors, or the coil former. Because the winding area is finite, and assuming only a moderate change in K_u with different winding strategies, it can be seen that an inverse relationship exists between the number of turns n and wire area A_w which are achievable under the assumption that the winding area is filled completely.

As the number of turns is increased, the flux density variation ΔB in the core material will decrease according to (2.29), resulting in a decrease in core loss P_{core}. However, the resulting decrease in A_w required to maintain the window area from being over-filled will result in an increase in DC copper loss P_{cu} according to (2.32). This relationship can be visualized as in Fig. 2.17. It is

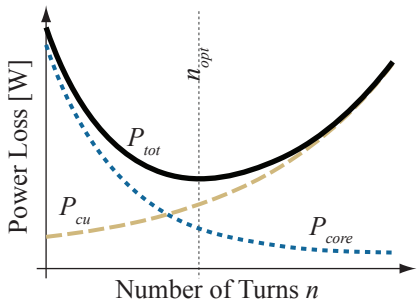


Figure 2.17: Core loss P_{core}, DC copper loss P_{cu}, and total magnetic device loss $P_{tot} = P_{cu} + P_{core}$ for a core with constant K_u and voltage excitation as n is varied.

therefore feasible to solve for the optimal number of turns n_{opt} that minimizes the total power loss $P_{tot} = P_{cu} + P_{core}$. This optimization occurs at the point at which

$$\frac{\partial P_{tot}}{\partial n} = 0 \ , \tag{2.36}$$

which can be expressed in terms of the two component power losses as

$$\frac{\partial P_{cu}}{\partial n} = -\frac{\partial P_{core}}{\partial n} \ , \tag{2.37}$$

which follows the method used in [22], though in that case the optimization is taken with respect to ΔB. Combining (2.30), (2.32) (2.33), and (2.35) and evaluating the partial derivatives, the relation is obtained

$$n_{opt}\frac{2MLT\rho {I_{L,RMS}}^2}{K_u W_A} = \beta {n_{opt}}^{-(\beta+1)} K_V {f_s}^{\alpha-\beta} \left(\frac{V_g}{2A_c}\right)^{\beta} A_c l_m \ , \tag{2.38}$$

which can then be solved for the optimal number of turns

$$n_{opt} = \left(\frac{\beta K_V {f_s}^{\alpha-\beta}\left(\frac{V_g}{2A_c}\right)^{\beta} A_c l_m K_u W_A}{2MLT\rho {I_{L,RMS}}^2}\right)^{\frac{1}{\beta+2}} \ , \tag{2.39}$$

which minimizes the sum of core (via Steinmetz) and DC copper loss. This analysis is simply extended to multi-winding magnetics by allocating window area according to the ratio of the squares of RMS currents in each winding [22].

2.3.1.3 Magnetics Size

The result in equation (2.39) can be recombined into the expressions for P_{cu} and P_{core} to obtain the optimal total power loss

$$P_{tot,opt} = V_c K_V {f_s}^{\alpha-\beta} \left(\frac{V_L}{2 n_{opt} A_c} \right)^{\beta} + {I_{L,RMS}}^2 \rho \frac{n_{opt} MLT}{A_w} \ , \tag{2.40}$$

with the resulting expression being a closed-form but expression for the minimum achievable power loss, given a specified core geometry, material, and application circuit waveforms. Note that, because the assumption of square-wave voltages was used in (2.30), this result is specific to the DAB converter with near-zero phase shift, though the method of analysis can be applied to any arbitrary application circuit.

The key implications of this analysis are difficult to discern through simple examination of equations (2.39) and (2.40) due to their complexity. However, it can be seen that the minimum achievable power loss in a given set of circumstances depends on both the core size parameters A_c and l_m as well as the switching frequency of the circuit f_s.

In order to further investigate the interplay of these parameters, the relationship is plotted in a normalized analysis for an example application in Fig. 2.18. In this plot, a set power loss $P_{tot,opt}$ is specified, then the minimum switching frequency for which this loss can be achieved is solved given equations (2.39) and (2.40). All of the standard core shapes and sizes from Appendix A.2 are plotted, with each point corresponding to a single geometry. A single core material is used [43], and the axes of Fig. 2.18 are therefore normalized according the the average size and usable frequency range of the material to decouple the result from the material itself. The core material parameters, α, β, and K_v vary with the frequency of excitation, and this variation is included in the numerical analysis.

From Fig. 2.18, it is apparent that in order to reduce the volume of the transformer in the DAB converter while maintaining a set amount of power loss, it is necessary to move toward higher switching frequency.

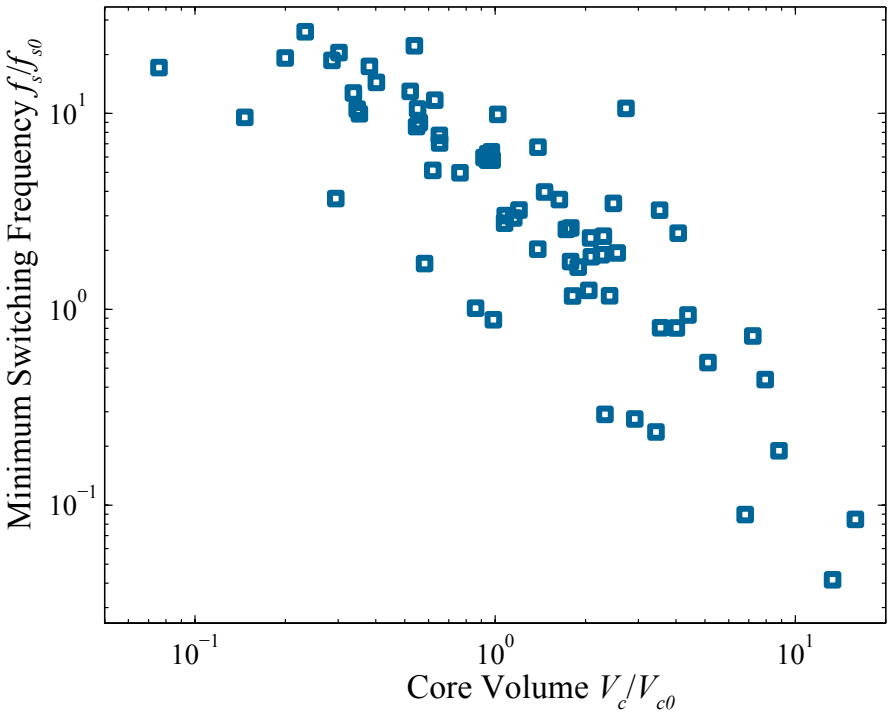


Figure 2.18: Normalized relationship between core volume and minimum switching frequency at which a set power loss P_{tot} is achievable in the transformer design for the DAB converter. Each point corresponds to one of a variety of standard cores shown in Appendix A.2 and a single core material [43].

2.3.1.4 Switching Frequency in DAB Converter

In order to design a converter capable of addressing the needs of the data center application detailed in Chapter 1, it is necessary to maintain a small overall footprint size. There is a high cost associated with additional floorspace in the data center, and an even greater premium associated with board space on the server motherboards themselves, which are the intended location for the proposed, integrated high step-down converter. In order to maintain a small footprint size and facilitate the incorporation of this converter directly onto the motherboards themselves, the analysis of the previous section indicates that a very low switching frequency is not appropriate. Instead, to reduce the size of magnetic devices in the DAB converter, a high switching frequency should be used. This is in direct contrast to the motivations on switching frequency design presented in the analysis of switching loss in Section 2.2.3, which indicated that a minimization of switching frequency was one approach to reducing switching loss in the converter and therefore maintaining high efficiency.

A tradeoff is therefore present in the selection of switching frequency, where the motivating design goals of small size and high efficiency cannot be simultaneously achieved through the selection of f_s alone. Fortunately, while the analysis has demonstrated that high switching frequency is *required* for the reduction of magnetic device size, it is only one method of reducing the switching loss of the converter. It is possible to allow the converter size constraints to dominate the selection of f_s while simultaneously meeting constraints on efficiency through alternate design decisions. In particular, both gate charge and output capacitance switching losses can be reduced through appropriate device selection, and the output capacitance loss can additionally be reduced or eliminated entirely through the use of zero-voltage switching (ZVS) techniques.

2.3.2 Selection of Tank Inductance

As given previously in equation (2.26), the turn-on of a switched-mode MOSFET with an established non-zero voltage present from drain to source results in the dissipation of all energy

stored in the parasitic device output capacitance. This energy loss can result in significant reduction of converter efficiency, particularly at high switching frequency. Because high switching frequency is required for small converter size, alternate methods of reducing this power loss must be considered.

The ZVS principle relies on operating the converter in a manner such that all energy is removed from the parasitic output capacitance of the MOSFETs prior to their turn-on, resulting in device turn-on with zero drain-to-source voltage [44–47]. A further advantage of the DAB topology that has not yet been mentioned is the inherent exhibition of zero-voltage transitions (ZVTs) on all eight devices under certain operating conditions [25,30]. To understand the process by which ZVS is achieved, the converter schematic and key waveforms during nominal operation are reproduced in Fig. 2.19 and Fig. 2.20, respectively. A key change is made in the waveforms of Fig. 2.20 compared

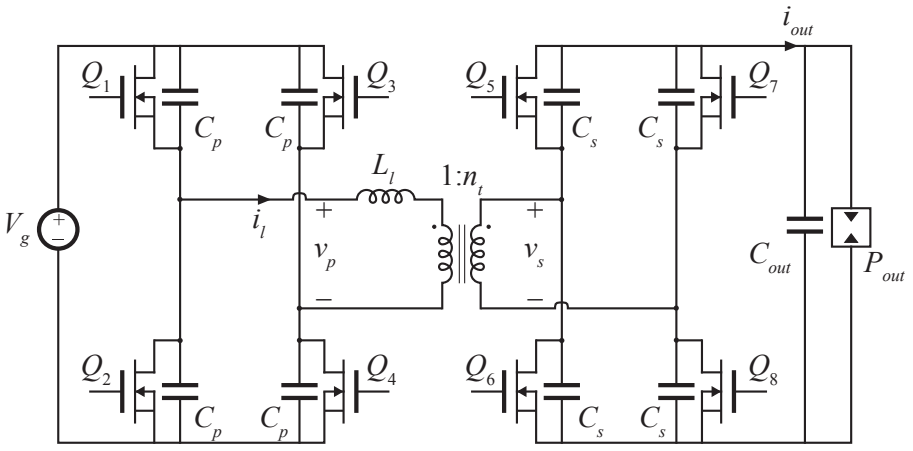


Figure 2.19: DAB converter schematic, including explicitly shown parasitic output capacitance of each MOSFET device.

to the previously developed operating waveforms: dead times are included in each of the switching transitions. That is, comparing the gate-drive waveforms of Fig. 2.20 to those of Fig. 2.10, small intervals have been inserted in both the primary and secondary switching transitions in which none of the MOSFET devices are conducting. These dead time intervals, t_1 on the primary and t_3 on the secondary, result in a resonance developing between the parasitic device capacitances and the tank inductance L_l. This induced resonant transition has the capability of transitioning all energy

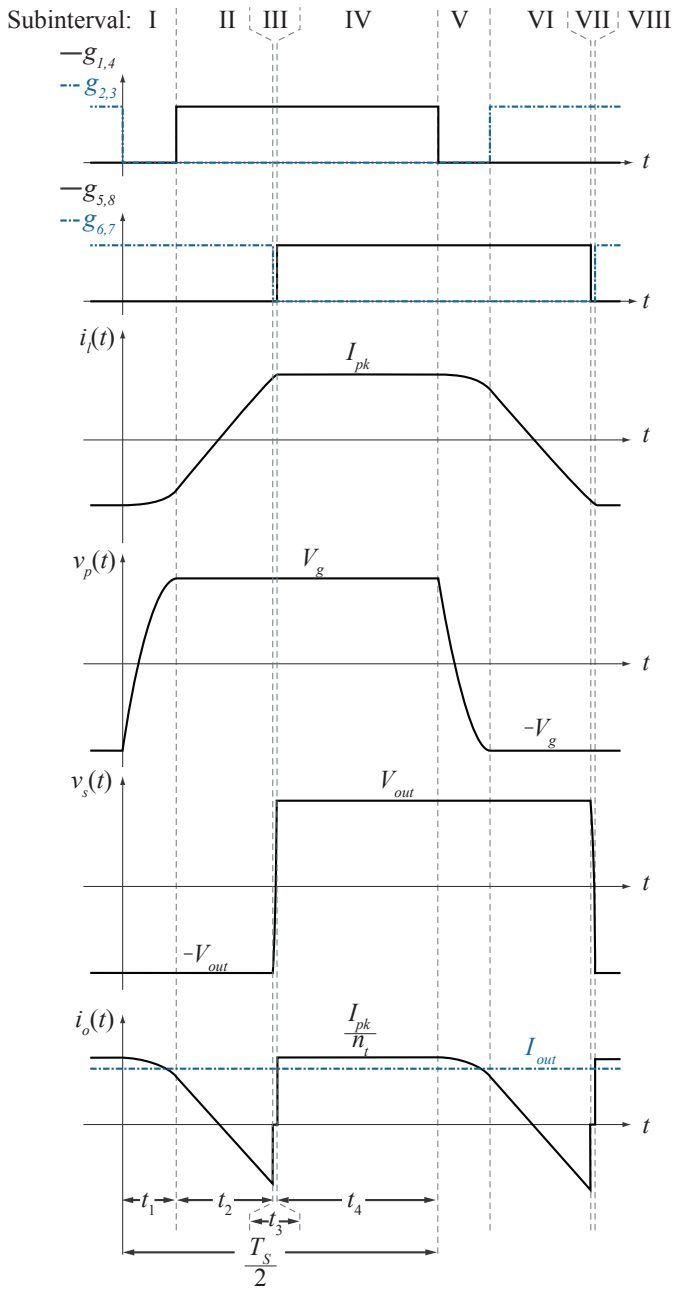


Figure 2.20: Key waveforms of the DAB converter under phase shift modulation, including the resonant ZVS dead time intervals.

from the parasitic device output capacitances to the tank inductance prior to device turn on. If this process is completed without fault, the result is a switch turn on with $V_{DS,sw} = 0$ and therefore full soft-switching of the converter, $P_{sw,ds} = 0$. The presence of ZVS therefore allows the converter to operate at high switching frequency – and therefore be constructed with small-volume magnetics – without incurring excessive efficiency penalties from switching loss.

The details of this resonant transition will be the studied in detail in the following chapter. However, at this point it is prudent to discuss the design impacts that ZVS operation will have on the converter. Examining the ZVT of the primary-side devices specifically, the ZVT can only occur if the tank inductor stores sufficient energy prior to the start of the resonance to transition all four primary-side capacitances C_p across the full input range. Thus a zero-voltage constraint is present in the circuit of the form

$$\frac{1}{2} L_l {I_{pk}}^2 > \frac{4}{2} C_p {V_g}^2 \ , \tag{2.41}$$

where for the given operating waveforms, I_{pk} is inductor current present just prior to the start of the resonant dead time interval. Because the current waveshape in phase-shift modulation is determined largely by the operating power level, the above inequality may be taken as a design constraint on the tank inductance

$$L_l > \frac{4 C_p {V_g}^2}{{I_{pk}}^2} \ , \tag{2.42}$$

which can be combined with (2.20) to yield

$$L_l > C_p \left(\frac{2 T_s V_g}{n_t I_{out} T_s + 8 C_p V_g} \right)^2 \ . \tag{2.43}$$

By using (2.20) to estimate the relation between I_{pk} and I_{out}, this result implicitly assumes that the dead times, and therefore the ZVS intervals, are relatively short and have little impact on current waveshapes. Results without this assumption are developed chapter 3.

When satisfied, the inequality in (2.43) results in the ability for the converter to fully ZVS all primary-side devices at an output power level greater than $P_{out} = I_{out} V_{out}$ [30]. Thus, for the purpose of maintaining ZVS even in the presence of peak currents, it is desirable to operate with a large tank inductance. This is in direct contrast to the previous analysis, which motivated the use

of the smallest achievable L_l in order to maintain low current stresses and low conduction losses throughout the converter. To illustrate the tradeoff, Fig. 2.11 is reproduced in Fig. 2.21 with the addition of a curve indicating the minimum output current required to obtain ZVS at the specified tank impedance $I_{o,ZVSmin}$. The curve added to the original plot is shown for a 100kΩ magnitude of capacitor impedance at the switching frequency, $Z_c = (2\pi f_s C_p)^{-1}$, again to allow the analysis to remain independent of switching frequency selection. In this example, for $f_s L_l < 525\Omega$ the

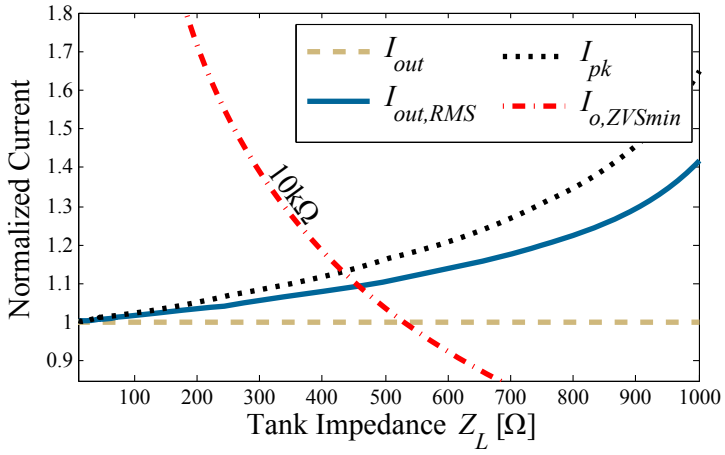


Figure 2.21: Normalized peak, average and RMS output current as well as the minimum output current required to obtain ZVS plotted against a range of inductor impedance magnitudes at the switching frequency $Z_L = 2\pi f_s L_l$ and a single 10kΩ value for the magnitude of the capacitance at the switching frequency, $Z_c = (2\pi f_s C_p)^{-1}$

minimum ZVS current $I_{o,ZVSmin} > I_{out}$ and therefore the converter will not obtain full ZVS. For $Z_L \geq 525\Omega$, ample energy is stored in the tank inductor at the onset of the primary dead time to obtain ZVS. However, further increases in tank impedance beyond $Z_L = 525\Omega$ result in uneccesarily elevated RMS currents in the converter. Therefore, considering only the single operating power plotted in Fig. 2.21, selecting a tank inductance equal to $L_l = 525/(2\pi f_s)$ will result in the minimum conduction losses possible while maintaining ZVS.

In general, this proposed approach to selecting tank inductance is one applicable method for approaching the tradeoff between switching and conduction losses in the case where only a single operating power P_{min} is considered most important. If L_l is made large enough such that

$I_{o,ZVSmin} = I_{out}$ at P_{min}, then the converter will obtain full ZVS at this operating point and all powers greater than P_{min}, with conduction losses additionally being optimized at P_{min}.

The analysis can additionally be applied to varying values of the primary side capacitance C_p, as may be present in a variety of real devices which could be used to implement the MOSFETs $Q_1 - Q_4$. The results of this application are shown in Fig. 2.22. Note that, as expected, a lower value of C_p, which correlates to increased Z_C, results in a lower current requirement to obtain ZVS of primary-side devices. It is therefore of interest to consider the tradeoffs associated with device

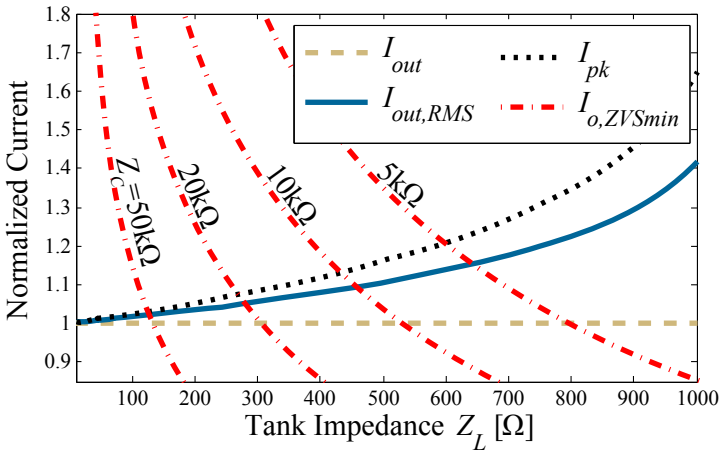


Figure 2.22: Variation in normalized peak, average and RMS output current are shown with respect Z_L with a multitude of curves for the minimum ZVS current $I_{o,ZVSmin}$ given for varying values of Z_C. For the case of each value of Z_C, ZVS is only obtained at I_{out} if Z_L is selected such that $I_{o,ZVSmin} < I_{out}$.

selection, including the feasibility of selecting devices with very low C_p to implement $Q_1 - Q_4$ and facilitate the ability to simply obtain a very small P_{min} and thus a wide range of power levels over which ZVS may be maintained.

2.3.3 Device Selection

In selecting optimal devices to implement MOSFETs $Q_1 - Q_8$, it is desired to reduce the contribution to converter loss of inherent parasitic elements such as Q_g, C_{ds} and r_{on}. Unfortunately, in even the most advanced devices available, it is not possible to simultaneously minimize all

parameters. The necessary tradeoff in them is understandable by assessing the dependence of each on overall device size.

2.3.3.1 Device Figures of Merit

Considering first the ability of the power electronics engineer who has available only commercial, discrete MOSFET devices, there remains significant ability to alter the values of MOSFET parasitics in two manners. First, the selection of devices will result in different distributions of these three parameters based on the inherent characteristics of the fabrication process used to create each device. Second, even with only a single process and device, the individual MOSFET devices may be paralleled in order to effectively reduce the resistance seen in-circuit, at the cost of increases in the stored charge of the effective device. Fig. 2.23 shows the result of paralleling three individual MOSFET devices of the same type. Replacing the devices with their parasitic model of Fig. 2.13(c), the circuit of Fig. 2.23(b) is obtained, which simplifies to the equivalent in Fig. 2.23(c) under the continued assumption of ideal diode behavior and perfectly matched devices, which will cause the three switches to always commutate simultaneously. Thus, for any MOSFET with individual parasitics, the on-resistance may be reduced by a factor of n and the stored charges including Q_g and C_{ds} may be increased by n when n devices are paralleled.

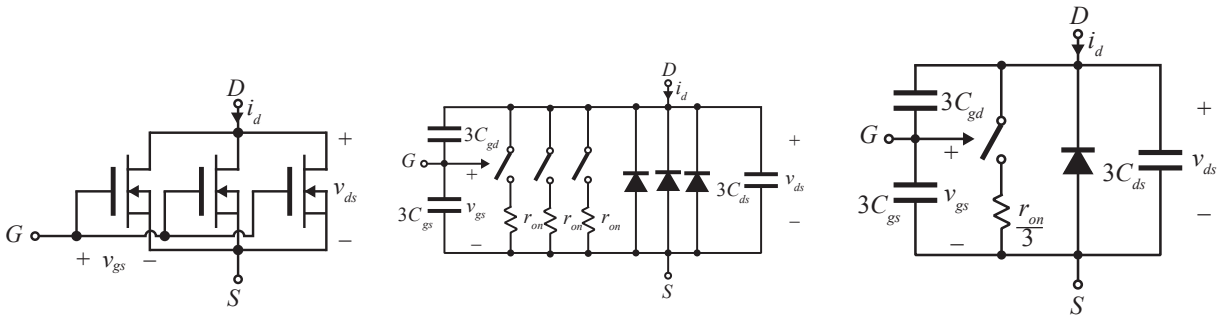


Figure 2.23: Schematic representation of three MOSFETs in parallel using their circuit symbols (a) and their equivalent circuit loss model (b). In (c), the loss model is simplified assuming ideal matching between each device.

Though this relationship has been considered for discrete devices, it remains valid when considering the size of a custom device implemented on a silicon substrate. In general, increasing the total area of a device on-chip proportionally decreases r_{on} and increases Q_g and C_{ds}. Thus, whether discrete devices or custom solutions are used to implement the switching devices, it is useful to compare the merits of a device line or fabrication process independent of device size. In order to do so, two figures of merit are considered which effectively cancel the dependence on device size by taking the product of r_{on} which is inversely proportional to size, and one of the stored charges, both of which are directly proportional to device size. These two resulting FOMs, $Q_g r_{on}$ and $C_{ds} r_{on}$ can be used to compare devices based on the relative tradeoff between conduction and switching losses, with device size as a second independent parameter available to determine the actual value of each.

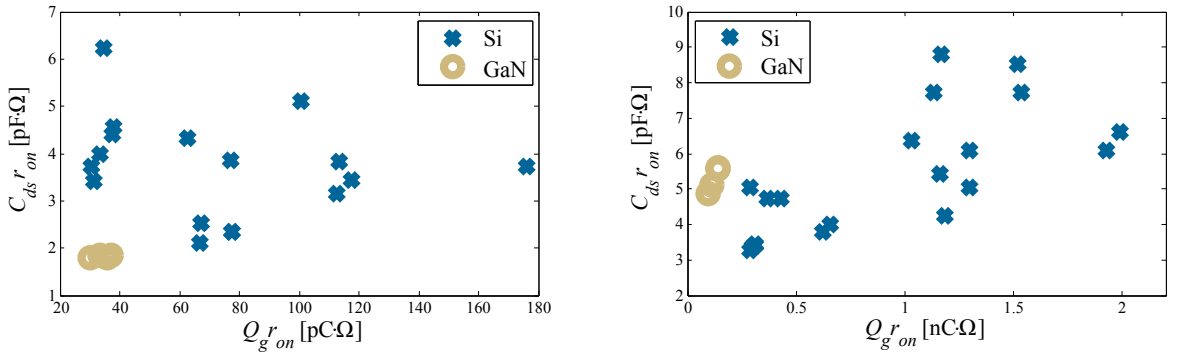
Once the optimal FOM devices are selected, further analysis of the DAB converter, as presented in the following chapters, will inform the selection of the device size in order to define the actual values of parasitic components from the normalized FOMs. This selection of size is motivated by knowledge of the relative magnitudes of conduction losses: small area devices will be appropriate when losses which depend on stored charge dominate, while large area devices should be used to implement devices dominated by conduction losses.

2.3.3.2 Gallium Nitride FOM comparison

Additionally, of particular interest in assessing the merit of discrete devices, is the inclusion of the recently available Gallium Nitride (GaN) FETs, which offer an alternative to traditional silicon (Si) devices. Owing largely to it's wide bandgap and large critical breakdown field – greater than 3x and 10x that of silicon, respectively [48,49] – GaN has been touted as a potential substrate for creating drop-in replacements for traditional silicon-based devices with significantly improved switching behavior in-circuit.

Despite its popularity in research, at the time of this research only a single series of GaNFETs was available for commercial purchase. Within this series, the highest available breakdown voltage

of an individual part is $V_{DS,max} = 200$ V [50]. Due to their promise for improved switching behavior, and because it is of interest to include GaN devices in the assessment of achievable efficiency in the DAB converter, devices are compared and the analysis of converter operation is carried out with a input bus voltage of $V_g = 150$ V rather than the previously discussed 400 V so that both GaN and Si devices may be included. Taking into account the reduced V_g, the two proposed FOMs are compared among the available GaN devices and a representative sampling of state-of-the-art Si MOSFETs which are potential candidates for implementing both the high-voltage input and low-voltage output devices, $Q_1 - Q_4$ and $Q_5 - Q_8$, respectively. The FOMs of these devices are plotted in Fig. 2.24. In assessing the relative merits of GaN and Si devices from this figure, it is



(a) Low Voltage 20-40 V $V_{DS,max}$ devices

(b) High Voltage 150-200 V $V_{DS,max}$ devices

Figure 2.24: Comparison of two switching FOMs for representative silicon MOSFETs and commercially-available GaNFETs, including both low-voltage secondary devices (a) and high-voltage primary devices (b)

apparent that silicon devices are available which come close to matching either the $Q_g r_{on}$ or $C_{ds} r_{on}$ FOM, but none match or exceed both simultaneously.

2.3.3.3 Other Parasitics in Si and GaN

Other parasitic behaviors are present in any real implementation of a transistor, including parameters for gate resistance, source and drain inductance, and body diode characteristics, in addition to nonlinear variations in any of the developed parasitic elements with parameters such as

gate voltage, drain voltage or current, and temperature. The contribution of these characteristics to device losses in a power converter can potentially be significant, however their inclusion in device selection does not lend itself to simple FOM tradeoffs, as these characteristics are largely determined only by the fabrication process. Additional details concerning an approach to address the nonlinearity of the output capacitance are detailed in Section 4.1.

Additionally, when comparing GaN and Si devices, a number of differences should be taken into account when selecting candidate devices to implement the converter [48, 49, 51–53]. GaN, by its nature, does not have an intrinsic body diode and therefore will be highly inefficient is exposed to reverse conduction operation $V_{gs} = 0$ V. Additionally, GaN MOSFETs are inherently depletion-mode devices; a conducting channel is present in the device at $V_{gs} = 0$ and requires a negative gate-to-source voltage to remove the inversion layer, unlike traditional enhancement-mode Si MOSFETs. In the available commercial devices [50], this inconvenience has been overcome through alterations in device characteristics to create an enhancement-mode device, however the resulting transistor has non-zero DC gate current which limits applied gate-to-source voltage range to a narrow range of permissible values which do not result in device failure.

Because of these issues with GaN devices, and because of the inherent risk of working with new technologies, both Si and GaN implementations of the DAB converter are considered in this thesis. Silicon devices are selected with specific consideration of the $C_{ds}r_{on}$ characteristic rather than the $Q_g R_{on}$ FOM. This allows the input-to-output characteristics of the converter power stage, including its efficiency, to be compared between GaN and Si implementations, as silicon devices are available which perform nearly on par with GaN at both the high voltage and low voltage ports, though with significantly higher gate charge for a set r_{on}. The additional losses in the silicon devices' gate drive circuits will be considered – though not emphasized – due to the perceived possibility of achieving significant reduction for similar circuit operation in the GaN implementation case.

Summary

Switched-mode power supplies (SMPS) present the only feasible option for implementing the high voltage conversion ratio, low-power, DC-to-DC converters necessary in the HVDC and other data center power distribution architectures. Among this class of circuits, the dual active bridge (DAB) converter is attractive due to its capability to operate with low switch stresses while simultaneously maintaining zero-voltage switching (ZVS) of all devices.

In order to design the DAB converter, a number of tradeoffs must be assessed. Three of these tradeoffs are repeated in Table 2.4, where the perceived benefits of both increasing or decreasing an given parameter are listed. These general principles, though derived from a simplified analysis of the converter, will continue to hold true even under further refinement of analysis. The following section will detail analysis techniques which may be used to solve for converter operational waveforms and losses/efficiency in greater detail and precision, and will propose further guiding principles by which the design tradeoffs may be undertaken.

Table 2.4: Design tradeoff summary

Parameter	Increasing	Decreasing
Switching Frequency f_s	Smaller Magnetics	Decreased Switching Losses
Tank Inductance L_l	Wider ZVS Range	Increased RMS Currents
Device Size	Smaller r_{on} and conduction losses	Smaller stored charge and switching losses

Chapter 3

Steady State Analysis of the DAB Converter

Previous analyses of the DAB converter have largely focused on high power and low switching frequency operation, as shown in Fig. 3.1. Under these conditions, sufficient energy is available in the tank inductance at the initiation of a ZVS interval to complete the resonant transition in a very short amount of time relative to the switching frequency, $t_1 \ll T_s$. In this case, converter steady-state operation is well approximated by the solution which considers only the linear intervals, neglecting the contributions of ZVS intervals, as presented in (2.19)-(2.23). The resulting converter behavior is modeled by the equivalent circuit of Fig. 3.2, which considers only the square-wave approximated waveforms of the voltages $v_p(t)$ and $v_s(t)$.

As the power level of the DAB converter is reduced, less energy is available to obtain ZVS, and the resulting ZVS interval duration will increase. Additionally, at higher switching frequencies, the duration of a set ZVS interval occupies a greater portion of each switching period. Together, the reduction in power and increase of switching frequency result in significant contributions to converter behavior from the ZVS intervals which are ignored in the traditional, linear converter analysis [25,30,54–71]. Even in those studies which do consider the dynamics of the converter during these intervals, the resonant circuit behavior is often either approximated [72, 73] or simulated [74].

Because of the need to minimize the overall converter footprint, and the resulting necessity of an increased switching frequency, as well as the modes power level requirements in the data center application, it is necessary to address the resonant intervals directly and with little approximation in the analysis and design of the DAB converter. A 1 MHz switching frequency will be used in

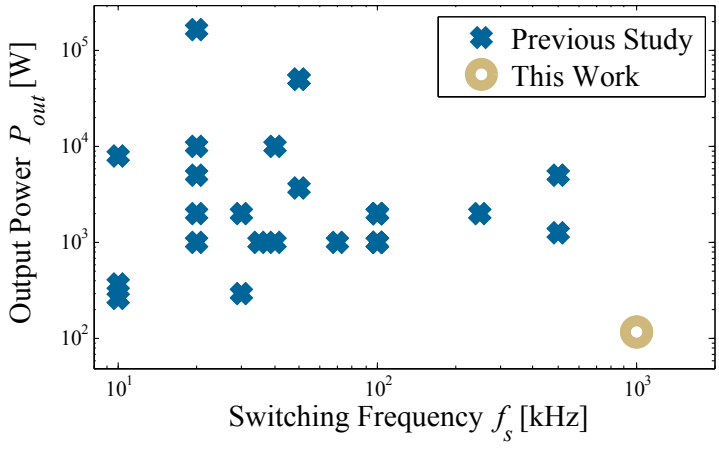


Figure 3.1: Switching frequency and rated output power level of previous studies of the DAB converter, as well as those of the work presented in this thesis. Note that the state of the art for DAB analysis focuses on the higher power and lower switching frequency design space [25,30,54–74].

the design analysis henceforth, to facilitate the possibility of a reduced converter footprint. In order to further verify the significance of resonant interval dynamics on converter operation in this design space, as compared to that of previous studies, converter simulations are compared to analytical predictions of behavior in Fig. 3.3 which make use of the squarewave model without ZVS dynamics which is widely present in literature. It can be seen that, while converter behavior is well predicted by the traditional model at low switching frequency and high power, the high switching frequency, low-power operating point behavior differs significantly from the prediction of the simplified analysis. It is therefore desired to perform analysis of the DAB converter which takes account the resonant ZVS transitions explicitly.

3.1 DAB Equivalent Circuit Modeling

In order to begin the DAB converter analysis, the operating waveforms derived in the previous chapter are considered in eight subintervals, as labeled in Fig. 2.20. These subintervals are defined by the current state of each switched-mode transistor, given in Table 3.1. There are four unique subintervals which are repeated in each half-period. Only the conducting device pairs and polarities of tank voltages and currents changing between the two half-periods; the circuit behavior, and

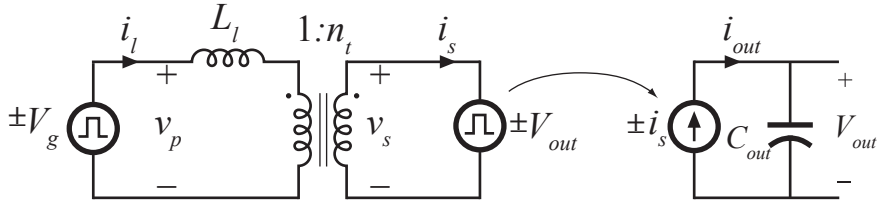
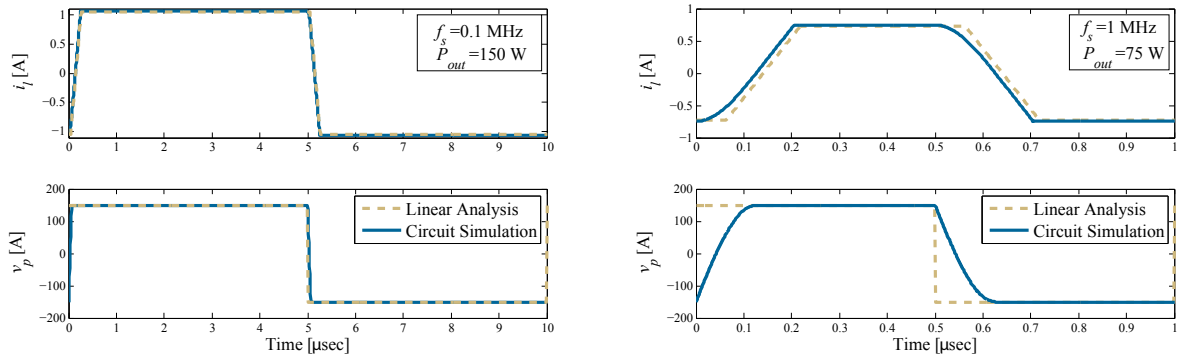


Figure 3.2: Linear, squarewave-only model of DAB converter operation. Though accurate for low switching frequency and high power, this model neglects ZVS transitions which are significant in the proposed operating conditions.

input/output waveforms are identical. It is therefore sufficient to examine subintervals I-IV only in solving the converter operation.

Knowing the state of each switch, it is possible to construct equivalent circuits for the DAB converter during each of subintervals I-IV which model the behavior of the tank waveforms in each set of switch states. In order to maintain simplicity of this analysis, on-resistances of the switches will be neglected, though output capacitances must be included due to the perceived importance of the ZVS interval dynamics. Additionally, the output capacitance of the circuit C_{out} will be assumed sufficiently large such that, in steady-state operation, the output voltage may be approximated as DC within a single switching period.

During subintervals I&III, input and output switch bridges effectively short their respective voltages to the tank, resulting in equivalent circuits as shown in Fig. 3.4 and Fig. 3.6. During subintervals II&IV, one of the bridges has all four devices off, resulting in a capacitive load presented to the tank, according to the parasitic output capacitances of the bridge devices, diagrammed in Fig. 3.5 and Fig. 3.7. As long as all four device capacitances are equal, the currents through each of the four capacitances must be equal in magnitude; this is due to the fact that any two capacitors oriented in half-bridge configuration have the same dv/dt and both half bridges will have the same total current flowing into them (e.g. i_l for both primary half-bridges). There is therefore zero current flowing in the input source during the primary ZVS transition, and zero current at the converter output during the secondary ZVS transition, and the effective load on the tank during each interval is a series-parallel combination of device output capacitances which has magnitude



(a) (b)

Figure 3.3: Comparison between circuit simulation and linear, squarewave model prediction for steady-state inductor current $i_l(t)$ and primary voltage $v_p(t)$ at two different power levels and switching frequencies. $L_l = 32\mu$H and $C_p = 200$nF are used, with $V_g = 150$V and $V_{out} = 12$V

Table 3.1: Description of each subinterval during phase-shifted DAB operation

Subinterval	Conducting Devices		Duration		Description
	Primary	Secondary			
I	–	Q_6 & Q_7	t_1		Primary ZVS transition
II	Q_1 & Q_4	Q_6 & Q_7	t_2	$\frac{T_s}{2}$	Inductor current ramping
III	Q_1 & Q_4	–	t_3		Secondary ZVS transition
IV	Q_1 & Q_4	Q_5 & Q_8	t_4		Main power delivery
V	–	Q_5 & Q_8	t_1		Primary ZVS transition
VI	Q_2 & Q_3	Q_5 & Q_8	t_2	$\frac{T_s}{2}$	Inductor current ramping
VII	Q_2 & Q_3	–	t_3		Secondary ZVS transition
VIII	Q_2 & Q_3	Q_6 & Q_7	t_4		Main power delivery

equal to that of a single device, though the effective voltage swing across it is double that of the actual device capacitances.

In order to solve converter operation, including parameters such as the required phase shift, optimal dead times, and RMS and average currents, each subinterval equivalent circuit can be examined independently and the results from each combined to obtain overall circuit behaviors. For all intervals other than those in which ZVS is obtained, the subinterval solution is simple due the linear,first-order nature of the equivalent circuit. In the ZVS transition intervals, however, a second-order resonant circuit is obtained, and the solution to converter waveforms requires additional detail.

3.2 Resonant Interval Analysis

Using subinterval I as an example, behavior of the equivalent circuit of Fig. 3.4(b) is defined by the pair of differential equations given by for each state

$$-\frac{V_{out}}{n_t} - v_p(t) = L_l \frac{d}{dt} i_l(t) \ , \tag{3.1a}$$

$$i_l(t) = C_p \frac{d}{dt} v_p(t) \ , \tag{3.1b}$$

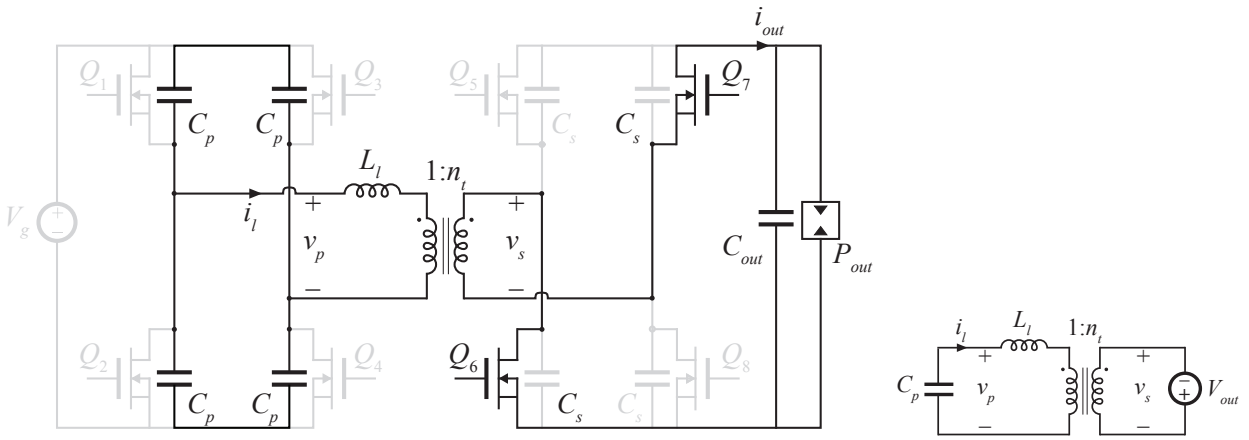


Figure 3.4: Conducting devices (a) and tank-equivalent circuit (b) of the DAB converter during subinterval I

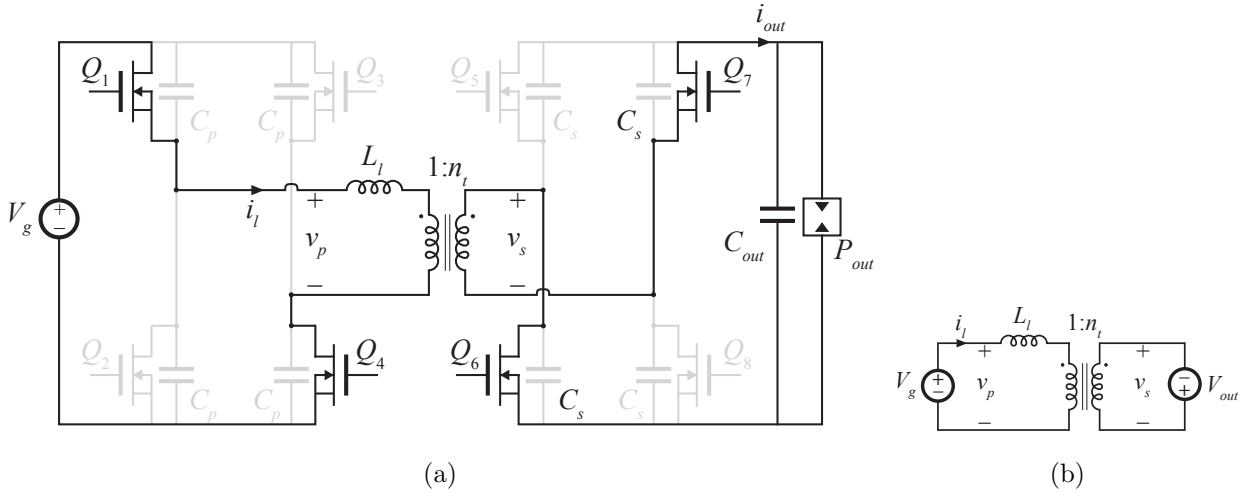


Figure 3.5: Conducting devices (a) and tank-equivalent circuit (b) of the DAB converter during subinterval II

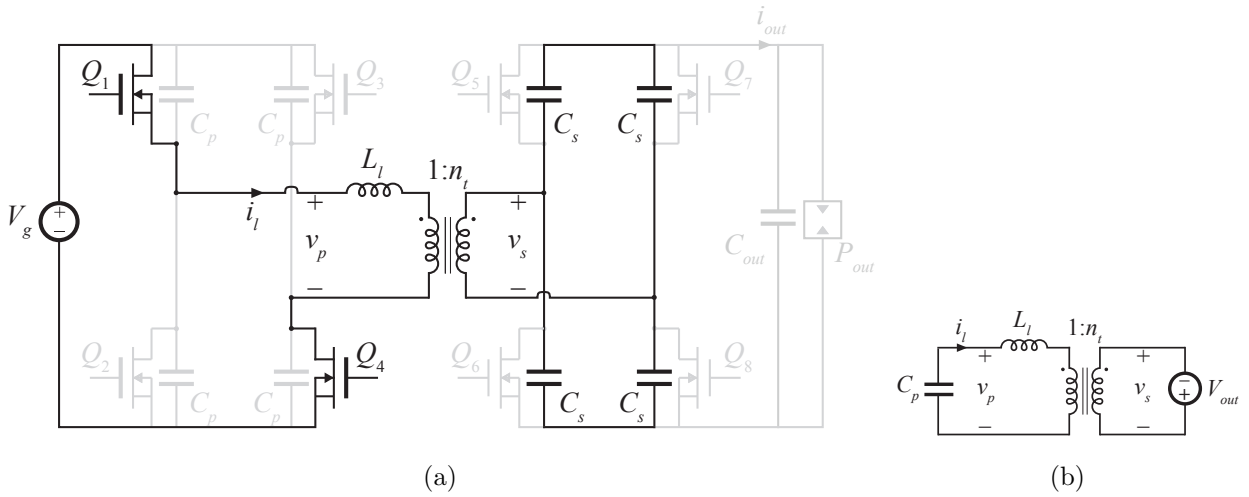


Figure 3.6: Conducting devices (a) and tank-equivalent circuit (b) of the DAB converter during subinterval III

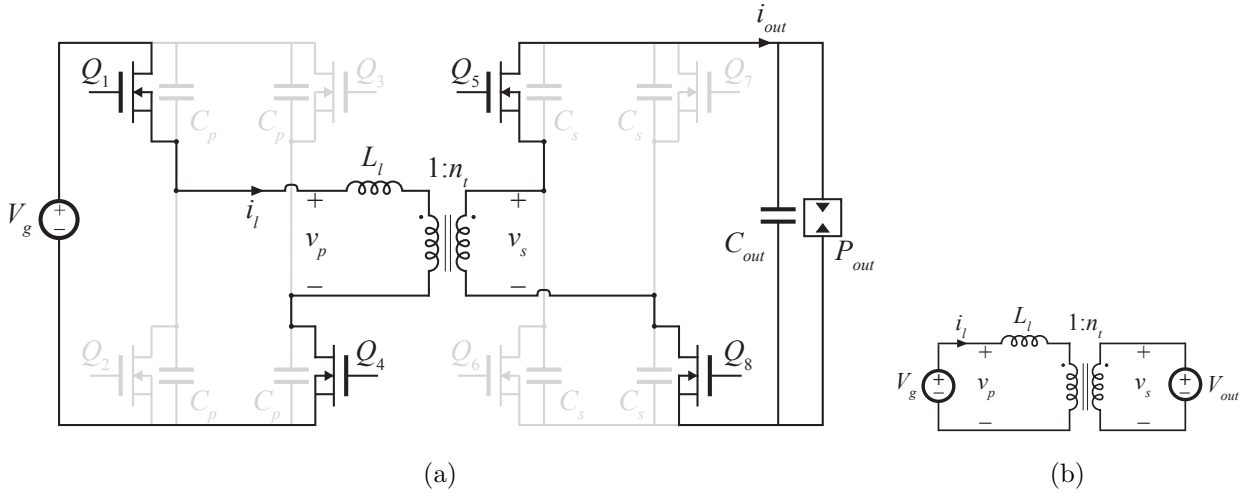


Figure 3.7: Conducting devices (a) and tank-equivalent circuit (b) of the DAB converter during subinterval IV

which can be combined to form the second-order differential equation

$$L_l C_p \frac{d^2}{dt^2} v_p(t) + v_p(t) = -\frac{V_{out}}{n_t} \ . \tag{3.2}$$

In addition, examining the converter waveforms, the initial conditions of the equivalent circuit in subinterval I are

$$v_p(t=0) = -V_g \ , \tag{3.3a}$$

$$i_l(t=0) = -I_{pk} \ . \tag{3.3b}$$

Using traditional methods, either by solving the differential equations or using laplace transforms, the solution for capacitor voltage and inductor current during the resonance are found as

$$v_p(t) = -I_{pk} R_0 \sin \omega_0 t - \left(\frac{V_{out}}{n_t} - V_g \right) \cos \omega_0 t - \frac{V_{out}}{n_t} \ , \tag{3.4a}$$

$$i_l(t) = -I_{pk} \cos \omega_0 t + \frac{\left(\frac{V_{out}}{n_t} - V_g \right)}{R_0} \sin \omega_0 t \ , \tag{3.4b}$$

with ${\omega_0}^{-2} = L_l C_p$ and ${R_0}^2 = L_l / C_p$. With this solution in hand, in addition to a similar solution for the secondary resonant interval and the analysis of the linear intervals in the previous chapter, all necessary converter solution elements have been developed to analyze the converter steady-state behavior. For example, the dead time required to obtain ZVS, assuming sufficient energy is available in the inductor at the start of the interval, is given by

$$t_1 = \frac{1}{\omega_0} \cos^{-1} \left(\frac{-\frac{V_{out}}{n_t} - V_g}{\sqrt{{I_{pk}}^2 {R_0}^2 + \left(-V_g + \frac{V_{out}}{n_t} \right)^2}} \right) - \frac{1}{\omega_0} \tan^{-1} \left(\frac{-I_{pk} R_0}{-V_g + \frac{V_{out}}{n_t}} \right) \ . \tag{3.5}$$

Though correct, these equations are cumbersome for hand analysis of the converter, and solutions developed though application of differential equation theory are nonintuitive. To simplify the analysis further, the established techniques of state plane analysis [75–78] are employed in the following section to give insight into converter operation and further simplify the analysis by allowing key parameters of circuit operation to be solved using geometric techniques.

3.3 State Plane Analysis

In the technique commonly known as state plane analysis [75–78], the states of a second-order resonant circuit under examination are normalized and plotted with respect to one another in a parametric plot termed the "state plane". These states, namely the capacitor voltage and inductor current, are normalized in such a way that the resulting state plane contains only circular and linear segments. This results in a plot which is simple to analyze via geometric arguments and, understanding the correspondence between the geometry of the state plane and the circuit waveforms which it comprises, an ease of obtaining arbitrary characteristics of the resonance.

The application of normalization and state plane solution are reviewed in the following section, and applied to the DAB converter thereafter.

3.3.1 Review of State Plane Analysis

For power converters with significant resonant components to operation, a normalized approach has long been the preferred method for analyzing circuit behavior due to the heavy dependence of operation on the elements' resonant frequency [79]. To begin the normalization process, base voltages and currents are selected from which the normalization of converter waveforms will take place. The base voltage may be selected arbitrarily, but for the circuit of subinterval I, the most convenient selection is

$$V_{base} = V_g \ . \tag{3.6}$$

The base current then follows from this selection as

$$I_{base} = \frac{V_{base}}{R_0} \ . \tag{3.7}$$

The advantage of this particular relation between base current and voltage can be seen when the normalization is applied to the solution developed in (3.4). The result is a pair of normalized, unitless waveforms, with notation as defined by the University of Colorado

$$m_p(t) = \frac{v_p(t)}{V_{base}} \ , \tag{3.8a}$$

$$j_l(t) = \frac{i_l(t)}{I_{base}} \ . \tag{3.8b}$$

Additionally, it will prove useful to define normalized switching frequency $F = f_s/f_0$ and converter conversion ratio $M_N = V_{out}/n_t V_g$. Applying this normalization to equations (3.4a) and (3.4b),

$$m_p(t) = -J_{pk} \sin \omega_0 t - (M_N - 1) \cos \omega_0 t - 1 \ , \tag{3.9a}$$

$$i_l(t) = -J_{pk} \cos \omega_0 t + (M_N - 1) \sin \omega_0 t \ . \tag{3.9b}$$

In addition to being significantly simplified, these equations have the advantageous property that

$$(m_p(t) + 1)^2 + j_l(t) = {J_{pk}}^2 + (M_N - 1)^2 \ , \tag{3.10}$$

which defines a circle in the two-variable plane bounded by $m_p(t)$ and $j_l(t)$ axes. The radius of the circle,

$$r_1 = \sqrt{{J_{pk}}^2 + (M_N - 1)^2} \ , \tag{3.11}$$

is a normalized value which represents the energy ringing back and forth between inductor and capacitor, while the center at $(m_p, j_l) = (-1, 0)$ represents the DC solution of the circuit, namely $i_l = 0$ and $v_p = -V_g$. Indeed, these correlations between circuit properties and the geometric parameters of the $m_p(t)$–$j_l(t)$ "state plane" hold true for second-order resonant circuits of arbitrary DC bias and initial conditions, wherein the two normalized points defined by the initial and DC solutions are sufficient to define the circle which the state progressions will have as a trajectory [75, 78].

For the DAB converter primary ZVS transition, operating as a DCX with $V_{out} = n_t V_g$ (i.e. $M_N = 1$), a segment of this circle is plotted in Fig. 3.8 for the equivalent circuit during subinterval I. The solid portion of the circle defined by the L_l–C_p resonance is the segment of interest. This arc carries the system from its initial condition to the point $(m_p, j_l) = (1, -J_1)$. Denormalizing, as diagrammed in Fig. 3.9 this point corresponds to a voltage $m_p = 1 \mapsto v_p = V_g$, which indicates that the primary side devices have completed a full ZVS transition, and the primary switches may be commutated in a losssless manner. During the ZVT, the inductor current moves in a resonant manner from its initial value $j_l = -J_{pk} \mapsto i_l = -I_{pk}$ to a final value at the end of the

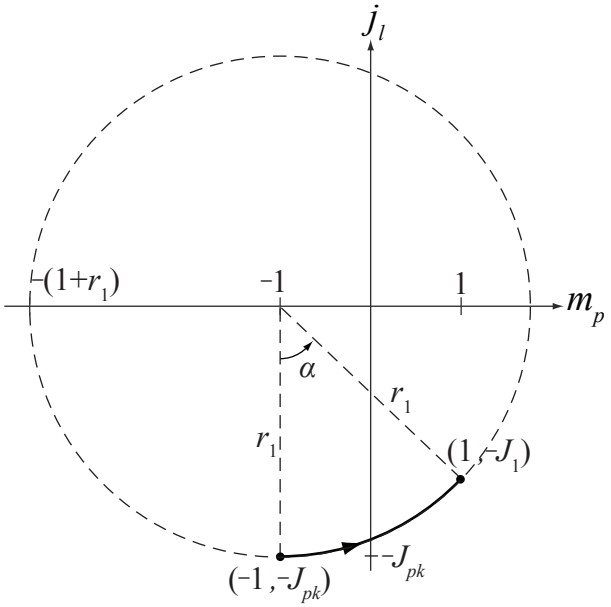


Figure 3.8: State plane corresponding to subinterval I of the DAB converter

transition $j_l = -J_1 \mapsto i_l = -I_1$. As was done in the non-normalized case, it is desired to solve for the duration of this resonant interval, t_1. Ostensibly, it is clear that as the circular arc is traversed, the state evolution will be periodic about a circular angle $\theta = 2\pi$; therefore, the state plane and non-normalized periodicity may be mapped to one another, $\theta = 2\pi \mapsto t = 2\pi/\omega_0$, and it can be concluded that angles within the normalized state plane map to times in the modeled resonant circuit. This being the case, the dead time required to complete the resonant transition in subinterval I can be solved by denormalizing the resonant angle α in Fig. 3.8 to obtain

$$t_1 = \frac{\alpha}{\omega_0} \ . \tag{3.12}$$

The angle α is then solved from the state plane diagram by noting that the resonant radius $r_1 = J_{pk}$ for the given mode of operation. Therefore, by trigonometric arguments,

$$\alpha = \sin^{-1}\left(\frac{2}{J_{pk}}\right) \ , \tag{3.13}$$

which is significantly simplified compared to the solution given by the general solution to the differential equation in (3.5), though valid only to the particular initial conditions and output voltage which are relevant to the DAB with $M_N = 1$.

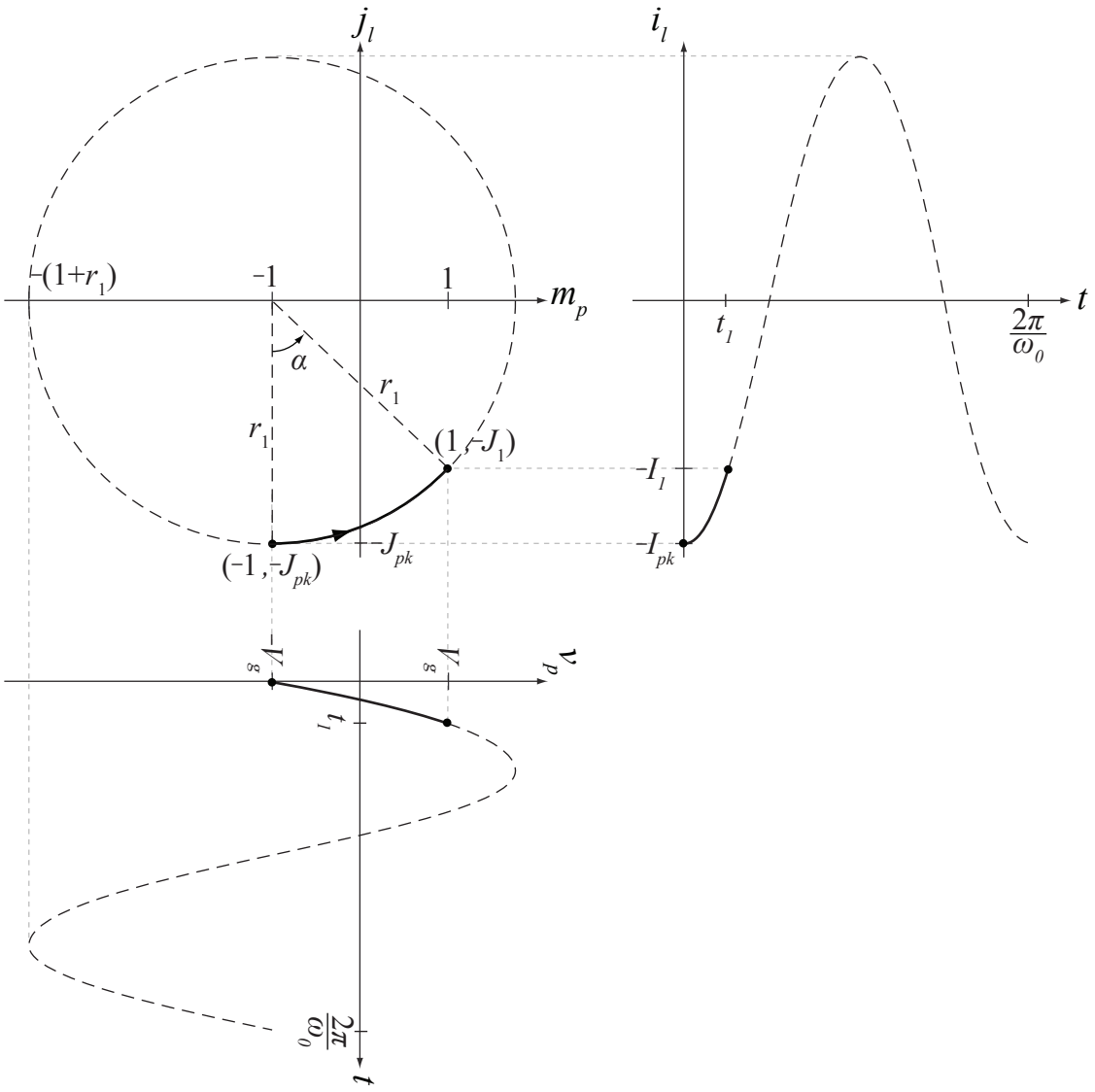


Figure 3.9: Correspondence between normalized state plane of subinterval I and the denormalized, time-domain inductor current and primary voltage waveforms in the DAB converter

In the full DAB converter, the remainder of the circle in the state plane beyond the solid line shown will not be traversed. Though the remaining portion of the trajectory is valid for the resonant circuit present in subinterval I, once the circuit reaches $m_p = 1$, commutation of switches will occur, altering the equivalent circuit to that of subinterval II, and thereby altering the state plane trajectories. In order to use state plane analysis to solve the DAB converter, a full converter state plane which consists of multiple segments, each with differing dynamics as defined by one of the developed equivalent circuit, must be employed.

3.3.2 State Plane Analysis Applied to the DAB Converter

State plane analysis has not previously been applied to the DAB converter. This is justified by the common exclusion of ZVS intervals in converter analysis in literature; when only the linear intervals of converter operation are considered, there is no benefit to using state plane techniques, which are advantageous in their simplification of resonant interval solutions. Because the ZVS intervals are expected to be significant in the high-frequency, low-power operation of interest, state plane analysis becomes an attractive option for the steady-state analysis of the DAB converter including ZVS intervals, and will be applied in this section.

The state planes of the DAB converter for both the primary and secondary resonances are shown in Fig. 3.10, along with the time domain waveforms to which they correspond. Table 3.2 lists the time domain waveforms and values of the DAB converter and their corresponding normalized, unitless variables in the state plane. Because the DAB converter operates with both resonant

Table 3.2: DAB Primary State Plane Naming Conventions

Time Domain	$i_l(t)$	$v_p(t)$	$v_s(t)$	V_g	I_1	I_2	I_{pk}	t_1	t_2	t_3	t_4
Primary State Plane	$j_l(t)$	$m_p(t)$	$m_s(t)$	1	J_1	J_2	J_{pk}	α	β	δ	ζ

intervals (I & III) and non-resonant intervals (II & IV), the state plane correspondingly contains both linear and circular segments. This type of converter is often termed "quasi-resonant" [47, 77, 80–82]. Additionally, it is necessary to develop two unique state planes, the previously discussed

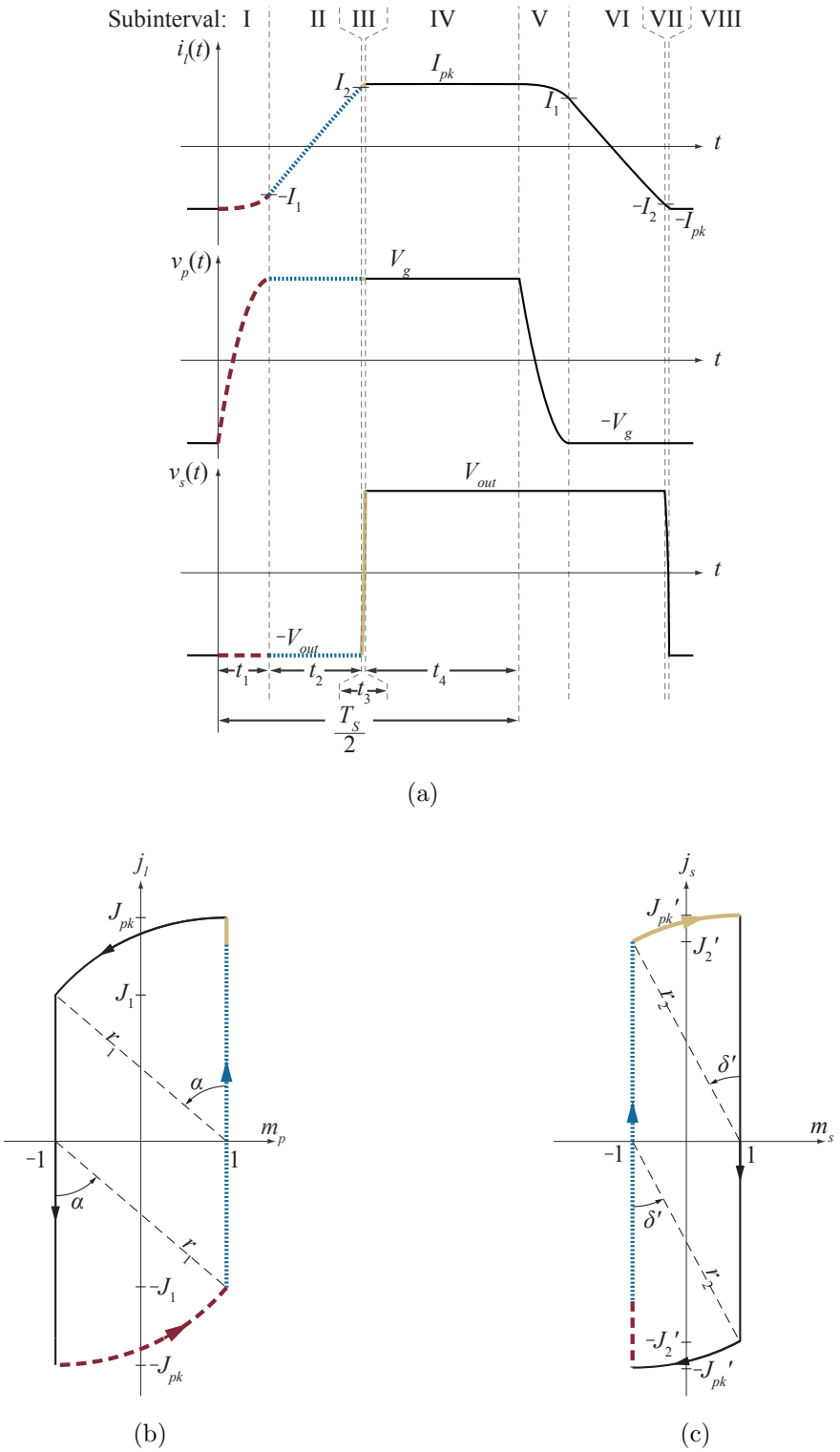


Figure 3.10: DAB time domain waveforms (a) as they correspond to the primary (b) and secondary (c) state planes. Line formatting shows the corresponding segments defined by subintervals I-III.

m_p–j_l state plane which describes the behavior of inductor current and primary side voltage, as well as the m_s–j_s state plane, which describes the resonance between the inductor current and secondary voltage, with the transformer turns ratio incorporated. The secondary normalization is with alternate base voltage and current due to a different capacitance, C_s, present in the circuit

$$m_s(t) = \frac{v_s(t)}{V_{out}} \ , \tag{3.14a}$$

$$j_s(t) = \frac{\frac{i_l(t)}{n_t} R_0{}'}{V_{out}} \ , \tag{3.14b}$$

where the inclusion of a prime ($'$) indicates that normalization is taken with respect to the secondary side parameters $V_{base} = V_{out}$ and $(R_0{}')^2 = {n_t}^2 L_l / C_s$, which uses the secondary side resonant capacitance C_s and the tank inductance reflected through the transformer turns ratio to the secondary in normalization. Equating values on the primary and secondary state planes can therefore be accomplished as, e.g. for normalized peak current

$$J'_{pk} = \frac{J_{pk}}{n_t} \sqrt{\frac{C_p}{C_s}} \ . \tag{3.15}$$

3.3.2.1 ZVS Condition in DAB Converter

Despite very similar appearance, it is important to note that the state plane for the primary-side transition is traversed in a counter-clockwise manner, while the state plane for the secondary transition is traversed in a clockwise manner. Examining the resonant transition intervals in the state planes, this directionality is indicative of an inductor current whose magnitude is decreasing during the primary transition, but increasing during the secondary transition. Therefore, though the primary ZVS transition is only achieved when the inductor begins the interval with sufficient energy, whereas secondary ZVS can be achieved independent of the energy stored in the inductor at the start of the secondary dead time, for the given mode of operation.

It was previously shown in the time domain that primary ZVS is only obtained if (from (2.42))

$$I_{pk} > 2V_g \sqrt{\frac{C_p}{L_l}} \ , \tag{3.16}$$

and therefore there is a minimum power P_{min} at which primary ZVS may be achieved. From the primary state plane of Fig. 3.10, it can be visually solved that full ZVS is only achieved if the radius of the resonance $r_1 > 2$. If this is not the case, then the circular segment will not be large enough to carry the resonance from its starting point at $m_p = -1$ all the way to $m_p = 1$, at which point ZVS is achieved. Further, by considering the starting point at $(-1, -J_{pk})$, and noting that the radius stays constant throughout the circular arc, it is apparent that the radius $r_1 = J_{pk}$. Thus, the ZVS condition in the normalized state plane is given by

$$J_{pk} > 2 \ , \tag{3.17}$$

which, when denormalized, gives the same result as (3.16). For the secondary transition, no such condition exists.

To understand how this condition relates to converter output power, as well as obtain a general solution for steady-state converter waveforms, the full details of the converter state planes are solved.

3.3.2.2 DAB State Plane Solution

The converter solution in the normalized domain can be approached by considering each subinterval in a single half-period independently, then aggregating the results from each to solve the averaged output current of the converter [83].

Subinterval I: In subinterval I, ZVS is achieved via a resonant transition which appears in the primary state plane of Fig. 3.10(b). The angle α is given previously in (3.13). Examining the triangle formed by r_1 and the m_p axis, the inductor current at the end of subinterval I is given by

$$J_1 = \sqrt{{J_{pk}}^2 - 4} \ . \tag{3.18}$$

Subinterval II: Because subinterval II is linear, it appears as only line segments in both primary and secondary state planes. It is therefore most advantageous to consider the time domain waveforms in order to solve the relation between the interval duration and its ending current, I_2.

A voltage of $V_g + V_{out}/n_t = 2V_g$ is applied to the inductor during the course of the subinterval. Therefore,

$$t_2 = \frac{L_l}{2V_g}\left(I_1 + I_2\right) \ . \tag{3.19}$$

Normalizing by multiplying both sides by w_0, the equation for the normalized phase shift duration, $\beta = t_2\omega_0$ is obtained

$$\beta = \frac{1}{2}\left(J_1 + J_2\right) \ . \tag{3.20}$$

Subinterval III: The ZVS transition in subinterval III takes place in the secondary state plane, and has identical geometry to that of subinterval I in the primary state plane. The same steps are taken to solve the interval duration

$$\delta' = \sin^{-1}\left(\frac{2}{{J_{pk}}'}\right) \ , \tag{3.21}$$

and the starting current,

$$J_2' = \sqrt{{J_{pk}}'^2 - 4} \ . \tag{3.22}$$

With the added step of transitioning between normalizations using (3.15),

$$\delta = n_t\sqrt{\frac{C_s}{C_p}}\sin^{-1}\left(\sqrt{\frac{C_s}{C_p}}\frac{2n_t}{J_{pk}}\right) \ , \tag{3.23}$$

and the starting current,

$$J_2 = \sqrt{{J_{pk}}^2 - 4{n_t}^2\frac{C_s}{C_p}} \ . \tag{3.24}$$

Subinterval IV: In the final subinterval, state plane analysis is again unnecessary due to its linear nature. Additionally, because the inductor current is constant at I_{pk} during the interval, only a single equation is obtained, which notes that the sum of the four subinterval durations should be equal to the half-period

$$t_1 + t_2 + t_3 + t_4 = \frac{T_s}{2} \ . \tag{3.25}$$

Defining the normalized duration of subinterval IV as $\zeta = t_4/\omega_0$, the normalization of (3.25) yields

$$\zeta = \frac{\pi}{F} - \alpha - \beta - \delta \ . \tag{3.26}$$

Averaging Finally, the results from all intervals can be assembled to solve for the averaged converter output current over a single half period

$$I_{out} = \frac{2}{T_s} \int_0^{\frac{T_s}{2}} i_{out}(t)dt \ . \tag{3.27}$$

During subinterval III, the output current is zero due to all current from the tank flowing through device output capacitances. The integral of (3.27) can then be broken up into components from the inductor current in each subinterval

$$I_{out} = \frac{2}{n_t T_s} \left[\int_0^{t_1} -i_l(t)dt + \int_{t_1}^{t_2} -i_l(t)dt + \int_{t_3}^{\frac{T_s}{2}} i_l(t)dt \right] \ . \tag{3.28}$$

The second and third integrals may be simply calculated by taking the area under the curve during the linear segments of subintervals II and IV. The remaining term from subinterval I requires integrating the sinusoidal segment present during the primary ZVS transition. However, in this subinterval, all inductor current i_l flows through the equivalent primary side capacitance C_p carrying the voltage across it from $-V_g$ to V_g. Thus, the integral of inductor current during the course of subinterval I is equal to the charge required to complete this transition,

$$\int_0^{t_1} -i_l(t)dt = 2V_g C_p \ . \tag{3.29}$$

Replacing all three subinterval integrals, the average output current is

$$I_{out} = \frac{2}{n_t T_s} \left[2V_g C_p + \frac{I_1 - I_2}{2} t_2 + I_{pk} t_4 \right] \ . \tag{3.30}$$

Normalizing and substituting (3.20) and (3.26) into (3.30),

$$J_{out} = \frac{F}{n_t \pi} \left[2 + \frac{1}{4} \left({J_1}^2 - {J_2}^2 \right) + J_{pk} \left(\frac{\pi}{F} - \alpha - \beta - \delta \right) \right] \ , \tag{3.31}$$

is obtained. Altogether, equations (3.31), (3.13), (3.18), (3.24), and (3.23) constitute a complete solution of converter steady-state behavior. Because the trigonometric terms present in the equations for α and δ in (3.13) and (3.23) cause the equation to be nonalgebraic, a single, closed-form equation for converter output current is not available.

A useful method for the examination of converter behavior is the consideration in the normalized domain of the relationship between the reflected output current, $J = n_t J_{out}$ and peak inductor current J_{pk}. This "output plane" is plotted for varying values of the normalized switching frequency $F = f_s/f_0$, in Fig. 3.11, where the resultant plot is independent of all details of converter implementation or operating point. Note that, as derived previously, ZVS cannot be obtained if $J_{pk} < 2$ and therefore the solution presented is not valid in this region. The normalized output plane

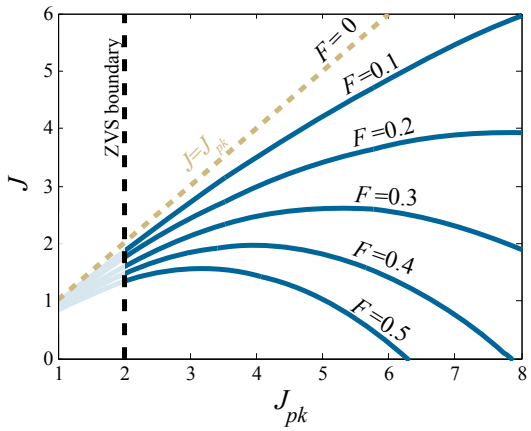


Figure 3.11: Normalized output plane of the DAB converter, for varying values of F.

reiterates many of the key design points argued previously for the DAB converter. To interpret the output plane, it is useful to substitute the value of f_0 into F to obtain

$$F = \frac{f_s \sqrt{L_l C_p}}{2\pi} \,, \tag{3.32}$$

which leads to the following conclusions from examination of the output plane

- Because J corresponds to the output power level and J_{pk} corresponds to the peak current stresses in the converter, a large discrepancy between J and J_{pk} corresponds to large device stresses and poor switch utilization.
- If $F = 0$ the converter approaches $J = J_{pk}$ and conduction losses are minimized.
- $F \approx 0$ can be obtained by making the switching frequency very low, or by allowing resonant elements L_l and C_p to approach zero. In any case, this results in resonant transitions which

occupy a negligible percent of the switching period.

- Large values of F have limited output power ranges due to the majority of the switching period spent in subintervals I-III when L_l and C_p are large.
- For an output current value given by J, increasing the value of F results in higher peak (and therefore RMS) currents.
- The minimum current stresses for a given output current are obtained when F is selected such that the converter operates on the ZVS boundary, $J_{pk} = 2$.

It is interesting to note that, as argued from the analysis prior to inclusion of ZVS intervals, the lowest conduction losses at a given output power which can be achieved while still maintaining ZVS are obtained when L_l is selected to place the converter at the minimum ZVS power P_{min}, as in (2.43).

This method for selecting L_l for high efficiency will be used in the ensuing section, which completes the power stage design by selecting primary and secondary transistor devices in order to obtain the highest efficiency, using the results of state plane analysis.

3.4 Converter Power Stage Design

For the power stage design, it will continue to be assumed that the DAB architecture, the phase shift modulation scheme, and the converter switching frequency are given, but the value of tank inductance and the device implementation are available as parameters for optimization of converter efficiency. At the moment, only a single operating power P_{out} is considered.

3.4.1 Selection of Tank Inductance

The selection of tank inductance follows from the analysis of the previous section. Namely, when considering only a single output power P_{out}, L_l should be selected as the minimum possible inductance for which primary ZVS can be maintained. This results in the minimum obtainable

converter RMS currents without forcing hard switching of any devices in the converter. By setting $P_{out} = P_{min}$, the converter operates with $J_{pk} = 2$ at the proposed operating point and the peak inductor current is *just* large enough to obtain primary ZVS. It is therefore true that $\alpha = \pi/2$ and the primary ZVS transition occupies exactly one-quarter of a resonant period of L_l and C_p. With this in hand, (3.31) and its constituents can be solved for the value of tank inductance which satisfies this design. Again, a closed-form solution is not available, but the resultant numerical solution is computationally simple.

The value of this inductance is mathematically dependent upon the values of C_p and C_s, and therefore one device selection. However, knowing that the inductance will be selected in this manner allows the solution of converter waveforms for any given set of devices, each with an inductance specific to converter optimization with their demonstrated capacitances. From this, a device loss model is used to select switch implementations in the following section.

3.4.2 Device Selection

The analytical converter solution developed from state plane analysis is generally applicable to the DAB under phase shift modulation independent of implementation details. When selecting devices, however, it is most useful to narrow the analysis scope to the application of interest for two primary reasons. First, this allows the design to address the unique requirements on device selection which are specific to the high-frequency, high conversion ratio converter, but would not be apparent in generalized analysis. Second, this allows the results to be interpreted numerically, which is preferable to further analytical manipulation due to the transcendental properties of the state plane solution.

For this purpose, device selection will be carried out with respect to the DAB converter defined by the following characteristics

- $P_{out} = 120$ W
- $V_{out} = 12$ V
- $f_s = 1$ MHz
- $V_g = 150$ V
- $n_t = 0.08$

Additionally, a representative sampling of available devices for both the primary and secondary full bridges will be considered. These devices, as well as values for parasitic parameters derived from datasheet specifications, are listed in Table 3.3 for high voltage and Table 3.4 for low voltage devices. The device sampling includes all GaN devices which were available at the time of this study, as well as a representative sampling of silicon devices which includes devices which span the same range of r_{on} as the GaN devices.

Table 3.3: Sample 200 V Devices

Part Number	Type	$r_{on,p}$ [mΩ]†	C_p [pF]‡	$Q_{g,p}$ [nC]†	$V_{DS,max}$ [V]
EPC1012	GaN	70	87	1.9	200
EPC1010	GaN	18	353	7.5	200
FDMS2672	Si	64	177	30	200
IPD320	Si	27	379	12	200
IRFS4020	Si	85	140	18	200
FDMC2610	Si	188	73	6	200

† taken at $V_{gs} = 5$V for GaN and $V_{gs} = 10$V for Si devices

‡ time-equivalent to nonlinear output capacitance, as developed in Section 4.1

All devices in the converter will obtain ZVS at the operating power of interest; therefore, only device conduction losses and gate drive will be present. Because only power stage efficiency is of primary concern, the gate drive losses which are supplied from auxiliary supplies are considered less important. The specious approach to device optimization would therefore attempt to select the devices with the minimum value of r_{on} for all eight switches in order to maximize power stage efficiency. However, this approach ignores the inherent dependence of the converter RMS currents on the values of C_p and C_s, which inform the length of dead time intervals and the magnitude of the selected tank inductance L_l. Thus, even without switching losses, device output capacitances continue to influence converter losses through the mechanism of conduction losses.

To view this effect explicitly, the normalized RMS currents present at various points in the converter can be solved in a similar manner to that used to solve for J_{out}. Although an individual

Table 3.4: Sample 20-40 V Devices

Part Number	Type	$r_{on,s}$ [mΩ]†	C_s [pF]‡	$Q_{g,s}$ [nC]†	$V_{DS,max}$ [V]
EPC1014	GaN	12	241	3.0	40
EPC1015	GaN	3.2	1000	12	40
CSD16325	Si	1.7	3200	20	25
STD60N3	Si	8.8	713	8.8	35
CSD16411	Si	11	486	3.1	25
IRF6713	Si	3.5	800	21	25

† taken at $V_{gs} = 5$V for GaN and Si devices

‡ time-equivalent to nonlinear output capacitance, as developed in Section 4.1

device conducts only during one half-period, the input and output current are always conducted by two series devices on the primary and secondary, respectively. Therefore for the converter loss analysis, the individual device RMS currents are not needed if the input and output RMS currents are solved. The normalized output, tank, and input current are given by

$$J_{out,rms}{}^2 = \frac{F}{n_t{}^2\pi}\left[\frac{\alpha}{2}J_{pk}{}^2\left(1+\frac{1}{\alpha}\sin\alpha\cos\alpha\right)+\frac{\beta}{3}\left(J_1{}^2-J_1J_2+J_2{}^2\right)+J_{pk}{}^2\left(\frac{\pi}{F}-\alpha-\beta-\delta\right)\right], \tag{3.33a}$$

$$J_{g,rms}{}^2 = \frac{F}{\pi}\left[\frac{\delta}{2}J_{pk}{}^2\left(1+\frac{1}{\delta}\sin\delta\cos\delta\right)+\frac{\beta}{3}\left(J_1{}^2-J_1J_2+J_2{}^2\right)+J_{pk}{}^2\left(\frac{\pi}{F}-\alpha-\beta-\delta\right)\right], \tag{3.33b}$$

$$J_{l,rms}{}^2 = \frac{F}{\pi}\left[\frac{\delta}{2}J_{pk}{}^2\left(1+\frac{1}{\delta}\sin\delta\cos\delta\right)+\frac{\alpha}{2}J_{pk}{}^2\left(1+\frac{1}{\alpha}\sin\alpha\cos\alpha\right)+\frac{\beta}{3}\left(J_1{}^2-J_1J_2+J_2{}^2\right)+J_{pk}{}^2\left(\frac{\pi}{F}-\alpha-\beta-\delta\right)\right]. \tag{3.33c}$$

Note that these three equations differ only in their inclusion of terms due to the dead time intervals, which have normalized duration α for the primary transition and δ for the secondary. The input current is zero during the primary bridge transition, and therefore the RMS current at the input does not contain the term derived from subinterval I. Similarly, the output current does not include the subinterval III term, but the tank current RMS contains components from all subintervals due to

its continuous conduction. Then, the dependence of each of these RMS currents can be considered for a range of values of C_p and C_s which spans all sample devices. Given the application-specific converter parameters, Fig. 3.12 shows how inductance and RMS currents vary with the value of C_p, assuming that r_{on} has little effect on converter waveforms, though it will be significant in loss calculations. The plot is constructed with a single value for $C_s = 2$ nF. It can be seen that all RMS currents and the tank inductance required to obtain ZVS at $P_{min} = 120$ W are strongly dependent on the value of C_p. The same parameters are plotted again in Fig. 3.13, where C_s is instead varied with a constant $C_p = 100$ pF.

By contrast, the RMS currents and tank inductance are very weakly dependent on C_s, even for a range of values triple that of the sample devices considered. This difference is due to the high step-down nature of the converter. The high current, low voltage secondary allows for very rapid ZVS transitions due to the small voltage which must be traversed on the device output capacitances, and the large current available to charge them. On the primary, the conditions are the inverse: There is a large voltage swing which must be made with relatively low inductor current. This results in a primary deadtime t_1 which is significant in duration, but a secondary deadtime t_3 which is not.

An additional detail which should be discerned from Fig. 3.12 and Fig. 3.13 concerns the magnitudes of each RMS current. As noted earlier, the three RMS currents differ only in their inclusion of the two dead time intervals, $t_1 \mapsto \alpha$ and $t_3 \mapsto \delta$. Because the secondary deadtime is insignificant due to the large current and low voltage, there is very little difference between $I_{l,rms}$ and $n_t I_{out,rms}$, which differ only by the RMS contribution of t_3. However, because the primary deadtime is significant, the value of $I_{g,rms}$ is significantly less than either of these currents, with the difference becoming smaller for smaller values of C_p.

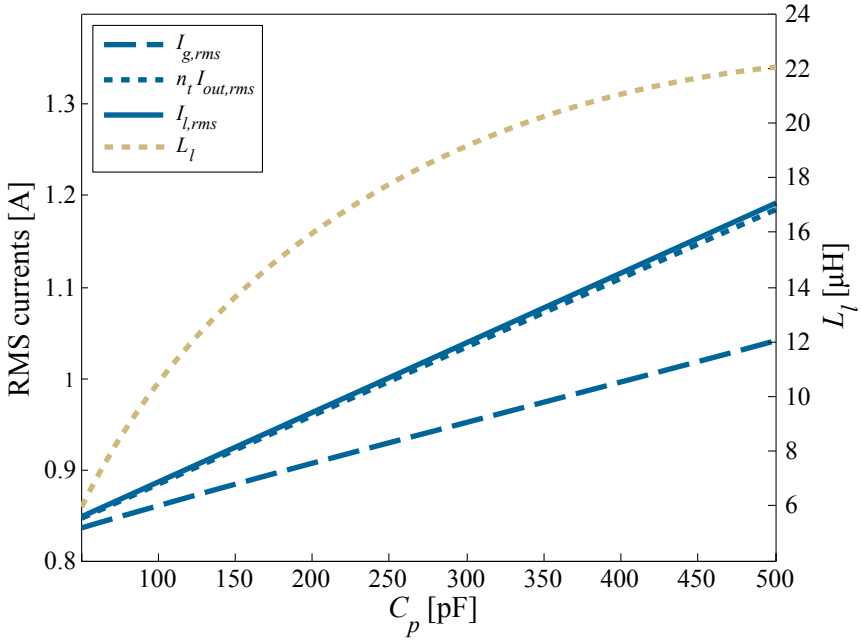


Figure 3.12: Dependence of converter RMS currents and tank inductance on C_p, evaluated with $C_s = 2$ nF and under the application-specified converter design.

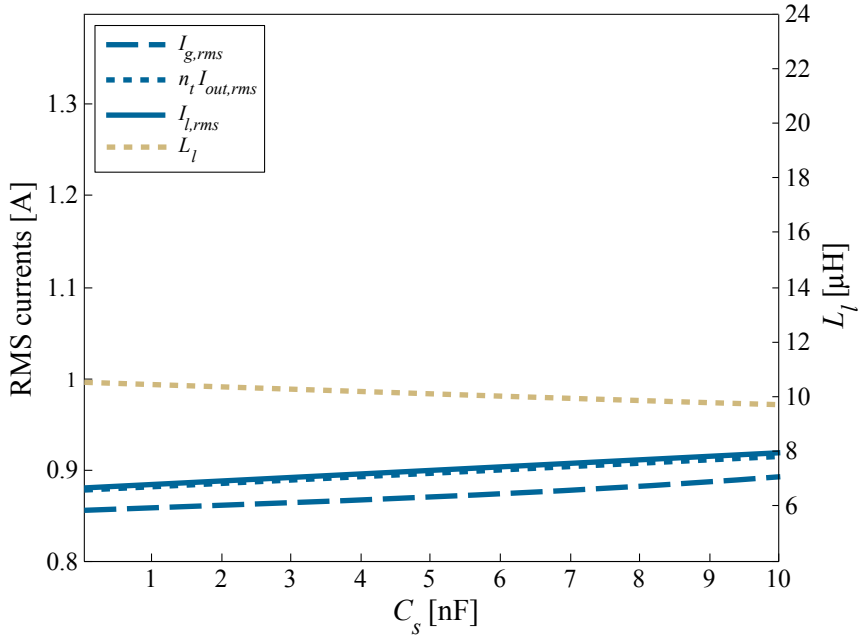


Figure 3.13: Dependence of converter RMS currents and tank inductance on C_s, evaluated with $C_p = 100$ pF and under the application-specified converter design.

The conclusions which may be drawn from this analysis are as follows

(1) Low C_p is required for low RMS currents

(2) Primary r_{on} is of lesser importance due to low currents on the primary

(3) C_s has little effect on RMS currents

(4) Low Secondary r_{on} is necessary due to large currents on the secondary

For power stage efficiency maximization, devices should be selected with preference given to low C_p on the primary and low r_{on} on the secondary. This is because C_p has significant influence on RMS currents, whereas secondary r_{on} has significant influence on the losses due to those currents, with C_s and primary r_{on} having substantially smaller contributions.

Table 3.5 shows the resultant converter parameters and RMS currents from the various primary devices of Table 3.3, again assuming a nominal influence of C_s. As expected, the lowest C_p devices yield the lowest resonant deadtimes t_1, lowest inductance L_l and normalized switching frequency F, and therefore the smallest RMS and peak currents throughout the converter.

Table 3.5: Comparison of Primary Side Devices

Part Number	Type	L_l [μH]†	t_1 [ns]	F	I_{pk} [A]	$I_{g,rms}$ [A]	$I_{o,rms}$ [A]
EPC1012	GaN	9.34	43.9	0.18	0.92	0.86	11.0
EPC1010	GaN	20.5	131	0.53	1.25	0.98	13.5
FDMS2672	Si	15.1	79.5	0.32	1.03	0.90	11.8
IPD320	Si	20.9	137	0.56	1.28	0.99	13.7
IRFS4020	Si	13.1	65.9	0.27	0.98	0.88	11.5
FDMC2610	Si	8.14	37.5	0.15	0.90	0.85	10.8

3.4.3 Switch Loss analysis

With the waveforms of the converter determined, it is possible to solve for the predicted losses in the converter for a given combination of devices. Though significant losses are expected

to be incurred due from magnetics, these losses are largely independent of device selection. It is therefore pertinent to consider transistor losses in isolation. Expected losses which are subject to optimization via device selection are the primary and secondary device conduction losses

$$P_{cond,p} = 2r_{on,p}{I_{g,rms}}^2 \ , \tag{3.34a}$$

$$P_{cond,p} = 2r_{on,s}{I_{out,rms}}^2 \ , \tag{3.34b}$$

as well as gate drive switching losses for both sets of devices,

$$P_{g,p} = 4\left(Q_{g,p}V_{gs}\right)f_s \ , \tag{3.35a}$$

$$P_{g,s} = 4\left(Q_{g,s}V_{gs}\right)f_s \ . \tag{3.35b}$$

Additionally of potential significance are losses due to parasitic inductance of the devices and their physical layout [58,84]. However, these losses depend largely on PCB design and device packaging, and are therefore not considered an intrinsic limitation of a transistor process. Discussion of these losses is therefore delayed to Section 3.5.2

For a sample of primary and secondary combinations, the conduction and gate drive losses are estimated analytically with the results given in Fig. 3.14. It can immediately be seen that the optimal device combination consists of one GaN and one Silicon device, with EPC1012 on the primary and CSD16325 on the secondary. Note that the secondary device is indeed the lowest r_{on} device, whereas the primary is actually the second lowest C_p device. This discrepancy is due to the barrier between GaN and Si. Though the EPC1012 which results in the lowest losses has slightly larger C_p than the FDMC2610 silicon device, its $C_{ds}r_{on}$ figure of merit is half that of the FDMC2610, and its $Q_g r_{on}$ is nearly tenfold better. Thus, as could be predicted, there is some limit under which the simple design methodology of minimizing C_p and $r_{on,s}$ is applicable. To further demonstrate the link between device parasitics and predicted device losses, the sample device combinations are shown again in Fig. 3.15, along with the parasitics of primary interest. Additionally, the gate drive losses have been de-emphasized to thereby emphasize only the power stage losses which are under consideration.

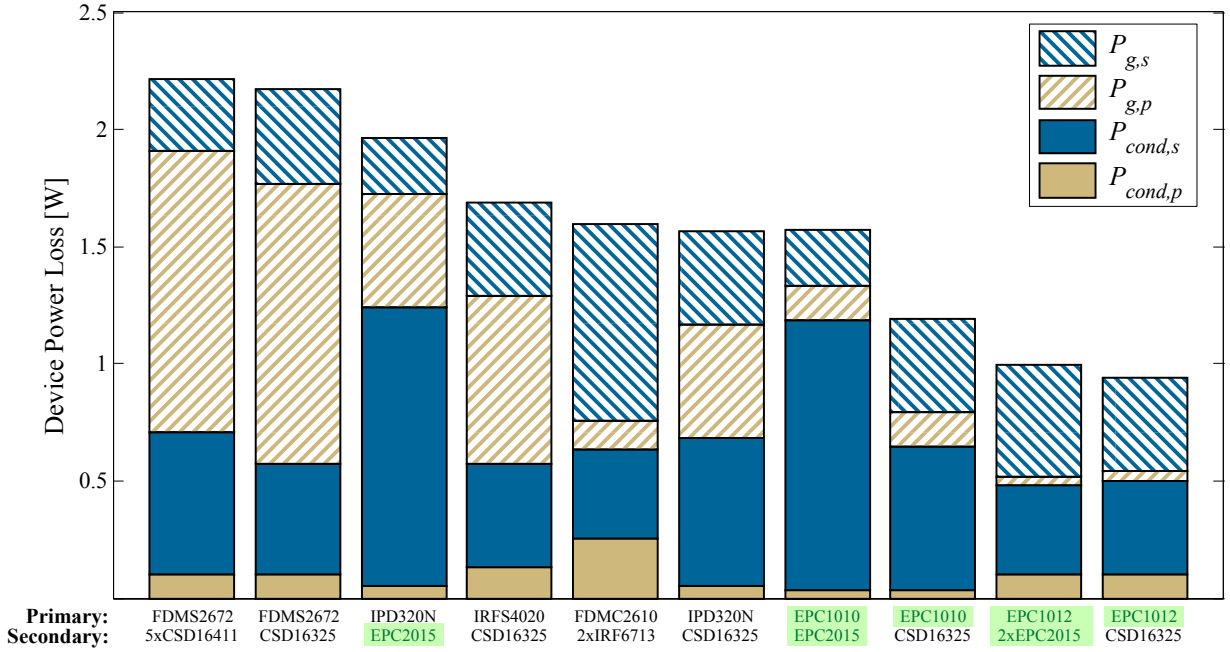


Figure 3.14: Comparison of predicted gate drive and conduction losses on primary and secondary devices for a variety of device combinations

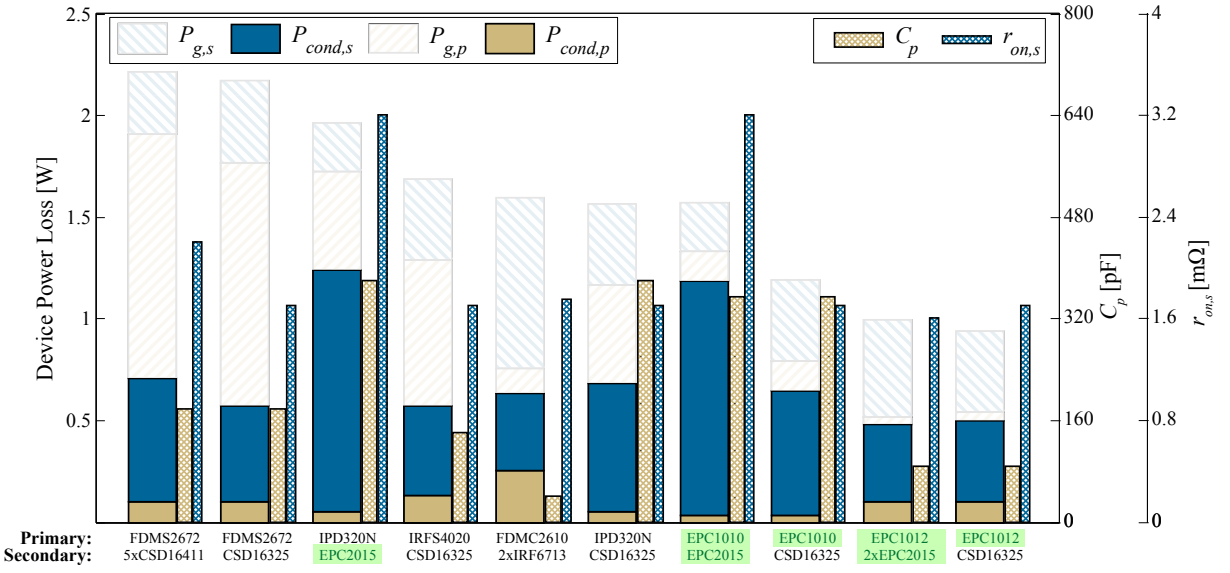


Figure 3.15: Comparison of predicted gate drive and conduction losses on primary and secondary devices for a variety of device combinations, with primary capacitance and secondary on-resistance shown for each combination. Gate drive losses have been de-emphasized.

As is done in some of the combinations in Fig. 3.14 and Fig. 3.15, it is possible to alter the tradeoff between r_{on} and C_{ds} for any device by paralleling discrete modules. However, if further ability to select device size at the time of fabrication is available, the performance of the circuit is only limited by the relevant FOMs for the process. It is then possible to consider optimizing device size in order to reduce total power stage conduction losses. For example on the primary, a larger device will have lower $r_{on,p}$ and therefore result in a decrease in $P_{cond,p}$, but will also have a larger C_p which increases secondary RMS currents and $P_{cond,s}$.

This optimization is carried out in Fig. 3.16 for a primary device with an assumed FOM $C_{ds}r_{on} = 6000$ pF $\cdot$ mΩ, which corresponds closely to that demonstrated by the high voltage GaN devices of Table 3.3. The secondary devices are assumed to be CSD16325 silicon MOSFETs. The optimal device size for this application and process, from Fig. 3.16, results in a device with nearly 60 mΩ on resistance and a corresponding output capacitance of 100 pF.

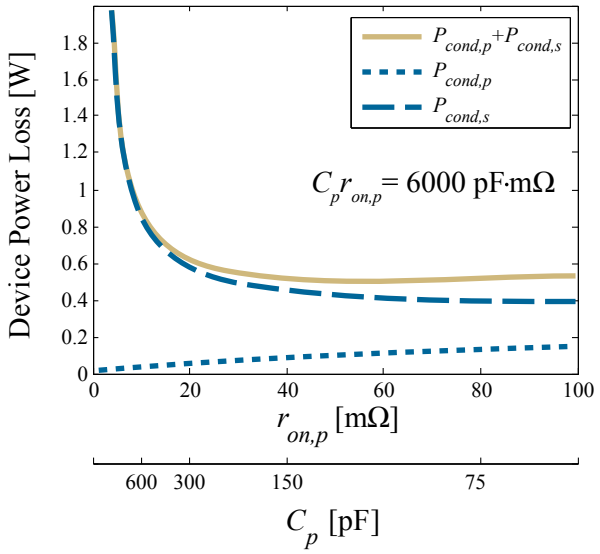


Figure 3.16: Device conduction losses as they vary with primary switch size for a set FOM close to that exhibited by the tested high voltage GaN devices.

When this optimization is run on the secondary devices, again with FOM $C_{ds}r_{on} = 3200$ pF $\cdot$ mΩ which corresponds with the low voltage GaN devices, the resultant curves of Fig. 3.17 reiterate

the weak system sensitivity to C_s and the significant dependence of total conduction losses on $r_{on,s}$.

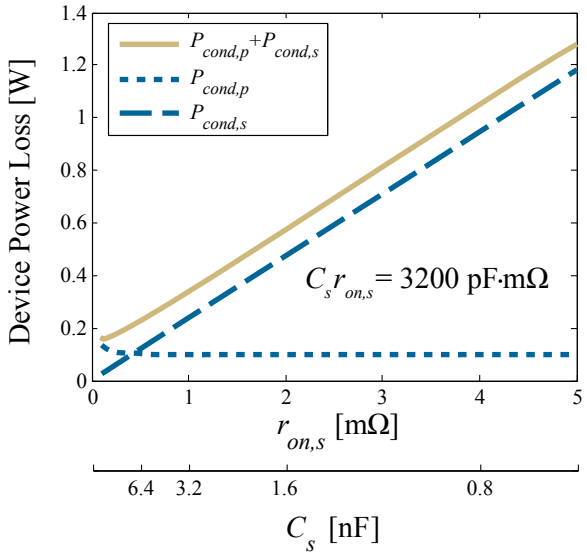


Figure 3.17: Device conduction losses as they vary with secondary switch size for a set FOM close to that exhibited by the tested low voltage GaN devices. Primary devices are represented by the parasitics of the EPC1012 device for the generation of this figure.

When taken to the extreme, reduction of $r_{on,s}$ and corresponding increase in C_s will begin to have significant effect on the RMS currents in the converter. From Fig. 3.17, this effect only becomes significant for C_s above about 12.8 nF, which is four times that exhibited by any of the sample devices considered. The secondary dead time will be much less than the primary dead time as long as

$$C_s \ll \frac{C_p}{{n_t}^2} \ , \tag{3.36}$$

which for a primary device modeled as EPC1012 results in $C_s \ll 13.6\ nF$. Furthermore, even when the secondary dead time becomes significant at high values of C_s, losses are only nominally increased. This is due to the fact that during the secondary deadtime, by definition, all secondary devices are turned off. Therefore, increasing this deadtime results in RMS currents in the secondary devices which are increased by a smaller margin than those in the low-current primary.

The plots generated in Fig. 3.16 and Fig. 3.17 vary with the chosen device FOMs and with

which devices implement the opposing full bridges. Larger $C_{ds} \cdot r_{on}$ FOMs result in optimums occuring at larger r_{on} values in both the primary and secondary. However, general shape and appearance of plots, as well as the design conclusions, remain valid for any device combination which is well suited to the application, and for which (3.36) remains true.

In addition to conclusions drawn about device selection, the very minor effect that even a wide variation in C_s has on converter waveforms and RMS currents implies that the secondary deadtime interval is not a significant factor in solving converter steady-state operation. This is in contrast to the primary dead time which does significantly affect the operational waveforms of the converter. Therefore, in all continued discussion of converter operation, secondary deadtime will be assumed negligible ($\delta \approx 0$) when considering any other characteristics of the converter, with the deadtime only explicitly solved afterwards when needed for loss analysis or gate drive timing implementation.

3.5 Optimal Switching Time Analysis

With respect to the constraint in (3.36), it can be seen that the converter solution during secondary deadtime intervals in (3.24) and (3.23) indeed breaks down if $C_s > {n_t}^2 C_p$. Although ZVS of secondary devices is possible regardless of inductor energy for the given mode of operation, if C_s actually exceeds the reflected primary capacitance, the resonance required to achieve ZVS of secondary devices will result in a peak current greater than the designed I_{pk}. This means that the converter will be forced to either operate at a larger power level, in a different operating mode, or actively hard switch secondary devices prior to the completion of the ZVS interval despite the resonant circuit having the capacity to achieve ZVS.

Despite the initial aversion any power electronics engineer will have to purposefully hard switching devices, this concept has some appeal. Particularly on the primary, where the duration of the resonant intervals has been shown to have significant effect on conduction loss, it is worth considering whether the losses accrued by full or partial hard switching would not be offset by reduced conduction losses which could be achieved if these resonant intervals were reduced or

eliminated entirely.

The present analysis will continue to consider operation at a single output power, with a converter power stage consisting of inductance value and switching devices which are selected via the design methods of the previous sections. This design process yields a converter which is *capable* of operating at the designed power with full ZVS of all devices and minimal conduction losses in the devices. However, the converter will only actually *achieve* ZVS of all devices if the gate drive waveforms of all devices are implemented precisely. Fig. 3.18 demonstrates the effects of small errors in gate drive timing on Q_1 during the primary dead time interval. In Fig. 3.18(b), the gate-to-source for Q_1 is implemented ideally, resulting in a device dead time equal to $t_1 = \alpha/\omega_0$, as may be solved for by state plane analysis. Under this condition, Q_1 is turned on immediately as $v_a(t)$ reaches V_g thus resulting in soft switching with zero drain-to-source voltage on Q_1 at turn-on.

In Fig. 3.18(c), the gate-to-source voltage on Q_1 goes high prior to the completion of the ideal t_1 dead time duration. Because the resonant transition has not completed, the voltage $v_a(t)$ has not reached V_g, and a small amount of voltage $V_g - V_1$ remains across the parasitic output capacitance of Q_1 when it is turned on. As Q_1 turns on at non-zero voltage, an energy loss is incurred which is given by the sum of the energy in the output capacitance of Q_1 and the conduction loss incurred by forcibly charging the output capacitance of Q_2 from V_1 to V_g in a nonresonant manner. For identical, linear output capacitors of both Q_1 and Q_2, the loss per transition due to this active hard switching is given by

$$P_{actHS} = C_p \left({V_g}^2 - V_g V_1 \right) f_s \ , \tag{3.37}$$

In Fig. 3.18(d), the gate drive turns on later than ideal. Because the converter is designed to operate with $J_{pk} = 2$, i.e. on the boundary of achievable ZVS, the inductor current hits zero directly as the voltage $v_a(t)$ reaches V_g. Any extension of the resonant period beyond the ideal value therefore results in the inductor current reversing polarity and reducing $v_a(t)$ further away from V_g. If the voltage $v_a(t)$ again takes value V_1 at turn on, the power loss is identical to that given in (3.37).

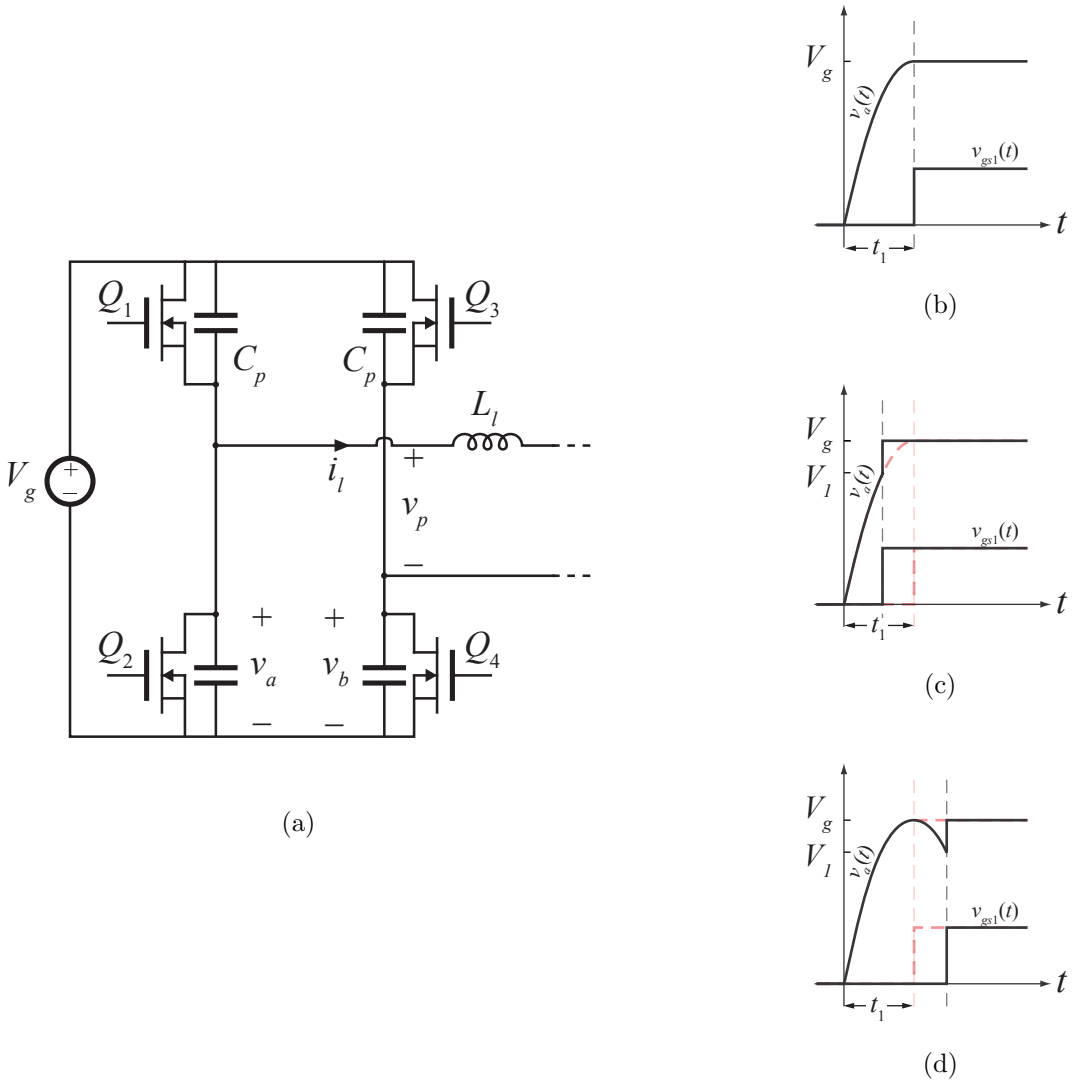


Figure 3.18: Waveforms of the resonant transition of the primary full bridge (a) in the DAB converter with ideal gate drive timing (b), decreased dead time duration (c) and increased dead time duration (d)

In order to avoid the partial hard switching of the primary, precise gate drive waveforms must be implemented with high current gate drive circuitry and a high resolution modulator. Appendix B details one method of implementing high resolution phase shift modulation circuitry in low cost FPGAs without dedicating significant amounts of time to routing, layout, and other implementation details. It is clear that the additional dead time of Fig. 3.18(d) will result in both switching losses and some increase in RMS currents to compensate for the extended dead time interval, and therefore should be avoided at all times. However, it would appear that the hard switching of Fig. 3.18(c) results in some tradeoff, as the shortened deadtime will decrease converter RMS currents and therefore decrease conduction losses by some margin. In order to justify the design decisions made previously which emphasize the maintenance of ZVS as a primary design goal, the analysis of this tradeoff is presented here. The result, as might be expected, is that any hard switching of voltage other than a token magnitude will be a detriment to converter efficiency in the proposed high-voltage, high-frequency converter.

3.5.1 State Plane Analysis with Active Hard Switching

For the converter as designed, the primary state plane is shown in Fig. 3.19 for the converter operating with active hard switching. The normalized voltage M_{HS} corresponds to the voltage present at v_p at the instant when the primary full bridge is commutated. For $M_{HS} < 1$, a voltage equal to $(1 - M_{HS})V_g/2$ is present on each primary device when turned on, and the total losses associated with the hard switching transition are given as per (3.37)

$$P_{actHS} = 4 \cdot \frac{C_p}{2} \left(1 - M_{HS}\right) {V_g}^2 f_s \ . \tag{3.38}$$

Beginning from the state plane solution developed in Section 3.3.2.2, only the subinterval I parameters have changed, and they are now given as

$$\alpha = \sin^{-1} \frac{1 + M_{HS}}{J_{pk}} \ , \tag{3.39}$$

$$J_1 = \sqrt{J_{pk}^2 - \left(M_{HS} + 1\right)^2} \ . \tag{3.40}$$

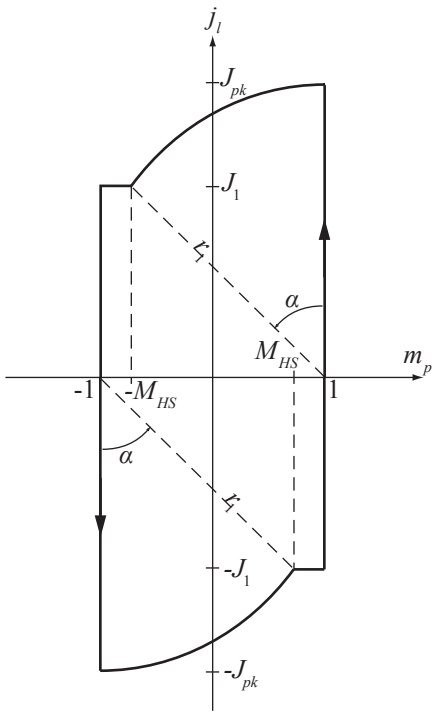
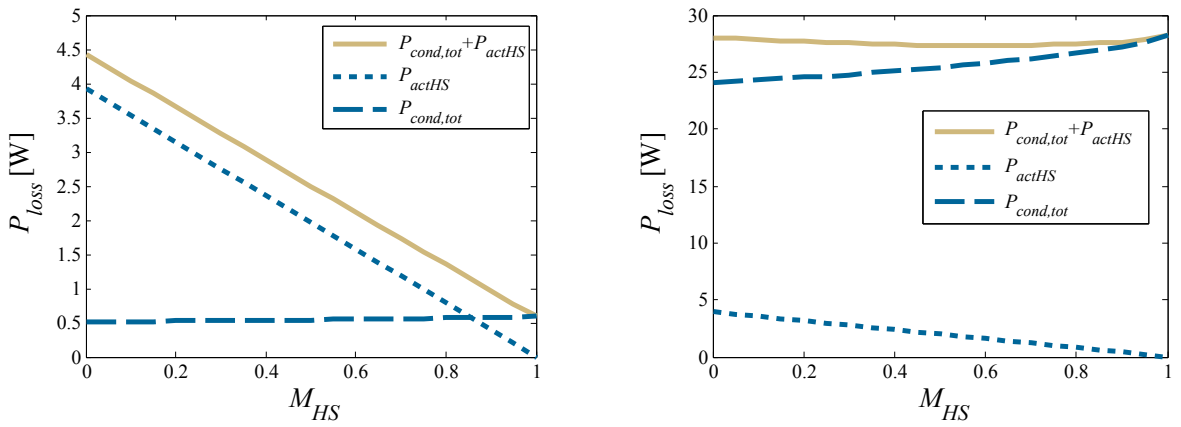


Figure 3.19: Primary state plane of actively hard switched DAB converter.

and the converter output current is

$$J_{out} = \frac{F}{n_t \pi}\left[(1 + M_{HS}) + \frac{1}{4}\left({J_1}^2 - {J_2}^2\right) + J_{pk}\left(\frac{\pi}{F} - \alpha - \beta - \delta\right)\right] \ , \tag{3.41}$$

and the equations for RMS currents remain unaltered. With this solution, it is possible to solve for the optimal amount of hard switch M_{HS} such that the sum of switching losses in (3.37) and conduction losses in (3.34) is minimized. For e.g EPC1012 primary devices and CSD16325 secondary devices, at the proposed 120 W operating point, the power losses are plotted as a function of M_{HS} for $0 < M_{HS} < 1$ in Fig. 3.20(a). This range of M_{HS} spans full soft switching down to partial hard switching of a voltage equivalent to half of the worst-case hard-switching loss. In this case, no amount of hard switching produces enough reduction in RMS currents to justify the added switching losses. By comparison, if the secondary device is instead implemented with $r_{on,s} = 100$ mΩ (a very poor design), the plot of Fig. 3.20(b) is produced, which shows that under these conditions, nearly 60 V of hard switching results in optimal power loss.



(a) (b)

Figure 3.20: Power loss as a function of normalized hard-switched voltage M_{HS} for the nominal circuit configuration (a) and an example with $100\times$ $r_{on,s}$ (b).

Though the result of this analysis is uncompelling, the implications are important for the converter design. The realization that, for a well designed converter, switching losses trump con-

duction losses all the way to $M_H S = 1$ justifies the design procedure developed in this chapter for a single operating power, in which maintenance of ZVS is considered paramount and switching loss reduction is addressed in the first design steps through the selection of tank inductance.

3.5.2 Parasitic Inductance Losses

Despite the exhibition of zero voltage switching on all devices, switching losses in any practical power stage implementation of the DAB circuit are not completely eliminated. When switch gate drive timing signals are implemented ideally as in Fig. 3.18(b), all energy contained in the parasitic drain-to-source capacitance is transfered in a resonant manner prior to the switching instant, resulting in no loss of the energy contained in this parasitic when each switch turns on. However, each switch additionally exhibits some parasitic inductance, L_D as in Fig. 3.21(a), which is a lumped parameter in series with the MOSFET channel representing the energy stored in the current loop formed by the device channel, source and drain wire bonds, packaging, and PCB layout, and typically takes value in the range of a few nanohenries [85]. The significance of these parasitic inductances to circuit operation can be seen in the waveforms of e.g. the secondary side devices Q_5 and Q_6 during nominal operation with and without L_D included in device modeling. These waveforms are diagrammed in Fig. 3.21(b). Examining the subinterval VII, the MOSFET Q_5 shuts off with a current in $i_d \approx -I_{pk}/n_t$ flowing through L_D. During the subinterval, resonance occurs between the tank inductance and the parasitic drain-to-source capacitance of Q_5 to obtain ZVS, during which time the small inductances L_D appear in series with the tank inductance and nominally alter circuit operation. However, the nature of the interval causes ZVS to be achieved at the moment when peak current is flowing at i_d. When opposing devices Q_6 and Q_7 are turned on to allow current flow to the output, the energy remaining in L_D is left to flow through a current loop which consists of the parasitic elements of nonconducting devices. This current loop does not include the tank, confining the $L - C$ ringing that results to the secondary device currents. Under the assumption that small resistances present in this loop are sufficient to damp the resonance sufficiently, the amplitude of the ringing reduces to zero prior to the next commutation period.

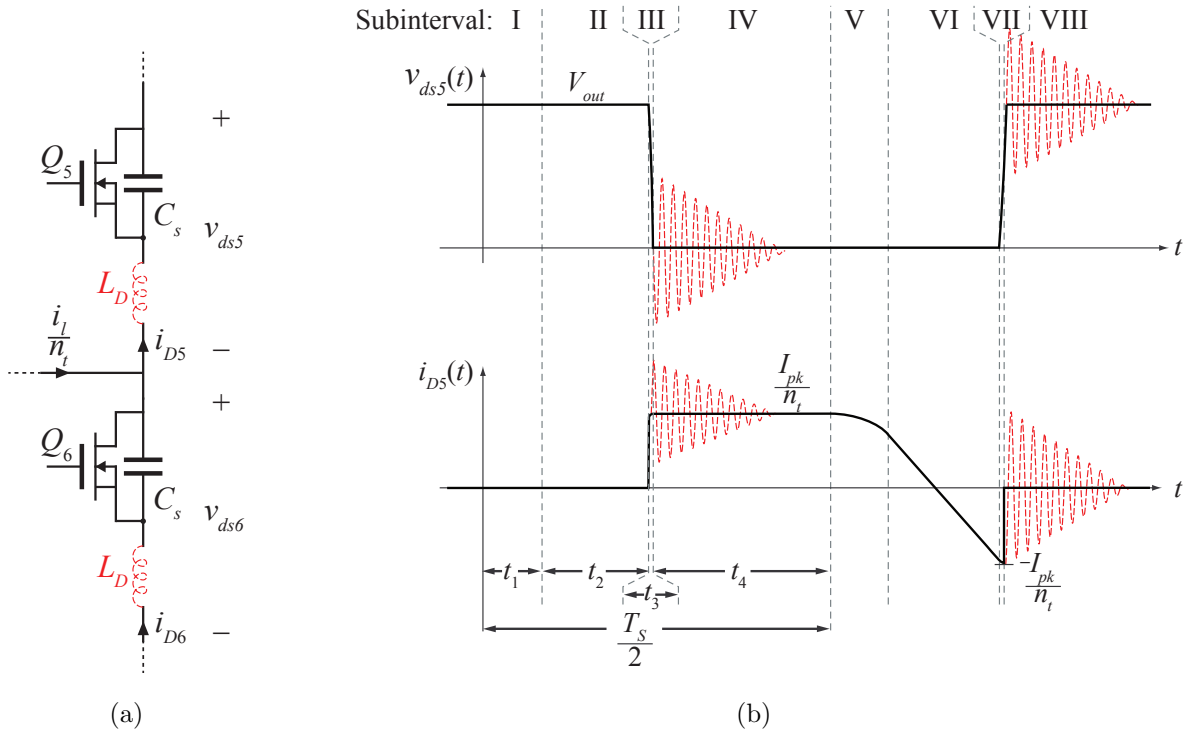


Figure 3.21: Location of lumped parasitic L_D on secondary side devices (a) and effect of circuit operation (b), where solid black plots indicate ideal behavior and dashed red give an example of observed waveforms with L_D present.

Assuming ZVS is still obtained on the initial turn off, the total energy present in the resonance is equal to the energy stored in L_D at the switching instant between subintervals VII and VIII, and all of this energy is lost to the damped resonance. Noting that DCX operation results in the inductor current reaching I_{pk}/n_t at the subinterval interface, the energy lost due to the damped resonance across Q_5 is given by

$$E_{sw,Q5,LD} = \frac{1}{2} L_D \frac{{I_{pk}}^2}{n_t} \ . \tag{3.42}$$

All four secondary-side devices exhibit this behavior once per switching period, resulting in a total power loss due to secondary-side parasitic inductances of

$$P_{sw,LD} = 2 L_D {I_{pk}}^2 f_s \ . \tag{3.43}$$

Equivalent loss mechanisms are not significant on the primary side for a number of reasons. First, because the parasitic inductances are determined largely by packaging, rather than device size, the value of the parasitic inductance on the primary is, in general, comparable to that on the secondary. The currents on the primary are scaled by the turns ratio, however, resulting in a nearly ${n_t}^2$ reduction in the peak energy stored by parasitic inductances on the primary relative to the high current secondary. Even more important, however, is the design of the converter that has been proposed in the previous sections, which selects the converter tank inductance L_l to place the converter on the boundary of ZVS; and additional side effect of this selection is that each primary device additionally has zero current at the end of the ZVS interval and therefore no energy remains in the parasitic drain inductance to cause additional loss.

Accurate analytical prediction of $P_{sw,LD}$ is notoriously difficult to obtain due to the obscurity of the inherent loss mechanisms. Often an empirical model is used to estimate the switching loss by measuring and integrating the device voltage and current v_{ds} and i_d at the designed operating point [58,84]. Though potentially accurate, this approach is a poor solution for informing converter design as it requires the converter to be constructed prior to completion of loss analysis.

Though it is simple to measure the voltage v_{ds} of any of the secondary-side devices, the insertion of any additional wire loops or resistive elements into the current path, as would be

required to measure i_d, results in significant additional parasitic elements which will often compare to or trump L_D itself and completely alter the dynamics which are to be measured. As the converter application moves further toward low power and high frequency, the resonant elements present on the secondary side reduce in magnitude and result in a resonant frequency which may be sufficiently high such that normal measurement devices will have poor resolution within a resonant period, making accurate power loss measurements difficult.

Additionally, it is not possible to experimentally measure the effective voltage across the capacitance C_s directly without also including the voltage across L_D. It is therefore difficult to confirm that full ZVS is obtained. In the event that C_s has not reached zero-voltage at the end of the dead time interval, the voltage remaining in C_s provides some additional energy to the resonant circuit with L_D, all of which is additionally lost in the damped ringing. This additional energy present in the resonance will also result an increased peak amplitude of the ringing waveforms v_{ds} and i_d. Experimental fine-tuning of secondary-side dead time is therefore more effectively accomplished by minimizing the amplitude of the measured voltage ringing, rather than attempting to time gate drive waveforms so that the measured rise of v_{gs} coincides with the measured zero-crossing of v_{ds}.

One potential alternate approach for developing an empirical loss model is to test device switching independently in a separate circuit which replicates voltage and current conditions at device turn off [86], but permits the measurement of power loss directly from a voltage source. However, any modeling technique based on measured losses is not well suited to informing device selection, in which it is useful to be able to compare a multitude of devices based on datasheet-reported parasitic elements without requiring the characterization of each.

The losses due to parasitic inductances can be mitigated through both design and control approaches. Reduction of the value of L_D through device selection focused on low package inductance and well-decoupled, optimal PCB layout will reduce the parasitic energy storage and therefore reduce the per-period energy loss. Additionally, alternate modulation schemes or converter operating modes can result in a decreased current in secondary-side switches at turn-off. These approaches

will be considered in further detail in Chapter 5 when operation is considered across a wide power range.

3.6 Magnetics Design

With the converter now designed and the proposed circuit parameters and device implementations known, the final remaining characteristic of steady state operation which must be considered is the implementation of magnetic devices. The transformer and tank inductance should be designed for optimal efficiency given the specified operating point, which assumes a known turns ratio n_t and tank inductance L_l. Though the specific implementation of magnetics will have minor effects on converter RMS currents, and the device implementation will nominally affect the voltage stresses on the magnetics, it is assumed that these effects remain relatively minor, permitting the proposed independent device selection and magnetic design.

3.6.1 Transformer Design

Following the magnetics theory review of Section 2.3.1.1, the optimization of transformer design is accomplished through the minimization of the core and copper losses exhibited by the component. However, the simplified models of core loss (Steinmetz) and copper loss (DC-only) must be refined in order to obtain accurate loss predictions at the 1 MHz switching frequency. Again, optimization is desired to be based only on manufacturer-reported data for the ferrite cores which may be used in the implementation so that the construction of candidate designs is not required for their evaluation.

With respect to core loss, the original Steinmetz equation presented in Section 2.3.1.2 has inherent limitation of being accurate only for sinusoidally-varying flux densities $B(t)$. Given the simplified definition of flux density in (2.29), it is clear that the flux densities incurred in the DAB converter will be definitively nonsinusoidal, and therefore the direct application of the Steinmetz equation for core loss prediction is not a valid approach. Instead, more recent techniques for empirical loss approximation in ferrite materials are reviewed, and the results applied for core loss

calculations.

3.6.1.1 Review of Core Loss Approximation Techniques

Stemming from the original Steinmetz [36] empirical modeling of core loss in magnetic materials for sinusoidal waveforms, a number of refined nonphysically-motivated models have been proposed to improve loss prediction for nonsinusoidal waveforms [37]. The modified Steinmetz equation (MSE) [39] alters the traditional Steinmetz equation of (2.33) as

$$P_{v,MSE} = K_V \left(\frac{2}{(\Delta B)^2 \pi^2} \int_0^{T_s} \frac{dB}{dt}^2 dt \right)^{\alpha - 1} \Delta B^{\beta} f_s \ , \tag{3.44}$$

which includes the magnetization rate dM/dt through its proportionality with dB/dt. This inclusion, though not analytically supported, is based on the physical motivation that core losses depend on domain wall movement. This inclusion resulted in increased accuracy under many test conditions compared to the traditional Steinmetz equation. Continuing on this path, the generalized Steinmetz equation (GSE) [40] attempted to include both the instantaneous value and rate of change of induced flux density in loss calculations, producing an equation of the form

$$P_{v,GSE} = k_1 \left| \frac{dB}{dt} \right|^{\alpha} |B(t)|^{\beta - \alpha} \ , \tag{3.45}$$

where k_1 is solved in order to ensure that the GSE matches the original Steinmetz equation under the condition of sinusoidally varying flux densities. The GSE was generally deemed suboptimal due to its dependence only on instantaneous flux density, rather than time-history of $B(t)$. This approach was therefore modified further in [41] and [42] to produce the improved generalized Steinmetz equation (iGSE) (also called the natural Steinmetz equation (NSE)), which again takes into account the total variation in flux density over a period, ΔB

$$P_{v,iGSE} = \frac{k_i \left(\Delta B \right)^{\beta - \alpha}}{T_s} \int_0^{T_s} \left| \frac{dB}{dt} \right|^{\alpha} dt \ , \tag{3.46}$$

where k_i is again set to obtain matching with the original Steinmetz equation under the condition of sinusoidal excitation. The comparison of the MSE, GSE, and iGSE to experimental data consisting of excitation which is sinusoidal plus a varying strength third harmonic is given in Fig. 3.22, which is

reproduced from [37]. Further refinements to the iGSE, including techniques for loop splitting [41] and the inclusion of relaxation effects [31] have since been proposed, but are deemed overly complex and unnecessary for the application at hand, considering the potential waveforms for $B(t)$ which may arise in the DAB converter.

Under the approximation that $\delta \approx 0$ and the tank inductance L_l is implemented entirely on the primary, the DAB transformer voltage stresses are defined by the secondary bridge switching, and result in square-wave AC voltage stresses. Under this assumption, the iGSE/NSE equations of [42] simplify to:

$$P_v = 4^{\alpha} k_N f_s^{\alpha} \left(\Delta B\right)^{\beta} \ , \tag{3.47a}$$

$$k_N = \frac{K_v}{(2\pi)^{\alpha-1} \int_0^{2\pi} \left|\cos\theta\right|^{\alpha} d\theta} \ , \tag{3.47b}$$

which are the most simplified form of the iGSE/NSE equations applicable to 50% duty cycle, square-wave voltage excitation and therefore may be used for transformer core loss prediction.

3.6.1.2 Review of Copper Loss Approximation Techniques

In addition to DC copper resistivity, the power loss incurred in the wires which constitute the transformer primary and secondary windings will be increased due to skin and proximity effects. Both of these phenomena are frequency-dependent. Because all magnetics in the DAB converter conduct purely AC current waveforms, both windings are exposed to currents with significant frequency components at and above the 1 MHZ switching frequency.

The nature of skin and proximity effects are examined by way of example in Fig. 3.23 and Fig. 3.24, respectively, both of which are generated using the finite element analysis tool FEMM [87]. In Fig. 3.23, a single, solid-core copper 22 AWG conductor in air carries 10 A peak sinusoidal current with frequency which varies between $f_s = 5$ kHz and 5 MHz. DC copper resistivity is assumed to be ρ =1.68 $\mu\Omega$/cm. The current density in a cross section of the conductor is shown via a contour plot in Fig. 3.23(a) and as a function of distance orthogonal to the wire surface in Fig. 3.23(b). The results show that the current density in the conductor is increasingly crowded toward its surface

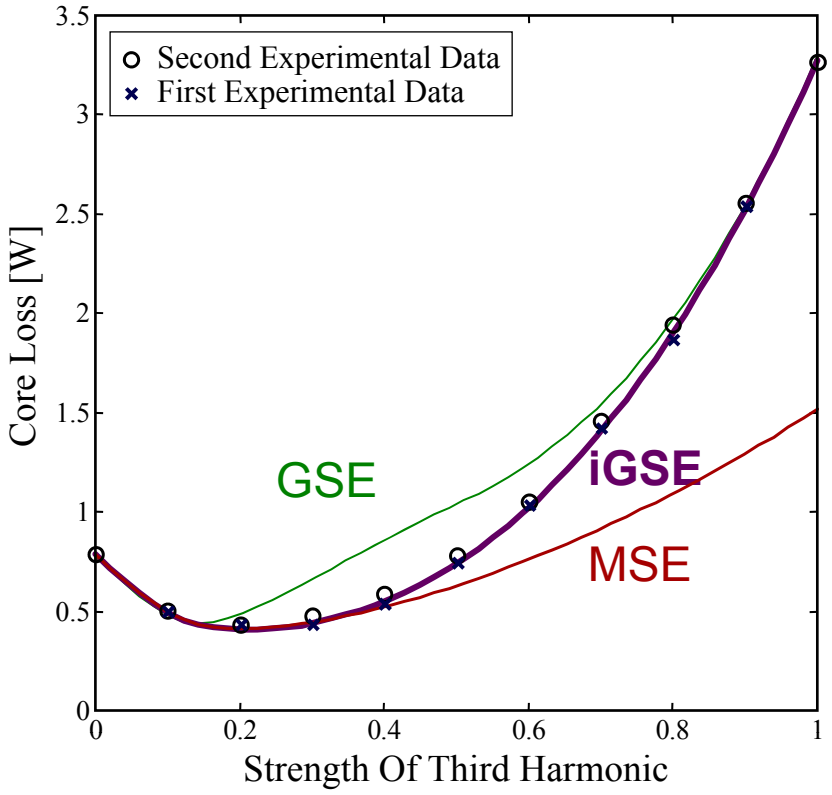
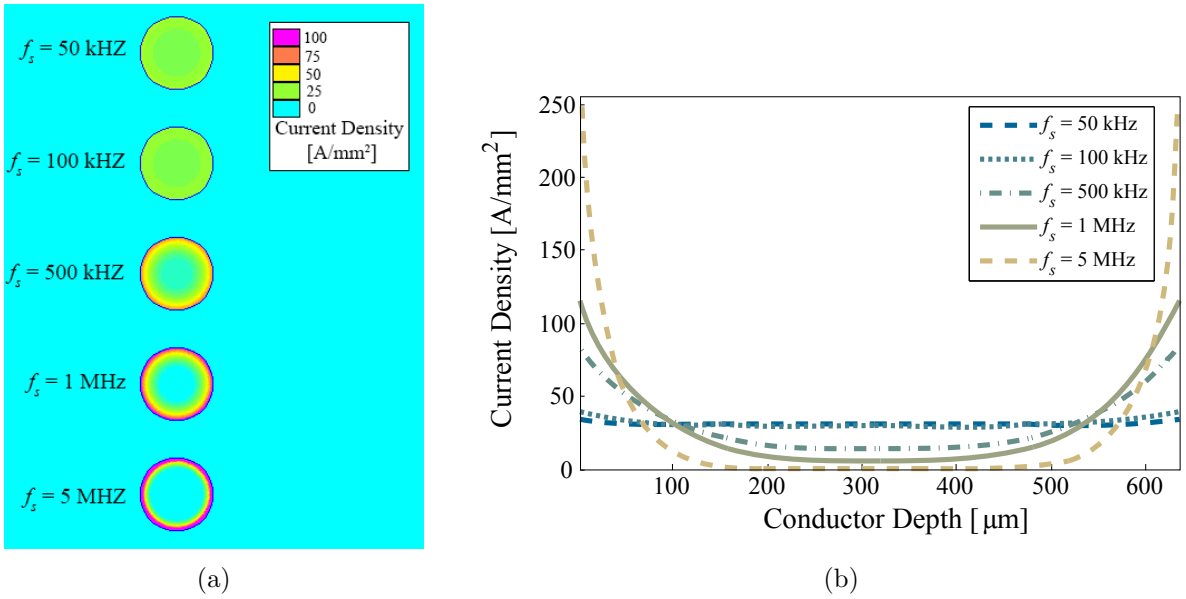


Figure 3.22: Comparison of core loss prediction and colorimetry-based experimental loss measurements for a sample transformer, excited at $f_0 = 20$ kHz with flux density waveform $B(t) = A\left[(1-c)\sin 2\pi f_0 t + c\sin 6\pi f_0 t\right]$, where $A = 200\text{mT}$ and the strength of the third harmonic c is varied. Figure is reproduced from [37].

as frequency increases, due to the presence of magnetic fields within the copper itself causing eddy currents to flow. This effect, known as the "skin effect", can be modeled by calculating the effective area of copper used at the given frequency, known as the skin depth δ [22]

$$\delta = \sqrt{\frac{\rho}{\pi \mu_0 f}} \,, \tag{3.48}$$

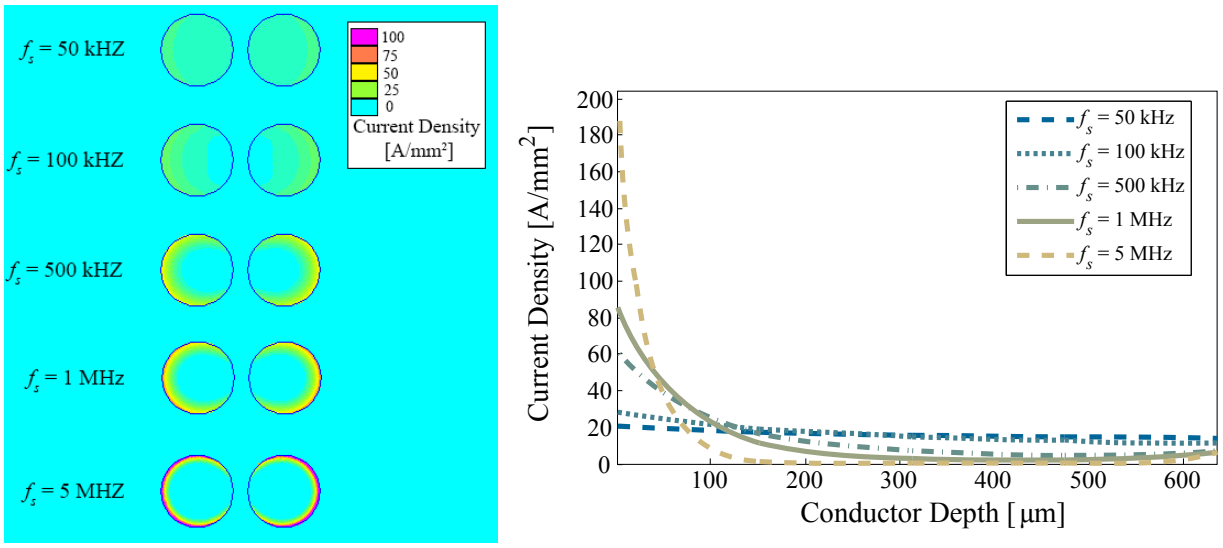
which can be calculated individually and applied to each frequency component in a fourier series expansion of the winding currents to obtain the conductor AC resistance.



(a) (b)

Figure 3.23: Current density distribution in a single, solid-core copper wire at varying frequencies shown for a 2-D cross-section (a) and a 1-D line bisecting the conductor on its diameter (b).

Calculations become more complex when multiple parallel conductors are considered. In Fig. 3.24, a second conductor is added in parallel with the original, with the pair still conducting a total current of 10 A. As frequency is increased, in addition to the skin effect reducing the current densities present in the conductor cores, H-field produce by the neighboring conductor causes additional eddy currents in the proximal surface of the adjacent windings. This further reduces the effective area of the conductor beyond that of skin effect alone. This increase in eddy currents in closely space parallel windings is termed "proximity effect". The effective resistivity of both the single-conductor and dual-conductor configurations are given for a range of frequencies in Table 3.6.



(a) (b)

Figure 3.24: Current density distribution in a two parallel, solid-core copper wire at varying frequencies shown for a 2-D cross-section (a) and a 1-D line bisecting a single conductor on its diameter (b).

At low frequency, the dual conductor case exhibits half the resistance of the single conductor case, as expected. However, as frequency increases, the advantage which the dual conductor configuration has over the single conductor case diminishes due to the additional eddy currents produced from the windings' close proximity. The magnitude of proximity losses increases with each layer in multi-

Table 3.6: AC Resistance in Single and Dual Conductors

	10 kHz	50 kHz	100 kHz	500 kHz	1 MHz	5 MHz
Resistance of Single Wire [mΩ/m]:	53.4	54.8	59.0	106.2	143.8	304.0
Resistance of Two Wires [mΩ/m]:	26.8	28.8	33.2	64.6	88.4	190.6
Ratio:	1.99	1.90	1.78	1.64	1.63	1.60

layer windings due to the additional buildup of field strength from the inner windings' current densities. One method for the mitigation of this buildup is to interleave winding layers of opposite current flow directions, as may be done by alternating layers of primary and secondary windings in a two-winding transformer. This allows some cancellation of field strength. Traditional approaches to the modeling of proximity effect broach the topic by approximating a single layer of windings as a single, effective copper foil, which reduces the complexity of calculations to allow the problem to be tractable [22,31]. However, these methods are quite complex and require exact knowledge of winding configuration prior to their execution. Further, in addition to the proximity between two windings, similar surpluses in eddy currents can be incurred due to winding proximity to air gap in the magnetic core such that they are exposed to the core flux which inherently fringes outwards at any air gap. This effect is even more difficult to model analytically due the necessity of quantifying the exact nature of the fringing flux path. Due to the complexity of these calculations, the most accurate and fastest method of analyzing the copper loss for a given winding configuration is found to be the direct finite element simulation of a specified transformer design. This process is further detailed in Appendix A.1.

A number of general principles may be applied to mitigate the effects of copper loss. In addition to the aforementioned interleaving of winding layers, the use of conductors whose width is

small relative to their skin depth has the potential to reduce the magnitude of skin effect in windings. This can be accomplished in one of two ways: either by converting from solid wire conductors to foils or hollow-core conductors so that a similar effective copper area can be obtained with a smaller depth, or through the use of bundled strands of higher-gauged wire whose total area matches that of the single solid-core conductor. However, either hollow-core or bundled wires will necessarily have a smaller area of copper due to the presence of air and insulation within the bundle cross-section which would be filled with copper in the single-conductor case. Additionally, if bundled conductors are implemented simply, bundle-level skin effect and strand-level proximity effects will quickly outweigh any advantage which may have been gained by reduced strand-level skin effect. The solution is the twisting of bundled conductors to create Litz wire, where twisting prevents any two conductors from residing in close proximity to one another for an extended distance.

3.6.1.3 DAB Transformer Implementation

In the initial implementation of the DAB transformer, both foil and Litz wire conductors are used to mitigate the effect of copper loss on converter efficiency. A foil secondary is used to maintain low conductor depth and small size while obtaining sufficient copper area to conduct the high secondary currents, while a litz primary is used to permit the high number of turns necessary to obtain the high step-down ratio of the transformer with minimal increase in losses above those predicted by DC resistance of the winding. With these two steps, it is assumed that the AC copper losses have been reduced to a sufficient extent that the transformer can be optimized based solely on DC winding resistance losses and the iGSE/NSE approximation of core losses. The magnitude of copper losses is later calculated analytically and simulated through finite element analysis to confirm the feasibility of the proposed design.

The high frequency "L" material from Magnetics Inc. is chosen to implement the DAB converter transformer. The characteristics of the material, as modeled from technical reference documents available from the manufacturer [43] are given in Table 3.7, where Steinmetz core loss parameters are given for ΔB in Tesla and f_s in Hz. Additionally, an array of core geometries

Table 3.7: Mag-Inc L-material Characteristics

Name	μ_r	K_v	α	β	B_{max} [mT]
L	900	9e-7	1.95	2.28	420

are used to aid in the consideration of transformer design. The effective (averaged magnetic) core length, area, volume, and winding area are given in Table 3.8 for five example cores. These cores correspond roughly to the toroids of Fig. 3.25(a), which are shown to aid in conception of the associated core size with each example geometry, though the effective dimensions could equally well represent non-toroidal geometries of similar size.

Table 3.8: Example Core Geometry Parameters

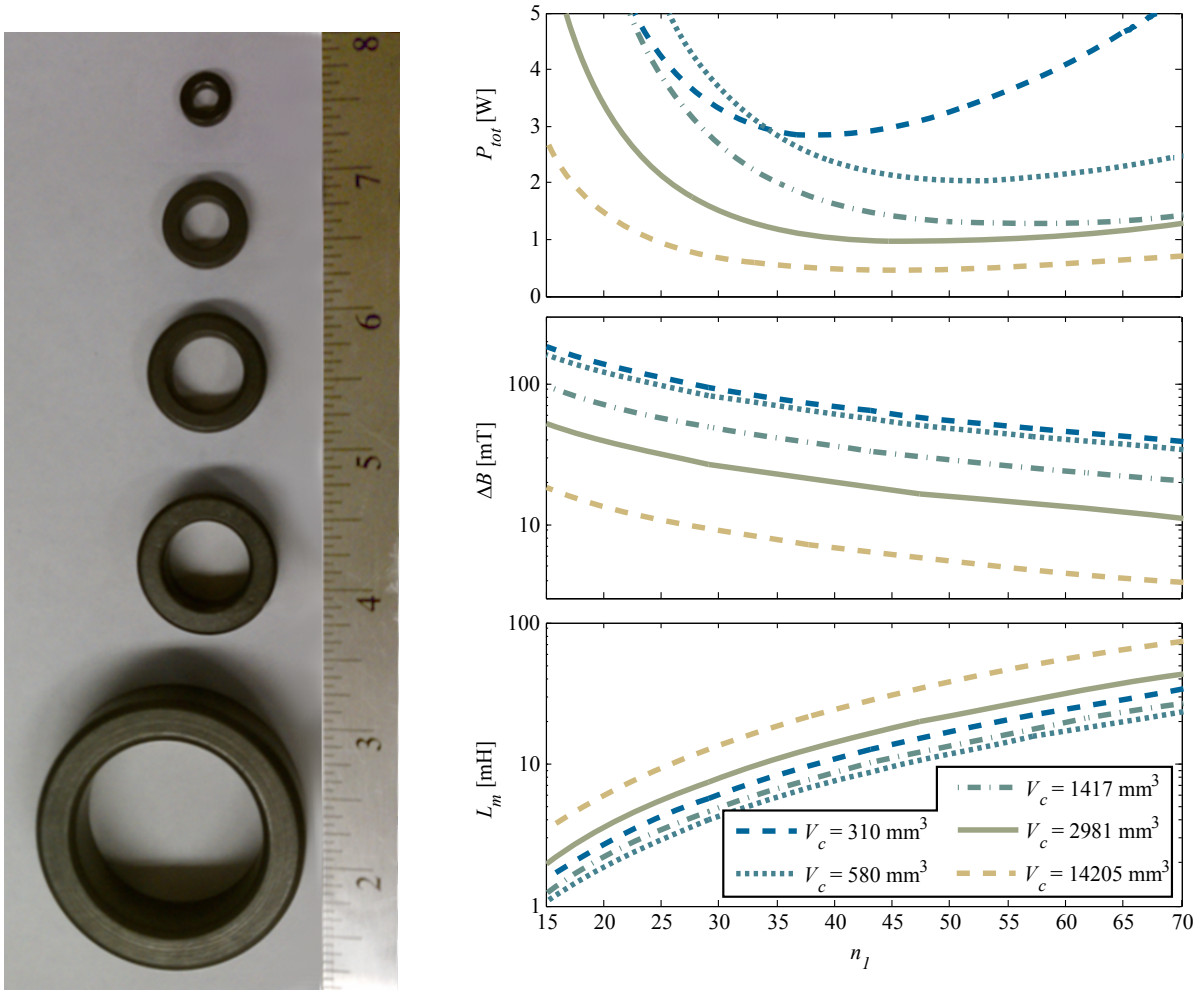
Core	L_e[mm]	A_e[mm^2]	V_e[mm^3]	W_A[mm^2]
#1	22.7	13.7	310	21.9
#2	37.2	15.6	580	57.7
#3	54.1	26.2	1417	141
#4	61.5	48	2981	185
#5	103	138	14205	540

An optimization can now be run in which for each example core the total loss $P_{tot} = P_{core}+P_{cu}$ is calculated for a varying number of primary turns n_1 and secondary turns $n_2 = n_t \cdot n_1$. It is assumed that the entire window area of each core will be filled with windings, but that a fill factor of only $K_u = 0.05$ results from the use of a winding bobbin, litz wire, and the complicated winding strategy of interleaving foil and litz. Though this value is significantly lower than the common approximations for traditional magnetics [88], the actual fill factor of the realized transformer is later calculated to be $K_u = 0.085$, indicating that this selection is indeed a relatively accurate but conservative value. It is further enforced that, in the analytical optimization, the available window area $K_u \cdot W_A$ is evenly split between primary and secondary copper.

Under these assumptions, the transformer total losses considering a 120 W, 1 MHz operating

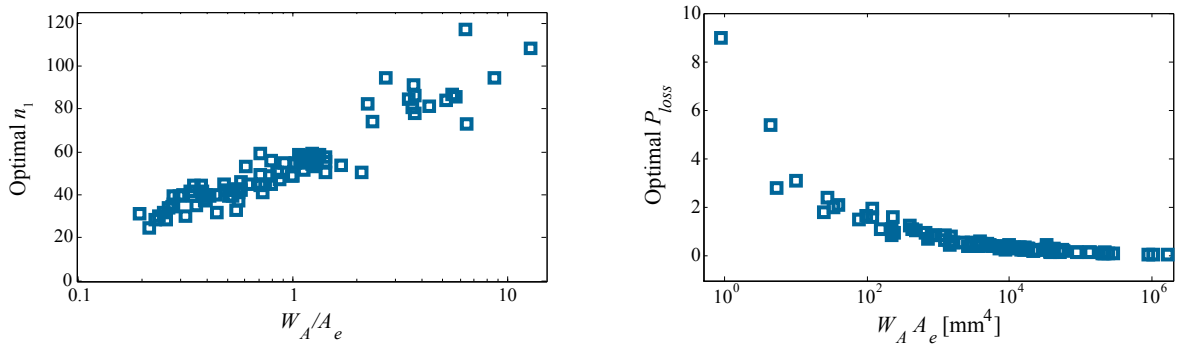
point and $n_t = 0.08$ are calculated iteratively for a range of primary turn counts n_1, and for each of the sample cores. The results are given in Fig. 3.25(b). As may be expected, the largest core offers the smallest achievable power loss. However, given the emphasis on retaining a small overall converter footprint, a toroid of nearly two inches diameter is not an appropriate design solution. Thus, the actual transformer core selection requires some non-quantitative comparison of the tradeoffs between device size and converter efficiency. Because the design has undertaken the elevated 1 MHz switching frequency, it is desired to take advantage of this through implementation of a small-footprint device.

One interesting facet of the plot of Fig. 3.25 is the low value of n_1 which results in minimum power loss in the smallest of the example core geometries. The optimal value of n_1 is determined by a tradeoff between core and copper losses in the device; a larger number of turns results in reduced peak flux density and core loss, but yields longer primary and secondary windings, each of which must be made of smaller area conductors in order to maintain within the winding area, therefore increasing winding resistance and conduction losses. In a similar manner, for a given core volume, a tradeoff may be made in the relative values of the winding area W_A and effective ferrite area A_e. To view this tradeoff more explicitly, Fig. 3.26(a) shows the results when the optimization is run on all of the cores in Appendix A.2. The value of n_1 at which minimum power loss occurs is plotted with respect to a newly fabricated figure of merit for the cores, W_A/A_e. This FOM attempts to capture how much of the volume of a given core is dedicated to ferrite and how much is left as winding window which can be used for copper. For a given transformer size, as W_A is increased, A_e will decrease accordingly, and the optimal n_1 will be forced to increase to counteract the greater flux densities which would result from the smaller A_e. Increasing A_e reduces flux density, but will in turn decrease the possible winding area, therefore requiring fewer total turns n_1 in order to keep conduction losses down. The W_A/A_e FOM is therefore a measure of the inherent bias of the core toward core or copper loss. This is in contrast to the more traditional $W_A \cdot A_e$ FOM in Fig. 3.26(b) which is sometimes included in manufacturer data. This product of winding area and ferrite area gives a measure of the achievable efficiency of the core assuming that the designer will



(a) (b)

Figure 3.25: Example output of iterative design calculations for core loss, magnetizing inductance, and flux density in a transformer with varying number of primary turns (a). In (b), the cores used in the calculations of (a) are shown for size reference.



(a) (b)

Figure 3.26: Traditional and newly developed FOMs for the inherent relation between winding area and core cross-sectional area.

adjust winding turns and copper area to overcome any inherent bias and balance core and copper loss manually.

Because the design is biased toward high frequency and low power, core losses are expected to be of greater concern in the DAB transformer. Therefore, it is desired to select a core geometry which has a relatively small W_A/A_e FOM, which biases the core towards the reduction of core loss rather than conduction loss. Of the common core geometries in Appendix A.2, the pot-type cores in general exhibit the lowest W_A/A_e, as their geometries favor high ferrite area for a given volume. These include the PQ, POT, and RM cores. Among traditional ferrite shapes, ER cores obtain the lowest value of W_A/A_e on average.

With these motivating factors in mind, it was chosen to implement the first revision of the DAB transformer using a PQ20/20 core, wound as detailed in Table 3.9

Table 3.9: DAB Transformer Implementation Details

Core	Material	n_1	n_2	Primary Conductor	Secondary Winding	$L_{lk}{}^{\dagger}$	$L_m{}^{\dagger}$
PQ20/20	L	25	2	135-strand, 46-AWG unserved Litz	3 oz copper foil	2 μH	1 mH

† referred to primary winding

3.6.2 Transformer Parasitic Elements

Traditionally, both the leakage inductance L_{lk} and magnetizing inductance L_m of a transformer are considered parasitic, with the ideal transformer exhibiting $L_{lk} = 0$ and $L_m \to \infty$. In the DAB converter, the transformer leakage inductance L_{lk} appears in series with the tank inductance, and is therefore non-parasitic, and incorporated into circuit operation. Further, if manufacturing constraints permit the precise control of L_{lk} through precisely wound primary and secondary coils, it is advantageous to incorporate all of the tank inductance L_l as leakage inductance L_{lk} due to the relative absence of core loss in air-core inductances. Barring this possibility, the designed tank inductance can be achieved with a supplemental inductor designed to exhibit an inductance which is equal to $L_l - L_{lk}$ so that the sum of transformer leakage and the discrete tank inductances yields

the desired effective inductance L_l. Though using the total L_l without differentiation between leakage or discrete inductance is sufficient in most analysis, the voltage division between the air core transformer leakage L_{lk} and the parasitic layout inductances L_D should be taken into account when calculating the tank inductance core loss. The air-core leakage and parasitic inductances will exhibit no core loss, whereas the tank inductor itself may exhibit core loss if a core material is used. When applying core loss calculation techniques to the tank inductance, its effective voltage at any moment in circuit operation is given by

$$v_l(t) = \left(v_p(t) - \frac{v_s(t)}{n_t} \right) \frac{L_l}{L_l + L_{lk} + 2\frac{L_D}{n_t}} \ , \tag{3.49}$$

The magnetizing inductance L_m is not considered in the current analysis of the converter. However, the analysis incorporating L_m is simple and results in little alteration to circuit operation under the assumption that $L_m \gg L_l$. Under these conditions, the magnetizing inductance current, as seen from the primary of the transformer, is very nearly a perfect AC-only triangle wave with peak value

$$i_{lm,pk} \leq \frac{V_g T_s}{4 L_m} \ , \tag{3.50}$$

which bounds the magnetizing current for the given design to 37.5 mA, which is sufficiently small to only negligibly affect circuit operation. It should be noted, however, that should a design be constructed in which magnetizing current does significantly affect circuit operation, its polarity is such that it can assist in obtaining primary ZVS, though at the detriments of RMS currents. Thus one possible approach for extension of ZVS range of the converter considers intentionally reducing L_m through introducing an air gap into the transformer core; this work does not consider this approach due to the inherent penalties in conduction losses at all power levels.

3.7 Experimental Results

The proposed DAB converter was constructed in two models, one with entirely GaN and one with entirely Si FETs. Both used the same transformer, as described in Table 3.9, and both used a discrete, 50 nH tank inductance implemented on the transformer secondary to achieve a total

tank inductance which is slightly larger than the designed $L_l = 8\ \mu$H. The secondary inductor was implemented as a commercial part, the LP02-500-1S from ICE Components [89]. Though exposed to higher currents if implemented on the secondary, the tank inductance may be implemented with much smaller value and footprint due to the turns ratio of the transformer. Core loss data for this inductor was furnished upon request.

In the all-Si DAB, FDMC2610 devices were used for all primary transistors and CSD16325 on the secondary. In the GaN implementation, EPC1015 and EPC1012 were selected. In both cases, primary devices were selected to obtain low capacitance, while secondary devices were chosen with minimal on-resistance. Because gate drive losses are considered independent of the proposed optimization, eight DCH0105 isolated supplies are implemented on a separate PCB to provide power to gate drivers with very low common mode coupling. The converter power stage occupies roughly 3 in^2 on a dual-sided PCB, without the isolated supplies or control circuitry. Waveforms for

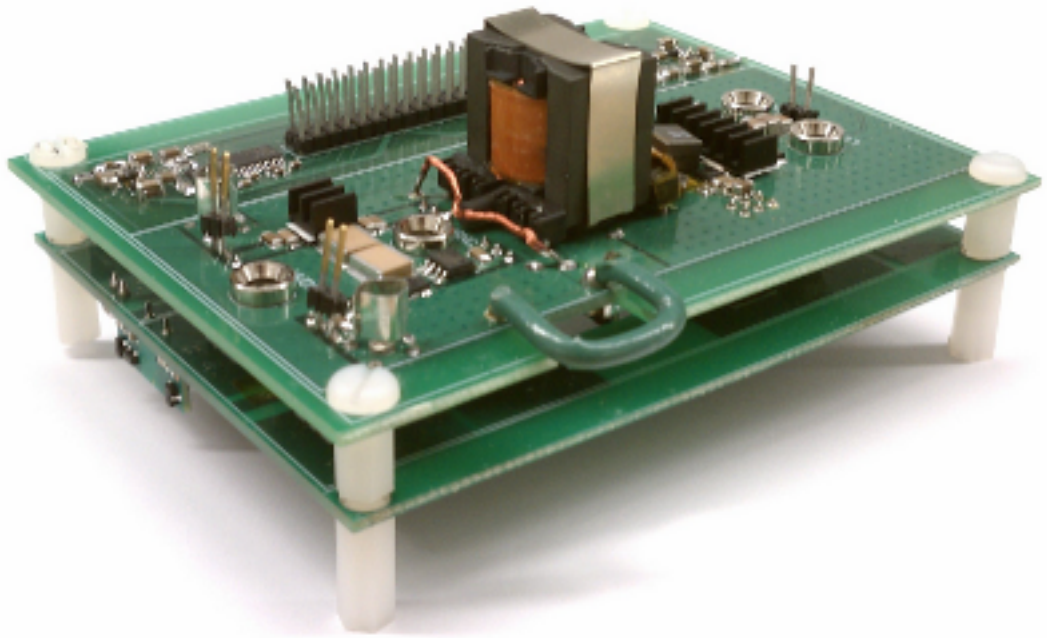
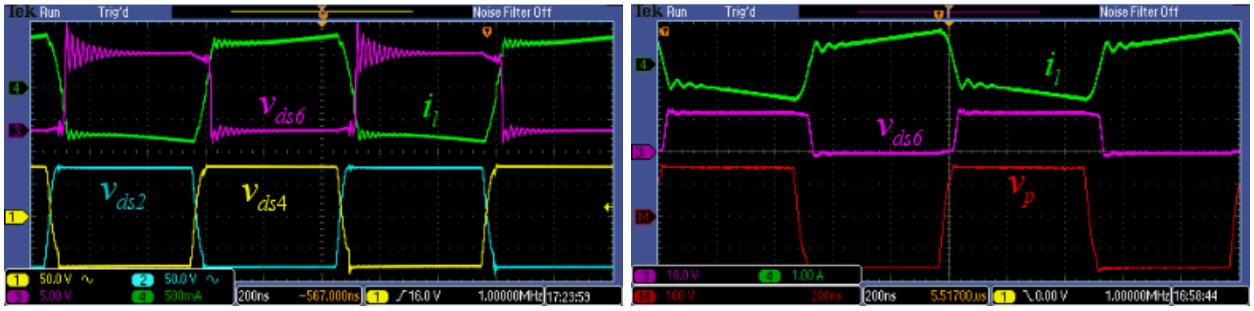


Figure 3.27: Prototype DAB converter. Gate drive circuitry is implemented seperately from the power stage, and is contained on a second PCB mounted below the power stage PCB.

150-to-12 V, 100 W, 1 MHz power conversion are given in Fig. 3.28(a) for the silicon implementation

and Fig. 3.28(b) for the GaN converter. For the silicon converter, the analytical and measured state



(a) (b)

Figure 3.28: Prototype experimental waveforms of the DAB converter operating at 100 W with Si devices (a) and GaN devices (b) on both primary and secondary

planes are additionally compared in Fig. 3.29. Efficiencies at this operating point were 97.0% and 96.6%, respectively. The breakdown of losees as predicted by the results of the analysis presented in this chapter, are given in Table 3.10. Gate drive losses are not included in measured or calculated efficiency numbers, but are estimated based on datasheet parameters to be approximately 880 mW for the Si converter and 330 mW for the GaN converter.

A number of interesting characteristics emerge from the results of Table 3.10. First, the switching losses due to secondary-side inductance vary significantly between the GaN and Si case; this is due to the packaging of the devices. While the CSD16325 Si MOSFETs are encased in a DualCool micro-leadframe package (MLP), the EPC GaN devices are distributed with a minimal, wafer-level land grid array (LGA). Both packages are shown in Fig. 3.30. The minimal packaging of the EPC GaN devices allows parasitic inductances L_D on the secondary devices to be significantly lower than those of the silicon MOSFETs in MLP package [85, 90, 91]. This results in a lower total energy stored in L_D at device turn-off, and therefore a lower loss and less ringing on the secondary, as is noticeable when comparing the waveforms of Fig. 3.28.

It is additionally noteworthy that, despite this reduced loss and larger predicted efficiency of the GaN converter, the experimental results show a lower efficiency in the GaN prototype as compared to the Si version of the DAB. One potential explanation for this discrepancy is that

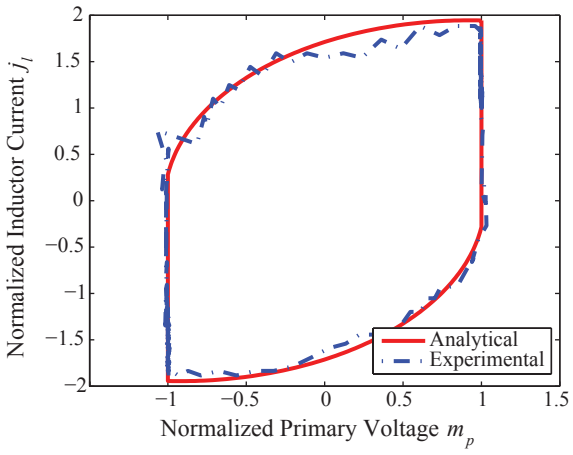


Figure 3.29: Analytical and experimental results for primary state plane of prototype DAB operating at 80 W output power.

(a) (b)

Figure 3.30: Images showing the device packages; the EPC GaN devices are packaged in wafer-level LGA (a) while the CSD16325 Si MOSFETs are encased in a DualCool MLP package (b)

Table 3.10: Si and GaN DAB Experimental Efficiency

	Converter	
Power Loss [mW]	Si	GaN
Primary Device Conduction	172	67
Secondary Device Conduction	271	511
Secondary Parasitic Inductance	515	260
Transformer Core	397	391
Transformer Copper	392	393
Inductor Core	321	308
Inductor Copper	80	80
Predicted Efficiency	97.8	98.0
Measured Efficiency	97.0	96.6

inherent issues with the GaN technology, including phenomena such as current collapse, charge trapping [92], and dynamic r_{on} discrepancies [93], cause the apparent loss parameters of the GaN devices in a switching power converter to differ from their values as measured at DC. Tests were not undertaken to confirm this hypothesis, but communications with the manufacturer revealed that this explanation is possible, if not likely. Although the magnitude of these effects' contribution to losses is not known, it has been stated that updated GaN transistors in this product line have significantly mitigated these effects to the point where they now result in less than 10% increase in device on-resistance after thousands of hours of accelerated life testing [92]. The work which forms the basis of this thesis did not continue to work with GaN devices due to the unavailability of the second-generation devices at the time of testing.

Summary

Although ignored in typical applications, the impact of the primary resonant interval on converter operation is significant in the case of the low-power, large step-down, and high-frequency dual active bridge (DAB) converter. State plane analysis techniques present a simple and intuitive

approach for analyzing converter operation using geometrical arguments, in order to solve converter operation with the primary resonant interval included explicitly. From this, loss models can be developed which may then be used to design the converter for high efficiency.

To this end, one approach to high efficiency DAB design at a single operating power consists of selecting a tank inductance which will store sufficient energy at the designed operating power to just obtain ZVS of primary devices. This allows all devices to operate with zero voltage switching, eliminating the significant power loss that would be associated with non-ZVS at high frequency. From the state plane analysis results, it is discerned that while the primary resonant interval significantly impacts converter operational waveforms, the secondary interval does not, and therefore may be neglected when solving converter waveforms. Therefore, when selecting devices to implement each of the transistors, primary devices should be selected to obtain low parasitic output capacitance C_p and secondary device to obtain low on-resistance $r_{on,s}$. These choices will, respectively, minimize the RMS currents throughout the converter, and minimize the device conduction losses associated with those currents. The converter magnetics can then be designed independently to obtain a desired trade-off between low-loss and small overall converter footprint.

Chapter 4

Detailed Resonant Transition Analysis

The analysis of the previous section has shown that the details of the resonant, ZVS transitions may have significant impact on converter design, analysis, and operation. With this realization as motivation, traditional circuit analysis techniques including, primarily, state plane analysis were applied to discern converter operation with the resonant interval dynamics included explicitly. However, this analysis relied heavily on the assumption of a single, linear value – C_p on the primary – which can be used to model the parasitic energy storage behavior of the transistor devices. The actual behavior of this parasitic, $C_{ds}(v_{ds})$ is highly nonlinear and is a strong function of the drain-to-source voltage present on the device when not conducting.

4.1 Nonlinearity of Transistor Output Capacitance

The inherent MOSFET parasitics, diagrammed in Fig. 2.13(c), can be understood by reviewing semiconductor theory for the generalized cross section of a power silicon MOSFET, as in Fig. 4.1. Though other variations exist, this cross section shows many of the general features common among n-substrate, vertical, power MOSFET device (NMOS) [22,94]. The vertical device allows both high blocking voltage and low r_{on}, relative to traditional lateral devices, making them the standard for switched-mode devices in most applications where discrete devices are permissible.

In Fig. 4.1, hatched regions indicate metalized contacts while shaded regions indicate electrically-insulating oxide layers. Within the silicon, n and p denotations indicate regions of silicon doped

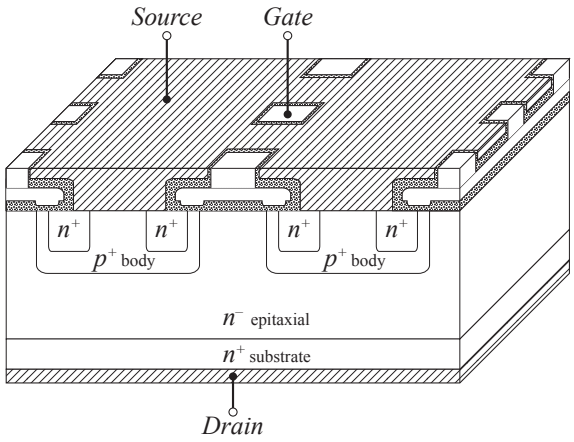


Figure 4.1: Cross section of a general silicon power MOSFET.

to increase donor or acceptor concentrations, respectively, with superscript + or − used to indicate relative doping concentrations. The highly-doped p^+ body region electrically isolates the n^+ wells of the source tie from the n^+ substrate, which is tied to the device drain contact. The height of the large, n^- epitaxial layer determines the device voltage-blocking capabilities, while the overall width and length may be adjusted to obtain a desired device area; as discussed previously, this area will reduce r_{on} at the expense of increased parasitic stored charges. Operated in switched mode, the MOSFET will ideally jump between the nonconducting state with $V_{gs} \approx 0$ V and the MOSFET in cutoff, and the conducting state in which $V_{gs} > V_{th}$ and $V_{ds} \approx 0$ V, placing the device in the triode (or ohmic) region. The individual components which constitute r_{on} in the conducting state, and each of the stored charges in the non-conducting state of the device are shown in Fig. 4.2.

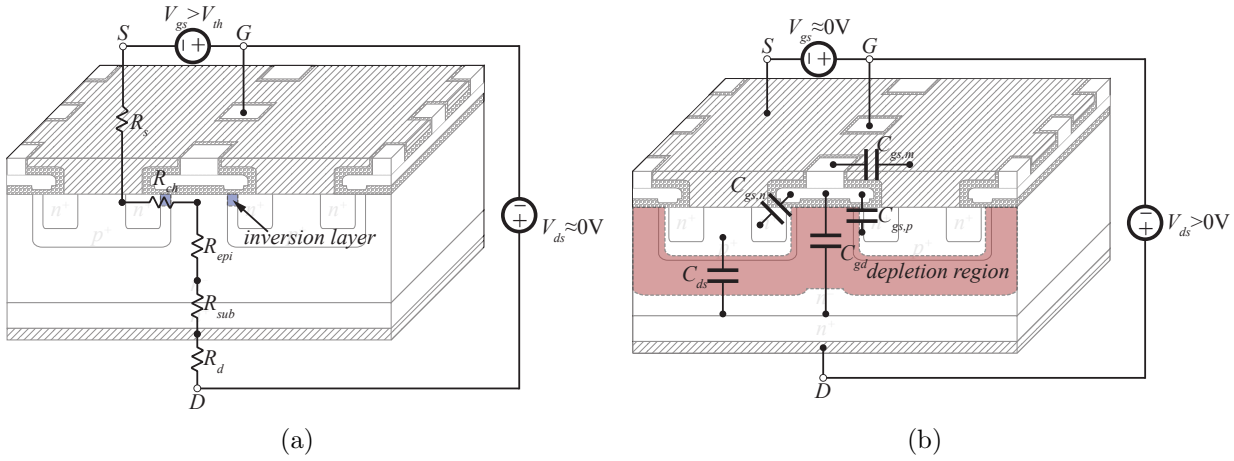


Figure 4.2: Physical origins of the silicon MOSFET r_{on} during the conducting state (a) and device capacitances (b).

To switch the device on, increasing the gate-to-source voltage above the inherent threshold voltage V_{th} of the process draws electrons into the p^+ body region below the gate, effectively inverting the carrier concentration in this region and forming a conducting channel from source to drain of the device. With a channel formed, significant amounts of current may now flow between the contacts, with the effective resistance of the device given by the sum of the resistive behavior of each region in its path. The source metal, channel, epitaxial layer, substrate layer, and drain

metal combine to give the device on-resistance

$$r_{on} = R_s + R_{ch} + R_{epi} + R_{sub} + R_d \ . \tag{4.1}$$

For high voltage devices, where the height of the epitaxial layer must be large in order to obtain the rated blocking abilities of the device, the overall on-resistance of the device is generally dominated by R_{epi}.

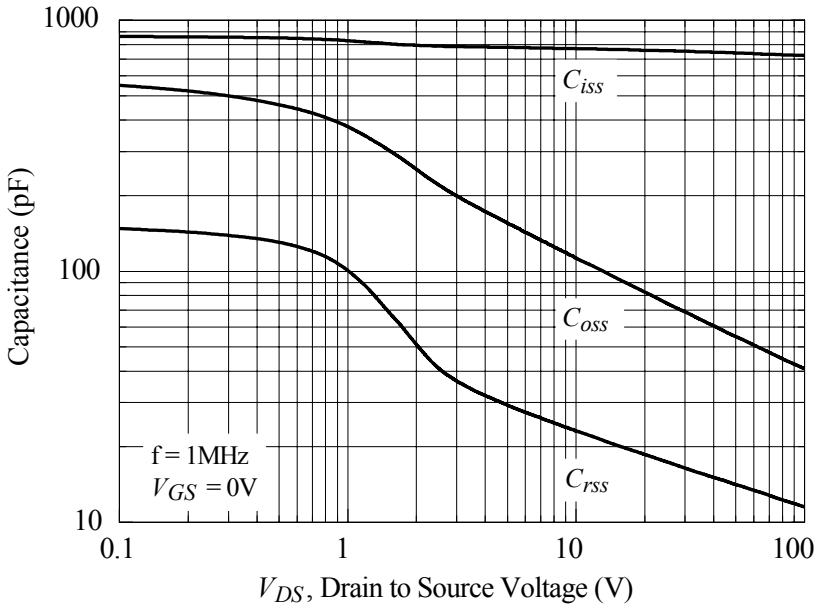
In the non-conducting state, $V_{gs} \approx 0$ V and the inversion layer is dispersed preventing current conduction between drain and source. With the device fully off, the drain-to-source voltage V_{ds} may rise to the rated blocking voltage of the device. As it does so, a depletion region is formed at the p-n junction between drain and body (shorted to source) whose width is directly correlated to the magnitude of V_{ds}; the region extends further into the lightly doped n^- epitaxial layer than the heavily doped p^+ body. Capacitances exist between any two regions or materials in the device in this state. Those capacitances which traverse the depletion region, C_{gd} and C_{ds}, will have magnitudes which vary heavily with the width of this depletion region, and therefore with the magnitude of V_{ds}. The gate-to-source capacitance, C_{gs} has multiple components due to capacitances between the gate metal and the various regions which make up the body and source of the device, none of which exhibit significant dependence on the depletion region, though the overall C_{gs} will be heavily nonlinear with respect to V_{gs} due to the changes in regions presented when the inversion layer is formed for $V_{gs} > V_{th}$.

Typically, manufacturer data for parasitic capacitances in a MOS device is given in a plot of the form shown in e.g. Fig. 4.3 [95]. Where the three measured capacitances, C_{oss}, C_{iss}, and C_{rss} are the measured values between any two ports with either V_{gs} or V_{ds} shorted together, where appropriate. These measured values can be related to the theoretical port capacitances as

$$C_{oss} = C_{gd} + C_{ds} \ , \tag{4.2a}$$

$$C_{iss} = C_{gd} + C_{gs} \ , \tag{4.2b}$$

$$C_{rss} = C_{gd} \ . \tag{4.2c}$$



(a)

Dynamic Characteristics

C_{iss}	Input Capacitance	V_{DS} = 100V, V_{GS} = 0V, f = 1MHz		720	960	pF
C_{oss}	Output Capacitance			41	55	pF
C_{rss}	Reverse Transfer Capacitance			12	20	pF
R_g	Gate Resistance	f = 1MHz		0.7		Ω

(b)

Figure 4.3: Parasitic capacitances of FDMC2610, as reported in the device datasheet. The plot of (a) demonstrates the capacitances as they vary with V_{ds} while the table values of (b) are evaluated at a single value $V_{ds} = 100$ V.

Examining the plot of Fig. 4.3(a), a few characteristics should be noted which are generally applicable to silicon MOS devices. First, $C_{gd} \ll C_{ds}$ and therefore

$$C_{ds} \approx C_{oss} \ . \tag{4.3}$$

This relation could be predicted from the origin of the capacitances in Fig. 4.2(b), where the distance between ports is larger and the area smaller for the effective capacitor formed between gate and drain, as compared to that formed between drain and source. Similarly, the gate-to-source capacitance is expected the be the largest of the three. Second, taking note of the log-scale axes, the variation in value of both C_{gd} and C_{ds} is very large with respect to V_{ds}, while that of C_{gs} is minimal, as predicted. Additionally, for both C_{gd} and C_{ds}, magnitudes are largest for very small values of V_{ds}, for which the width of the induced depletion region narrows accordingly.

The GaN devices considered and used in this work are enhancement-mode (eGaN) devices, the structure of which is diagrammed in Fig. 4.4(a) [96]. The transistor is constructed as a lateral device, in contrast to the vertical power MOSFET. The eGaN-FET begins with a silicon substrate, though devices may also be constructed with silicon-carbide (SiC) or even GaN substrates with resulting increases in manufacturing costs and complexity. GaN is grown on the Si substrate using a thin layer of aluminum nitride (AlN), which is then topped with a thin layer of aluminum gallium nitride (AlGaN). The interaction of GaN and AlGaN causes the formation of a two-dimensional electron gas (2DEG) which is filled with abundant, mobile electrons. As opposed to the inherent depletion-mode GaN-devices which result from the use of GaN as semiconductor material, eGaN devices use techniques such as recessed gate, flooring implant, or positively doped GaN crystal to dissipate the 2DEG underneath the gate under zero-bias gate conditions and obtain enhancement-mode behaviors [92]. As with the MOSFET, the structural cross section shown is repeated many times to obtain the desired device area and FOM tradeoffs.

Fig. 4.4(b) shows the location of the parasitic capacitances in the lateral eGaN structure [96]. Due, in part, to the lateral device structure, the capacitances are fairly small, particularly

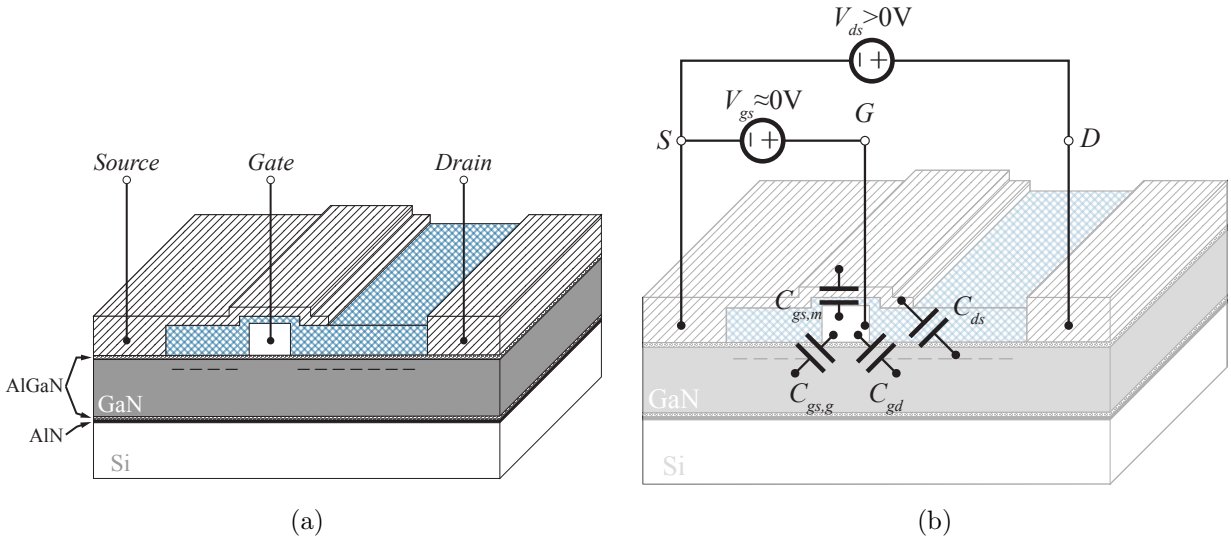


Figure 4.4: Cross section of a general eGaN-FET (a) and physical origin of device capacitances (b). Hatched regions indicate metalized contacts while shaded regions indicate AlGaN layers and cross-hatched regions are protection dielectrics.

both C_{gd} and C_{ds} which arise only from gate and source overlap with the drain region of the 2DEG, respectively. The gate-to-source capacitance is relatively prevalent in comparison to C_{gd} and C_{ds}, but remains minimal when compared to similar silicon MOSFETs. Further, because of the high electron mobility and critical field strength of GaN relative to silicon, a given amount of on-resistance may be obtained with a smaller overall die size, resulting in the improved FOM characteristics exhibited by GaN.

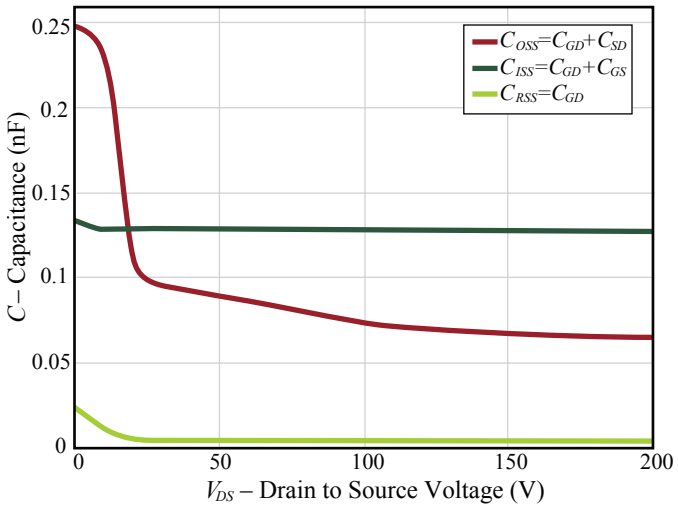
For an example eGaN device [50], the datasheet-reported capacitances are shown in Fig. 4.5. Note that, although the magnitude and variation of the eGaN devices is significantly smaller (and is plotted on linear, rather than logarithmic axes), the same conclusions stated for silicon devices hold true for GaN devices as well.

In both the silicon and GaN cases, the nonlinearities of the output capacitance C_{ds} are significant. Given the established significance of resonant interval behavior on converter operation in the high step-down, high-frequency DAB, a method of addressing the nonlinearity directly is needed, and is developed here, as first presented in [97].

4.2 Circuit-Oriented Treatment of Nonlinear Capacitances

Circuit-oriented treatment of nonlinear capacitances has been addressed in various ways in prior studies. Most commonly the capacitances themselves are assumed to be negligibly small [46, 80, 81], leading to the common approximation that a FET initially blocking a large voltage v_{ds} can be zero-voltage switched as long as its drain current i_d turns negative prior to the switching instant [26,98], e.g. any transistor bridge with an inductive load impedance. This approach neglects the necessary duration of the ZVS interval entirely, which leads to significant discrepancy at high switching frequency and low power, where the time required to discharge the capacitor may be significant in comparison to the switching period.

Works such as [83,99–101] have replaced the nonlinear capacitor with a linear equivalent, but have rarely detailed in what way the equivalent capacitance was chosen. Further, many studies have used a single equivalent linear capacitance to model multiple characteristics of circuit behavior. It



(a)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic Characteristics (T_J = 25°C unless otherwise stated)						
C_{ISS}	Input Capacitance	V_{DS} = 100 V, V_{GS} = 0 V		128	145	pF
C_{OSS}	Output Capacitance			73	95	
C_{RSS}	Reverse Transfer Capacitance			3.3	4.4	

(b)

Figure 4.5: Parasitic capacitances of EPC2012, as reported in the device datasheet. The plot of (a) demonstrates the capacitances as they vary with V_{ds} while the table values of (b) are evaluated at a single value $V_{ds} = 100$ V.

is shown experimentally, e.g. in [102], that the nonlinearity cannot be modeled correctly in terms of time, energy, and charge simultaneously by a single linear capacitor. The dependence on drain-to-source voltage of the MOSFET output capacitance can be modeled in its entirety in circuit simulators. Often, such simulations have been carried out with a simplified empirical fit to the C_{oss} curve of the form

$$C_{oss}(v_{ds}) = \frac{C_0}{\left(1 + \frac{v_{ds}}{V_0}\right)^m}, \tag{4.4}$$

which is sufficiently accurate for simple devices [103], but errant for more complex in modern devices, including superjunction devices [104] as well as varying architectures of GaN [51, 52, 105] and SiC [106, 107] switching devices. Further, this analysis approach remains overly cumbersome for any hand analysis [104, 108, 109]. So long as the output capacitor remains nonlinear, the circuit analysis methods traditionally used in power electronics circuits cannot be applied directly. Thus, it is useful to create a clear and consistent framework for treating nonlinear capacitors in switching power converters by replacing them with linear equivalents.

4.2.1 Circuit Analysis with Nonlinear Capacitors

To further demonstrate the variation in C_{oss} among a variety of devices, materials, and fabrication processes, a number of example curves are shown in Fig. 4.6. If datasheets do not contain sufficient data, a simple impedance analyzer with DC bias is capable of producing the C_{oss} curves, though more precise methods exist [107, 110–114]. It is desired to develop linear equivalents directly based on this data, so that circuit designers may compare the merits of many different devices prior to circuit construction and testing. Further, because the shapes of the curves for differing devices vary widely, it is desired to avoid empirical fit formulas such as that of (4.4), and instead develop a method that remains valid for arbitrarily shaped C_{oss}-V_{DS} data.

Given a curve containing C_{oss}-V_{DS} data, it must be understood in what sense the plots of C_{oss} model the behavior of the device in a circuit. C_{oss} can be understood as a small-signal equivalent

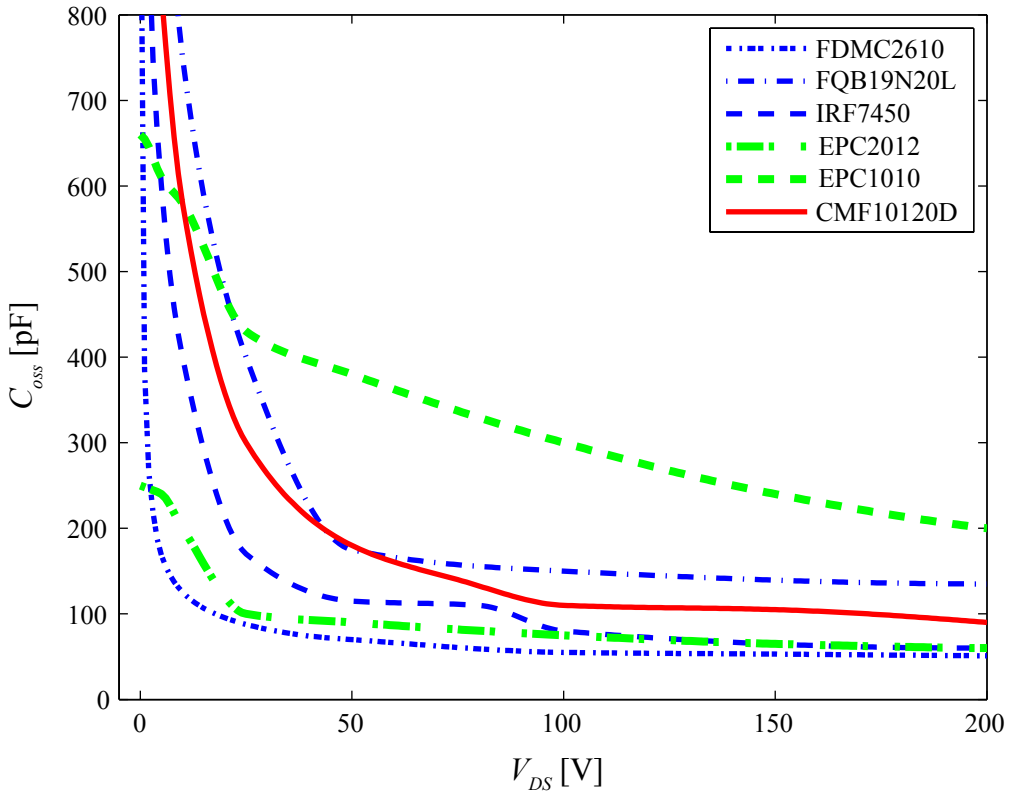


Figure 4.6: Examples of differing C_{oss} voltage dependencies for three silicon devices, two GaN devices, and one SiC device.

capacitance, such that

$$\hat{i}_c = C_{oss}\Big|_{V_{DS}} \frac{d\hat{v}_{ds}}{dt} \tag{4.5}$$

holds true at any given bias voltage V_{DS}, assuming a small-signal perturbation $\hat{v}_{ds} \ll V_{DS}$.

It is important to consider how the analysis in this manner differs from the traditional knowledge base developed for linear capacitors. As a simplified and generalized example en route to the DAB converter, the half-bridge circuit of Fig. 4.7 can be used to model behavior of resonant intervals depending on relative magnitudes of V_A and V_B and the direction of power flow. Because the output capacitances of both devices are connected between the switching node and a DC node, the two capacitances do not represent independent states of the circuit. Thus, in traditional analysis, they can be combined into a single capacitance, $C_{sw} = C_{oss}(v_{ds1})||C_{oss}(v_{ds2})$. To do so with nonlinear capacitances, the voltage dependence of each device must be taken into account. Given that $v_{ds2} = V_A - v_{ds1}$, the resulting nonlinear switched-node capacitance C_{sw} can be calculated as shown in Fig. 4.8. Since the DC bias information on the capacitance of M_2 has been removed from the circuit, the use of C_{sw} is equivalent only in an AC sense. Equivalently stated, C_{sw} is a small-signal capacitance which considers V_A as an AC ground. This is true in the linear case as well, and means that the use of C_{sw} correctly models the impedance seen at v_{sw}, but cannot accurately represent the energy storage of the system, which relies on DC bias information.

Using the bulk nonlinear capacitance C_{sw}, the half-bridge circuit can be reduced during a switching transition to the equivalent circuit of Fig. 4.9a in the case of a hard switching transition, or that of Fig. 4.9b when soft switching is obtained. Though each of these circuits are well known for the case of linear capacitors, the established solutions for quantities such as supplied energy, resistive loss, transition time or inductor stored energy do not hold for the nonlinear case, and thus must be reformulated.

In the following section, the general nature of nonlinear capacitances is addressed directly, and linear equivalent capacitors are developed for which the traditional analysis tools and results can once again be used to obtain correct predictions of capacitor energy storage, hard switched

loss, and resonant transition time, among other parameters.

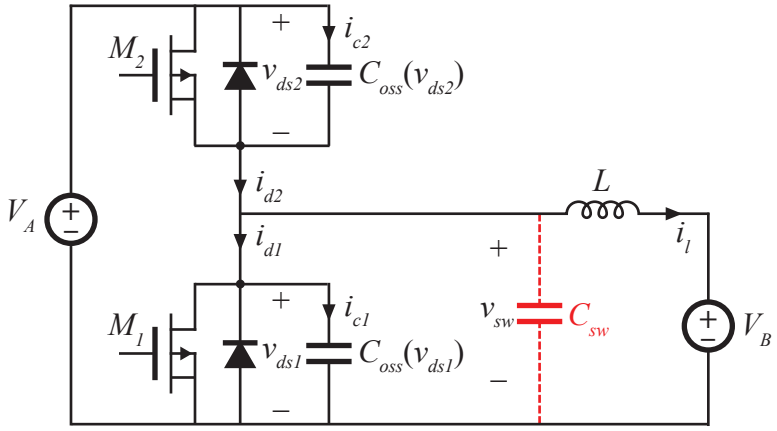


Figure 4.7: Half-bridge circuit. C_{sw} represents the combined output capacitances of M_1 and M_2

4.2.2 Development of Linear Equivalent Capacitances

In order to develop equivalent linear capacitors, analysis must focus on parameters of interest on which to base the equivalence. Because of their fundamental nonlinearity, a constant-valued, linear capacitance will only be able to correctly model a single parameter for a given voltage transition. First, independent of the application circuit, both the energy and charge required to move the capacitance between two voltages should be addressed. Beyond these two, all other parameters of interest pertain to the application circuit itself. To remain as general as possible, the circuit of Fig. 4.9c is used, and a transition is considered throughout this section which results in v_c moving from zero to $v_c = V_A$. The capacitance C_x is a generalized nonlinear capacitance and may represent C_{oss} or C_{sw}, where appropriate, or any other capacitance-versus-voltage curve of interest. In these voltage transitions, the energy stored, supplied, or dissipated in the remaining components of the circuit is also of interest, as well as the time taken by a resonant voltage transition, which informs optimal dead time selection in a soft-switched converter.

The simplest parameter to address in the nonlinear case is the stored energy of the capacitance. Because the stored energy depends only on voltage, the analysis can be performed on a

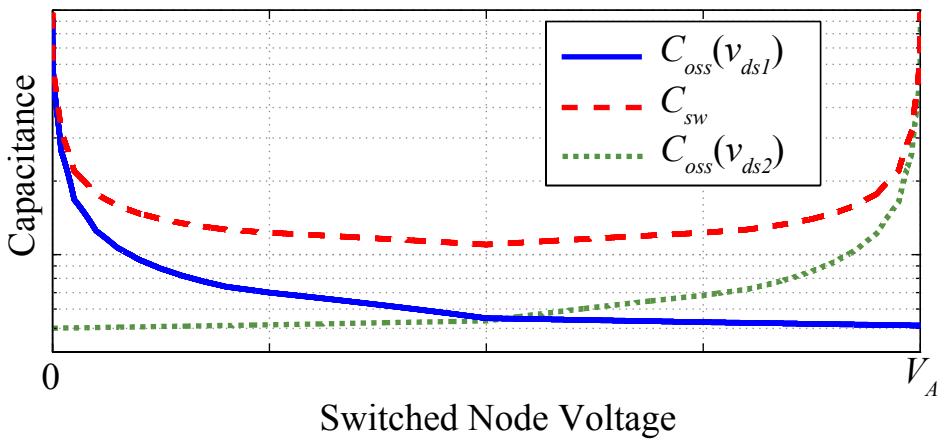


Figure 4.8: Qualitative plot showing the effective capacitance C_{sw} and output capacitance of M_1 versus the switched node voltage.

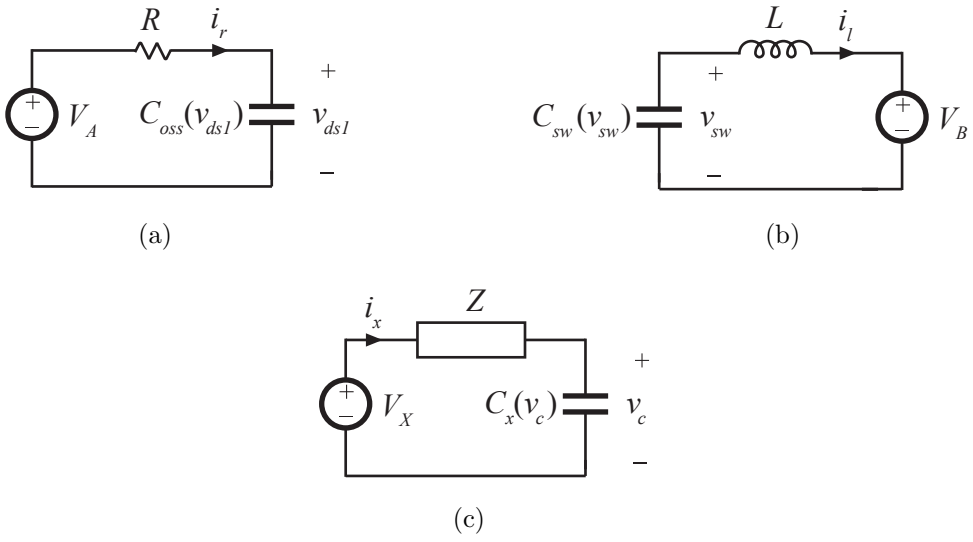


Figure 4.9: Equivalent circuit to Fig. 4.7 during (b) a resonant transition, (a) a hard-switched transition, and (c) the general case.

single capacitor, independent of its application circuit. Using the small-signal definition of $C_x(v_c)$ from (4.5), it has been shown previously that the total energy in a nonlinear capacitor is given by integrating the product of C_x and v_c across the voltage range e.g. from 0 to V_A [22]

$$E_c = \int_0^{V_A} v_c C_x(v_c) dv_c. \tag{4.6}$$

Since the DC bias conditions were removed to obtain C_{sw}, E_c only represents an observable energy if $C_x = C_{oss}$. This energy can then be used to find a linear capacitance value that contains the same amount of energy at V_A by considering the solution to the energy stored in some equivalent capacitor $C_{eq,E}$, which is linear, constant-valued

$$E_c = \frac{1}{2} C_{eq,E} {V_A}^2. \tag{4.7}$$

By combining (4.6) and (4.7) an expression for the energy-equivalent linear capacitor can be obtained

$$C_{eq,E} = \frac{2}{{V_A}^2} \int_0^{V_A} v_c C_x(v_c) dv_c, \tag{4.8}$$

where $C_{eq,E}$ and C_x store the same amount of energy at $v_c = V_A$.

A similar process may be used to find the charge-equivalent linear capacitance,

$$C_{eq,Q} = \frac{1}{V_A} \int_0^{V_A} C_x(v_c) dv_c, \tag{4.9}$$

which will have the same amount of stored charge at V_A as the nonlinear capacitor C_x. As seen from (4.9), this value is simply the average of the C_x curve with respect to voltage, $C_{eq,Q} = \langle C_x \rangle \Big|_{V_A}$.

Next, consider the energy sourced by a supply in charging a nonlinear capacitance. This energy can be solved independently of the series element impedance, and thus the circuit of Fig. 4.9c is used. The total energy supplied, E_s, from V_X is the integral of its instantaneous power over the time taken to charge the capacitance, C_x

$$E_s = \int_t V_X i_x(t) dt, \tag{4.10}$$

where $i_x = i_c$ and therefore the definition from (4.5) can be used to transfer the variable of integration and obtain

$$E_s = \int_0^{V_A} V_X C_x(v_c) dv_c, \tag{4.11}$$

which, given the previous definition of $C_{eq,Q}$, can be reduced to

$$E_s = C_{eq,Q} V_X V_A. \tag{4.12}$$

Comparing to the linear case, it is apparent that the charge-equivalent capacitance is also the correct value to use when solving for supplied energy. This follows intuition, as the power supplied by the constant voltage source should be determined entirely by the charge supplied to C_x. Additionally, combining (4.12) and (4.7), the energy processed by the impedance Z can be found as

$$E_Z = E_s - E_c = \left(C_{eq,Q} \frac{V_A}{V_X} - \frac{1}{2} C_{eq,E} \right) {V_X}^2, \tag{4.13}$$

and an equivalent capacitance $C_{eq,Z}$ can be given for the energy processed by the impedance

$$C_{eq,Z} = 2C_{eq,Q} \frac{V_A}{V_X} - C_{eq,E}. \tag{4.14}$$

This capacitance has slightly different meaning depending on whether Z is inductive or resistive. If a soft-switching transition is considered in the half-bridge circuit of Fig. 4.7, $C_{eq,Z}$ may be used to model the inductor behavior during the switching transition when Z is purely inductive. In this case, both M_1 and M_2 are turned off during the transitions, and the inductor resonates with the output capacitance of both devices, producing the equivalent circuit of Fig. 4.9b. Then, because the inductor current resonates with both devices $C_x = C_{sw}$ is used, and the resulting $C_{eq,Z}$ is a capacitor which results in the same change in stored energy on L during the transition from $V_c = 0$ to $V_c = V_A$. If instead a hard-switching transition is considered, one of M_1 and M_2 turns on with $v_{ds} = V_A$, shorting out its own output capacitance. The opposite device capacitance is then charged through a resistance equal to the on-resistance of a single device. This yields the equivalent circuit of Fig. 4.9a, where Z is resistive, and C_x is the output capacitance of a single device, C_{oss}. In this case, $C_{eq,Z}$ is the linear capacitor which results in the same amount of energy dissipated on the resistance during the voltage transition.

Finally, it desired to develop a time-equivalent capacitor; such a value is useful in determining the dynamics of any resonance between the nonlinear capacitance and an inductance, e.g. as would occur in a zero-voltage switching (ZVS) converter. Such a value is not useful in the hard-switched

case, thus analysis assumes that $Z = j\omega L$, with initial condition $i_x(t=0) = I_{L0}$ in Fig. 4.9c. The time t_{zvs} taken to move voltage v_c from 0 to V_A is fundamentally given through the solution to a system of nonlinear differential equations. For Fig. 4.9c, the two differential equations describing circuit operation are

$$i_x = C_x(v_c)\frac{dv_c}{dt}, \tag{4.15a}$$

$$V_X - v_c = L\frac{di_x}{dt}. \tag{4.15b}$$

These equations can be combined, taking care to remember that C_x is now time-varying, and thus cannot be pulled out of the time derivative. Instead, the chain rule for derivatives is used to obtain

$$LC_x(v_c)\frac{d^2v_c}{dt^2} + L\left(\frac{dv_c}{dt}\right)^2\frac{d}{dv_c}C_x(v_c) + v_c = V_X\ . \tag{4.16}$$

The numerical solution for the ZVS interval duration is then, for the nonlinear circuit

$$t_{ZVS} = \int_0^{V_A} \frac{C_x(v_c)dv_c}{\sqrt{I_{L0}^2 - \frac{2}{L}\int_0^{v_c} C_x(v_y)\,(V_B - v_y)\,dv_y}}\ . \tag{4.17}$$

Which contains nested integrals due to the second-order nature of the circuit. Though complex, this equation may be simply applied to obtain numerical solutions in a program such as Matlab. For example, if `cx` is an array of capacitances with correspondingly indexed voltage array `vx`, and `r` is an array with the indexes into both which correspond to the range $0 < v_c < V_A$, (4.17) can be solved by a single command

```
tzvs = trapz(vx(r),cx(r)./sqrt(Il0^2+2/L*cumtrapz(vx(r),cx(r).*(Vb-vx(r)))));
```

The value of t_{zvs} can then be combined back into the solution of Fig. 4.9b with a time-equivalent linear capacitance $C_{eq,t}$; for the circuit at hand, this solution is given by the integral

$$t_{ZVS} = C_{eq,t}\int_0^{V_A} \frac{dv_c}{\sqrt{I_{L0}^2 - \frac{C_{eq,t}}{L}\left({v_c}^2 - 2V_B v_c\right)}}\ . \tag{4.18}$$

which emits solution

$$\omega_0 t_{zvs,lin} = \cos^{-1}\left(\frac{V_X - V_A}{\sqrt{{I_{L0}}^2{R_0}^2 + (V_{c0} - V_X)^2}}\right) - \tan^{-1}\left(\frac{I_{L0}R_0}{V_{c0} - V_X}\right) \tag{4.19}$$

where ${R_0}^2 = L/C_{eq,t}$ and ${\omega_0}^{-2} = LC_{eq,t}$ are the characteristic impedance and frequency of the resonant elements, and V_{c0} is the initial voltage on the capacitor, in this case $V_{c0} = 0$. By plugging in the value for t_{ZVS} solved previously, a numerical solution for $C_{eq,t}$ can be obtained through iterative analysis.

With these developed linear capacitors, all parameters of interest in a power converter can be solved for. Slight modifications of integral limits and defining functions of C_x are needed to accommodate different circuit configurations or transition types (e.g. partial soft-switching), but the process of solving linear equivalents remains the same. In the following section, simulation results are used to compare the dynamics of the LC circuit of Fig. 4.9b containing a nonlinear device capacitance as well as each of the four linear equivalents developed in this section.

4.2.3 Nonlinear Device Simulation

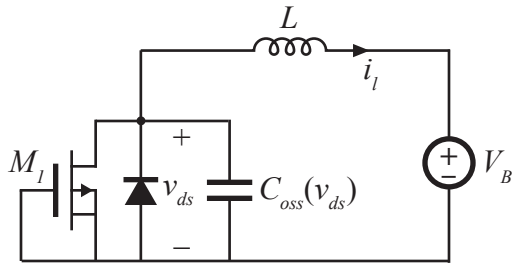


Figure 4.10: Circuit used in Simulink simulations. M_1 is a single FDMC2610 device, $V_B = 200$ V, $L = 12.5$ μH, and $I_{L0} = 0$ A.

To confirm the analysis of the previous section, simulations of circuits containing a nonlinear capacitance are carried out in Simulink. A single FDMC2610 silicon MOSFET is used as an example device with curves for $C_{oss}(v_{ds})$ taken from the datasheet as shown in Fig. 4.3. The circuit simulated is shown in Fig. 4.10. The circuit is allowed to resonate with v_{ds1} starting at an initial voltage of zero volts and resonating until reaching $V_A = 200$ V; for the time-equivalent $C_{eq,t}$, an inductance of $L = 12.5$ μH and initial current $I_{l0} = 0$ A are assumed. In parallel, the four equivalent linear capacitances are simulated under identical conditions. The calculated values for the linear

equivalents of the FDMC2610 devices in this circuit are

$$C_{eq,Q} = 70.5 \text{ pF}, \qquad C_{eq,E} = 56.4 \text{ pF},$$

$$C_{eq,t} = 64.1 \text{ pF} \qquad C_{eq,Z} = 84.5 \text{ pF}.$$

None of these values approach the value for C_{oss} quoted in the datasheet, which is 41 pF nominally at $V_{ds} = 100$ V.

Simulation results are shown in Fig. 4.11. The voltage v_{ds}, current i_l, capacitor energy E_{tot}, and capacitor charge Q_{tot} are shown with respect to time in individual plots, and each circuit is allowed to resonate for precisely the amount of time required to reach $v_{ds} = V_A$. In each plot, a dashed black line shows the correct value of the parameter being plotted, as determined by simulation of the full nonlinear characteristic. There is a clear necessity to choose the appropriate capacitance when solving for a certain aspect of the resonant circuit: $C_{eq,t}$ for resonant time, $C_{eq,Z}$ for final inductor current, $C_{eq,E}$ for energy stored in the capacitor, and $C_{eq,Q}$ for its charge; also, no one value of capacitance is capable of simultaneously modeling all of the characteristics of interest in the circuit.

4.2.4 Application and Experimental Verification

It is desired to use the developed linear-equivalent capacitors to aid in the analysis of the phase-shifted (DAB) converter, whose schematic and typical operating weaveforms are repeated in Fig. 4.12. The previously developed silicon-transistor prototype is used, which consists of FDMC2610 devices on the input side, and operation at 110 W with a 150-to-12 V step-down conversion ratio and matched transformer turns ration $n_t = 0.08$. All devices are switched at $f_s = 1$ MHz to emphasize the impact of resonant intervals. A single bulk capacitance is considered between nodes a and b in Fig. 4.12 which consists of the series/parallel combination of all four nonlinear capacitances on the primary full bridge. During the switching transition, the voltage on this equivalent capacitance is moved from -150 V to $+150$ V. To begin, it is of interest to know the amount of losses incurred if the primary side devices are not zero-voltage switched. For this,

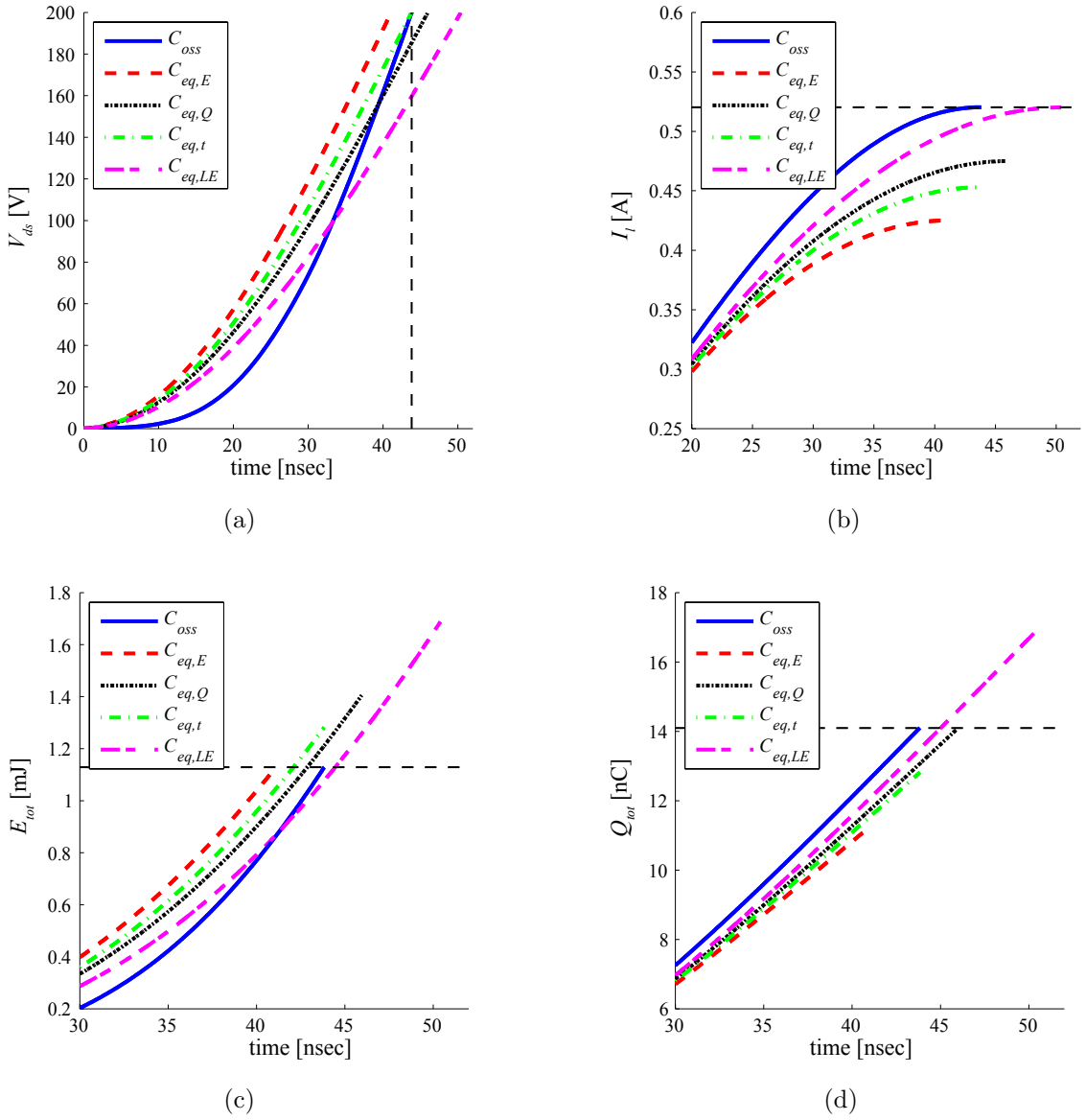
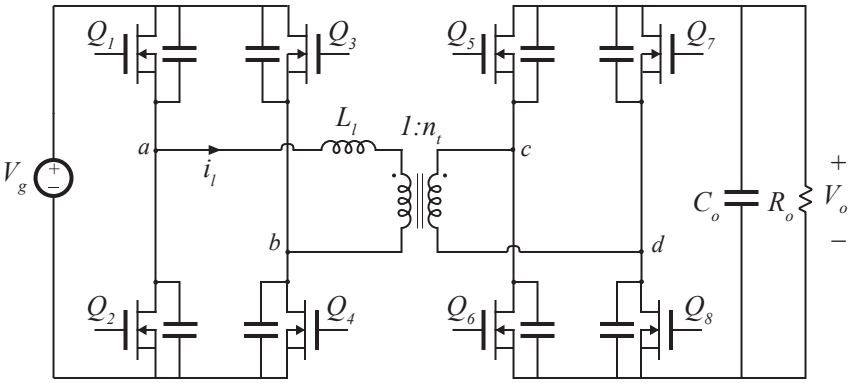
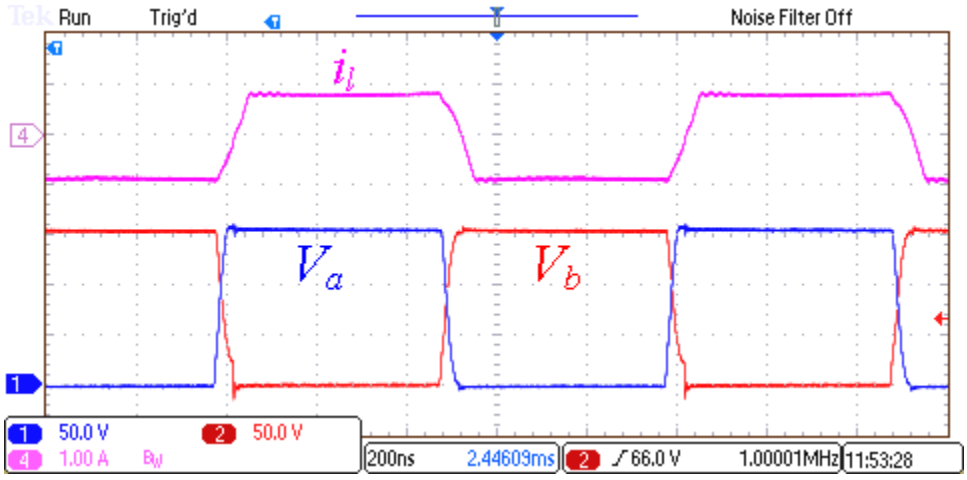


Figure 4.11: Simulations of the circuit of Fig. 4.10 for the nonlinear capacitance, C_{oss} and the four linear equivalents developed here. The dashed black line indicates the correct value of the respective simulation parameter which a linear equivalent should match. In each case, only the single, appropriate linear equivalent leads to a correct approximation i.e. (a) $C_{eq,t}$, (b) $C_{eq,Z}$, (c) $C_{eq,E}$, and (d) $C_{eq,Q}$.



(a)



(b)

Figure 4.12: (a) Schematic of DAB converter and (b) operating waveforms. MOSFET equivalent capacitances, C_{oss} are shown explicitly.

the tank of the circuit is disconnected, and the primary devices are switched separately, with dead times to prevent shoot-through current. The expected losses from hard switching are divided into two categories for each half bridge transition: losses from shorting out device capacitances, and losses from the RC-type charging of the opposite device in each half-bridge. With this in mind, both $C_{eq,E}$ and $C_{eq,Z}$ are calculated for an individual device to obtain the total switching losses; considering all four devices and switching frequency f_s this is

$$P_{loss} = 4\left(\frac{1}{2}C_{eq,E}{V_g}^2 f_s\right) + 4\left(\frac{1}{2}C_{eq,Z}{V_g}^2 f_s\right), \tag{4.20}$$

which can be reduced via (4.14) to

$$P_{loss} = 4C_{eq,Q}{V_g}^2 f_s. \tag{4.21}$$

Next, the ZVS boundary and soft-switching time are evaluated by reducing the output power of the converter until ZVS of primary side devices is achieved just as the inductor current reaches 0 A. From the previous state plane analysis, it is known that the ZVS condition on inductor current I_{pk} at the start of the resonance, and total resonant time t_α, are given in normalized state plane form by

$$J_{pk} > 2, \tag{4.22}$$

$$\alpha = \frac{\pi}{2} - \cos^{-1}\left(\frac{2}{J_{pk}}\right). \tag{4.23}$$

Here one can observe that standard state-plane analysis benefits from the development of linear capacitors i.e. traditional state plane analysis can be used without modification to solve characteristics of circuit operation; one only needs to select the correct linear equivalent capacitor to denormalize the results. Because (4.22) is a condition on inductor energy, $C_{eq,Z}$ is used, while $C_{eq,t}$ is used to denormalize time in (4.23) to obtain:

$$I_{pk} > 2V_g\sqrt{\frac{C_{eq,Z}}{L_l}}, \tag{4.24}$$

$$t_\alpha = \sqrt{L_l C_{eq,t}}\left[\frac{\pi}{2} - \cos^{-1}\left(\frac{2V_g}{I_{pk}}\sqrt{\frac{L_l}{C_{eq,t}}}\right)\right]. \tag{4.25}$$

The linear-equivalent predictions for hard-switching loss, ZVS condition, and resonant time are compared to experimental results in Table 4.1, showing good agreement. Also included as reference are the analytical estimates one would obtain if the same calculations were made using the approximation that C_{oss} is linear, with magnitude equal to that quoted on the datasheet for the device (41 pF at 100 V), and with magnitude taken from the datasheet plot for C_{oss} at V_g. These approximations are shown to be highly inaccurate, indicating a clear need for the use of appropriate linear equivalents.

Table 4.1: Experimental Results for Full Bridge

Parameter	Capacitors Used	Value			
		Analytical	Experimental	Reference 1[†]	Reference 2[‡]
Hard Switched Primary Loss P_{loss}	$C_{eq,Q}$	6.9 W	7.05 W	3.69 W	2.25 W
Minimum ZVS Current I_{pk}	$C_{eq,Z}$	819 mA	850 mA	579 mA	452 mA
Soft-Switched Time t_α	$C_{eq,t}$	40.68 ns	39 ns	16.9 ns	9.7 ns

[†] Values obtained if datasheet listed value for C_{oss} (at 100 V) is used in calculation
[‡] Values obtained if datasheet plot is used to obtain C_{oss} at $V_g = 150$ V

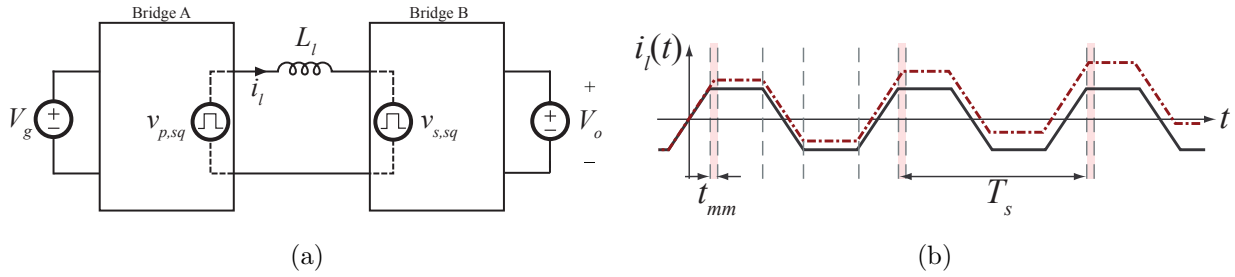
Summary

The direct treatment of nonlinearities in the output capacitance, C_{oss} of switching devices is a daunting task which is often neglected or treated in an inaccurate manner. Because the nature of the resonant switching transitions in the DAB converter are significant in determining converter operation, this significant nonlinearity needs to be addressed with precision in order to accurately determine converter operation. In order to accommodate both accuracy and simplicity of circuit analysis, linear equivalent capacitances to the nonlinear C_{oss} can be used to extract the nonlinear analysis into an algorithmic approach which results in the feasibility of using traditional circuit analysis techniques after linearization. The previously developed state plane analysis, in particular, is well suited to the application of linear equivalent capacitances due to the removal of the value of C_p from the analysis, with its actual value only used when denormalization of resultant parameters takes place. The process results in highly accurate prediction of circuit operation under

both hard-switched and soft-switched operation.

4.3 Inherent Volt-Second Balancing of Tank Magnetics

An additional issue which is exacerbated by the significant, nonlinear ZVS transitions of the DAB converter concerns the details of the voltage waveforms applied to the tank magnetics. In the previous analysis of the DAB, it has been assumed that $v_p(t)$, $v_s(t)$, and $v_l(t)$ were purely AC waveforms, with zero DC component when averaged over a switching period. This assumption stemmed from the nature of steady-state analysis; any DC component of voltage applied to a magnetic would result in a net change in the current through that device over the switching period, and therefore violation of the assumed steady state. In practice, some DC component in applied voltage waveforms can result from any manner of mismatch in the converter, including unmatched parasitics of devices or layout, or slight modulator timing errors. These mismatches can, over time, lead to the saturation of magnetic devices. Figure 4.13a shows a generalized, nonresonant model of the DAB inductor behavior where L_l is driven by two pulsating voltage waveforms. Ideally, the voltage across L_l is AC-only and current i_l has zero DC component. However, even small timing errors t_{mm} in applied voltages can cause an imbalance in per-period volt-seconds applied to L_l, which steadily accumulate as shown in Fig. 4.13b, causing the eventual runaway of inductor current and core saturation, assuming conduction losses are small.



(a) (b)

Figure 4.13: Generalized model of a family of converters with regard to inductor dynamics (a); and (b) comparison between idealized inductor current waveforms with zero modulator error (solid) and the result of a small modulator mismatch t_{mm} (dashed).

To combat this issue, converter implementations have commonly taken one of two design approaches. First, and most common, a series DC blocking capacitor may be introduced in order to block any mismatch in volt-seconds applied [22]. For steady-state converter operation to remain intact, this capacitor must be large enough such that any resonance with magnetic components occurs well below the converter switching frequency. Additionally, a damping circuit may be required to prevent high-Q resonances between the inductor and blocking capacitor, particularly as may occur during converter startup and transient conditions. In a second approach, active control can be implemented either through current-mode control directly [115–120], or through auxiliary control circuits [121, 122]. In any case, circuit operation is impaired through increased component count, size, complexity, and cost. The issue is even more pronounced at high switching frequencies, where even relatively small modulation timing errors represent significant percent-changes in applied volt-seconds. In order to combat this, high resolution modulators can be used, with the added benefit of better tracking of small dead times in the DAB [123]. A simple example of an approach to construction of high resolution, hybrid delay line digital modulator circuitry in low cost FPGAs is detailed in Appendix B. However, any digital modulator will have inherent timing uncertainty equal to at least half of the LSB duration.

In multi-phase synchronous buck converters, it has been observed previously that zero-voltage switched operation with resonant transitions has an inherent effect on volt-second balancing, which can lead to automatic current balancing [124, 125]. The mechanism functions via an inherent feedback mechanism where any DC offset in inductor current results in alteration of ZVS dynamics, which in turn adjust the applied volt-seconds, and is present to some extent in any converter with significant ZVS transitions. This mechanism, though discovered previously, had not been analyzed in significant detail to allow its leverage in converter design prior to the analysis developed here which was first presented in [126]. In the case of the high step-down DAB converter, the significant ZVS transitions can be used to provide passive balancing of applied volt-seconds on all magnetics, allowing converter operation without requiring DC-blocking capacitors or active control and protection.

4.3.1 Volt-Second Balancing Analysis

In the same vein as the analysis of ZVS transitions with nonlinear capacitances, the analysis of the volt-second balancing inherent to resonant transitions is undertaken given the simplified circuit of Fig. 4.14a. This circuit models the equivalent tank behavior of a generalized converter during a zero-voltage transition (ZVT) interval of a single bridge, where C_r represents a linear equivalent to the the effective bridge capacitance during resonance. In the generalized analysis, the voltage V_g held by the non-transitioning bridge may be positive, negative, or zero volts, and the voltage $v_c(t)$ may move between $\pm V_g$ or 0 V. The specific case of $v_c(t)$ transitioning $-V_g \rightarrow V_g$ is shown in the time-domain waveforms of Fig. 4.14b, which models the DAB primary transition when $C_r = C_p$ and $I_0 = I_{pk}$.

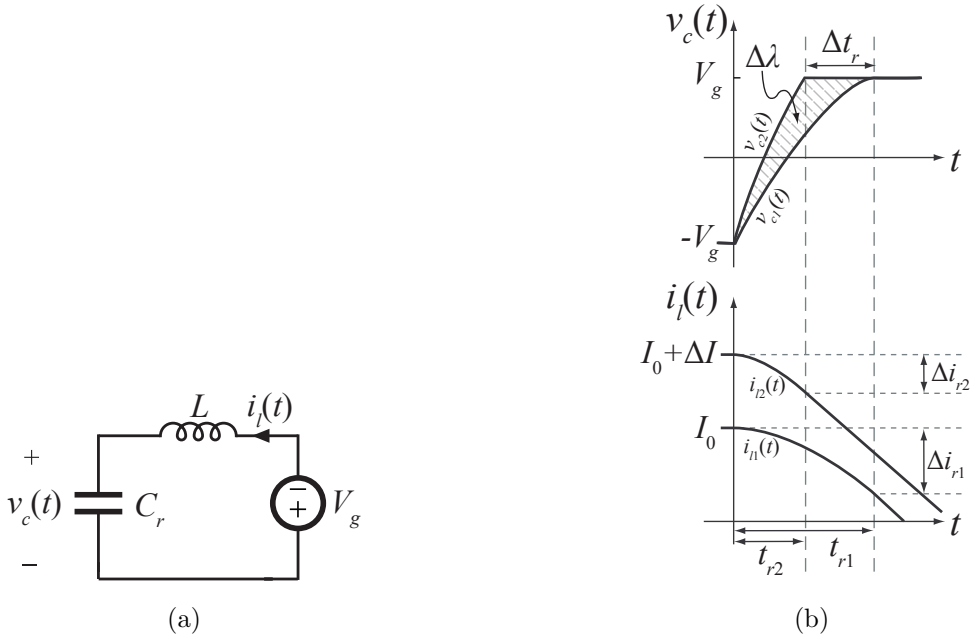


Figure 4.14: (a) Test circuit used to examine volt-second feedback from ZVS transitions; and (b) example waveforms demonstrating the effect.

Analysis is initiated by considering the difference in interval dynamics between two cases: first, the nominal ZVT waveforms $v_{c1}(t)$ and $i_{l1}(t)$ and second, the same transition under the condition of increased initial current I_0 as shown by $v_{c2}(t)$ and $i_{l2}(t)$. The increase ΔI in I_0 can

be considered as the effect of a DC offset in the inductor current due to an applied volt-seconds mismatch t_{mm} from the modulator. The increased current results in a faster ZVT in $v_{c2}(t)$, which gives a net increase $\Delta\lambda$ in volt-seconds applied to the left side of the inductor. This increase in applied volt-seconds will tend, over time, to decrease the inductor current, effectively counteracting the initial offset ΔI. Thus, there is an inherent feedback mechanism in the ZVT wherein inductor current offset results in the application of volt-seconds which tend to counteract this offset. If the converter were assumed to operate in steady-state with only this one ZVT present, and the applied voltage waveforms are AC-only except for the modulator mismatch t_{mm}, the steady-state ΔI value can be determined by equating counteracting volt-seconds $\Delta\lambda$ from the resonant transition with the applied volt-seconds due to modulator error,

$$\Delta\lambda = V_g t_{mm} \ . \tag{4.26}$$

Of primary interest in this study is the relationship between the modulator error t_{mm} and current offset ΔI. Such a relation has multiple applications to circuit design, e.g. defining digital modulator resolution requirements from permissible current offset or selecting circuit elements to bound the current offset for a specific modulator design. From (4.26), this relationship can be approximately obtained by ascertaining the linearized relationship between $\Delta\lambda$ and ΔI near the nominal operating point. In order to do so, the waveforms of Fig. 4.14b are used to solve an expression for $\Delta\lambda$, starting with its definition,

$$\Delta\lambda = \int_0^{t_{r1}} \left(v_{c2}(t) - v_{c1}(t)\right) dt \ , \tag{4.27}$$

which can be separated into three components,

$$\Delta\lambda = \int_0^{t_{r2}} v_{c2}(t)dt + \int_{t_{r2}}^{t_{r1}} V_g dt - \int_0^{t_{r1}} v_{c1}(t)dt \ , \tag{4.28}$$

where the resonant volt seconds of each can be solved using the inductor $i - v$ relationship, for $i = \{1, 2\}$,

$$v_{li}(t) = L\frac{di_{li}}{dt} \ . \tag{4.29}$$

Integrating (4.29) and replacing $v_{li}(t) = V_g - v_{ci}(t)$,

$$\int_0^{t_{ri}} v_{ci}(t)dt - V_g t_{ri} = L\Delta i_{li} \ . \tag{4.30}$$

The change in inductor current Δi_{ri} is given by the energy balance in the circuit during the transition. The total energy supplied by V_g must be equal to the sum of the changes in stored inductor and capacitor energy,

$$\Delta E_{C_r} = \Delta E_{Li} - \int_0^{t_{ri}} i_g V_g dt \ , \tag{4.31}$$

where the energy changes in capacitor and inductor are given by

$$\Delta E_{C_r} = \frac{1}{2} C_r v_{ci}(0)^2 - \frac{1}{2} C_r v_{ci}(t_{ri})^2 \ , \tag{4.32a}$$

$$\Delta E_{Li} = \frac{1}{2} L i_{li}(0)^2 - \frac{1}{2} L i_{li}(t_{ri})^2 \ . \tag{4.32b}$$

Finally, the resonant time is taken from the previous state plane analysis and denormalized to obtain

$$t_{r1} = \frac{1}{\omega_0} \sin^{-1}\left(\frac{2V_g}{R_0 I_0}\right) \ , \tag{4.33}$$

where, again, ${1/\omega_0}^2 = LC_r$ and ${R_0}^2 = L/C_r$. Equations (4.28)-(4.33) are then combined to obtain a closed-form but cumbersome expression (4.34) that relates ΔI and $\Delta\lambda$.

$$\Delta\lambda = \frac{2V_g}{\omega_0}\left(\sin^{-1}\frac{2V_g}{I_0 R_0} - \sin^{-1}\frac{2V_g}{(I_0+\Delta I)\,R_0}\right) + L\Delta I + L\sqrt{I_0^2 - 4\frac{C_r}{L}{V_g}^2} - L\sqrt{(I_0+\Delta I)^2 - 4\frac{C_r}{L}{V_g}^2} \tag{4.34}$$

This expression is then approximated by a first order Taylor-series expansion to obtain

$$\frac{\Delta\lambda}{\Delta I} = L - L\sqrt{1 - \left(\frac{2V_g}{R_0 I_0}\right)^2} \ , \tag{4.35}$$

which is the desired relationship between applied volt-seconds and inductor current offset.

The derivation is slightly different when the capacitor voltage transition moves $0 \rightarrow V_g$ rather than $-V_g \rightarrow V_g$ or when the polarity of the V_g source is reversed. However, all cases can be represented an expression of the form

$$\frac{\Delta\lambda}{\Delta I} = L - L\left(\sqrt{1 - k\left(\frac{\Delta V_c}{R_0 I_0}\right)^2}\right)^k \ , \tag{4.36}$$

where ΔV_c is the change in capacitor voltage required to achieve ZVS and k is an integer whose value is ± 1 depending on the polarity of V_g.

If the circuit being analyzed has multiple ZVT intervals, the volt-second contributions from each can be summed and equated to the total volt-seconds due to modulator error, as given in (4.26). If only the ZVT of Fig. 4.14b is present, (4.35) can be combined with (4.26) to obtain the desired relationship between ΔI and t_{mm}

$$\frac{\Delta I}{t_{mm}} = \frac{{I_0}^2}{4 C_r V_g} \left(1 + \sqrt{1 - \left(\frac{2 V_g}{R_0 I_0} \right)^2} \right) \ . \tag{4.37}$$

It is worth noting here that the expression $2V_g/(R_0 I_0) \leq 1$ is the denomalization of $J_{pk} \geq 2$, the ZVS condition of the circuit, and so the expression in the radical is thus guaranteed positive for the given mode of operation. It follows from (4.37) that

$$\frac{\Delta I}{I_0} < \frac{I_0}{2 C_r V_g} t_{mm} \approx \frac{t_{mm}}{2 t_{r1}} \ , \tag{4.38}$$

i.e. as long as the transition continues to achieve ZVS, the resulting steady-state relative current offset is less than half of the ratio of timing mismatch to resonant transition time, even when only one ZVS transition is considered. This implies that the inherent volt-second balancing can offer a very simple and practical solution to transformer saturation or current balancing issues in ZVS converters, as long as circuit timing mismatches are kept to a fraction of resonant transition intervals.

In the following section, the analysis is applied to two example converter circuits to demonstrate the relationship between per-switching-period modulator error and magnetic component offset current. Application to both the inductor and transformer in the high-step down DAB converter will be presented following this example.

4.3.2 Application of Analysis to Converter Circuits

In order to demonstrate the application of analysis from the previous section to complete circuits, with multiple differing ZVT intervals in a single switching period, the inductively-loaded

full-bridge (ILFB) circuit of Fig. 4.15 is first considered. The ILFB represents a simplification of the DAB converter, where modulation waveforms are altered in order to obtain similar inductor current waveshape, but only a single magnetic device needs to be considered. On its own, this circuit is commonly found as part of larger power converters, and may find use e.g. as a ZVS-assisting circuit. In such applications, however, the circuit has traditionally required additional treatment to prevent inductor saturation, such as the addition of a DC-blocking capacitor in series with L [120]. Operational waveforms of the circuit under simple phase-shift modulation are shown in Fig. 4.16. For nominal operation without modulator error, the converter exhibits two equal phase shift intervals per switching period, $\varphi_1 = \varphi_2$, and four dead time intervals in each of which ZVS is obtained on a single bridge.

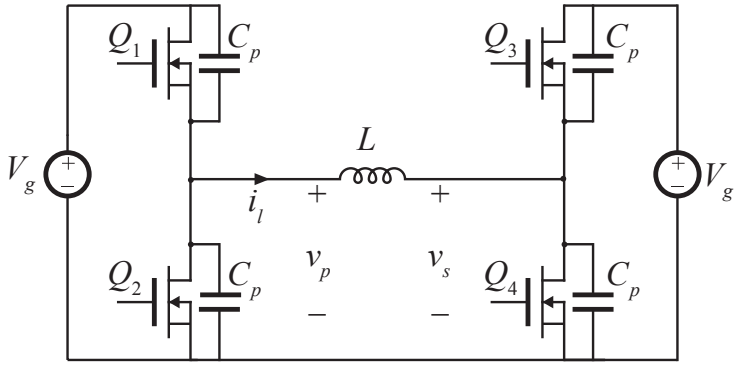


Figure 4.15: Inductively-loaded full-bridge circuit used in analysis. Input and output voltages are equal, and phase-shifted modulation is employed to obtain operational waveforms as given in Fig. 4.16. C_q is the output capacitance of the switching devices.

The previous analysis is applied to the phase-shifted full-bridge by again assuming the presence of an offset in inductor current ΔI as shown in Fig. 4.16a. This current offset then affects each of the four resonant intervals present in converter operation, resulting in four changes in applied volt-seconds $\Delta\lambda_{1-4}$ to the inductor. The effect of each of the four is to decrease the applied volt-seconds to the inductor, either through reduced positive or increased negative voltage applied to the inductor during each dead time interval. Using (4.36), the relation between each λ_i and the overall ΔI can be solved for a given converter configuration, noting that $k = 1$ and $I_0 = I_{pk}$

for $\lambda_{1,3}$, while $k = -1$ and $I_0 = I_{r2}$ for $\lambda_{2,4}$. In all cases, the voltage swing $\Delta V_c = V_g$ and the equivalent capacitance C_r is given by the parallel combination of the high- and low-side MOSFET output capacitance C_p, for which a charge-equivalent linear capacitor is used.

With each $\Delta\lambda$ solved, the analysis is completed by equating the overall change in applied volt-seconds $\sum_{i=1}^{4} \Delta\lambda_i$ to an amount of applied volt-seconds λ_{mm} which result from an error in modulation. The modulation error t_{mm} results in phase shift intervals which are not equal, $\varphi_1 \neq \varphi_2$, as shown in Fig. 4.16b. By equating volt-seconds, the modulator mismatch which exactly balances the change in applied volt-seconds resulting from ΔI can be ascertained, thus solving the amount of modulator mismatch which results in steady-state operation with offset current ΔI. One further simplification can be made by noting that due to the linearization around the nominal operating point, the values solved for $\frac{\Delta\lambda_i}{\Delta I}$ are identical regardless of whether the transition is sped up or slowed down by ΔI. Thus, the values for $\Delta\lambda_1 = \Delta\lambda_3$ and $\Delta\lambda_2 = \Delta\lambda_4$, simplifying the relationship to

$$\Delta I = \frac{V_g t_{mm}}{2 \sum_{i=1}^{2} \frac{\Delta\lambda_i}{\Delta I}} \,. \tag{4.39}$$

Results are compared with simulation and analysis in the following section for the full bridge.

The next circuit considered is the 1:1 phase-shifted DAB converter of Fig. 4.17. Note that a 1:1 turns ratio is used here to facilitate significant ZVS transitions on both primary and secondary windings, where only the primary ZVS transition is significant in the high step-down case. Under phase-shift modulation, the operating waveforms of the DAB converter are very similar to those of the full-bridge converter analyzed previously. As is commonly the case in the converter design, analysis will assume $L_m \gg L_l$, allowing L_l to be equivalently modeled as a primary-side inductance despite being evenly distributed throughout the transformer windings. However, this assumption does not allow the complete neglect of the contribution of the magnetizing inductance to circuit operation when considering the effects of modulator mismatch. Unlike the previous full bridge circuit, both transformer saturation and the runaway of series inductance L_l must be considered.

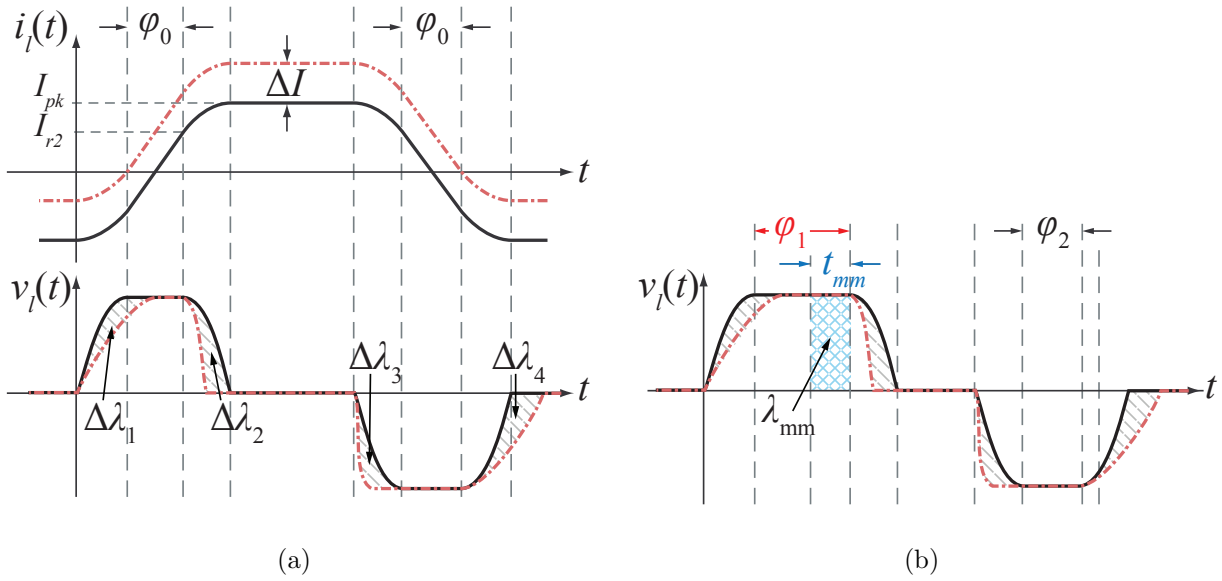


Figure 4.16: (a) Nominal inductor current and voltage waveforms for the phase-shifted full-bridge (solid black) and result of an offset in inductor current (dashed red). The offset ΔI causes changes in four resonant intervals, each resulting in some change in applied inductor volt-seconds $\Delta\lambda_i$. In (b), the modulator mismatch t_{mm} is included, which causes a mismatch in the two phase shift intervals, resulting in mismatched volt-seconds λ_{mm} which are balanced by $\Delta\lambda_i$ with steady-state offset ΔI.

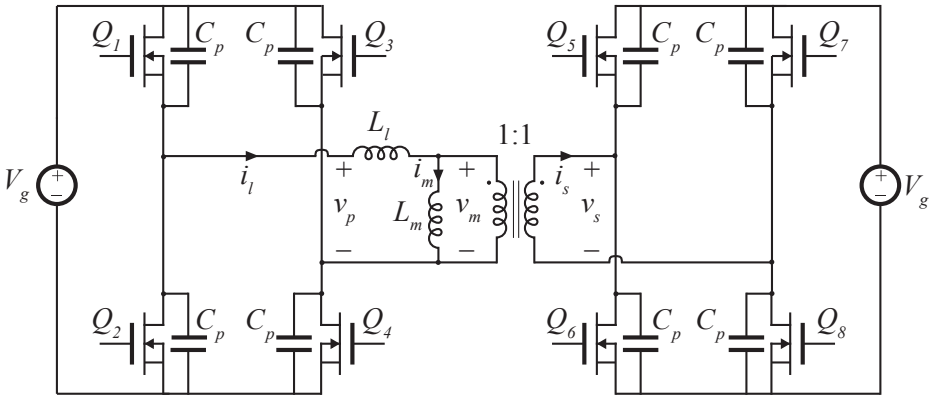


Figure 4.17: Schematic of the 1:1 DAB converter with both L_l and L_m. Primary-referenced Transformer leakage L_l and magnetizing inductance L_m, as well as switching device output capacitance C_q are shown explicitly.

Thus, two types of modulator error may be considered. In the first, mismatch between the phase shift intervals $t_{mm,\varphi}$ results in $\varphi_1 \neq \varphi_2$ and DC volt-seconds applied to L_l. The second type of mismatch, $t_{mm,s}$, results in equal phase shift intervals, $\varphi_1 = \varphi_2$, but nonequal duration of intervals between them, yielding DC volt-seconds applied to the magnetizing inductance. Examples of both types of mismatch and the resulting effect on v_l and v_m are shown in Fig. 4.18, with resonant transitions excluded to simplify the waveforms and emphasize the mismatch present. Note that $v_m(t) = v_s(t)/n_t$ for the tank inductance modeled on the primary only. Analysis for the case of

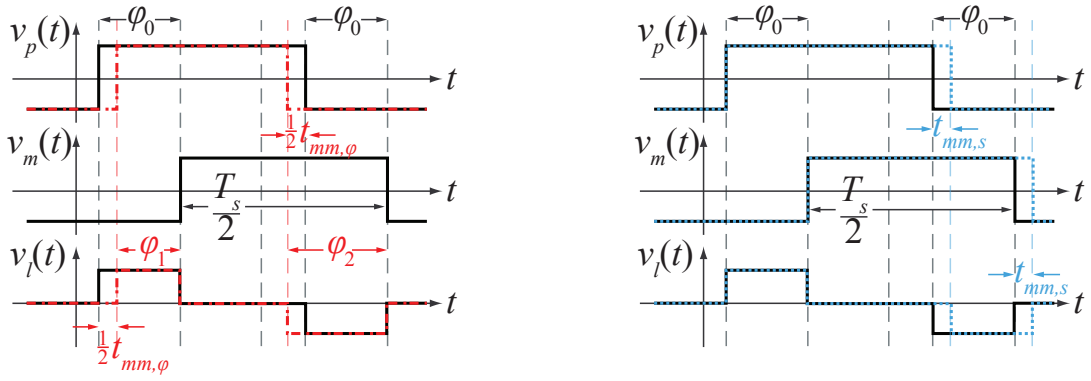


Figure 4.18: Simplified, non-resonant waveforms for voltage of the DAB converter demonstrating the effect of mismatch in nominal phase shift intervals φ_0 (a) and applied switching half-period $T_s/2$ (b). Note that DC volt-seconds are applied to L_l only in (a) and L_m only in (b).

mismatch in phase shift looks identical to analysis associated with Fig. 4.16 for the full bridge circuit, with notable exceptions that the ΔV_c and the voltage applied to the inductor during the mismatch interval are doubled, and C_r is now replaced the linear equivalent to the output capacitance of all four devices.

$$\Delta I = \frac{2V_g t_{mm,\varphi}}{2\sum_{i=1}^{2} \frac{\Delta\lambda_i}{\Delta I}} . \tag{4.40}$$

Interestingly, the analysis is unaltered for the case of magnetizing inductance mismatch. Under the assumption that $L_m \gg L_l$, resonant interval dynamics are dominated by L_l. Then, equations from the previous analysis remain valid for the offset current ΔI, regardless of whether it

is derived from magnetizing or leakage inductance. Waveforms under the assumption of magnetizing current offset are shown in Fig. 4.19. The magnetizing current i_m is expanded for emphasis, but is assumed in actuality to be much smaller than i_l or i_s, and thus only the offset in i_m is considered. It can be seen that an offset ΔI_m in magnetizing current splits evenly between primary and secondary currents, under the assumption that the distributed leakage inductance presents equal impedance on both primary and secondary windings, despite being modeled as primary-only. This again results in four locations in which volt-seconds applied to the inductor are altered, $\Delta\lambda_{1-4}$. However, comparing to Fig. 4.16, it is apparent that the polarity, though not the nature, of $\Delta\lambda_2$ and $\Delta\lambda_4$ have reversed, resulting in cancellation which maintains zero DC voltage component on the series inductance. The voltage on the magnetizing inductance, however, does have a DC component.

For the case where L_l is modeled on the primary side, the voltage on the magnetizing inductance is equal to v_s, which now has only two periods of altered volt-seconds $\Delta\lambda_{mi}$ per switching period, as shown in Fig. 4.19. In a similar manner, the volt-seconds from these two intervals are summed, then equated to a value λ_{mm} which represents volt-second error introduced by the modulator, as shown in Fig. 4.19b,

$$\Delta I_m = \frac{2V_g t_{mm,s}}{\sum_{i=1}^{2} \frac{\Delta\lambda_{mi}}{\frac{\Delta I_m}{2}}}, \tag{4.41}$$

where $\Delta I_m = 2\Delta I_s = |2\Delta I_l|$ and thus, equations for transformer (4.41) and inductor (4.40) result in identical expressions for the magnitude of current offset observed at i_l or i_s.

4.3.3 Simulation and Experimental Results

In order to test the analysis presented in the previous section, both the phase-shifted full bridge and 1:1 dual-active bridge circuits of Fig. 4.15 and Fig. 4.17 were constructed. In both, $V_g = 50$ V and the switching frequency $f_s = 1$ MHz in order to emphasize the impact of resonant transitions. Each device is implemented as a single MOSFET, Fairchild FDMC2610, in parallel with DFLS1200 diode, which together exhibit an effective output capacitance C_p near 150 pF. A

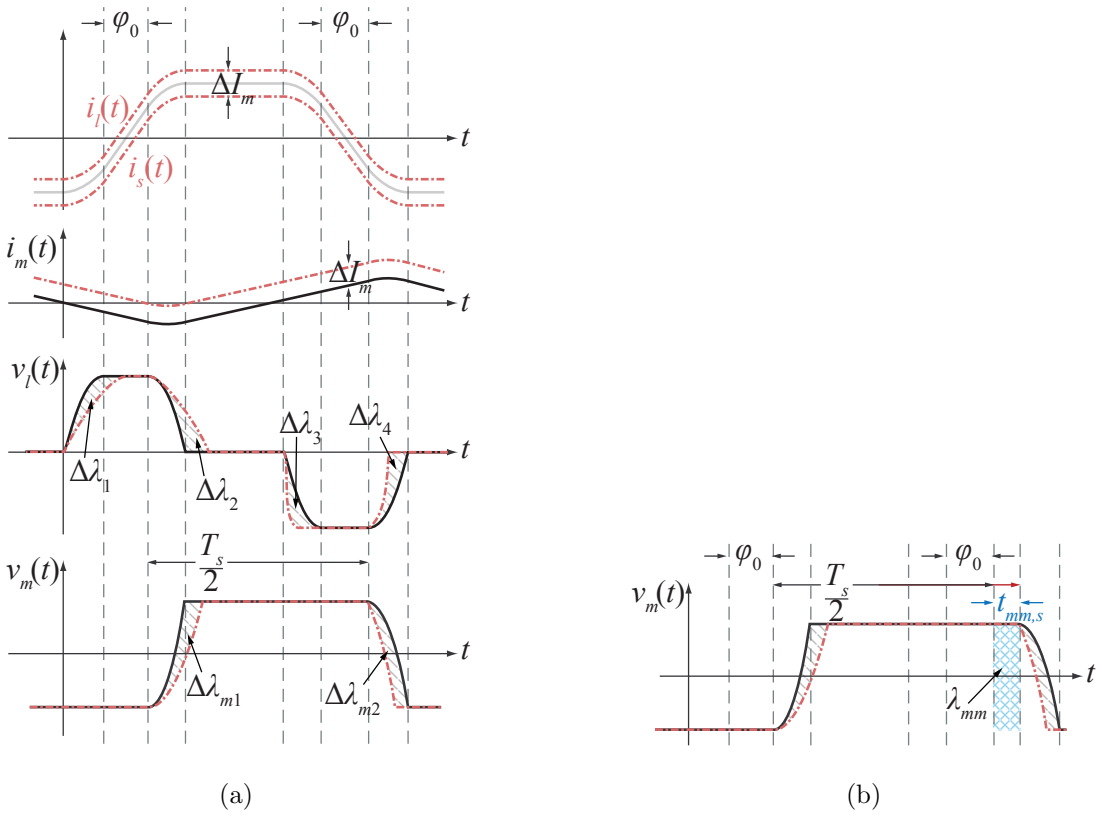


Figure 4.19: (a) Nominal inductor current and voltage waveforms for the phase-shifted DAB (solid black) and result of an offset in magnetizing current (dashed red). The offset ΔI_m causes changes in four resonant intervals each resulting in some change in applied inductor volt-seconds $\Delta\lambda_i$ and transformer volt-seconds $\Delta\lambda_{mi}$. In (b), modulator mismatch t_{mm} is included, which results in mismatched volt-seconds λ_{mm} applied to L_m

transformer with unity turns ratio is constructed and is found to exhibit a magnetizing inductance of $L_m = 1$ mH, with transformer-incorporated leakage inductance $L_l = 30$ μH chosen to obtain significant resonant transitions. In the case of the full bridge circuit, the transformer secondary is shorted and leakage inductance L_l is used as the loading inductance L. Circuit components and parameters are summarized in Table 4.2 and Table 4.3, respectively.

Table 4.2: 1:1 DAB Prototype Circuit Components

MOSFETs	FDMC2610
Diodes	DFLS1200
Transformer Core	0R44916TC
Transformer Turns Ratio	20:20

Table 4.3: 1:1 DAB Prototype Circuit Parameters

C_q	L_l	L_m	V_g	f_s	$r_{DS_{(on)}}$
150 pF	30 μH	1 mH	50 V	1 MHz	200 mΩ

Modulation signals are supplied by a Xilinx Virtex 4 FPGA, using a simplified hybrid delay line architecture based on [127, 128] and detailed in Appendix B to achieve 30 ps resolution with excellent linearity. This high resolution modulator is then used to model the behavior of a low-cost, low-resolution digital modulator by intentionally introducing mismatch in applied phase shift or switching period. For the purposes of converter design, this mismatch may be taken as representative of resolution limits in a low-cost commercial modulator. An introduced timing mismatch of magnitude t_{mm} corresponds to a worst-case offset error of less than ± 1 LSB in a monotonic modulator of resolution $1/t_{mm}$. Thus, given permissible bounds on inductor and/or transformer current offsets for a given mode of operation, the modulator resolution required to maintain that offset can be determined. Similarly, for a given modulator resolution presenting a possible mismatch up to 1 LSB, the circuit can be designed to maintain current offset within specified limits by altering the duration of the ZVS interval, either by increasing effective ZVS capacitance C_p or inductance L_l.

To demonstrate the presence of the phenomena described here, oscilloscope waveforms are

provided in Fig. 4.20-4.23 for various operating points of the demonstration circuits. In all cases, applied mismatch is purposefully tested to much greater values than would be present with an adequately-designed modulator. In Fig. 4.20, inductor current and voltage waveforms in the inductively-loaded full bridge circuit of Fig. 4.15 are shown for both nominal operation with zero modulator mismatch, and for a timing mismatch of 30 ns applied to both φ_1 and φ_2. This corresponds to an error of greater than 50% in the two phase shift intervals, yet corresponds to only a 25% offset in inductor current (relative to nominal peak value) due to the inherent volt-second balancing of the resonant transitions, a zoomed view of which is shown in Fig. 4.21 for the same operating point.

For comparison, the circuit is operated with the resonant dead time interval reduced to a minimum value to force hard switching of devices. A non-zero deadtime is maintained, however, to prevent destructive shoot-through currents in the bridge legs. In this case, mismatched volt-seconds applied by the modulator can no longer be adequately balanced through ZVT intervals. Instead, converter losses associated with increased RMS currents eventually balance the applied volt-seconds at a much larger current offset. Fig. 4.22 shows the same 25% offset in inductor current is obtained with just a 5 ns timing mismatch when the full-bridge circuit is hard switched. With an identical 40 ns offset in the hard-switched case, the current offset is measured experimentally as 850 mA, or a nearly 400% offset relative to nominal peak current.

Waveforms of the DAB converter are shown in Fig. 4.23 for offset applied to both the leakage inductance a and magnetizing inductance b. As predicted by the analysis of the previous section, the magnitude of the current offset measured from i_l is the same in both cases.

The relation between applied timing mismatch and inductor current offset is given over a full range of values in Fig. 4.24 for the full bridge and Fig. 4.25 for the 1:1 DAB. In these plots, experimental data is compared with the predictions from the analysis of the previous sections, as well as simulations of the circuit constructed in Simulink. Simulations use large-signal, switching, state-space models as developed in [129] which consider only losses due to MOSFET on resistance $r_{DS_{(on)}}$ and any losses due to the hard-switching of C_q. In all cases, excellent agreement is achieved.

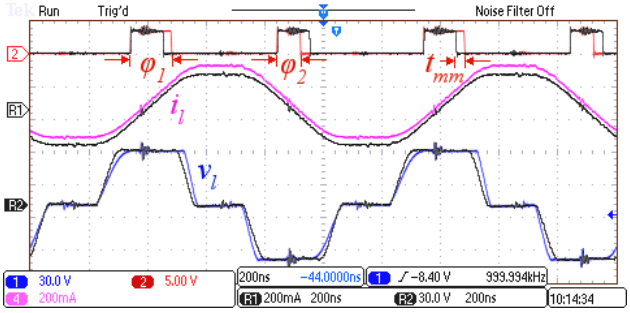


Figure 4.20: Experimental waveforms of the inductively-loaded full bridge circuit of Fig. 4.15. Black (Reference) waveforms show nominal circuit operation with zero mismatch in modulator waveforms at an operating point with I_{pk}=215mA. Colored waveforms show operation with a 30 ns offset applied to both phase shift intervals.

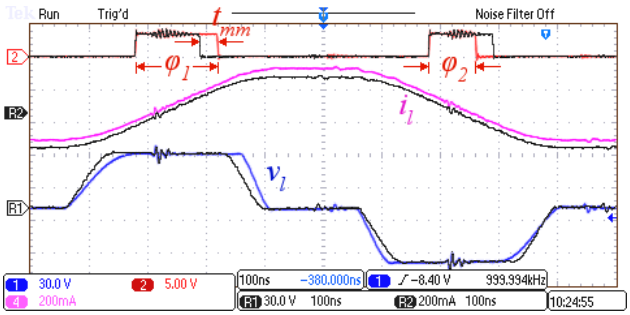


Figure 4.21: Zoomed in waveforms of the inductively-loaded full bridge circuit operating as in Fig. 4.20.

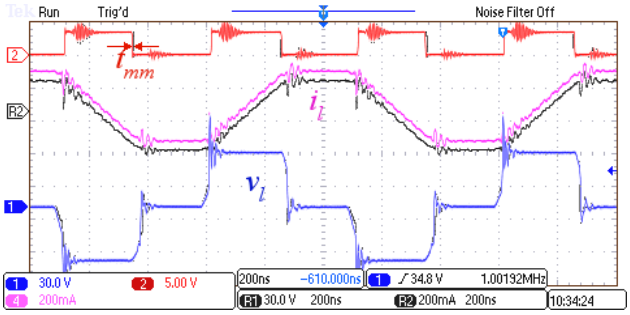
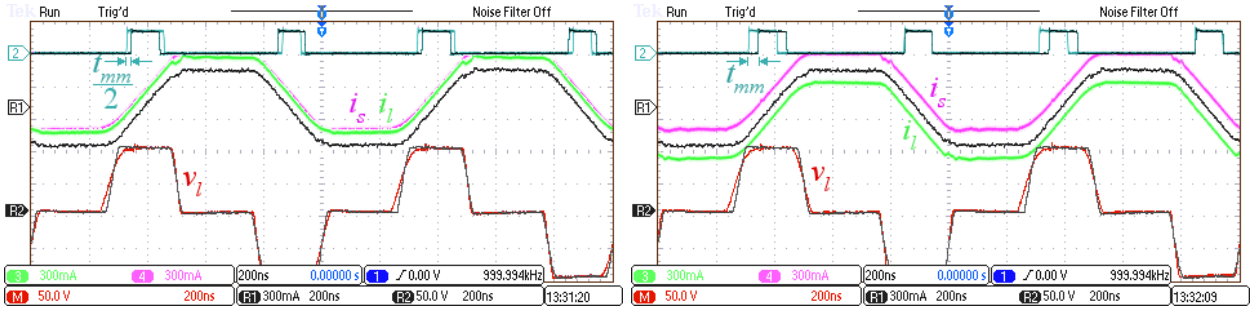


Figure 4.22: Experimental waveforms of the inductively-loaded full bridge circuit with resonant dead time intervals reduced to a minimum. The applied phase shift mismatch is now only 4 ns, but results in the same inductor current offset as was obtained in Fig. 4.20 due to the lack of inherent volt-second balancing abilities of significant ZVT intervals.



(a) (b)

Figure 4.23: Experimental waveforms of DAB converter of Fig. 4.17 with modulation mismatch applied to (a) leakage inductance L_l, and (b) magnetizing inductance L_m. Black (Reference) waveforms show nominal circuit operation with zero mismatch in modulator waveforms at an operating point with I_{pk}=350mA. Colored waveforms show operation with a 30 ns offset applied to (a) both phase shift intervals or (b) split between each half-period

Due to the linearized nature of the analysis, results will become increasingly inaccurate as timing mismatch becomes very large. However, practical applications of the analysis are only concerned with small mismatch and offset values, around which the linearization remains an accurate predictor of circuit behavior.

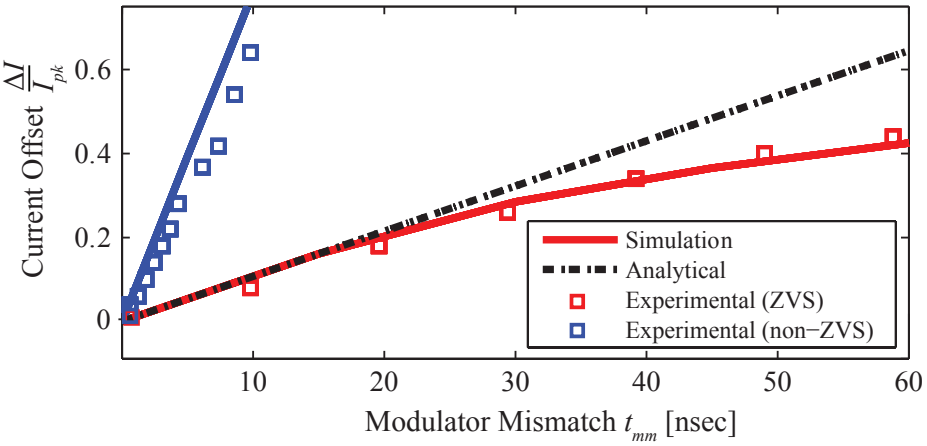


Figure 4.24: Comparison between experimental, simulation, and analytical results for the relation between modulator mismatch in phase shift and inductor current offset in the inductively-loaded full bridge circuit of Fig. 4.15. Experimental and simulation results are shown for both the nominal operation with ZVS and for the case where resonant dead times are set to a minimum to force hard-switching.

4.3.4 Application to High Step-Down DAB

In general, without considering the analysis presented here, modulator resolution in a PWM converter is selected in order to obtain good resolution of PWM signals relative to the switching frequency of the converter. The frequency of a digital modulator is therefore often chosen to obtain some number of discrete timesteps N_{res} within a switching period, e.g. a 100 MHz modulator may be used to obtain $N_{res} = 1,000$ timesteps in a 100 kHz converter. Assuming again that a worst case of 1 LSB error is present in any monotonic digital modulator implementation, and applying the simplified expression of (4.38) for operation well above ZVS, the balancing capabilities of one

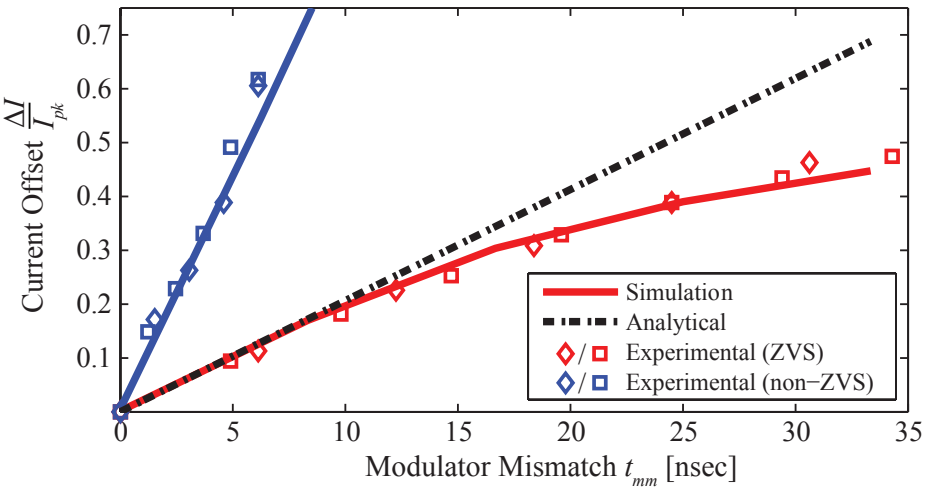


Figure 4.25: Comparison between experimental, simulation, and analytical results for the relation between modulator mismatch and inductor current offset in the 1:1 DAB converter of Fig. 4.17. Experimental and simulation results are shown for both the nominal operation with ZVS and for the case where resonant dead times are set to a minimum to force hard-switching. Further, experimental results are shown both for the case where mismatch volt-seconds are applied to L_l (squares) and to L_m (diamonds).

ZVS transition in a general converter are given by

$$\frac{\Delta I}{I_{pk}} \lessapprox \frac{1}{2N_{res}} \left(\frac{T_s}{t_{r1}} \right) . \tag{4.42}$$

Thus, the relative DC offset of inductor current to peak current value is proportional to the ratio of switching period to the resonant deadtime. This approximation is useful, as it informs the necessity of including an alternate method of preventing transformer saturation in previous analyses of the DAB converter. As shown previously in Fig. 3.1, prior applications of the DAB converter have focused on high power and low switching frequency. Together, these two characteristics result in small t_{r1} and large T_s, and therefore give a potentially large relative current offset. In these cases, the inherent volt-second balancing abilities of the ZVS transitions are not adequate to maintain low inductor current offset because the resonant transitions occupy a very small percent of the overall switching period. In contrast, in the high frequency, low power, high step-down DAB that is proposed in this work, the primary ZVS transition duration is very significant, resulting in significant balancing capability of these transitions. This makes it feasible to operate the DAB without additional circuitry or control techniques to prevent saturation of magnetics, including operation without a DC blocking capacitor. All results presented in this thesis for the DAB converter are taken without any additional DC blocking capacitance.

One potential issue is the relative insignificance of the ZVS transitions on the secondary side in the high step-down DAB converter. Further, the secondary side transition dynamics may be dominated by the parasitic inductances L_D as shown previously, which invalidates the analysis presented here for the secondary-applied volt-seconds, though the primary transitions remain well-modeled by this analysis. If the magnetics are truly implemented as shown in the circuit diagram of Fig. 4.17, with the tank inductance implemented entirely on the primary, this would result in the secondary voltage applied directly to the transformer winding and poor ability for the circuit to natively balance applied transformer volt-seconds due to the relatively insignificant secondary resonant transitions. However, the real implementation of the transformer results in a distributed leakage inductance which will include some component on the secondary buffering the transformer

from having the secondary voltage applied directly to it. Further, this presents some motivation for implementing any discrete tank inductance on the secondary. As long as there is some inductance on the secondary of the transformer, both the effective tank inductance and transformer magnetizing inductance can have their applied volt-seconds balanced dominantly by the significant primary transitions, despite the relatively insignificant secondary transitions. In the worst-case scenario, if zero contribution is made from secondary transitions, the inherent balancing ability of the circuit is simply half of that offered in the 1:1 DAB case when implemented with the same devices. With this conservative approximation, the analytical and simulated results for the 150-to-12 V DAB converter that was implemented in Chapter 3 with all silicon devices are compared in Fig. 4.26. Because the

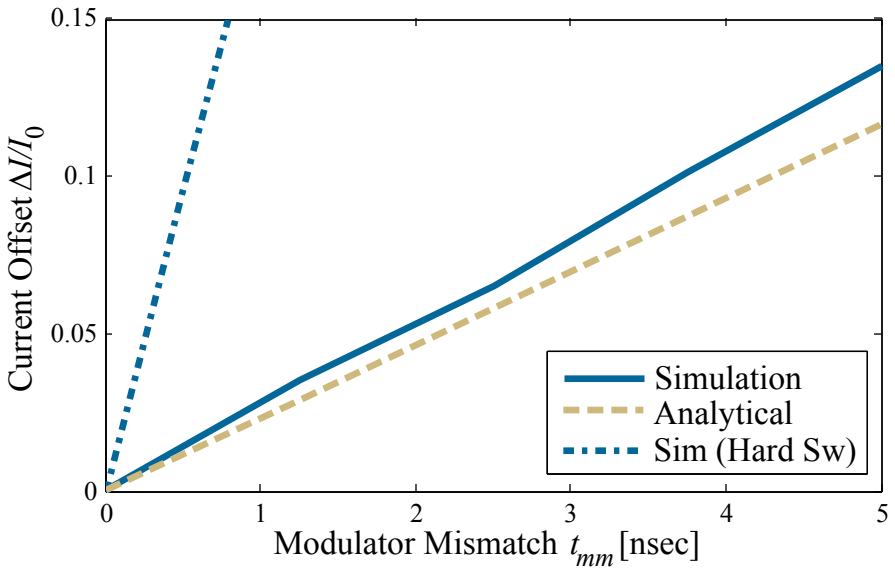


Figure 4.26: Comparison between simulated and analytically solved results for the relation between modulator mismatch and inductor current offset in the 100 W, 150-to-12 V, 1 MHz DAB converter with all silicon devices.

high resolution, low-cost hybrid digital PWM modulator of Appendix B is used, $t_{mm} < 100$ ps in the prototype DAB converter, which even in this worst-case scenario results in less than 2% current offset for operation near 100 W.

Summary

Small mismatches in applied inductor volt-seconds may arise in power converters as a result of asymmetries in circuit modulation. Left unchecked, these mismatch volt-seconds accumulate over multiple switching periods, causing the eventual runaway of inductor currents, which may significantly impact circuit operation through increased loss, saturation of magnetic components, or loss of regulation. Significant effort has been expended in both active control and passive circuit design to prevent DC volt-seconds from being applied to magnetic components in the presence of nonideal modulation waveforms. This paper presents analysis of the inherent inductor volt-second balancing abilities of ZVS circuits in response to modulator timing mismatch. Through linearized analysis of the phenomena, a simple analytical formula which relates modulator mismatch to inductor current offset has been developed. The analysis is confirmed through simulation and experimental results using two prototype circuits comprised of an inductively loaded full-bridge and a dual active bridge (DAB) converter. Excellent agreement is obtained in both cases.

Because of the significant portion of the switching period devoted to the primary resonant transition in the high frequency, high step-down, low power DAB, this inherent feedback between ZVS interval dynamics and applied volt-seconds on magnetic devices makes it feasible to operate the converter without additional circuitry or control to prevent their saturation. As long as a modulator is used which obtains sufficient resolution to accurately track the nominal timing waveforms of the converter, the circuit will natively operate with low offset in inductor currents, and prevent undue accumulation of DC volt-seconds which may cause decreased circuit performance.

Chapter 5

DAB Operation over a Wide Power Range

Until this point, operation of the DAB converter has been considered at a single operating point. Converter design was formulated in Chapter 3 to maximize efficiency at the single designed operating point in which $P_{out} = P_{min}$ and $V_{out} = n_t V_g$, forcing the converter to operate on the boundary of primary ZVS with minimum RMS currents. However, the data center application discussed in Chapter 1 is not well suited to a converter which only operates at a single power, as computational loads in the average data center vary widely and rapidly. Thus, provisions must be made to ensure that the DAB converter is capable of operating across a wide range of output power levels. Beyond this capability, the converter should be able to continue to accomplish all design goals even in the presence of varying output power levels, including the maintenance of high efficiency (or low loss) and exhibition of stable, well-behaved voltages. Recall, however, that strict regulation of the DAB converter output voltage is not required due to the presence of downstream POL and VRM converters, a fact which will be leveraged in the steady-state control design presented in this chapter. Following this, the dynamics and control implementation of the proposed DAB operation techniques will be analyzed in Chapter 6.

One of the most simple and straightforward approaches to extending converter operation to a wide range of output powers is to simply use the converter phase shift interval duration as control input to the converter and make no changes to modulation schemes or control techniques. Beginning at the designed operating point, increasing the phase shift between primary and secondary full bridge will result in increased inductor peak currents, and increased current flow to the output

of the converter; a decrease in phase shift will similarly result in a reduction in output current. If a control loop is implemented which matches the phase shift to the load power requirements, this phase shift modulation can effectively regulate the converter power flow. The issue with this approach concerns the efficiency and stability of the converter at these alternate operating points. When the converter operates at powers above the designed ZVS boundary P_{min}, ZVS will be maintained. However, as soon as operation is incurred at power levels below P_{min}, ZVS will be lost. Hard switching of the high voltage primary devices not only results in significant energy loss and efficiency penalties, but common-mode feedback of the high dv/dt that results on the input bridges has the potential to result in shoot-through currents and, in the worst-case, failures of switching devices.

To prevent hard-switched operation, P_{min} may be reduced by increasing the tank inductance L_l. However increasing L_l results in a greater phase shift interval duration at a given power level, and therefore higher RMS currents and conduction losses in the converter. Because the optimization of converter design was undertaken with the specific goal of optimizing the efficiency at P_{min}, the magnitude of the efficiency penalty for operating above this power are not taken into account and may be significant. Further limiting, larger L_l will result in a reduced range of achievable power levels. This is most simply demonstrated using the linear, nonresonant analysis. By combining equations (2.20) and (2.19) the output current of the DAB converter can be approximated as

$$I_{out} = \frac{V_g t_\varphi}{n_t L_l}\left(1 - \frac{2t_\varphi}{T_s}\right) , \tag{5.1}$$

which has maximum with respect to phase shift occurring at $t_\varphi = T_s/4$. For phase shifts beyond one quarter of the switching period, the inductor current approaches a triangular wave which, although having higher peak value, will result in lower average output current than the ideal squarewave-shaped current. Plugging this in, an expression for the maximum converter output power is obtained, for $V_{out} = n_t V_g$, which is an overestimate due to the linear approximation neglecting resonant intervals

$$P_{out,max} < \frac{{V_g}^2 T_s}{8L_l} . \tag{5.2}$$

For 400-to-12 V conversion at $f_s = 1$ MHz, this results in $P_{out,max} < 20000/L_l$, with P_{out} in watts and L_l in μH. Combining this concept with the linear approximation to P_{min} given in (2.43), the resulting plot of Fig. 5.1 is created, wherein the range over which the DAB converter can operate with ZVS is shown as a function of L_l, for phase shift modulation techniques only and 400-to-12 V conversion at $f_s = 1$ MHz. This plot is constructed with $C_p = 100$ pF; P_{min} is a strong function of C_p, and the span of the ZVS region can be increased if lower-capacitance devices can be used to implement all primary transistors. Increasing the size of the tank inductance L_l, in addition to

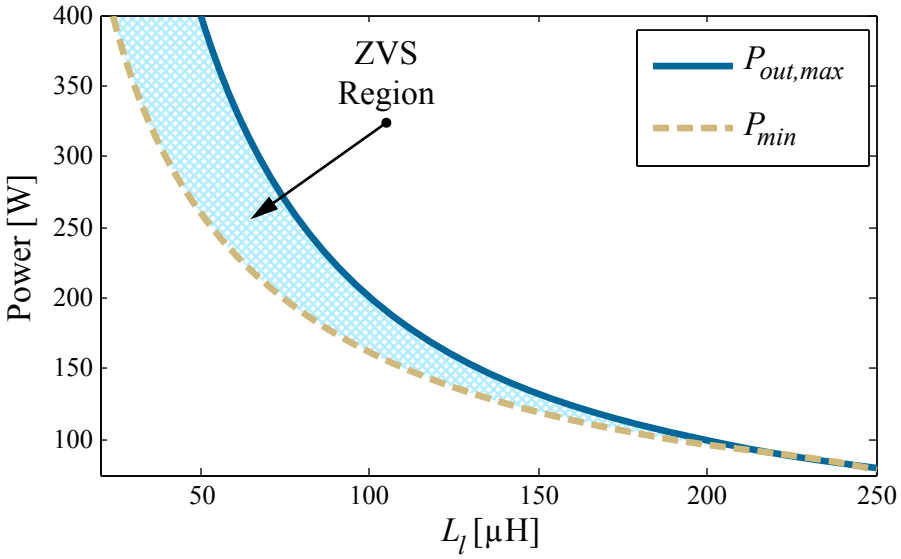


Figure 5.1: ZVS region of the 400-to-12 V, $f_s = 1$ MHz DAB converter, with $C_p = 100$ pF, as defined by the linear approximations to the minimum ZVS power and maximum achievable power with phase shift modulation techniques.

the aforementioned tradeoffs with ZVS minimum power and conduction losses, narrows the region over which the converter can operate with ZVS of primary devices.

It remains possible to use simple phase shift modulation to control the DAB converter if, in the application circuit, the nature of the converter load allows two conditions to be met:

- A power P_{min} can be set such that the load power never reduces below this value
- The variation between P_{min} and $P_{out,max}$ is sufficiently small so that it can be spanned by

the converter's ZVS region.

In order to determine whether or not such an approach is feasible, the nature of the load variations in the data center application need to be examined.

5.1 Load variation in the Data Center

Average computer processor (CPU) use data collected from 5,000 Google servers during a six month period is shown in Fig. 5.2. Though the details of this plot are specific to the subset of servers included in the study [7], the shape of the curve is representative of the behavior of a common server CPU in a data center, where the processor spends very little time under heavy load, but spends a majority of time in the 15-50% load range, or with nearly zero load. This behavior is almost a polar opposite to the DAB converter characteristics mentioned, where proper operation can only be obtained between P_{min} and $P_{out,max}$. This CPU utilization profile is normal and is in fact desirable

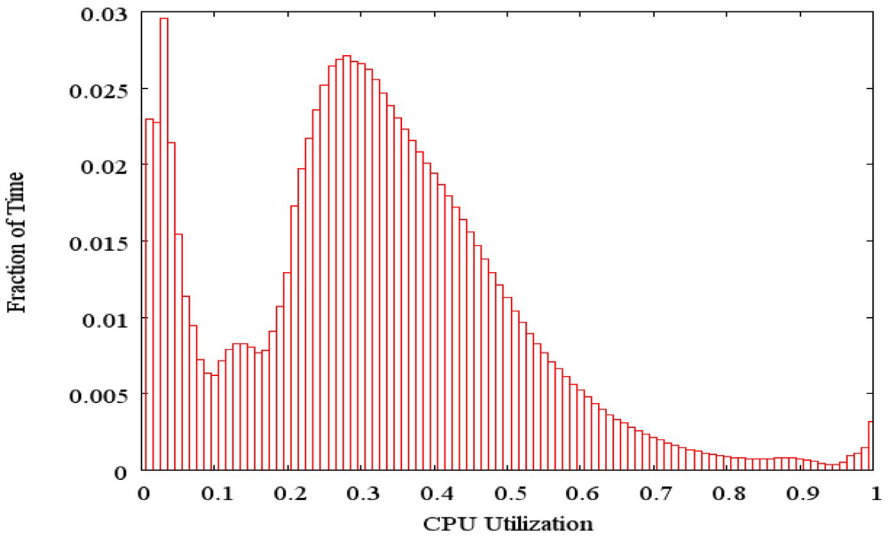


Figure 5.2: Activity profile of a sample of 5,000 Google servers over a period of 6 months. Taken from [7]

for a number of reasons which extend beyond the analysis of power conversion efficiency. Large scale data centers often purposefully distribute computational loads evenly across a large number of servers rather than forcing very high utilization of a small number of CPUs. This practice results

in favorable characteristics in areas such as facility-wide thermal management, resiliency and fault tolerance of data storage, complexity of workload dispatch algorithms, and server responsiveness and latency of computation [7]. It is possible, and in some cases fairly simple, to facilitate high efficiency power conversion by redesigning data center operations so that individual CPUs are preferentially run with close to zero or full utilization. However, it is important to understand that the optimization of data center operation is a multidisciplinary and multiobjective operation; in general, computational performance and data integrity are paramount to system efficiency.

The emphasis on performance metrics of the data center computation have an additional effect on power consumption which is not readily apparent in Fig. 5.2. To ensure that servers which are not currently in use are ready and available to respond immediately to changes in workload, even CPUs which are operating with zero utilization are generally not operating at zero power. With zero instantaneous workload, processors will be kept in an "active idle" state rather than shutting down. This keeps the computational hardware running and ready to respond without the need to reboot when workload increases with associated penalties in latency. This practice results in significant penalties in terms of power loss, as a processor may consume more than 30% of its peak power (at 100% utilization) when in active idle mode (at 0% utilization). Fig. 5.3 quantifies power consumed and its ratio with computational output in an example server at various levels of utilizaiton. In this scenario, even at 0% utilization, the server consumes over 60% of peak power.

In addition to the poor scaling of processor power consumption with utilization, the power consumed by non-CPU hardware on the server is often nearly independent of computational load, as demonstrated in Fig. 5.4. Even with significant reduction in CPU power consumption, there is only minor reduction in the power consumed by DRAM, and almost no reduction in power consumed by the hard disk and auxiliary computational circuitry on the server motherboard. The reduction in power consumption between full utilization and server idle is greater than 250% for the server CPU, but nearly 100% for DRAM, 30% for hard disks, and just 20% for networking switches.

In contrast to the practice of distributing computational load across multiple servers, this poor energy-proportionality of computation in servers is well suited to facilitating efficient power

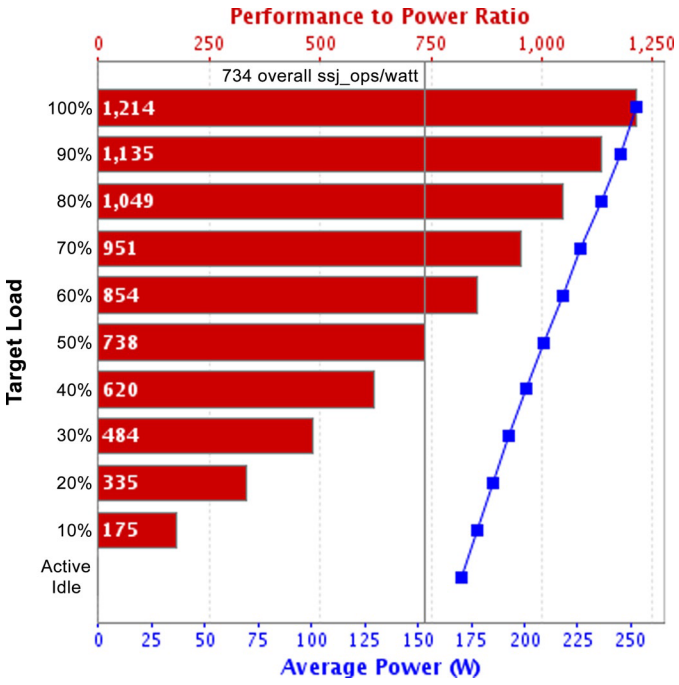


Figure 5.3: Computational energy efficiency (bars) and power consumption (squares) for a single-chip 2.83 GHz quad-core Intel Xeon processor, 4 GB of DRAM, and one 7.2 kRPM, 3.5" SATA disk drive. The processor was running SPECpower_ssj2008, an industry standard benchmarking tool. Taken from [7]

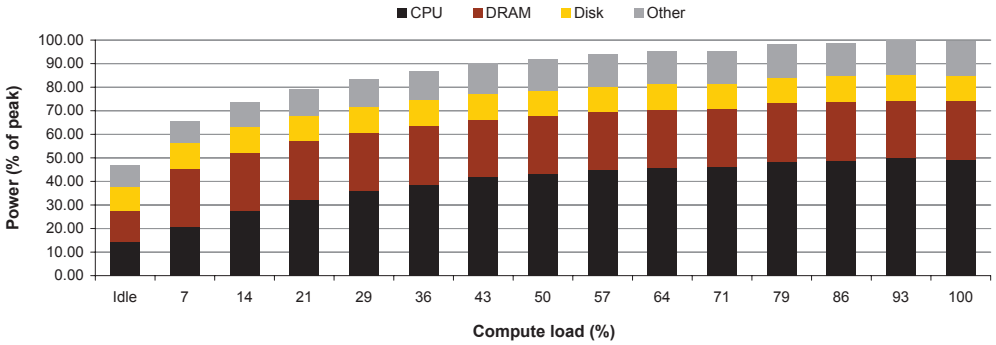


Figure 5.4: Component power consumption in an example x86 server from a recent Google installation as a function of CPU utilization. Taken from [7]

conversion. In fact, examining Fig. 5.4, it seems feasible to design an DAB converter to supply power to the server which was tested using only the general phase shift modulation techniques to control power flow. As long as a suitable combination of device output capacitance and tank inductance can be found to accomplish it, the DAB can be implemented with P_{out_max} placed somewhere above 100% of peak power and P_{min} placed at or below 46% of peak power. For the given server power profile, this arrangement will allow the operation of the DAB converter with ZVS maintained from full load to active idle continuously, feasibly covering all possible power levels which may be incurred during server operation.

However, similar to the practice of distributing computational load across multiple servers, the energy proportionality of computational hardware is an area which is subject to optimization from multidisciplinary approaches, and is an area which is constantly progressing. Server hardware design is increasingly progressing toward a goal of "energy proportional computing", in which the power consumed by server hardware scales directly with the intensity of computations performed with a near equivalence in the percent of peak computational load and the percent of peak power consumption. Progress towards this goal is being made continuously, with devices currently available in mobile and embedded markets which far outperform standard server hardware in energy proportionality [7]. Recent consumer processors require computer power supplies to maintain integrity of the 12 V supply at current loads as low as 50 mA to support power-efficient processor sleep states. With progress continually being made in this field, it is clear that a DAB converter design approach which relies on load power always exceeding some large P_{min} is not an appropriately robust and effective method of constructing the data center power supply architecture. Instead, efforts must be made to alter converter operation so that high efficiency, performance, and stability of operation can be maintained at output powers ranging from zero to full rated load. In order to do this, the unregulated nature of the converter will be taken into account in the converter analysis, with the output voltage used as a variable to tune the efficiency of the converter over the output power range. In the ensuing analysis and application of this practice, it is shown that with a small variation in output voltage it is feasible to maintain favorable operation of the DAB converter over

the full load range while maintaining very simple steady state control [130, 131].

5.2 DAB Operation with Varying Output Voltage and Power

Previous studies have shown methods for offline efficiency optimization of the DAB converter that are able to set wide ZVS range while maintaining low RMS currents through all devices [30,84]. Additionally, online efficiency improvements have been proposed which alter switch control schemes in order to extend the ZVS range and improve light load efficiency [55–58, 132]. In these methods, multiple switch modulation schemes are used across varying load conditions, resulting in improved efficiency at the expense of increased control complexity. Because of the unique characteristics of the bus converter present as the front end converter in the data center, it is feasible to operate the DAB in an unregulated converter; in this work the term "unregulated" refers to the output voltage not being controlled to follow a fixed reference but instead being adjusted in closed loop for the purpose of improving efficiency. This method of converter control in the steady-state results in an output voltage which is not constant, but is nevertheless well controlled. The value to which the output voltage is driven is determined by the output power level of the converter, with the optimal $V_{out} - P_{out}$ "trajectory" determined by careful loss analysis of the converter.

In order to determine the optimal efficiency trajectory, the state plane analysis of Chapter 3 must be extended to include converter operation at the full range of output power levels and with $V_{out} \neq n_t V_g$, as was the case in the previous analysis. As the output power and voltage are varied in the phase-shifted DAB converter, multiple operating modes arise. Boundaries between operating modes are determined by the relative magnitudes of phase shift and dead time intervals, and the ZVS boundaries of both primary and secondary-side devices.

Continuing from the single-point analysis results, the secondary dead time interval will be assumed to have negligible effect on converter operating waveforms and will be neglected in the state plane analysis of the converter in each operating mode. It does, however, have significant effect on converter efficiency and will therefore be included in the loss analysis.

5.2.1 Analysis of DAB Operating Modes

The analysis of Chapter 3 was completed under the condition that output power is precisely large enough to achieve ZVS of all devices, $P_{out} = P_{min}$, and $V_{out} = n_t V_g$; i.e. the conversion ratio is equal to the transformer turns ratio. A new solution is developed for the more general case of $V_{out} = n_{ctrl} V_g$, where n_{ctrl} is the converter conversion ratio, and is not necessarily equal to the transformer turns ratio n_t. For simplicity, a variable M_N is defined as the conversion ratio normalized by transformer turns ratio,

$$M_N = \frac{V_{out}}{n_t V_g} \ . \tag{5.3}$$

Important waveforms of converter operation under operating steady-state conditions sufficient to provide ZVS of all devices are shown in Fig. 5.5 for the case where $V_{out} < n_t V_g \mapsto M_N < 1$. This reduction in output voltage from the case previously modeled results in key changes to converter waveforms. Most notably, the inductor current is no longer flat during the ζ subinterval (subintervals IV and VIII), as it was in the $M_N = 1$ case shown previously in Fig. 2.20. When $V_{out} \neq n_t V_g$, the difference between input and reflected output voltages is applied across the inductor during this subinterval, $v_{l,\zeta} = V_g - V_{out}/n_t$ is applied across the inductor. This ramping of inductor current causes increased RMS currents for a given average power level; Fig. 5.5 shows that there is significant increase in peak input current $i_g(t)$ above its average value I_g. This characteristic of converter operation has been depicted as undesirable in previous analysis. However, a second characteristic must be noted that stems from the increase in reactive power: the operating current I_{pk} which is present in the inductor just prior to the start of the primary resonant interval α is increased. This allows more energy to be available to obtain ZVS of the high voltage primary devices without increasing the output power, and is the feature which will be leveraged to extend the converter ZVS range. Thus, the variation in output voltage again leads to an optimization of converter efficiency which must consider a tradeoff between switching losses on the primary side devices if I_{pk} is not large enough to obtain ZVS and the conduction losses which result from elevated I_{pk} values.

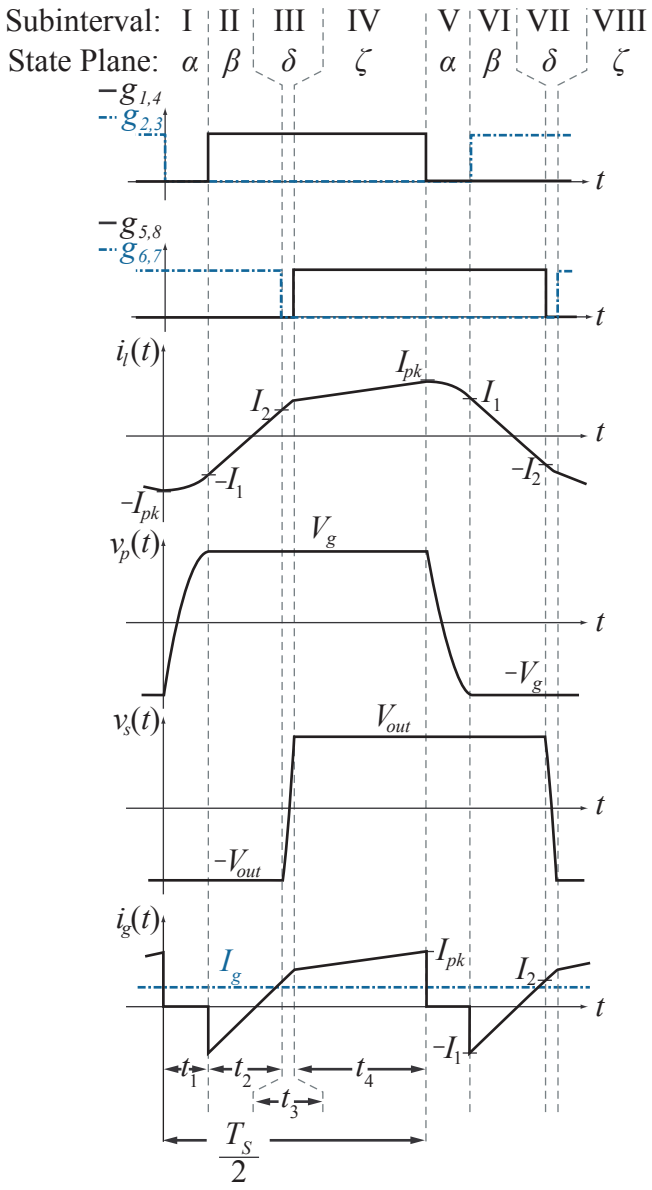


Figure 5.5: Operational waveforms of DAB for the case where $V_{out} < n_t V_g \Leftrightarrow M_N < 1$ and the converter operates in Mode 1. Subinterval names, time domain durations, and corresponding state plane conduction angles are labeled.

5.2.1.1 Mode 1: Operation with $\beta > 0$ and primary ZVS

In Mode 1, the phase shift subinterval has duration $\beta > 0$, and the value of I_{pk} is sufficient to obtain ZVS of primary devices. Because the secondary dead time interval δ is not considered, Mode 1 encompasses operating points with both hard and soft switching of secondary devices. Under the assumption of $\delta \approx 0$, the primary state plane and relevant time domain waveforms in Mode 1 are shown in Fig. 5.6

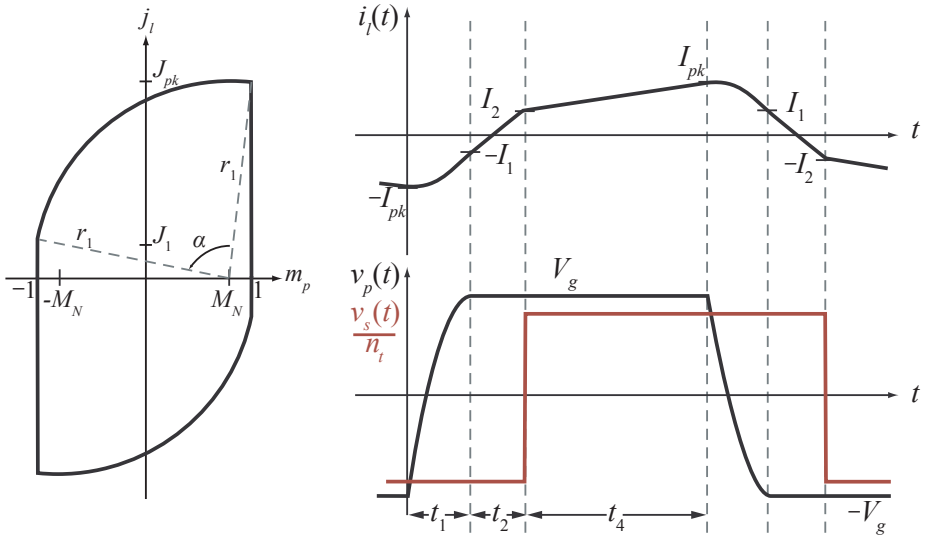


Figure 5.6: Operating waveforms of the DAB converter in Mode 1 as both normalized state plane (a) and corresponding time-domain waveforms (b).

The state plane is solved using geometric arguments to find the average output current. First, the radii r_1 are related to give the value of J_1

$$J_1 = \sqrt{J_p k^2 - 4M_N} \ . \tag{5.4}$$

Then, using the law of cosines, the conduction angle of the primary resonance is given by

$$\alpha = \cos^{-1}\left(1 - \frac{(J_p k - J_1)^2 + 4}{2J_p k^2 + 2\left(1 - M_n\right)^2}\right) \ . \tag{5.5}$$

The conduction angles for the β and ζ intervals are found in the same manner previously for β.

Due to the linear nature of these intervals, the time domain plots are used to obtain

$$t_2 = L_l \frac{I_1 + I_2}{V_g + \frac{V_{out}}{n_t}} \ , \tag{5.6a}$$

$$t_4 = L_l \frac{I_{pk} - I_2}{V_g - \frac{V_{out}}{n_t}} \ , \tag{5.6b}$$

which are normalized to give

$$\beta = \frac{J_1 + J_2}{1 + M_N} \ , \tag{5.7a}$$

$$\zeta = \frac{J_p k - J_2}{1 - M_N} \ . \tag{5.7b}$$

The switching period is $T_s = 2(t_\alpha + t_\beta + t_\zeta)$ which, when normalized, remains the same as in the simplified case previosuly

$$\frac{\pi}{F} = \alpha + \beta + \delta \ , \tag{5.8}$$

with $F = f_s/f_0$. Finally, the averaged output current is solved in the same manner as presented in Section 3.3.2.2 – applying charge balance to the output capacitor and integrating the charge transferred to the output in each interval. This yields the final equation which gives the normalized average value of the output current

$$J_{out} = \frac{F}{n_t \pi} \left(2 + \frac{J_p k + J_2}{2} \zeta + \frac{J_1 - J_2}{2} \beta \right) \ . \tag{5.9}$$

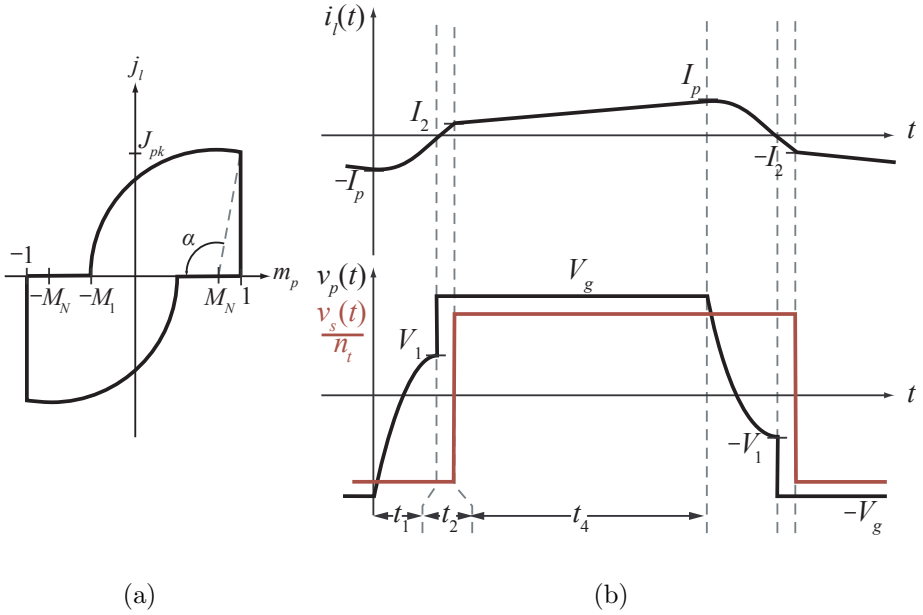
5.2.1.2 Mode 2: Operation with $\beta > 0$ and hard-switched primary

As output power decreases or output voltage increases, the current I_{pk} available to obtain ZVS of primary devices decreases accordingly. Eventually, the energy store in the inductor will be insufficient to obtain ZVS of primary devices, and hard switching will begin to occur on the primary devices. From the state plane diagram of Fig. 5.6, it can be seen that this boundary occurs when $J_p k$ becomes so small that $r_1 < 1 + M_N$, resulting in a ZVS condition of operating mode 1

$$J_{pk} > \sqrt{4 M_N} \ . \tag{5.10}$$

which simplifies to the familiar $J_{pk} > 2$ for $M_N = 1$. Below this boundary, the inductor current is reduced to zero before full ZVS can be achieved. If the primary devices are then switched directly

at $i_l = 0$ to obtain minimal switching loss, the state plane of operation becomes modified as shown in Fig. 5.7. A new variable M_1 is defined, where $(1 - M_1)$ is the normalized voltage remaining on v_p just before devices Q_1 and Q_4 are turned on. Thus, for $M_1 = 1$, soft-switching is obtained, and the converter operates at the boundary of this operating mode and Mode 1. Since $J_1 = 0$, $J_2 \geq 0$ in this mode, soft-switching is obtained on all secondary devices. Note that, although similar, this



(a) (b)

Figure 5.7: State plane and time-domain waveforms of the DAB converter in Mode 2, with hard switched primary devices. Because $M_1 < 1$, stored energy in L_l is insufficient to achieve primary ZVS.

type of hard switching is different from the active hard-switching analyzed in Section 3.5. In the previous analysis, hard switching was enforced through decreasing t_1 below the value required to obtain ZVS, and hard switching devices at a point where $i_l \neq 0$ and energy remains in the inductor. In Mode 2, hard switching is not actively enforced, but is unavoidable due to insufficient energy available to obtain ZVS.

To solve the converter operation, note that $J_1 = 0$ always, by definition. M_1 is then found by examining the triangle formed between r_1 and the m_p axis as

$$M_1 = \sqrt{{J_{pk}}^2 + (1 - M_N)^2} - M_N \ . \tag{5.11}$$

Equations (5.7a), (5.7b), and (5.8) are unchanged, and the equations for α and J become

$$\alpha = \cos^{-1}\left(1 - \frac{{J_{pk}}^2 + (1+M_1)^2}{2\left(M_1 - M_N\right)^2}\right) \ , \tag{5.12}$$

$$J_{out} = \frac{F}{n_t \pi}\left(1 + M_1 + \frac{J_{pk} + J_2}{2}\zeta - \frac{J_2}{2}\beta\right) \ . \tag{5.13}$$

5.2.1.3 Mode 3: Operation with $\beta < 0$ and soft-switched primary

In Mode 3, the secondary devices are hard-switched during the dead time of the primary devices, resulting in two distinct resonant intervals whose combined effect is to achieve ZVS on the primary side devices. Because β is defined as the time interval between the end of the primary dead time and beginning of secondary dead time, the converter can operate with $\beta < 0 \mapsto t_2 < 0$ and still remain in positive power flow operation so long as the total phase shift $\Phi_{ab} = t_1 + t_2 + t_3 > 0$ remains true.

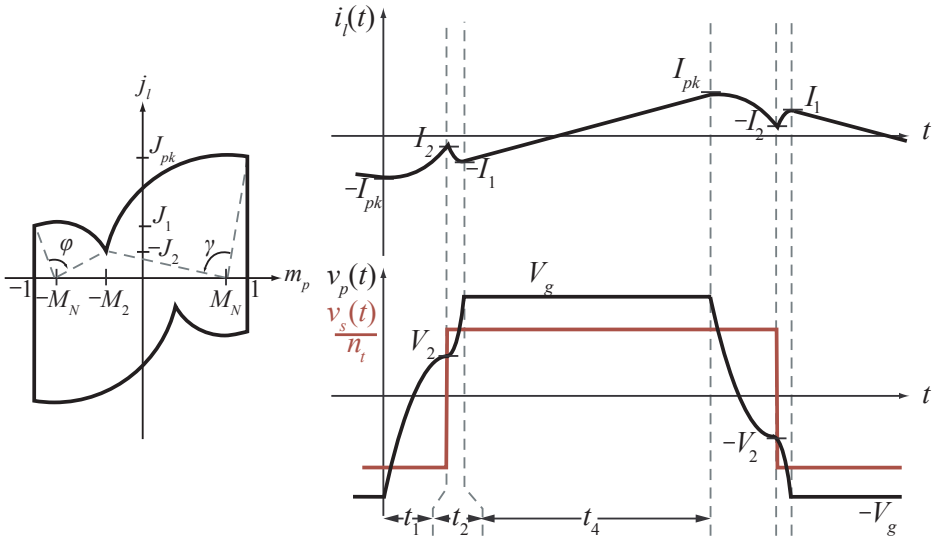
The state plane diagram for this mode of operation is shown in Fig. 5.8. To match boundary conditions with other operating modes, two new angles are defined as

$$\gamma = \alpha + \beta \ , \tag{5.14a}$$

$$\phi = -\beta \ . \tag{5.14b}$$

Additionally, the value $(1 - M_2)$ is the normalized absolute value of the voltage v_p when the secondary side is switched. Switching the secondary during the primary resonant interval inverts v_s, altering the DC voltage biasing the resonant circuit formed by L_l and C_p, as shown by the altered center of resonance in Fig. 5.8. Therefore, the secondary full bridge is commutated with previously conducting devices still having positive drain-to-source currents, causing hard-switching of secondary devices; this results in an output current which is now negative for a significant portion of the switching period. The resulting circulating current can allow sufficient energy to be available for soft-switching primary devices below normal ZVS boundaries, even at low values of P_{out}

The converter solution as shown takes the form of a set of coupled equations derived from



(a) (b)

Figure 5.8: State plane and time-domain waveforms of the DAB converter in Mode 3 under $\beta < 0$ conditions. Because $J_2 < 0$, the converter loses secondary ZVS.

the conduction angles

$$\gamma = \cos^{-1}\left(1 - \frac{(J_{pk} + J_2)^2 + (1 + M_2)^2}{2(1 - M_n)^2 + 2{J_{pk}}^2}\right) , \tag{5.15a}$$

$$\phi = \cos^{-1}\left(1 - \frac{(J_1 + J_2)^2 + (1 - M_2)^2}{2(M_n - M_2)^2 + 2{J_2}^2}\right) , \tag{5.15b}$$

and from the two radii

$${J_2}^2 = (1 - M_N)^2 + {J_{pk}}^2 - (M_2 + M_N)^2 , \tag{5.15c}$$

$${J_1}^2 = -(1 - M_N)^2 + {J_2}^2 + (M_N - M_2)^2 . \tag{5.15d}$$

The equation for the ζ interval is slightly modified due to I_2 occurring before I_1 to get

$$\zeta = \frac{J_{pk} + J_1}{1 - M_N} . \tag{5.16}$$

Because $\beta < 0$, the normalized switching period equation becomes

$$\frac{\pi}{F} = \gamma + \phi + \zeta = \alpha + \zeta . \tag{5.17}$$

Finally, the averaging of the output current yields

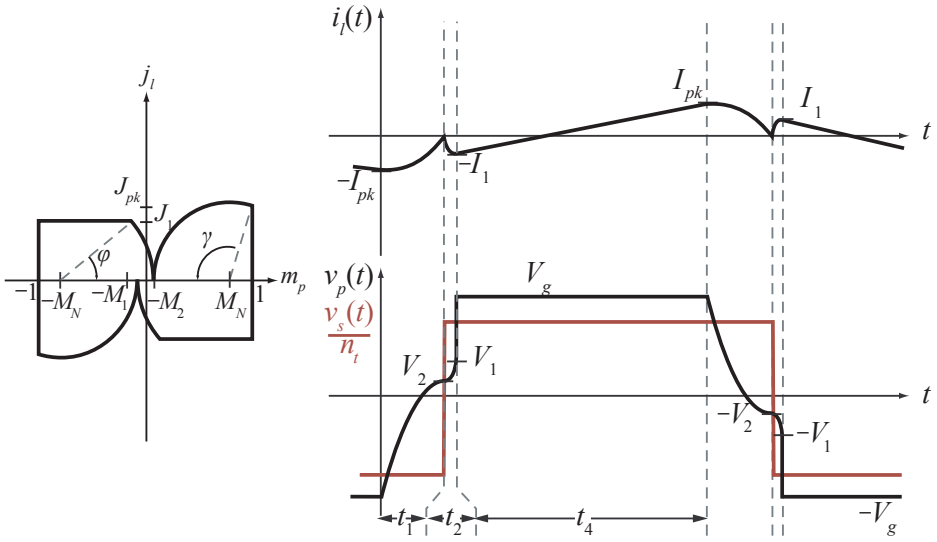
$$J_{out} = \frac{F}{n_t \pi}\left(2M_2 + \frac{J_{pk} - J_1}{2}\zeta\right) . \tag{5.18}$$

5.2.1.4 Mode 4: Operation with $\beta < 0$ and All Devices Hard Switched

The final operating mode necessary to define converter operation consists of the area bounded by the $J_2 = 0$ boundary of Mode 2 and the $J_2 = 0$ boundary of Mode 3. The converter is solved by setting $J_2 = 0$ for the entire region and again introducing the variable M_1, at which point all primary transistors are switched with associated energy loss. By its nature, this region consists of some hard switching on all devices. The state plane diagram for this mode of operation is shown in Fig. 5.9.

The converter solution in Mode 4 follows closely that of Mode 3 with $J_2 = 0$ and notable exceptions occuring only in the equations for ϕ and J_{out}

$$\phi = \cos^{-1}\left(1 - \frac{{J_1}^2 + (M_1 - M_2)^2}{2(M_n - M_2)^2}\right) , \tag{5.19}$$



(a) (b)

Figure 5.9: State plane and time-domain waveforms of the DAB converter under $\beta < 0$ conditions, with all devices hard switched.

$$J = \frac{\langle i_o \rangle}{I_{base}} = \frac{F}{n_t \pi} \left(2M_2 + 1 - M_1 + \frac{J_{pk} - J_1}{2} \zeta \right) \ . \tag{5.20}$$

Further operating modes beyond the four detailed here are possible, but are not included in this analysis due to their necessary exhibition of either decreased efficiency (e.g. in the active hard switching case) or increased modulator complexity.

5.2.2 Converter Loss Modeling

In order to ascertain a trajectory for adjusting V_{out}, as well as for selecting optimal dead times, the previously developed loss model is extended to converter operation in any one of the four operating modes. The majority of the loss calculations remain unaltered from the previous analysis in Sections 3.6.1, 3.5.2, and 3.4.3, though solutions to converter operating parameters have changed. Switching loss of primary devices was addressed for actively hard switched operation in Section 3.5. For the current analysis, switching loss due to the output capacitance of the high voltage devices occurs only in Modes 2 and 4, and consists at each switching transition of two devices turning on with a voltage $V_g \left(1 - M_1\right)/2$ across them, and two devices being forcedly charged in a non-resonant manner from $V_g \left(1 + M_1\right)/2$ to V_g. Taking into account the nonlinearity of device capacitances, this results in a primary switching loss of

$$P_{sw,p} = 4 f_s V_g \int_{V_g(1+M_1)/2}^{V_g} C_{oss,p}(v) dv \ , \tag{5.21}$$

if $-1 < M_1 < 1$, resulting in partial hard switching of the primary devices. If $M_1 = 1$, ZVS is obtained and the converter is not operating in Modes 2 or 4. If full hard switching of the primary occurs, $M_1 = -1$, and this becomes

$$P_{sw,p}\big|_{(M_1=-1)} = 4 C_{peq,Q} {V_g}^2 f_s \ . \tag{5.22}$$

Similarly, under conditions in which the secondary devices are hard switched, the losses due to full hard switching are given by $4 C_{seq,Q} {V_{out}}^2 f_s$. In order to make the transition between soft switching and full hard switching continuous, a variable, $M_{1,s}$, is introduced which is the dual of M_1 for hard switched primary devices. State plane analysis is then carried out for the secondary resonance

between L_l and C_s at the nominal operating point solved for by the primary state plane analysis which originally neglected δ. The δ-interval is assumed to have a programmed-constant dead time equal to $t_{\delta 0}$, where resonance occurs between C_s and L_l if the tank current is positive during any portion of the interval. If the current remains negative during the entire interval, device antiparallel diodes will conduct for the duration of the interval, resulting in full hard switching of secondary device capacitances. Otherwise, M_{1s} is calculated in the same manner as M_1 on the primary side, and the switching losses due to partial hard switching of C_s are given by:

$$P_{sw_s} = 4 f_s V_{out} \int_{V_{out}(1+M_{1s})/2}^{V_{out}} C_{oss,s}(v) dv \ , \tag{5.23}$$

Conduction losses are calculated as before, and core losses are again calculated using the NSE/iGSE.

5.2.3 Analysis of Optimal Efficiency Trajectory

In order to further examine converter efficiency across a range of operating modes and conditions, a prototype DAB converter is used to obtain numerical results. The converter is implemented with all silicon devices, again using FDMC2610 primary devices but now using IRFS6713 DirectFETs as the secondary devices; the packaging on the DirectFET devices has very low parasitic inductance, which has been found to have significant contribution to power loss in the previous analysis. Tank magnetic components are unaltered. Details of this converter are given in Table 5.1, with derived analytical values in Table 5.2. Of considerable interest is determining the boundaries

Table 5.1: Prototype Circuit Components

Primary MOSFETs	FDMC2610
Secondary MOSFETs	2x IRFS6713
Tank Inductance	LP02-500-1S
Transformer Core	0L42020UG
Transformer Turns Ratio	25:2

of each operating mode from the converter solution. These regions are defined by the range of

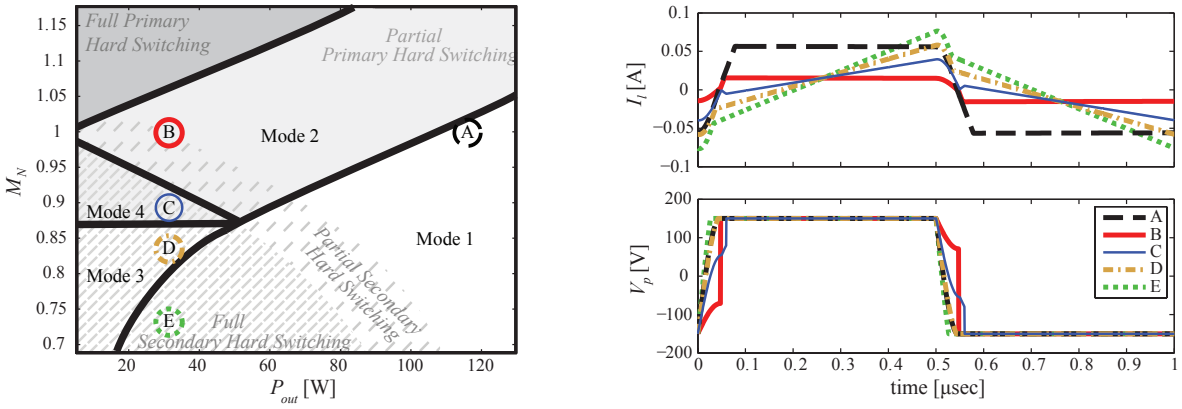
Table 5.2: Prototype Circuit Parameters

C_p	C_s	L_l[†]	L_{lk}	L_x	n_t	V_g	P_{out}
70 pF	2 nF	8 μH	2 μH	1.5 nH	0.079	150 V	0-120 W

[†] reflected from 50 nH inductor on secondary-side, not including stray/leakage inductances

values M_N and P_{out} over which the converter solution remains internally consistent i.e. where the solved voltages, currents, and times are of value that do not violate the form of the state planes in the respective operating modes. These boundaries are solved iteratively, with the results shown in Fig. 5.10a, and example waveforms i_l and v_p corresponding to points A-E given in Fig. 5.10b. The converter is designed for a nominal output voltage of 12 V, which occurs when $V_{out} = n_t V_g$, or $M_N = 1$. In this case, without output voltage variation, the converter will cross from Mode 1 to Mode 2 at an output power of roughly 110 W, with hard switching of the high voltage primary occurring at lower powers. However, if the output voltage can be dynamically decreased as the power falls below 110 W, ZVS can be maintained on all devices as low as 70 W by tracking the boundary between Mode 1 and Mode 2, and on primary devices to zero power if $M_N \geq 0.88$ is permitted, corresponding to an output voltage as low as 10.4 V. The extension of ZVS range comes at the cost of increased RMS current. By decreasing the output voltage, a higher average output current is needed to maintain output power; in addition, any move away from $M_N = 1$ causes increased ramping of inductor current during the ζ-interval, resulting in a higher peak-to-average current ratio, though lower absolute RMS currents remain possible by increasing M_N above unity. Thus, following directly the boundary between Mode 1 and Mode 2 for the power range 70 W $\leq P_{out} \leq$ 110 W maintains primary ZVS with the lowest RMS currents possible.

For $P_{out} >$ 110 W, larger values of M_N result in lower RMS currents, which help quell the dominance of conduction losses at high current. However, also of significance are the losses due to stray inductance L_D, and the inductor core losses, both of which increase at high power due to large phase shift and peak currents. Losses due to L_D, particularly, decrease at lower M_N, where the inductor current waveshape during the ζ-interval allows smaller currents in L_D when the secondary



(a) (b)

Figure 5.10: Operating mode locations for prototype converter are shown in (a). Shaded regions indicate primary hard switching, while the dashed region indicates hard switching of secondary devices. The points labeled A-E correspond to the time-domain waveforms of (b).

is switched.

Below $P_{out} = 50$ W, switching and core losses are dominant due to the low current levels. Mode 4 can be safely assumed to be a poor choice for low power operation, as significant switching losses are contributed from both primary and secondary bridges. Further, hard switching of the secondary is preferable to hard switching of the primary, as the high voltage input leads to greater losses from hard switching the primary than the secondary as long as

$$C_p > C_s \left(M_n n_t\right)^2 \tag{5.24}$$

which is true for most device combinations when n_t is sufficiently small, as is the case in this application. Further, transformer voltage stresses are only marginally affected by converter operating point, and the lack of a large phase shift limits voltage stresses on the inductor. Thus, within Mode 3, efficiency is determined largely by constant losses, and output voltage has only a minor effect on determining losses.

To verify the efficiency analysis, losses in each operating mode are calculated to produce the efficiency contour plot of Fig. 5.11. The optimal efficiency trajectory across all output powers follows largely the expected trajectory. A second, proposed trajectory is also illustrated, which will be shown in the following section to have significant advantage in terms of controllability. For now, the proposed trajectory can be seen to be very near to optimal efficiency across the majority of the load range, with some deviation at low and high power. The breakdown of the losses on both trajectories is compared to experimental measurements with the prototype converter in Fig. 5.12.

5.3 Automatic Regulation of Converter Dead Times and Output Voltage

For the simple, unregulated DAB operating as a DCX (i.e. with a fixed conversion ratio $M_N = 1$), closed-loop digital control can be implemented as shown in Fig. 5.13. The input and output voltage are sensed through sensing and ADC conversion gain H, then compared with scaling factor n_t. This $1/n_t$ multiplication can be combined into the analog circuitry which implements voltage sensing to prevent the need for digital multiplication which increases controller complexity.

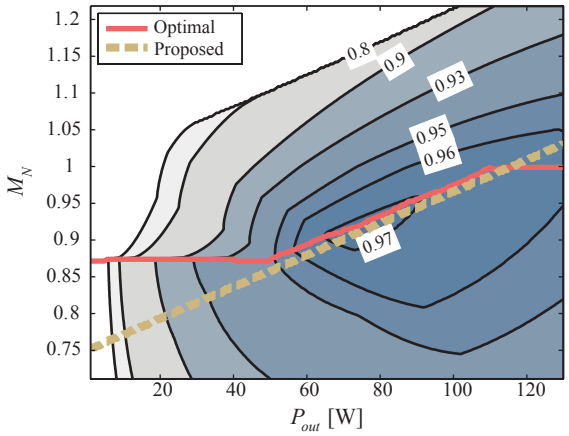
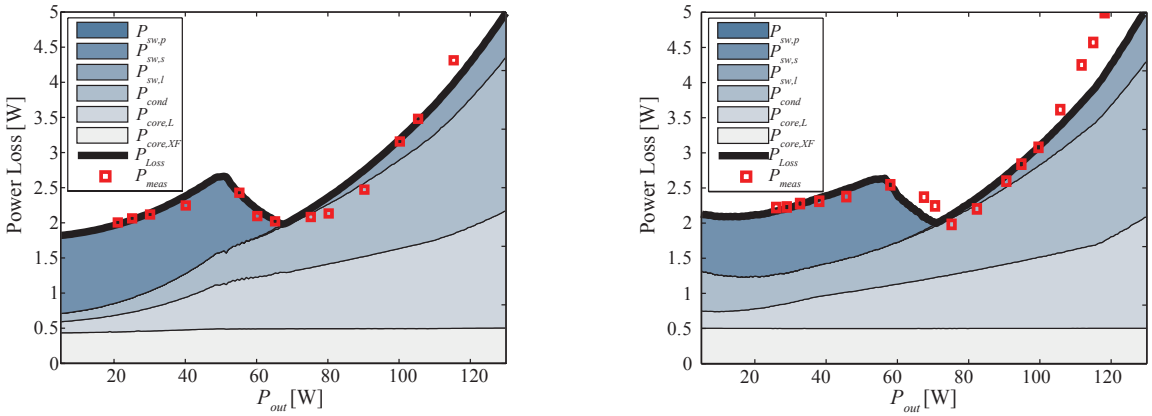


Figure 5.11: Efficiency contours of DAB converter in Modes 1-4. The solid line indicates the highest efficiency trajectory.



(a) (b)

Figure 5.12: Analytical loss breakdown for both optimal (a) and proposed (b) trajectories. Note that $P_{sw,p}$ is not included, as neither trajectory contains points in which any hard switching of the primary devices is incurred.

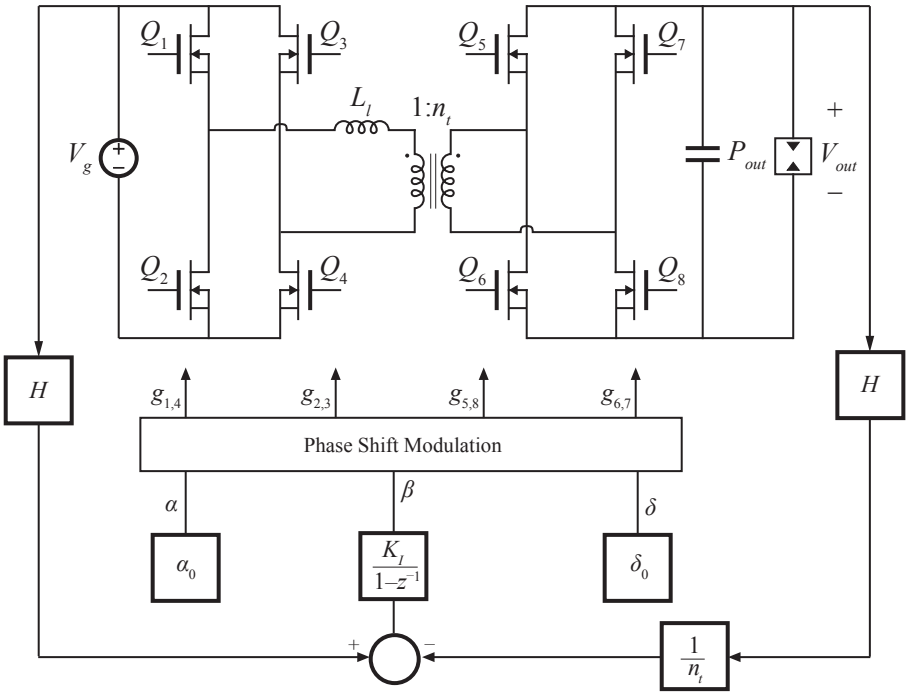


Figure 5.13: Block diagram of closed-loop phase shift modulation of DAB converter to maintain a constant conversion ratio equal to the transformer turns ratio. A discrete time integral compensator is used as an example.

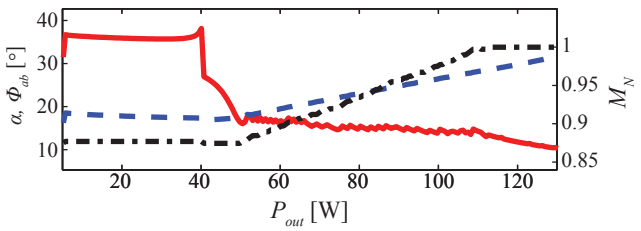
The error between input and scaled output voltages is then used to feed a compensator, which is shown as a discrete integral compensator. If primary and secondary dead times are kept constant with normalized values α_0 and δ_0 respectively, the overall converter phase shift

$$\Phi_{ab} = \alpha + \beta + \delta \ , \tag{5.25}$$

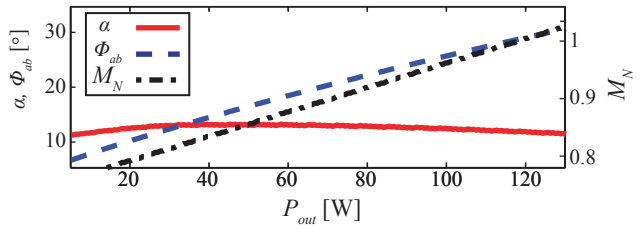
can be set through adjustment of $t_2 \mapsto \beta$. A phase shift modulation block then takes the timing variables α, β, and δ as inputs and generates the gate drive signals for all devices.

The DCX controller in Fig. 5.13 regulates the converter onto the trajectory on which $M_N = 1$ for all output powers by setting a constant conversion ratio $V_{out}/V_g = n_t$. In order to regulate the converter onto either the proposed or optimal trajectories, an effective controller must adjust both the converter primary dead time α and total phase shift Φ_{ab} to the specified values at each output power to obtain the correct value of the varying conversion ratio. Fig. 5.14 shows the steady-state dead time α and total phase shift along with the normalized conversion ratio required to keep the converter on either the optimal or proposed trajectories of Fig. 5.11. For the optimal controller, the values in Fig. 5.14a are both nonlinear and widely varying; in order to accurately track this trajectory, a controller is likely to require measurement of the output power and a lookup table to find the appropriate control parameters for each power. An example implementation of such control is shown generally in Fig. 5.15. This controller has a number of undesirable features which were not present previously. First, the use of current sensing at the output port requires additional circuitry which increases the cost and complexity of the converter control, particularly as the output current is potentially quite large in value. Second, the use of a control timing lookup table (LUT) constrains the controller to digital implementation, and may require large storage if high resolution is required. Additionally, the necessary multiplication of output voltage and power will require significant resources on the digital controller. Finally, the dynamic behavior of the system is potentially quite complicated due to the nonlinear behavior of the LUT and the presence of two varying inputs to converter operation; both α and β are varied.

Conversely, the control parameters of Fig. 5.14b, for the proposed trajectory, are quite simple.



(a)



(b)

Figure 5.14: Plot of control angles α and phase shift $(\alpha + \beta)$, in radians, plotted across a range of output powers for both the ideal efficiency trajectory (a) and proposed control trajectory (b) from Fig. 5.11.

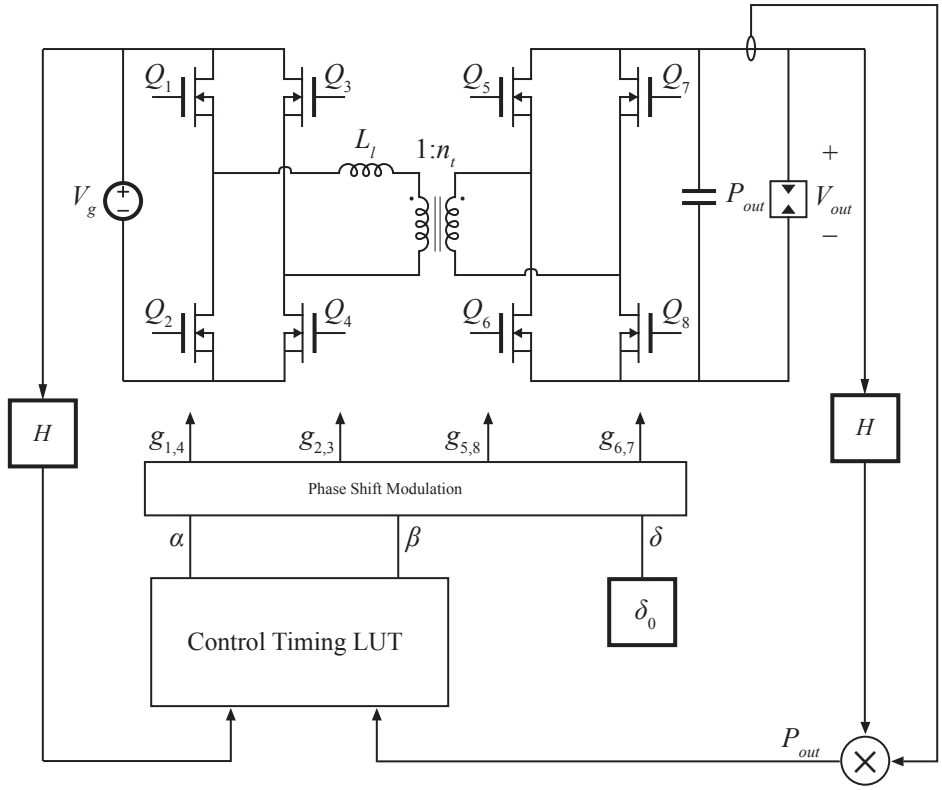


Figure 5.15: Control block diagram implementing control which is capable of driving the DAB to operate on the ideal efficiency trajectory.

On this trajectory, primary dead time α may be approximated as constant with only minimal additional detriment to converter efficiency in terms of diode conduction or minor partial hard switching or primary. Further, it can be seen that both the total phase shift Φ_{ab} and conversion ratio M_N are very nearly linear functions of P_{out}; and are thus collinear. Therefore, it is possible to construct a controller for this trajectory which does not require measuring the output power, but instead enforces a linear relationship between Φ_{ab} and M_N, of the form

$$M_N = K\Phi_{ab} + C \ . \tag{5.26}$$

For this purpose, the controller of Fig. 5.16 is employed. The dead times t_1 and t_3 are set to constants of value slightly less than one-quarter of the resonant period of L_l and the respective primary and secondary capacitances, $\alpha_0 \approx \delta_0{}' \approx \pi/2$. The phase shift is then set through adjustment of t_2 by a feedback loop consisting of sensed values (through ADC gain H) for V_g and V_{out}, whose difference is the input to an integral compensator. Around this integrator, a second loop adjusts the conversion ratio by adding or subtracting both a constant offset C_ϕ and an offset proportional to the total phase shift, $K_\phi\Phi_{ab}$. This additive approach allows the controller to be implemented digitally without the need for floating point division. The controller implements a feedback which, through the use of an integral compensator, forces steady-state behavior

$$M_N = \left(\frac{K_\Phi}{HV_g}\right)\Phi_{ab} + \left(\frac{C_\Phi}{HV_g} + 1\right) \ , \tag{5.27}$$

which appropriately matches the desired form from (5.26). Proper operation of the proposed controller, as well as verification of the loss model is given in the following section.

5.4 Experimental Results

The converter depicted in Table 5.1 is constructed. The control loop of Fig. 5.16 is implemented using a Xilinx Virtex 4 FPGA to demonstrate controller operation. A delay line is implemented as in Appendix B to achieve 3.2 GHz modulator resolution, and 12-bit, 15 MSPS ADCs are used to track input and output voltages. Values for K_ϕ and C_ϕ are tuned experimentally, and K_I is set to stabilize the loop. The PWM and control circuitry occupy fewer than 5,000

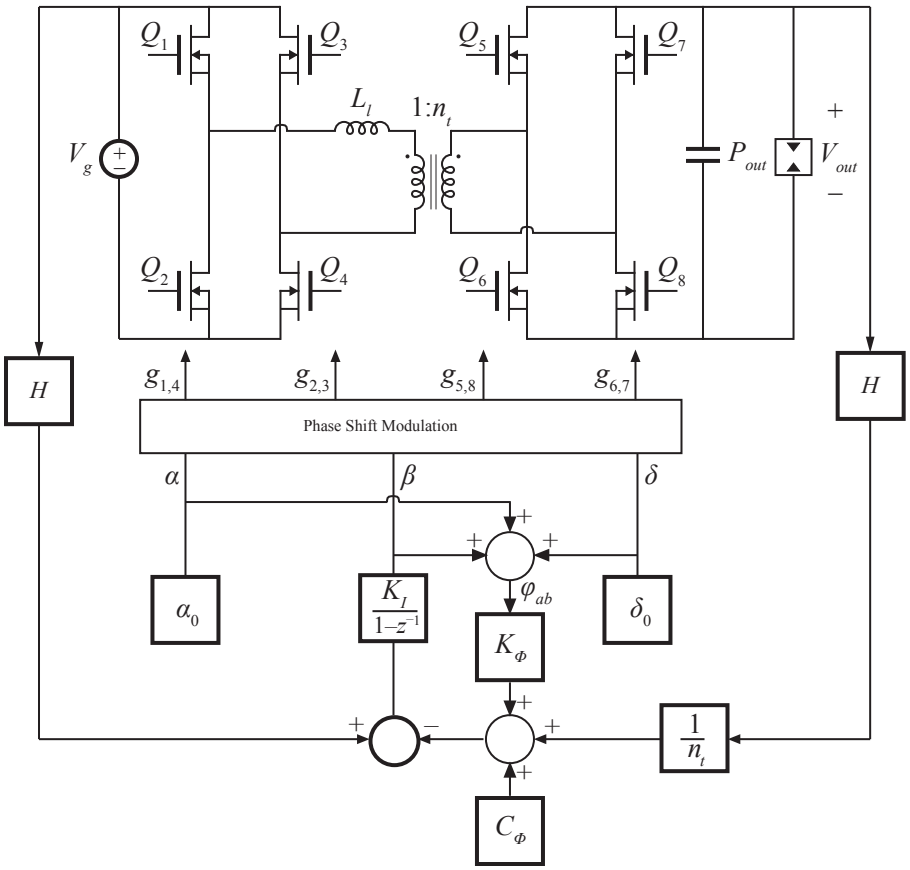


Figure 5.16: Proposed control architecture for DAB converter. Linear feedback of Φ_{ab} is used to set conversion ratio M_N.

gates on the Virtex 4, verifying that the simple control strategy could be implemented on a low-cost IC.

Conversion ratio and efficiency are measured experimentally using two calibrated Agilent 34411A multimeters to measure input current and output voltage, as well as two Fluke 45 multimeters for output current and input voltage, while converter waveforms are measured using a Tektronix DPO2014 oscilloscope with TCP0030 current probe. A comparison between the obtained experimental efficiencies and the predicted efficiencies for both the proposed closed-loop control method, and for manually optimized timing parameters and output voltage for maximum efficiency, is given in Fig. 5.17. Example waveforms are given in Fig. 5.18, including a peak power stage efficiency of 97.4% at $P_{out} = 100\ W$ Note that, like the analysis, the efficiency results presented here do not include the gate drive losses, which are taken from a separate supply, and are estimated analytically to be 2.75 W for the given device combination. Note that the proposed control is able to operate the converter all the way to $P_{out} = 0$ W while maintaining primary ZVS as shown in Fig. 5.18. At zero power, V_{out} remains 10 V, and power losses are measured at just 2.5 W. Over the full output power range, $0 < P_{out} < 120$ W, the output voltage remains in the range $10 < V_{out} < 12.5$ V.

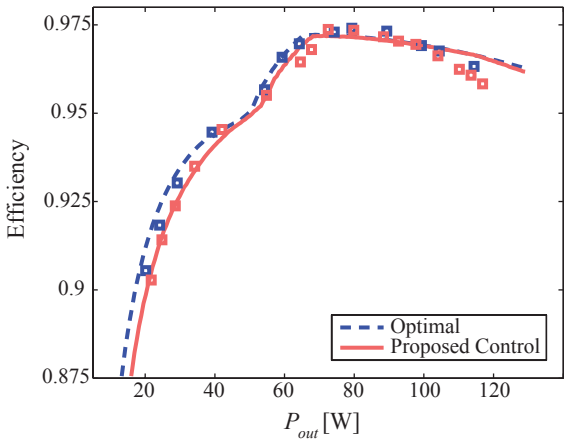


Figure 5.17: Comparison of analytical solutions (lines) and experimental data (boxes) for optimal and proposed trajectories.

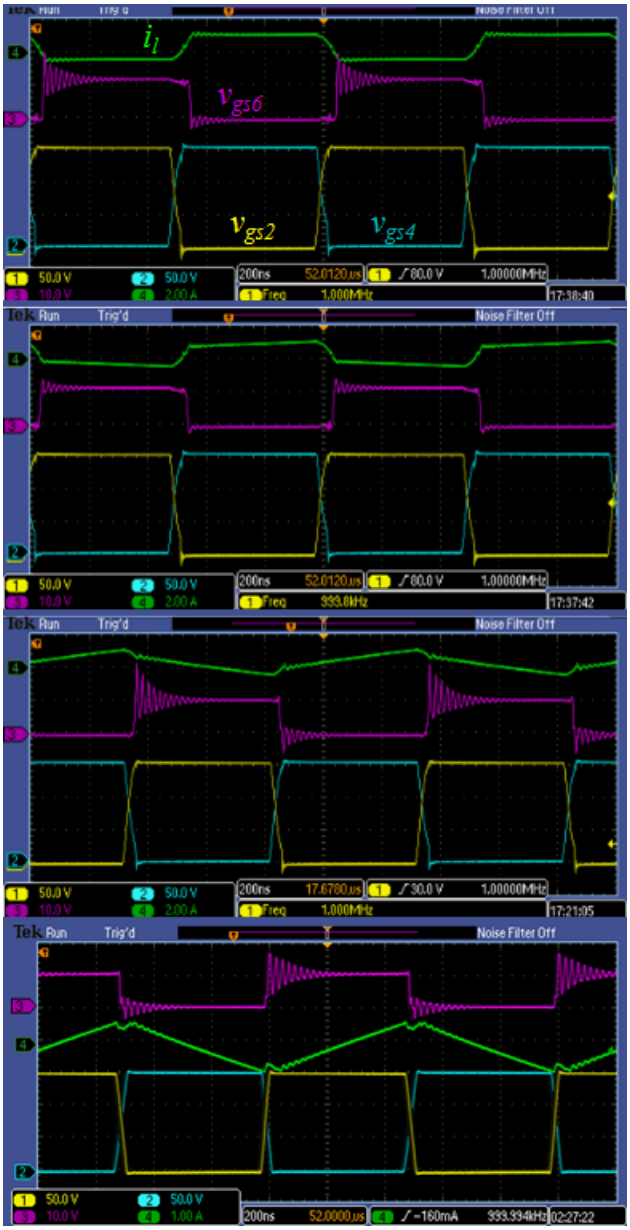


Figure 5.18: Sample waveforms for DAB converter with proposed closed loop control. From top to bottom, depicted output power levels are 100, 80, 20, and 0 W.

Summary

This chapter considers the analysis and control of an unregulated, high step-down, high frequency dual active bridge converter. The previously detailed state plane analysis is extended to analyze the converter across four different operating modes which encompass the full range of operating conditions and output powers. The loss model is then used to solve for a method of varying the output voltage of the converter in response to changes in output power so that the highest efficiency can be obtained at each power without altering control or modulation techniques. This optimal trajectory is then slightly modified to obtain a proposed trajectory for variation of V_{out} which very nearly approximates the optimal efficiency trajectory, but has significant favorable characteristics in terms of the cost and simplicity of control circuitry.

Further refinements to transformer design, PCB layout, and adjustment of constant dead time intervals have allowed even further improvement of converter efficiency beyond the results presented above and in [130,131], increasing peak power stage efficiency to a measured 98.4%. The steady-state behavior of the converter is summarized in a single figure in Fig. 5.19, which depicts experimentally measured data for the prototype converter under the proposed control. Efficiency and normalized values for primary dead time, conversion ratio, and phase shift are depicted on the same axis. Key features of the proposed control method are

- Primary dead time α remains constant
- Both conversion ratio M_N and phase shift Φ_{ab} are linear with P_{out}
- Efficiency remains high across all operating powers

which allow for simple control, and favorable steady-state operation of the converter.

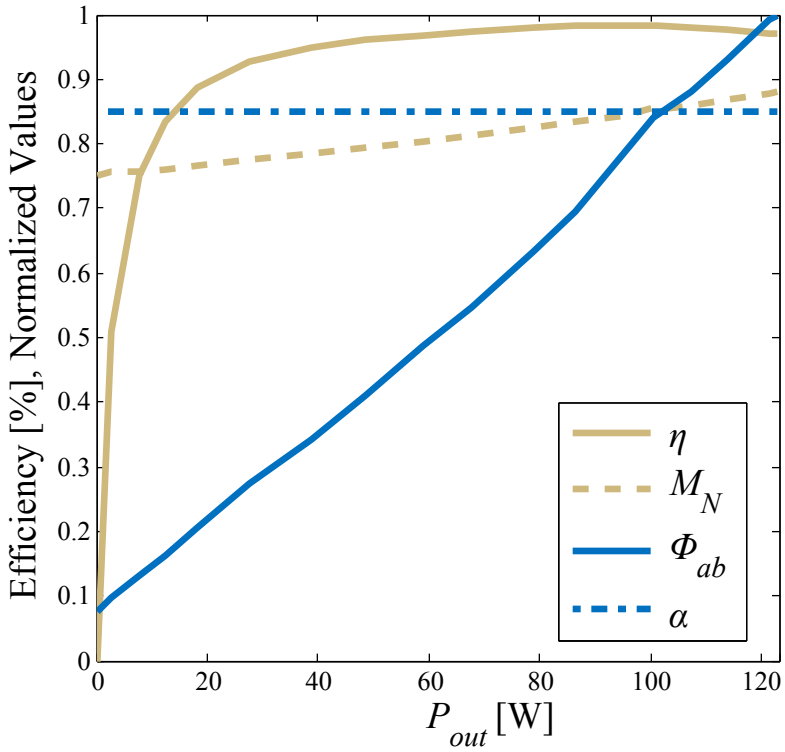


Figure 5.19: Closed loop DAB steady-state behavior on the proposed trajectory. Efficiency is shown in addition to normalized conversion ratio, phase shift, and primary dead time on the same y-axis while output power is varied on the x-axis

Chapter 6

Dynamic Operation of DAB Converter

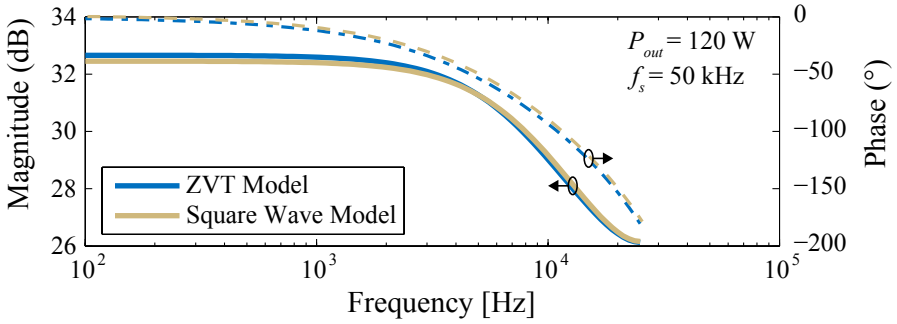
The variation of output voltage with output power proposed in Chapter 5 led to favorable steady-state operation of the converter, as characterized by high efficiency operation across the full span of the output power range. However, the implications on dynamic operation were not considered in the construction of the $V_{out} - P_{out}$ trajectory. Example controller implementations given previously have relied on the (experimentally verified) assumption that a low-gain integral compensator is capable of stabilizing the system. In order to determine the merit of the proposed control method, the implications on converter transfer functions of the steady-state control trajectory must be discerned.

Much like the steady state analysis, previous work in the area has largely approached dynamic models under the assumption that converter tank dynamics are well approximated by modeling the primary and secondary bridge voltages v_p and v_s as perfect square waves, neglecting the impact of resonant transitions. This leads to a converter model with dynamics only depending on output capacitance and load [59, 133, 134]. For the DAB converter operating at sufficiently high power and low switching period, this gives an accurate model due to the relatively small portion of the switching frequency required to obtain ZVS. However, as in the steady-state analysis, it is expected that the significance of the primary ZVS intervals in the proposed converter will have significant impact on converter dynamics. To verify this, a comparison of simulated frequency responses for an example DAB converter with the same characteristics as the current prototype is shown in Fig. 6.1. Two operating conditions are considered. In Fig. 6.1(a), there is very little disparity between the

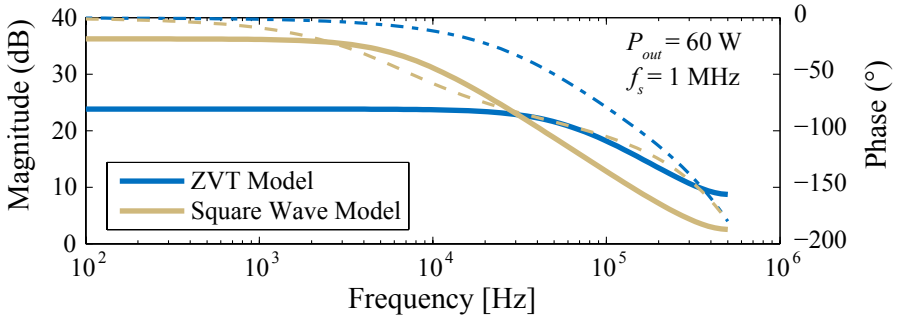
Bode plots with and without ZVS transitions included due to the relatively low switching frequency and higher power level, resulting in short duration of ZVS intervals. In contrast, Fig. 6.1(b) shows significant error in the square wave model Bode plots which neglect ZVS transitions due to their increased significance at lower-power, higher-frequency operating points. This confirms that while the square-wave model is accurate at the relatively low frequency and high power operating points that it is commonly employed in the literature, it is insufficient to accurately model converter dynamics at high frequency and low power due to its neglect of zero voltage switching transitions. ZVS interval dynamics have been modeled previously in [135], but operation was considered at a single, high-power operating point far above ZVS boundary points and resulted in a computationally intensive model.

Thus it is desired to develop a discrete-time small-signal model of the 1 MHz, 100 W, 150-to-12 V nominal prototype DAB converter operating over the full load range and varying the output voltage in accordance with the proposed trajectory. Because a digital controller is employed, the converter dynamics will be modeled in discrete-time following methods developed in [136–139].

In attempting to model the DAB converter with resonant transitions across a full range of operating powers, it must be noted that the ZVS boundary in the steady-state analysis also represents a boundary between dynamic models. When ZVS is not obtained, the duration of the resonant dead time is determined entirely by active control from the modulator. When ZVS is obtained, the conduction of antiparallel diodes will move the converter from the resonant dead time interval to the ensuing phase shift interval even if MOSFETs do not commutate immediately as ZVS is obtained. Though conduction through antiparallel diodes will exhibit increased loss relative to conduction through an active MOSFET channel, the dynamic behavior is otherwise unaltered. Thus, the subinterval duration, progression, and operating conditions are fundamentally different for operation above or below the ZVS boundary. This implies that the dynamic model of the converter will therefore be different in each region, though it must remain continuous at the boundary. Similar discontinuities in converter dynamics are observed at the boundary between discrete- and continuous-conduction modes (DCM/CCM boundary) in PWM converters [140].



(a)



(b)

Figure 6.1: Simulation results for Bode plots of the converter from Section 6.4. Dashed lines indicate phase, with solid lines giving magnitude for (a) $f_s = 50$ kHz and $P_{out} = 120$ W; and (b) $f_s = 1$ MHz and $P_{out} = 60$ W.

A defining characteristic of the proposed control trajectory for the DAB converter is that, at all powers, the converter is intended to operate at or near the boundary of ZVS for the primary-side devices. This behavior prevents the high-loss hard switching of high-voltage primary devices with the largest permissible output voltage, which reduces conduction losses in the converter. Because the converter is intended to operate at the ZVS boundary, the converter dynamics will also exist on the boundary between the behavior above and below the ZVS boundary. Dynamic models in each region are, in general, different and the transition between them potentially highly nonlinear. Therefore, to model the converter dynamics effectively, a single region should be selected. Because previous work [135] has shown that modeling the converter above the ZVS boundary results in a complex and non closed-form model for converter dynamics, the model will instead be derived here for operation at or below the ZVS boundary, which results in the simplification of solving for resonant interval duration and thereby gives a simple, closed-form model for converter dynamics. Using the discrete-time small-signal model of the converter power stage, this chapter shows that the proposed trajectory for variation in output voltage leads to nearly constant converter dynamics across the full load range, and therefore has favorable characteristics in both steady-state and dynamic behavior [129].

6.1 DAB Converter Dynamic Operation

To proceed with development of a discrete-time model of the converter, continuous time state-space representations of the converter in each subinterval should be examined, each taking the form

$$\dot{x}(t) = A_i x(t) + B_i V_g, \tag{6.1}$$

where $x(t) = [\, v_p \; i_l \; V_{out} \,]^T$ is the state vector, and $i = \{1, 2, 4, 5, 6, 8\}$. For this analysis, the input is assumed to be an ideal voltage source and the output port loaded by a constant resistance, as we are primarily concerned with the control-to-output transfer function, $G_{v\phi}$, for the purpose of converter control design.

Continuing the simplification developed previously, the secondary resonant interval (subinterval III) will continue to be assumed to occur nearly instantaneously (i.e. $t_3 = t_7 = 0$) due to the high output current allowing negligibly fast ZVS transitions. Assuming all switches are ideal except for their respective output capacitances, the equivalent circuits corresponding to DAB subintervals I, II, and IV developed in Section 3.1 are reviewed in Fig. 6.2. State transition matrices are then derived from these circuits for each subinterval. In order to reset the magnitude of the primary side voltage to the input voltage at the end of each resonant interval, the state matrices for intervals II and IV are modified to also short the input capacitance to the proper voltage through the on-resistance of two primary side devices, $2R_p$. Though the effect of conduction losses on converter dynamics is not considered here, the resistance is included in this case to prevent infinitely fast dynamics in the case of hard-switched operation. The resulting matrices for subintervals I, II, and IV are given in (6.2-6.4)

$$A_1 = \begin{bmatrix} 0 & 0 & \frac{-1}{C_p} \\ 0 & \frac{-1}{C_{out}R_{out}} & \frac{1}{C_{out}n_t} \\ \frac{1}{L_l} & \frac{-1}{L_l n_t} & 0 \end{bmatrix} \quad B_1 = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix}, \tag{6.2}$$

$$A_2 = \begin{bmatrix} \frac{-1}{2R_pC_p} & 0 & 0 \\ 0 & \frac{-1}{C_{out}R_{out}} & \frac{1}{C_{out}n_t} \\ 0 & \frac{-1}{L_l n_t} & 0 \end{bmatrix} B_2 = \begin{bmatrix} \frac{-1}{2R_pC_p} \\ 0 \\ \frac{-1}{L_l} \end{bmatrix}, \tag{6.3}$$

$$A_4 = \begin{bmatrix} \frac{-1}{2R_pC_p} & 0 & 0 \\ 0 & \frac{-1}{C_{out}R_{out}} & \frac{-1}{C_{out}n_t} \\ 0 & \frac{1}{L_l n_t} & 0 \end{bmatrix} B_4 = \begin{bmatrix} \frac{-1}{2R_pC_p} \\ 0 \\ \frac{-1}{L_l} \end{bmatrix}, \tag{6.4}$$

With A_3 and B_3 not considered because $t_3 = 0$ has been assumed.

For low power operation in Modes 3 and 4, operation with $\beta < 0$ is incurred. The equivalent circuit of subinterval II in Fig. 6.2b is replaced by that of Fig. 6.3, with corresponding changes in

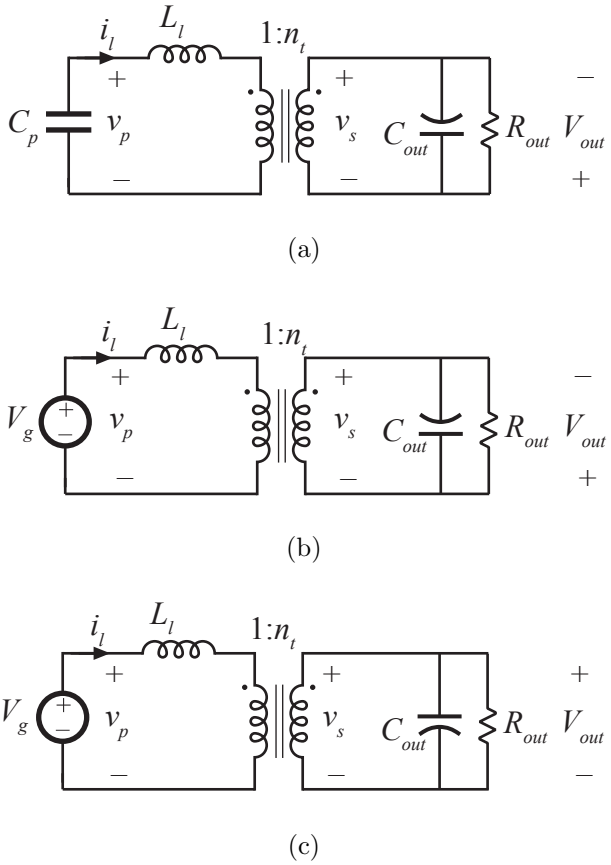


Figure 6.2: Equivalent circuits during subintervals I, II, and IV (top to bottom). C_{out} is drawn with reference polarity to emphasize the commutation of the secondary side bridge

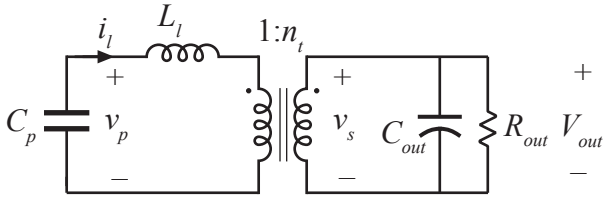


Figure 6.3: Equivalent circuit during subinterval II when $\phi_{ab} < t_1$, modeled by A_2^* and B_2^*.

the A_2 and B_2 matrices

$$A_2^* = \begin{bmatrix} 0 & 0 & \frac{-1}{C_p} \\ 0 & \frac{-1}{C_{out}R_{out}} & \frac{-1}{C_{out}n_t} \\ \frac{1}{L_l} & \frac{1}{L_l n_t} & 0 \end{bmatrix} \qquad B_2^* = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix}, \tag{6.5}$$

where $t_2^* = |\phi_{ab} - t_1|$. This alternate operating mode results in two resonant intervals per half-period.

In general, the total resonant time t_1 varies with operating point and mode, and contains some nonlinearity as the converter moves between operating conditions below or above ZVS boundaries, causing either hard switching or diode conduction, respectively. The model previously proposed in [135] takes this into account by including a computationally intensive non-closed form method for solving t_1 in the converter model, assuming the converter always operates above ZVS boundaries and $\phi_{ab} > t_1$ to maintain operating mode. The model developed here takes a simplified approach which is correct for points at or below the ZVS boundary. This is then coupled with the steady-state control method of Chapter 5, which guarantees all steady-state operating points are placed near this boundary, with t_1 being nearly constant across load conditions. The result is a model which is less computationally intensive, is expressible in closed form, and remains valid across all load conditions on the proposed trajectory.

6.2 Discrete-Time Modeling of DAB Converter

In order to develop a discrete time model, the state vector $x(t)$ is sampled at time instances corresponding to the start of the primary ZVS interval $t = nT_s$ to create the discrete time state

vector, $x[n] = x(nT_s)$. Waveforms of the three signals which make up this vector are shown in Fig. 6.4 in continuous time, with sampling instances shown explicitly.

A discrete-time, sampled data model of the DAB converter based on [136–139] is developed using the results of the previous section. The goal is to produce a model of the form

$$\hat{x}[n] = F\hat{x}[n-1] + G\hat{\phi}_{ab}[n-1], \tag{6.6}$$

where hats denote small signal variables. Small-signal perturbations are only considered on the duration of the phase-shift ϕ_{ab}; both the source and load are considered constant. To solve values for F and G, the converter response to a perturbation in state $\hat{x}$ and a perturbation in phase shift $\hat{\phi}_{ab}$ are considered independently.

6.2.1 Response to Perturbation in State

Beginning by examining the independent effect of a state perturbation $\hat{x}[n-1]$ on states, a diagram of the state propagation which results about steady-state time-varying vector $x(t)$ is shown in 6.5, where the waveshape of the vector $x(t)$ is drawn with waveshape of the inductor current for illustrative purposes. The perturbation $\hat{x}[n-1]$ propagates passively through the six subintervals to give the resulting small signal perturbation in states $F\hat{x}[n-1]$ which results from $\hat{x}[n-1]$.

The state propagation vector F can be found by considering the solution to the continuous time state space definition of the subsystem in each subinterval, as given in (6.1) with constant inputs

$$x(t) = e^{A_i t}x_0 + A_i^{-1}\left(e^{A_i t} - I\right)B_i V_g \ . \tag{6.7}$$

With known durations for each subinterval $t_1, t_2, t_4, ...$ and zero small-signal component on V_g, equation (6.7) is applied consecutively for the six subintervals to obtain

$$F = e^{A_8 t_8}e^{A_6 t_6}e^{A_5 t_5}e^{A_4 t_4}e^{A_2 t_2}e^{A_1 t_1} \ . \tag{6.8}$$

If, as diagrammed in 6.5, there is no variation in phase shift $\hat{\phi}_{ab} = 0$, then $F\hat{x}[n-1] = \hat{x}[n]$. However, if there is a non-zero small-signal component on the converter phase shift, $\hat{x}[n]$ will contain components from both $\hat{\phi}_{ab}$ and $\hat{x}[n-1]$.

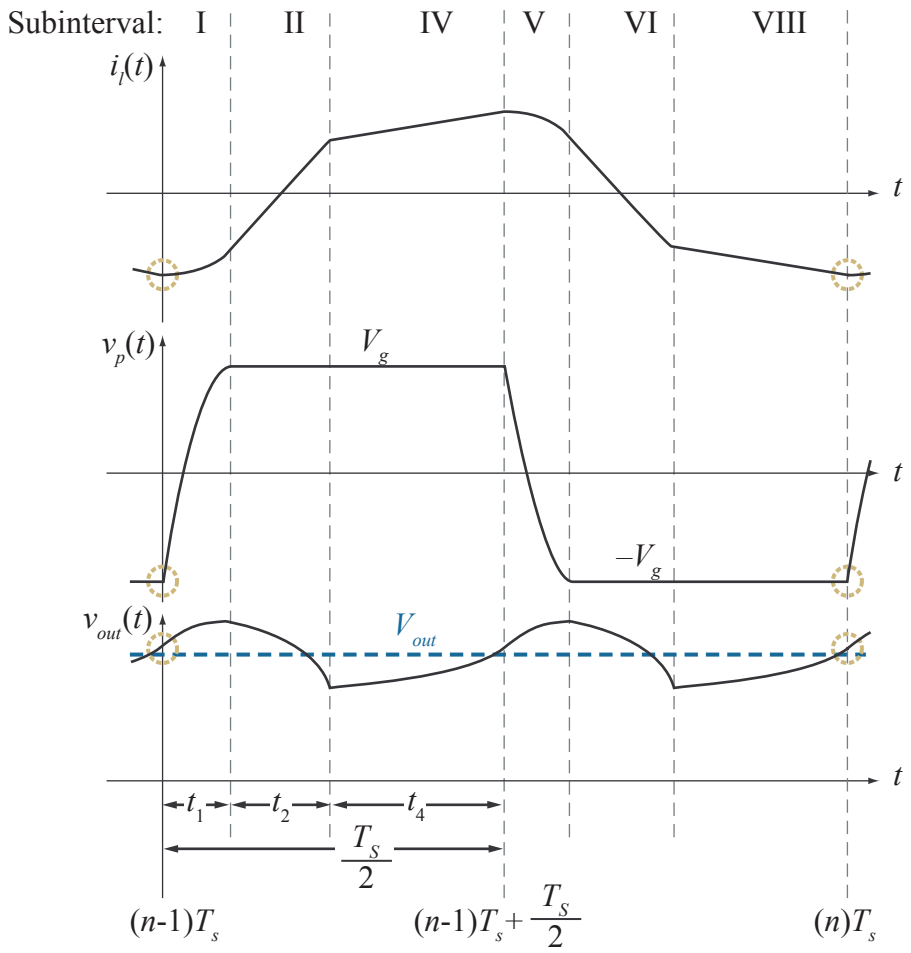


Figure 6.4: Continuous time waveforms of the three states considered in the DAB operation. When sampled at $t = nT_s$, the resulting sampled values of the waveforms are circled.

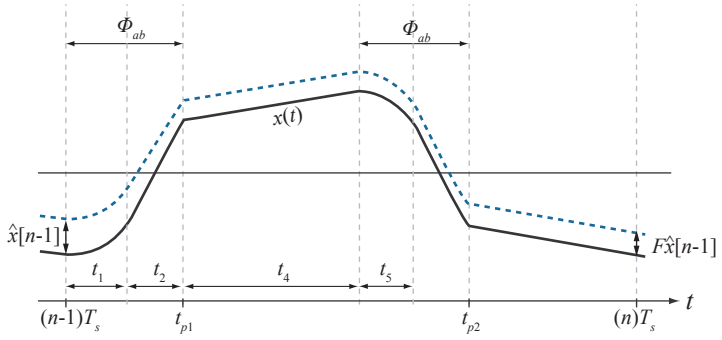


Figure 6.5: Diagram of effect of small-signal perturbations in the state vector $x(t)$, sampled at $t = nT_s$. The small-signal perturbation $\hat{x}[n-1]$ present at $t = (n-1)T_s$ propagates through all states in one switching period to yield the resulting small-signal perturbation $F\hat{x}[n-1] = \hat{x}[n]$ at the end of the switching period.

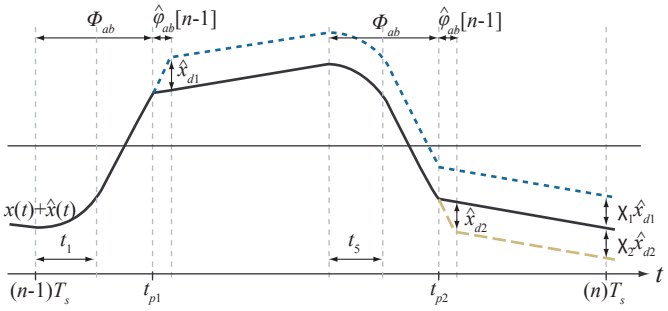


Figure 6.6: Diagram of effect of small-signal perturbations in phase shift on state vector $x(t)$, sampled at $t = nT_s$. The small-signal perturbation $\hat{\phi}_{ab} = 0$ for $t < (n-1)T_s$, and updated to $\hat{\phi}_{ab} > 0$ at $t = (n-1)T_s$ with $t_1 = t_5$ held constant.

6.2.2 Response to Perturbation in Phase

To solve the component due to $\hat{\phi}_{ab}$, the result of a small signal pertubation in phase shift is shown in Fig. 6.6. Because the converter has two phase-shift intervals per switching period, a perturbation in phase alters the states at two points, t_{p1} and t_{p2}, corresponding to the end of phase-shift subintervals II and IV. The net results of the phase perturbations at each point are two corresponding state perturbations, $\hat{x}_{d1}$ and $\hat{x}_{d2}$. The state perturbations can be solved by considering the difference between the steady-state and perturbed propagation of the states during the $\hat{\phi}_{ab}$ interval. If X_{p1} and X_{p2} are the steady-state values of the system at t_{p1} and t_{p2} respectively,

$$\hat{x}_{d1} = \left[e^{A_2\hat{t}_2}X_{p1} + {A_2}^{-1}\left(e^{A_2\hat{t}_2} - I\right)B_2V_g\right] - \left[e^{A_4\hat{t}_2}X_{p1} + {A_4}^{-1}\left(e^{A_4\hat{t}_2} - I\right)B_4V_g\right] \ , \tag{6.9a}$$

$$\hat{x}_{d2} = \left[e^{A_6\hat{t}_6}X_{p2} + {A_6}^{-1}\left(e^{A_6\hat{t}_6} - I\right)B_6V_g\right] - \left[e^{A_8\hat{t}_6}X_{p1} + {A_8}^{-1}\left(e^{A_8\hat{t}_6} - I\right)B_8V_g\right] \ , \tag{6.9b}$$

where

$$t_2 = t_6 = \frac{T_s}{2\pi}\phi_{ab} \ . \tag{6.10}$$

The steady state values of the states X_p may be solved from the state plane analysis in Chapter 5, or through recursive application of (6.7) until a steady state is reached. Further, the steady-state vector at $t = nT_s$ can be determined by noting that, by definition, when steady state is reached

$x[(n-1)T_s] = x[nT_s]$, so the recursive propagation can be solved explicitly as

$$x_{ss}[nT_s] = \left(I - \prod_{i=1}^{n} e^{A_i t_i}\right)^{-1} \left(\sum_{i=1}^{n} \left(\prod_{k=i+1}^{n} e^{A_k t_k}\right) {A_i}^{-1} \left(e^{A_i t_i} - I\right) B_i V_g\right) , \tag{6.11}$$

which is valid if all A_i are invertible. If there exists some subinterval such that $|A_i| = 0$, a steady state solution is likely still obtainable, but the complexity of numerical approximations to the matrix exponential make the use of alternate methods, including state plane analysis, preferable for solving the steady state.

To obtain a linear model, the perturbations $\hat{x}_d$ are then approximated by their first order expansions to obtain

$$\hat{x}_{d1} = \left[(I + A_4)X_{p1} + B_4 V_g\right] \frac{T_s}{2\pi}\phi_{ab} - \left[(I + A_2)X_{p1} + B_2 V_g\right] \frac{T_s}{2\pi}\phi_{ab} , \tag{6.12a}$$

$$\hat{x}_{d2} = \left[(I + A_6)X_{p2} + B_6 V_g\right] \frac{T_s}{2\pi}\phi_{ab} - \left[(I + A_8)X_{p2} + B_8 V_g\right] \frac{T_s}{2\pi}\phi_{ab} . \tag{6.12b}$$

These expressions are simplified, noting that $B_2 = B_3$ and $B_5 = B_6$, to obtain

$$\hat{x}_{d1} = (A_2 - A_4)X_{p1} \frac{T_s}{2\pi}\hat{\phi}_{ab}, \tag{6.13a}$$

$$\hat{x}_{d2} = (A_6 - A_8)X_{p2} \frac{T_s}{2\pi}\hat{\phi}_{ab}. \tag{6.13b}$$

In accordance with the linearized small signal model assumptions, the effect of perturbations from the input will be assumed to happen instantaneously at the points t_{p1} and t_{p2}, which is a good approximation so long as the phase perturbation is sufficiently small compared to the steady-state phase-shift. With this, the instantaneous state perturbations are propagated to the end of the period through χ_1 and χ_2, which follow the form of (6.8)

$$\chi_1 = e^{A_8 t_8} e^{A_6 t_6} e^{A_5 t_5} e^{A_4 t_4}, \tag{6.14a}$$

$$\chi_2 = e^{A_8 t_8}. \tag{6.14b}$$

Finally, (6.13) and (6.14) are combined to give the resulting state perturbation at $t = nT_s$ from the phase perturbations,

$$\begin{aligned} G = e^{A_8 t_8} e^{A_6 t_6} e^{A_5 t_5} e^{A_4 t_4} (A_2 - A_4) X_{p1} \frac{T_s}{2\pi} + \\ e^{A_8 t_8} (A_6 - A_8) X_{p2} \frac{T_s}{2\pi}. \end{aligned} \tag{6.15}$$

Combining (6.8) and (6.15), the control-to-output transfer function is

$$G_{v\phi}(z) = C(zI - F)^{-1}G, \tag{6.16}$$

with sampling rate T_s and $C = [\,0\;0\;1\,]$ for V_{out} as the output variable.

6.2.3 Half-Cycle Model

Examining the state waveforms of Fig. 6.4 it is apparent that, in addition to the periodicity of the waveforms about the switching period, each of the three state waveforms are either symmetric or anti-symmetric about the half-cycle point $t = nT_s + T_s/2$. In fact, because all waveforms in the DAB tank are AC-only and the bridges are operated with nearly 50% duty cycle, it is generally true that all tank waveforms are anitsymmetric about the half-cycle and all input and output waveforms are symmetric about it due to the rectification from the bridges. This feature can be leveraged to model and control the converter with sampling rate $2f_s$, extending the permissible bandwidth of the system and reducing the complexity of the derived discrete time small signal model. In the particular case of output voltage control, a digital controller can sample the output voltage and generate a unique phase response twice per switching period.

To construct the half-cycle model of the converter control-to-output transfer function, the same approach is taken. However, in this case propagation of state perturbations need only be carried through the end of subinterval 4, rather than to the end of the entire switching period. Additionally, in the half-cycle, only one perturbation in phase exists rather than two. The only additional step added to this model is that, at the end of the half-cycle, the values for all antisymmetric states must be inverted in order to match the polarity expected in the model for the next interval. This is accomplished simply by including an inverting quasi-identity matrix

$$I_{HC} = \begin{bmatrix} -1 & 0 & 0 \\ 0 & -1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{6.17}$$

which defines the symmetry of the states, $x(t + T_s/2) = I_{HC}x(t)$. This will invert the states of i_l and c_p without altering v_{out}. The state space model of the system then simplifies to

$$\hat{x}[n] = \left(e^{A_4 t_4} e^{A_2 t_2} e^{A_1 t_1}\right) I_{HC} \hat{x}[n-1] + \left(e^{A_4 t_4}(A_2 - A_4) X_{p1} \frac{T_s}{2\pi}\right) \hat{\phi}_{ab}[n-1] \ , \tag{6.18}$$

with sampling rate $2T_s$.

6.2.4 Converter Transfer Function

Whether the full or half-cycle modeling approach is taken, the resulting analytical model of the open loop converter dynamics will be identical. The two models will only differ in their sampling time and resulting closed loop bandwidth constraints. In either case, the transfer function $G_{v\phi}(z)$ is found to take the form

$$G_{v\phi}(z) = G_{v\phi 0} \frac{1 - q_1 z^{-1}}{(1 - p_1 z^{-1})(1 - p_2 z^{-1})}, \tag{6.19}$$

with low-frequency gain $G_{v\phi 0}$, one zero, and two poles with natural frequencies f_{z1}, f_{p1}, and f_{p2}, respectively. The model derivation and final form are the same for the case when $\phi_{ab} < t_1$, as in Mode 3 and Mode 4 operation, but with A_2 and A_6 replaced by A_2^* and A_6^*, and instead considering the propagation through subinterval 2 according to $t_2^* = |\phi_{ab} - t_1|$.

Although the system contains three states as modeled, the resulting control-to-output transfer function is only second order. This behavior could have been predicted from the state waveforms plots of Fig. 6.4; because the chosen sampling instance occurs just prior to the start of the primary ZVS interval, the system will always sample the primary side voltage at $v_p[n] = -V_g$ in the full cycle case. In the half cycle case, the inclusion of I_{HC} will invert the value of $v_p[n]$ each half cycle to yield the same result. Thus, the v_p state appears DC to the sampled system. However, it is important that this state not be neglected, as the dynamics during the propagation through the converter ZVS intervals result in significant effect on the other two states. This is made clear by the considerable error incurred when neglecting the v_p state entirely, as presented in Fig. 6.1.

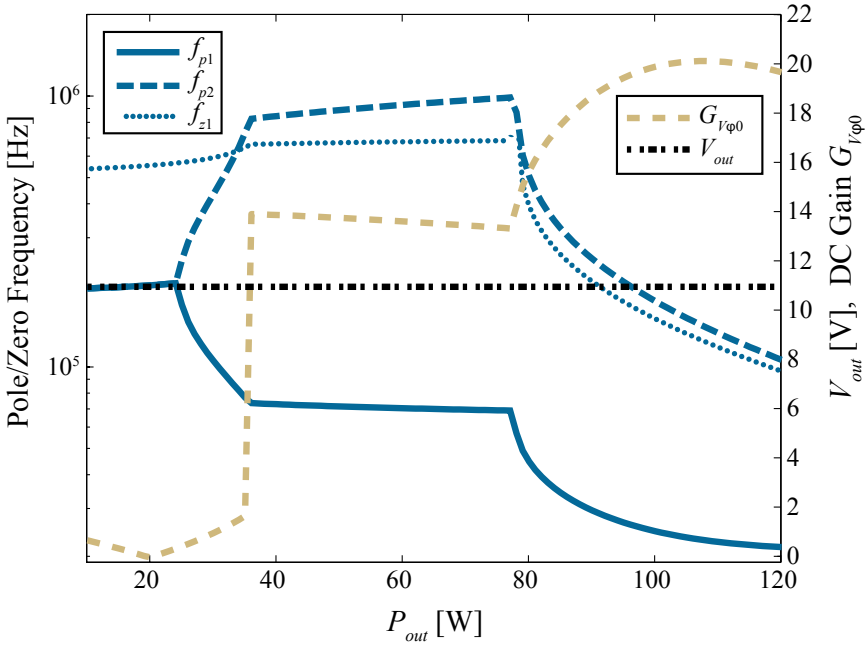
6.3 Model Application Across Wide Load Range

It is desired to use the model developed in the previous section to assess the variations in converter dynamics across the full range of load conditions. To do so, the components and parameters of the all-silicon prototype converter from Table 5.1 and Table 5.2 and are used in conjunction with the analysis of the previous section to numerically solve for the poles, zero, and DC gain for the converter operating with a varying output resistance corresponding to $10\ W < P_{out} < 120\ W$.

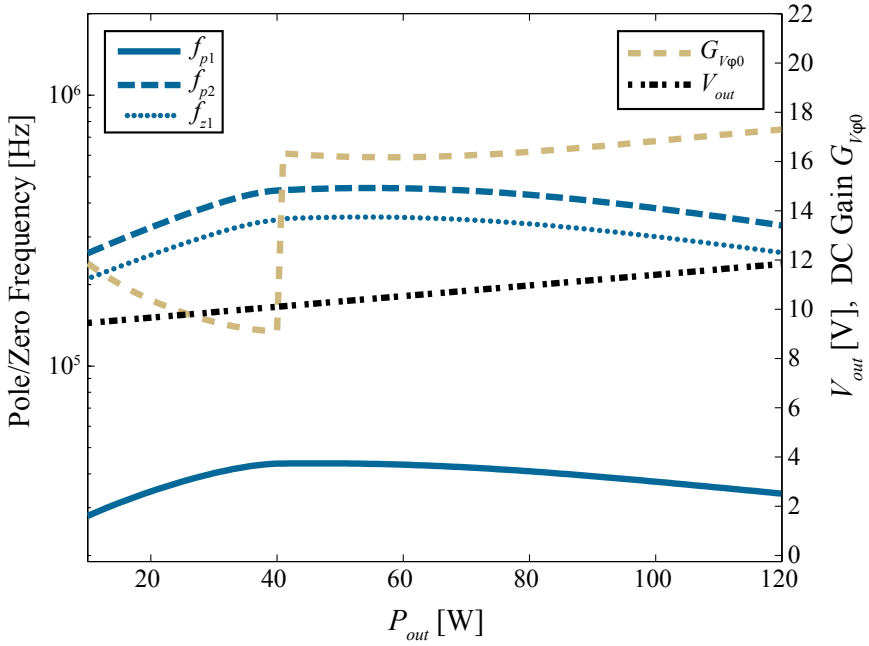
Two cases are considered. First, a constant output voltage equal to $V_{out} = 11\ V$, which permits converter operation with ZVS for powers below the maximum output power. Second, dynamics are considered on the proposed trajectory of Chapter 5, on which V_{out} is varied between $10 < V_{out} < 12.5$ V, proportional to P_{out}. The resulting converter dynamics are plotted across the load range in Fig. 6.7, with corresponding pole-zero maps given in Fig. 6.8 and Fig. 6.9. It can be seen that the proposed trajectory in Fig. 6.7b results in decreased variation in converter dynamics, with all but the DC Gain remaining nearly constant across the full load range, despite the converter moving between different operating modes. In the case of constant V_{out} in Fig. 6.7a, converter dynamics vary much more widely, requiring the control design to either be overly conservative to account for the worst case, or overly complex to account for the variation in converter dynamics. Because converter dynamics are nearly constant on the proposed trajectory, the system can be well controlled by a single, constant compensator, greatly simplifying control requirements.

6.4 Experimental Results

Experimental verification of the discrete-time model is given in both the time domain and frequency domain in Figs. 6.10 and 6.11, respectively. Transient results are obtained using the data export capability of the Tektronix DPO2014 oscilloscope when a step input is applied to the converter phase shift using Xilinx Chipscope software to interface to the Virtex 4 FPGA used as controller. To obtain the frequency response plots, a THS1215 15 MSPS analog-to-digital converter

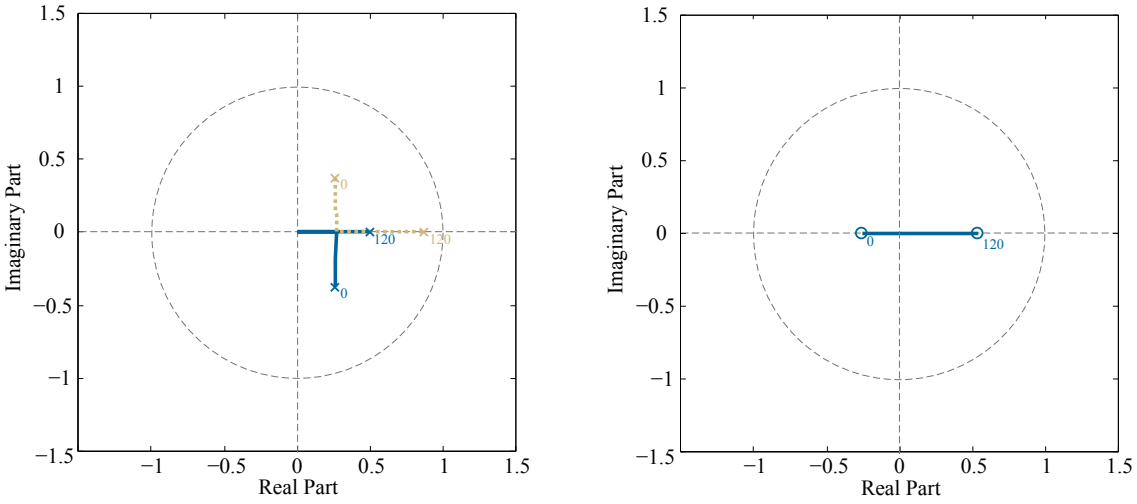


(a)



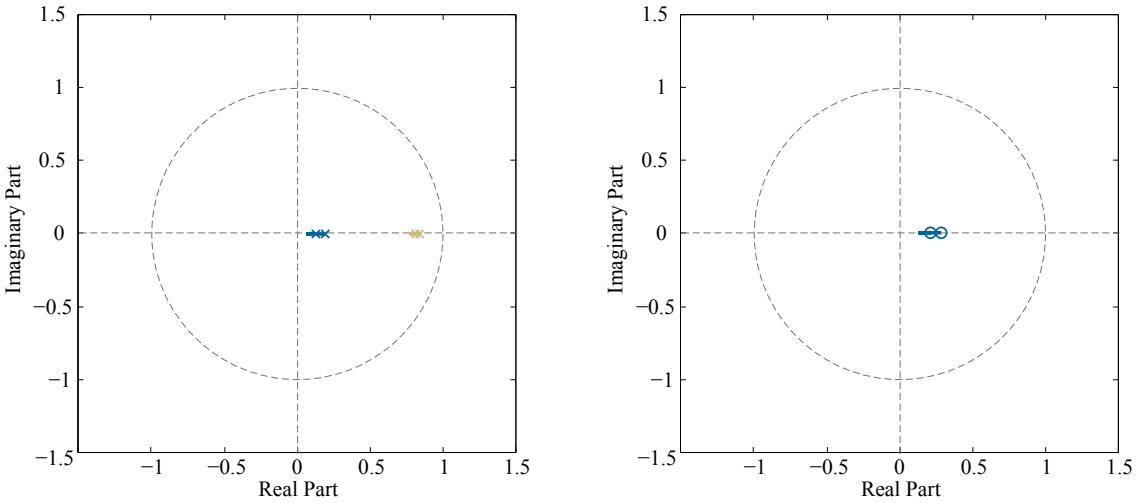
(b)

Figure 6.7: Dynamics and operating point characteristics across full load range for a converter on a constant output voltage trajectory (a) and the proposed trajectory with output voltage proportional to output power (b). Note that in the plot of (b), varying the output voltage greatly reduces the variation in converter dynamics.



(a) (b)

Figure 6.8: Maps of poles (a) and zeros (b) of the control-to-output transfer function of the converter as the output power increases from zero to 120 W (denoted by subscripts) with a constant output voltage $V_{out} = 11$ (V).



(a) (b)

Figure 6.9: Maps of poles (a) and zeros (b) of the control-to-output transfer function of the converter as the output power increases from zero to 120 W with a variable output voltage controlled to place the converter on the proposed trajectory.

is used to sample a varying frequency sine wave generated by a function generator. This sampled value is then added as an offset to the converter phase shift internally to the FPGA. The generator sine wave magnitude and phase relative to the phase shift magnitude and phase are calibrated removed from calculations. Then, the magnitude and phase of the function generator sine wave and resulting AC component of output voltage are compared to assess the converter frequency response at the designated operating points shown in Fig. 6.11.

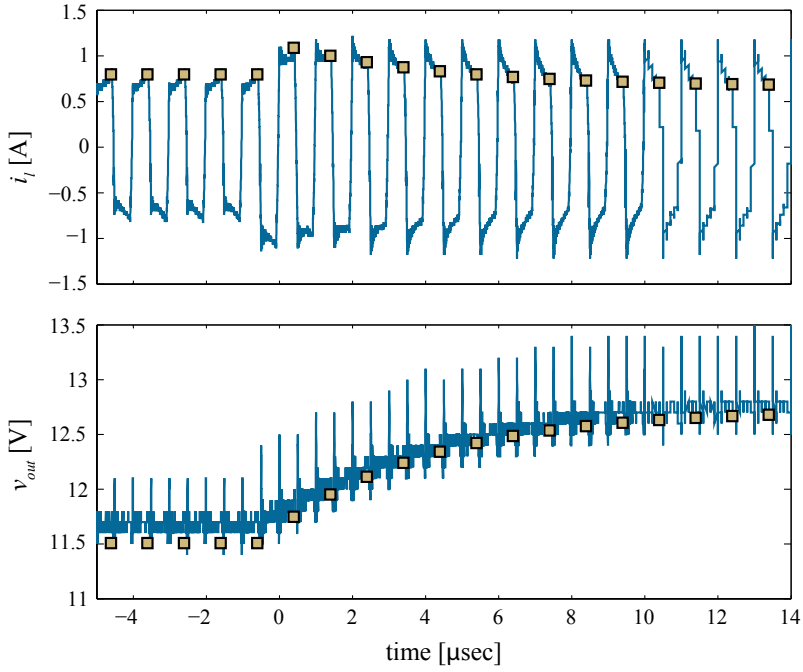
In the transient case, the full-cycle model is used, whereas the half-cycle and full-cycle models give identical results in the frequency response plots. Both figures show the converter operating at $P_{out} = 30$ W and $P_{out} = 90$ W, with output voltage set according to the proposed power-proportionality of Chapter 5. It can be seen that the proposed model is well matched to experimental results and that, as expected, dynamics other than the DC gain show very little variation between the two operating points.

Additionally, the Bode plots of Fig. 6.11 show the comparison between the proposed small-signal model, and the model obtained when the zero-voltage switching transitions are ignored, confirming the need to include C_p in the modeling process for the converter, as first proposed in [135].

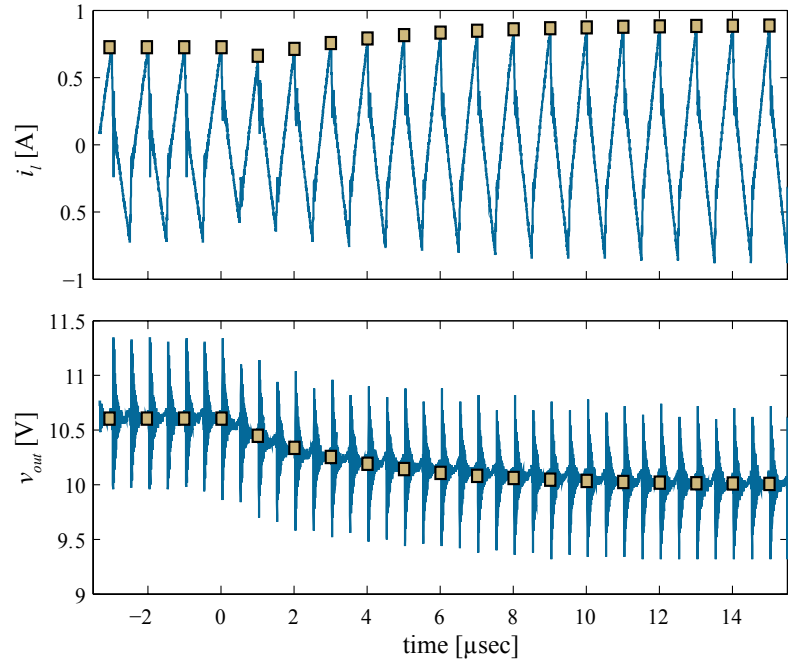
6.5 Modeling of Output Impedance

Of additional interest is the modeling of the converter response to perturbations in load. Fig. 6.12 shows example power consumption at runtime of a server running benchmarking test software, indicating the presence of many large-scale load transients which any power supply must be capable of tracking in a stable and well-behaved manner. For the purposes of DAB control design, it is useful to determine the converter output impedance in addition to the control-to-output transfer function presented previously, in order to extend the converter model to respond to changes in load.

In order to continue modeling the output impedance of the converter in the proposed closed-loop configuration, a suitable model of the open-loop converter output impedance must be derived.

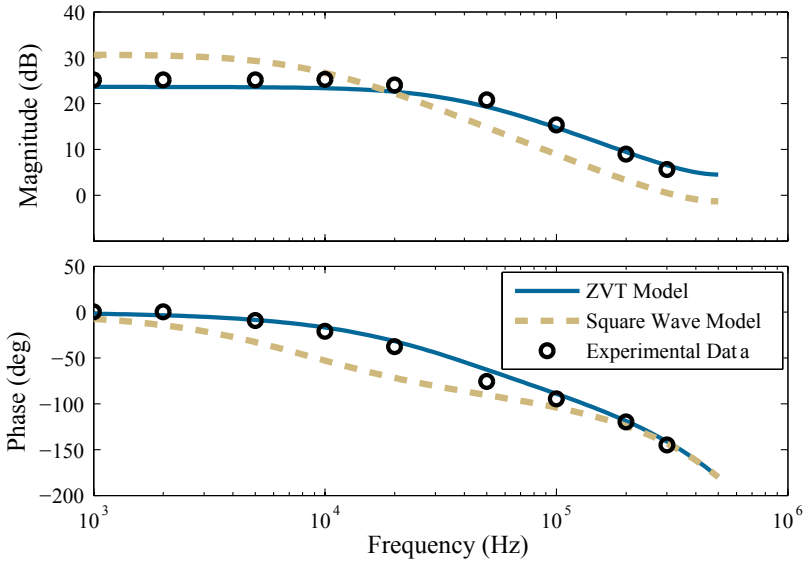


(a)

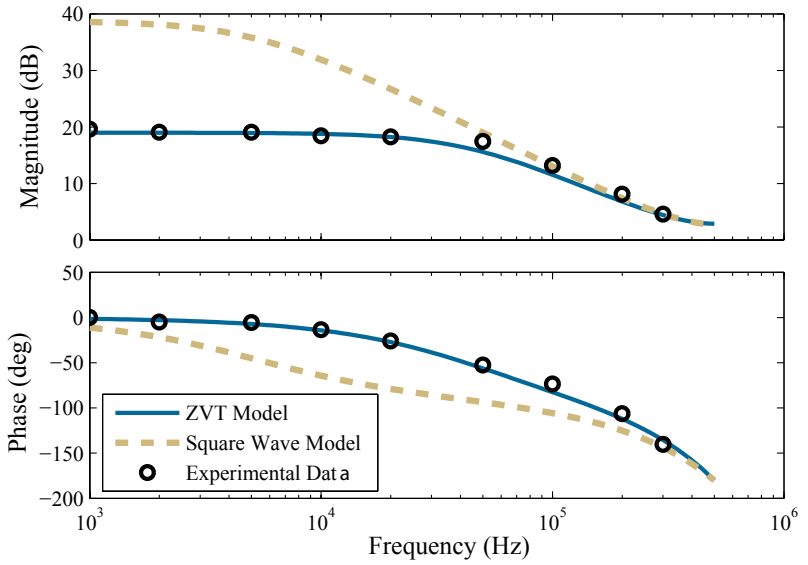


(b)

Figure 6.10: Transient response in both output voltage and inductor current to a step change in ϕ_{ab} with $R_{out} = 1.5\ \Omega$ (a) and $R_{out} = 3\ \Omega$ (b), corresponding to output powers of $P_{out} = 90$ W and $P_{out} = 30$ W, respectively. The derived sampled data model is overlaid, offset by the steady-state solution



(a)



(b)

Figure 6.11: Experimental frequency response comparison to the small-signal model developed in this work and traditional square-wave model, which ignores the effect of zero-voltage switching transitions (ZVT) on converter dynamics. Comparisons are made at both $P_{out} = 90$ W (a) and $P_{out} = 30$ W (b). Circles indicate experimentally measured data.

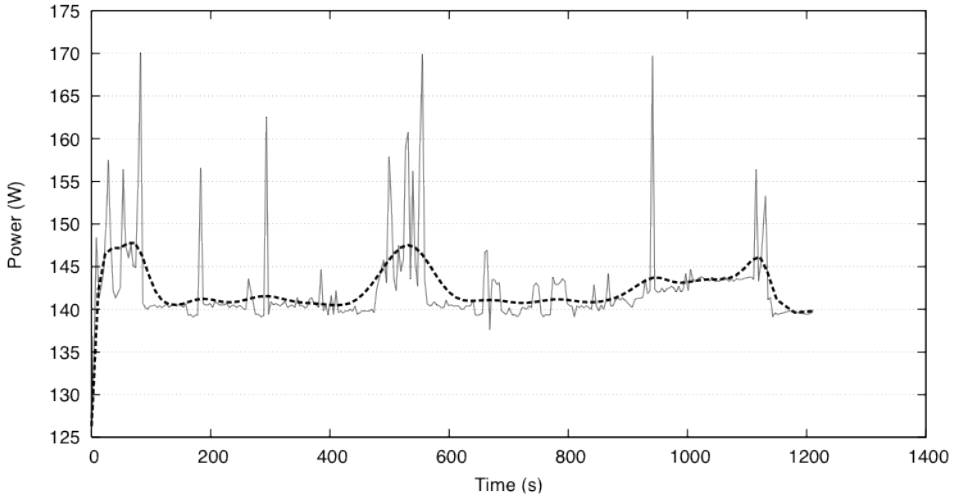
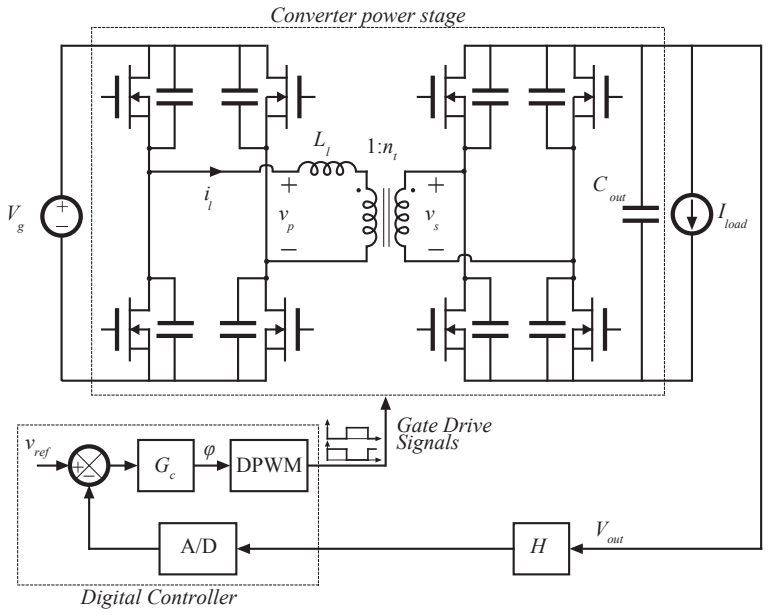


Figure 6.12: Example runtime power consumption of a high performance computing server unit during benchmarking test. Reproduced from [141].

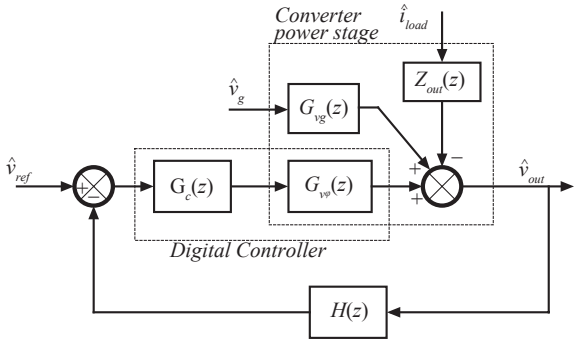
For this purpose, the closed-loop, small-signal block diagram of the DAB converter including potential disturbances in both input voltage and load current is shown in Fig. 6.13, where $G_{v\varphi}(z)$ is the control-to-output transfer function previously solved.

The open-loop output impedance of the converter, $Z_{out}(z)$ is shown modeled in discrete time. This allows the application of similar techniques to those used in the derivation of $G_{v\varphi}(z)$, and facilitates the explicit incorporation of the impact of resonant intervals on converter output impedance. Traditional models of output impedance used previously have neglected resonant intervals, resulting in a solved output impedance which is, in continuous time, $Z_{out} = -\left(sC_{out}\right)^{-1}$. This model indicates an infinite low frequency gain, i.e. any step in load current results in runaway of the output voltage. This prediction occurs due to the imbalanced output and load current having no inherent balancing mechanism in the ideal, lossless model. In [142], this problem was mitigated by including a series resistance for the tank inductor L_l which provides some compensatory behavior through conduction losses that increase when the load is unmatched to the converter output current; the resulting continuous time model demonstrated a finite low frequency gain in Z_{out}. However, the transformer volt-second balancing analysis of Section 4.3 has shown that, in addition to converter losses, converter ZVS transitions are capable of applying some counterbalancing to compensate for converter mismatches, and their effect is much more significant in determining low frequency behavior than are the conduction losses in converters operated at high frequency and low power. Unfortunately, the ZVS transitions are not easily incorporated into the continuous time models developed previously, motivating the use of the discrete time modeling methods.

However, the primary difficulty in incorporating transients in load current into the current discrete-time, small-signal power stage model lies in the asynchronous nature of load variations. Unlike variation in phase shift, which must occur exactly at the end of the t_2 subinterval, variations in load current may occur at any point in the period. This results in different state propagation in the first switching period in which the transient occurs, with the appropriate model of converter behavior exhibiting non LTI behavior. Due to this difficulty, the converter behavior is approximated by assuming that load transients occur always at the start of a switching period. This approximation



(a)



(b)

Figure 6.13: Control schematic of phase shift modulated DAB converter (a) and small-signal, discrete-time, closed-loop control block diagram of the DAB converter with closed loop transfer functions of the power stage included (b).

has inherent error, which will be addressed in the following section.

To begin solving for $Z_{out}(z)$, the original continuous time, large-signal plant model of the DAB converter presented in (6.1) is modified to include the load current as an independent variable,

$$\dot{x}(t) = A_i' x(t) + B_i V_g + P_i i_{load} \ , \tag{6.20}$$

Where $A_i' = A_i\big|_{R_{out}\to\infty}$, and for all subintervals

$$P_i = P = \begin{bmatrix} 0 \\ \frac{-1}{C_{out}} \\ 0 \end{bmatrix} \ . \tag{6.21}$$

The small signal model is then developed in a similar manner to the derivation of the state propagation matrix F previously. The solution to the state propagation within a single subinterval is updated to take the form

$$x(t) = e^{A_i t} x_0 + {A_i}^{-1} \left(e^{A_i t} - I\right) \left(B_i V_g + P_i i_{load}(t)\right) \ , \tag{6.22}$$

which can be applied simply if all A_i are invertible. If there are subintervals for which A_i is singular, the solution will still exist; this fact can be seen by examining the taylor series expansion of the matrix exponential in the term containing ${A_i}^{-1}$

$$\begin{aligned} {A_i}^{-1} \left(e^{A_i t} - I\right) &= {A_i}^{-1} \left(\sum_{k=0}^{\infty} \frac{1}{k!} {A_i}^k t^k - I \right) \\ &= {A_i}^{-1} \left(\sum_{k=1}^{\infty} \frac{1}{k!} {A_i}^k t^k \right) \\ &= \sum_{k=0}^{\infty} \frac{1}{(k+1)!} {A_i}^k t^{k+1} \ , \end{aligned}$$

which has removed the inverse from the equation. However, estimating the matrix exponential sum is an issue which requires some effort due to non-monotonic convergence with increased number of terms included. In practice, R_{out} can be made arbitrarily large, though non-infinite, to preclude

any of the matrices A_i from becoming singular and therefore allow traditional built-in routines in tools such as Matlab to solve the matrix exponential directly.

With the solution from (6.22) in hand, the discrete time model of the system with variations in i_{out} can be developed by applying the solution recursively for all six subintervals to obtain a model of the form

$$\hat{x}[n] = F\hat{x}[n-1] + K\hat{i}_{load}[n-1] \ . \tag{6.23}$$

The state propagation matrix F is unaltered from (6.8). Then, the dependence of the states on perturbations in output current, which are assummed to occur directly at $t = nT_s$, takes the form

$$K = \sum_{i=1}^{n} \left(\prod_{k=i+1}^{n} e^{A_k t_k} \right) A_i \left(e^{A_i t_i} - I \right) P \ . \tag{6.24}$$

This model can then be simplified, again applying the knowledge of the converter symmetry about the half-period, to obtain

$$\hat{x}[n] = \left(e^{A_4 t_4} e^{A_2 t_2} e^{A_1 t_1} I_{HC} \right) \hat{x}[n-1] + \left(\sum_{i=1}^{4} \left(\prod_{k=i+1}^{4} e^{A_k t_k} \right) A_i \left(e^{A_i t_i} - I \right) P \right) \hat{i}_{load}[n-1] \ . \tag{6.25}$$

The response of the converter to perturbations $\hat{v}_g$ can be solved in the same manner, with the results taking nearly the same form. The resulting full model of converter behavior in response to perturbations in any input parameter is given by

$$\begin{aligned} \hat{x}[n] = & \left(e^{A_4 t_4} e^{A_2 t_2} e^{A_1 t_1} I_{HC} \right) \hat{x}[n-1] \\ & + \left(\sum_{i=1}^{4} \left(\prod_{k=i+1}^{4} e^{A_k t_k} \right) A_i \left(e^{A_i t_i} - I \right) B_i \right) \hat{v}_g[n-1] \\ & + \left(\sum_{i=1}^{4} \left(\prod_{k=i+1}^{4} e^{A_k t_k} \right) A_i \left(e^{A_i t_i} - I \right) P \right) \hat{i}_{load}[n-1] \\ & + \left(e^{A_4 t_4} (A_2 - A_4) X_{p1} \frac{T_s}{2\pi} \right) \hat{\phi}_{ab}[n-1] \ . \end{aligned} \tag{6.26}$$

The output model is verified through simulation and experimental comparison. Results for a simulated, open-loop, 50% load step-up from 8 A to 12 A with constant control parameters are given in Fig. 6.14. The model of (6.25) is compared against the continuous time, large-signal state space model of the DAB converter constructed in Simulink, with both output voltage and

inductor current plotted. For inductor current, an absolute value is taken in order to more clearly demonstrate the significance of the discrete-time model outputs at the half-cycle.

To again verify the necessity of including ZVS transitions explicitly in modeling DAB behavior in the proposed application, bode plots of Z_{out} are compared for the proposed model, the simplified linear model $Z_{out} = -1/sC_{out}$ and the continuous time model proposed in [142] with $R_L = 1\Omega$ in Fig. 6.15. Note that while all models consider high frequency dynamics defined by the output capacitance, each results in varying pole locations and low frequency impedances of the converter.

Experimental verification has been completed using the same prototype converter detailed previously, but at an operating point with reduced voltage and power. In Fig. 6.16, the proposed model is verified experimentally, for operation with $V_g = 50\ V$ input, through the use of an open loop 2.5-3.5 A transient load step generated by a BK Precision 8512 electronic load. The realized current step is non-instantaneous, with the rate limited current waveform shown in the bottom plots of Fig. 6.16. This load current profile is then used to feed the discrete time small signal model defined by (6.25) and the output is compared to experimental waveforms in Fig. 6.16 for both the full step and a zoomed portion of the transient. The excellent agreement of both high and low frequency behaviors indicates both the validity of the proposed model and the errant nature of alternative models in Fig. 6.15, both of which predict much larger changes in V_{out} from their larger low frequency gain.

6.5.1 Discrete Time Modeling of Asynchronous Disturbances

The state space model derived in the previous section was simplified through the assumption that any step in load current occurred exactly at the start of a switching period, synchronously with a time instance in the discrete time model. In order to account for the possibility of a step change in load current occurring at an arbitrary time instance within the switching cycle, an additional small-signal state vector is used, X_{dev} which models the deviation in states generated in the time between the initial load current step and the following sampling instance. If the load step occurs

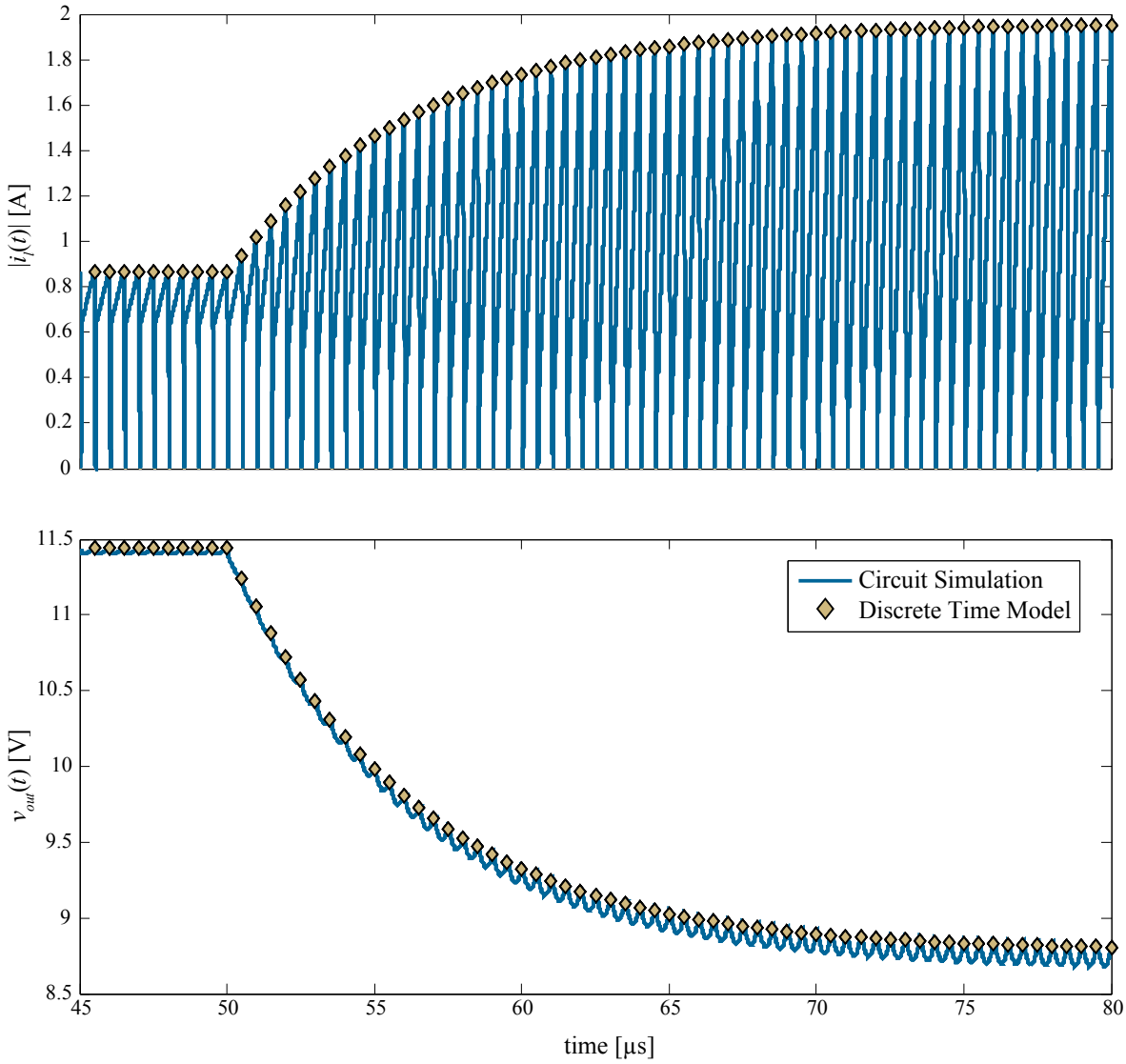


Figure 6.14: Comparison of small-signal, discrete-time model of DAB output impedance to the large-signal state space model of the converter. output voltage and inductor current states are shown, with the absolute value of the latter plotted due to its anti-symmetry about the half cycle.

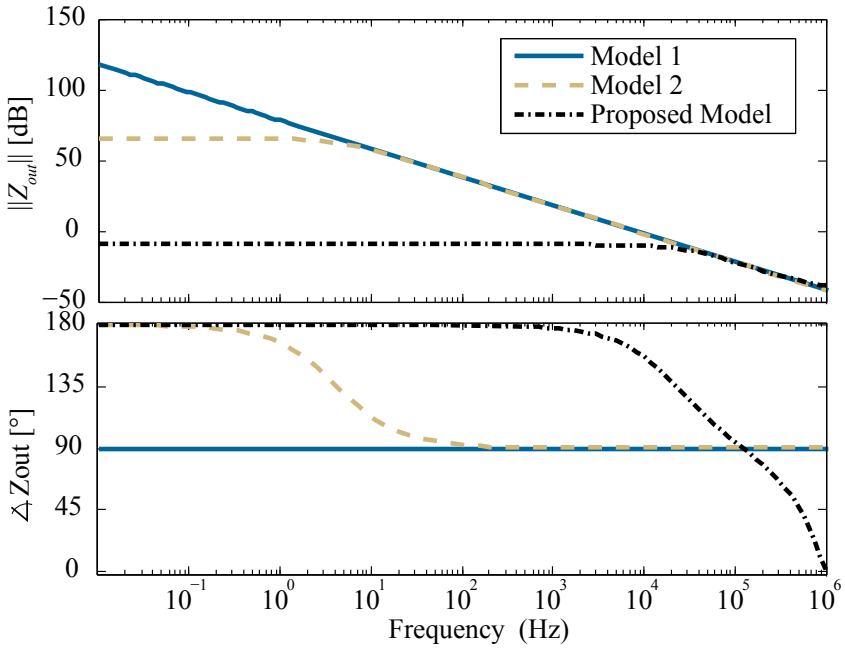


Figure 6.15: Bode plots of DAB output impedance solved by including nothing but output capacitance (Model 1), the effect of series inductor resistance (Model 2) [142] and the full inclusion of ZVS intervals in the proposed discrete time model.

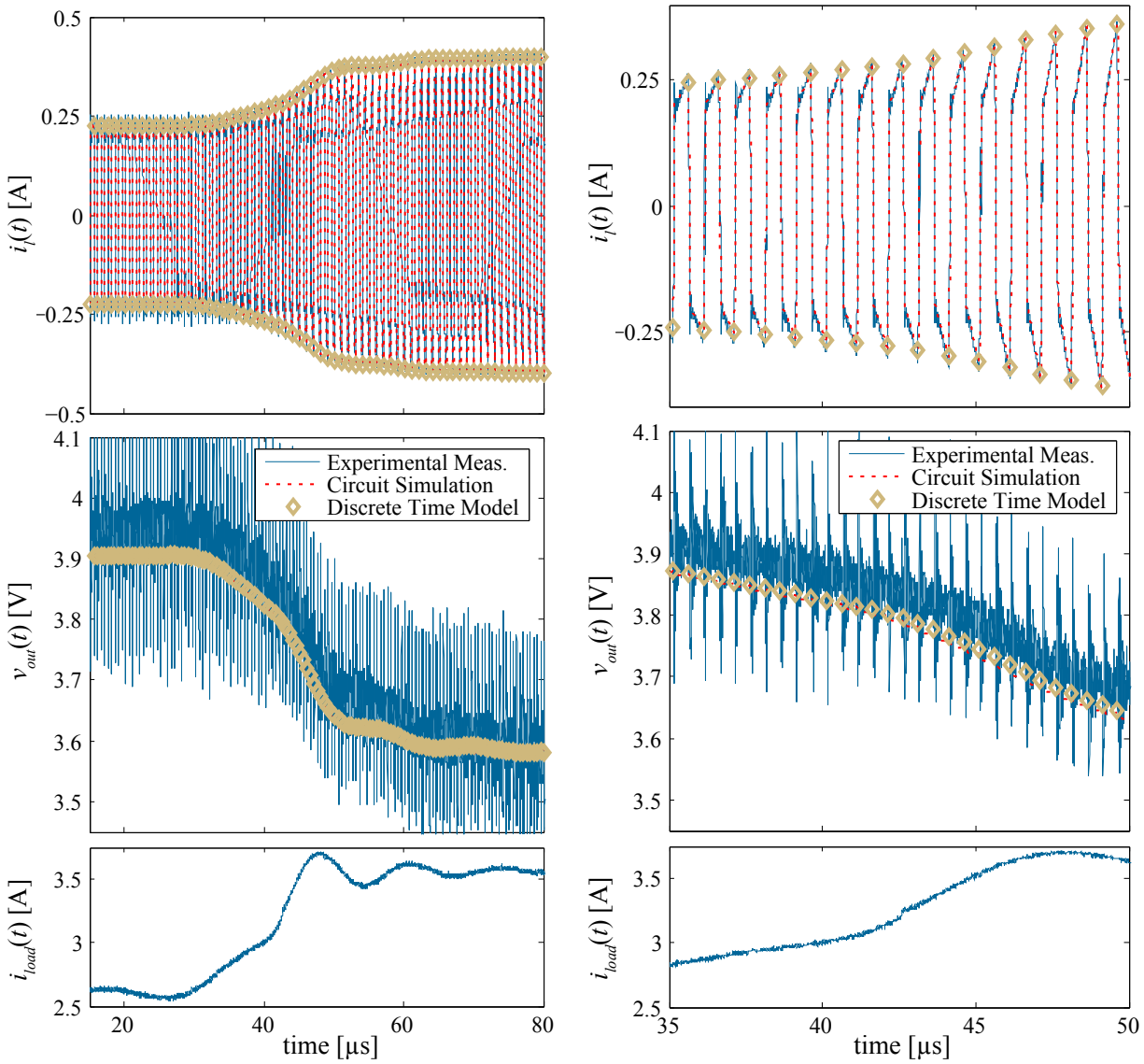


Figure 6.16: Discrete time DAB output impedance model comparison to experimental and large-signal, nonlinear state space simulations in Simulink for a load step from 2.5-3.5 A. The same experiment is used to generate (a) and (b), with the latter being a zoomed segment around the load step.

synchronously with a sampling instance, $X_{dev} = 0$. Otherwise, for a step change of magnitude Δi_{out} occurring at time t_{step} within the switching cycle, $0 < t_{step} < T_s/2$, the state deviation is given by

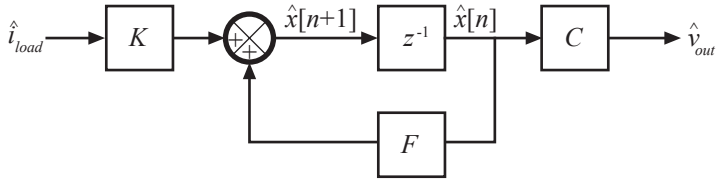
$$X_{dev} = \sum_{i=1}^{n} \left(\prod_{k=i+1}^{n} e^{A_k t_k^*} \right) A_i \left(e^{A_i t_i^*} - I \right) P \Delta i_{load} \ , \tag{6.27}$$

where

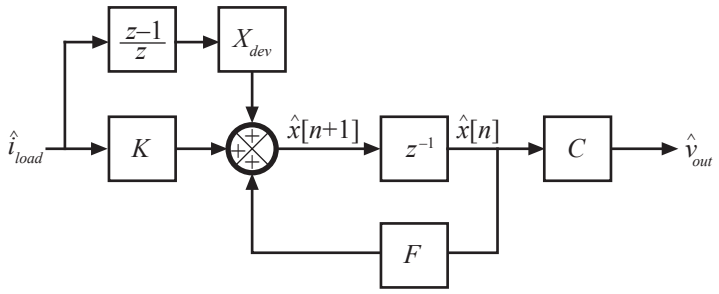
$$t_i^* = \begin{cases} 0, & \text{if } t_{step} > \sum_{0}^{i} t_i \\ -t_{step} + \sum_{0}^{i} t_i, & \text{if } \sum_{0}^{i-1} t_i < t_{step} < \sum_{0}^{i} t_i \\ t_i, & \text{otherwise} \end{cases} \ . \tag{6.28}$$

By adding X_{dev} to the perturbed states $\hat{x}$, the discrete time state space model can be corrected to include the effects of asynchronous perturbations in load current. Beginning with the traditional discrete time state space block diagram of Fig. 6.17(a), the correction vector X_{dev} is added at the load step instance to produce the modified model shown in Fig. 6.17(b). To allow the implementation of this model using only simple state space and discrete transfer function blocks in, e.g. a simulator such as Matlab/Simulink, the model is rearranged to the form shown in Fig. 6.17(c) which is functionally equivalent to (b) and results in simplified derivation of overall transfer functions.

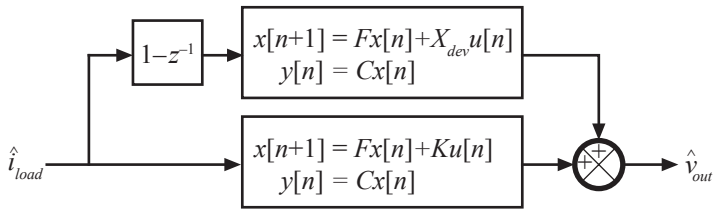
The results of the modeled output impedance are compared to large-signal, nonlinear state space simulations in Fig. 6.18 for the prototype converter detailed previously. In these simulations, the output capacitance has been reduced to $C_{out} = 5$ pF to shorten transient duration. An ideal load step from 2.5-3.5 A is simulated with the step occurring mid-way between sampling instances. Including the correction from X_{dev} correctly modifies the high frequency behavior of the discrete time model for load steps occurring asynchronously to the sampling instances.



(a)



(b)



(c)

Figure 6.17: Traditional discrete time state space model of $Z_{out}(z)$ a. The modified state space model which takes into account state deviation due to asynchronous disturbances is given in b and simplified in c to include only traditional state space and transfer function blocks.

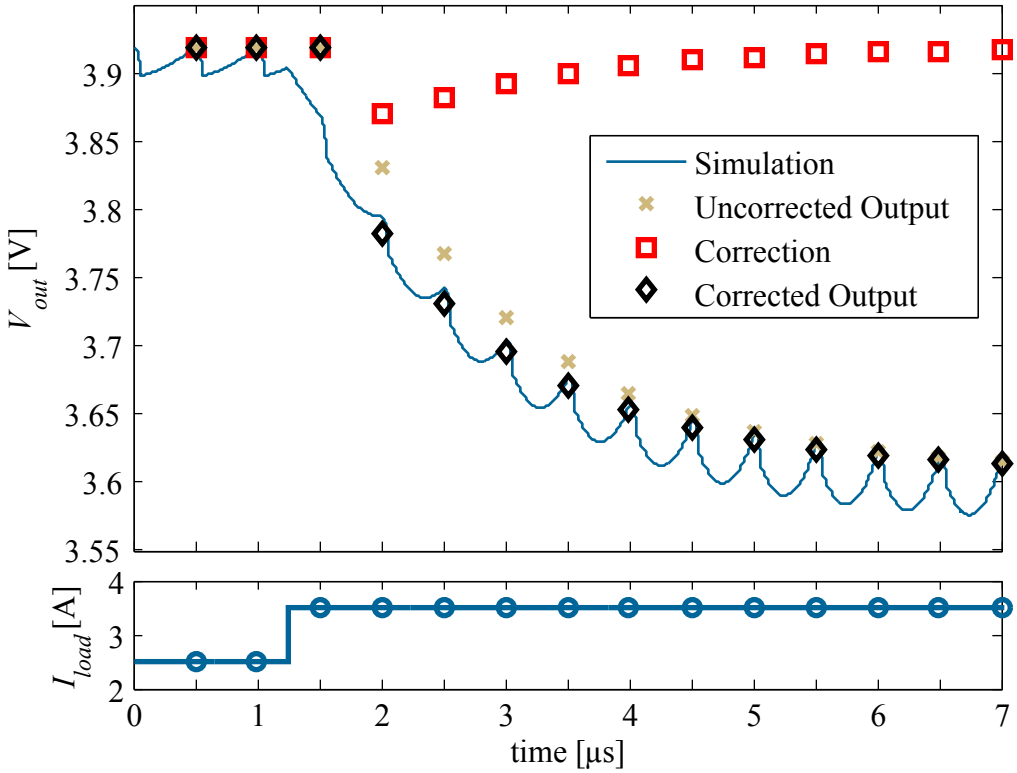


Figure 6.18: Simulation results demonstrating the error resulting from using a discrete time model with disturbances which are asynchronous to the sampling interval and the ability of the proposed model in Fig. 6.17(c) which includes the state deviation X_{dev} to correct for this error.

Summary

In Chapter 5, an output voltage control trajectory was proposed which led to near-optimal efficiency of the converter across all operating points while maintaining very simple steady state control. In order to determine the true value of the proposed control method, the dynamic characteristics of the converter on the proposed trajectory are considered in this chapter. A discrete-time, small-signal model is developed for use in the design and control of the DAB converter, operating in steady-state on the proposed trajectory. The model is verified to be accurate through experimental tests of the dynamic response of the converter across a full range of load conditions and associated operating modes. With its accuracy verified, the model is used to determine the nature of the variation in converter dynamics on the proposed trajectory, and comparison is made to the variation which occurs on a constant output voltage trajectory. The resulting analysis shows that while traditional, constant output voltage control of the DAB leads to a converter power stage open-loop frequency response which varies heavily with operating power level, the proposed trajectory exhibits nearly constant dynamics across the full range of output powers. The lack of variation in converter dynamics permits the aggressive design of a single, constant, linear compensator which will give favorable closed loop converter response across all operating points, without need for overly conservative or increasingly complicated control approaches.

The DAB design analysis presented in this thesis therefore present a method of constructing and operating a DAB converter which is well behaved from many different viewpoints. Through power stage design, component selection, and implementation of accurate modulation signals, the converter is made to operate with low RMS currents and full ZVS of all devices at a single nominal operating point. This results in highly efficient power conversion, while additionally avoiding stability and EMI issues which may arise if hard switching is incurred. Through additional analysis across a wide range of output powers, a control trajectory is developed which extends these favorable characteristics to all operating points. Finally, the dynamic behavior of the converter is verified to be simple and nearly constant on the proposed trajectory. The converter behavior

is therefore excellent in both steady-state and dynamic conditions, and the control requirements remain exceedingly simple in both senses as well.

Chapter 7

Conclusions and Future Work

Motivated by the need for a power converter which exhibits high efficiency, high step-down, low power, and small footprint in modern data centers, this thesis details the analysis, design, control, and implementation of a zero-voltage switching quasi-resonant dual active bridge converter. Through careful circuit analysis, it is discovered that current circuit analysis approaches for this class of power converters are insufficient for the application requirements due to the widespread neglect of ZVS transitions present in prior art. Instead, previously established techniques in steady-state and dynamic converter analysis are applied to the application-specified DAB to extend converter operating analysis to include the effects of significant ZVS transitions. In the process, interesting characteristics of the ZVS transitions are discovered, including the nature of the nonlinear capacitance involved in ZVS transitions and the inherent volt-second balancing of tank magnetics present when such transitions become significant. New analysis techniques are developed to characterize the nature of these characteristics. Separately, from the resulting converter models, techniques for the component selection, converter design, steady-state operating trajectory, and dynamic control are proposed. These techniques permit favorable converter behavior in terms of both steady-state and dynamic behavior, while maintaining simple, low-cost control design and implementation. Original contributions of the thesis are summarized as follows.

7.0.2 State Plane Analysis of DAB Converter

Motivated by the simplified, linear analysis of Chapter 2, a rough outline of the converter design constraints is constructed. Included in this specification are motivations for operating the DAB with high switching frequency and relatively low output power; this is a unique design space for the converter which has been traditionally implemented in relatively low frequency and higher power applications. These constraints combine to produce a converter in which ZVS transitions significantly affect converter operation; low power levels slow the speed with which ZVS can be obtained, while high switching frequencies cause resonant transition times to constitute an increasingly significant portion of the switching period.

Because the resonant ZVS transition intervals are expected to be significant in the intended application, the traditional linear converter analysis is refined through the use of state plane analysis techniques in Chapter 3. This analysis approach permits the direct inclusion of all resonant intervals in converter analysis, and yields solutions for converter steady-state operational characteristics with ZVS accounted for directly.

The resulting converter solution can be applied with benefit to multiple ends. First, the direct analysis of ZVS intervals allows formal definition of the ZVS boundary in the converter and how it relates to output power levels. Second, the ZVS interval inclusion yields values for the resonant interval durations, which can be used to program optimal dead times in gate drive waveforms. To achieve precise dead time regulation in gate drive waveforms, a low-cost, simple delay line modulator is presented in Appendix B. Finally, the converter solution yields predicted values for average and RMS currents throughout the converter. Combined with equations for the power losses throughout the converter, this permits the development of the loss model presented in Chapter 3, which is used to predict the converter losses and efficiency at a given operating point, for a given converter design.

7.0.3 DAB Design and Component Selection

Based on the developed loss model, guidelines are proposed which yield a converter design exhibiting optimal efficiency at a single operating power. Design parameters which are subject to optimization include primary and secondary transistor device selection and tank inductance value.

The proposed single-point optimization dictates that the converter tank inductance be selected to place the ZVS boundary directly at the operating power. This action permits the maintenance of ZVS switching of all devices, without the significant efficiency penalties incurred when hard switching the high voltage primary transistors, while simultaneously minimizing the incurred RMC current increase associated with an increased tank inductance. When solved, the ZVS boundary of the converter is defined by the inductor stored energy which is required to provide the necessary capacitor energy to primary devices during a full ZVS transition. Therefore, the optimal inductance is a function of primary device selection as well as converter operating point parameters.

The selection of both primary and secondary devices is undertaken with the motivation of minimizing the losses which they exhibit at the specified operating power. Based on their influence on converter losses in the proposed loss model, transistor device parasitics are assessed to ascertain their importance in device selection. In particular, the tradeoff between stored charge and on-resistance is evaluated to determine how to best maximize power stage efficiency through device selection. The resulting analysis in Chapter 3 dictates that primary-side transistors be selected with a minimum of stored charge to reduce the ZVS interval duration and therefore the RMS currents throughout the converter, while devices on the high-current secondary be selected to obtain minimum on-resistance and therefore minimum conduction losses resulting from the RMS currents.

7.0.4 Output Voltage Trajectory Control

In order to extend converter operation beyond a single operating point, a new method of extending ZVS range below the traditional ZVS boundary is proposed. Based on the lack of

requirements for tight output voltage regulation in the application, the converter is operated in an unregulated manner; here the term "unregulated" implies that the output voltage is adjusted in closed loop in order to maximize converter efficiency, rather than being controlled to a fixed reference value.

To ascertain the proper trajectory for the adjustment of the output voltage in order to maximize efficiency across all operating powers, the state plane analysis of Chapter 3 which was employed at a single operating point, is extended in Chapter 5 to four different operating modes of the converter which together span the full range of output powers and voltages at which the converter may operate. The developed loss models are similarly extended to the full range of operating points, yielding a converter loss model which is able to predict the power stage efficiency for all output powers and output voltages.

Based on the analytical efficiency predictions, a steady-state control trajectory by which the output voltage should be set in order to maximize efficiency across all operating powers is solved numerically. A similar, though simplified trajectory is proposed and implemented experimentally which exhibits nearly the same efficiency as the optimal trajectory, but has favorable characteristics in terms of the simplicity of sensing and control implementation.

7.0.5 DAB Discrete Time Modeling

The proposed output voltage trajectory which leads to excellent steady-state behavior of the converter is analyzed in terms of dynamic behavior in Chapter 6. Discrete time modeling techniques are applied to the converter with primary ZVS transitions included in the converter state description. The resulting model, which assumes operation at or below the ZVS boundary of the converter, is simplified through the application of half-cycle control, which permits control action at twice the converter switching frequency. Converter control-to-output transfer functions are derived in simple, closed-form notation.

The transfer functions are then used to assess converter dynamic behavior on the proposed trajectory from Chapter 5. The results confirm that the proposed trajectory exhibits favorable

characteristics in terms of dynamic behaviors as well. Converter frequency response is kept nearly constant across the full range of operating powers, permitting very simple compensation of closed-loop control to achieve well-regulated converter responses.

Thus, the proposed control trajectory for the DAB converter is shown to exhibit high efficiency and simple control in both steady-state and dynamic conditions across the full range of output powers.

7.0.6 Resonant Transition Details

Two additional contributions stemmed from the careful analysis of DAB ZVS transitions which was required in this work. Both are covered in detail in Chapter 4.

Nonlinear Capacitor Circuit Modeling

In order to incorporate its effects in traditional circuit analysis techniques, a method for the derivation of linear equivalents to the highly nonlinear output capacitance of switching devices is derived. Because the nonlinearity of the capacitance causes a variation in value with applied transistor voltage, substitution of any linear equivalent will necessarily result in a loss of information. Therefore, a multitude of linear equivalents are derived, each of which will exhibit correct circuit behavior only in terms of a single parameter, e.g. capacitor charge, energy, or ZVS time.

Automatic Volt-Second Balancing of ZVS Transitions

It is additionally found that the nature of the resonant transitions in soft switched converters is such that any offset current present in supposedly-AC converter magnetics will cause the speeding up or slowing down of voltage waveforms during ZVS transitions. This inherent feedback applies additional volt-seconds to the magnetic devices which counteract the initial offset. This behavior had been previously observed, but not analyzed. Chapter 4 details the linearized analysis of the behavior which may be used to discern the amount of current offset which will result from a specified amount of applied DC volt-seconds, as may occur with errors in switch modulation waveforms.

7.1 Future Work

In addition to the latter two contributions which were derived from the employed DAB analysis and testing techniques, further research directions have been identified in the process of completing this thesis. A selection of additional research directions are presented here, some of which have been broached through initial results, while others remain entirely unaddressed at the time of this thesis.

7.1.1 Automatic Dead Time Control

In the proposed application, a carefully designed output voltage control trajectory permits the converter to operate with favorable characteristics across all operating points, while maintaining a nearly constant resonant ZVS interval duration. Fortunately, the use of a constant primary dead time removes a significant complexity in control implementation. However, in applications of the DAB for which variation in output voltage is not permissible, an alternate means of regulating the dead time interval is necessary.

The importance of precisely matching the modulation waveforms to the resonant ZVS time was addressed in Section 3.5 and diagrammed in Fig. 3.18 for the case of operation at the ZVS boundary. When operating at or below this boundary, any deviation from ideal modulation waveforms results in an increased voltage hard switched on all primary devices. When operating above the ZVS boundary, any decrease below ideal dead times results in hard switching, whereas any increase above the ideal dead times yields a converter interval in which the full input current is conducted through antiparallel or body diodes rather than the transistor itself, with associated increase in conduction losses. Thus, primary dead time intervals must be precisely calibrated to their optimal values to maintain converter efficiency.

It is possible to track optimal dead times through direct sensing of the ZVS waveforms during converter operation. Such an approach would require either very high frequency voltage sensing, or prior knowledge of the resonant transition characteristics. The prior results in significant increase

in cost and complexity, while the latter requires extensive precalibration due to the potential for variation in the values of resonant transition components.

An approach has been considered, and initial results taken, which allows for sensorless dead time optimization similar to [143] for duty cycle controlled converters, but with significant differences to adapt to phase shifted converters. The optimization operates under the assumption of a successfully designed control loop which regulates the output voltage in closed loop through adjustment of the converter phase shift. This manner of regulated, constant-voltage phase-shift modulation is a standard control method in traditional DAB designs. For the proposed method, it is assumed that any changes in operating characteristics, e.g. through variations in load conditions, occur much slower than the proposed optimization, and that the converter voltage regulation occurs much faster. Under these conditions, it is warranted to analyze any dead time optimization loop as quasi-static with respect to the output voltage control.

7.1.1.1 Sensorless Characterization of Switching Behavior

In order to establish a criterion for dynamic dead time optimization, the relationship between primary-side dead time t_1 and phase shift of the converter Φ_{ab} is considered in Fig. 7.1 for a nominal operating point and three cases of a perturbation Δt_1 in converter dead time interval t_1. In Fig. 7.1(a), a partial waveform of inductor voltage under nominal ZVS operation is shown, with properly set converter dead time and phase shift set in closed loop to obtain the specified output voltage. In Fig. 7.1(b)-Fig. 7.1(d), variations in dead time interval t_1 cause the controller to adjust Φ_{ab} in order to maintain the set output voltage under the current load conditions. To do so, the controller must adjust the phase shift so that additional volt-seconds are applied to the inductor when the perturbation Δt_1 causes a reduction in them, or vice versa.

In Fig. 7.1(b), t_1 is set to the correct value prior to perturbation, and the converter operates well above the ZVS boundary. A positive perturbation Δt_1 then causes an increase in dead time; however, as ZVS has already been obtained and excess energy remains in the inductor because the converter is above the ZVS boundary, this additional dead time only results in diode conduction,

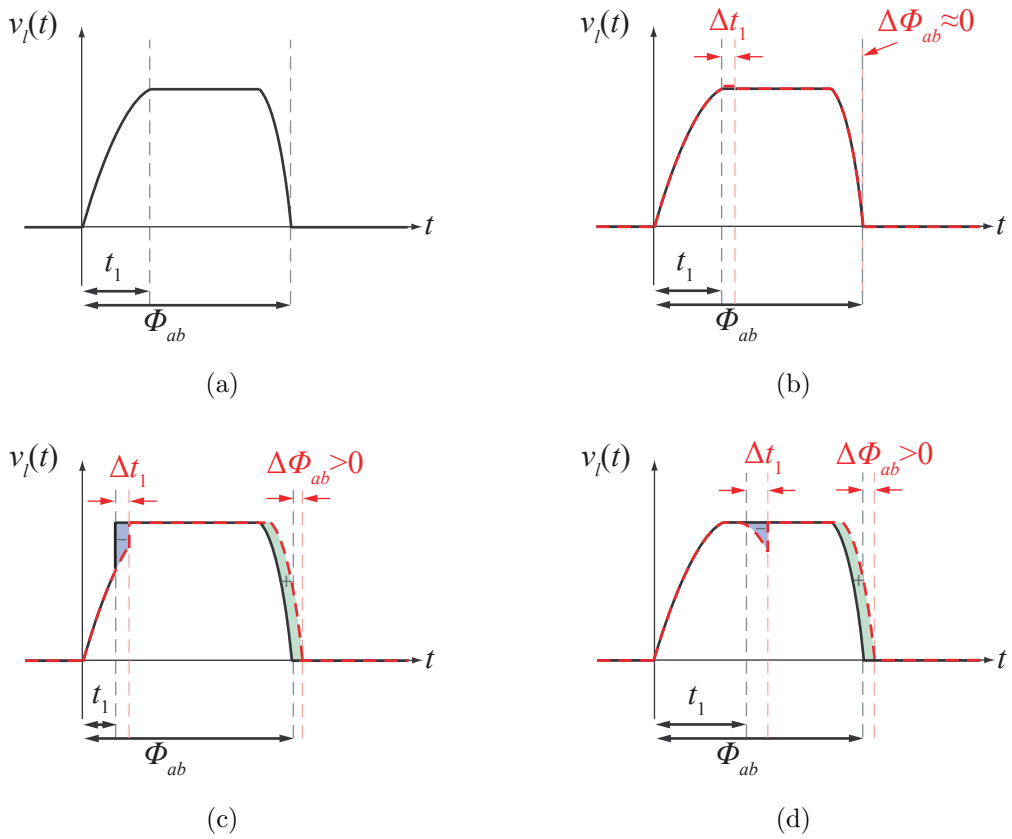


Figure 7.1: Partial waveforms of inductor applied volt-seconds in the DAB converter for nominal ZVS operation (a), and perturbations in primary dead time Δt_1 when the steady-state when t_1 is at its nominal value (b), too short (c), or too large (d).

rather than conduction through the MOSFET channel. Though there is a small additional voltage applied to the inductor during this interval due to the diode drop, this value is insignificant in comparison to the high voltage at the input, and therefore leads to little change in v_l. The closed-loop controller therefore does not need to make a noticeable adjustment to the phase shift, $\Delta\Phi_{ab} \approx 0$ to maintain output voltage regulation.

In Fig. 7.1(c), t_1 is set below its optimal value, resulting in unnecessary hard switching of primary devices. When a perturbation Δt_1 is introduced, the resonant period is extended and the converter moves closer to ZVS. However, the additional resonant time results in fewer applied volt-seconds to the tank inductor compared to the case where the converter is hard-switched earlier, and the closed-loop controller must increase Φ_{ab} in response to maintain constant output voltage.

Finally, in Fig. 7.1(d), t_1 is set to a value much larger than the ideal dead time, resulting in steady state diode conduction of duration so long that the inductor energy is completely depleted. At this point, if t_1 is increased further through a perturbation, the resonance responsible for obtaining ZVS on the primary will reverse direction and the primary voltage will begin to resonate away from ZVS. As it is allowed to do so, it again results in fewer volt-seconds applied to the tank inductor which must be compensated for by the voltage controller.

Aggregating these characteristics, the optimal dead time of the DAB converter can be discerned by examining the relationship between δt_1 and $\delta\Phi_{ab}$. If a perturbation δt_1 results in a significant phase response $\delta\Phi_{ab} > 0$, then the steady-state value of t_1 must be as represented in either Fig. 7.1(c) or Fig. 7.1(d) i.e., far from the ZVS value. If, however, the perturbation results in $\delta\Phi_{ab} \approx 0$, the converter is in the ZVS region, but possibly exhibits significant diode conduction. Therefore, if a second control loop, slower than the voltage loop, can be designed which searches for the minimum value of t_1 such that δt_1 results in $\delta\Phi_{ab} \approx 0$, then the converter can be forced to the optimal dead time without sensing dead time waveforms.

The relationship between the value of steady-state t_1 and Φ_{ab} for varying output powers is shown in the curves of Fig. 7.2. The shape of the t_1-Φ_{ab} curves is as predicted. Considering the slope of the curve, $d\Phi_{ab}/dt_1$ is positive outside of the ZVS range, but nearly zero everywhere in the

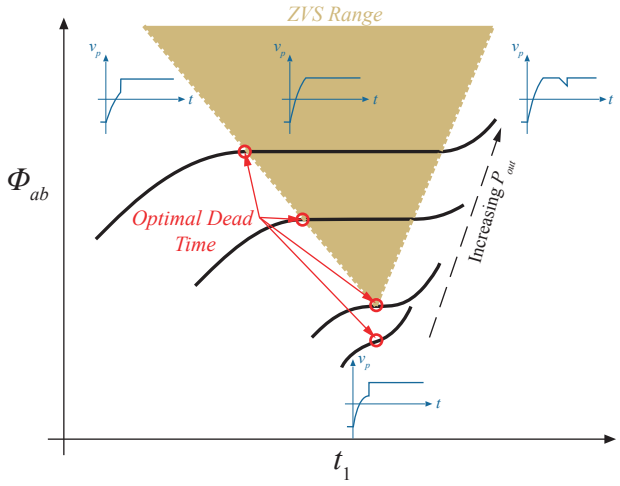


Figure 7.2: Plot of the relation between primary dead time and converter phase shift for varying values of converter output power level. Blue subplots give example waveforms of $v_p(t)$ at various points on the plot. Optimal selections of t_1 obtain ZVS – or have a minimum of hard switching below the ZVS bound – with the minimum phase shift possible to minimize diode conduction.

region where ZVS is obtained. Further, the concavity of the curves, $d^2\Phi_{ab}/dt_1{}^2$ is positive in the region where t_1 is larger than the optimal value, and negative below the optimal ZVS time.

For the bottom curve in Fig. 7.2, the output power level is below the ZVS boundary. Because ZVS is unobtainable for this mode of operation, the dead time optimization should seek out the operating point with the minimum amount of hard switching. This point now occurs at the value of t_1 at which $d\Phi_{ab}/dt_1$ reaches a minimum. Neglecting the nonlinearity of the resonant capacitance, this value would occur at a constant dead time equal to one-quarter of the resonant period of L_l and C_p for all points below the ZVS boundary, if $V_{out} = n_t V_g$. If output voltage is set differently, or if the nonlinearity in output capacitance of primary devices is considered, the value of optimal t_1 will differ slightly with power level, but will always occur at the peak of the voltage waveform resonance.

7.1.1.2 Dead Time Regulation

From the analysis of the previous section, a controller can be conceptualized which is capable of automatically searching out the optimal primary dead time. An example architecture for such a controller is given in Fig. 7.3, where the "Min Slope Tracking" block represents an algorithmic controller. This controller attempts to force the value of $\alpha = \omega_0 t_1$ to its minimum value such that the value of $d\Phi_{ab}/dt_1$ takes its minimum value for the given power level. In order to ascertain the correct direction for adjustment of t_1, the controller may also calculate the value of $d^2\Phi_{ab}/dt_1{}^2$, noting that if this value is greater than zero t_1 needs to be decreased, whereas a negative value indicates t_1 needs to be increased.

Implementations of such a controller may vary based on whether the dead time optimization needs to be implemented at run-time, or whether it is desired to use the approach as a precalibration routine through which the controller determines optimal deadtimes for all operating points prior to deployment. If design-time implementation is considered, a simple sweep of dead time values at a range of power levels would be capable of determining the $t_1 - \Phi_{ab}$ trajectory which includes only optimal operating points. These values could then be referenced in a lookup table when the

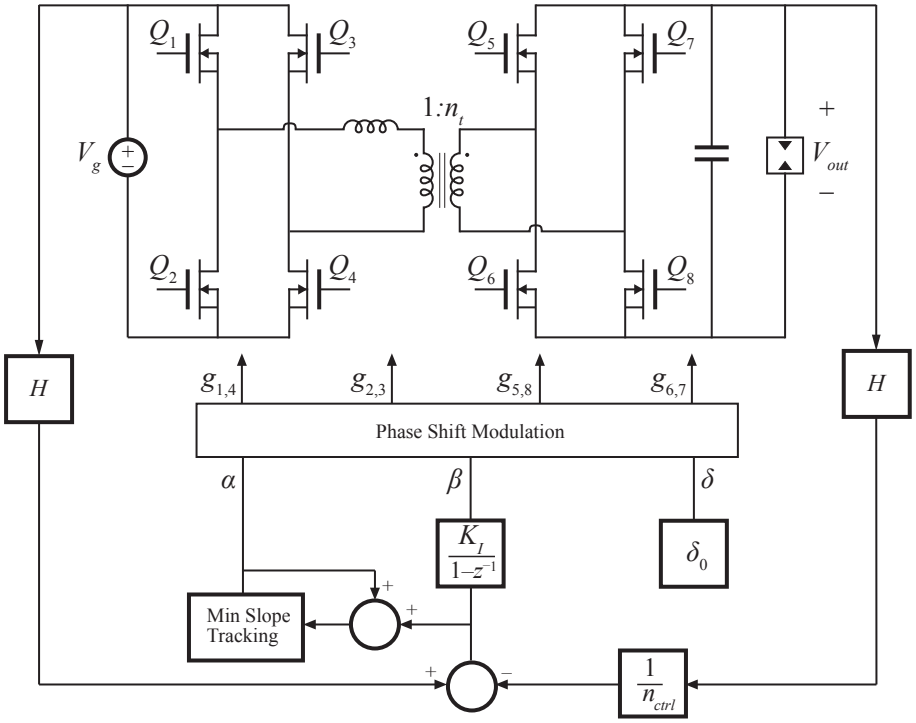


Figure 7.3: Example controller implementation for sensorless dead time optimization. The voltage loop compensator is shown, as an example, as a discrete integral compensator with gain K_I. The optimization block then adjusts the primary dead time through α and monitors the resulting closed-loop steady-state phase shift, given in normalized form by $\alpha + \beta$, in order to minimize $d\Phi_{ab}/dt_1$.

system is deployed. If run-time optimization is necessary, similar occasional sweeps or algorithmic approaches such as the continuous or occasional perturbation of t_1 and observation of resulting changes in phase shift may be used.

The largest issue with a continuous, run-time tracking of the optimal dead time is the necessity of computing $d^2\Phi_{ab}/dt_1{}^2$ in order to determine the direction of t_1 adjustment. In any real system, the derivative operator is inherently susceptible to noise. In order to effectively implement a second-order differentiation, extremely low-noise circuitry and very high resolution modulation are necessary. In attempted implementations constructed at the time of this thesis, these factors have limited the success of run-time optimization attempts.

7.1.1.3 Experimental Results

Initial experimentation has been completed using the all-silicon prototype DAB converter as a test circuit, with the same Xilinx Virtex 4 FPGA comprising the control circuitry. To allow nondestructive hard switching, the converter is run with only 50 V input and 3.8 V output, with output power set to place the converter at the ZVS boundary. Fig. 7.4 shows the experimentally measured values for timing intervals corresponding to the phase shift and primary dead time, as reported by the FPGA through Xlinix Chipscope software. The primary dead time t_1 is swept from 10 ns to 100 ns and back down, with a closed-loop integral compensator setting the duration of interval t_2 in order to maintain the output voltage. The resulting closed loop relation between primary dead time t_1 and total phase shift, shown by t_1+t_2, closely follows the predicted relationship from the previous analysis.

Examining Fig. 7.4, the smallest value of t_1 for which minimum slope is achieved appears to be approximately $t_1 \approx 60$ ns. Converter waveforms at the same 50 V operating point are given in Fig. 7.5 with $t_1 = 60$ ns manually set, showing that ZVS is indeed achieved at this optimal dead time. Because the output power is set to place the converter at the ZVS boundary, the minimum slope occurs at a single point, and any increase or decrease in t_1 results in additional hard switching.

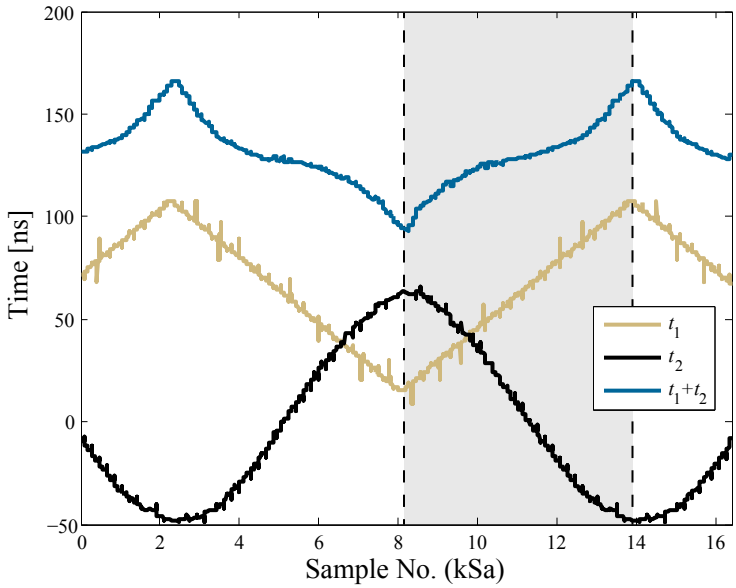


Figure 7.4: Experimental measurements, as reported by Xilinx Chipscope, for primary dead time t_1, inductor current ramping interval t_2, and their sum. Because secondary dead time is constant, the waveshape of $t_1 + t_2$ is the same as that of Φ_{ab}. The shaded region indicates one full sweep of values for t_1.

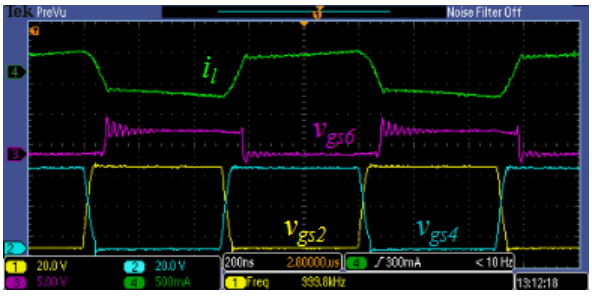


Figure 7.5: Waveforms during converter operation with $t_1 = 60$ ns, which is approximately the predicted optimal value from Fig. 7.4.

From the data in Fig. 7.4, the slope and concavity of the $t_1 - \Phi_{ab}$ relationship are calculated onboard the FPGA and their values over the same t_1 sweep are plotted in Fig. 7.6. Although the expected relationship is apparent in Fig. 7.4, the measurement noise present on the signal results in indiscernible behavior of the differentiated signals. Clearly, without extensive filtering, the current implementation of the slope and concavity calculations prohibit the implementation of a stable, well-behaved dead time optimization loop in real time.

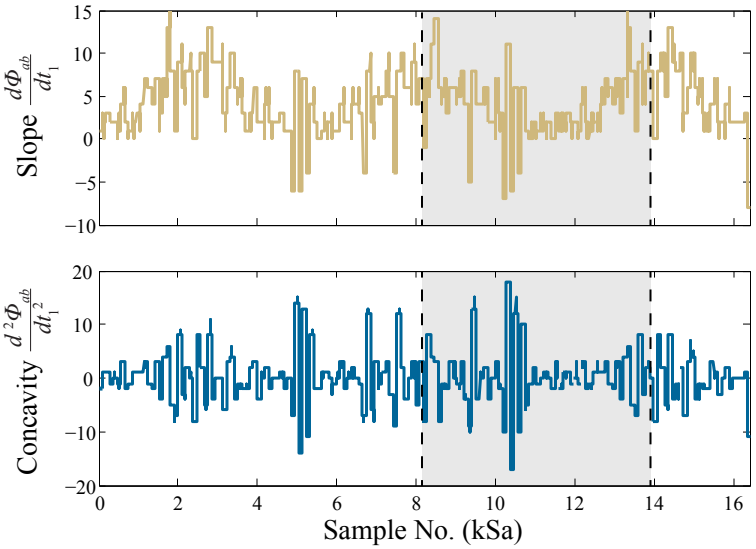


Figure 7.6: Experimental measurements, as reported by Xilinx Chipscope, for the slope $d\Phi_{ab}/dt_1$ and concavity $d^2\Phi_{ab}/dt_1{}^2$ of the $t_1 - \Phi_{ab}$ relationship. The shaded region indicates one full sweep of values for t_1.

At a second operating point, converter output power is increased to place operation well above the ZVS boundary. For this new setup, the experimental $t_1 - \Phi_{ab}$ relationship is measured directly using an oscilloscope, with results reported in Fig. 7.7. In contrast to the characteristic shown in Fig. 7.5, there is a significant portion of the curve for which nearly zero slope is obtained; this is due to the higher operating power and the presence of significant diode conduction when t_1 is increased beyond its optimal value.

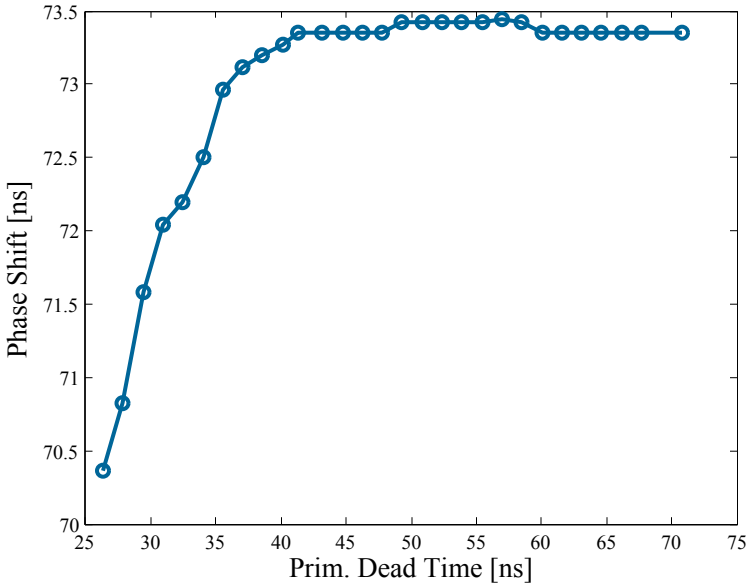


Figure 7.7: Experimental measurements, taken from oscilloscope waveforms, of $t_1 - \Phi_{ab}$ relationship for the converter operating well above the ZVS boundary.

7.1.1.4 Dead Time Optimization Next Steps

Because the derivative operation in discrete time is extremely susceptible to noise, an alternate means of making use of the described $t_1 - \Phi_{ab}$ relationship needs to be determined to make this analysis useful. If sufficient filtering can be applied to the measured signals, constructing a precalibration routine for which a known load power is used to populate a look-up table of the optimized $t_1 - \Phi_{ab}$ relationship may be feasible, but requires further investigation.

7.1.2 Auxiliary Bridge

An alternate means of maintaining ZVS below the traditional boundaries without adjusting output voltage has been formulated by making use of a third full bridge in addition to the two which comprise the traditional DAB converter. The proposed converter configuration is given in Fig. 7.8. This modification to the DAB adds an additional "auxiliary" bridge, also connected to the input source, and joined to the primary and secondary bridges through a third transformer winding which may exhibit the same number of turns as the original primary.

The fundamental issue with ZVS maintenance in the constant output voltage, phase-shift modulated DAB converter is the lack of sufficient energy available in the inductor during low power operation to fully ZVS the primary devices. Without the ability to alter output voltage, input voltage, or converter modulation scheme, there is no approach which permits the increase of converter reactive power at a constant real power output, which is necessary to obtain sufficient inductor energy at low power. The inclusion of the auxiliary bridge in Fig. 7.8 creates a path through which current can be circulated, from input source, through primary bridge and transformer, then through auxiliary bridge and back to the input. By controlling the phase shift between primary and auxiliary bridge, the reactive power which circulates in this loop can be increased or decreased, effectively increasing or decreasing the energy available for the ZVS or primary devices. Additionally, because the auxiliary bridge acts as a load to the primary, the ZVS condition for devices in the auxiliary bridge is the same as that of the secondary bridge in the nominal DAB i.e. ZVS can

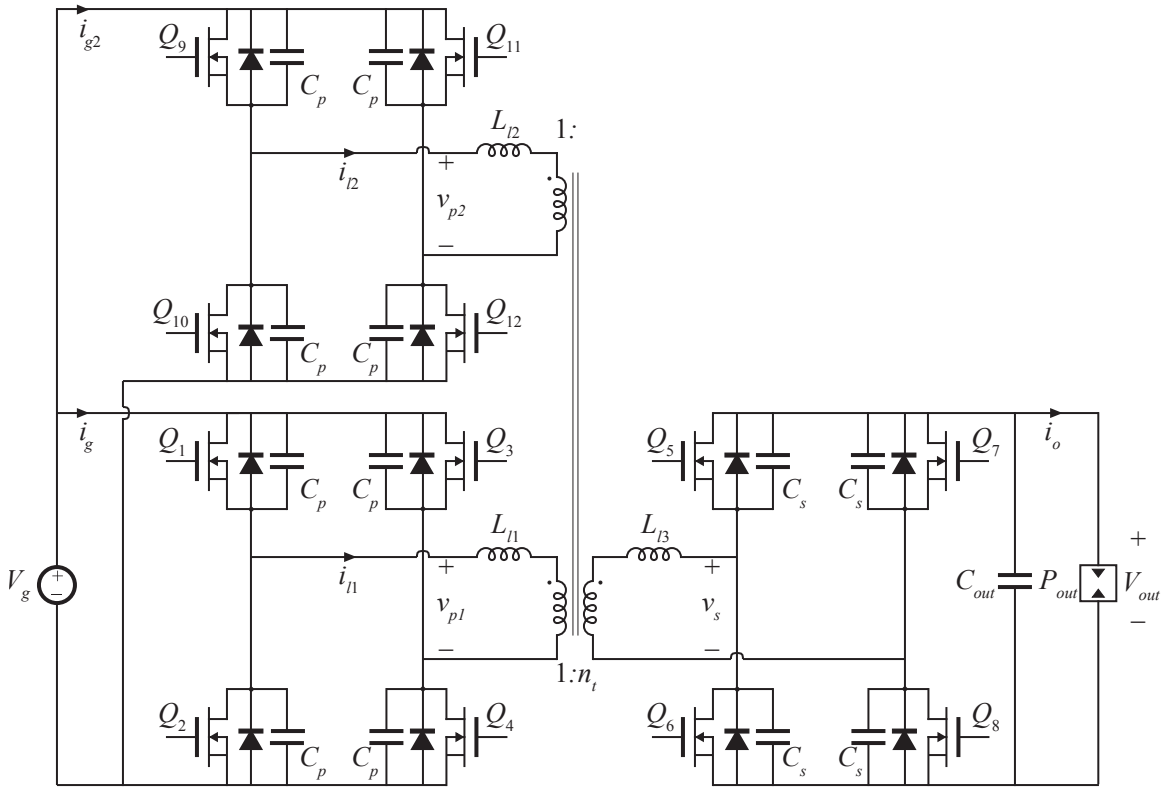


Figure 7.8: Schematic of DAB converter with auxiliary bridge.

always be obtained if dead times are appropriately large.

In contrast, at high power operation, when the DAB converter inherently has sufficient power to ZVS primary and secondary devices, additional reactive power is not advantageous to the system. Under these operating conditions, the auxiliary bridge can be operated with very little phase shift relative to the primary, effectively splitting the input current between the primary and auxiliary bridges with each exhibiting the forward flow of real power to the output.

Thus a control implementation can be conceptualized, though analysis remains a subject of future work, whereby the primary-to-secondary phase shift is used to control output power according to e.g. voltage control requirements while the primary-to-auxiliary phase shift is used to maintain ZVS of all devices. At low output power, the auxiliary bridge behaves as a load with large primary-auxiliary phase shift, while at high output power nearly zero primary-auxiliary phase shift effectively parallels the two high voltage bridges.

Initial simulations constructed in Simulink have shown that such a control is feasible, and all devices may be operated with ZVS across all operating powers. For an example converter with 1:1:1 transformer and all devices, inductances, and bridge voltages matched, tank inductor currents and bridge voltages are plotted for all three bridges in Fig. 7.9, Fig. 7.10, and Fig. 7.11 for output powers of 5 W, 40 W, and 120 W, respectively. In all three cases, all devices in the circuit operate with ZVS. Additionally, at low and medium power, the phase shift between primary and auxiliary inductor currents demonstrates the auxiliary bridge acting as a load to the primary to maintain ZVS, while at high power the auxiliary and primary bridges operate in parallel to split the current flow to the secondary evenly. The merits of the proposed auxiliary bridge are thereby established, though additional analysis and refinement of control strategies remains the subject of future work.

A potential drawback to the proposed design considers the addition of four more switching devices. However, because the primary and auxiliary bridges are operated in parallel at high power, the total silicon area of the eight high voltage devices should remain similar to that of the traditional DAB. To further argue this point, consider a design in which the auxiliary bridge

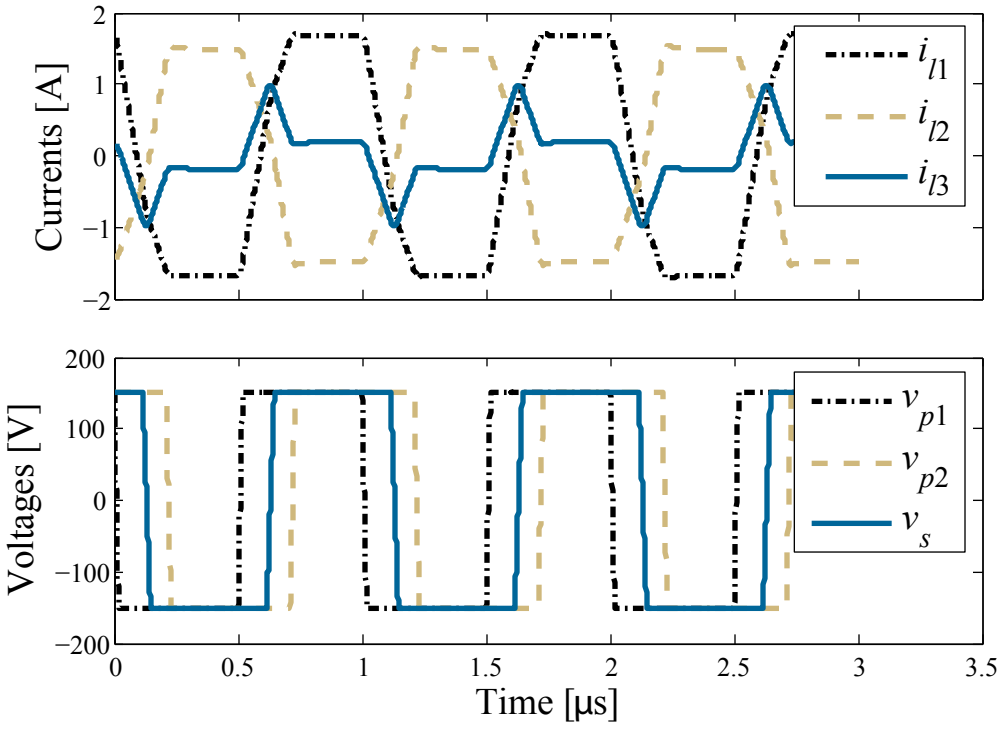


Figure 7.9: Simulated waveforms of the 1:1:1 DAB converter with auxiliary bridge circuit for operation with 5 W output power.

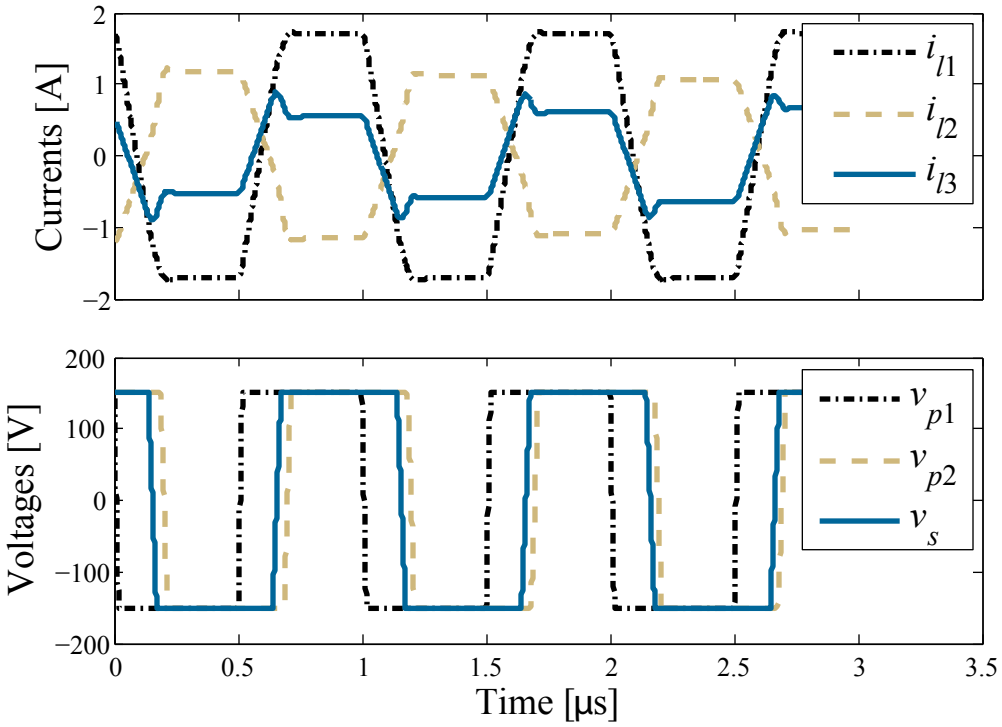


Figure 7.10: Simulated waveforms of the 1:1:1 DAB converter with auxiliary bridge circuit for operation with 40 W output power.

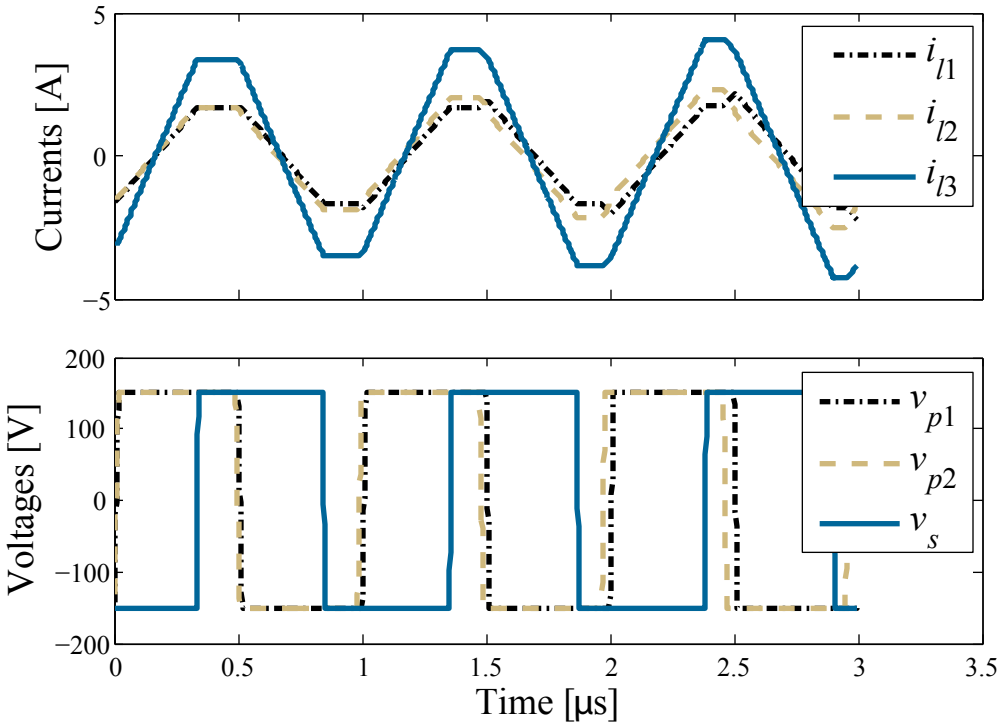


Figure 7.11: Simulated waveforms of the 1:1:1 DAB converter with auxiliary bridge circuit for operation with 120 W output power.

and primary bridge are made identical; in this case each of the high voltage devices $Q_1 - Q_4$ and $Q_9 - Q_{12}$ can be made half the size of the original devices in the DAB converter to obtain the exact same silicon area. The average current conducted by each device is the auxiliary bridge converter is exactly half – and the on-resistance twice – the values of the traditional DAB high voltage transistors. However, because conduction losses depend on the RMS currents in devices rather than their average values; if tank inductance is unaltered, $L_{l1} = L_{l2} = L_l$, the auxiliary bridge converter will have RMS currents in each bridge which are slightly larger than half of the primary RMS currents in the DAB converter. However, because the selection of L_l in the DAB was dictated by the requirements to store sufficient energy to provide primary ZVS, the values of tank inductors in the auxiliary bridge implementation can be significantly reduced, therefore potentially resulting in RMS currents in each high voltage bridge which are *less* than the required values in the DAB converter. This gives the auxiliary bridge converter significantly reduced switching losses at low power, reduced conduction losses at high power, and equivalent total silicon area, affecting both converter size and cost.

The main drawback of the proposed converter structure is then the increased complexity introduced by the additional transformer winding. Though it is potentially possible to achieve nearly equivalent losses in the three- and two-winding transformer implementations, achieving this would require more complicated winding patterns in order to maintain low proximity loss in adjacent windings. This results in additional winding layers in the transformer, which necessarily increase either the size or cost of the transformer implementation.

Further analysis of the auxiliary bridge converter is warranted using similar techniques to those applied to the DAB converter, to determine with more precision the relative merits of the architecture.

7.1.3 Multivariable Power Stage Optimization

The device and component value selection employed previously in the design of the DAB power stage was completed under the motivation of achieving maximum power efficiency, neglecting

gate drive losses, at a single operating power with $M_N = 1$. Though it is reasoned qualitatively that this power stage design should lead to favorable efficiencies over the whole load range, future work should address directly the optimization of power stage parameters for performance over a full range of output powers.

To this end, initial work has been completed which considers only the tank inductance and turns ratio values for a given selection of MOSFETs on primary and secondary. Using the results from Chapter 5, the efficiency of a converter with any arbitrary selection of transformer turns ratio and tank inductance are be assessed at all operating points in a specified range of normalized conversion ratio M_N and output power P_{out}. For the designed DAB in the designated application, this results in plots as shown in 7.12 and as used previously in the selection of the optimal trajectory over which to vary V_{out}. Assuming similar control methods are employed, the optimal output voltage

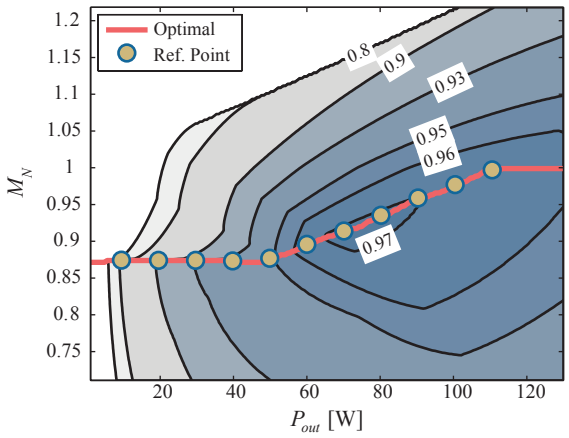


Figure 7.12: Aggregate efficiency for a given converter design is given, e.g. as the numerical average of the highest achievable efficiency at each reference point given for output power in the range $P_{out} = \{10, 20, 30, ..., 110\}$.

at each output power is solved numerically to obtain the highest converter power stage efficiency. Then, in order to assess the relative merit of this selection of n_t and L_l with alternatives, an aggregate efficiency is taken as a single figure of merit for the design which consists of the weighted

average of the converter efficiency evaluated at 10 W intervals between 10 and 110 W,

$$\eta_{agg} = \frac{1}{n}\sum_{i=1}^{n} W_i \eta_{conv}\big|_{\left(P_{out}=P_{max}\frac{i}{n}\right)} , \tag{7.1}$$

with W_i a selected weighting function, in this case $W_i = 1 \forall i$ and $n = 11$. Different definitions may potentially be used here so long as the result is a single value which represents the relative merit of the design.

Following this, the values of L_l and n_t are swept over a range of values, with the aggregate efficiency calculated for each combination to yield the plot shown in 7.13. This figure demonstrates that, for the given design and definition of η_{agg}, the optimal tank inductance and transformer turns ratio are $L_l = 8\mu$H and $n_t = 0.072$, respectively. These values are well matched, though with slightly different turns ratio, than the values employed in the prototype converter, $L_l = 8\mu$H and $n_t = 0.08$.

In the future, this optimization should be extended to include additional parameters. Examples include the addition of gate charge related losses to the efficiency calculations as well as the selection of transistor devices on primary and secondary. Both of these additions would be well suited to design in a known fabrication process in which transistor figures of merit $Q_g r_{on}$ and $C_{oss} r_{on}$ may be used to optimally select the size of devices according to tradeoffs in switching and conduction losses. As more dimensions are added to the optimization, the algorithm employed will need to be improved to obtain reasonable computation times. A simple iteration over a full range of P_{out} and M_N at each operating point to find η_{agg} at each analysis point was permissible in the case of only two-variables considered for power stag optimization, but is a poor approach as the additional variables are added. Methods such as Newtonian iteration may be employed to speed computations, or inherent assumptions about the continuity of the optimal efficiency trajectory may be employed to speed the calculation at adjacent output powers to those already solved.

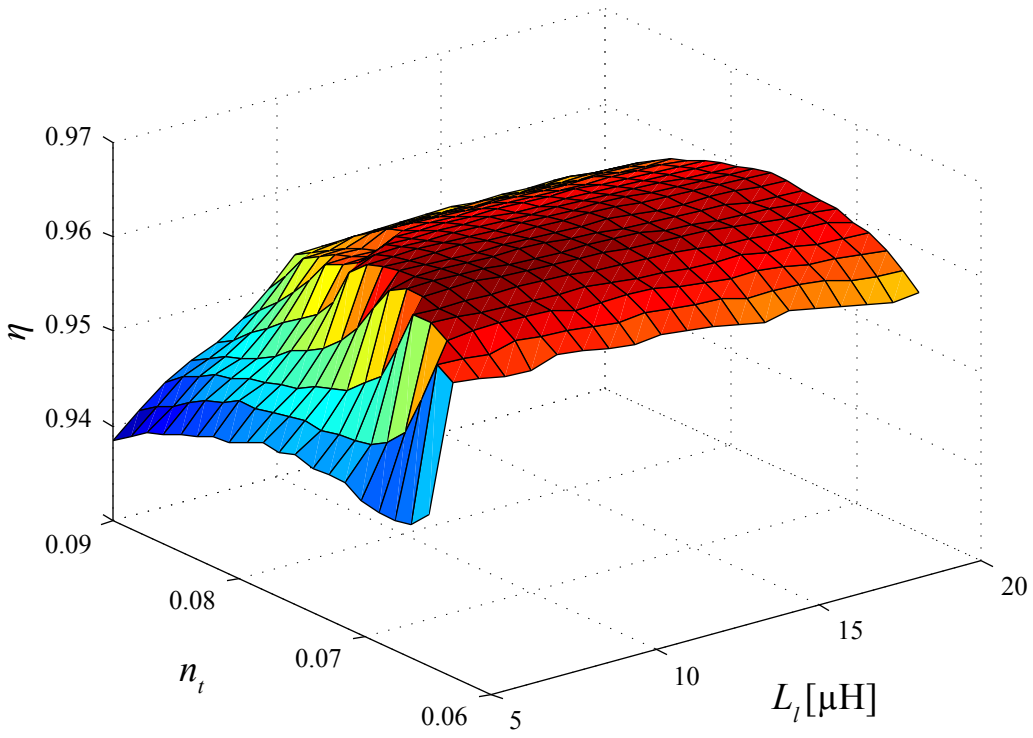


Figure 7.13: Aggregate efficiency as defined in (7.1) is plotted for tank inductance in the range $5 < L_l < 20\mu$H and turns ratio in $0.06 < n_t < 0.09$. The optimal combination is found to occur at $L_l = 8\mu$H and $n_t = 0.072$.

7.1.4 Facility-Level Power Conversion Analysis

A significant additional area of research which is not addressed directly in this thesis is the system-level analysis of power conversion in the data center application, including details of how the proposed control trajectories alter behaviors of downstream power conversion stages.

The proposed DAB control trajectory leverages the presence of downstream VRM and POL converters to permit the variation of output voltage within a small range around its nominal value. This variation, however, will inevitably affect the VRM and POL converters themselves, both in terms of dynamic response and steady-state efficiency. It is posited that these latter conversion stages will be codesigned along with the DAB; their construction will take into account the presence of a varying input voltage and preemptively mitigate any extreme negative effects thereof. If this codesign is completed successfully, there is reason to believe that the input voltage variation could, in fact, improve the operating efficiency of downstream converters. The voltage trajectory is such that the input voltage to the VRM and POL modules will be high at high power and low at low power. This permits the reduction of input conduction losses at high power, where the high currents dominate overall efficiency, and the reduction of any switching losses (or switching transition dependent effects in ZVS converters) at low power, where they dominate.

Additionally, the dynamic details of bus stability should be examined in detail for the DAB implemented as proposed in the data center application. Because the trajectory causes the output voltage to rise and fall in phase with the output power, the output port of the DAB converter may be seen as presenting a negative impedance to the 12 V nominal bus line. Analysis of how this negative impedance effects the voltage stability in the presence of multiple independent DC-to-DC converter loads is necessary before such an architecture may be deployed.

Finally, facility-wide analysis of the data center power conversion architecture permits the determination of optimal voltage levels on the various buses present, including the traditional 12 V nominal bus and the high-voltage bus which forms the input port of the DAB converter.

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Appendix A

Magnetics Design Tools

A.1 Finite Element Simulation of Magnetics using FEMM

For the numerical calculation of operational characteristics of magnetic components, including field strength, flux distribution and winding current distributions, a free software package, Finite Element Method Magnetics (FEMM), was used [87]. FEMM consists of a GUI interface and Matlab/Octave integration, which allows for simple automation of device design and simulation from within Matlab code. Additionally, the tool is capable of both magnetic and electric analysis, the latter of which was used to simulate inter- and intra-winding capacitances, which can produce significant effects on circuit behavior if significant.

While powerful, FEMM has considerable limitations for magnetics design. First, the analysis is magnetostatic (or electrostatic) and can therefore only analyze a single steady-state operating point per program execution, and is incapable of dynamic analysis. Second, the analysis is sinusoidal, fixed-frequency; nonsinusoidal or multimodal current waveforms cannot be analyzed in a single execution. Finally, the analysis two-dimensional with either planar or axisymmetric extrusions to the third dimension. Thus, any magnetic devices which are do not exhibit full symmetry about a single plane or axis cannot be simulated, or will be simulated inaccurately with respect to any nonsymmetric features.

These limitations are significant in the converter design presented in this thesis, as current waveforms in all components contain significant frequency components beyond the fundamental. Additionally, PQ and planar ER cores were used to construct different revisions of the transformer

design, neither of which are fully symmetric about a single axis or plane, but both of which contain fully axisymmetric winding patterns. The design approach employed in this work attempted to use multiple simulations at varying frequency, and with both planar and axis symmetry extrusions in order to inform transformer design and construction. While planar simulations provide a good approximation of core-dependant characteristics, including flux density distribution, fringing fluxes, and magnetizing inductance, axisymmetric simulations provide more accurate insight into winding current distributions and capacitances.

Examples of diagrams constructed in FEMM to model both planar and traditional transformer implementations, with both planar and axisymmetric simulation options, are shown in Fig. A.1. For the designs as modeled in Fig. A.1, the simulated flux density under circuit operation

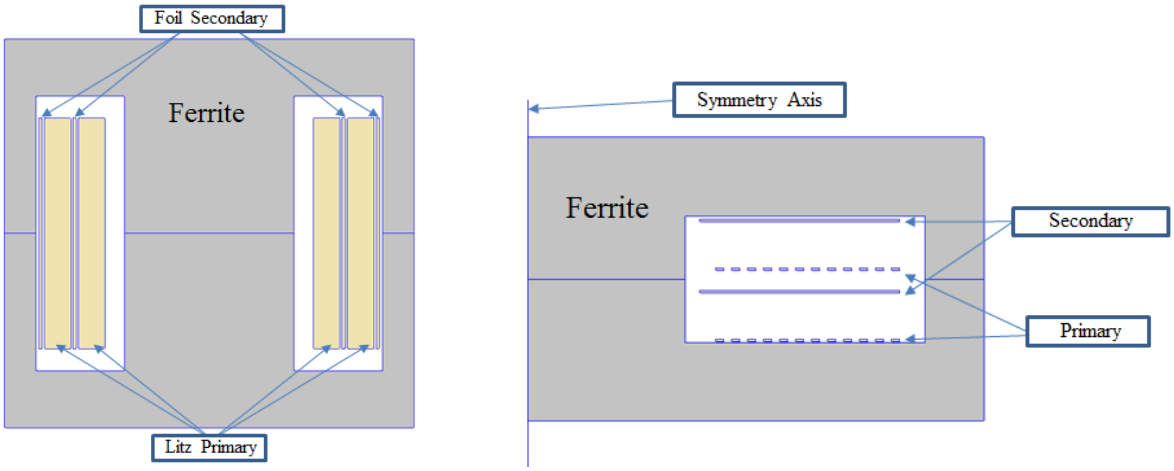
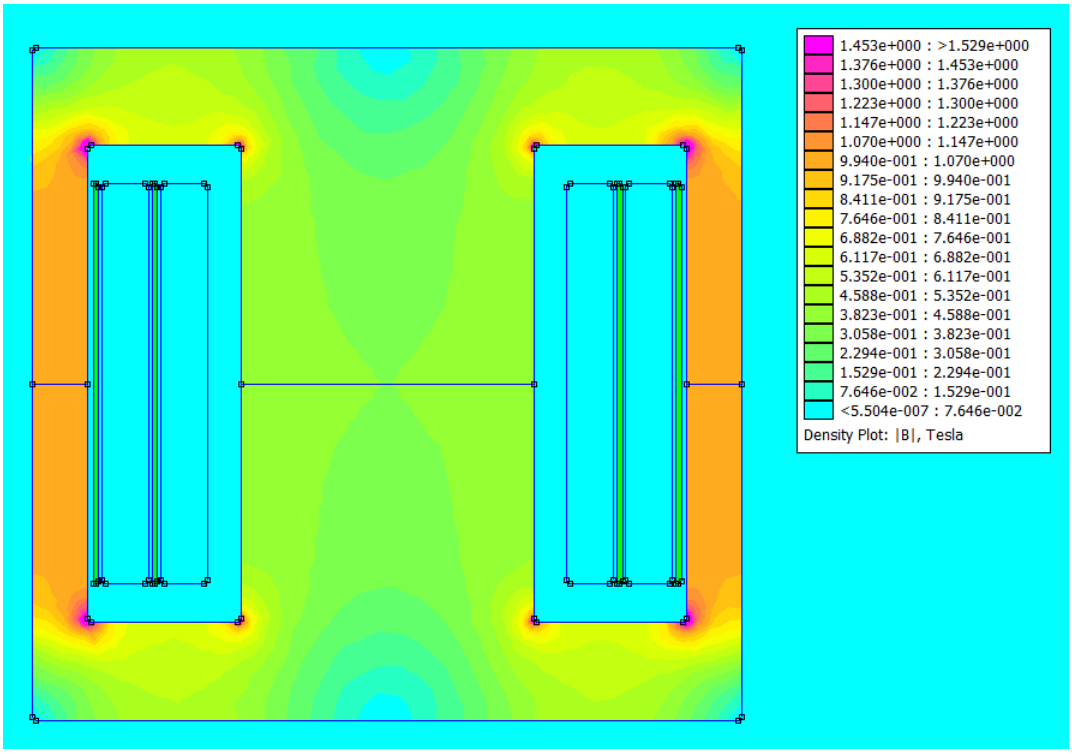
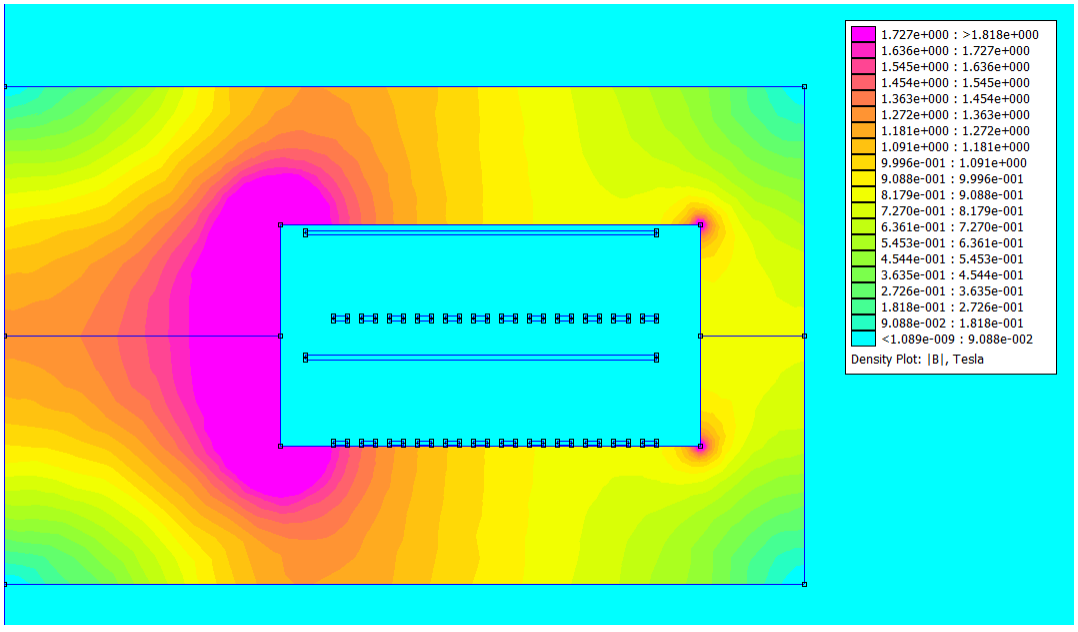


Figure A.1: Diagrams of two transformer simulations run in FEMM. Colors and labels are added externally to the tool. In (a), a PQ20/20 ferrite core is simulated with planar symmetry. A solid copper foil secondary, and evenly distributed litz primary are used. In (b), a planar ER2313 core is considered with both primary and secondary comprised of PCB traces; axis symmetry is considered.

with 1 MHz, sinusoidal, 1 A peak current primary current and an open-circuited secondary is shown in Fig. A.2.



(a)



(b)

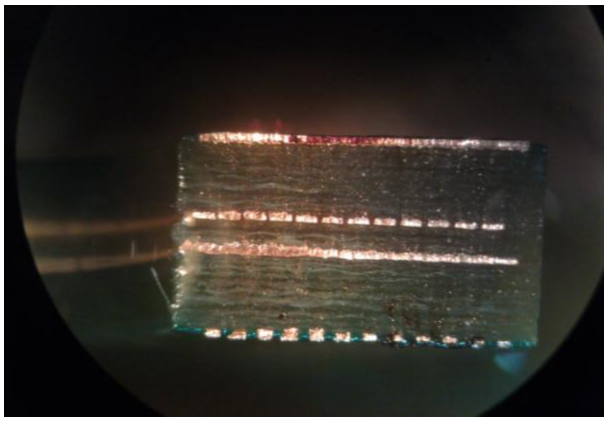
Figure A.2: Simulations of flux density present in cores when primary current is excited with 1 A peak current at 1 MHz. The secondary is left as an open circuit.

A.1.1 Low Cost Planar Transformer Implementation

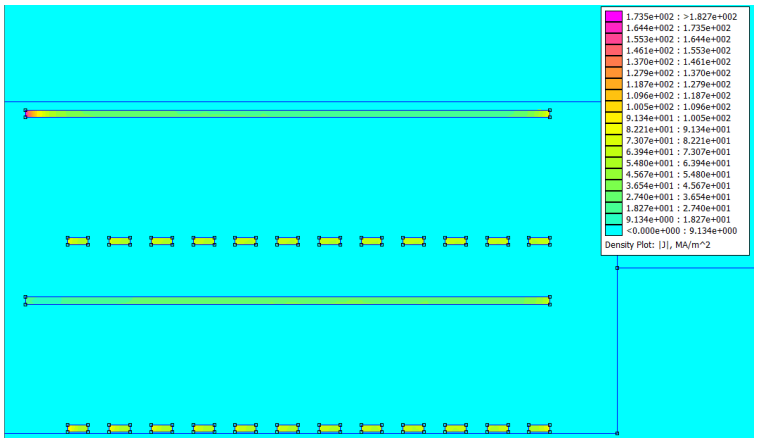
The planar transformer implementation of the DAB transformer was constructed using the standard 4-layer printed circuit board (PCB) available from PCB manufacturer Advanced Circuits. One issue incurred in the process was the uneven copper layer distribution in these boards; as can be seen in Fig. A.3(a), the distance between layers 2 and 4 is much less than that between 1 and 2, or 3 and 4. Winding current density is simulated in Fig. A.3(b) for 100 W power processed by the transformer at 1 MHz, indicating that the close proximity does not unduly elevate eddy currents in windings, largely due to the already low window fill factor achievable in planar transformers. However, the electric field shown in Fig. A.3(c) clearly indicates that the uneven spacing will cause additional capacitance between the copper on layers 2 and 4, in this case, the primary and secondary windings. This capacitance across the isolation barrier of the transformer causes additional common mode currents in transformer windings and has the potential to significantly impact converter efficiency.

A number of solutions are available to mitigate or eliminate the effect of uneven copper layer distribution in the PCBs, with the most simple being to upgrade from standard to custom PCB specifications and enforce even layer spacing. However, this approach significantly increases the cost of PCB manufacturing. In large quantity production of these converters, this static cost is negligible; however, for single-run prototype boards used for design and evaluation, this may increase the overall cost of the PCB more than 20-fold.

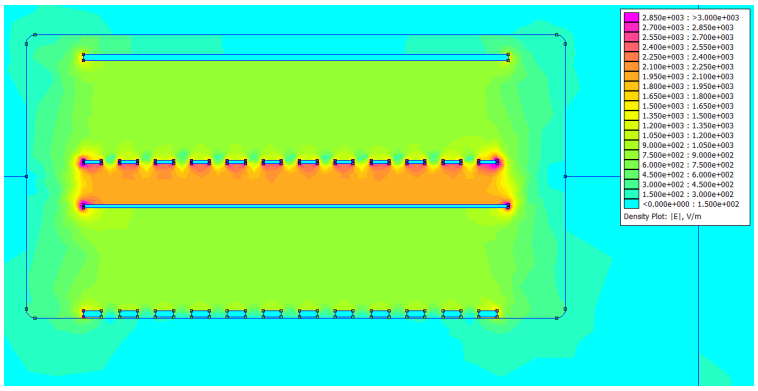
Similarly, characteristics such as high copper weight, high number of layers, and blind/buried vias would be useful in designing and constructing an optimal planar transformer, but also require a significant increase in the fabrication complexity, and therefore cost, of prototype boards. Therefore, an approach was used to evaluate planar transformer design which used only the standard specification, 4-layer PCBs from Advanced Circuits, but stacked two boards together to achieve improved copper area and number of winding layers. The winding pattern of the two stacked boards is shown in Fig. A.4.



(a)



(b)



(c)

Figure A.3: FEMM simulations of winding characteristics in a planar transformer. In (a), a microscope image shows the spacing between layers in the standard Advanced Circuits, 4-layer PCB. Winding current distributions is shown in (b) for operation at 100 W of real power. An electrostatic simulation shows the electric field strength produced when the primary winding is held a 1 V.

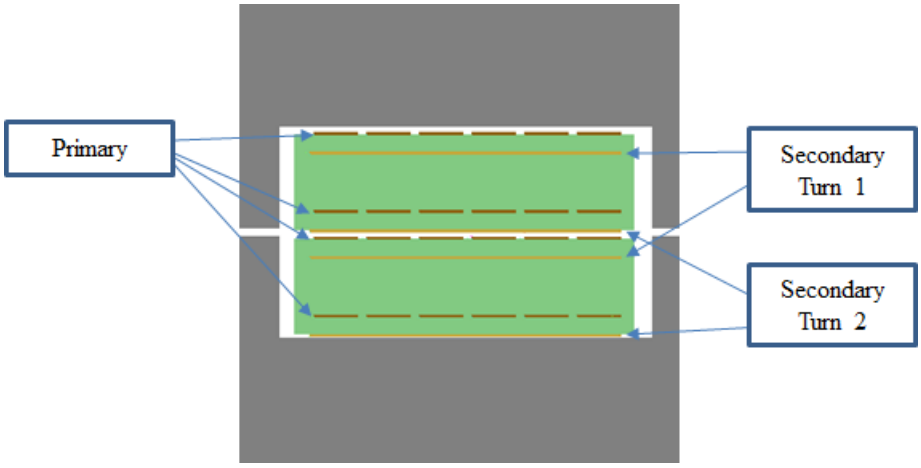
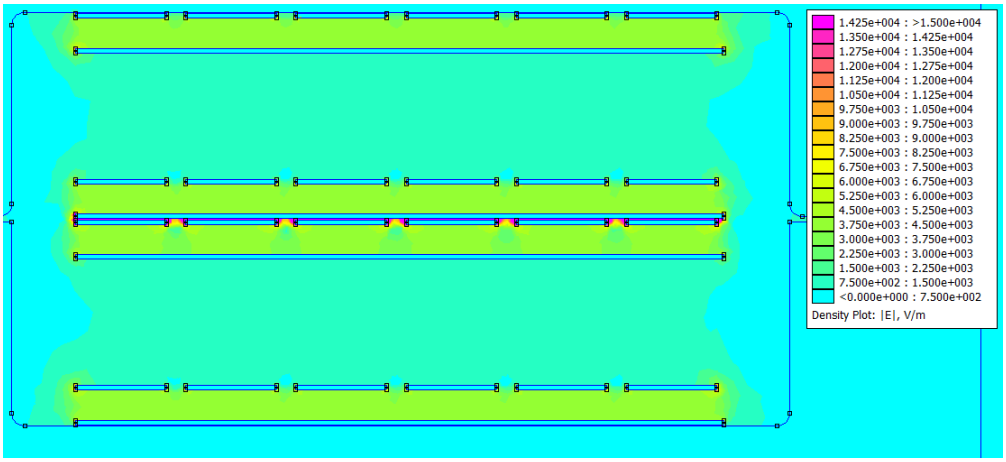


Figure A.4: Stacked PCB planar winding diagram

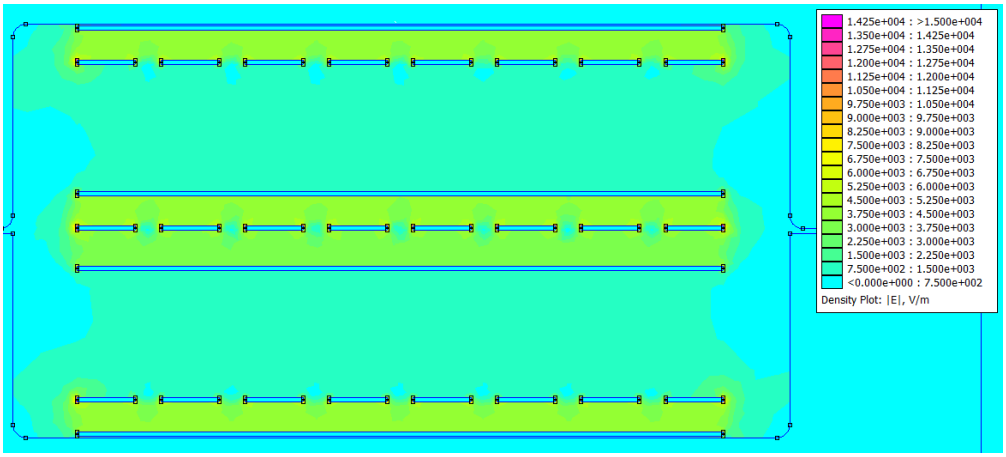
When stacked, the top layer of the bottom board was left without any windings to eliminate the high capacitance that would otherwise occur due to the close proximity between outer layers on the two stacked boards. This allowed the use of a 7-layer PCB design, permitting wider PCB traces and fewer turns per layer on the primary, and paralleling of layers to achieve larger effective wire area on the secondary. The design cross section of both a fully eight-layer and 7-layer implementation are shown in Fig. A.5. The capacitance between primary and secondary in the full 8-layer board simulated at 247 pF, whereas the 7-layer implementation exhibits only 37 pF. Both designs were constructed to test the effect of the barrier capacitance on converter efficiency. Measured capacitances were within 10% of FEMM predictions in both cases. When implemented in the all-silicon prototype DAB converter, operated at 150-to-12 V conversion ratio and 100 W output power, the 8-layer board achieved 95.3% power stage efficiency whereas the 7-layer board operated with 96.4% efficiency. Clearly, the effect of increased common mode currents due to the transformer primary-to-secondary capacitance is significant, and the 7-layer implementation is adviseable for the reduction thereof.

The effect of the primary-to-secondary capacitance can be seen most clearly in circuit waveforms when the DAB is operated with extreme phase shift to make inductor current appear closer to a triangle wave than the traditional nearly square waveshape, as in Fig. A.6. Waveforms of the 7-layer transformer with smaller phase shift to place converter operation at the nominal, 100 W operating point are given in Fig. A.7

An image of one of the constructed planar transformer and inductor prototypes is shown in Fig. A.8.

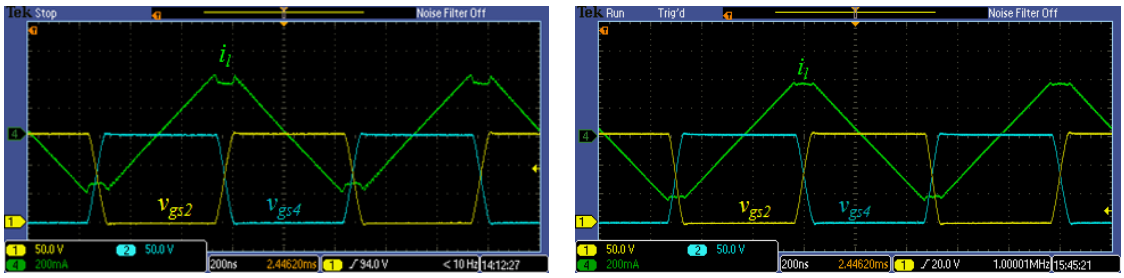


(a)



(b)

Figure A.5: Electrostatic simulations of electric field strength produced when the primary winding is held a 1 V for both two, four-layer boards stacked in (a) and the proposed configuration with one inner layer left devoid of copper (b)



(a) (b)

Figure A.6: Waveforms of the DAB converter with large phase shift. Ideal current waveshape should be a triangle wave with rounded points due to resonant transitions. In (a), the 8-layer transformer's high barrier capacitance causes significant common mode current during voltage transitions. In (b), the 7-layer board has waveforms much closer to ideal due to the reduced capacitance.

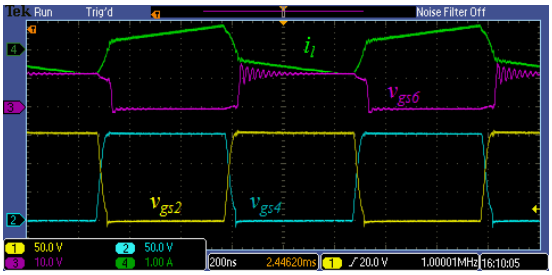
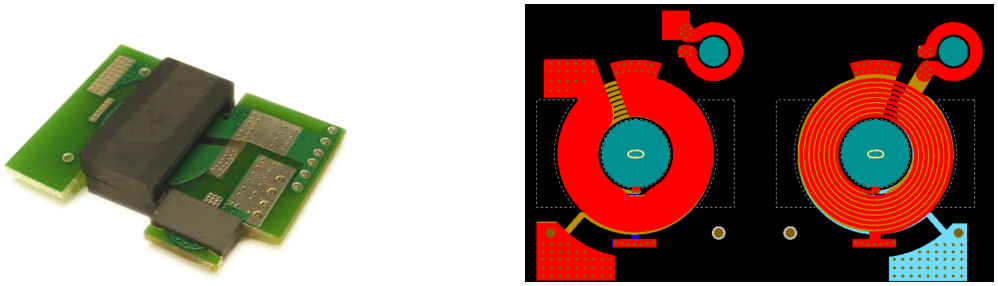


Figure A.7: Waveforms of DAB converter under nominal operating conditions with 7-layer planar transformer. Efficiency is 96.4%. The effect of the primary-to-secondar capacitance can be seen in common mode currents which cause a slight inversion of concavity in current waveshape during the primary resonant interval.



(a) (b)

Figure A.8: Constructed prototype planar transformer and inductor (b) and PCB layout of windings in the two boards which comprise the windings (a).

A.2 Magnetics Tables

Table A.1 was created using data taken from [43,144,145], with K_g and K_{gfe} FOMs calculated as in [22].

Table A.1: Geometrical Data for Standard Ferrite Cores

Name	K_g [cm^5]	K_{gfe} [cm^x]	A_e [cm^2]	W_A [cm^2]	MLT [cm]	L_e [cm]	weight [g]
ETD29	0.098	0.008	0.760	0.90	5.30	7.20	28
ETD34	0.193	0.013	0.971	1.23	6.00	7.86	40
ETD39	0.401	0.020	1.250	1.77	6.90	9.22	60
ETD44	0.832	0.030	1.730	2.14	7.70	10.30	94
ETD49	1.430	0.041	2.110	2.73	8.50	11.40	124
ETD54	2.581	0.056	2.800	3.16	9.60	12.70	180
ETD59	4.676	0.077	3.680	3.66	10.60	13.90	260
E5.3	8.46E-06	3.32E-05	0.025	0.02	1.30	1.27	
EE12	7.31E-04	4.58E-04	0.140	0.09	2.28	2.70	2
E16	2.64E-03	9.92E-04	0.201	0.22	3.30	3.76	4
EE19	4.07E-03	1.30E-03	0.230	0.28	3.69	3.94	5
E20	0.007	1.77E-03	0.312	0.29	3.87	4.28	8
EE22	0.008	1.80E-03	0.410	0.20	3.99	3.96	9
E25	0.031	4.16E-03	0.520	0.56	4.90	5.80	16
EE30	0.086	0.007	1.090	0.48	6.60	5.77	32
E30	0.051	0.006	0.600	0.80	5.60	6.70	22
E34	0.096	0.008	0.807	1.02	6.90	6.93	28
EE40	0.209	0.012	1.270	1.10	8.50	7.70	50
E4215	0.606	0.022	1.780	1.78	9.30	9.70	88
E4220	0.939	0.028	2.330	1.73	10.00	9.70	112

Table A.1: Geometrical Data for Standard Ferrite Cores

Name	K_g [cm^5]	K_{gfe} [cm^x]	A_e [cm^2]	W_A [cm^2]	MLT [cm]	L_e [cm]	weight [g]
E47	0.757	0.024	2.340	1.31	9.47	8.89	106
E50	0.901	0.029	2.250	1.78	10.00	9.29	152
E55	2.701	0.050	3.540	2.50	11.60	12.40	216
E60	0.287	0.008	2.480	1.35	28.90	11.00	480
E65	7.659	0.091	5.400	3.94	15.00	14.70	410
EE70	5.060	0.127	3.240	6.75	14.00	9.00	280
E80	9.589	0.123	3.920	5.54	17.76	18.40	360
PlE14	8.20E-04	6.10E-04	0.145	0.08	4.10	2.07	2
PlE18	0.005	1.64E-03	0.395	0.10	6.00	2.43	8
PlE22	0.029	4.40E-03	0.785	0.19	8.06	3.25	21
PlE32	0.091	0.008	1.290	0.30	10.91	4.17	46
PlE38	0.284	0.016	1.940	0.50	13.32	5.26	86
PlE43	0.486	0.021	2.250	0.72	14.97	6.17	118
PlE58	1.265	0.036	3.050	1.36	20.03	8.12	212
PlE64	2.430	0.048	5.110	1.11	23.78	7.97	356
ER9.5	2.51E-04	3.67E-04	0.085	0.03	1.84	1.42	1
ER11	4.38E-04	4.86E-04	0.119	0.03	2.16	1.47	1
ER14.5	1.24E-03	8.55E-04	0.176	0.05	2.70	1.90	2
ER23	4.86E-03	1.20E-03	0.502	0.10	5.06	2.66	
ER28	0.137	0.012	0.814	0.58	5.60	6.40	28
ER35	0.385	0.022	1.070	1.10	6.51	9.08	46
ER40	0.759	0.032	1.490	1.26	7.37	9.80	74
ER48	2.028	0.056	2.550	1.47	9.42	10.00	128
ER54	1.606	0.048	2.500	1.26	9.83	9.18	122

Table A.1: Geometrical Data for Standard Ferrite Cores

Name	K_g [cm^5]	K_{gfe} [cm^x]	A_e [cm^2]	W_A [cm^2]	MLT [cm]	L_e [cm]	weight [g]
U10	6.08E-04	4.42E-04	0.081	0.28	3.00	3.83	2
U15	0.009	1.80E-03	0.323	0.39	4.66	5.20	8
U20	0.042	4.80E-03	0.560	0.73	5.40	6.80	18
U25	0.050	0.006	0.403	0.90	2.96	8.36	16
U25	0.194	0.011	1.040	1.31	7.30	8.82	47
U30	0.615	0.022	1.610	2.30	9.70	11.10	86
U67	0.883	0.019	2.040	1.61	7.60	17.30	170
U93	46.242	0.331	4.480	23.04	10.00	35.40	800
T2.5	1.18E-06	2.70E-05	0.005	0.02	0.36	0.60	
TC2.5	9.94E-07	2.42E-05	0.005	0.02	0.36	0.60	
TN4	1.29E-05	9.91E-05	0.014	0.04	0.58	0.92	
TN6	6.10E-05	2.49E-04	0.020	0.13	0.80	1.53	
TN10	1.19E-03	1.26E-03	0.078	0.28	1.44	2.41	
TN16	0.012	4.60E-03	0.197	0.72	2.29	3.85	
TN20	0.033	0.007	0.336	0.79	2.72	4.36	
TN25	0.117	0.016	0.489	1.77	3.60	6.02	
TN32	0.358	0.030	0.765	2.84	4.64	7.60	
TN36	0.725	0.045	0.960	4.15	5.28	8.96	
TL42	0.896	0.050	0.958	5.31	5.44	10.30	
TL58	4.078	0.121	1.524	13.20	7.52	15.24	
TX74	6.460	0.144	2.080	11.95	8.00	16.50	
T102	23.096	0.309	2.670	34.21	10.56	25.50	
T107	69.800	0.568	5.140	33.18	12.56	25.90	
POT7	7.38E-07	1.61E-06	0.070	0.00	1.46	1.00	1

Table A.1: Geometrical Data for Standard Ferrite Cores

Name	K_g [cm^5]	K_{gfe} [cm^x]	A_e [cm^2]	W_A [cm^2]	MLT [cm]	L_e [cm]	weight [g]
POT9	1.83E-04	2.56E-04	0.101	0.03	1.90	1.26	1
POT11	5.57E-04	4.73E-04	0.162	0.05	2.26	1.55	4
POT14	1.88E-03	9.62E-04	0.251	0.09	2.90	1.98	6
POT18	0.009	2.41E-03	0.433	0.17	3.67	2.58	12
POT22	0.024	4.32E-03	0.634	0.26	4.45	3.15	24
POT26	0.062	0.007	0.939	0.37	5.26	3.76	40
POT30	0.161	0.013	1.370	0.53	6.20	4.52	68
POT36	0.398	0.021	2.020	0.72	7.43	5.32	108
POT42	1.150	0.041	2.660	1.40	8.60	6.81	104
POT66	15.818	0.175	7.170	4.00	13.00	12.30	1100
PQ2016	0.020	3.34E-03	0.619	0.24	4.40	3.76	22
PQ2020	0.032	4.49E-03	0.626	0.36	4.40	4.57	28
PQ2620	0.084	0.007	1.190	0.33	5.62	4.63	31
PQ2625	0.122	0.009	1.200	0.48	5.64	5.43	64
PQ3220	0.192	0.011	1.690	0.45	6.67	5.59	94
PQ3230	0.203	0.012	1.700	0.47	6.71	5.55	42
PQ3230	0.384	0.019	1.610	1.00	6.71	7.46	55
PQ3535	0.444	0.017	1.900	0.93	7.52	8.61	160
PQ4040	1.200	0.039	2.010	2.50	8.39	10.20	95
RM4	1.66E-03	9.11E-04	0.212	0.07	2.00	2.14	3
RM5	2.39E-03	1.23E-03	0.251	0.10	2.50	1.98	6
RM8	0.011	2.73E-03	0.395	0.31	4.20	3.55	22
RM10	0.059	0.007	0.832	0.44	5.20	4.17	40
RM14	0.613	0.027	1.980	1.11	7.10	7.00	148

Table A.1: Geometrical Data for Standard Ferrite Cores

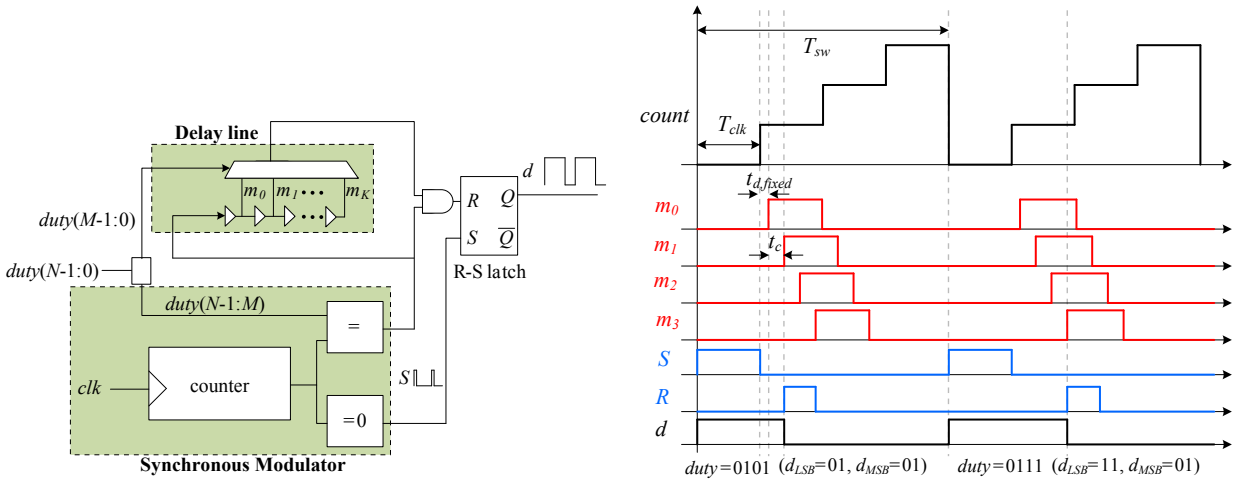
Name	K_g [cm^5]	K_{gfe} [cm^x]	A_e [cm^2]	W_A [cm^2]	MLT [cm]	L_e [cm]	weight [g]
EC35	0.131	0.010	0.843	0.98	5.30	7.74	36
EC41	0.374	0.020	1.210	1.35	5.30	8.93	57
EC52	0.914	0.032	1.800	2.12	7.50	10.50	111
EC70		0.056	2.790	4.71	12.90	14.40	256

Appendix B

Simple, High Resolution DPWM Implementation

In the high frequency DAB converter, as well as in many other FPGA or custom integrated circuit controlled digital power converters, there is a need for high performance, high resolution circuitry to generate required PWM signals [146,147]. While most of the features required from the digital pulse width modulator (DPWM) can be obtained with conventional digital design procedures, achieving fine time resolution to precisely implement resonant dead times, meet the required voltage regulation accuracy, or to avoid undesired limit cycling [148,149] is still a challenge. Many approaches have been proposed in recent years to address this issue. The hybrid DPWM architecture, shown in Fig. B.1, is one of the most widely used architectures: it combines reliable, synchronous modulation techniques to achieve coarse (clock frequency) resolution, with a delay-line based approach that provides high resolution without the need for a very high frequency clock. The delay line section usually contains tapped delay elements and a multiplexer to control the amount of delay applied to the input signal.

Within FPGA implementations of hybrid DPWMs, two different approaches have been pursued. The first one takes advantage of embedded resources present in modern FPGAs, such as Phase Locked Loops (PLLs) or Digital Clock Managers (DCM), to perform the delay-line functionality. A DCM-based DPWM with 2.5 ns resolution was proposed in [150], but it requires a considerable amount of additional logic and manual placement effort. A similar approach in [151] achieved under 20 ps resolution, which is the highest resolution reported to date. However, it requires a high performance DCM which may not be present in general-purpose FPGAs, and it also



(a) (b)

Figure B.1: (a) Simplified hybrid DPWM architecture; (b)typical operating waveforms.

relies on the update time of the DCM phase-shift command, thus limiting its applicability. Recent work in [152] has claimed resolutions as high as 56 ps are achievable with specialized I/O delay buffers, but such elements are present exclusively in high-end Virtex-6 FPGAs.

The second family of solutions makes use of standard internal logic elements/blocks of the FPGA to construct the delay line [153, 154]. This approach removes the need for specialized PLL or DCM resources, but requires more complex implementations that depend on manual placement and routing, and the resolution is limited by propagation delays of FPGA logic elements/blocks. Carry chain logic paths are often used to implement the delay line functionality due to their low-latency and presence in most FPGAs [155–158]. This approach was used to construct a DPWM with 70-80 ps resolution in [159] without the need for a multiplexer. However, such approach still requires significant manual placement effort which, if not done properly, may lead to non-monotonic operation or other timing errors.

In order to generate the high precision dead times needed to properly drive the transistors in the high frequency DAB converter used throughout this thesis, this appendix details a very simple delay line hybrid DPWM based on [159] that uses internal resources present in most FPGAs and leverages inherent routing constraints of manufacturer design tools to achieve very high timing resolution, monotonicity and predictable operation while, importantly, requiring no manual placement or routing efforts by the designer. Implementation is detailed for the Xilinx Virtex 4 FPGA and version 13.1 of the Xilinx ISE Design Suite, though similar design approaches have been demonstrated on Altera FPGAs [127, 128], and the general approach can be applied with minor modification to most low-cost FPGA units.

B.0.1 DPWM architecture

In the N-bit carry-chain-based hybrid DPWM shown in Fig. B.1, the output signal d is set high by the counter at the beginning of the switching period, and is reset by the delay line output within the desired clock period selected by the most significant bits (MSB) of the duty cycle, $d_{MSB} = duty(N-1:M)$. The system clock is usually taken as the input signal to the

delay line, and delayed by an amount controlled through a multiplexer, using the least significant bits (LSB) of the duty cycle command, $d_{LSB} = duty(M-1:0)$. Therefore, synchronous logic handles the MSB part of the duty cycle command, whereas an asynchronous section (tapped delay line and multiplexer) resets the duty cycle signal and determines the resolution. Careful routing and placement are required to match the delay of the critical signal paths; the 2^M tapped delay line outputs that go through the multiplexer must be delay-matched within at least one unit delay. Failure to do so causes non-monotonicity and malfunctioning of the DPWM. Due to the inherent mismatch of delay paths in implementations which are not manually routed, this approach is only well suited to delay line implementations with relatively large per-element delay; an example implementation which achieves approximately 300 ps resolution is given in section B.1.2.

Figure B.2 shows a simplified delay line based on carry chain logic as proposed in [159]. The

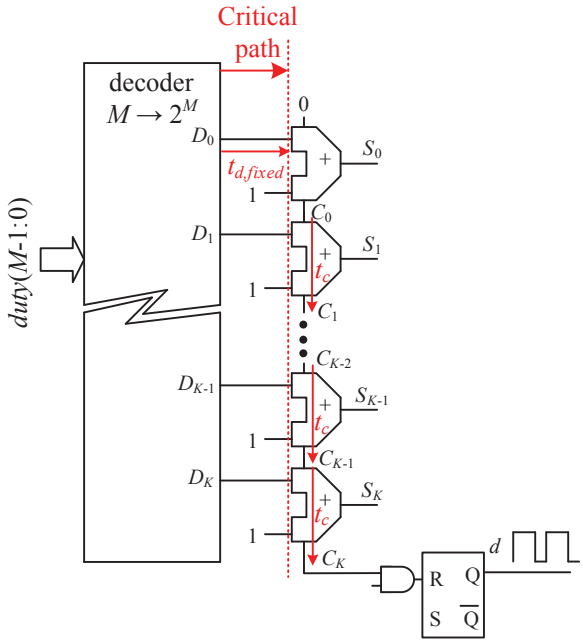


Figure B.2: High resolution section of a hybrid DPWM based on carry chains.

carry chain is a low latency path, which is used to propagate the carry bit through consecutive 2-bit adders to implement high speed arithmetic operations. When D_i goes high, a logic 1 propagates through the carry chain. Rather than tapping and multiplexing each delay element output, the

Table B.1: Ideal delay and control word D as functions of the duty cycle.

$duty(M-1:0)$	ideal t_{delay}	$D_K D_{K-1} \cdots D_1 D_0$
$00\cdots000$	0	$10000\cdots00$
$00\cdots001$	t_c	$01000\cdots00$
$00\cdots010$	$2t_c$	$00100\cdots00$
$\vdots$	$\vdots$	$\vdots$
$11\cdots111$	Kt_c	$00000\cdots01$

control word D is used to select the position of the chain where the carry begins to propagate. The propagation delay t_c of the carry bit through each adder is fixed and predictable, and usually lays in the range of 10-100 picoseconds, depending on the FPGA. This propagation delay sets the minimum achievable time resolution of the DPWM.

The digital word $duty(M-1:0) = d_{M-1}d_{M-2}...d_0 \in [0, 2^M - 1 = K]$ determines the total delay, t_{delay}, of the carry chain, in the following manner:

$$t_{delay} = t_{d,fixed} + duty \cdot t_c \ , \tag{B.1}$$

t_d being the propagation delay from the output of the decoder to the actual input of the carry chain element where the propagation begins. From (B.1) and Fig. B.2, it can be seen that 2^M delay elements are required to implement a M-bit delay line. Furthermore, note that an ideal hybrid DPWM should fulfill

$$T_{clk} = t_{d,fixed} + K \cdot t_c \ , \tag{B.2}$$

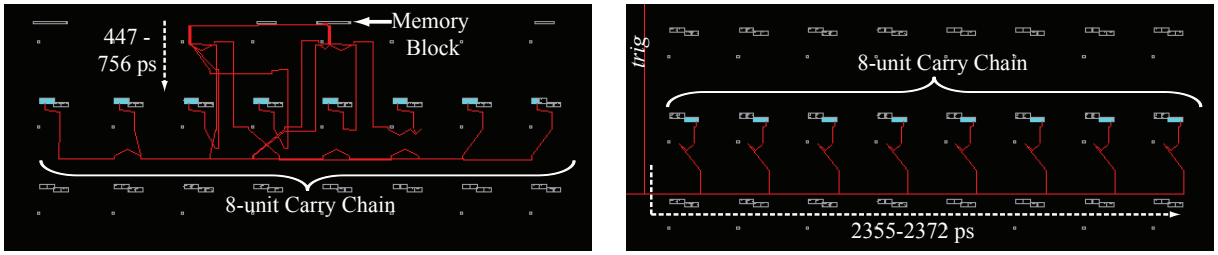
T_{clk} being the system clock period. Table B.1 shows the value of the digital word D and the desired delay as a function of the duty cycle command.

Note that t_c remains approximately constant among different elements and thus, according to (B.1), linearity and monotonicity are mainly determined by the delay through the critical path, $t_{d,fixed}$. Given the low value of t_c that the carry chain logic provides, an almost perfect match between the routing delay from each output of the decoder, D_i, to the input of each corresponding adder is required to achieve a monotonic, repeatable and reliable behavior. This means that,

although the carry chain is automatically placed by the FPGA programming tools, the decoding logic still requires very careful manual placement and routing, significantly increasing complexity and development time. However, it is possible to augment the delay line design further through the use of individual logic elements, rather than the adder abstractions, to precisely control the delay line implementation without the need for signal routing.

B.0.2 Implementation in Xilinx FPGAs

According to Fig. B.2, there are at least 2^M signals in the critical path that need to be matched within a few picoseconds. Unfortunately, the Xilinx Virtex 4 and associated auto-routing tools do not natively match the routing delay of each output from the decoder block. Fig. B.3a demonstrates the achieved routing when a carry chain delay line was implemented and auto-routed in a Virtex 4 device. Calculated propagation delays from the decoder to carry chain elements vary



(a) (b)

Figure B.3: Routing of signals in Xilinx Virtex 4 FPGA. In (a) the path between a single RAM block and 8 carry chain units is routed automatically, with severe mismatch; in (b) the gating signal *trig* is used to provide well matched low-skew routing to all delay cells.

by greater than 300 ps, effectively ensuring non-monotonicity due to the individual carry chain elements having propagation delay of less than 20 ps. Manual routing of each of the 16 paths has the possibility of rectifying this issue, but is overly complex and time-intensive. Rather, the modification of Fig. B.4 is used to remove the routing from the decoder to the carry chain as a critical circuit path. In Fig. B.4, the multiplexer devices responsible for implementing the fast carry chain path are shown explicitly as the delay elements, and a NAND gate is used to control their

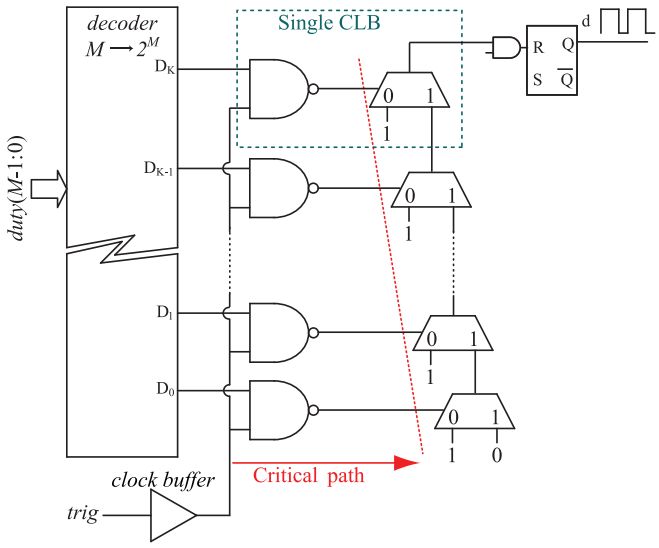


Figure B.4: Virtex 4 implementation of a high resolution delay line. NAND gates are used to gate the decoder output to alleviate the requirement on matched routing delays from decoder to carry chain.

selection input so that propagation through the carry chain is only allowed to begin when the *trig* signal goes high. By gating the output of the decoder thusly, the path from decoder to NAND gate is no longer critical to be delay-matched; instead only the delay of the *trig* signal through each NAND is critical. This implementation is similar to that presented previously in [159], where the reduced matching requirements allowed near-monotonic operation, with full monotonicity obtained with a small manual placement effort. However, inherent Xilinx routing routines can be used to ensure optimal placement natively by instantiating devices from primitives directly, eliminating the need for *any* manual placement or routing.

To accomplish this, the internal structure of each Xilinx Virtex 4 Configurable Logic Block (CLB) is examined [160]. As is the case with most FPGAs, the select pins of carry chain multiplexers implemented within each CLB are directly wired to the output of a look up table (LUT). Because the NAND function can be implemented in this LUT, internal to the same CLB as the multiplexer, the delay from NAND output to multiplexer can be extremely well matched between CLBs and thus between delay elements. In order to ensure such matching, the `lock_pins` constraint is used on each LUT to maintain identical signal paths from *trig* to each delay element. Finally, to ensure that the *trig* signal itself is delay matched to each NAND, a clock buffer primitive is used to give the signal access to low-skew routing paths, the result of which can be seen in Fig. B.3b, which show less than 17 ps propagation mismatch of the *trig* signal to the 16 NAND gates, according to the delays calculated by the Xilinx tools.

Default routing routines inherent to the Xilinx development tools for the Virtex 4 natively maintain the structure of the carry chain for optimal timing, so no manual placement or routing is necessary. Further, by instantiating carry-chain multiplexers (MUXCY) and NAND gates (LUT2) directly from primitives, the LUT elements are automatically combined into the same CLB as the carry chain they control in the default layout optimization of the development tools. An example delay line implementation in verilog is given in Section B.1.1, showing the simplicity of the implementation. Experimental verification is presented in the following section.

B.0.3 Experimental Results

The architecture detailed in Section B.0.2 was implemented in a Xilinx Virtex 4 FPGA using the code from Section B.1.1 and version 13.1 of the Xilinx ISE Design Suite. In the Virtex 4 implementation, the delay of a single carry chain multiplexer is found to be nearly 20 ps, leaving very little room for delay mismatch if monotonicity is to be obtained in the delay line as a whole. Because of this, four carry chain multiplexers are used to implement a single delay element, with the latter three all having their selection inputs tied high. This decreases the delay line resolution to slightly better than 90 ps, but leads to reliable monotonicity without any manual routing. Due to the clustering of slices within CLBs in the Virtex IV, using exactly four delay elements leads to the ability for the *trig* signal to take identical paths through individual switch tables for each delay element, further ensuring good matching of timing signals.

The delay line of Fig. B.4 is combined with a low frequency counter as shown in Fig. B.1a to obtain a 1 MHz hybrid DPWM capable of better than 90 ps resolution across the full duty cycle range from < 1 % to > 99 %. In accordance with (B.2), internal DCM resources are used to match the clock period to a delay line of 2^M elements. Considering the DCM frequency limit of 200 MHz, a *clk* frequency of 178 MHz is tuned experimentally to be well matched to the full string of $K = 63$ delay elements.

Waveforms of the hybrid counter and delay-line DPWM are shown in Fig. B.5, where a 50 % duty cycle, 1 MHz is varied across the entire range of delay line inputs, as well as across two boundaries of the counter, where the MSBs are changed.

It can be seen that not only is very high resolution achieved, but excellent linearity is obtained even across the boundary from delay line to counter. This behavior is further characterized in the results of Fig. B.6, where the low-frequency modulation has a linear fit with $R^2 > 0.9999$ due to the high precision DCM clock output, and the high frequency delay line modulation has $R^2 = 0.9994$. Worst case INL and DNL are 0.178 LSB and 0.180 LSB, respectively, including boundary conditions of the delay line.

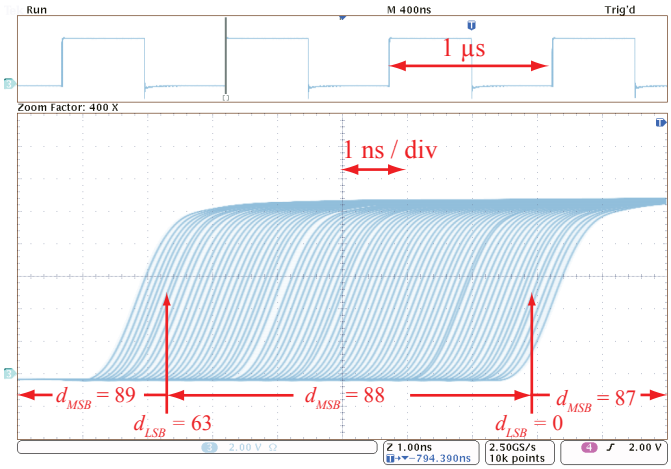
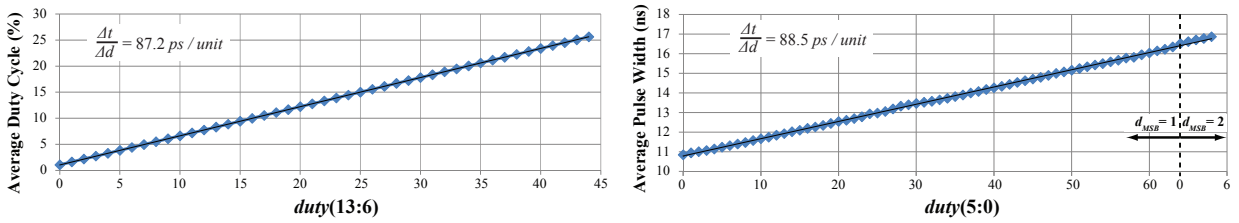


Figure B.5: Waveforms of a nearly 50 % duty cycle PWM output of the hybrid delay line as the duty cycle command is varied across 74 adjacent values. One full traversal of delay line values is shown between the points labeled $d_{LSB} = 0$ and $d_{LSB} = 63$, outside of which the delay line duty cycle rolls over as the counter duty cycle, d_{MSB}, is incremented, maintaining good linearity.



(a) (b)

Figure B.6: (a) 1 MHz PWM duty cycle as a function of the MSBs of the duty cycle command for the low frequency counter; (b) detailed results showing the individual steps of the delay line around a nearly 1 % duty cycle. Note that because $M = 6$, for $duty(5:0) \geq 64$ the LSBs roll over and the counter pulse width is increased. Good linearity is still obtained at this boundary.

B.1 Example Verilog and VHDL Hybrid DPWM implementations

B.1.1 Verilog code for Xilinx Delay Line

```
module DelayCell(input c_in, output c_out, input trig, input sel);
  wire mux_s;
  wire[4:0] line;
  LUT2 #(.INIT(4'hD)) L1 (.O(mux_s), .I0(trig), .I1(sel));
  //synthesis attribute LOCK_PINS of L1 is all;
  MUXCY M1 (.O(line[1]), .CI(line[0]), .DI(1), .S(mux_s));
  MUXCY M2 (.O(line[2]), .CI(line[1]), .DI(1), .S(1));
  MUXCY M3 (.O(line[3]), .CI(line[2]), .DI(1), .S(1));
  MUXCY M4 (.O(line[4]), .CI(line[3]), .DI(1), .S(1));
  assign line[0] = c_in;
  assign c_out = line[4];
endmodule
```

```
module DelayLine(output l_out, input [5:0] dutycycle, input trig);
  wire trig_buf;
  wire [64:0] dl_tap;
  wire [63:0] decode = ~(2^63 >> dutycycle);
  BUFG BUFG_inst ( .O(trig_buf), .I(trig));
  genvar i;
  generate
    for(i=0; i<64; i=i+1) begin: DelCellPlace
      DelayCell D1 ( .c_in(dl_tap[i]), .c_out(dl_tap[i+1]),
                     .trig(trig_buf), .sel(decode[i]) );
    end
  endgenerate
  assign dl_tap[0] = 1'b0;
  assign l_out = dl_tap[64];
endmodule
```

B.1.2 Alternate Xilinx Delay Line

If less resolution is permissible, and FPGA logic elements need to be conserved, a single LUT can be used in place of the four multiplexers to achieve a delay line with approximately 300 ps resolution, though in this case `rloc` constraints need to be used to constrain element layout because the carry chain multiplexers are no longer present to cue inherent optimization routines. With these relative placement macros, the generic multiplexer implementation of Fig. B.1 can be used. This approach is well established in the field, but proved useful during experimental testing in this thesis. Therefore an example two-module VHDL implementation is included below, which uses attribute declarations within the code to ensure proper placement of individual elements, thus preventing the need to use the placement and routing tools within the software. The example is a 16 bit delay line, which matches monotonically with a single period of a 200 MHz synchronous modulator period.

```
entity DelCell is
  Port ( d_in : in  STD_LOGIC; d_out : out  STD_LOGIC);
  attribute keep_hierarchy : string;
  attribute keep_hierarchy of DelCell: entity is "yes";
end DelCell;
architecture structural of DelCell is
  component LUT1
    generic (INIT: bit_vector(1 downto 0) := "10");
    port (O : out std_logic; I0 : in std_logic);
  end component;
  attribute rloc: string;
  attribute rloc of L1: label is "X0Y0";
begin
  L1 : LUT1
   generic map (INIT => "10")
   port map (O => d_out, I0 => d_in);
end structural;
```

```
entity DelayLine is
    Port ( l_in : in  STD_LOGIC;
           l_out : out  STD_LOGIC;
           sel : in  STD_LOGIC_VECTOR (3 downto 0));
  attribute keep_hierarchy : string;
  attribute keep_hierarchy of DelayLine: entity is "yes";
end DelayLine;
architecture structural of DelayLine is
  component DelCell
    Port ( d_in : in  STD_LOGIC;
           d_out : out  STD_LOGIC);
  end component;
  component MUXCY
    port (O : out STD_ULOGIC;
          CI : in STD_ULOGIC;
          DI : in STD_ULOGIC;
          S : in STD_ULOGIC);
  end component;
  component LUT2
    generic (INIT : bit_vector := X"E");
    port (O : out STD_ULOGIC;
          I0 : in STD_ULOGIC;
          I1 : in STD_ULOGIC);
  end component;
  attribute rloc: string;
  attribute bel : string;
  signal dl_taps : STD_LOGIC_VECTOR (15 downto 0);
  signal O1 : STD_LOGIC_VECTOR (8 downto 1);
  signal O2 : STD_LOGIC_VECTOR (4 downto 1);
  signal O3 : STD_LOGIC_VECTOR (2 downto 1);
  signal O4 : std_logic;
  attribute rloc of D1: label is "X0Y0";
  attribute rloc of M3_12: label is "X2Y2";
  attribute rloc of M3_34: label is "X3Y2";
  attribute rloc of M4_12: label is "X2Y3";
  attribute rloc of LUT_1: label is "X4Y3";
  attribute bel of D1: label is "F";
begin
  D1: DelCell port map (l_in, dl_taps(0));
  gen1: FOR i IN 1 TO 15 GENERATE
    gen2: if (i mod 2) = 0 generate
      attribute rloc of D1: label is  "X"  & INTEGER'image((i/2) mod 2) &
        "Y" & INTEGER'image(i/4);
      attribute bel of D1: label is "F";
      begin
        D1: DelCell port map (dl_taps(i-1), dl_taps(i));
    end generate;
    gen3: if (i mod 2) = 1 generate
      attribute rloc of D1: label is  "X"  & INTEGER'image((i/2) mod 2) &
        "Y" & INTEGER'image(i/4);
      attribute bel of D1: label is "G";
      begin
          D1: DelCell port map (dl_taps(i-1), dl_taps(i));
      end generate;
  end generate;
  gen4: FOR i IN 1 TO 8 GENERATE
  attribute rloc of M1: label is  "X"  & INTEGER'image((i-1) mod 2) & "Y" &
    INTEGER'image((i-1)/2);
  begin
    M1 : MUXF5 port map (O => O1(i), I1 => dl_taps(2*i-2),
      I0 => dl_taps(2*i-1),
      S => sel(0));
  end generate;
  gen5: FOR i IN 1 TO 4 GENERATE
  attribute rloc of M2: label is  "X"  & INTEGER'image(2+((i-1)/2)) & "Y" &
    INTEGER'image(2+((i-1) mod 2));
  begin
    M2 : MUXF5 port map (O => O2(i), I1 => O1(2*i-1), I0 => O1(2*i),
      S => sel(1));
  end generate;
  M3_12 : MUXF6 port map (O => O3(1), I1 => O2(1), I0 => O2(2), S => sel(2));
  M3_34 : MUXF6 port map (O => O3(2), I1 => O2(3), I0 => O2(4), S => sel(2));
  M4_12 : MUXF7 port map (O => O4, I1 => O3(1), I0 => O3(2), S => sel(3));
  LUT_1 : LUT2
   generic map (
       INIT => X"E")
   port map (O => l_out, I0 => O4, I1 => l_in);
end structural;
```

The following verilog module can then be used to combine the 16-bit delay line with a 200 MHz modulator,

```
`define MAX_MOD_VALUE  99 // Modulator # of periods -1
`define MOD_SIZE  8       // Modulator length
`define DL_SIZE  4        // Delay line size;
`define MSB_DUTY  (`MOD_SIZE + `DL_SIZE - 1)
`define MSB_MOD  (`MOD_SIZE - 1)
`define MSB_DL  (`DL_SIZE -1)
// synthesis attribute keep_hierarchy of HybridDPWM is true;
module HybridDPWM(
    input [`MSB_DUTY:0] dutycycle,
    input clk_2x,                    //200 MHz clock from internal DCM
    output DPWM,
    input reset,
   output [`MSB_MOD:0] mod_value,    //output can be used for synchronization
   output dsample_w                  //output can be used for synchronization
    );
  reg [`MSB_DL:0] duty_DL;           //Delay line duty cycle
  reg [`MSB_MOD:0] duty_Mod;         //Modulator Duty Cycle
  (* KEEP = "TRUE" *) reg dsample;
  (* KEEP = "TRUE" *) reg line_in;
  (* KEEP = "TRUE" *) reg [`MSB_MOD:0] modulator;
  assign mod_value = modulator;
  assign dsample_w = dsample;
  always @ (negedge dsample)
  //duty cycle sampled at end of modulator period; broken up into delay line
  //    duty cycle and modulator duty cycle
  begin
    duty_DL[`MSB_DL:0] <= dutycycle[`MSB_DL:0];
    duty_Mod[`MSB_MOD:0] <= dutycycle[`MSB_DUTY:`DL_SIZE];
  end
  DelayLine DL1(.l_in(line_in), .l_out(DPWM), .sel(~duty_DL));
  always @ (posedge clk_2x or posedge reset)
  //Modulator implementation
  if (reset == 1)
    modulator <= 0;
  else
  begin
    modulator <= (modulator > `MAX_MOD_VALUE) ? 0 : modulator+1;
    line_in <= (modulator < duty_Mod) ? 1 : 0;  //Input to delay line
    dsample <= (modulator == `MAX_MOD_VALUE);   //sample new duty on overflow
  end
endmodule
```