GaN Microwave DC-DC Converters

by

Ignacio Ramos Franco

B.S., University of Illinois at Chicago, 2009

M.S., University of Colorado, 2013

A thesis submitted to the

Faculty of the Graduate School of the

University of Colorado in partial fulfillment

of the requirements for the degree of

Doctor of Philosophy

Department of Electrical and Computer Engineering

August 2016

This thesis entitled:

GaN Microwave DC-DC Converters

written by Ignacio Ramos Franco

has been approved for the Department of Electrical and Computer Engineering

_____

Zoya Popović

_____

Dragan Maksimović

Date _____

The final copy of this thesis has been examined by the signatories, and we find that both the content and the form meet acceptable presentation standards of scholarly work in the above mentioned discipline.

Ramos Franco, Ignacio (Ph.D., Electrical Engineering)

GaN Microwave DC-DC Converters

Thesis directed by Professor Zoya Popović

Increasing the operating frequency of switching converters can have a direct impact in the miniaturization and integration of power converters. The size of energy-storage passive components and the difficulty to integrate them with the rest of the circuitry is a major challenge in the development of a fully integrated power supply on a chip. The work presented in this thesis attempts to address some of the difficulties encountered in the design of high-frequency converters by applying concepts and techniques usually used in the design of high-efficiency power amplifiers and high-efficiency rectifiers at microwave frequencies. The main focus is in the analysis, design, and characterization of dc-dc converters operating at microwave frequencies in the low gigahertz range.

The concept of PA-rectifier duality, where a high-efficiency power amplifier operates as a high-efficiency rectifier is investigated through non-linear simulations and experimentally validated. Additionally, the concept of a self-synchronous rectifier, where a transistor rectifier operates synchronously without the need of a RF source or driver is demonstrated. A theoretical analysis of a class-E self-synchronous rectifier is presented and validated through non-linear simulations and experiments.

Two GaN class-E^2 dc-dc converters operating at a switching frequency of 1 and 1.2 GHz are demonstrated. The converters achieve 80 % and 75 % dc-dc efficiency respectively and are among the highest-frequency and highest-efficiency reported in the literature. The application of the concepts established in the analysis of a self-synchronous rectifier to a power amplifier culminated in the development of an oscillating, self-synchronous class-E^2 dc-dc converter.

Finally, a proof-of-concept fully integrated GaN MMIC class-E^2 dc-dc converter switching at 4.6 GHz is demonstrated for the first time to the best of our knowledge. The 3.8 mm $\times$ 2.6 mm chip contains distributed inductors and does not require any external components. The maximum measured dc-dc efficiency is approximately 45 %.

Dedication

A mis padres, por haberme inculcado la importancia y el valor de la educación ...

and to coffee and beer for helping me get here.

Personal Acknowledgments

It has been a great pleasure to experience graduate school with everyone in the CU microwave group. I would like to especially thank Andrew Zai, Sean "Honey badger" Korhummel, Scott Schaffer, Rob Scheeler, Mike Litchfield, and Mike Coffey for keeping the atmosphere in the lab fun and interesting and making grad school a very enjoyable experience. I'll always cherish DOTA breaks and the darts nights at downers.

I am very grateful to have worked with current and past members in the CU microwave group including Michael Roberg, Erez Falkenstein, Frank Trang, Jon Chisum, Dan Kuester, Xavier Palomer, David Sardin, Cesar Sanchez, Asmitha Dani, Jennifer Imperial, Mauricio Pinto, Gregor Lasser, Sushia Rahimizadeh, Parisa Momenroodaki, Patrick Blum, Jose Antonio Estrada, Allison Duh, William Haines, Jerome Cherome, Leonardo Ranzzani, and Maxwell Duffy.

Finally I would like to thank my parents, my brother Eloy, and my sister Maricela for all their support throughout the years.

Professional Acknowledgments

First I would like to thank my adviser Prof. Zoya Popović for funding me and giving me the opportunity to attend graduate school. I am thankful for all the knowledge and professional advice she has bestowed on me. I would also like to thank Prof. Dragan Maksimović for all the time and guidance he provided me with through my studies at CU Boulder. Dr. Tibault Reveyrand deserves special recognition for helping me with anything related to non-linear modeling and for serving as a measurements guru. I would also like to thank Prof. Jose Angel García from the University of Cantabria for all the useful comments, edits, and for being an excellent collaborator.

I'm also very thankful to the rest of the members of my PhD committee and all the other professor from the University of Colorado who have taught me so much including Prof. Edward Kuester, Prof. Dejan Filipović, and Prof. Khurram Afridi. Additionally, my undergrad adviser Prof. Danillo Erricolo from the University of Illinois at Chicago deserves credit for encouraging me to attend graduate school.

I would like to thank ARPA-E for funding most of the research presented in this thesis under the ADEPT program and ARPA-E IDEAS. Additionally, I extend my gratitude to QORVO, especially Dr. Charles Campbell for all his help and advise to the entire CU microwave group.

Contents

List of Tables

List of Figures

Chapter 1

Introduction

The research presented in this thesis addresses fundamental concepts involved in designing dc-dc converter circuits that operate at frequencies that are three orders of magnitude higher than current high-speed converters in commercial power supplies. The miniaturization and integration of the power supply and voltage regulators in a system can achieve significant improvements in the overall miniaturization and manufacturability of electronics. Traditional switching power supplies are very efficient, reliable, robust, and are well understood. However, the manufacturing focuses on the assembly of modules or bricks from discrete components, instead of focusing on integrated hardware solutions derived from semiconductor and microelectronics technologies [7]. A traditional 10-W dc-dc converter module from TI is shown in Fig. 1.1. It can be observed that discrete passive components take a significant portion of real estate in the converter module. In specific, magnetic components such as inductors and transformers, have been proven difficult to effectively integrate with the rest of the converter.

The size and value of energy-storage components such as capacitors, inductors, and transformers, is inversely proportional to frequency. Fundamentally, increasing the switching frequency of power converters should reduce the size of converters to be as compact as possible. There are, however, practical constraints that severely limit the switching frequency of converters. The leading cause being a severe decrease in efficiency by a number of factors exacerbated at higher frequencies.

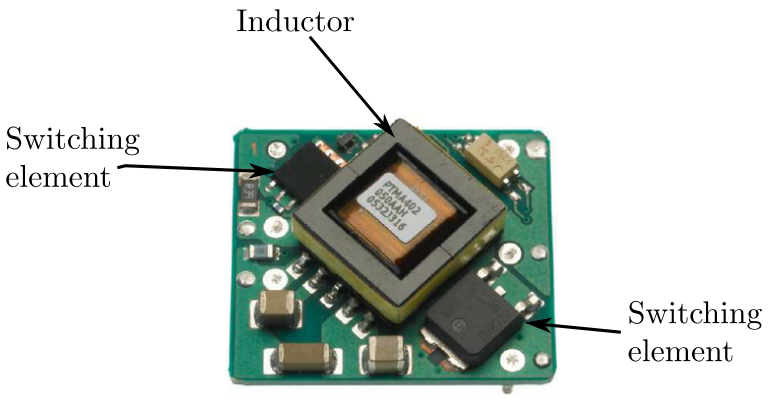


Figure 1.1: Photograph of a traditional 10-W dc-dc converter module from Texas Instruments. The model is the PTMA403033

Increasing the switching frequency of of dc-dc converters with a goal of reduced size, faster transient response, and increased power density was attempted early in the development of switching converters [8–10]. Nonetheless, recently there has been a renewed interest in increasing the operating frequency of converters [11–14] encouraged by the availability of wide-bandgap semiconductors and higher performance, fast transistors. For instance, part of this thesis was funded by the Agile Delivery of Electrical Power Technologies (ADEPT) program from the Advanced Research Project Agency-Energy (ARPA-E). The ADEPT program funded several teams to develop and demonstrate the effectiveness of SiC and GaN devices in power converters. Moreover, in 2013 ARPA-E launched the SWITCHES (Strategies for Wide Bandgap, Inexpensive Transistors for Controlling High-Efficiency Systems) program, which focuses on the development of high voltage (1200 V) high current (100 A) single die power semiconductor devices using SiC, GaN, and diamond [15].

Lately, the European Union program for research and technological development FP7 funded the project "'Power Supply With Integrated PassivEs" or PowerSwipe. The PowerSwipe consortium proposed to develop the next generation Power Supply in Package (PwrSip) and Power Supply on Chip (PWrSoC) technology platforms by investigating innovations in integrated power passives, nanoCMOS technologies, and advanced packaging [16]. The inability to integrate the power passive components for high efficiency dc-dc converters was determined to be a major roadblock in the integration of low efficiency linear regulators, switched

capacitors converters, and switched-mode dc-dc converters with the micro-controller SoC. A review of high frequency, highly integrated inductive dc-dc converters is shown in [17], where all but one of the converters are implemented in Si-CMOS and are therefore limited to low voltage, and low power.

The work presented in this thesis attempts to address some of the difficulties encountered in the design of high-frequency converters by applying concepts more commonly used in the design of high-efficiency power amplifiers and rectifiers at microwave frequencies. Fundamentally, a resonant dc-dc converter is composed of three main blocks as shown in Fig. 1.2: a dc-ac converter implemented as an inverter, an amplifier or an oscillator; a resonant coupling network that can be realized with inductors and capacitors; and an ac-dc converter implemented by a diode or transistor rectifier circuit. High-efficiency in PAs and rectifiers at microwave frequencies is obtained by wave-shaping through harmonic terminations that enable low power dissipation at the switching element. Load pull is an essential tool that facilitates determination of matching impedances that enable design of wave-shaping networks [18–20] and can applied to the resonant converter from Fig. 1.2.

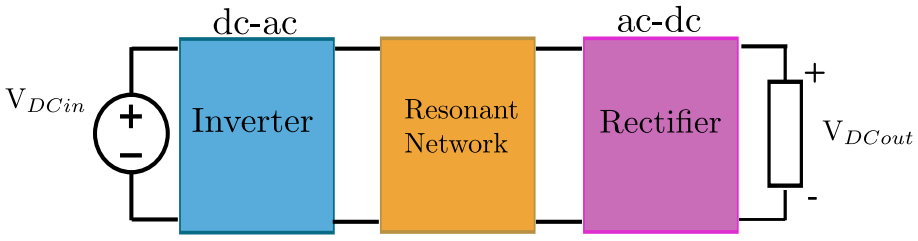
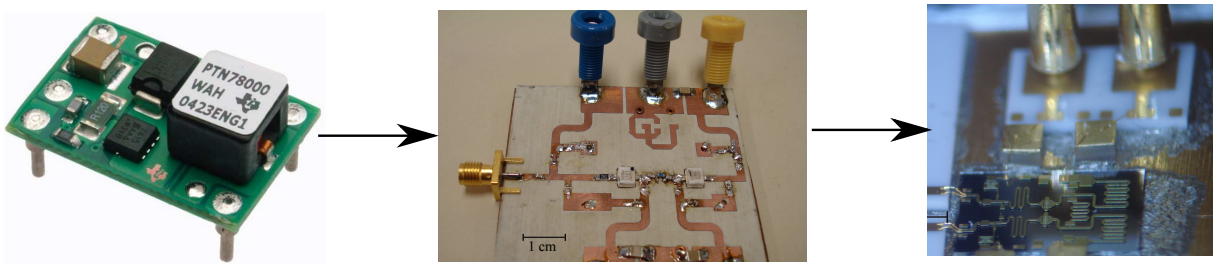


Figure 1.2: High-level block diagram of a resonant dc-dc converter

The main goal of the thesis is illustrated in Fig. 1.3. The first part of the thesis investigates different configurations of the fundamental resonant converter shown in Fig. 1.2 to first realize a hybrid dc-dc converter operating in the 1-GHz region which is implemented on a printed circuit board with low-profile components. The substantial increase in switching frequency is pursued to later explore the possibility of a monolithically integrated dc-dc converter using processes normally used in monolithic microwave integrated circuits (MMICs) where the implementation is with transmission lines. Because of the high switching frequencies, GaN on SiC high electron mobility transistors (HEMTs) are used in all the designs instead of the more typical metal-oxide-semiconductor field-effect transistor (MOSFETs).



Commercial TI dc-dc converter

Hybrid GHz dc-dc converter

Integrated MMIC dc-dc converter

Figure 1.3: Progression of the design of the GHz dc-dc converter compared to a commercial example. The goal of the thesis is to first design a watt level hybrid dc-dc converter operating around 1 GHz with a low profile on a PCB using GaN on SiC Microwave transistors. After realizing a 1 GHz converter, complete monolithic integration is pursued to achieve a monolithically integrated dc-dc converter, with the GaN chip (2.3×3.8 mm) shown on the right.

1.1 Thesis outline and chapter overview

The organization of this thesis and a summary of each chapter are presented below.

Chapter 2 presents an overview of important concepts and some of the challenges encountered in the design of high-frequency converters. The discussion provides a basic understanding of the main problems encountered in the design of dc-dc converters at high frequencies, as relevant to this thesis. Switching losses associates with FET transistors are first overviewed, followed by a review of high-frequency losses in magnetic components commonly used in dc-dc converters. The advantages of wide-bandgap semiconductor devices, such as gallium nitride HEMS are discussed along with a comparison with typical Silicon power MOSFETs.

Chapter 3, details the concept of time-reversal duality for PAs and rectifiers proposed originally by David C. Hamill in 1990, and applies the concept to microwave dc-dc converters. Analysis of a class-E rectifier and the design of a class-E^2 dc-dc converter is also shown together with non-linear simulations of a GaN transistor operating as a PA and as its time-reversal dual rectifier. Further, experimental validation of the time-reversal results are given on the example of a 2.14 GHz class-F^{-1} PA as a power amplifier and as a rectifier. Finally, an idealized theoretical analysis of a class-E self-synchronous rectifier is given. The proposed analysis is validated using nonlinear harmonic-balance simulations and measurements.

Chapter 4 presents the design and experimental demonstration of class-E^2 dc-dc converters operating around 1 GHz. The design methodology relies on PA-rectifier duality and the design of a high-efficiency class-E^2 converter consisting of a high-efficiency class-E RF power amplifier and a high-efficiency class-E power rectifier presented in Chapter 3. Synchronous, self-synchronous, and oscillating, self-synchronous converters are demonstrated with hybrid circuits using GaN on SiC packaged HEMTs. The oscillating, self-synchronous converter is part of a collaboration with Prof. Jose Angel Garciá from the University of Cantabria in Santander, Spain. The efficiency of this 1-GHz converter reaches nearly 80 % with over 10 W of output dc power.

Chapter 5 demonstrates the feasibility of a resonant converter consisting of only distributed passive components. A completely distributed class-E^2 dc-dc converter is designed in Qorvo's 0.15 μm GaN on SiC process as a proof-of-concept demonstration of a fully monolithically integrated dc-dc converter. A detailed description of the MMIC design is given. The distributed converter is then measured with the rectifier driven synchronously and a manual external tuner is used to operate the rectifier self-synchronously. Finally, losses in the converter and efficiency improvements are addressed.

The microwave dc-dc converters from chapter 3-5 all contain a PA(inverter) reactively coupled to a rectifier. This coupling is implemented with capacitors and inductors, but can also be accomplished using impedance transformers (such as the ones presented in appendix B), or through electric and magnetic fields more generally.

In Chapter 6, the concepts from previous chapters are applied to wireless power transfer (WPT), where the coupling between the PA and the rectifier from Fig. 1.2 is accomplished through electric and magnetic near-fields. Near-field wireless power transfer has been most commonly done using inductive coupling at lower frequencies (100 kHz-13 MHz). The applications range from sub-watt implants to electric vehicles and industrial machinery. In this chapter, an array approach to capacitive WPT aimed at a modular and scalable system for charging electric vehicles is presented. The goal of the distributed array approach is to increase maximum transferable power while decreasing the fringing electric field produced by the WPT system, accomplished by field focusing through phase control. In this kW-level WPT system, the full-bridge inverter and rectifier are designed by Prof. Kurram Afridi and the power electronics group at the University

of Colorado at Boulder, while the goal of the work presented in this thesis is to determine the focusing effects at different frequencies and for several array configurations and relative phasing between the modules is shown. The primary frequencies of interest are the 6.78, 13.56 and 27.12 MHz ISM bands.

Specific contributions of the thesis are discussed in the concluding chapter, a long with some directions for future work. Most of the content of this thesis has been published in [21–26].

Chapter 2

Background for High Frequency DC-DC Converters

Contents

This chapter presents an overview of important concepts and some of the challenges encountered in the design of high-frequency converters. The discussion provided in this chapter is not intended to serve as a comprehensive review of high-frequency dc-dc converters or power electronics, it only aims to provide a basic understanding of the main problems encountered in the design of high-frequency converters that are relevant to this thesis. For a more comprehensive analysis of power electronics, the reader is referred to "Fundamentals of Power Electronics" by Erickson and Maksimović [27].

The chapter is divided as follows: Section 2.1 overviews switching losses associates with FET transistors in high-frequency converters. In Section 2.2, high-frequency magnetic components commonly used in dc-dc converters are reviewed briefly. Section 2.3 shows a brief overview of the advantages wide bandgap semiconductor devices such as gallium nitride devices have over typical Silicon power MOSFETs.

2.1 DC-DC CONVERTERS AT HIGH FREQUENCIES AND SWITCHING LOSSES

Increasing the switching frequency of dc-dc converters to just the VHF range between 3-300 MHz brings with it a plethora of opportunities as well as challenges [11]. [12] presents a summary of the evolution of very high frequency (VHF) power supplies. The merger of circuit techniques used in radio frequency power amplifiers and those used in classical power electronics starts to develop at VHF frequencies. Power amplifiers are generally divided in classes characterized by the amount of time the power transistor conducts. A class-A power amplifier conducts 100 % of the time and has a maximum theoretical efficiency of 50 % . A class-B PA conducts 50 % of the time and has a maximum theoretical efficiency of 78.5 %. A class-C PA conducts between 0-25 % of the time and has a theoretical maximum efficiency of 100 %. These amplifier classes are the power electronics equivalent of linear regulators; detailed analysis of their operation is shown in [19, 28, 29] and will not be repeated here.

A class-D PA, first invented by Baxandall in 1959 [30] is considered a switching power amplifier because the power transistor is operated as a switch. The class-D PA has a maximum theoretical efficiency of 100 % and does not suffer from high voltage levels at the power transistor. The power electronics equivalent to the class-D amplifier are typically the half-bridge and full-bridge converters. Detailed analysis of class-D amplifiers is shown in [29].

Class-F and class-F^{-1} PAs introduced by Tyler in 1919 [31] utilize harmonic resonators to shape the voltage and current across the switching element in order to minimize current and voltage overlap and consequentially minimize power dissipation in the transistor. Class-F PAs can achieve very high efficiencies and have been widely used to improve efficiency of RF transmitters. The power electronics equivalent topologies are multi-resonant converters that use zero-voltage (ZVS) or zero-current (ZCS) switching techniques. When

a circuit operates in ZVS, the transistor turns ON when there is zero voltage across the transistor, and when it operates in ZCS, the transistor turns OFF at zero current. A more detail explanation of ZVS is shown below. Similarly, the class-E PA first introduced by Sokal in 1975 [32], displaces the current and voltage waveforms with respect to time to avoid power dissipation at the transistor. The ideal class-E PA not only achieves ZVS but it also achieves zero voltage-derivative switching (ZVDS), hence the switching losses are either eliminated or significantly reduced. Because power converters are required to be efficient, high-frequency designs focus mainly around switching or harmonically terminated circuits such as the class-D, class-F, and class-E amplifiers.

2.1.1 High-frequency switching losses and soft switching

There are several ways in which a semiconductor device operating as a switch can incur losses generally attributed to "switching losses." The reverse-recovery process of a diode, dissipated energy stored in the output capacitance of a FET, or losses due to the current tailing typical of thyristors and IGBT are some known examples. Because the majority of the designs presented in this thesis use a High Electron Mobility Transistor (HEMT), which is a form of Field Effect Transistor (FET) [33], only the switching losses most common to FETs are addressed.

The ON-OFF and OFF-ON transition of switching converters can be classified as hard-switched, zero-current switched , or zero-voltage switched. Generally, when a transistor employs ZVS and ZCS during the switching transitions, it is said to use soft switching. Circuits with hard-switched operation such as PWM converters depend on voltage and current waveforms changing abruptly from a high value to zero when the switch is turned ON and OFF. In FETs, and specifically HEMTs, the majority of the switching losses occur due to the energy stored in the output capacitance of the transistor. When the transistor is switched OFF, there is almost no loss, because the output capacitance of the transistor holds the voltage across the transistor at nearly zero volts, and the current that was previously flowing through the switch, starts flowing through the output capacitor. However when the switch is turned ON, the energy stored in a FET output capacitance at the time the switch is turned ON, is completely dissipated in the transistor's ON resistance. Fig. 2.1 shows a simplified comparison between the voltage and current waveforms of a transistor operating under

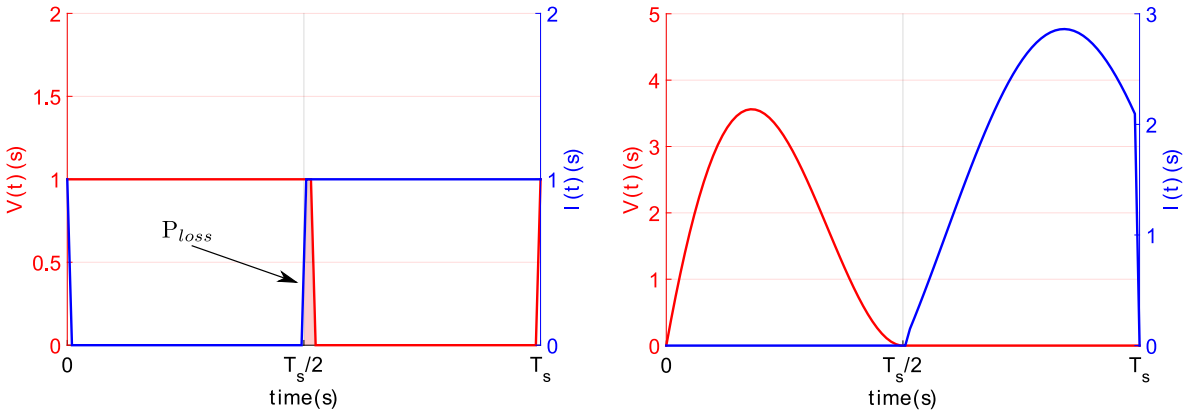


Figure 2.1: Voltage and current waveforms comparison between a hard-switch transition (a) and the soft-switching transition of a class-E amplifier (b). The voltage and current waveforms are normalized to the voltage and current of the supply.

hard-switching and a transistor operating under soft-switching conditions.

The energy stored in the output capacitance of the transistor is given by

$$W = \frac{1}{2} C_{out} V^2 \tag{2.1}$$

and depends only on the output capacitance and the voltage across the transistors. Hence reducing the ON resistance of the transistor has no effect in the switching power lost and since C_{out} is an inherent parameter of the transistor, the only option left is to ensure the transistor turns ON when there is zero voltage across the switch. This is one of the reasons why ZCS has little to no effect in the switching losses of MOSFETS [27] or why the ZCS class-E PA is not as efficient as the ZVS version [29]. Furthermore, the total switching power loss is given by

$$P_{loss} = \frac{1}{2} f C_{out} V^2 \tag{2.2}$$

which increases linearly with frequency. Thus, at high-frequencies it is imperative to operate the transistor in ZVS. A simplified model of the parasitic components that cause loss in a MOSFET presented in [34] is shown in Fig. 2.2. The model ignores the coupling drain to gate capacitance C_{gd}. R_{on}, R_{dis} and R_g correspond to conduction loss, displacement loss, and gating loss, respectively. C_{in} and C_{out} are the input

and output capacitance, while C_{ext} is the external capacitance. Conduction loss is proportional to R_{on} and independent of frequency. However, both i_{disp} and i_{gate} are directly proportional to frequency because the impedance of both C_{in} and C_{out} decreases linearly with frequency. Furthermore, because gating losses and displacement losses are of the form i^2R, the losses are proportional to f^2. Table 2.1 summarizes the losses in hard-switched and soft-switched converters and how they scale with frequency.

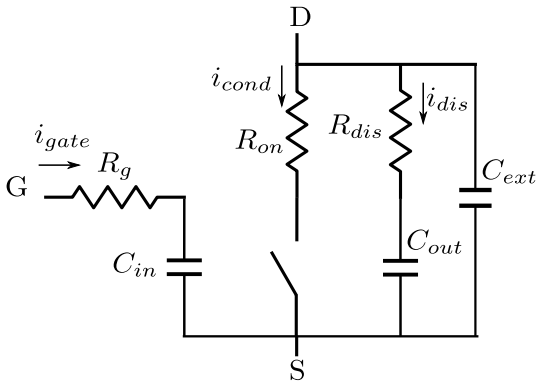


Figure 2.2: Simplified model of a MOSFET and the main parasitic components that cause power loss. The simplified model ignores the coupling drain to gate capacitance C_{gd}.

Table 2.1: Soft-switched vs. hard-switched loss

Loss	Hard-switched	Soft-switched
Conduction	$i^2_{cond,RMS}R_{on}$	$i^2_{cond,RMS}R_{on}$
Gating	$C_{in}f_{sw}$	$C^2_{in}R_{gate}f^2_{sw}$
Off-state conduction	N/A	$C^2_{out}R_{dis}f^2_{sw}$
Overlap	f_{sw}	N/A
Cap. discharge	$C_{out}f_{sw}$	N/A

There has been extensive research and many topologies have been proposed to achieve soft switching via resonant converters [35, 36] or by modifying PWM converters by implementing resonant switches [37, 38]. More recently, architectures suitable for VHF operation are presented on [39, 40], where an unregulated 100 MHz converter consisting of a class-E inverter with a self-oscillating gate driver and a resonant rectifier achieved 75 % efficiency at 4 W output power. A feedback network provides the required phase shift between the fundamental component of the drain voltage and the gate signal to attain sustain oscillations

and minimize gating losses. Similarly in [41], a class-E inverter with a self-oscillating gate driver and a class-E rectifier using a shunt diode achieved 55 % efficiency with an output power of 1.7 W switching at approximately 100 MHz. In both cases conduction losses due to the ON resistance of the transistor R_{on} and conduction losses in the resonant inductors contribute to most of the power losses. This highlights one of the main disadvantages of using resonant topologies. Resonant topologies transfer power at the fundamental frequency component, as opposed to PWM converters that transfer power at DC, fundamental frequency, and harmonics. This causes very high current and voltage peaks through resonant networks and switching elements. The high-current spikes cause an increase in conduction losses that can sometimes undermine or even outweigh the reduction in switch losses at high frequencies. Additionally, resonant topologies are optimized for a single load and their performance declines when operating with a big range of loads.

Most of the recent work at VHF has focused on class-E converters or derivatives of it. Class-E PAs and class-E rectifiers offer the advantage of an additional degree of soft switching achieved by enforcing not only ZVS but ZDVS or zero derivate voltage switching. Enforcing ZDVS means that not only is the voltage across the switch zero when the switch turns ON, but the derivative of the voltage across the switch is also 0. A class-E inverter enforces both ZVS and ZDVS only for the optimum design load R_{opt}. However, a class-E inverter can still operate under ZVS for a load $0 > R > R_{opt}$ with the use of an anti-parallel or a series diode ensuring low to non-existent switching losses. A detailed analysis of a class-E^2 dc-dc converter is shown in subsection 3.2.1

2.2 Magnetics

Magnetic components such as inductors and transformers have been a bottleneck in the development of high frequency and integrated power converters. Not only are magnetics usually the largest component of a converter, making integration difficult or impossible, but magnetic components used at high frequencies fail to achieve comparable electrical performance to their low frequency counterpart. Transformers are seldom used at frequencies above a couple of megahertz because of the increase in losses with frequency, hence this section will focus on inductors used in resonant circuits. Losses in a resonant inductors can be generally

divided into core losses and winding losses. At frequencies used in this thesis (>1 GHz), magnetic and ferrite cores have high loss, and are therefore not considered.

Using low permeability RF materials [42], can extend the performance of cored inductors up to the HF region (3-30 MHz) but not much more. Currently available cored magnetics thus present a fundamental frequency limit and therefore high frequency magnetic component have to rely on coreless or air-core designs. Air-core inductors are inductors without a magnetic core, the actual core of the inductor does not need to be air and can be made out of a dielectric. The majority of the inductors used in UHF and microwave frequencies are built with a core made out of ceramic. Up to date, most if not all the inductors used in power converters operating above 50 MHz are [7] either discrete or on-chip integrated air-core inductors. Even in the development of on-chip integrated inductors, core losses present a limit in operating frequency. A comparison between the performance of an air-core inductor and a magnetic-core inductor on silicon is shown in [1]. The magnetic-core inductor is a racetrack design and the air-core inductor is a square spiral design, both are described in [43]and are shown in Fig. 2.3 It is found that the magnetic-core inductor performs better up to 50 MHz, but the air-core inductor performs similar or better from 70-100 MHz due to high eddy current loss in the core material.

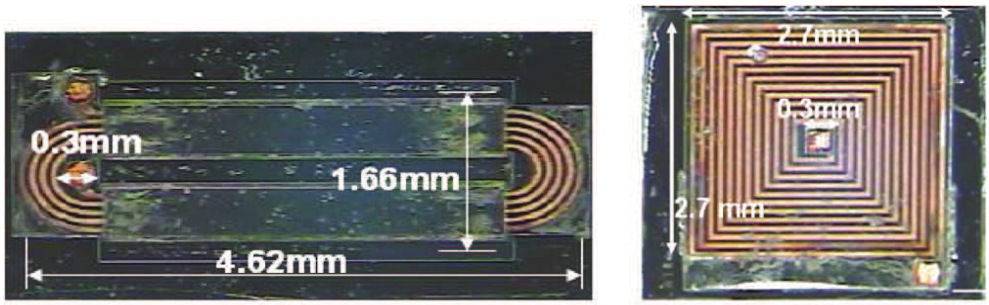


Figure 2.3: Top view of (a) fabricated magnetic-core microinductor and (b) air-core inductor compared in [1]

2.2.1 Winding losses

As shown in the previous section the use of cored inductors is limited to the VHF region, therefore circuits operating at higher frequencies are required to use coreless or air-core inductors. In an air-core inductor

conduction losses produced by the resistance of the conductor are the main source of loss. At DC and lower frequencies, the power loss in the windings can be simply expressed as

$$P_{cu} = I_{RMS}^2 R_{DC} \tag{2.3}$$

however, at high frequencies, eddy-currents induced in the winding conductors can increase winding losses via the skin effect and the proximity effect. The skin effect causes high-frequency currents to congregate at the surface of the conductor without penetrating to the center of the conductor, effectively reducing the cross-sectional area. The skin depth of a conductor is given by

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}} \tag{2.4}$$

where ρ is the resistivity of the conductor, f is the frequency of the current waveform, and μ is the permeability of the conductor which is equal to μ_0 for most conductors. The penetration depth of a copper conductor is

$$\delta = \frac{7.5}{\sqrt{f}} cm \tag{2.5}$$

Additionally, a conductor carrying a high-frequency current produces a field that can induce more complex eddy-currents in other windings. The proximity effect can sometimes increase the effective ac resistance R_{ac} more than the skin effect [44]. There are two approaches to mitigating the proximity effect. One is to use conductors that are small compared to the skin depth to avoid giving room for eddy-currents to circulate in a conductor. An example is the use of litz-wire in in wire-wound components [45]. The other approach, is the configuration of the windings in a single layer in such a way that the current can flow on the surface of that layer in a region one skin-depth deep [46].

In the case of air-core inductors, specially inductors used for RF application, the performance of the component is usually quantified by the quality factor Q. Where Q is the ratio between inductive and resistive impedance magnitudes and can be expressed as

$$Q = \frac{\omega L}{R_{ac}} \tag{2.6}$$

Typical Q values of RF inductors are approximately in the 50-100 range. Table 2.2 shows a comparison of some of the 10-nH low profile air-core RF inductors from Coilcraft®. The Q of all of the inductors is less than 100 at approximately 1 GHz. The high-frequency resistance can be obtained from the Q values provided by the manufacturer. For example, all of the discrete inductors used in the designs of the converter presented in Chapter 4 are non-magnetic inductors with a ceramic core from Coilcraft®. According to [47], all of the frequency dependent losses are included in the measurement of Q, including skin effect, proximity effect, and core losses when relevant.

Table 2.2: Typical RF inductors from coilcraft

Part number	Inductance (nH)	Q	SRF (GHz)	DC resistance (mΩ)	Irms (mA)
0402HP-10NX-L	10	62 @ 900 MHz	4.70	110	1300
0603HP-10NX-L	10	90 @ 900 MHz	4.30	48	1400
0805HT-10NT-L	10	55 @ 750 MHz	3.30	80	800
0807SQ-10N_L	10.2	100 @ 400 MHz	4	7	2700
1606-9_L	9.85	100 @ 800 MHz	5.2	13	1600
1606-9_L	9.85	100 @ 800 MHz	5.2	13	1600

2.3 Semiconductor device technology

For high-frequency dc-dc converters to offer comparable performance to readily available low frequency converters, the semi-conductor device used as the switching element is required to have exceptional electrical characteristics. The output capacitance C_{out}, the input capacitance C_{in}, and the ON resistance R_{ON} are of particular importance for high-efficiency. Typical MOS devices used in power converters can efficiently operate into the low VHF region but not much higher than that. [48] shows a comparison of MOS devices operating above 30 MHz. A list of 10 devices the authors identified as good candidates for high-frequency operation under soft-switching, and soft-gate switching is provided. The authors note that a subset of the

devices shown has been used to realize designs operating up to 110 MHz at tens of Volts. Silicon devices are generally limited by low breakdown field, low thermal conductivity (operating at junction temperature around 200° C) and limited switching frequency. Wide band-gap semiconductors such as GaN, SiC, and diamond offer the potential to overcome all of the limitations of silicon technology except current price. Various properties of wide bandgap semiconductors are summarized in Table 2.3 for comparison with silicon [49]. A wider band-gap means the semiconductor device has higher activation energies and can operate at higher voltages and higher temperatures. High-electron mobility is related to high-frequency operation, while high saturation drift velocity is directly proportional to high-frequency switching capabilities [50].

Diamond offers the highest bandgap, highest electric-breakdown field, highest thermal conductivity, and highest saturated E-drift velocity. Nonetheless, research in diamond semi-conductors is at an infant stage and currently diamond has a number of problems related to device fabrication that need to be solved before it becomes a viable technology [49, 50].

Table 2.3: Table of properties of major wide band-gap materials

Material	μ_n Electron mobility (cm^2/Vs)	μ_p Hole mobility (cm^2/Vs)	ϵ_r Dielectric constant	E_g Bandgap (eV)	E_c Breakdown field (kV/cm)	λ Thermal Conductivity (W/cm-K)	V_{sat} Saturated E-drift velocity (cm/s)
Si	1450	450	11.7	1.12	300	1.3	10^7
GaAs	8500	400	12.9	1.4	400	0.54	2×10^7
6H-SiC	415	90	9.7	2.9	2500	5	2×10^7
GaN	1000	350	8.9	3.39	5000	1.3	2×10^7
Diamond	2200	1800	5.7	5.6	56000	20	3×10^7

GaN devices are the obvious candidate to replace LDMOS and GaAs in RF and microwave applications due to their high frequency performance at a higher voltage. In specific, the GaN HEMT can alleviate many of the problems presented by LDMOS devices, such as low input and output impedances. The material properties of GaN HEMTs, such as breakdown field, mobility, and speed, lend themselves to high-power switching applications with a projected V_{BR}^2/R_{ON} hundred times larger than in silicon [49].

The lack of a readily available GaN substrate requires heteroepitaxy on compatible substrates, silicon,

sapphire and SiC are commonly used. With the right composition, a 2-dimensional electron gas (2DEG) forms at the AlGaN/GaN interface allowing very high electron mobility between the drain and source electrodes. The channel between the drain and source can be directly controlled by the gate-source voltage [51]. A simplified structure of a GaN HEMT is shown in Fig. 2.4.

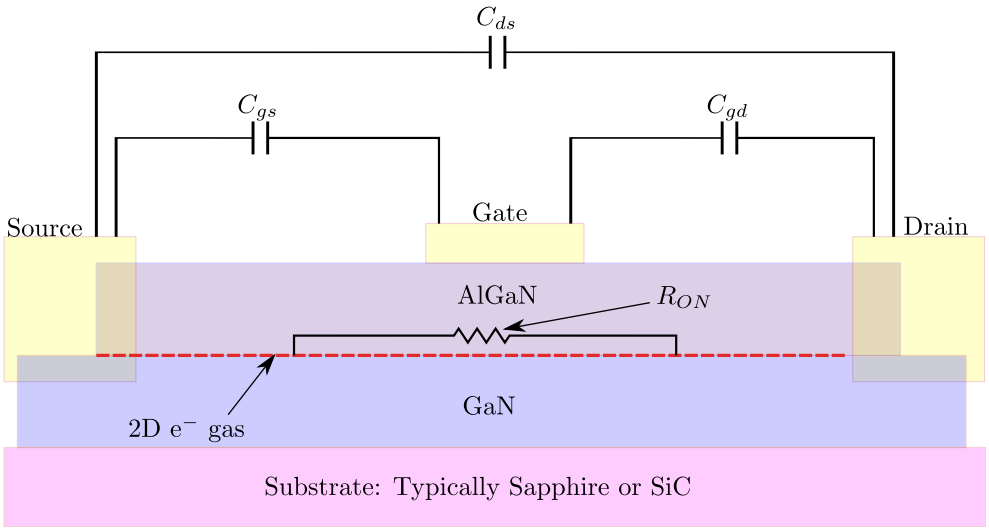


Figure 2.4: Simplified GaN HEMT structure and main parasitic components.

The largest market for GaN HEMTs is in optoelectronics, RF, and microwave applications [50, 51], however GaN on silicon is expected to be the future of medium voltage power applications [52]. Consequentially, the majority of GaN HEMT devices available are generally optimized for linearity and gain at a broad range of frequencies, and not for switching power converters. In [53], a GaN HEMT typically used for microwave applications is characterized as a switch and implemented in conventional PWM converters. The transistor used is the TGF2023-02 form Qorvo (previously TriQuint semiconductor), like the majority of the state of the art RF GaN HEMTs, is a depletion mode device. A depletion mode device is a transistor normally ON that requires a negative gate-source voltage to turn off. The measured drain to source capacitance C_{ds} is less than 1 pF, and the measured R_{on}= 1 Ω. A rise time lower than 1 ns was obtained experimentally using he transistor as a resistive switch and in a floating buck converter. It is important to note that the authors experienced stability issues even while performing simple DC measurements. This is because as previously mentioned, the HEMT is optimized for high gain at a broad range of frequencies, which can produce unwanted oscillations caused by internal feedback through the device intrinsic capacitances.

A high-frequency silicon LDMOS device and a GaN HEMT are compared for VHF applications in [11]. The main parameters are reproduced below. Although, R_{on} is similar in both devices, the input and output capacitance of the GaN device is significantly smaller. Thus, the losses given by RC^2 are much smaller and the device can operate at higher frequencies.

Part Number	Description	R_{on} (mΩ)	R_g(mΩ)	C_{gs} (pF)	C_{ds} (pF)	V_{br} (V)
MRF6S9060	Si LDMOS	175	135	110	50	68
CGH40045	GaN HEMT	200	?	19	8.3	100

2.4 Summary and conclusion

This chapter is meant to highlight some of the difficulties and limitations encountered in the design of high-frequency dc-dc converters and possible ways to circumvent them. In the next chapters, some of the concepts introduced here will be applied to the design of resonant dc-dc converters operating at microwave frequencies. At frequencies above a few megahertz, circuits typically used in the design of RF power amplifiers merge with circuits used in dc-dc converters. Switching losses at high frequencies require the use of resonant converter operating under ZVS to avoid power loss caused by the overlap between the current and voltage waveforms at the switching element, and by the discharge of the output capacitance of a transistor when the transistor turns ON. Magnetic components above 50 MHz are limited to air-core or coreless designs due to an increase of losses in the core material proportional to frequency. The use of wide bandgap devices allows for much higher switching frequencies because of their low C_{out} and high power due to their high-voltage breakdown.

Chapter 3

Power Amplifier (PA)-Rectifier Duality

Contents

3.1 Introduction

In the design of high frequency converters, a different approach from traditional hard-switching pulse width modulated (PWM) dc-dc converters has to be adopted. As discussed in Chapter 2, several topologies have been proposed in recent years to mitigate some of the problems that arise with more traditional PWM converters at higher frequencies. However, this can prove a difficult transition for engineers and designers due to the different techniques and design methodologies used at UHF-GHz frequencies. Although most of the research in high-frequency dc-dc converter has been focused in VHF (30-300 MHz) and very limited research has been done in the area of UHF-GHz dc-dc converters, there has been a significant increase in research in the area of high-efficiency switching power amplifiers in the last 30 years, driven by the raise of the cellular-communication industry. One of the main goals of this thesis is to leverage the vast knowledge available for power amplifiers at microwave frequencies and apply it to the development of UHF-GHz power converters. Furthermore, with the advent of commercially available (GaN) on SiC microwave transistors, medium-power UHF-GHz dc-dc converters have become an interesting topic worth exploring.

To take advantage of well-known techniques in power amplifier design, the concept of time-reversal duality proposed by David C. Hamill in 1990 is investigated in the application of microwave dc-dc converters. Section 3.2 presents the concept of the principle of time reversal duality and the analysis of a class-E^2 dc-dc converter and the duality between a class-E PA and a class-E rectifier. Section 3.3 presents non-linear simulations of a GaN transistor operating as a PA and as its time-reversal dual rectifier. Both simulations are performed with an improved non-linear model of a GaN transistor presented in [4, 5]. Section Section 3.4 experimentally validates the time-reversal results simulated in Section 3.3, by measuring a 2.14 GHz class-F^{-1} PA as a power amplifier and as a rectifier. Finally, in Section 3.5, an idealized theoretical analysis of a class-E self-synchronous rectifier is given. The proposed analysis is validated using nonlinear harmonic-balance simulations and measurements.

3.2 Time reversal duality and the class-E^2 converter

The concept of time-reversal duality as it applies to inverters and rectifiers was introduced by David C. Hamill in [54] and recognized before that by Severns [55, 56]. The principle relates the voltage and current time-domain waveforms of an inverter and a rectifier. Time reversal duality suggests that for a network A (in this case an inverter), there exists a network A^+ (a rectifier) such that the waveforms of one are time-reversed versions of the other. For instance, a voltage waveform $v(t)$ in an inverter becomes a voltage $v(-t)$ in a rectifier. Table 3.1 summarizes the electrical circuit relationships between a network and its time-reversed dual.

Table 3.1: Summary of electrical quantities and their time-reversal equivalents

	Original network	TR-dual
Voltage	v(t)	v(-t)
Current	i(t)	-i(-t)
Power	p(t)	-p(-t)
Inductance	L	L
Capacitance	C	C
Resistance	R	R

As observed in Table 3.1, most quantities are time reversed but otherwise they remain unchanged. The only exception is current and power. Both quantities change sign and become negative quantities with respect to the original network. The change in sign of power only represents the direction of the power with respect to the original network.

3.2.1 Synthesis of a class-E^2 DC-DC Converter

A number of dc-dc converter topologies can be be generally described as a number of fundamental two-port blocks cascaded as shown in Fig. 3.1. Each converter consists of an input filter, an inverter, a matching network, a rectifier, and an output filter. The six basic topologies: buck, boost, buck/boost, Ćuk, SEPIC and dual SEPIC can be described in such a way [57].

An example of time-reversal duality is the synthesis of a double class-E or class-E^2 dc-dc converter as

Figure 3.1: Diagram of the synthesis of dc-dc converters by cascading fundamental two-port networks

presented by Hamill. The class-E^2 converter has been researched greatly for high frequency applications and is a significant component of this thesis. Fig. 3.2 shows the classical class-E PA first introduced by Sokal in [32]. The FET transistor operates as an ideal switch with a duty cycle D. The RF choke is assumed ideal and only dc current flows through it. C_{out} is the output capacitance of the transistor. The series resonator is tuned to resonate just below the switching frequency ω_s, presenting an inductive reactance X to the switch. The current flowing through the resonator is sinusoidal at the switching frequency ω.

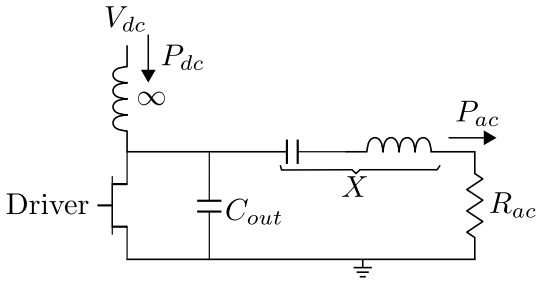


Figure 3.2: Schematic of ideal Class-E power amplifier

Detail analysis of the operation of the PA has been presented extensively in [29, 58, 59] and will not be repeated here. The main results for the class-E PA are summarized below and a class-E rectifier is analyzed in the next subsection. Looking at Fig. 3.2, optimum operation occurs at a duty cycle $D = 0.5$ and with the following impedance presented to the output capacitance of the switch.

$$R_{ac} = \frac{0.1836}{\omega C_{out}} \tag{3.1}$$

$$X_{ac} = \frac{0.2116}{\omega C_{out}} \tag{3.2}$$

During optimum operation, the equivalent impedance the PA presents to the dc supply is equal to

$$R_{dc} = \frac{1}{\pi\omega C_{out}} \tag{3.3}$$

3.2.1A Analysis of a class-E rectifier

To analyze a class-E rectifier, the circuit shown in Fig. 3.3 is used along with the following assumptions [60]:

(1) The switch in the rectifier is ideal with R_{on}=0 and $R_{off} = \infty$ and the output capacitance C_{out} is linear.

(2) The rectifier is driven by an ideal sinusoidal current source i.

(3) The RF choke is ideal and the ac ripple on the dc current I_0 is negligible.

(4) The rectifier switches when there is zero voltage across the switch v_{sw}. Hence, $v_{sw}(0) = 0, v_{sw}((2\pi(1-D)) = 0$.

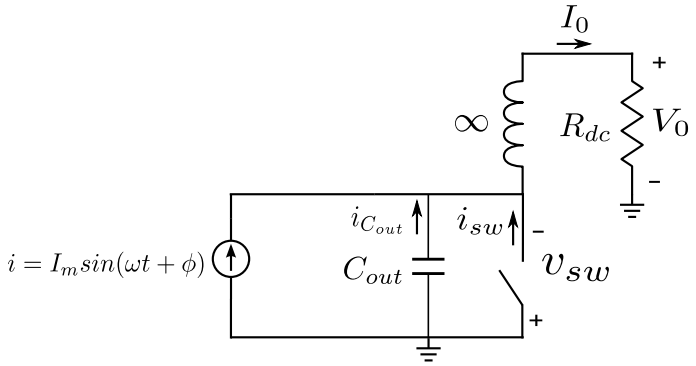


Figure 3.3: Class-E rectifier circuit

Starting with the assumptions that the RF choke in Fig. 3.3 is large enough so that the output filter and load resistance can be replaced by a current I_0. The rectifier can be replaced by the simplified circuit from Fig. 3.4.

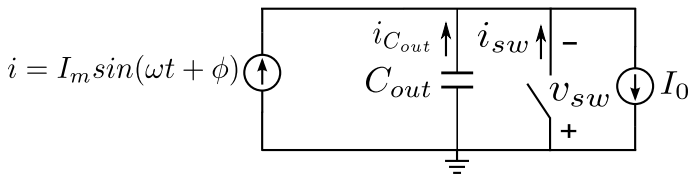


Figure 3.4: Simplified model of a Class-E rectifier.

The rectifier is driven by an ideal sinusoidal current source

$$i = I_m \sin(\omega t + \phi) \tag{3.4}$$

where I_m and ϕ are the amplitude and initial phase of i respectively. When the switch is off during the interval $0 \leq \omega t \leq 2\pi(1\text{-}D)$, where D is the duty cycle of the switch, the current through the output capacitance can be expressed as

$$i_{C_{out}} = I_0 - i = I_0 - I_m \sin(\omega t + \phi) \tag{3.5}$$

applying $i_{C_{out}}(0) = 0$,

$$I_0 = I_m \sin(\phi) \tag{3.6}$$

substituting into equation 3.5,

$$i_{C_{out}} = I_0 \left[1 - \frac{\sin(\omega t + \phi)}{\sin(\phi)}\right] \tag{3.7}$$

using I_0=V_0/R_{dc} the voltage across the switch and C_{out} can be obtained as

$$v_{sw} = \frac{1}{\omega C_{out}} \int_0^{\omega t} i_{C_{out}} d(\omega t) = \frac{V_0}{\omega C_{out} R_{dc}} \left[\omega t + \frac{\cos(\omega t + \phi) - \cos(\phi)}{\sin(\phi)}\right] \tag{3.8}$$

The relationship between the duty cycle D and the initial phase of the input current i can be obtained by applying the boundary condition $v_{sw}(2\pi(1 - D)) = 0$ into equation 3.8.

$$\tan(\phi) = \frac{1 - \cos(2\pi D)}{2\pi(1 - D) + \sin(2\pi D)} \tag{3.9}$$

For a duty cycle $D = 0.5$, $\tan(\phi)$= $2/\pi$, and ϕ=32.48°. The output voltage V_0 can be related to the average voltage across the switch as

$$\begin{aligned} V_{sw} = -V_0 &= \frac{1}{2\pi} \int_0^{2\pi(1-D)} v_{sw} d(\omega t) \\ &= \frac{V_0}{2\pi\omega C_{out} R_{dc}} \left[\frac{2\pi^2(1 - D)^2 - 1 + \cos(2\pi D) - 2\pi(1 - D) + \sin(2\pi D)}{\tan(\phi)}\right] \end{aligned} \tag{3.10}$$

by using equation 3.9 and simplifying the expression, the following relationship between D and $\omega C_{out} R_{dc}$ is found

$$\omega C_{out} R_{dc} = \frac{1}{2\pi}\left[1 - \cos(2\pi D) - 2\pi^2(1-D)^2 + \frac{(2\pi(1-D) + \sin(2\pi D))^2}{1 - \cos(2\pi D)}\right] \tag{3.11}$$

Fig. 3.5 shows the rectifier circuit when the switch is ON or conducting during the interval $2\pi(1\text{-}D) < \omega t < 2\pi$. During this interval, the switch shorts the capacitor C_{out} and no current flows through the capacitor.

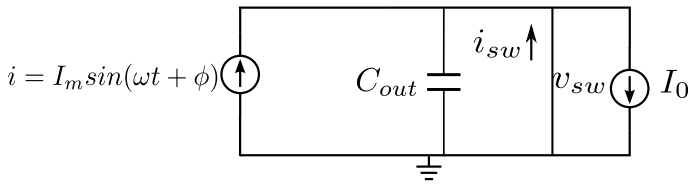


Figure 3.5: Simplified model of a Class-E rectifier when the switch is closed.

The current through the switch can be expressed as

$$i_{sw} = I_0 - I_m \sin(\omega t + \phi) = I_0\left[1 - \frac{\sin(\omega t + \phi)}{\sin(\phi)}\right] \tag{3.12}$$

Because the input current i is assumed sinusoidal, the input impedance of the rectifier at the fundamental can be estimated from the input voltage at the fundamental frequency. The input voltage of the rectifier v_{rec}=-v_{sw} and can be expanded into the Fourier series such that the sinusoidal components represents the voltage across the input impedance of the rectifier at the fundamental frequency. The fundamental component of the input voltage of the rectifier can be expressed as

$$v_1 = v_{R1} + v_{X1} = V_{R1} \sin(\omega t + \phi) - V_{X1} \cos(\omega t + \phi) \tag{3.13}$$

where V_{R1} and V_{X1} are the amplitudes of v_{R1} and v_{X1}. The negative sign in equation 3.13 assumes a capacitive reactance. Using equation 3.8.

$$\begin{aligned} V_{R1} &= \frac{1}{\pi}\int_0^{\pi} v_{sw} \sin(\omega t + \phi) d(\omega t) \\ &= \frac{V_0}{2\pi\omega C_{out} R_{dc}}\left[\frac{1}{2}\cos(\phi)\sin(4\pi D) + \sin(\phi)\left(1 - \cos(2\pi D + \frac{1}{2}\sin^2(2\pi D))\right)\right. \\ &\left. + 2\pi(1-D)\cos(2\pi D - \phi) + \frac{\cos(\phi)(1 - \cos(2\pi D) + \frac{1}{2}\sin^2 2\pi D)}{\tan\phi}\right] \end{aligned} \tag{3.14}$$

which for $D = 0.5$, simplifies to

$$V_{R1} = \frac{4}{\sqrt{\pi^2 + 4}} V_0 = 1.074 V_0 \tag{3.15}$$

The real part of the input impedance of the rectifier at the fundamental is then

$$R_i = \frac{V_{R1}}{I_m} = 2\sin^2(\phi) R_{dc} \tag{3.16}$$

which can be normalized to the reactance of the output capacitance of the switch as it is normally shown for the class-E PA by substituting equation 3.16 into equation 3.11

$$\begin{aligned} \omega C_{out} R_i &= \omega R_{dc} C_{out} \frac{R_i}{R_{dc}} \\ &= \frac{\sin^2(\phi)}{\pi} \left[1 - \cos(2\pi D) - 2\pi^2 (1 - D)^2 + \frac{(2\pi(1 - D) + \sin(2\pi D))^2}{1 - \cos(2\pi D)} \right] \end{aligned} \tag{3.17}$$

which for $D = 0.5$ it simplifies to

$$R_i = \frac{8}{\pi(\pi^2 + 4)} = \frac{0.1836}{\omega C_{out}} \tag{3.18}$$

Following a similar procedure, the voltage across the imaginary part of the input impedance of the rectifier can be expressed as

$$\begin{aligned} V_{X1} &= -\frac{1}{\pi} \int_0^{2\pi} v_{sw} \cos(\omega t + \phi) d(\omega t) \\ &= \frac{V_0}{\pi \omega C_{out} R_{dc}} \left[\frac{\cos(\phi)[\pi(1 - D) + \sin(2\pi D) - \frac{1}{4}\sin(4\pi D)]}{\tan(\phi)} \right. \\ &\left. + \sin(\phi) \left[\pi(1 - D) + \frac{1}{4}\sin(4\pi D) + \sin(2\pi D) \right] - \cos(\phi)\sin^2(2\pi D) + 2\pi(1 - D)\sin(2\pi D - \phi) \right] \end{aligned} \tag{3.19}$$

The input reactance of the rectifier at the fundamental frequency is then

$$X_i = \frac{V_{X1}}{I_m} = \frac{\pi(1-D) + \sin(2\pi D) - \frac{1}{4}\sin(4\pi D)\cos(2\phi) - \frac{1}{2}\sin(2\phi)\sin^2(2\pi D) - 2\pi(1-D)\sin(\phi)\sin(2\pi D - \phi)}{\pi\omega C_{out}} \tag{3.20}$$

For a duty cycle $D = 0.5$, the reactance simplifies to

$$X_i = \frac{.2116}{\omega C_{out}} \tag{3.21}$$

The normalized input impedance of the class-E rectifier with a duty cycle $D = 0.5$ from equations 3.21 and 3.18 is the complex conjugate of the impedance the class-E PA requires for optimum operation from equations 3.1 and 3.2. Evaluating equation 3.16 at $D = 0.5$ and $\phi = 32.48°$, the input impedance of the rectifier as a function of dc load is obtained

$$R_{ac} = 0.1836\pi R_{dc} \tag{3.22}$$

which is a dual of equation 3.3 during optimum operation. The voltage and current time domain waveforms across the switch for the class-E PA and class-E rectifier are shown in Fig. 3.6.

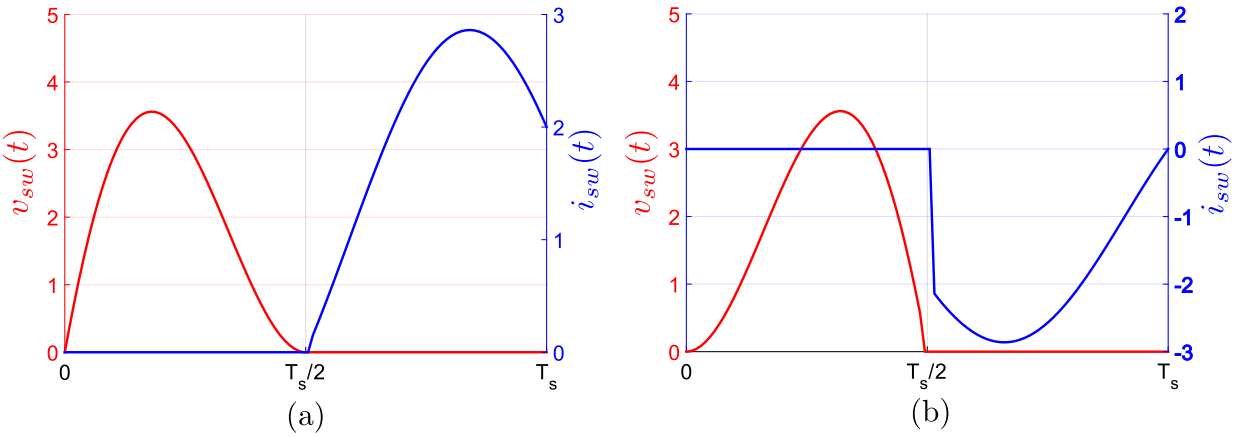


Figure 3.6: Voltage and current time-domain waveforms across the switching element of a class-E PA (a) and a class-E rectifier. The waveforms are normalized to the dc voltage and current of the supply or load. The waveforms are time-reversal dual of each other.

The waveforms are time-reversal dual of each other and follow the relationship shown in table 3.1. Hence, the class-E rectifier is the time-reversed dual of the class-E PA. Furthermore, the class-E rectifier presents the impedance R_{ac} necessary for optimum operation of the PA as shown in Fig. 3.7. This convenient realization makes it possible to simply cascade a class-E PA and a class-E rectifier to form a class-E^2 dc-dc converter as shown in Fig. 3.8.

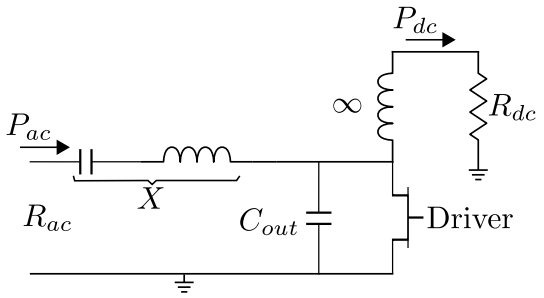


Figure 3.7: Schematic of ideal Class-E rectifier.

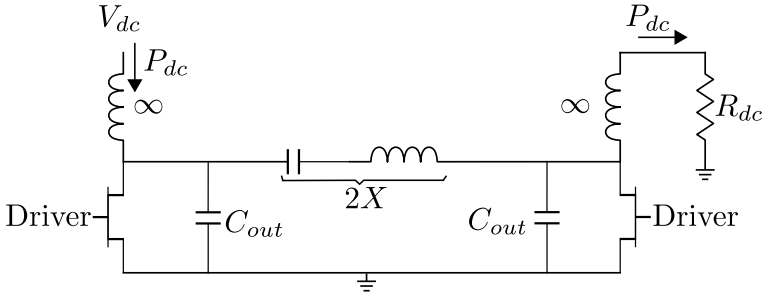


Figure 3.8: Schematic of a class-E^2 dc-dc converter composed of a class-E PA and its time-reversal dual class-E rectifier.

Not only does the rectifier supply the equivalent real load R_{ac} for the PA to operate under optimum condition but the two reactances X from eq.3.2 needed for class-E operation can be added into a single reactance $2X$ as shown in Fig. 3.8. In this particular case, the dc-dc converter operates under optimum performance with the same input and output voltage and when the rectifier appears as a purely resistive load to the PA, which only happens when the dc load is equal to equation 3.3. When the dc load R_{dc} is less than equation 3.3, the impedance presented by the rectifier is inductive and the PA can still operate under soft-switching. However, when R_{dc} is more than equation 3.3, the impedance presented by the rectifier is capacitive and the PA stops operating under soft-switching.

3.3 Non-linear simulations of microwave power amplifiers, microwave rectifiers and their duality

Having introduced the concept of time-reversal duality in the last section, we next turn our attention to the application of the concept to microwave PAs, microwave rectifiers, and ultimately to microwave dc-dc converters.

In the design of high-efficiency RF PAs, the typical design methodology is to present the appropriate output impedances at the fundamental and harmonic frequencies, so as to shape the current and voltage waveforms across the current source of the device to minimize the power dissipation $v(t) \times i(t)$. In the past few years, PAs implemented in GaN technology have demonstrated power added efficiencies (PAEs) above 80 % using a single transistor. In this section, a high-efficiency PA is designed using standard design procedures [22]. After the PA is characterized, the exact same design is then simulated and characterized as a RF rectifier to illustrate the duality between both.

All the simulations are performed with the 8×75 μm GaN HEMT model described in [4, 5]. This nonlinear model includes: nonlinear capacitances C_{gs}, C_{gd}, and C_{ds}, gate-source and gate-drain diodes, as well as breakdown and trapping effects. In addition, the HEMT model accurately reproduces the nonlinear transistor behavior not only for positive but also for negative values of the drain voltage which is necessary for the proper simulation of the HEMT operating as a rectifier. The I-V curves of the HEMT model are shown in Fig. 3.9.

3.3.1 Simulation of the power amplifier

First, a semi-ideal class-F PA is simulated. The PA is considered semi-ideal because both input and output matching networks as well as both bias-T are lossless and ideal, however, the transistor is not ideal. The input and output matching networks are implemented using an impedance tuner as shown in Fig. 3.10. The tuner at the output matching network terminates the first 5 harmonics according to class-F amplifier theory [28]. The impedance at the fundamental frequency is optimized through load-pull simulations for maximum efficiency.

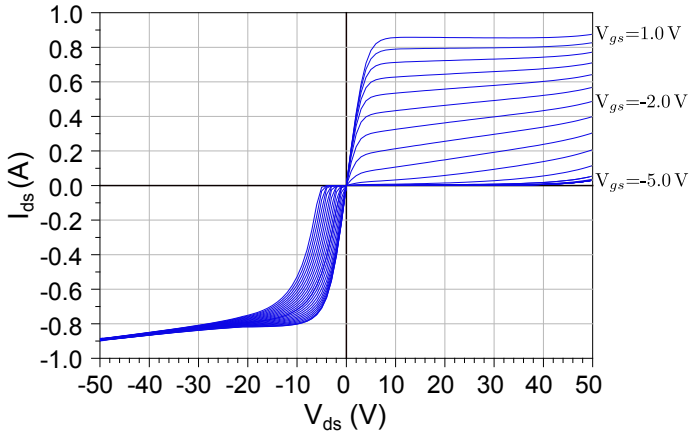


Figure 3.9: I-V curves of the 8 x 75 μm GaN HEMT model used in all the non-linear simulations.

For the amplifier mode of operation, when an input RF signal is injected into the gate terminal, the efficiency considered is the drain efficiency, or DC-to-RF conversion efficiency:

$$\eta_D = \frac{P_{out,RF}}{P_{DC}}. \tag{3.23}$$

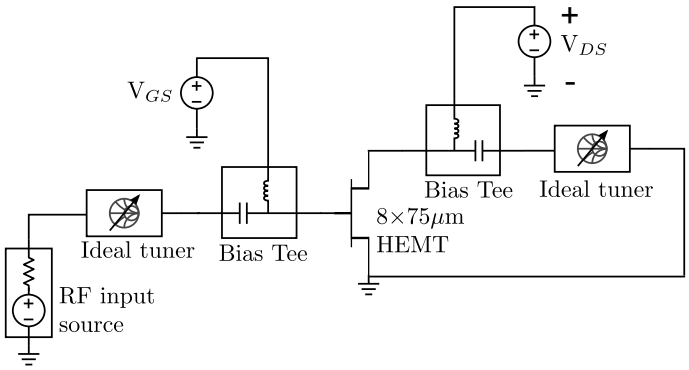


Figure 3.10: Schematic of the semi-ideal power amplifier simulation. The input and output matching networks are implemented using ideal impedance tuners. The impedance of the fundamental frequency as well as the first 5 harmonics are terminated by the tuner.

A maximum efficiency of η_{PA}= 72 % is obtained for a drain voltage V_{ds}= 28 V and with the transistor biased close to pinch-off at V_{gs}=-4.9 V. The same class-F PA circuit is then simulated in rectifier mode. In rectifier mode, the drain DC power supply is replaced by a DC load resistance R_{DC} and the input to the circuit is now RF power $P_{in,RF}$ injected into the drain port of the circuit as illustrated in Fig. 3.11. Assuming the DC gate current is negligible, the rectifier RF-to-DC conversion efficiency is defined as

$$\eta_R = \frac{P_{DC}}{P_{in,RF}} = \frac{2|V_{DC}|^2}{R_{DC}\,\mathrm{Re}\left\{V_{drain}(f_0)I^*_{drain}(f_0)\right\}} \tag{3.24}$$

An impedance tuner connected at the gate input of the rectifier allows load-pull at the gate resulting in η_R=80 % with R_{DC} = 120 Ω (f_{RF} = 2.14 GHz). The input power injected into the drain is approximately equal to the output power of the $P_{out,RF}$ of the amplifier.

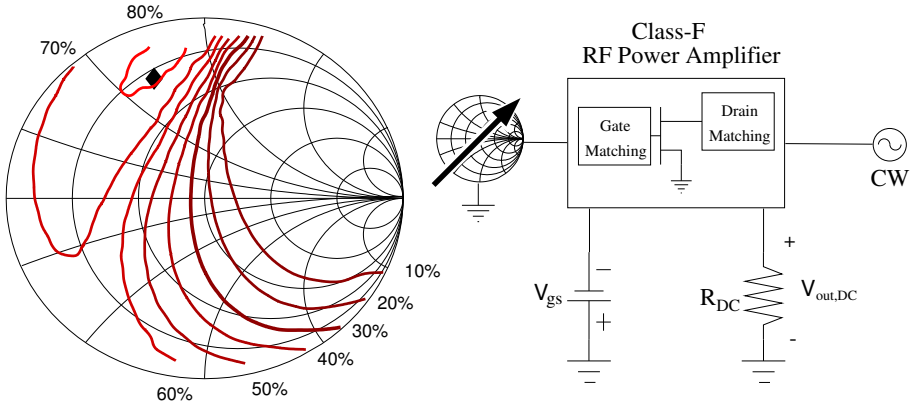


Figure 3.11: Load-pull simulations for rectifier efficiency obtained at transistor terminals. Frequency is 2.14 GHz and RF drain input power is 40 dBm. Marker shows impedance for maximum efficiency.

The dynamic load lines of the PA (a) and the rectifier (b) are presented in Fig. 3.12 for different RF input power for comparison. RF power is swept from 0 to 40 dBm. The class-F PA operates in the first quadrant of the I-V curves and the dynamic load lines approximate the operation of a switch as is expected for class-F power amplifiers. On the other hand, when the circuit is simulated as a rectifier, the transistor operates in the third quadrant or in the negative I_{ds} region. The dynamic load lines of the transistor also approximate the behavior of a switch, except with the current flowing in the opposite direction. A better understanding of the time-reversal duality between a microwave power amplifier and a microwave rectifier can be realized by looking at the simulated time domain waveforms at the intrinsic drain.

The time-domain waveforms at the intrinsic drain of the PA (a) and the rectifier (b) are shown in Fig. 3.13. The voltage waveform of the amplifier approximates a square wave with a DC offset equal to the drain voltage while the current waveform approximates a half sine wave, as it's expected for a class-F PA with 5 harmonics [61]. The voltage waveform of the rectifier also approximates a square wave, the only difference is that the square wave for the rectifier contains a DC component. The current waveform

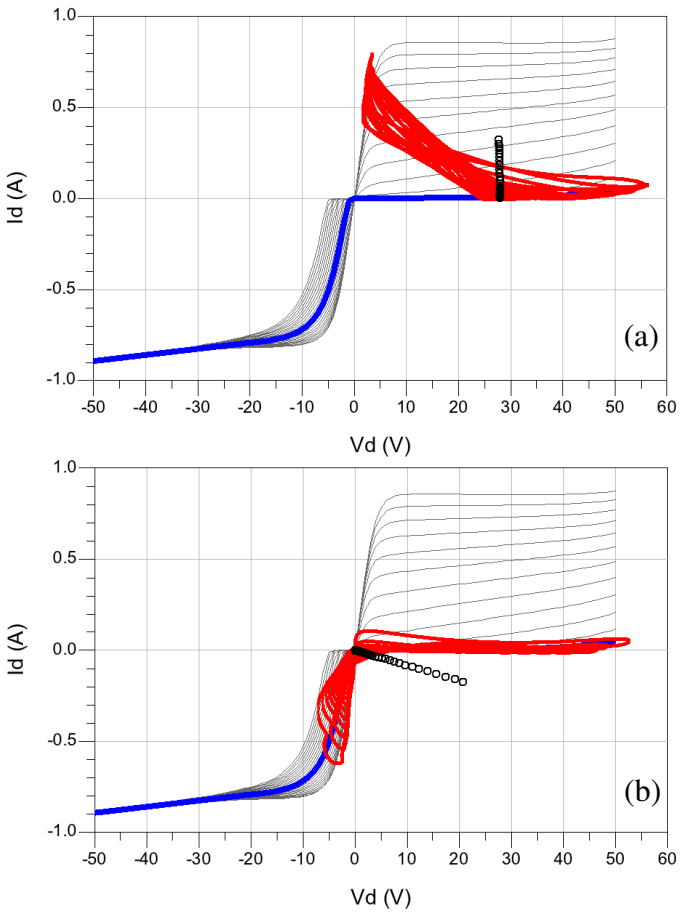


Figure 3.12: Simulated GaN transistor I-V curves (grey), dynamic load lines (red) and drain DC voltage and current (black) for PA (a) and rectifier (b). Blue line corresponds to the I-V curves of $V_{gs} = -4.9$ V, the quiescent bias voltage of the rectifier. Time-reversal duality is seen as RF power at drain is swept from 0 to 40 dBm at 2.14 GHz.

of the rectifier retains the form of a half sine wave, however, because the transistor is supplying power to the DC load instead of drawing power from the DC power supply the direction the current is flowing is reversed. Although not immediately obvious due to the current and voltage waveforms being symmetric, the time-domain waveforms of the rectifier correspond to the time-reversed class-F waveforms of the power amplifier and are related by the relation outlined in Table 3.1 i.e.

$$v_{PA}(t) = v_{REC}(-t)$$

$$i_{PA}(t) = -i_{REC}(-t)$$

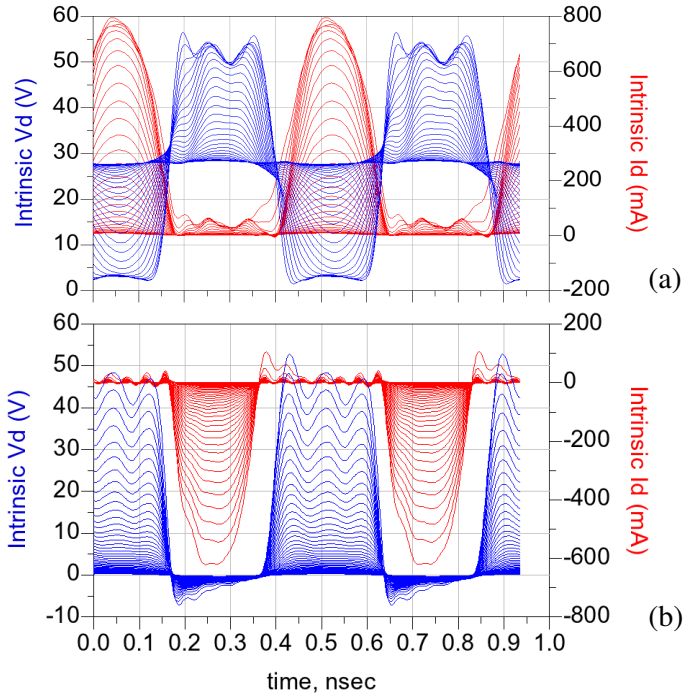


Figure 3.13: Simulated time-domain intrinsic drain voltage (blue) and current (red) waveforms for RF input power ranging from 0 to 40 dBm at intrinsic drain of power amplifier (a) and rectifier (b).

3.4 Experimental validation of PA-rectifier duality with a class-F^{-1} power amplifier

3.4.1 Circuit design

Having shown the duality of harmonically terminated PAs and rectifiers through simulations, the next natural step is to prove said duality experimentally. In order to achieve such a goal, a high-efficiency class-F^{-1} PA was designed, fabricated, and measured. The PA used for all the measurements is described in [2] and pictured in Fig. 3.14. The PA is designed using the Triquint TGF2023-02 GaN HEMT and it operates at 2.14 GHz. Class F^{-1} harmonic terminations are implemented at the second and third harmonic using quarter-wavelength open circuit shunt stubs as harmonic traps. An additional stub is used to match 50 Ω to 164.5-j4.5 Ω at the fundamental frequency. 164.5-j4.5 Ω is the impedance resulting in maximum PAE with at least 5 W of output power and it was obtained through a large signal load pull and the method outlined in [62].

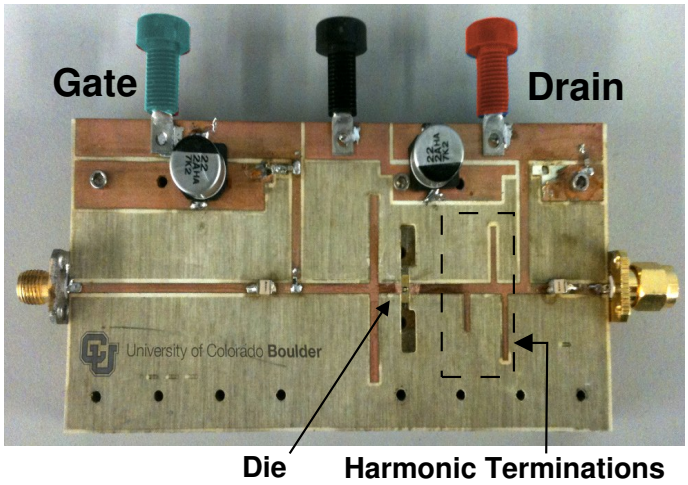


Figure 3.14: Photograph of the class-F^{-1} power amplifier, working at 2.14 GHz and presented in [2].

3.4.2 Measurement setup

The performance of the PA, illustrated in Fig. 3.15, was characterized at 2.14 GHz with a drain voltage bias of 28 V and a bias current of 160 mA. The PA exhibits a PAE of 84% with an output power of 37.6 dBm and a gain of 15.7 dB under 3 dB compression.

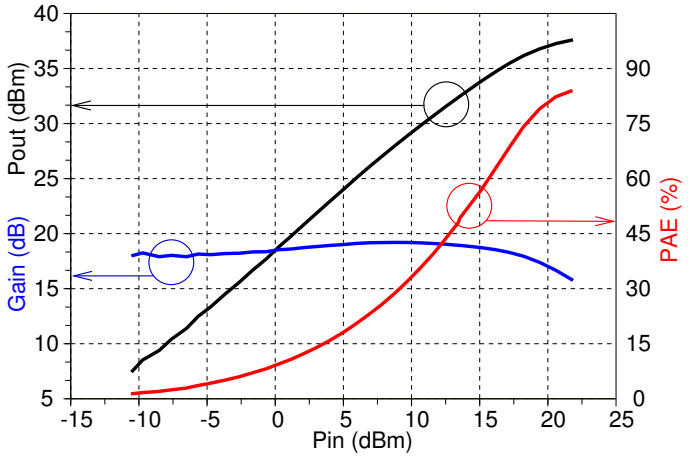


Figure 3.15: Large-signal measurements performed on the class-F^{-1} power amplifier at $f_0 = 2.14$ GHz, $V_{GS} = -3.8$ V and $V_{DS} = 28$ V

The class-F^{-1} power amplifier described above is fully characterized in large signal in a rectifier configuration with the setup shown in Fig. 3.16. The gate terminal is biased, and connected to an impedance tuner, converting the two-port transistor PA to a one-port rectifier. In the rectifier measurements, RF power

is input into the drain which is unbiased. The gate is terminated in a variable impedance and biased close to pinch-off. Measurements of efficiency and DC voltage are performed in time domain as a function of input RF power, gate RF load, gate bias and drain DC load. The commercial time-domain large signal measurement instrument used is a VTD SWAP four-channel receiver [3]. In order to acquire time domain waveforms at the reference plane, an 8 error term model calibration similar to the one performed for LSNA (Large Signal Network Analyzer) measurements is applied. After an absolute VNA-like calibration [63], the RF voltage and current waveforms at the input (V1 and I1) and at the output (V2 and I2) of the DUT are measured at the coaxial reference plane. In this case, the RF input is the drain port of the PA, while the RF output is connected to the gate port. Thus, performing a load pull on this device consists of varying the load at the fundamental frequency f_0 at the RF gate port of the PA with a passive tuner. This kind of measurement is similar to large signal characterization of switch devices recently reported in [64, 65]. The gate DC path is connected to a power supply so the gate bias can be varied. The drain DC bias is the output of the rectifier and is connected to a variable resistance R_{DC}, and the DC voltage across it is measured with a voltmeter. The DC current is then found from the value of R_{DC} as $I_{DC} = V_{DC}/R_{DC}$. During the measurement, several parameters are varied systematically: the RF load impedance applied at the PA gate port $Z_g(f_0) = V_g(f_0)/I_g(f_0)$; the resistor in the DC drain output R_{DC}; and the gate bias voltage V_{GS}. The conversion efficiency of the rectifier and the DC power delivered at the drain output of the rectifier $P_{DC} = V_{DC} \cdot I_{DC}$ are measured as these parameters are varied, and as a function of input power at the drain port $P_{in}(f_0)$.

3.4.3 Self-synchronous transistor rectifier results

The measurements of the rectifier are performed in self-synchronous mode, i.e. there is no input RF power incident externally into the gate port of the PA, unlike in previous transistor rectifier work [66, 67]. The following parameters are varied in order, while keeping the other parameters constant and sweeping the input RF power at the drain port, and the results are described in the same order:

(1) RF impedance at the gate, Z_g;

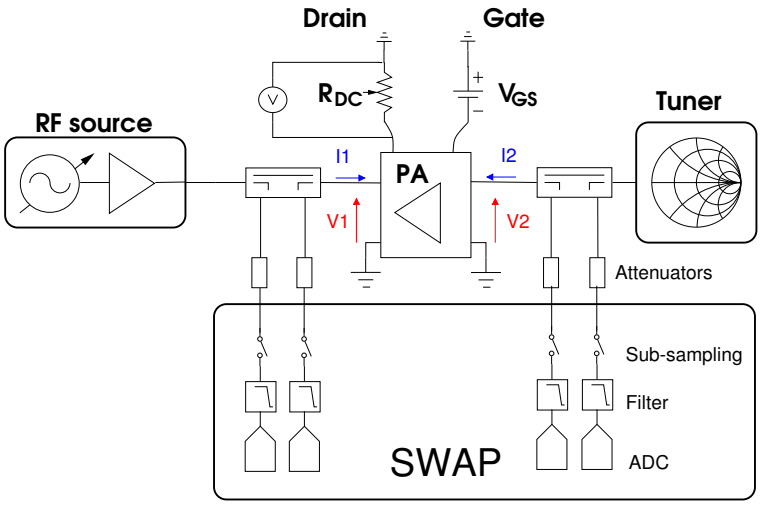


Figure 3.16: Time-domain non-linear rectifier measurement block diagram. The SWAP [3] performs sampling of current and voltage and the calibration refers the sampled quantities to the reference planes at the DUT. The drain output DC resistance R_{DC} , the gate bias V_{GS} and the gate RF impedance Z_g are varied as the input power at the drain is swept from 10 to 42 dBm.

(2) load resistance at drain bias output, R_{DC};

(3) gate DC bias, V_{GS}.

The gate load-pull was performed to determine the optimum impedance for maximum efficiency with a constant resistive DC load of 98.5 Ω (nominally 100 Ω) and a constant transistor gate bias in pinch-off of -4.4 V. The RF signal is coupled from the drain to the gate matching network through the intrinsic feedback capacitances C_{gd}, and C_{gs} and thus the precise impedance presented at the gate of the transistor is imperative to achieving high efficiency. Fig. 3.17 shows the time-domain voltage and current waveforms measured at the drain and gate RF port of the amplifier when the RF input power at the drain port is swept from 11 dBm to 42 dBm. These values are chosen because the rectifier in PA operation gives up to 42 dBm output power. Fig. 3.17 (b) clearly shows a voltage waveform with an amplitude of approximately 5 V is present at the gate port of the rectifier. It's important to point out that the time-domain waveforms shown here are referenced at the reference plane of the connector and not at the drain and gate of the transistor. The feedback signal present at the gate allows for the rectifier to operate in self-synchronous mode without any additional control signal. Unlike in the synchronously driven case where an external generator is connected to the gate, here the impedance presented at the gate is always passive (inside the Smith chart).

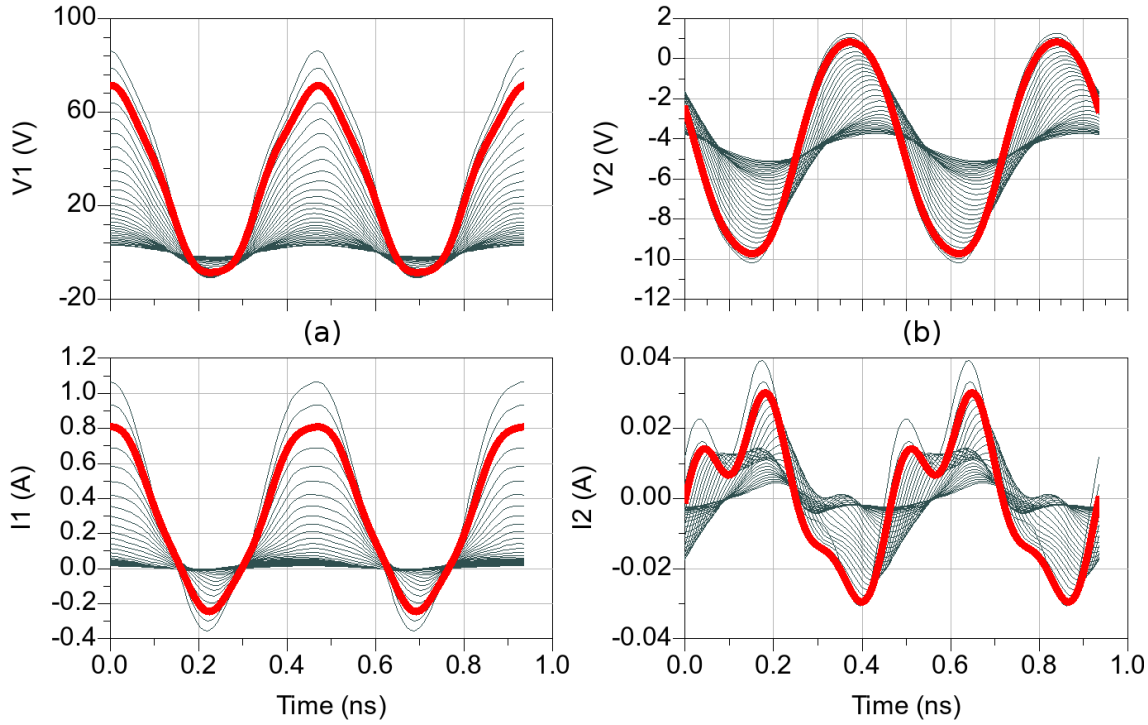


Figure 3.17: Time-domain waveforms measured at drain (a) and gate (b) of the rectifier with $V_{GS} = -4.4\,\text{V}$, $R_{DC} = 98.5\,\Omega$ and $Z_g(f_0) = (230 + j10)\,\Omega$. The RF input power at the drain is swept from 10 to 42 dBm, corresponding to the range of output power of the class-F^{-1} PA.

Measured RF-DC conversion efficiency is shown in Fig. 3.18 for four different RF gate impedances. A maximal conversion efficiency of 85% is achieved with a DC output voltage of 36 V and an input power at the drain of 42 dBm with $R_{DC} = 98.5\,\Omega$. This peak efficiency is for a RF gate load of around $230\,\Omega$ (green hexagon in the Smith chart in Fig. 3.18), which is the highest impedance that was achievable with the tuner used in the measurement setup. For the low gate impedance (red triangle in the Smith chart), the efficiency is significantly lower. By observing the gate current (Fig. 3.18 (d), it can be seen that for a low RF gate impedance, the gate diode turns on at around $P_{in} = 25\,\text{dBm}$. Since the input power cannot be increased much beyond this point to avoid breakdown, this limits the DC voltage at the output to around 4 V. For the gate impedance with highest efficiency (green line with hexagon symbol), the gate diode is off for input drain powers below 41 dBm, allowing for high DC voltage output.

After the optimal gate impedance for highest efficiency was obtained, a power sweep for three different R_{DC} values in the drain output was obtained. From Fig. 3.19, a maximal efficiency of 85% was measured for a DC resistive load of $98\,\Omega$ while an efficiency drop of 13% was observed for a DC load of $21\,\Omega$ with

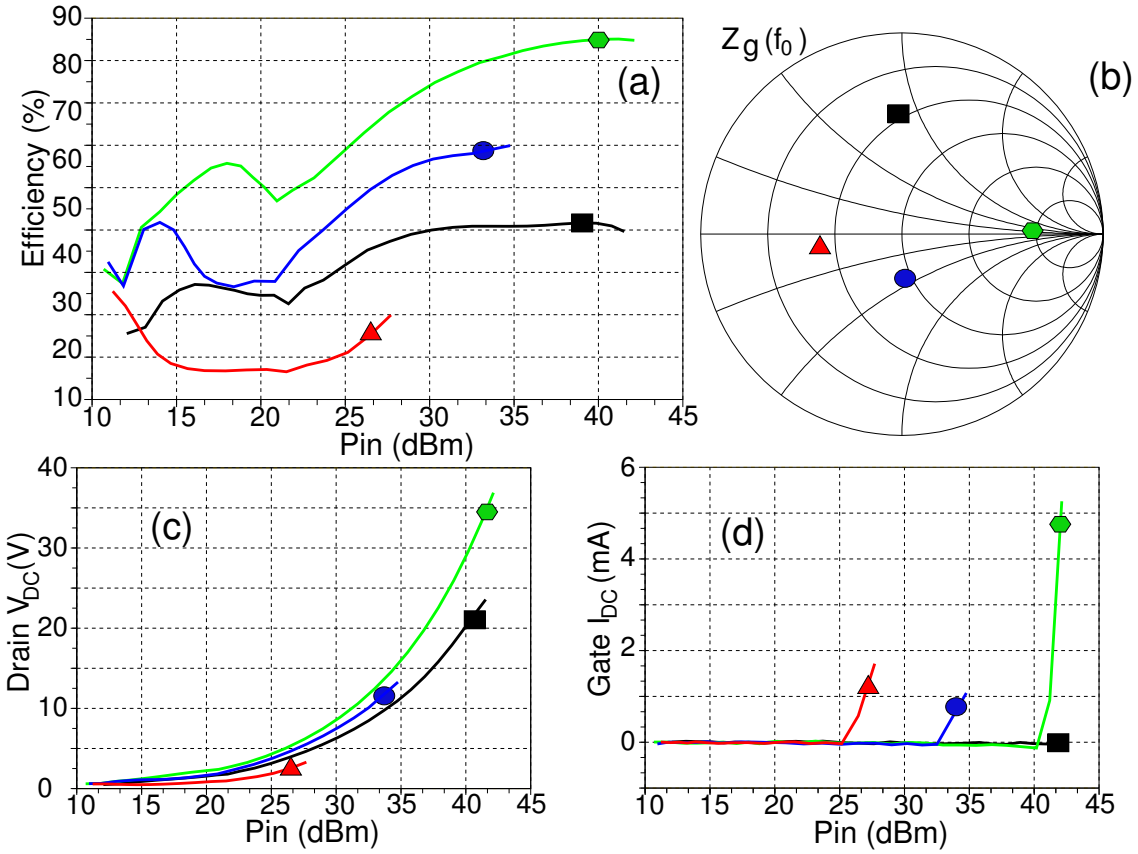


Figure 3.18: Conversion efficiency, gate DC current and drain DC voltage versus input power for several RF load impedance values presented at the gate. $V_{GS} = -4.4\,\text{V}$ and $R_{DC} = 98.5\,\Omega$. The green point on the Smith chart corresponds to the highest efficiency point at $Z_g(f_0) = (230 + j10)\,\Omega$.

40 dBm input power. As expected, the DC output voltage decreases from a maximum 30 V for $R_{DC} = 98\,\Omega$ at 40 dBm input power, to a maximum of 13.4 V for $R_{DC} = 21\,\Omega$ with the same input power. It is interesting to see how the input impedance of the rectifier at the RF drain port approaches $50\,\Omega$ as the input power increases, Fig. 3.20. This is expected, since the PA was designed for maximal saturated power delivered into a $50\,\Omega$ load. This again points to the similarities between the same circuit operated as a power rectifier and a power amplifier.

Finally, the effect of the gate bias V_{GS} on the rectifier efficiency, output voltage and input impedance was investigated. The gate impedance in this case was set for highest efficiency ($230\,\Omega$), and a DC load of $58\,\Omega$ was selected in order to protect the transistor from high drain voltages that occur for the $98\,\Omega$ load that corresponds to the highest efficiency. The measurements were performed for six different values of gate bias

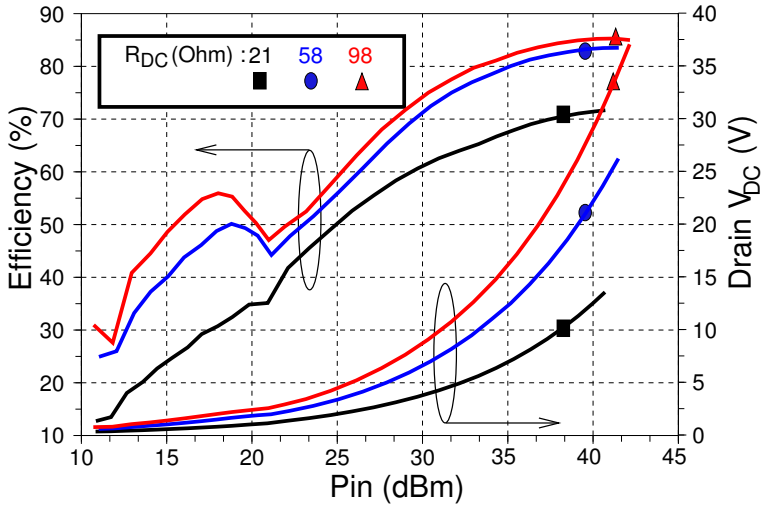


Figure 3.19: Conversion efficiency and drain DC output voltage versus input power for several DC drain resistor values. $V_{GS} = -4.4V$ and $Z_g(f_0) = (230 + j.10)\,\Omega$. The highest efficiency of 85% is obtained at P_{in}=40 dBm with a V_{DC}=30 V.

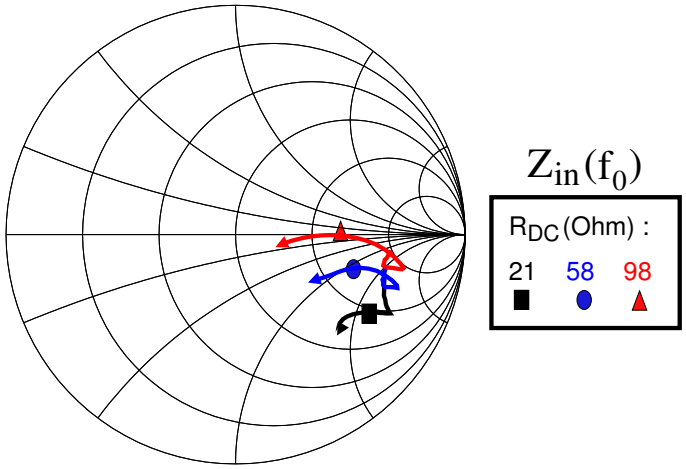


Figure 3.20: RF impedance at f_0 measured at the input (drain port) versus input power for several DC drain resistor values. $V_{GS} = -4.4V$ and $Z_g(f_0) = (230 + j10)\,\Omega$.

V_{GS} as shown in Fig. 3.21.

With $R_{DC} = 58\Omega$, a maximum efficiency of 83% was obtained with the transistor biased deeply into the pinch-off region with $V_{GS} = -4.4$ V, and a drop of only 3% was measured for $V_{GS} = -3.5$ V. The gate bias has a minimal impact on the output DC voltage or on the drain impedance, this is rather disappointing since the gate bias of the rectifier cannot be used as a way to control and regulate the output voltage of the rectifier.

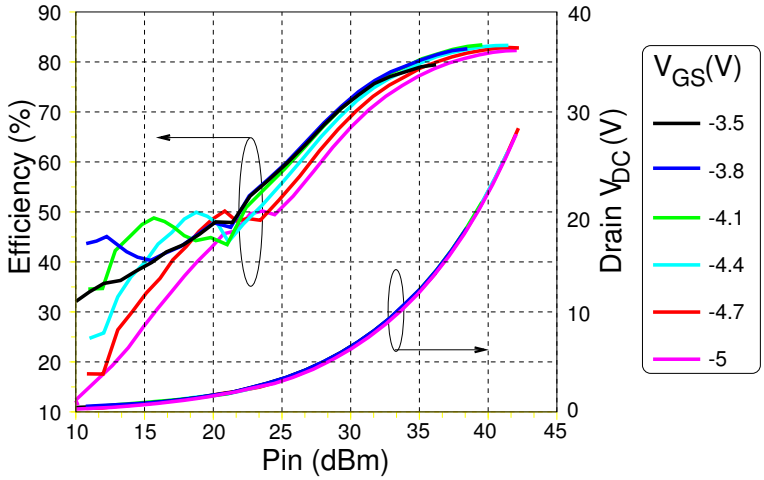


Figure 3.21: Measured conversion efficiency and drain DC voltage versus input power for several DC gate voltage biases. For this data, $R_{DC} = 58\Omega$ and $Z_g(f_0) = (230 + j10)\,\Omega$.

3.5 Self-synchronous rectifier

As shown in Chapter 3 a GaN HEMT transistor rectifier can be operated without the need of an RF input, or operated in self-synchronous operation. This type of operation is demonstrated in a number of recent publications related to this thesis [21, 22, 68, 69]. This is mainly enabled by the drain-to-gate feedback capacitance and through the presence of an unknown impedance at the gate-port of the rectifier. This unknown impedance is usually found through experimental measurements or a load-pull measurement at the gate port of the rectifier. In this section, an analysis of self-synchronous rectifiers is presented to give designers a better understanding of the operation of the rectifier as well as a more methodical method to find the impedance necessary to operate in self-synchronous mode.

3.5.1 Theoretical analysis of self-synchronous rectifier

The goal of this analysis is to determine the theoretical value of the gate impedance Z_g that satisfies self-synchronous class-E rectification. Fig. 3.22 shows a simplified intrinsic model for a HEMT transistor [70]. When the transistor is pinched off, the two diodes can be approximated as open circuits. This is true when the dynamic load line keeps v_{gs} and v_{gd} below the forward-bias knee value. To investigate a class-E self-synchronous rectifier, the idealized circuit shown in Fig. 3.23 is developed from the model shown in

Fig. 3.22. It assumes a sinusoidal input current source driving an ideal switch. The input current includes a negative DC term representing the rectified DC output current.

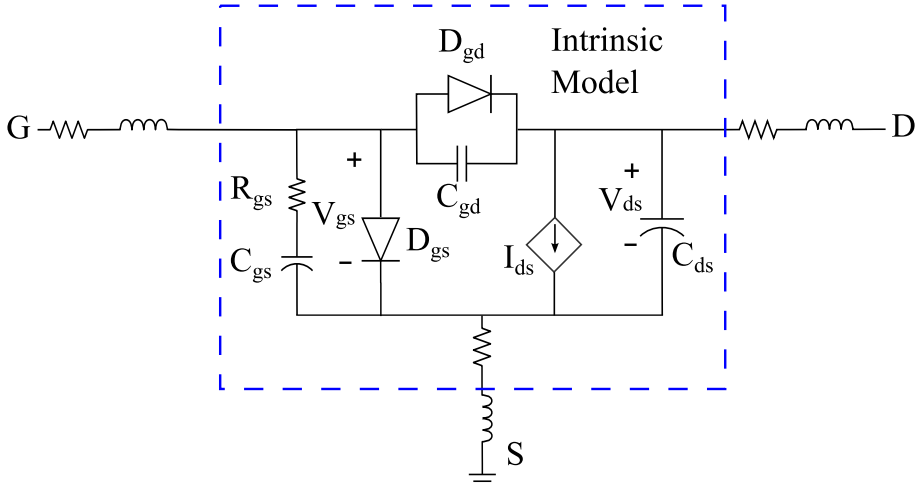


Figure 3.22: Simplified intrinsic model of a GaN HEMT. Diodes D_{gd} and D_{gs} are modeled as open circuits for self-synchronous analysis.

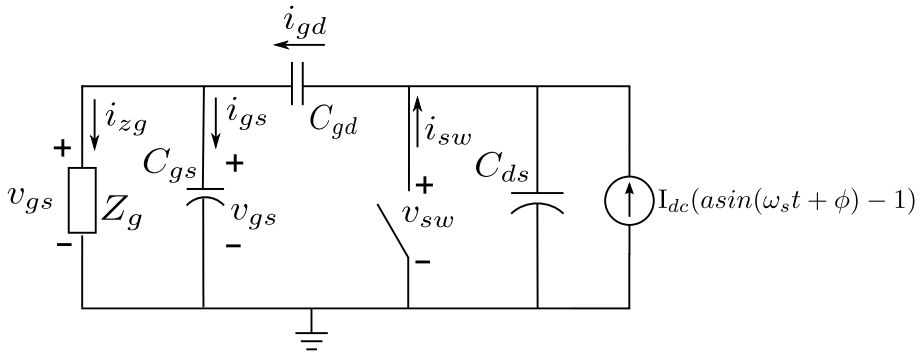


Figure 3.23: Idealized switch model for class-E self-synchronous conditions. The switch is assumed ideal, with R_{on}=0 and R_{off}=∞. v_{sw} is assumed to be an ideal class-E waveform, and v_{gs} is approximated as a sinusoid. Unknown impedance Z_g is found under these conditions.

The conditions for soft-switching class-E rectifier operation are

$$v_{sw}(0) = 0 \tag{3.25}$$

$$\frac{dv_{sw}}{dt}(0) = 0 \tag{3.26}$$

$$v_{sw}\left(\frac{T_s}{2}\right) = 0 \tag{3.27}$$

For simplicity, the voltage class-E time-reversed waveform from [32, 54] is assumed across the switch, which can be expressed using the formulation in [71] as

$$v_{sw}(t) = \begin{cases} -\frac{I_{dc}}{C_{out}\omega_s}[a\cos(\omega_s t + \phi) + \omega_s t - a\cos(\phi)], & 0 \le t \le \frac{T_s}{2} \\ 0, & \frac{T_s}{2} \le t \le Ts \end{cases} \tag{3.28}$$

where C_{out} represents the equivalent output capacitance when the switch is off. The constants a and ϕ are found as in [71] to be 1.862 and 32.48^o respectively. The normalized waveforms are shown in Fig. 3.24.

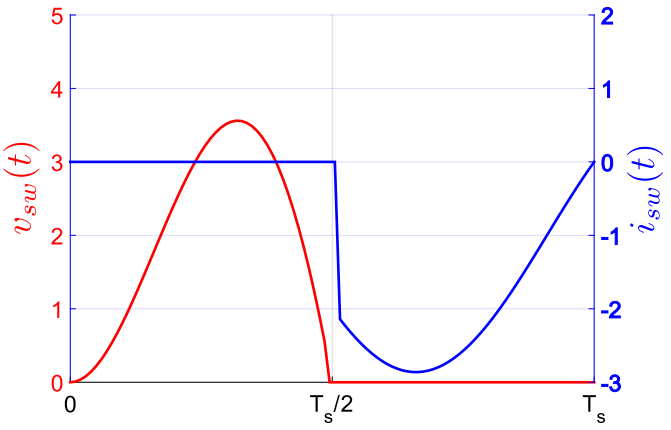


Figure 3.24: Time domain waveforms of an ideal class-E rectifier. The waveforms are normalized. v_{sw} is assumed across the switch in Fig. 3.23.

In addition to the classic class-E boundary conditions, for the rectifier to operate self-synchronously, the voltage across C_{gs} should be less than the turn-off voltage of the transistor during the interval $0 \le t \le \frac{T_s}{2}$ and greater than the turn-on voltage of the transistor during the interval $\frac{T_s}{2} \le t \le T_s$. A simple approximation

for v_{gs} is the following

$$v_{gs}(t) = -V_0 \sin(\omega_s t) \tag{3.29}$$

where the switch is off for $v_{gs} \leq 0$, and on for $v_{gs} > 0$. Fig. 3.25 illustrates the operation of the switch.

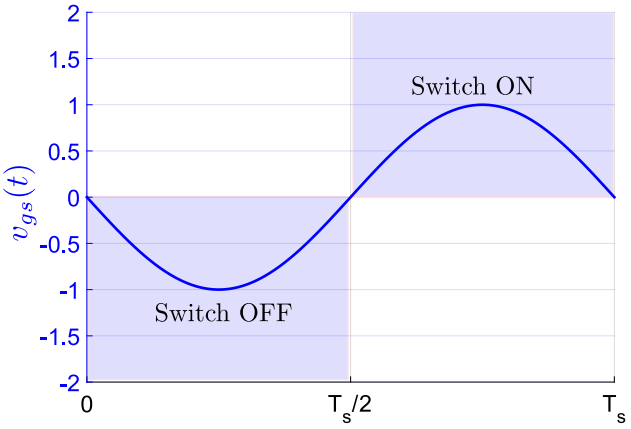


Figure 3.25: Operation of the switch as a function of assumed v_{gs}. The switch is off for $v_{gs} \leq 0$, and on for $v_{gs} > 0$.

From Fig. 3.23, the current i_{gd} through capacitor C_{gd} can be written as

$$i_{gd}(t) = C_{gd} d\frac{(v_{sw} - v_{gs})}{dt} = C_{gd}\left(\frac{dv_{sw}}{dt} - \frac{dv_{gs}}{dt}\right) \tag{3.30}$$

Kirchoff's current law results in

$$i_{gs} + i_{zg} = i_{gd} \tag{3.31}$$

When the switch is off, following (3.28)-(3.31), we obtain

$$i_{zg}(t) = C_{gd}\left[-\frac{I_{dc}}{\omega_s C_{out}}\{\omega_s - a\omega_s \sin(\omega_s t + \phi)\} + V_0 \omega_s \cos(\omega_s t)\right] + C_{gs} V_0 \omega_s \cos(\omega_s t) \tag{3.32}$$

When the switch is on, the voltage across the switch is 0, but the voltage across C_{gs} is not, hence the voltages across C_{gs} and C_{gd} are the same and equation (3.30) significantly simplifies. Following the previous procedure, during the interval $\frac{T_s}{2} \leq t \leq T_s$, i_{zg} is found to be

$$i_{zg}(t) = (C_{gd} + C_{gs})\omega_s V_0 \cos(\omega_s t) \tag{3.33}$$

The unknown load Z_g can now be found from the voltage v_{gs} and i_{zg}. It is easier to start with the interval when the switch is on. Because the current $i_{zg}(t)$ from (3.33) lags the voltage from (3.29) by $\frac{\pi}{2}$ it is safe to assume that Z_g has to be inductive. To find the required equivalent inductance that imposes a class-E self-synchronous rectification, the current-voltage relationship is

$$v_{gs}(t) = L_g(C_{gd} + C_{gs})\frac{d(\omega_s V_0 \cos(\omega_s t))}{dt} = -V_0 \sin(\omega_s t) \tag{3.34}$$

Solving for L_g,

$$L_g = \frac{1}{(C_{gs} + C_{gd})\omega_s^2} \tag{3.35}$$

which is the inductance required to resonate C_{gd} and C_{gs} in parallel. The L_g value in (3.35), however, would short the output capacitance during the OFF-state, leading to a zero voltage across the switch. Resonating C_{gs} + C_{gd} at a slightly higher frequency would ensure a finite C_{out} and the desired class-E operation. Therefore, the idealized theoretical analysis gives the designer a starting point for choosing the gate termination for class-E synchronous rectification.

3.5.2 Non-linear model simulations

To validate the above simplified analysis, ADS simulations of a semi-ideal class-E rectifier using harmonic balance are performed. The improved 8×75 μm GaN HEMT model from [4,5] previously used in Section 3.3 is used again in this section. The simulation involves ideal bias-Tees and an ideal tuner presenting an open circuit at $5f_s$, $4f_s$, $3f_s$, $2f_s$ and the ideal class-E impedance given by equation 3.1 and 3.2 at f_s for a C_{ds}= 0.202 pF and f_s=1.2 GHz. The DC load R_{DC} is set equal to 90 Ω and the transistor is biased in pinch off with $V_g \approx$ -4. V. A load pull was performed at the gate port of the rectifier to find the impedance Z_g that achieves maximum RF-DC convertion efficiency and maximum output power for an input power of 33 dBm (2 W). The optimum impedance is found to be approximately $j89.46\,\Omega$, which represents the reactance a

11.9 nH inductor produces at 1.2 GHz. Fig. 3.26 shows the DC output power (blue) and efficiency (red) contours resulting from the simulated load pull. The maximum efficiency is 66.7 % with a DC output power of 31.14 dBm. Fig. 3.27 shows the dynamic load line for the respective impedance points a), b), c), and d) marked in Fig. 3.26.

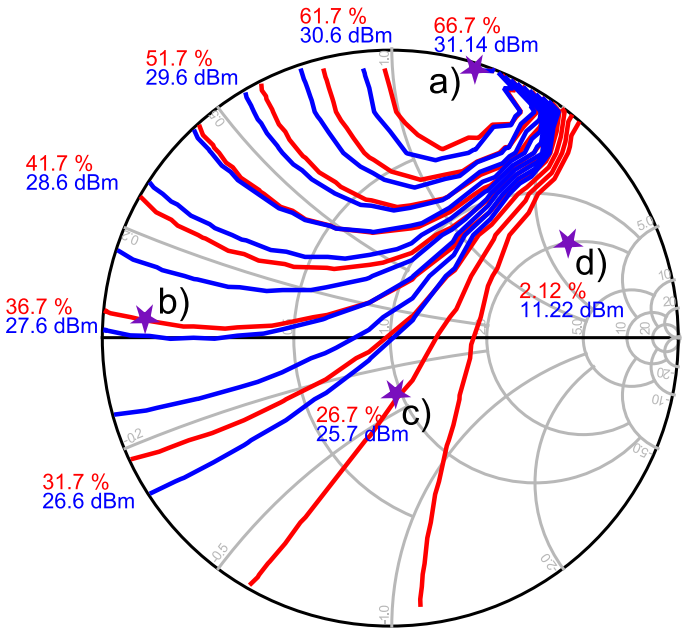


Figure 3.26: RF-DC efficiency contours (Red) and DC output power contours (blue) obtained in a load pull simulation preformed at the gate port of a class-E self-synchronous rectifier using an improved non-linear GaN HEMT model [4, 5]. Results are obtained under a V_{gs}=-4 V bias, R_{DC}= 90 Ω and an input power of 33 dBm (2 W). Impedance points a, b, c, and d, correspond to the impedance at the gate port for the dynamic load lines presented in Fig. 3.27.

The contours and the dynamic load lines clearly illustrate how the performance of the rectifier diminishes as the equivalent reactance presented to the input of the GaN HEMT fails to approximately resonate $C_{gs}+C_{gd}$. Impedance a) in Fig. 3.26 is the optimum impedance that minimizes power dissipation by approximating an ideal diode as shown in Fig. 3.27 (a). When the transistor is off and the voltage v_{ds} swings positively, the transistor should block the voltage and operate on the I_{ds}=0 region along the V_d axis. To ensure this, v_{gs} swings deeper into the pinch-off region as v_{ds} increases. As v_{ds} decreases toward 0 due to the resonant nature of the output network, v_{gs} increases and approximates the operating (I-V) characteristics of an ideal conducting diode near the I_d axis in the third quadrant. As the impedance gets farther away from the

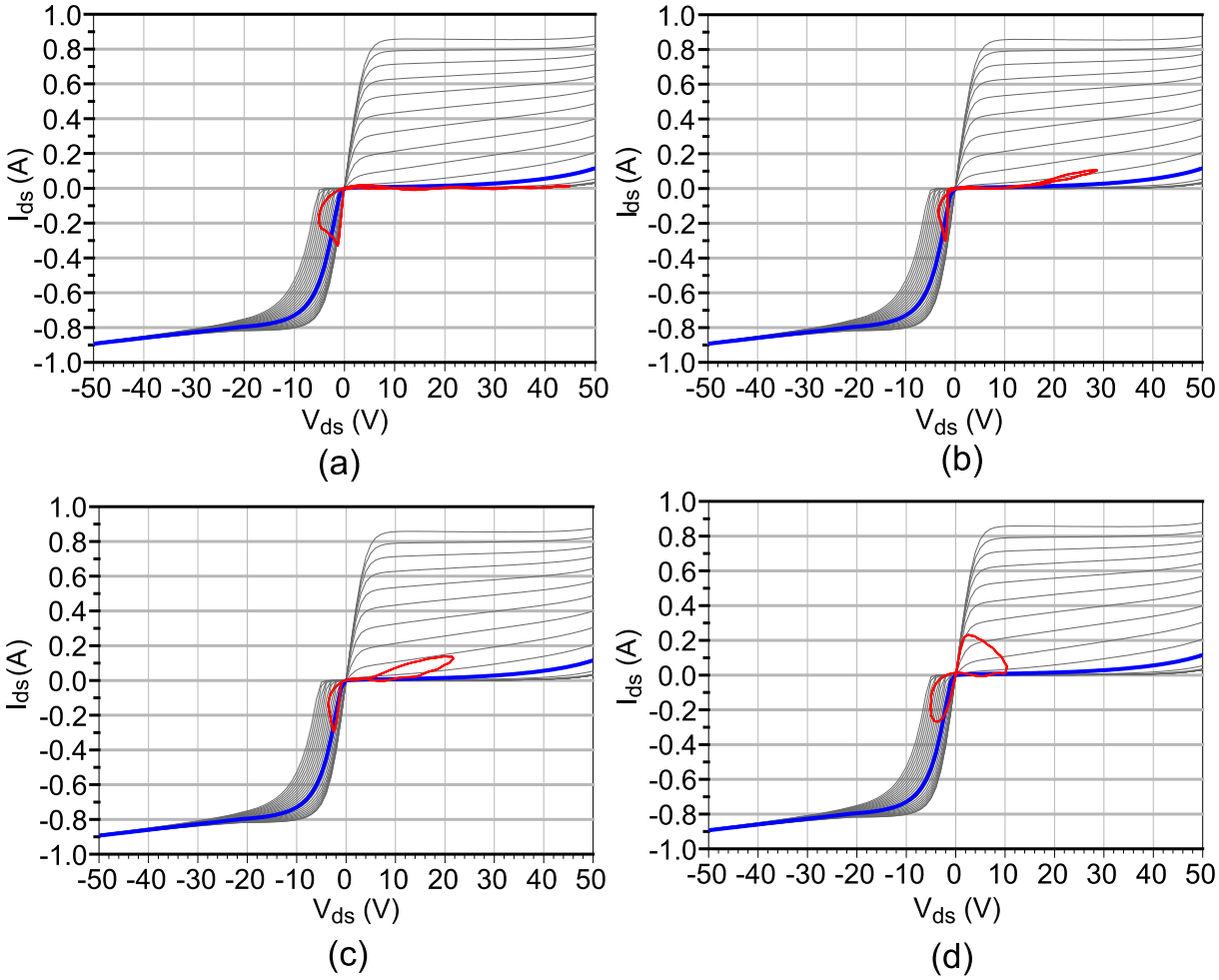


Figure 3.27: Simulated dynamic load line (red) corresponding to impedance points a, b, c, and d in Fig. 3.26. The blue line shows the I-V curves for the quiescent bias ($V_g = -4$ V).

equivalent reactance necessary to approximately resonate $C_{gs} + C_{gd}$, more power is dissipated because the transistor momentarily conducts when the switch should be off, as shown in Fig. 3.27 (b-d). The performance degrades as the impedance resonates C_{gs} and C_{gd} below f_s as in Fig. 3.26d and 3.27d. Thus the impedance presented to the gate should resonate at a slightly higher frequency than f_s as discussed in section III A, and equation (3.35), as well as to account for non-linearities of C_{gs} and C_{gd}.

For the simulated design, C_{gs} and C_{gd} are highly non-linear, with their profile plotted in Fig. 3.28 and Fig. 3.29 respectively.

C_{gd} has a maximum of ≈ 0.47 pF at $v_{gs} \approx 1$ V and C_{gd} has a maximum of ≈ 0.95 pF at $v_{gs} \geq$ -2 V. Using the maximum value of those two capacitances and the equivalent inductor presented by the optimum impedance,

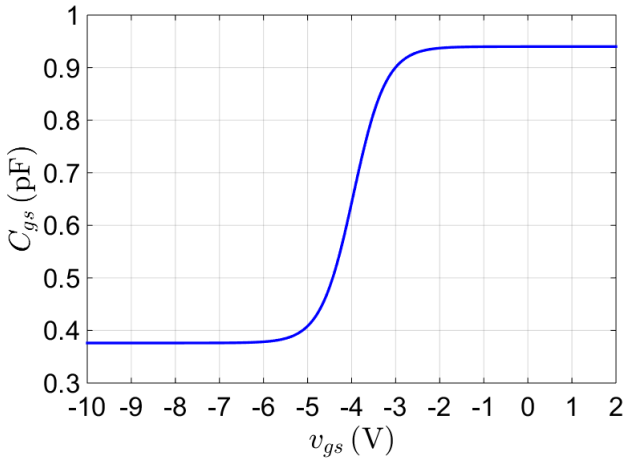


Figure 3.28: Simulated non-linear capacitance C_{gs} as a function of v_{gs} for the 8x75 μm GaN HEMT model [4, 5].

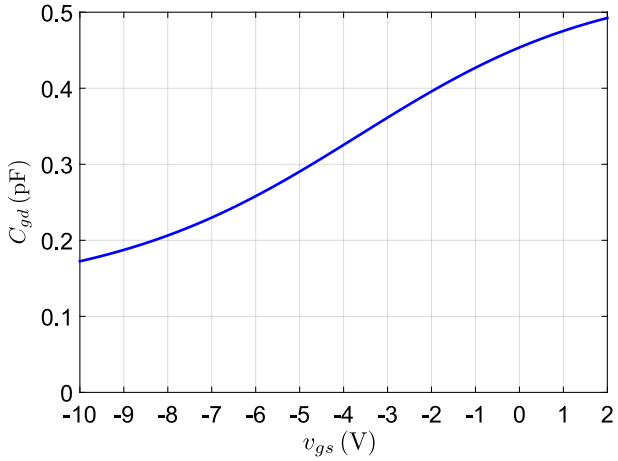


Figure 3.29: Simulated non-linear capacitance C_{gd} as a function of v_{gs} for the 8×75 μm GaN HEMT model [4, 5].

the resonant frequency f_r is

$$f_r = \frac{1}{2\pi\sqrt{(0.47\,\text{pF} + 0.95\,\text{pF})(11.9\,\text{nH})}} = 1.22\,\text{GHz} \tag{3.36}$$

which is only slightly larger than the switching frequency of 1.2 GHz. It is important to note that as the two non-linear capacitances change with v_{gs}, the presented impedance will always resonate at a higher frequency than the switching frequency, hence the requirement derived in subsection 3.5.1 is satisfied for all v_{gs}.

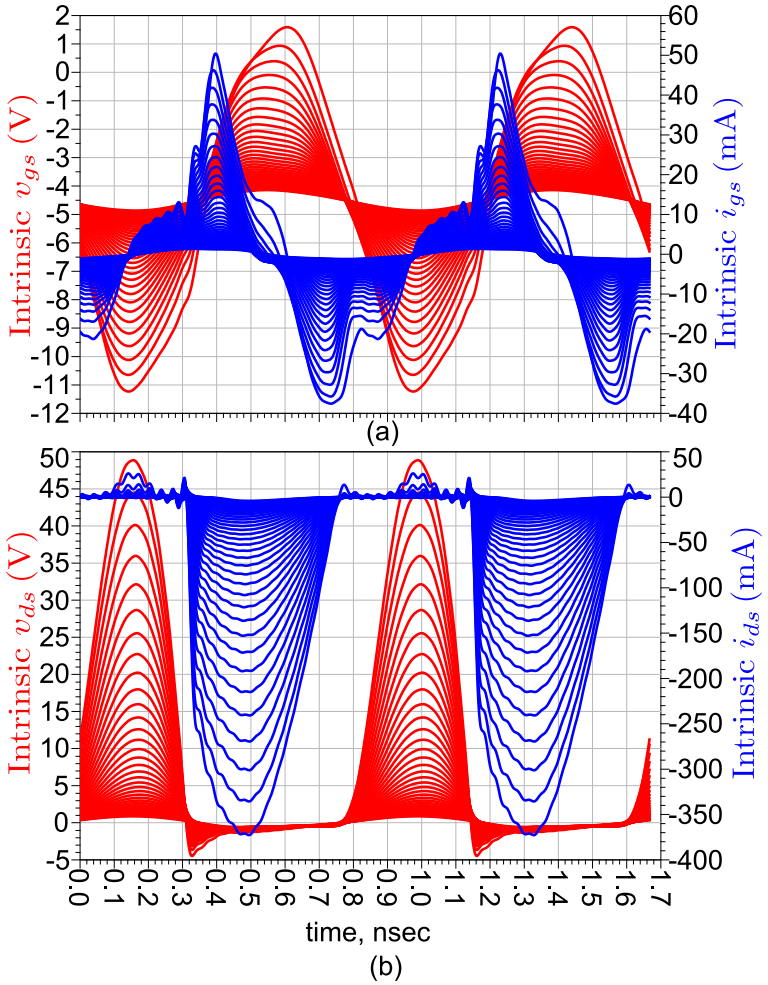


Figure 3.30: Time domain waveforms of class-E rectifier. Voltage and current waveforms at intrinsic gate (a), and at intinsic drain (b). Waveforms are shown for input powers varying from 0-35 dBm in dB steps.

Fig. 3.30 shows the time domain waveforms at the intrinsic drain and at the intrinsic gate of the transistor for varying input powers (4-34 dBm) when the gate impedance is at point (a) in Fig. 3.26. The waveforms in Fig. 3.30 (b) show approximate time-reversed class-E current and voltage waveforms at the intrinsic drain of the transistor which corroborates the ideal waveforms assumed in Fig. 3.24. Furthermore, the voltage v_{gs} simulated in Fig. 3.30 (a), approximates the sinusoidal voltage assumed in equation 3.29 and plotted in Fig. 3.25. Fig. 3.31 shows the dynamic load lines for the corresponding power levels of Fig. 3.30, which approximate the of an ideal diode for all input power.

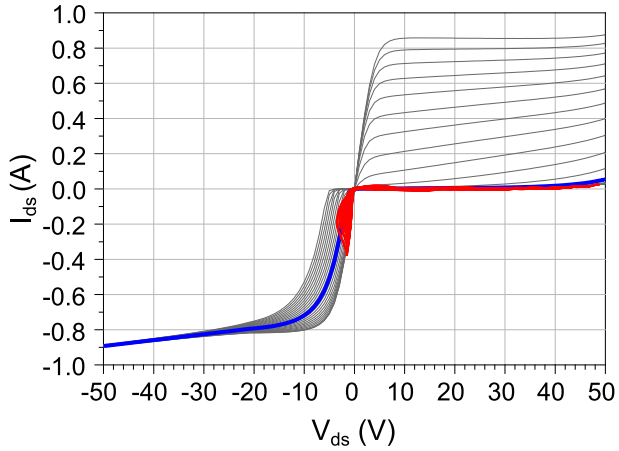


Figure 3.31: Simulated dynamic load line (red), and I-V curves of quiescent bias (blue) for class-E self-synchronous rectifier for an input power range of 0-35 dBm with Z_g resonating equivalent input capacitance at 1.22 GHz. As expected, transistor minimizes power dissipation and approximates an ideal diode.

3.5.3 Experimental validation

A series of experimental measurements are performed to validate the theoretical and simulated findings from the previous sections. In [68], a GaN HEMT MMIC class-B power amplifier operating at 10.1 GHz is also measured as a rectifier. As shown in Chapter 3, the rectifier can be expected to be approximately as efficient as the PA for the same output power. Table 3.2 shows a summary of the efficiency, RF power, and DC power measured when the circuit is operated as an amplifier and as a rectifier.

Table 3.2: Summary of X-band amplifier measured as a PA and as a rectifier

	PA	Rectifier
Max efficiency (%)	67.87	64.40
DC power (W)	4.19	1.67
RF power (W)	3.28	2.59

When the circuit is used as a rectifier, the rectifier is operated self-synchronously. A load-pull for maximum efficiency was performed at the gate port of the rectifier to find the impedance necessary for self-synchronous operation. The MMIC is mounted in a text fixture with coaxial connectors and the input and output of the MMIC is connected through bond wires to alumina de-embedding lines. By de-embedding

both, the mounting fixture and the alumina lines, the impedance presented at the input of the amplifier when the rectifier is operating self-synchronously can be determined. Furthermore, the input matching network of the MMIC is EM simulated using AXIEM as well as the process design kit (PDK) provided by TriQuint, to be able to estimate the impedance presented at the gate of the transistor. According to subsection 3.5.1, the impedance presented to the transistor should resonate C_{gs} and C_{gd} slightly above the operating frequency of 10.1 GHz. The input capacitance C_{in} of the transistor along with its output matching network is extracted from a non-linear model of the GaN HEMT. C_{in} is dominated by C_{gs} and it can serve as a good estimate of $C_{gs} + C_{gd}$. Using the estimated value of $C_{in} \approx 1.45\,\text{pF}$, the impedance at the gate of the transistor should be an equivalent inductance less than

$$L_g = \frac{1}{(2\pi f)^2 C_{in}} = \frac{1}{(2\pi 10.1\,\text{GHz})^2 1.45\,\text{pF}} = .171\,\text{nH} \tag{3.37}$$

Fig. 3.32 shows a comparison between the impedance presented to the gate of the amplifier and the 0.171 nH inductor required to resonate C_{in} at 10.1 GHz. The impedance results in an equivalent inductance equal to 0.157 nH at 10.1 GHz which would resonate C_{in} at $\approx 10.55\,\text{GHz}$. Hence, the impedance necessary for the class-B amplifier to operate self-synchronously agrees with the prediction made in subsection 3.5.1.

Additionally, the impedance presented to the gate of the class-F^{-1} PA measured in subsection 3.4.1 as a self-synchronous rectifier, also agrees with the theoretical prediction.

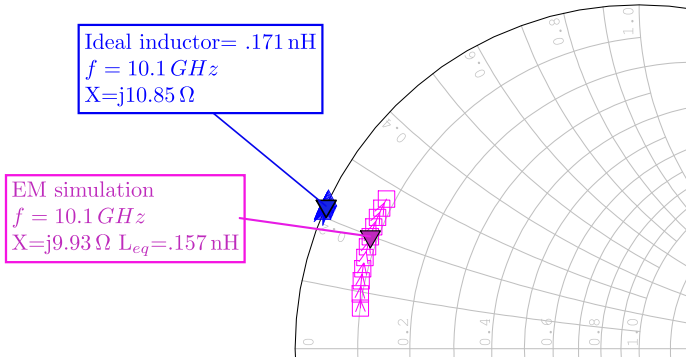


Figure 3.32: Comparison between the impedance presented to the gate of the transistor when the rectifier is operated self-synchronously (Pink) and the ideal 0.171 nH inductor (blue) required to resonate the 1.45 pF input capacitance of the transistor. The figure shows the impedance presented to the transistor resonates the input capacitance above the operating frequency of 10.1 GHz

3.6 Conclusion

In this chapter the implementation of the concept of time-reversal duality is applied to the design of high-efficiency RF power amplifiers and high-efficiency RF rectifiers. It was shown that a high-efficiency PA designed using well known techniques to improve the efficiency, such as harmonic terminations, can change its mode of operation to that of a high-efficiency rectifier. Therefore, the duality between a RF PA and a RF rectifier is introduced. In addition, for the first time, a detail theoretical analysis of the operation of a self-synchronous rectifier was presented. The theoretical analysis is validated through simulations and experimental measurements and it gives designers sufficient insight to design a self-synchronous rectifier without the need of a load-pull setup. The goal of the chapter is to lay the groundwork for the development of a RF dc-dc converter by leveraging the PA-rectifier duality. Contributions of this chapter include:

- The application of the concept of time-reversal duality to the design of high-efficiency RF power amplifier and high-efficiency RF rectifiers.
- Investigation of the RF PA-rectifier duality through non-linear simulations using an improved non-linear model of a GaN HEMT that accurately represented the third quadrant of the transistor. The non-linear simulations are reported in [22].
- Experimental verification of the PA-rectifier duality through Large Signal measurements of a 2.14 GHz PA operating as a high-efficiency power amplifier and a high-efficiency rectifier.
- Demonstration of a RF rectifier operating as a synchronous rectifier without the need of a driver i.e. operating self-synchronously.
- A theoretical analysis of the operation of a class-E self-synchronous rectifier. As well as a theoretical approach to the design of a self-synchronous rectifier instead of a measurement based approach.
- Non-linear simulations validating and expanding the theoretical analysis of a class-E self-synchronous rectifier

- Experimental validation of the analysis presented through the measurement of a GaN class-E self-syncrhonous rectifier as well as a GaN class-B power amplifier operating as a self-synchronous rectifier.
- The work presented in this chapter is published in IEEE Transactions on Microwave Theory & Techniques [21, 24]

Chapter 4

RF Class-E^2 DC-DC Converter Design

Contents

4.1 Introduction

In the past five years, there has been significant advances in the performance of converters operating into the tenths of megahertz and even into hundreds of MHz e.g. [11,13,14]. Some of the advances are no doubt been driven by developments in bandgap semiconductors and high frequency magnetics. The increased voltage and power densities enabled by bandgap semiconductors such as GaN, present a potential for monolithic integration towards a chip-scale power supply implementation [72]. Thus, the interest to further increase the frequency of dc-dc converters has become a topic of interest.

Higher switching frequencies are accompanied by reduced efficiency and attainable power levels, since the losses in both passive and active components increase with frequency as shown in Chapter 2. In addition, parasitic reactances in the active devices and packages limit switching frequencies. Table 4.1 presents an overview of high-frequency dc-dc converters and their respective efficiencies reported in the literature in recent years. In [73], a 30-MHz 200-W dc-dc converter operating at up to 200 V is demonstrated. A 23-W, 87 % efficient boost converter switching at 110 MHz is implemented using LDMOS technology in [74]. In [75] an integrated low power four-phase buck converter is implemented in a 90-nm CMOS process with switching frequencies of 100-317 MHz. An off-chip air-core inductor is used in this case, resulting in efficiencies of 80 % to 87 %. In [14], a 100-MHz switching frequency buck converter is integrated together with its drive circuitry on a single 2.3 mm $\times$ 2.3 mm chip in the TriQuint (Qorvo) 150-nm GaN on SiC D-mode pHEMT process. This converter exhibits an efficiency of over 90 % at 7 W.

This chapter presents the design and experimental demonstration of class-E^2 dc-dc converters operating at UHF and microwave frequencies. The design methodology relies on PA-rectifier duality and the design of a high-efficiency class-E^2 converter consisting of a high-efficiency class-E RF power amplifier and a high-efficiency class-E power rectifier presented in Chapter 3. Fig. 4.1 depicts the different converter topologies developed in this chapter. Section 4.2 presents detail design and measurement results for the well-known

Table 4.1: High frequency DC-DC converters comparison

Ref.	Year	f (GHz)	Technology	P_{out} (W)	η (%)
[73]	2008	0.030	MOSFET	220	87
[14]	2014	0.100	GaN	7	91
[74]	2009	0.110	LDMOS	25	86
[75]	2005	0.233	CMOS	0.55	82
[76]	2012	0.780	GaN	11.5	72
This work	2015	0.9	GaN	12.8	79
[77]	2013	1	GaN	8.5	77
This work	2015	1.2	GaN	5.0	75
[78]	1999	4.5	GaAs	0.053	64

synchronous operation [77, 79], presented in [23, 24] and shown in Fig. 4.1 (a). The synchronous operation requires a RF source or driver for the gate of both PA and rectifier, transistors. Section 4.3 then reconfigures the synchronous converter to operate the rectifier self-synchronously. The overall performance of the converter with a self-synchronous rectifier is comparable to the synchronous version, but eliminates an entire RF part of the circuit as shown in Fig. 4.1 (b). Finally, in Section 4.4, a 900 MHz class-E^2 converter with the original topology modified so as to have no RF inputs is shown. This converter is part of a collaboration with the University of Cantabria in Santander, Spain. In this circuit, the input of the inverter is modified to transform the power amplifier into a power oscillator, while the rectifier is operated self-synchronously. The topology of the converter is depicted in Fig. 4.1 (c). The efficiency of this converter reaches nearly 80 % with over 10 W of dc output power.

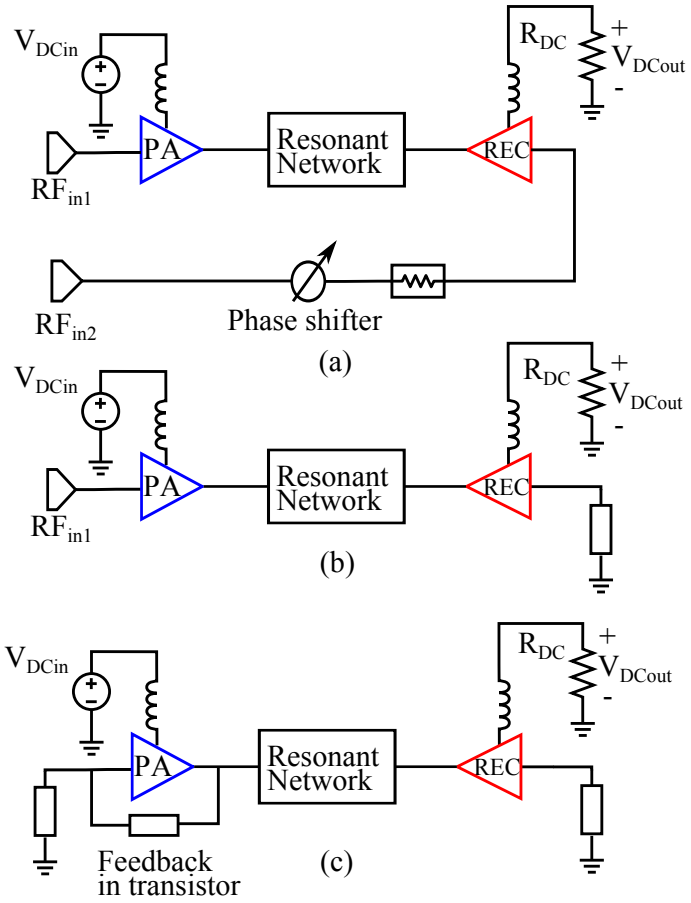


Figure 4.1: Block diagram of high frequency class-E^2 dc-dc converter. (a) a synchronous topology; (b) a self-synchronous topology with a single RF input at the inverter input; and (c) a oscillating, self-synchronous topology with no RF inputs.

4.2 Synchronous class-E^2 DC-DC converter

4.2.1 Design and fabrication

Extensive research has been performed in class-E switching power amplifiers since Sokal introduced it in 1975 [32]. Some examples are [58, 59, 80] just to name a few. As early as 1980, the idea of incorporating a class-E PA into a dc-dc converter was suggested by Gutmann [81]. In that paper, Gutmann coupled a 1-MHz class-E inverter to a harmonically terminated diode from [82]. A couple of years later, Redl and Molnár published a series of articles expanding on Gutmann's work [83–85]. Kazimierczuk investigated applications of class-E power amplifiers, including class-E power oscillators [86, 87] and class-E PAs with

non-sinusoidal output voltage. He later explored class-E diode rectifiers [67,88–90], and ultimately proposed a class-E^2 dc-dc converter [60,79,91]. [92] offers a summary of resonant topologies for high frequency dc-dc converters suggested by Kazimierczuk in 1989. In this section, a class-E^2 dc-dc converter similar to the one shown in Section 3.2 operating at gigahertz frequencies is designed and measured. First, the maximum frequency of operation was estimated using equation 4.1 from [71]

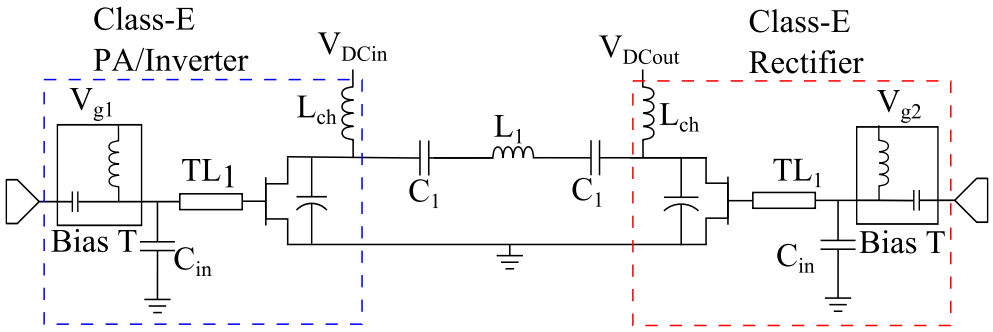
$$f_{max} = \frac{I_{DS}}{2\pi^2 C_{out} V_{DS}} \tag{4.1}$$

The transistor chosen for the design of the converter is the T2G6001528-Q3 GaN pHEMT from TriQuint Semiconductor. The output capacitance C_{out} is estimated using models provided by Modelithics and TriQuint, the capacitance is estimated to be 2.7 pF. Using the estimated value of C_{out}, V_{DS}= 18 V and I_{DS}=1.4 A in (4.1), a maximum switching frequency of ≈1.5 GHz is obtained. 18 V is used because lower voltages than the nominal 28 V are of interest for the intended application. In order to account for additional parasitic capacitance, and inaccuracies in the model while maintaining a high switching frequency, a more conservative operating frequency of 1.2 GHz is chosen. The impedance to be synthesized by the matching network for a class-E amplifier according to [71] is given by

$$Z_{net} = \frac{0.28015 e^{j49.0524^\circ}}{\omega_s C_{out}} = 9 + j10.4\,\Omega \tag{4.2}$$

As described in Section 3.2, the rectifier provides the correct value of Z_{net} and the reactances presented to the amplifier and the rectifier can be combined into one, resulting in Z_{net}. According to ideal class-E theory, all the harmonics should be terminated in an open or short circuit at the output capacitance C_{out}. In lower frequency converters the termination of individual harmonics does not usually present a problem, but at 1.2 GHz, the proper termination of the second and third harmonic becomes imperative for high efficiency operation. According to [80], termination of only the second and third harmonics in a class-E amplifier can achieve a maximum efficiency of more than 80% ignoring other losses such as R_{ON}. Different topologies were investigated to synthesize Z_{net} at f_s and provide an open circuit at $2f_s$ and $3f_s$. Incorporating harmonic traps at $2f_s$ and $3f_s$ with lumped elements resulted in a better termination of harmonics but in lower

overall efficiencies due to the added conduction losses brought by the additional capacitors and inductors. Ultimately, the approach used in [76] resulted in the best compromise between harmonic termination and overall efficiency at approximately 1 GHz switching frequency. The approach consists of using the parasitic capacitance of a series inductor L_1 as shown in Fig. 4.2 to provide an approximately open circuit at $2f_s$ and $3f_s$ by using the inductor's self resonance (SRF). This is done by ensuring the inductor resonates with its parasitic capacitance at a frequency between $2f_s$ and $3f_s$. This approach provides harmonic terminations for both, the PA and the rectifier using a single inductor. Z_{net} is then synthesized by using the series capacitor C_1 from Fig. 4.2 to tune the impedance at the fundamental. The input and output bias-T are realized using a LC low pass filter optimized for low loss and the input of the transistor, for both rectifier and PA, is matched to 50 Ω with a shunt capacitor to ground and a section of transmission line.



C_{in}	3.9 pF	C_1	12 pF
L_{ch}	24 nH	TL_1	4 mm
L_1	1.8 nH	Bias T	28 nH 33 pF

Figure 4.2: Circuit schematic for class-E^2 converter consisting of a class-E PA and rectifier coupled through a resonant network. The value of all components is given in the table

For the sake of maintaining a low circuit profile, only passive components with a maximum thickness of 2 mm are considered in the design. This restriction limits the value of inductors that can be considered because commercially available high-frequency inductors have current handling capabilities proportional to their size. Inductors from Coilcraft's 0603HP series, and capacitors from ATC's 600L and 600S series are chosen for the 1.2-GHz design presented in this chapter. The inter-stage network is simulated using NI/AWR MWO with high frequency models for the passive components provided by Modelithics. Because the non-linear model of the transistor does not accurately model the third quadrant where the rectifier operates, the

transistor was replaced by the ideal resistive load given by Re$\{Z_{net}\}$. The design is implemented on a 30- mil Rogers RO4350B substrate. The simulated frequency response of the output matching is shown in Fig. 4.3.

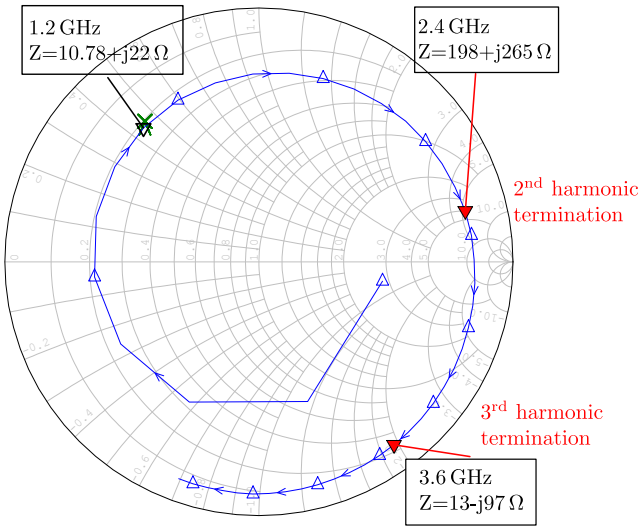


Figure 4.3: Frequency response of the simulated inter-stage network. The rectifier transistor is replaced by the ideal resistive load given by Re$\{Z_{net}\}$ and high frequency models from Modelithics are used for all the passive components. The termination of the second and third harmonics are shown at 2.4 and 3.6 GHz. The green marker indicates the targeted impedance at the fundamental.

The second harmonic is terminated in an impedance equal to 198 + j265 Ω and the third harmonic is terminated in 3 - j97 Ω. Priority is given to the termination of the second harmonic since it has a bigger effect in efficiency. The green cross in Fig. 4.3 indicates the targeted impedance at the fundamental frequency for a class-E^2 converter and the marker shows the impedance presented by the simulated inter-stage network. A photograph of the prototype built is shown in Fig. 4.4.

4.2.2 Measurement results for the synchronous converter

The converter is then characterized with the measurement setup shown in Fig. 4.5. The PA is biased at a quiescent current of 10 mA for input voltages ranging from 12-27 V. The rectifier is pinched off at approximately V_{gs}=-4.5 V. R_{DC} is implemented using a BK Precision 8500 electronic DC load in a constant voltage mode enforcing output voltages ranging from 10-27 V. An electronic load is used as R_{DC} in order to automate and expedite the characterization of the converter. The measurements were reproduced using a

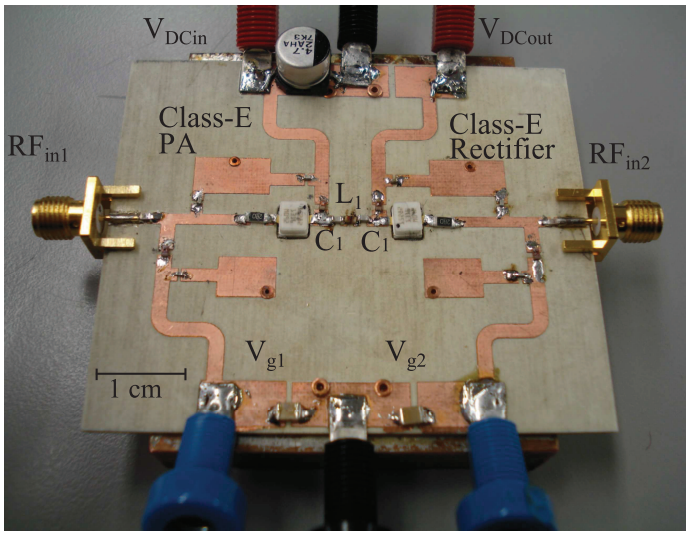


Figure 4.4: Photograph of class-E^2 converter prototype. The left side of the circuit is the class-E inverter and the right a synchronous rectifier. They are coupled through the reactive network consisting of L_1=1.8 nH and C_1= 12 pF

passive resistive load to ensure the electronic load did not influence the measurements in any way. All the measurements are performed with P_{in}= 23 dBm. The phase shift is adjusted for maximum efficiency and synchronous operation.

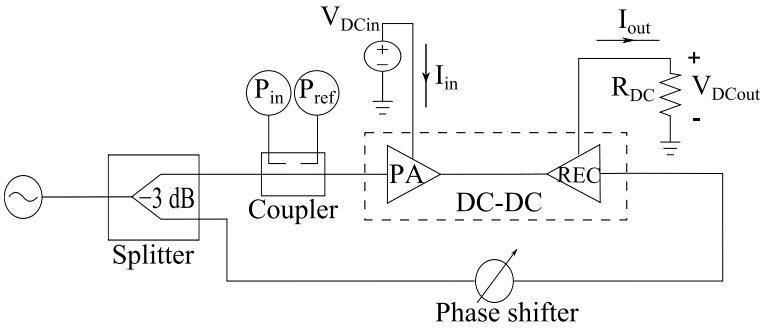


Figure 4.5: Setup used to characterize the class-E^2 converter prototype. The output voltage is enforced by the electronic load while the current is allowed to be set by the converter itself.

The efficiency of the converter is defined as

$$\eta_{DC-DC} = \frac{V_{DCout} I_{DCout}}{V_{DCin} I_{DCin}} \tag{4.3}$$

The performance of the converter is more efficient at medium to lower voltages as designed. The output

power of the converter increases with input voltage, while the efficiency of the converter decreases with increasing input and output voltage. This is expected, since the higher dc input voltage allows for a higher-amplitude ac voltage waveform at the output of the PA. The decrease in efficiency at higher dc input voltages seems to point out to the switching losses at the PA's transistor being the main source of loss. Fig. 4.6, shows the efficiency and output power as a function of output voltage for 13 (low), 17 (medium) and 27 (high) V input voltages. The maximum efficiency of the converter is 70 % at an input voltage of 13 V and an output voltage of 10 V with an output power of 4.5 W. As previously explained, higher output power is obtained with increase input voltage up to a maximum output power of 11.5 W with an efficiency of 54 %.

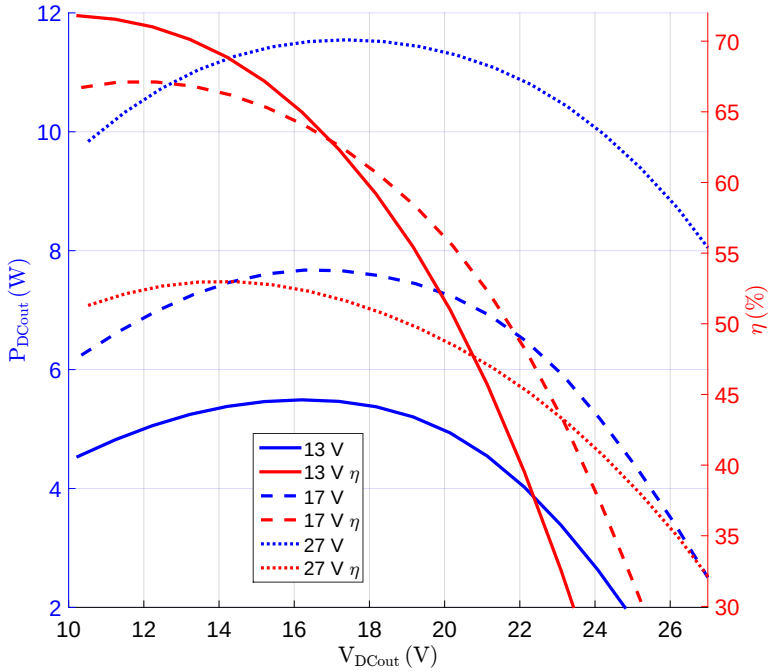


Figure 4.6: Measured converter efficiency (red) and output power (blue) plotted as a function of output voltage for input voltages of 13, 17 and 27 V.

4.3 Class-E^2 DC-DC converter with self-synchronous rectifier

4.3.1 Design and fabrication

In order to implement a self-synchronous rectifier in the class-E^2 converter design in Section 4.2, a load pull for maximum efficiency is first performed at the gate port of the rectifier at an input voltage of 13, 17 and 27 V. It is found that the optimum gate impedance for maximum efficiency is not significantly affected by the output voltage of the converter. The results for 17 V are plotted in Fig. 4.7, with the optimum impedance found to be approximately 3.7 + j44.3 Ω at the connector reference plane.

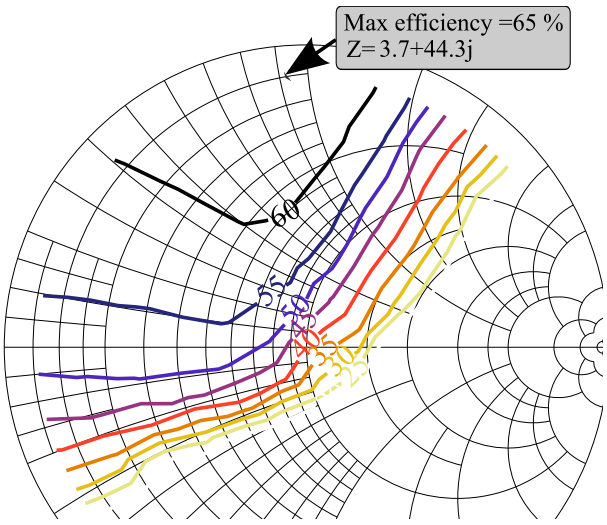


Figure 4.7: Impedance constellation and efficiency contours produced by a load pull performed at the gate port of the rectifier for maximum efficiency for a DC output voltage of 17 V. The Smith chart is normalized to 50 Ω.

A length of transmission line and a 8 pF shunt capacitor to ground are used to present this impedance to the transistor. The equivalent input capacitance of the transistor is estimated using a non-linear model to be approximately 8.5 pF. Following the theory presented in Section 3.5, the impedance that the matching network of the rectifier presents to the input of the transistor should resonate the 8.5 pF slightly above the switching frequency of 1.2 GHz. Fig. 4.8 plots a EM simulation of this impedance and the impedance of an ideal 2.07 nH inductor necessary to resonate the 8.5 pF at 1.2 GHz. Fig. 4.8 clearly shows the impedance of the matching network follows that of the inductor, supporting the theory.

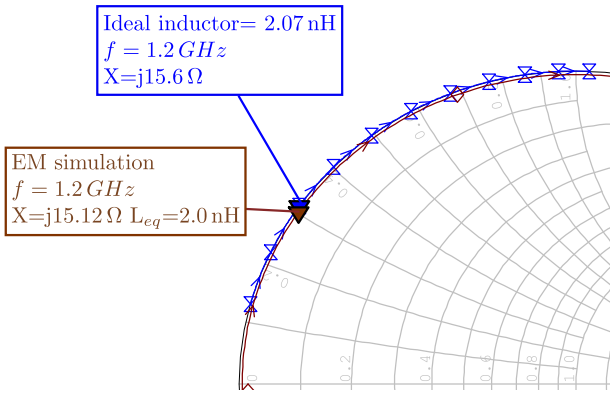


Figure 4.8: Comparison between the impedance presented by the rectifier's input matching network EM simulated (Brown) and the ideal 2.07 nH inductor (blue) required to resonate the 8.5 pF input capacitance of the T2G001528 transistor model. The figure shows the impedance of the matching network closely follows the impedance of the ideal inductor around the switching frequency.

The prototype of a class-E^2 converter with its rectifier operating self-synchronously is shown in Fig. 4.9.

The design is almost identical except for the removal of the rectifier's connector and input matching network.

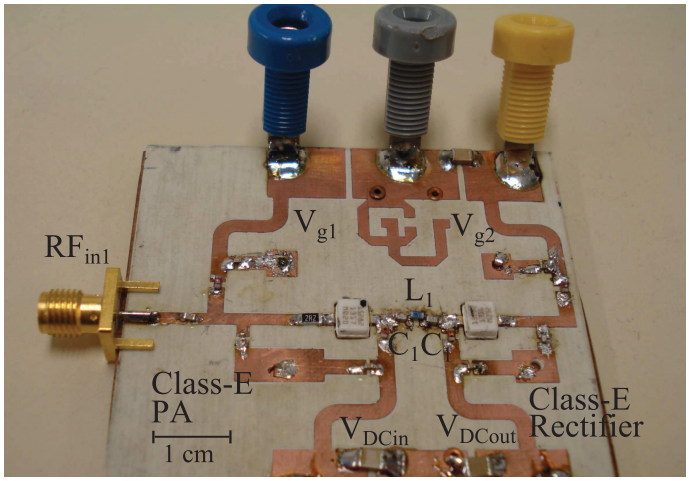


Figure 4.9: Photograph of class-E^2 converter with the rectifier operating self-synchronously. The RF port at the gate of the rectifier is removed and the input matching network is modified to present the optimum impedance to the rectifier. The size of the circuit board is 5.6 cm by 6 cm.

4.3.2 Measurement results for the converter with self-synchronous rectifier

The converter is then characterized following the procedure described in subsection 4.2.2 but without the need of a second RF driver for the rectifier. Fig. 4.10 shows the efficiency and output power as a function of

output voltage for 13, 17, and 27 V. The results are improved compared to those of Fig. 4.6. The converter is the most efficient at 13 V input voltage and at lower output voltages in general, achieving an efficiency above 70 % for output voltages ranging from 11-17 V, with a maximum efficiency of 75 % and 4.6 W compared to the 72 % efficiency of the converter from section II. The improvement can be attributed to a shift in the value of the passive components used in the resonator, specifically the inductors which have a ±5 % tolerance. This converter of course completely removes the need of a secondary driver for the rectifier, which not only eliminates a RF source but also the phase shifter necessary for synchronous operation.

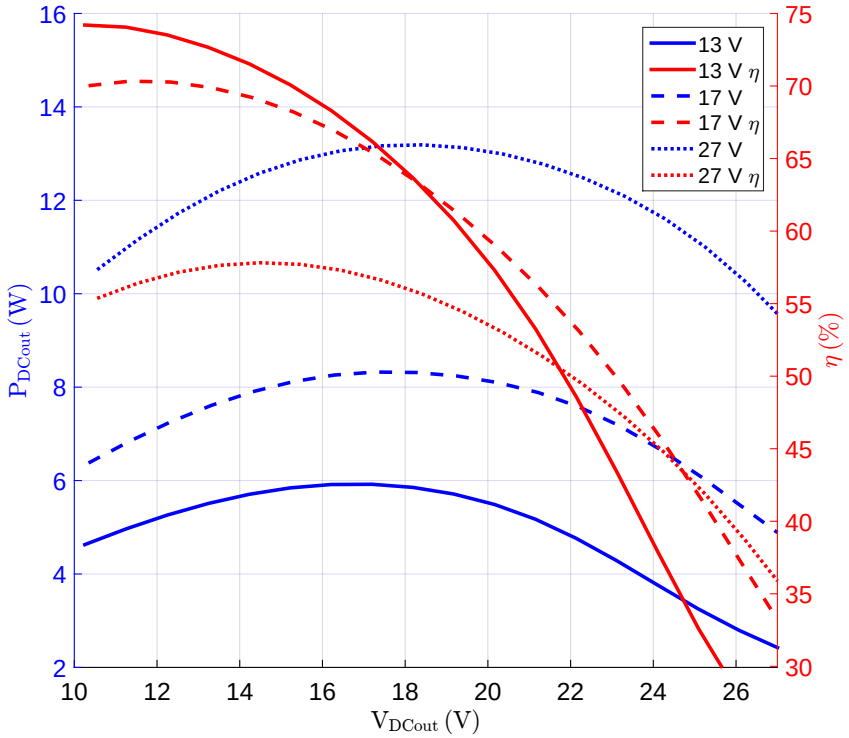


Figure 4.10: Measured self-synchronous class-E^2 converter efficiency (red) and output power (blue) as a function of output voltage for input voltages of 13, 17 and 27 V.

4.3.3 Estimate of losses in the converter

Allocating losses in the converter becomes particularly challenging for the converter shown here due to lack of traditional equipment such as oscilloscopes being able to operate at such high frequencies. Additionally,

not having access to the inter-stage network, makes measuring losses in the resonator difficult or nearly impossible. Therefore, the losses are estimated theoretically according to known parameters of all the passive and active components, and measured results. For example, the losses in the resonator are estimated as follows:

From the datasheet provided by coilcraft, the 1.8 nH inductor from the 0603HP series has a Q of 40. From the definition of Q

$$Q_L = \frac{\omega_s L}{R_s} \tag{4.4}$$

the series resistance of the inductor can be obtained. Substituting the switching frequency of the converter and the inductance values we obtain

$$R_s = \frac{(2\pi 1.2\,GHz)(1.8\,nH)}{40} = 0.34\,\Omega \tag{4.5}$$

Assuming the current through the resonator is sinusoidal, the amplitude of the sinusoidal current waveform is

$$I_m = \frac{\sqrt{\pi^2+4}}{2} I_{dc} = 1.862 I_{dc} \tag{4.6}$$

which can be used to calculate the power dissipated in the resonating inductor. The losses are estimated for the case with maximum efficiency where V_{in}=13 V,I_{in}=.53 A, V_{out}=11 V, and I_{out}=0.44 A. The power dissipated in the resonating inductor then becomes

$$P_L = \frac{R_s I_m^2}{2} = \frac{(0.34\,\Omega) \times (1.862(0.53\,A))^2}{2} = 0.166\,W \tag{4.7}$$

the losses in the two resonating capacitors can be estimated from their equivalent series resistance (ESR) as

$$P_C = \frac{(ESR) I_m^2}{2} = \frac{(0.1\,\Omega) \times (1.862(0.53\,A))^2}{2} = 0.55\,W \times 2 = .110\,W \tag{4.8}$$

The conduction losses in the two bias-T choke inductors can be easily estimated by assuming a purely DC current flowing as

$$P_{chokePA} = R_s I_{in}^2 = (0.1\,\Omega)(0.53)^2 = .028\,W \tag{4.9}$$

$$P_{chokeREC} = R_s I_{in}^2 = (0.1\,\Omega)(0.44)^2 = .02\,W \tag{4.10}$$

The conduction losses when the transistor is conducting can be calculated by estimating R_{on} from the simulated I-V curves of the transistor. R_{on} for the T2G6001528-Q3 was estimated to be $\approx 0.5\,\Omega$, due to the lack of a transistor model that accurately represents the third quadrant of the transistor, the same value of R_{on} is used for the rectifier. The rms value of the current through the switch can be found by integrating the current through the switch for half a cycle or 0.5 duty cycle as

$$I_{srms} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} i_s^2 d(\omega t)} \tag{4.11}$$

which can be found from [29] as

$$I_{srms} = \frac{I_{dc}\sqrt{\pi^2 + 28}}{4} \approx 1.54 I_{dc} \tag{4.12}$$

hence the switch conduction losses for the PA and rectifier respectively are

$$P_{lossPA} = R_{on} I_{srms}^2 = (0.5\,\Omega)(1.54 \times 0.53\,A)^2 = .34\,W \tag{4.13}$$

$$P_{lossREC} = R_{on} I_{srms}^2 = (0.5\,\Omega)(1.54 \times 0.44\,A)^2 = .23\,W \tag{4.14}$$

A summary of the estimated losses is shown in Table 4.2

As shown in Table 4.2, almost half of the total losses are unaccounted for. The majority of those losses can be attributed to losses in the ON-OFF and OFF-ON transition which are not addressed here.

A photograph of the converter after operating for an entire day was taken using an infrared camera to assess the main source of heat dissipation in the converter. The photograph is shown in Fig. 4.11. Although the temperature shown is not accurate because the emissivity is not calibrated, the photograph is useful to

Table 4.2: Summary of estimated losses

Conduction losses PA transistor	0.34 W
Conduction losses Rectifier transistor	0.23 W
Resonator	.276 W
Inverter bias-T	0.03 W
Rectifier bias-T	0.02 W
Total passive components losses	.9 W
Other losses	1.15 W

conclude the main source of power dissipation, other than the transistor, is the small resonating inductor. Therefore, higher efficiency can be achieved by concentrating in reducing the conduction losses of the resonant inductor.

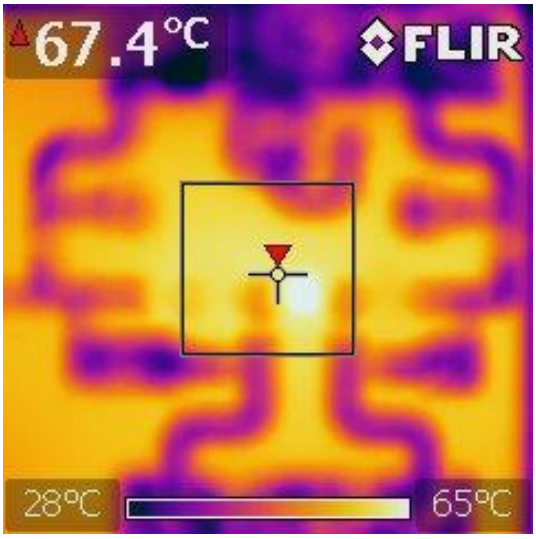


Figure 4.11: Infrared photograph of the class-E^2 dc-dc converter after operating for a full day. Emissivity is not calibrated therefore the photograph is only meant to serve as a comparison between components.

4.4 Oscillating, self-synchronous class E^2 DC-DC converter

Turning the PA of the converter into a free-running power oscillator becomes a logical, highly desirable step toward a self-driving microwave frequency resonant DC-DC converter with no RF inputs as in Fig. 4.1 (c). A similar MOSFET 2-MHz converter was published in [93] using a class-E oscillator design procedure

introduced in [94]. The converter achieved 78.9 % under 1.55 W output power using a feedback inductor to force the oscillation of the class-E inverter. In [78] a sub-watt 4.6 GHz class-E oscillator was demonstrated with a diode rectifier. In this section, the architecture of Fig. 4.1 (c) is demonstrated in a class-E^2 GaN DC-DC converter operating around 900 MHz.

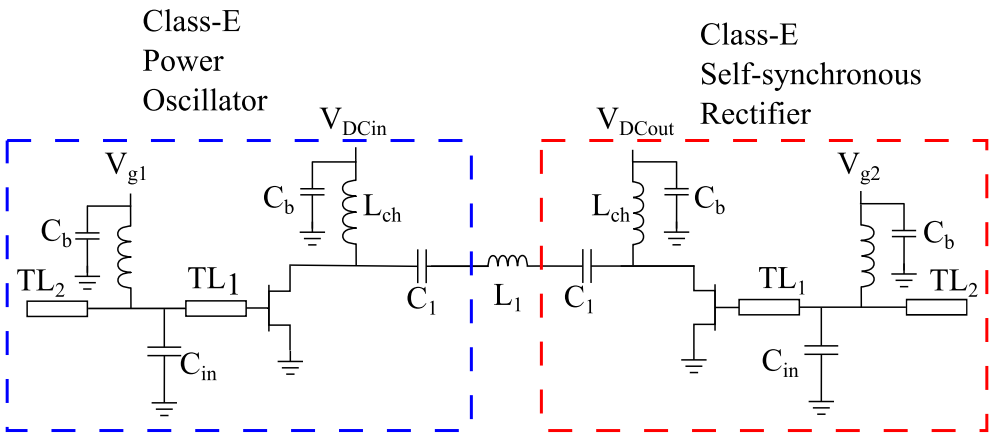
4.4.1 Design and fabrication

The design of the converter presented here is very similar to the one described in Section 4.2 and is described in [77]. The design and manufacturing of the converter were performed by Professor Jose Angel García and his group at the University of Cantabria in Santander Spain. The converter uses the CGH35030F packaged GaN HEMT from Cree Inc. The change to a higher power device and lower frequency allows for higher output power and efficiency and demonstrates feasibility of the approach by providing an alternate design. The schematic of the oscillating, self-synchronous rectifier is shown in Fig. 4.12. In order to interconnect the inverting and rectifying devices, an inductor L_1 and two capacitors C_1 are employed. Harmonic terminations at f_2 and f_3 are achieved as previously discussed through the self-resonance of L_1, while the choice of C_1 allows for reactance adjustment at the fundamental. An open circuit stub (TL_2), a high value capacitor to ground (C_{in}) and a length of transmission line (TL_1) are combined in order to synthesize the required gate impedance condition at the fundamental to operate the rectifier self-synchronously.

The simplified theoretical analysis used to analyze a class-E self-synchronous rectifier in subsection 3.5.1 can be applied to the class-E oscillating inverter, with some modifications. Substituting the current source in Fig. 3.23 by $I_{DC}(1 - a\sin(\omega_s t + \phi))$ to account for the DC current supplied to the inverter the voltage v_{sw} across the switch becomes

$$v_{sw}(t) = \begin{cases} \frac{I_{dc}}{C_{out}\omega_s}[a\cos(\omega_s t + \phi) + \omega_s t - a\cos(\phi)], & 0 \leq t \leq \frac{T_s}{2} \\ 0, & \frac{Ts}{2} \leq t \leq Ts \end{cases} \tag{4.15}$$

which corresponds to the classical ideal class-E waveforms shown in Fig. 4.13.



C_{in}	12 pF	C_1	10 pF
L_{ch}	12.5 nH	TL_1	10 mm
L_1	8 nH	TL_2	18 mm
L_b	120 nH	C_b	27 pF

Figure 4.12: Circuit schematic for self-oscillating, self-synchronous class-E^2 DC-DC converter.

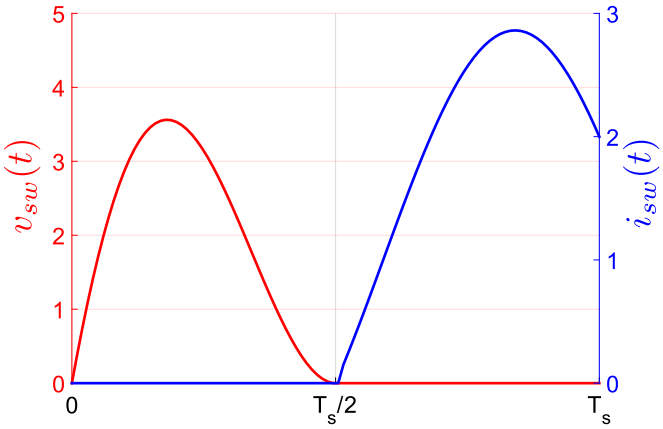


Figure 4.13: Time domain waveforms of an ideal class-E amplifier and oscillator. The waveforms are normalized.

the current i_{gd} through capacitor C_{gd} remains unchanged as

$$i_{gd}(t) = C_{gd}d\frac{(v_{sw} - v_{gs})}{dt} = C_{gd}\left(\frac{dv_{sw}}{dt} - \frac{dv_{gs}}{dt}\right) \tag{4.16}$$

When the switch is off, following (4.15) and Kirchoff's current law, we obtain

$$i_{zg}(t) = C_{gd}\left[\frac{I_{dc}}{\omega_s C_{out}}\{\omega_s - a\omega_s \sin(\omega_s t + \phi)\} + V_0\omega_s \cos(\omega_s t)\right] + C_{gs}V_0\omega_s \cos(\omega_s t). \tag{4.17}$$

When the switch is on, the voltage across the switch is shorted and the simplified circuit is identical to that of the class-E self-synchronous rectifier. Hence following the same procedure, during the interval $\frac{T_s}{2} \leq t \leq T_s$, i_{zg} is found to be

$$i_{zg}(t) = (C_{gd} + C_{gs})\omega_s V_0 \cos(\omega_s t) \tag{4.18}$$

To find the required equivalent inductance that imposes a class-E oscillator, the current-voltage relationship is

$$v_{gs}(t) = L_g(C_{gd} + C_{gs})\frac{d(\omega_s V_0 \cos(\omega_s t))}{dt} = -V_0 \sin(\omega_s t) \tag{4.19}$$

Solving for L_g,

$$L_g = \frac{1}{(C_{gs} + C_{gd})\omega_s^2} \tag{4.20}$$

which is the same inductance needed for the self-synchronous rectifier. Because equation (4.20) is identical to equation (3.35), the conclusions obtained from section Section 3.5 apply to the class-E oscillator as well. Hence, the impedance presented to the gate of the transistor should correspond to an equivalent reactance capable of resonating $C_{gs} + C_{gd}$ at a frequency slightly above the switching frequency to ensure the desired class-E soft-switching operation. For that reason, a gate matching network mirroring that of the self-synchronous rectifier was implemented in Fig. 4.12. A photograph of the oscillating, self-synchronous converter is shown in Fig. 4.14.

4.4.2 Measurement results for oscillating, self-synchronous converter

The converter is characterized in a modified setup of the one shown in Fig. 4.5; the main difference is the absence of any RF input source. The electronic load providing a constant DC output voltage is changed

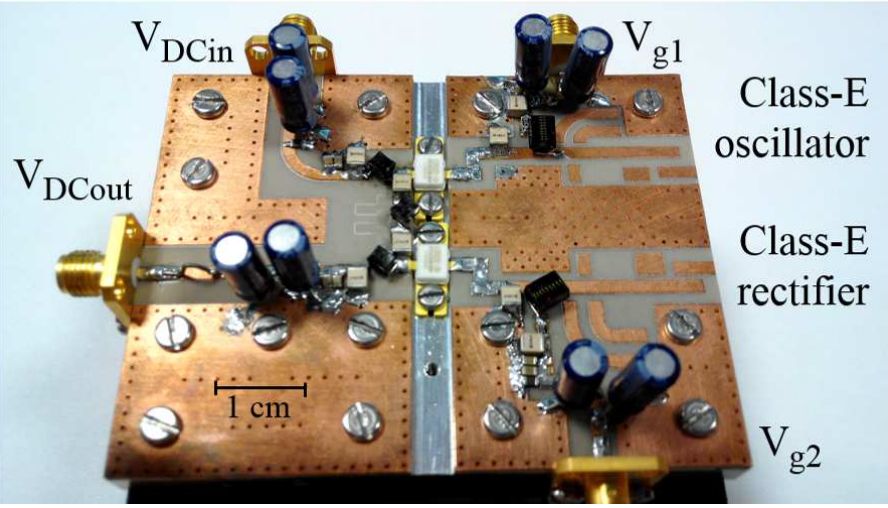


Figure 4.14: Photograph of oscillating, self-synchronous class-E^2 DC-DC converter.

to a passive 50 Ω load due to lower frequency oscillations produced by the electronic load. The rectifier was biased in pinch-off ≈ -4.0 V while the oscillator gate biasing voltage is used to initiate the oscillation by increasing the voltage above pinch-off. Once the oscillation starts at approximately -3 V, the voltage is lowered to a value approximately equal to that of the self-synchronous rectifier, where the maximum efficiency can be obtained [95].

Fig. 4.15 shows efficiency and DC output power for input voltages of 28, 22, and 17 V, as a function of output voltage. The oscillating, self-synchronous converter can only operate as a buck converter since the oscillations subside when the output voltage becomes higher than the input voltage, hence, more attention is given to higher input voltages. The converter is 79 % efficient at an input voltage of 28 V and an output power of 12.8 W. Similar to the 1.2 GHz E^2 converter, output power is directly proportional to input voltage, but efficiency is maintained above 70 % for an input voltage range of 11 V-28 V.

Output voltage control can be accomplished by FM through the oscillator's gate biasing voltage, due to the input capacitance C_{gs} variation with v_{gs} in a GaN HEMT, as shown in Section 3.5. This dependence can be exploited to control the output voltage of the converter for varying loads. When V_{g1}=-3 V, the frequency

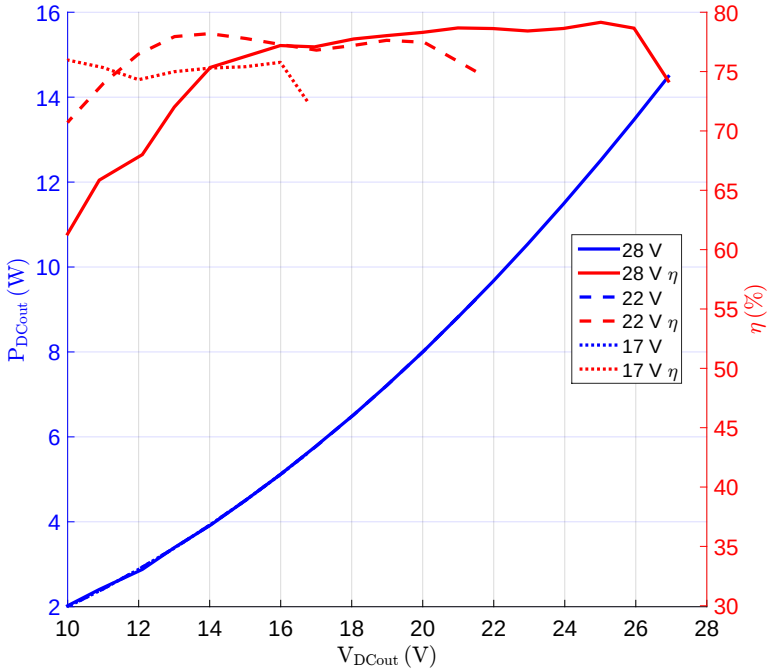


Figure 4.15: Measured performance of oscillating, self-synchronous class-E^2 DC-DC converter. Converter efficiency (red) and output power (blue) plotted as a function of output voltage for input voltages of 17, 22 and 28 V.

of oscillation starts around 920 MHz, and increases as the voltage decreases. At V_{g1}=-6.4 V the oscillation disappears, reaching a frequency of 1040 MHz. The FM control is possible thanks to the detuning of the resonant interconnecting network, as typical of class E^2 converters. Fig. 4.16 shows efficiency and output power as a function of R_{DC} when the output voltage is controlled through V_g to be 22, 17, and 12 V. FM modulation presents a viable alternative for open or closed loop output voltage control, however, performance of the converter degrades at higher loads and lower voltages.

4.4.3 Estimate of losses in the converter

The losses are estimated from simulations, since it is difficult to measure the separate sub-circuits at GHz frequencies. The simulations were performed for V_{DCin} = 28 V, V_{DCout}=25 V, a dc load of 24 Ω, and an operating frequency of 950 MHz. The converter is 80 % efficient and the losses are distributed as shown in Table 4.3.

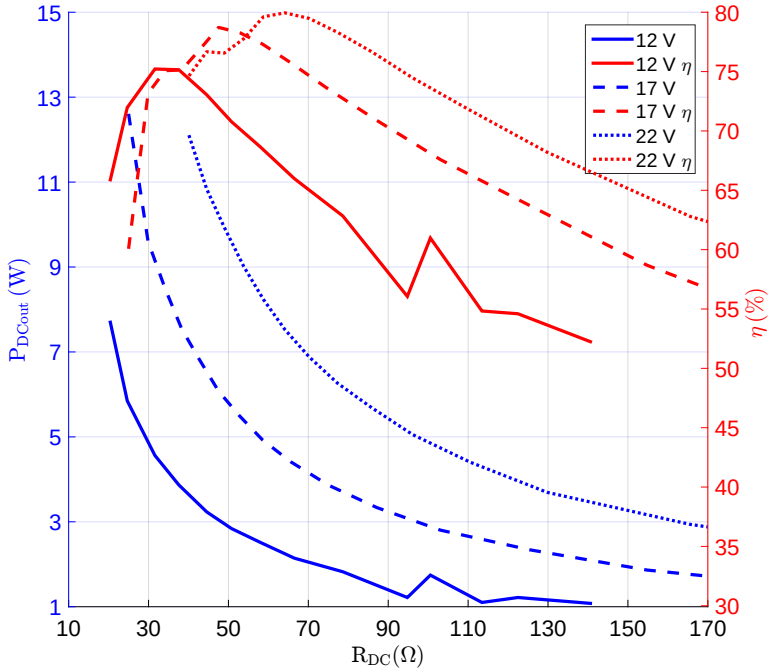


Figure 4.16: Measured performance of V_{out} control through V_{g1} for oscillating, self-synchronous converter. Input voltage is 28 V while output voltage is adjusted to 12, 17 and 22 V.

The biggest contributor to the dissipated power is the transistor's R_{ON} resistance for both the PA and the rectifier. Most of the losses in the passive elements come from power dissipated in the inductors which seems to agree with the losses estimated for the 1.2 GHz converter. The OFF-ON and ON-OFF transitions contributed to 31 % of the total losses, which explains most of the losses not accounted for in the loss budget of the 1.2 GHz converter.

Table 4.3: Estimated losses based on simulation

Total inverter transistor losses	49.0 %
OFF-ON tranistion	9.4 %
ON-OFF transition	10.4 %
Conduction losses	29.2 %
Total rectifier transistor losses	39.7 %
OFF-ON transition	11.3 %
ON-OFF transition	0.8 %
Conduction losses	27.6 %
Total passive components losses	8.4 %
Resonator	2.7 %
Inverter bias-T	3.1 %
Rectifier bias-T	2.6 %
Other losses	3.8 %

4.5 Conclusion

In this chapter two class-E^2 dc-dc converters operating at a switching frequency of 1 and 1.2 GHz are designed, analyzed and characterized. The converters achieve 80 % and 75 % dc-dc efficiency respectively and are among the highest-frequency and highest-efficiency reported in the literature. The application of the concepts established in the analysis of a self-synchronous rectifier to a power amplifier, culminated in the development of an oscillating, self-synchronous class-E^2 dc-dc converter.

Contributions of this chapter include:

- Design and characterization of a 1.2 GHz GaN class-E^2 dc-dc converter.
- Demonstration of a flat 1.2 GHz GaN class-E^2 dc-dc converter with a self-synchronous rectifier.
- A theoretical analysis of a class-E oscillator and a theoretical approach to the design of a class-E oscillator.
- Demonstration of a 900 MHz oscillating, self-synchronous E^2 dc-dc converter with the collaboration of Prof. Jose Angel García and María de las Nieves Ruiz from the University of Cantabria, Spain.
- The work presented in this chapter was presented at the IEEE International Microwave Symposium

2015 [23] and is published in IEEE Transactions on Microwave Theory & Techniques in [24].

Chapter 5

Distributed class-E^2 DC-DC Converter Microwave Monolithic Integrated Circuit (MMIC)

Contents

5.1 Introduction

As described in Chapter 1, one of the main motivations for very high frequency converters in the GHz frequency range, is to enable a fully integrated power supply on a chip. The integration of the power supply

circuitry and the control logic circuitry, or the integration of the power supply and the power amplifier in the same chip, can significantly reduce the size and cost, and improve manufacturability of electronic systems and wireless devices [96].

When integrating dc-dc converters, the biggest challenge is the integration of the magnetic components. Successful demonstrations of monolithic integrated dc-dc converters have had to rely on off-chip inductors as in [75] or are mainly focused on low voltages and low power. In [97], a 200-MHz integrated buck converter with resonant gate drivers is demonstrated. The converter is implemented in a 0.25-μ BiCMOS process and it uses an input voltage of 3.6 V. The converter achieves a maximum efficiency of 77 % and an output current of 329 mA at 2.2 V. The design uses two 8 nH air-gap, resonant inductors. In [98], a fully monolithic cellular buck converter is shown, the converter is designed for 3-D power delivery for future microprocessors [99–102] and is implemented in a 0.18-mm SiGe BiCMOS process with an input voltage of 1.8 V, and an output voltage of 0.9 V with a nominal output current of 500 mA. The converter operates with a switching frequency of 200 MHz and it achieves a maximum efficiency of 64 % for an output power of 0.45 W. A 2.14-nH air-core spiral inductor with 25 μm wide tracks is used as the on-chip filter inductor. The majority of the losses in that design can be attributed to the ON resistance of the transistors used as switches and the dc resistance of the inductor. The ON resistance of the control switch and the switch of the synchronous rectifier are estimated to be 152 mΩ, and 62 mΩ respectively, while the dc resistance of the inductor is estimated to be 201 mΩ. In [103], a different approach to a fully integrated on-chip converter is presented. A software controllable integrated dc-dc downconversion power management system that combines switched-capacitor voltage dividers and linear regulators is proposed to regulate 2.5 V down to 0.65 V at 6.5 mW.

In this chapter the feasibility of a resonant converter consisting of only distributed passive components is investigated. A completely distributed class-E^2 dc-dc converter is designed in Qorvo's 0.15 μm GaN on SiC process as a proof-of-concept demonstration of a fully monolithic integrated dc-dc converter.

Section 5.2 shows a detailed description of the design of the MMIC. Because of the distributed nature of the design, the drain bias-T of the PA and the rectifier make termination of the second and the third harmonic in an open circuit difficult, hence priority is given to the second harmonic. Furthermore, the two

bias-Ts are incorporated into the design of the matching network. In Section 5.3 the distributed converter is measured with the rectifier driven synchronously and in Section 5.4 a manual external tuner is used to operate the rectifier self-synchronously. Finally, Section 5.5 addresses losses in the converter and efficiency improvements.

5.2 Design of integrated converter

The design of the converter is based on the same class-E^2 topology presented in Chapter 4, which is a PA (inverter) reactively coupled to a synchronous rectifier. The typical characteristics of the 0.15 μm GaN on SiC process from Qorvo are I_{max}=1.15 A/mm, $g_{m,max}$= 380mS/mm, and 3.5 V pinch-off at V_{ds}=10 V. The breakdown voltage exceeds 50 V at I_{gd}=1 mA/mm. The size of the transistors for both inverter and rectifier is 100 μm in gate width, with twelve gate fingers each, which is the largest single transistor with an available non-linear model. A non-linear Angelov model developed by Modelithics is used to extract the output capacitance of the transistors. The intrinsic capacitances are estimated to be C_{gs}=1.4 pF, C_{ds}=0.36 pF, and C_{gd}=0.09 pF.

The switching frequency has to be high enough for the distributed circuit to fit in a 2.5 mm × 3.8 mm die size but low enough to approximate class-E waveforms at the intrinsic drain of the transistor. The guided wavelength λ_g at 1 GHz is equal to 96 mm in GaN, the length of a λ/4 bias-T would be around 24 mm which is too big to fit in the space available. Based on a die size of 2.5 mm × 3.8 mm and a breakdown voltage of 50 V at I_{gd}=1 mA/mm, an initial switching frequency range between 4-5 GHz is investigated. At 4 GHz λ_g=24 mm which makes fitting the design of the required bias-Ts in the available space more feasible. The max voltage across the switching device according to well known class-E theory is $3.56V_{DC}$. Considering the specified breakdown voltage of ≈ 50 V, a dc input and output voltage of no more than 15 V should be the regular operating voltage. The simulated I-V curves of the 12x100μm transistor are shown in Fig. 5.1. The slope of the red line is used to estimate the ON resistance resulting in $R_{ON} \approx 2.5\,\Omega$.

Based on previous designs [104] using the same process and device size, the transistor can be expected to draw a DC current of 400 mA at 15 V. As a starting point, following equation 4.2, the impedance required

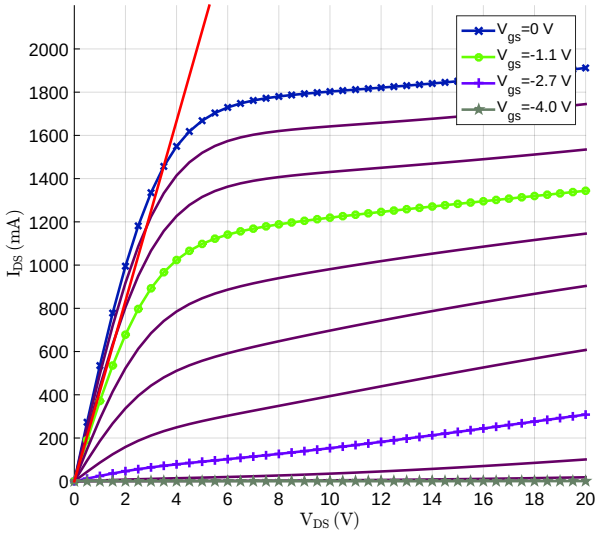


Figure 5.1: Simulated I-V curves for the 12x100 μm transistor device used in the design of the distributed converter. The red line is used to estimate R_{ON} when the transistor is fully ON.

for an ideal class-E PA is

$$Z_{net} = \frac{0.28015 e^{j49.0524^\circ}}{(2\pi 4.5\,\text{GHz})(0.36\,\text{pF})} = 18.03 + 20.8\,\Omega \tag{5.1}$$

therefore according to subsection 3.2.1, the inter-stage matching network should present an impedance of $Z_{net} = 18 + j41.6\,\Omega$ to the PA and the rectifier.

Because of the distributed nature of circuit, the bias-T makes the termination of 2nd and 3rd harmonic simultaneously in an open circuit very difficult. Priority is given to the termination of the 2nd harmonic, since the 2nd harmonic has the most influence on efficiency. Implementing the bias-T using a quarter wavelength line and a shunt capacitor to ground is not an option due to the size limitation (a quarter wavelength line on SiC would be approximately 5 mm at 4.5 GHz). A spiral inductor is a good alternative, however, the maximum width and length of an air bridge allowed in the process is 75 μm and 100 μm respectively. The max current density of the metal layers used in the under-pass is equal to 6.4 mA/mm. Hence the maximum current recommended for the underpass is 480 mA. As previously stated, at 15 V the PA is expected to draw approximately 400 mA. The current drawn by the PA can increase based on the input voltage and since the

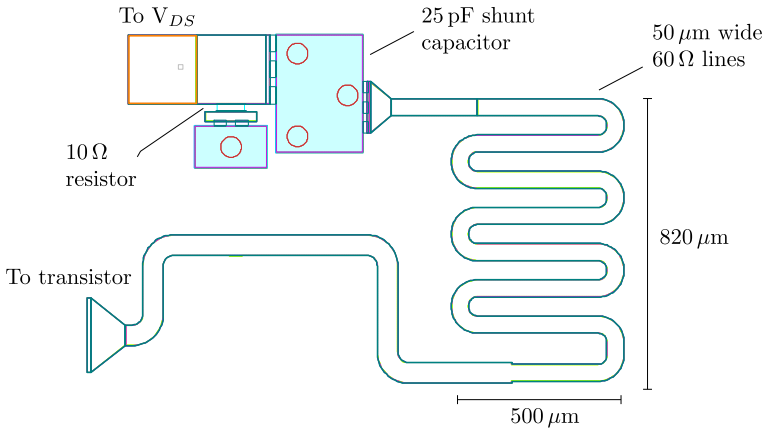


Figure 5.2: Layout of the output bias-T. Because the distributed nature of the circuit, the bias-T does not appear like an open circuit at the fundamental frequency and it becomes a matching element.

converter will be characterized at different input voltages, the use of a spiral inductor in the drain bias-T could result in currents higher than recommended. Therefore, the output bias-Ts avoid the use of air-bridges and spiral inductors, and become part of the output matching network.

Fig. 5.2 shows the layout of the output bias-T. The two bias networks at the output are implemented with a meandered 48 μm line and a 24 pF shunt capacitor to ground. Fig. 5.3 shows the frequency response of the bias-T. Rather than presenting an open circuit at the fundamental frequency f_0 and $2f_0$, the bias-T presents an inductive impedance that becomes part of the resonant network between the two transistors. The CLC resonator used in Chapter 4 is implemented by a meandered line and two 5.7 pF capacitors. Fig. 5.4 shows the layout of the resonator.

The input matching network consists of a meandered transmission line with a shunt 2.3 pF capacitor that matches the input of the transistor to 50 Ω. The input bias-T uses a spiral inductor and a 30 pF capacitor shunt to ground, the spiral inductor can be used without a problem in the input bias-T because the transistor is expected to draw very low DC current at the gate. The input matching network also includes a 3 Ω and a 4 Ω resistor for stability. Because the rectifier is not simulated, a proper stability analysis is not possible and ensuring $S_{11} < 0$ dB for the amplifier at all frequencies is used to estimate stability. Fig. 5.5 shows the layout of the input matching network.

In order to finalize the design, an optimizer simulation with a setup shown in Fig. 5.6 is performed. As

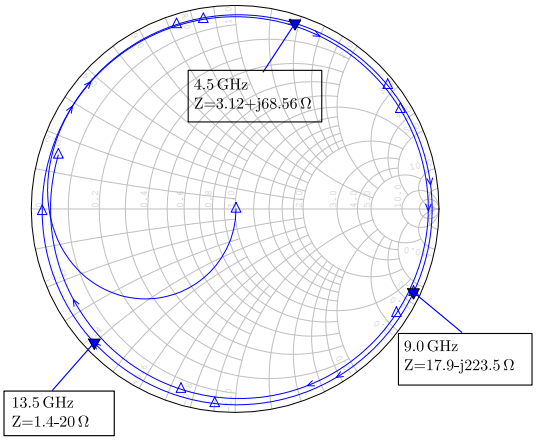


Figure 5.3: Frequency response of EM simulated Bias-T from DC to 30 GHz. The bias-T does not look like an open circuit at f_0 and becomes part of the output matching network.

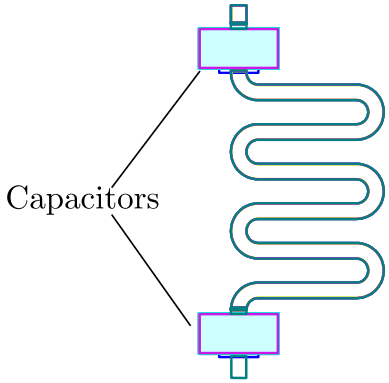


Figure 5.4: Layout of CLC resonator used between the two transistors of a distributed class-E^2 converter. The two capacitors are 5.7 pF, given process variation.

previously described, the majority of non-linear transistor models do not accurately model the third quadrant region where a GaN HEMT rectifier operates. For that reason, the transistor used as the switching element of the rectifier, is substituted by a simple resistive load equivalent to the load the rectifier presents to the PA under ideal operation as shown in subsection 3.2.1. Although switching losses in the rectifier are ignored in this simulation, the optimization of the design with the goal of maximizing the efficiency of the PA can provide a good estimate of the efficiency and output power of the converter.

The simulation results of the optimization are shown in Fig. 5.7, the maximum DC-RF efficiency is 63 % with an RF power of 35 dBm delivered to the equivalent load of the rectifier. The maximum efficiency results

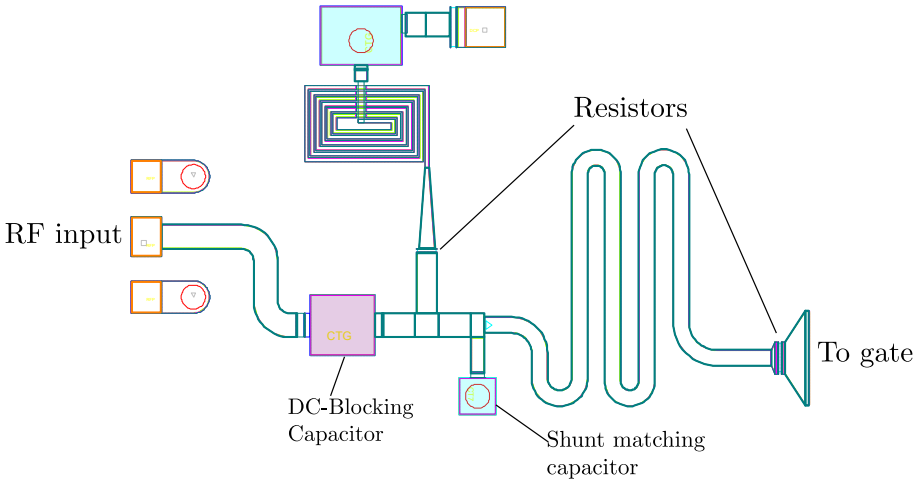


Figure 5.5: Layout of the input matching network.

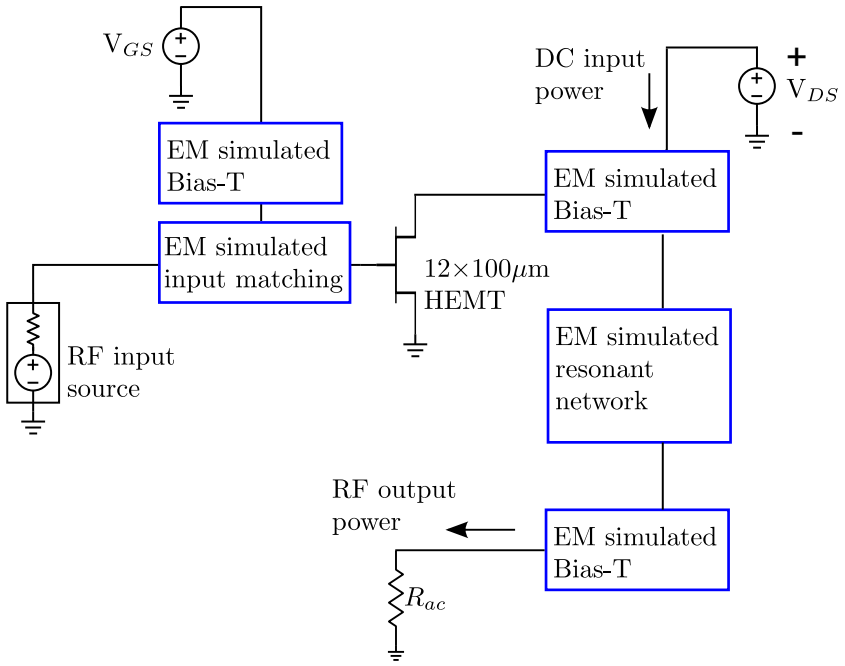


Figure 5.6: Setup used to optimize the design of the converter. The rectifier's switch is replaced by the equivalent resistor the class-E rectifier presents to the class-E inverter under ideal operation. The simulation is used to optimize the design for maximum DC-RF efficiency.

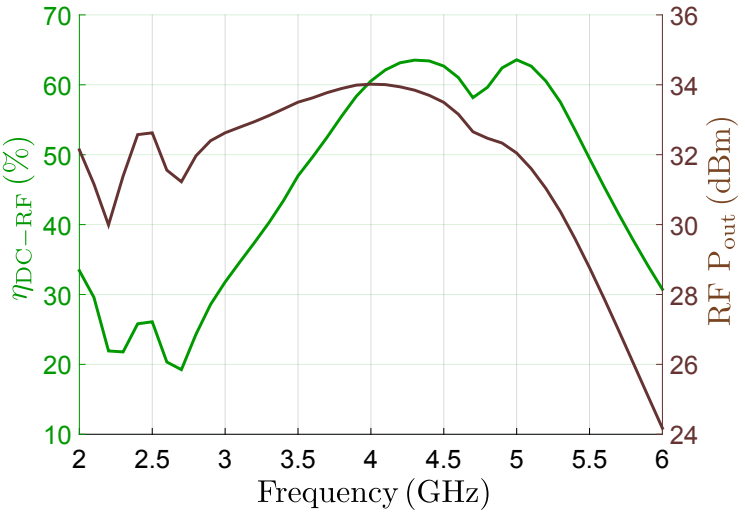


Figure 5.7: DC-RF efficiency and RF output power as a function of frequency after performing an optimization of the circuit shown in Fig. 5.6.

were obtained at a frequency around 4.5 GHz with an input DC voltage of 15 V and a RF power of 22 dBm. The impedance presented to the, PA and rectifier transistors by the final output matching network is plotted in Fig. 5.8 as a function of frequency. The impedance at the fundamental frequency after optimizing the circuit for efficiency resulted in 23.5+j39.9 Ω, while the second harmonic was terminated at an impedance equal to 49.2-j0.8 Ω. Both impedances are in accordance with the initial design estimates within 15 %.

A microscope photograph of the distributed class-E^2 converter is presented in Fig. 5.9.

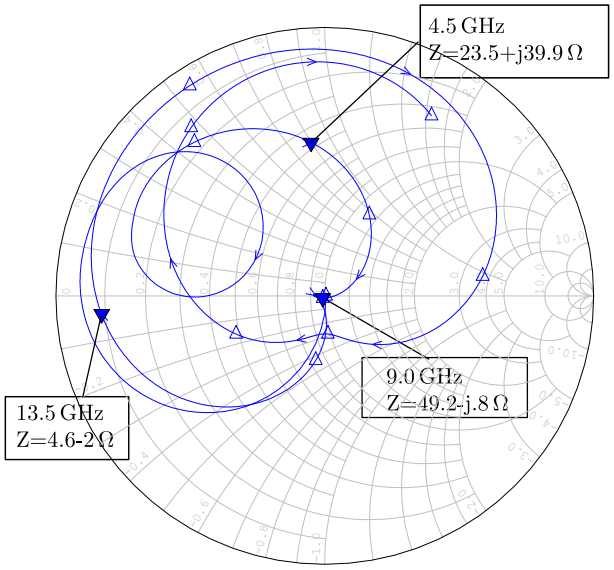


Figure 5.8: Frequency response of the EM simulated output-matching network after optimizing the entire design for maximum PA efficiency.

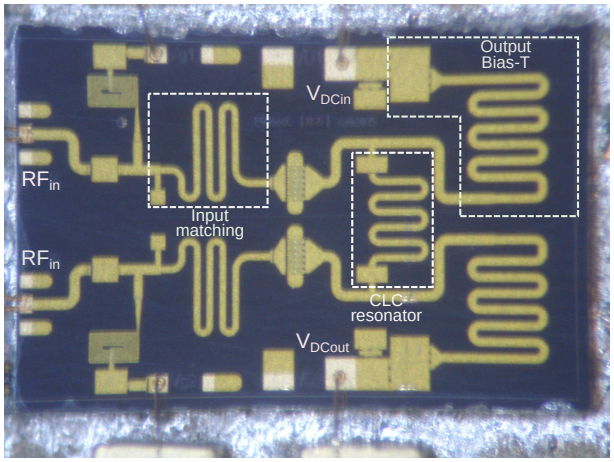


Figure 5.9: Photograph of the monolithically integrated class-E^2 DC-DC converter. The total area of the die is 2.5 mm × 3.8 mm.

5.3 Measurements with synchronous rectifier

The die from Fig. 5.9 is soldered to a 40-mil thick CuMo carrier plate. The RF inputs for both the power amplifier and the rectifier are connected to 50-Ω lines on an alumina substrate and bonded with two 1-mil gold bond wires each. The carrier plate is then inserted into an aluminum fixture that also serves as a heat sink for the circuit. The 50-Ω launchers that make contact with the lines are shown in Fig. 5.10. The DC gate and drain pads are connected with bondwires to a shunt 1000 pF capacitor, which is in turn connected through a bondwire to external DC pads.

The converter is characterized using the setup shown in Fig. 5.11. The PA is biased at different quiescent currents for input voltages ranging from 5-20 V. The rectifier is biased at pinched-off with V_{gs}= -4.0 V. The DC load used for testing is a BK Precision 8500 electronic DC load in constant voltage mode. The output voltage is set by the electronic load and swept from 1-15 V. All the measurements are performed with an RF input power of P_{in}= 22 dBm for both the PA and the rectifier. The phase of the signal driving the rectifier gate is adjusted until synchronous operation is achieved. Fig. 5.12 shows a summary of the performance of the converter. Output power and efficiency are plotted as a function of output voltage for different input voltages. The operation of the converter is very similar to the converter shown in Chapter 4, the output power is proportional to input voltage as expected. Highest efficiency is achieved at lower input voltages

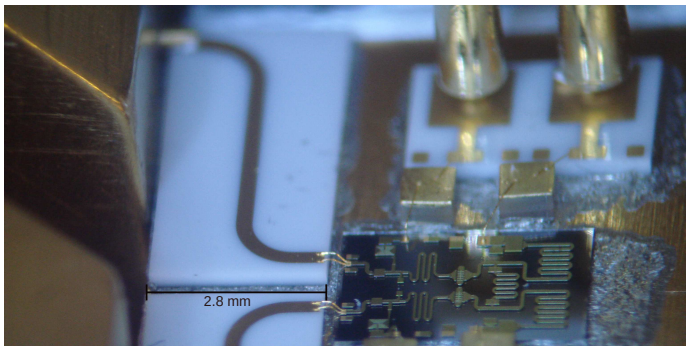


Figure 5.10: Photograph of the fixture used to measure the class-E^2 MMIC. The two RF inputs are connected to the alumina lines via two bondwires. The center pin of the launchers is settled on the alumina line. The gate and drain DC pads are connected to a 1000 pF capacitor shunt to ground and then connected to DC pads for external pins (two cylinder on top) to make contact with.

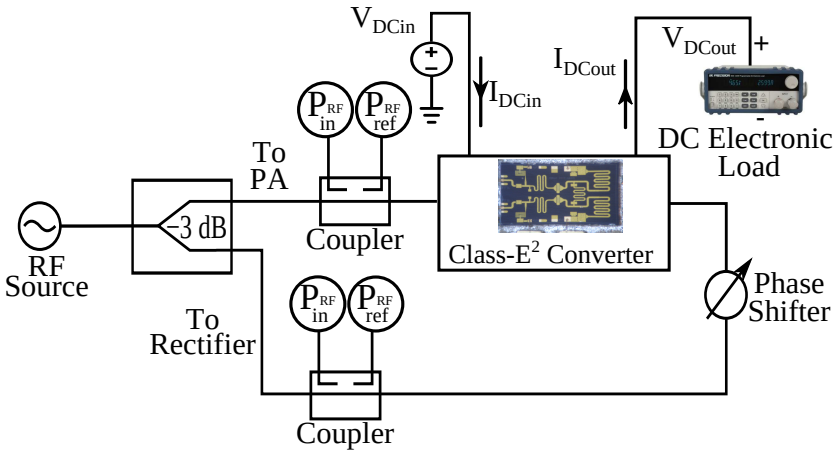


Figure 5.11: Setup used to characterize the monolithic integrated class-E^2 converter. The RF source is split in two signals, one is driving the PA and the other one drives the rectifier. The incident and reflected power of the driving signal is measured using two couplers. The phase of the signal driving the rectifier is adjusted for synchronous operation. The output voltage is enforced by the electronic load.

with a maximum total dc-dc efficiency of 48 % at an output power of 0.68 W. The maximum rectified power is 1.3 W for an input voltage of 18 V. The efficiency of the converter plotted in Fig. 5.12 is defined as

$$\eta_{DC} = \frac{V_{DCout} I_{DCout}}{V_{DCin} I_{DCin}} \tag{5.2}$$

The maximum efficiency is significantly lower than the DC-RF efficiency simulated in Fig. 5.7. The decrease in efficiency is attributed to the switching losses of the rectifier which could not be taken into account in the simulation due to lack of model. The simulated maximum RF output power delivered to the rectifier's equivalent load in Fig. 5.7 at an input voltage of 15 V is approximately 33 dBm or 2.0 W at 4.5 GHz. The maximum measured DC output power at an input voltage of 13 V is equal to 1.3 W which suggests the rectifier is approximately 65 % efficient.

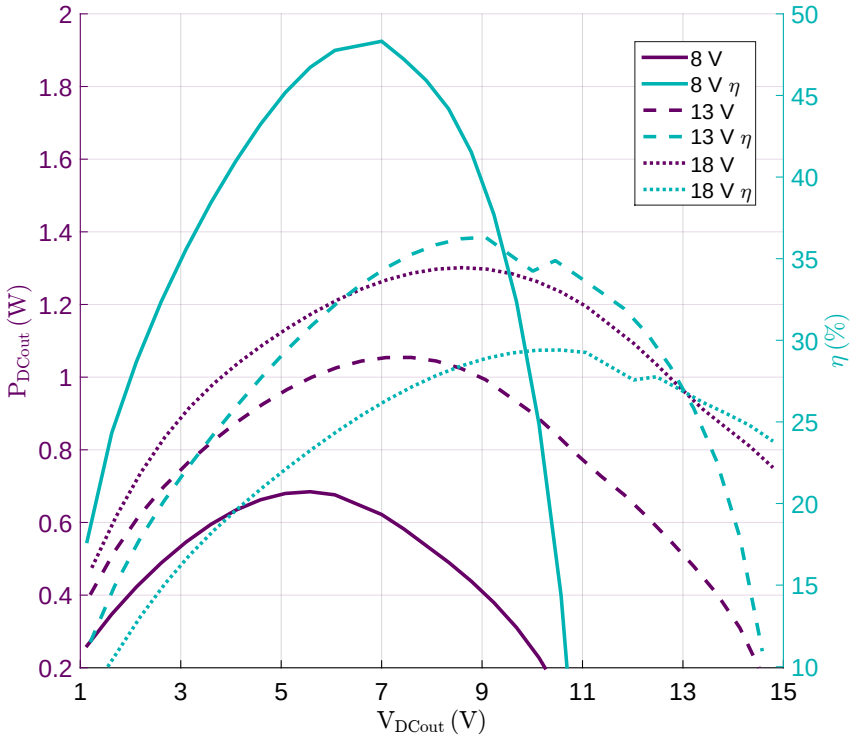


Figure 5.12: Measured results of the integrated converter. Efficiency (cyan) is shown in the right y-axis and output power (purple) is shown in the left y-axis; both are plotted at 4.5 GHz as a function of output voltage for an input voltage of 8, 13 and 18 V.

5.4 Measurements with self-synchronous operation

Having characterized the distributed converter by driving the PA and the rectifier synchronously, following the analysis from Chapter 3, the rectifier should be able to operate self-synchronously if an equivalent inductive impedance less than

$$L_g = \frac{1}{(C_{gs} + C_{gd})\omega_s^2} = \frac{1}{(1.4\,\text{pF} + .088\,\text{pF})(2\pi 4.6\,\text{GHz})^2} = 0.8\,\text{nH} \tag{5.3}$$

is presented to the input of the transistor. However, due to matching to a 50 Ω connector, the alumina lines and the launchers used in the measurement of the MMIC converter, the impedances that can be presented to the transistor are limited to a small area on the Smith chart. Fig. 5.13 shows a simulation of the transformation of the impedances presented by an ideal tuner to the impedances presented to the gate of the transistor. A

load pull is performed at the gate port of the rectifier using a manual tuner to attempt to operate the converter running the rectifier self-synchronously.

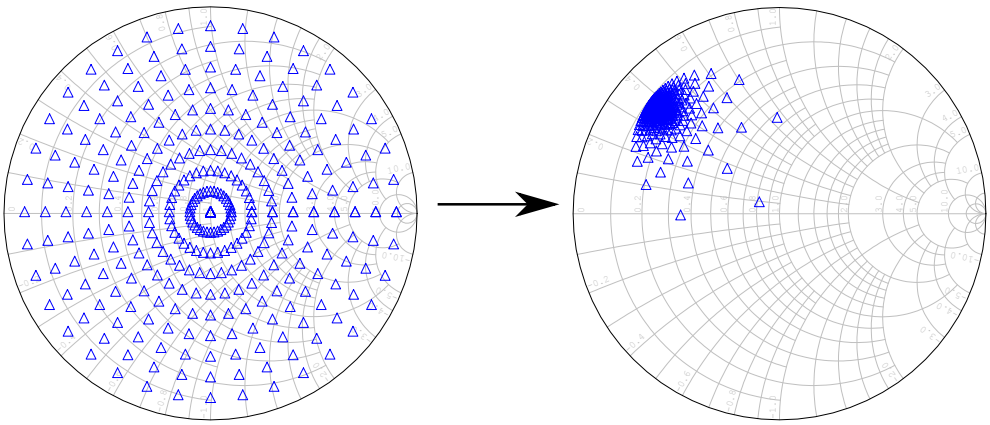


Figure 5.13: Simulation of the transformation of the impedances presented by an ideal tuner to the impedances presented to the gate of the transistor after the launchers, alumina-lines, wire bonds, and input matching network of the MMIC. The results are shown at 4.5 GHz.

Fig. 5.14 shows the measured results of the converter without a drive signal at the rectifier gate and with only a passive tuner connected to the RF input port of the rectifier. The performance of the converter running self-synchronously undergoes a drop in both efficiency and output power. The performance degradation is likely due to the inability to reach the optimal value of the equivalent inductance from equation (5.3) externally. This is further supported by the inability to make the PA oscillate as the oscillating, self-synchronous converter in Section 4.4.

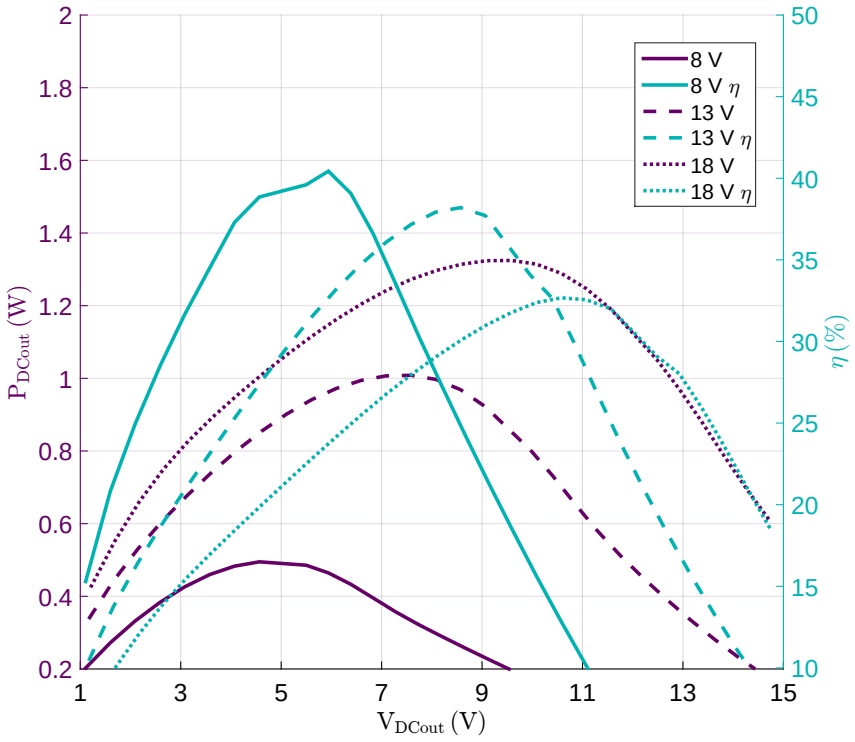


Figure 5.14: Measured output power and efficiency of the integrated converter with the rectifier running self-synchronously. Efficiency (cyan) is shown in the right y-axis and output power (purple) is shown in the left y-axis; both are plotted as a function of output voltage for input voltages of 8, 13 and 18 V.

5.5 Losses estimate and efficiency improvement

The DC-RF efficiency and output power of the distributed converter have to be increased to make a distributed converter practical. The simulated PAE of 63 % does not include switching losses in the rectifier and that is one of the reason why the measured efficiency is much lower. The power loss in the inter-stage matching network can be estimated by simulating the insertion loss in the network. Fig. 5.15 shows the simulated loss in the network between the PA and the rectifier using full-wave EM analysis. The loss is approximately 0.5 dB at 4.5 GHz or a 10 % loss. The rest of the losses in the circuit are mainly switching losses in the transistor.

To project the maximum efficiency possible with the HEMT used in the design, an ideal load-pull

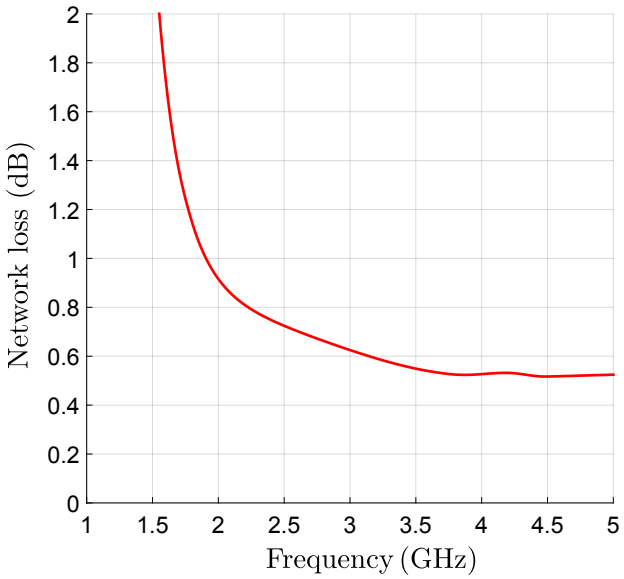


Figure 5.15: EM simulated loss in the network of the distributed converter.

simulation at f_0, $2f_0$ and $3f_0$ is performed with $f_0 = 4.5\,\text{GHz}$. The transistor is biased in the same way as in the simulations shown in Fig. 5.7. Fig. 5.16 shows the results of the simulation. The maximum efficiency achieved is 75 %. Therefore one can expect the maximum efficiency of the class-E PA and rectifier to be approximately 75 % with a total converter efficiency of 56 % at 4.5 GHz. Considering the 10 % loss in the network, the PA is operating close to the maximum efficiency point possible with only two harmonics. Hence, there is little room for design improvement with a similar topology at 4.5 GHz.

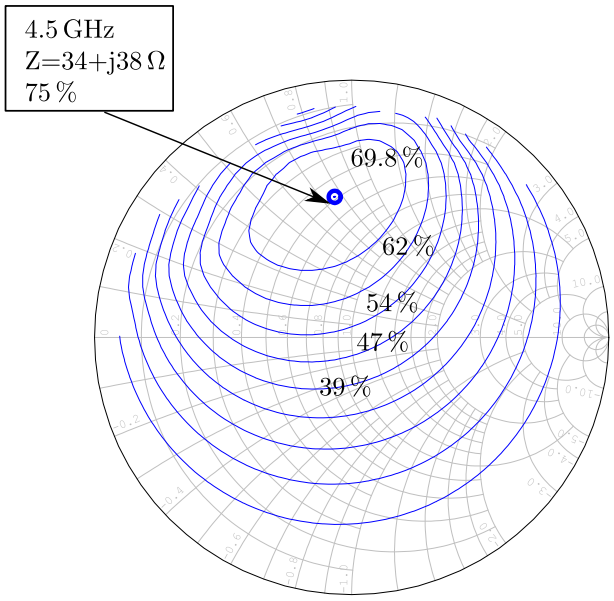


Figure 5.16: Results of ideal losless load-pull simulation of the $12 \times 100\ \mu$m HEMT used in the design. The simulation is performed at 4.5 GHz with the 2^{nd} and 3^{rd} harmonic optimized for efficiency. The maximum efficiency obtained is 75 %.

5.6 Conclusion

A proof-of-concept fully integrated GaN MMIC dc-dc converter switching at 4.6 GHz is demonstrated for the first time to the best of our knowledge. The circuit uses two GaN HEMTs, one for the inverter (PA) and one for a synchronous rectifier. The 3.8 mm $\times$ 2.6 mm chip has two RF 50-Ω inputs, a dc input and a dc output, and does not require any external elements. By connecting an external RF tuner to the rectifier gate input, it is demonstrated that the converter can also operate in self-synchronous mode with a single RF input, but with lower efficiency. The efficiency can be increased in this mode of operation by including the appropriate impedance in the rectifier gate on-chip. The maximum end-to-end efficiency is 48 % and can be increased in this particular process by lowering the frequency of operation. It should be noted that the nonlinear device models do not accurately (or at all) predict device behavior for the dynamic load line in the 3rd quadrant of the IV characteristics, making the design only an approximate process since only the inverter (PA) can be simulated.

Contributions of this chapter include:

- The design and characterization of an integrated distributed class-E^2 dc-dc converter switching at 4.6 GHz with a maximum dc-dc efficiency of 48 % at an output power of 0.5 W and a maximum output power of 1.3 W at a dc-dc efficiency of 30 %. All the inductors in the converter are implemented by transmission lines.

- The demonstration of a proof-of-concept of the 4.6 GHz class-E^2 dc-dc converter operating with a self-synchronous rectifier. Terminating the gate of the rectifier and the amplifier on-chip can lead to an integrated distributed class-E^2 dc-dc converter with only dc inputs.

- The work is reported in [25] at the IEEE International Microwave Symposium 2016.

Chapter 6

Near-field Capacitive Wireless Power Transfer Array For Electric Vehicles

Contents

6.1 Introduction

The concepts from previous chapters are applied to wireless power transfer (WPT), where the coupling between the PA and the rectifier is accomplished through electric and magnetic near-fields. Near-field wireless power transfer has been most commonly done using inductive coupling at lower frequencies (100 KHz-13 MHz). The applications range from sub-watt implants to electric vehicles and industrial machinery. In this chapter, an array approach to capacitive WPT aimed at a modular and scalable system for charging electric vehicles is presented.

Despite the progress in development of electric vehicles over the past decade, their penetration remains under 0.1 % and this is mainly due to high cost, limited range, and long charging times. Limited range and long charging times can both be traced to limitations in battery technology. One way to mitigate both problems is to reduce the on-board energy storage and deliver power wirelessly to the car. Inductive wireless power transfer (WPT) has been the main focus of research, and the majority of high-power WPT systems currently operating are inductive [105]. However, inductive powering is limited by the requirement of expensive and heavy ferrites required for cores and for external field reduction [106]. State-of-the-art inductive WPT systems achieve power densities of up to 27 kW/m^2 and efficiencies of approximately 80 % [107].

On the other hand, limited work has been done in capacitive power transfer, mostly at lower power levels and short distances, e.g. [105], [108], [109]. In [110], a capacitive wireless transfer system through the wheels of a vehicle is proposed. The system achieved a maximum power transfer of 50 W at approximately 50 MHz. In [111], a high power density of 1.1 W/mm^2 is achieved at 2.6 W by WPT at 100 MHz across a 1-pF capacitance. Recently in [112], a 2.4-kW prototype was demonstrated with four 61×61-cm copper plates. The system achieves 90 % efficiency at 1 MHz and an air gap distance of 15 cm. The work in this chapter builds upon the idea presented in [113], where a new capacitive WPT approach for large air-gap applications is introduced. The goal of the distributed array approach is to increase maximum transferable power while decreasing the external electric field produced by the WPT system, accomplished by field focusing through phase control.

Section 6.2 Explains the general architecture of the CWPT, in which multiple conducting plates located at the bottom of the vehicle couple capacitively to multiple plates located on the road. The full-bridge inverter and rectifier are designed by Prof. Kurram Afridi and the power electronics group at the University of Colorado at Boulder. In Section 6.3 a preliminary full-wave simulation study of the focusing effects at different frequencies and for several array configurations and relative phasing between the modules is shown. The primary frequencies of interest are the 6.78, 13.56 and 27.12 MHz bands.

6.2 Design and description of capacitive WPT system

The WPTC system is intended to power vehicles through plates located on the road and on board of the vehicle as shown in Fig. 6.1. However, due to the large air-gap between the plates, the idealized approach to model electric fields between two parallel plates is not applicable because significant fringing fields exists around the plates. In [113], the maximum power transfer capability of a capacitive WPT module is derived by relating it to the fringing field strength generated by each pair of plates. The maximum electric field strength under the electro-quasistatic approximation assuming the plates are much smaller than the wavelength and the plates are separated enough so the fields of one plate do not interact with the fields generated by the other is given by

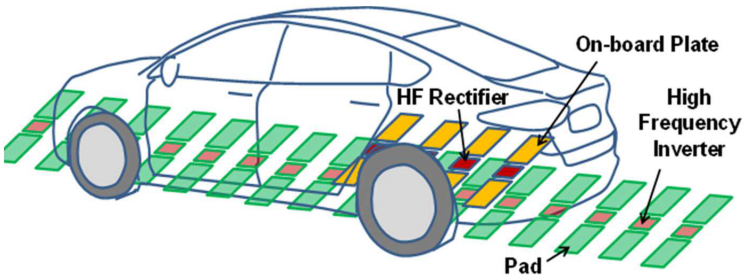


Figure 6.1: Diagram of the proposed capacitive wireless power system.

$$E_{max} = \frac{CV_{C,max}}{\pi\epsilon_0 A}\left(\tan^{-1}\frac{2w(r+l)}{d\sqrt{d^2+w^2+4(r+l)^2}} - \tan^{-1}\frac{2wr}{d\sqrt{d^2+w^2+4r^2}}\right)$$
$$= \frac{CV_{C,max}}{\pi\epsilon_0 A}\frac{1}{\mathcal{F}_{dim}} \tag{6.1}$$

C refers to the effective capacitance of each pair of plates, A is the area of each plate, l and w are the length and width of the plates, d is the length of the air-gap, r is the distance for the edge of the plates where the fringing fields are measured, $V_{C,max}$ is the peak voltage across the plates during power transfer, and $\mathcal{F}_{dim}$ is defined as the reciprocal of the expression inside the parenthesis in equation 6.1. The maximum power transfer capability is then given by

$$P_{max} = \pi\sqrt{2K_{rec}}G_2 V_{out} C V_{C,max} f_s \tag{6.2}$$

where f_s is the switching frequency of the inverter, K_{rec} is the resistance transformation ratio of the rectifier (=$8/\pi^2$ for a full-bridge rectifier), G_2 is the current provided by the matching network on the secondary side, C is the effective capacitance of each pair of plates, and V_{out} is the dc output voltage of a single module.

From 6.1 and 6.2, the maximum power transfer density of the CWPT can be related to the restrains imposed in the system by electric field safety regulations as:

$$\Pi_{max} = \frac{P_{max}}{2A} = \pi^2 \epsilon_0 \sqrt{\frac{K_{rec}}{2}} G_2 V_{out} \mathcal{F}_{dim} f_s E_{max} \tag{6.3}$$

The maximum levels for general public exposure to time-varying electric and magnetic fields according to the International Commission on Non-Ionizing Radiation Protection (ICNIRP) are given in Fig. 6.2. The maximum E-field strength for the frequencies of interest is $87/f^{1/2}$V-m^{-1} for 1-10 MHz and 28 V-m^{-1} for 10-400 MHz.

Frequency range	E-field strength (V m^{-1})	H-field strength (A m^{-1})	B-field (μT)	Equivalent plane wave power density S_{eq} (W m^{-2})
up to 1 Hz	—	3.2×10^4	4×10^4	—
1–8 Hz	10,000	$3.2 \times 10^4/f^2$	$4 \times 10^4/f^2$	—
8–25 Hz	10,000	$4{,}000/f$	$5{,}000/f$	—
0.025–0.8 kHz	$250/f$	$4/f$	$5/f$	—
0.8–3 kHz	$250/f$	5	6.25	—
3–150 kHz	87	5	6.25	—
0.15–1 MHz	87	$0.73/f$	$0.92/f$	—
1–10 MHz	$87/f^{1/2}$	$0.73/f$	$0.92/f$	—
10–400 MHz	28	0.073	0.092	2
400–2,000 MHz	$1.375f^{1/2}$	$0.0037f^{1/2}$	$0.0046f^{1/2}$	$f/200$
2–300 GHz	61	0.16	0.20	10

[a] Note:
1. f as indicated in the frequency range column.
2. Provided that basic restrictions are met and adverse indirect effects can be excluded, field strength values can be exceeded.
3. For frequencies between 100 kHz and 10 GHz, S_{eq}, E^2, H^2, and B^2 are to averaged over any 6-min period.
4. For peak values at frequencies up to 100 kHz see Table 4, note 3.
5. For peak values at frequencies exceeding 100 kHz see Figs. 1 and 2. Between 100 kHz and 10 MHz, peak values for the field strengths are obtained by interpolation from the 1.5-fold peak at 100 kHz to the 32-fold peak at 10 MHz. For frequencies exceeding 10 MHz it is suggested that the peak equivalent plane wave power density, as averaged over the pulse width does not exceed 1,000 times the S_{eq} restrictions, or that the field strength does not exceed 32 times the field strength exposure levels given in the table.
6. For frequencies exceeding 10 GHz, S_{eq}, E^2, H^2, and B^2 are to be averaged over any $68/f^{1.05}$-min period (f in GHz).
7. No E-field value is provided for frequencies <1 Hz, which are effectively static electric fields. perception of surface electric charges will not occur at field strengths less than 25 kVm^{-1} . Spark discharges causing stress or annoyance should be avoided.

Figure 6.2: Reference levels for general public exposure to time-varying electric and magnetic fields according to ICNIRP [6]

For example, the maximum achievable power transfer density for a single module with 2.5 cm × 5 cm plates, a current gain G_2=10, a full bridge rectifier (Krec=$8/\pi^2$), a gap between the plates of 12 cm and the maximum E-field according to Fig. 6.2 measured 25 cm from the plates is plotted in Fig. 6.3 as a function of frequency. The maximum power transfer at 6.48 MHz is 16 kW/m^2 and it can be even higher at higher frequencies, this highlights the opportunity for a capacitive wireless power transfer system if the fringing fields can be kept below hazardous levels.

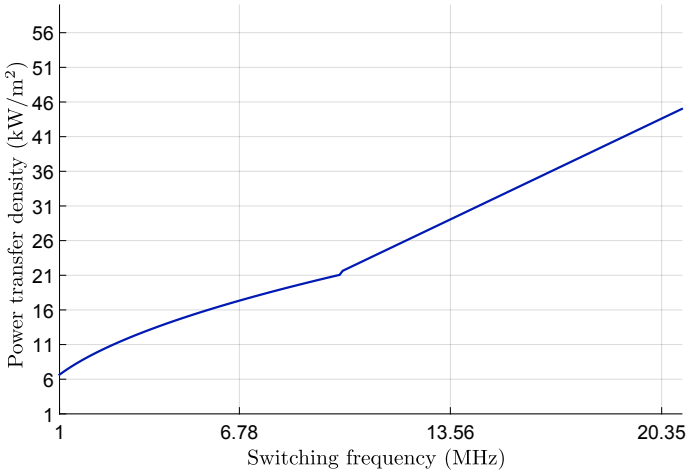
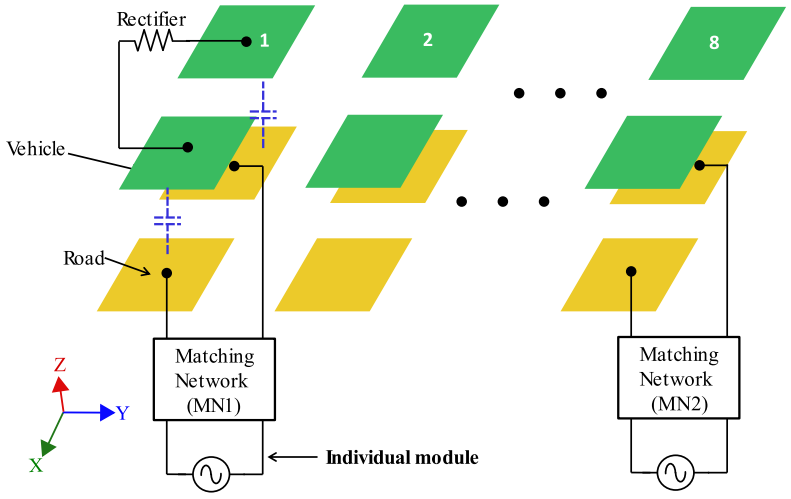


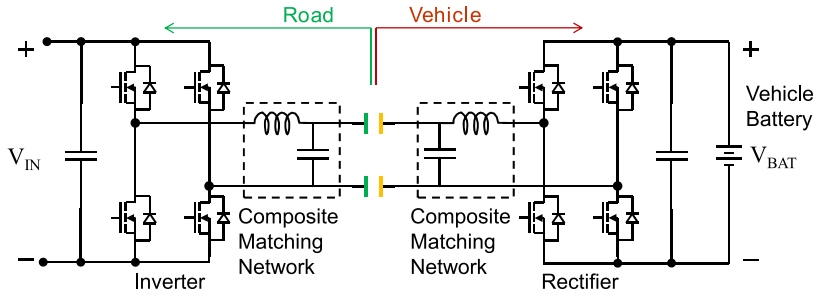
Figure 6.3: Maximum achievable power transfer density for a single module with 2.5 cm×5 cm plates, a current gain G_2=10, a full bridge rectifier (Krec=$8/\pi^2$), a gap between the plates d=12 cm and the maximum E-field according to Fig. 6.2 measured 25 cm from the plates

A simplified block diagram of the proposed system is shown in Fig. 6.4 (a). The capacitive WPT system consists of multiple conducting plates located at the bottom of the vehicle that couple capacitively with multiple plates located on the road. The architecture of the system is modular, with a single module defined as two road-plates powered by a high-frequency resonant inverter, and an identical pair of plates on the bottom of the vehicle, with a high-frequency rectifier connected between the plates, closing the loop with the plates to the ground.

An equivalent simplified circuit is shown in Fig. 6.4 (b). Both the inverter and the rectifier are implemented using a full-bridge architecture designed by Prof. Khurram Afridi and PhD student Brandon Regensburger from the power electronics group at the University of Colorado at Boulder. Initially, the distance between the plates is set to 12 cm. In order to be able to effectively transfer power through the



(a)



(b)

Figure 6.4: (a) Block diagram of the capacitive array wireless power transfer system for a stationary vehicle. N pairs of plates are placed in the road, with inverters (dc-ac converters) connected between each pair. N identical pairs of plates are placed on the bottom of the vehicle, with rectifiers connected between the plates, closing the current loop with the plates in the ground. (b) Equivalent circuit of an individual WPT module, consisting of 4 plates, a resonant inverter and a rectifier.

small equivalent capacitance without the use of very high voltages, the operating frequency has to be very high. The operating frequency is determined by the required power transfer through the small equivalent capacitance with a limited voltage level. Three different industrial, scientific, and medical (ISM) frequencies are considered in the initial design of the prototype: 6.78, 13.56 and 27.12 MHz. In a single plate-pair capacitive system, the maximum allowable power transfer density is limited by the fringing electric fields, which need to remain below the safety limits for human exposure to electromagnetic fields [6, 114]. The modular approach proposed here can substantially reduce the fringing electric fields by focusing the electric

field through a near-field phase array. The phase of each inverter is adjusted accordingly, to achieve field cancellation in the area of interest.

A simplified full-wave electromagnetic model of the capacitive system is created and simulated using Ansys HFSS in order to determine the optimum parameters for electric field cancellation. HFSS is used because the parasitic capacitances between the plates have to be accurately modeled and although the dimensions of the plates are very small compared to the wavelength, a electrostatic solver such as ANSYS Maxwell neglects the displacement current term $\partial_t \vec{D}$ in Ampere's law which is necessary to calculate the capacitances. The next section explains in detail the model created as well as the results of the simulations.

6.3 Full wave electromagnetic model

The HFSS model created is shown in Fig. 6.5. Initially, the effect of the road and the the car is not considered and only the plates and lumped ports representing the inverters and rectifiers are simulated. The area of each plate depends on the total number of plates simulated for a fixed power level. Due to restrictions outlined in the project, the total area occupied by the plates on the car and on the road is limited to 200 cm^2. All the plates are modeled with a thickness of 1 Oz ($\approx$ 0.0347 mm). The distance between adjacent modules d_1 and the distance between positive (+) and negative (-) plates d_2, are adjusted to minimize fringing electric field while keeping a high power transfer efficiency. To better quantify and optimize the design, two main zones are defined, where the magnitude of the electric field is calculated. The two zones are highlighted in Fig. 6.5. The Energy-transfer zone is located 1 cm below the rectifier plates where the electric field is expected to be very high and is used as an estimate of the power transferred. The safety zone, on the other hand, is where the magnitude of the electric field needs to be below the safety exposure limit for humans and is located 25 cm in the x direction away from the vehicle The electric field is calculated along the y-axis, which is the orientation along the vehicle body. The inverters are modeled as lumped ports with an impedance of 121.8 kΩ, corresponding to inverter modules with an output voltage of 4010 V and and output power of 132 W. The rectifiers are modeled as lumped ports with and equivalent impedance of 2.6 kΩ, this is based on the estimated equivalent output impedance of the rectifier.

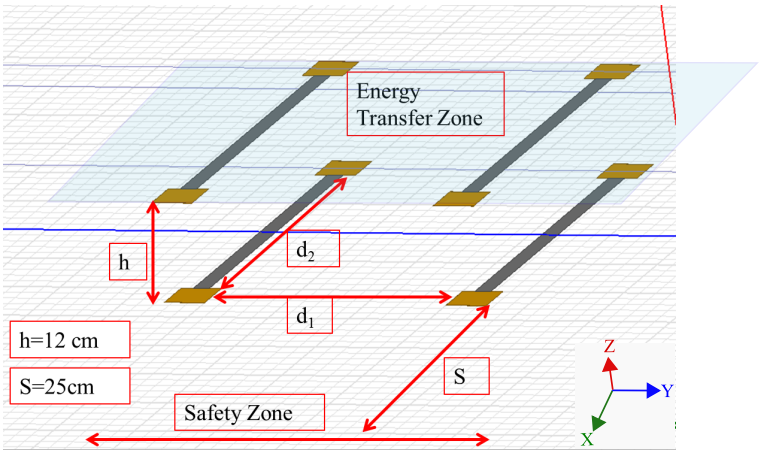


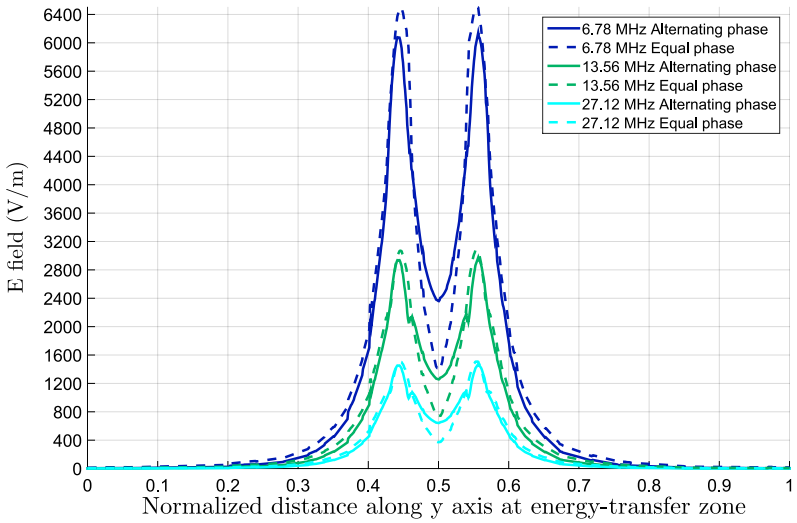
Figure 6.5: Depiction of zones where the magnitude of the electric field is calculated.

Simulations were performed with 2, 4, 5, and 8 modules, with d_1 held constant at 30 cm, and d_2 held constant at 40 cm. The area of the plates and the power of each inverter module is adjusted to achieve the maximum total area of 200 cm^2 and a total power of 1.12 kW. For example, the two-module simulation contains 4 plates with a 50 cm^2 area and two inverter ports with 560 W, and 28.7 kΩ impedance.

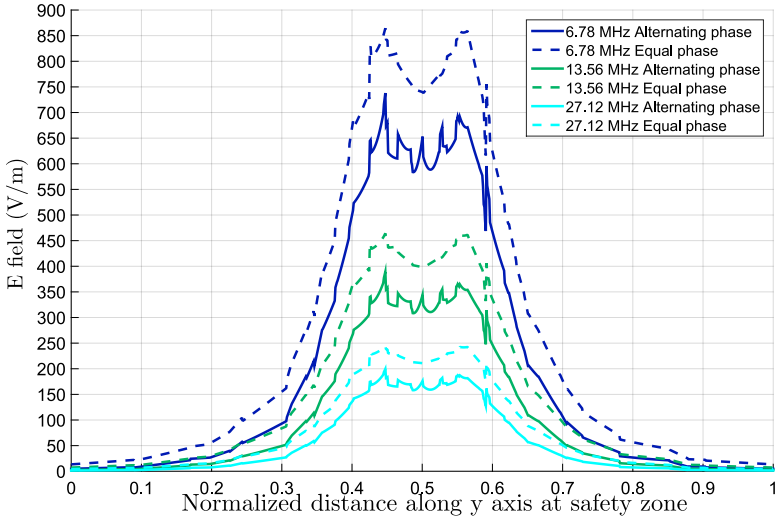
Fig. 6.6 shows the simulated magnitude of the electric field as a function of normalized distance in the energy-transfer zone (a) and in the safety zone (b) for the two-module case. The dashed lines correspond to the simulation results when the inverter modules are in phase, while the solid lines shows the results for the two modules 180° out of phase. It can be observed that the phase difference between the plates causes approximately a 17 % field reduction of the fringing field at the safety zone plane at 6.78 MHz. Higher frequencies also experience a reduction of the E-field, however the effect decreases with frequency for a constant $d_1 = 30$ cm.

The addition of more modules further reduces the fringing E-field in the safety zone plane. Fig. 6.7 and 6.8 show the simulated E-field for a 5-module and 8-module system respectively. The phase alternates 180° between adjacent modules. The field reduction in the safety zone with 8 modules is approximately 60 %. It is important to note that, as shown in Fig. 6.8 (a), the magnitude of the E-field in the energy-transfer zone also decreases with alternating phase between adjacent modules, which could impact the overall efficiency of the CWPT system and needs to be quantified.

In order to determine if the 180 ° alternating phase shift accomplishes the highest field cancellation, the



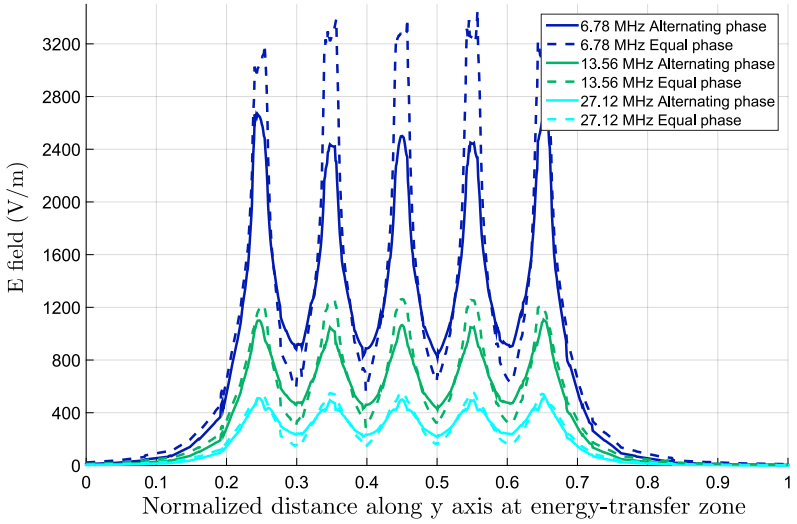
(a)



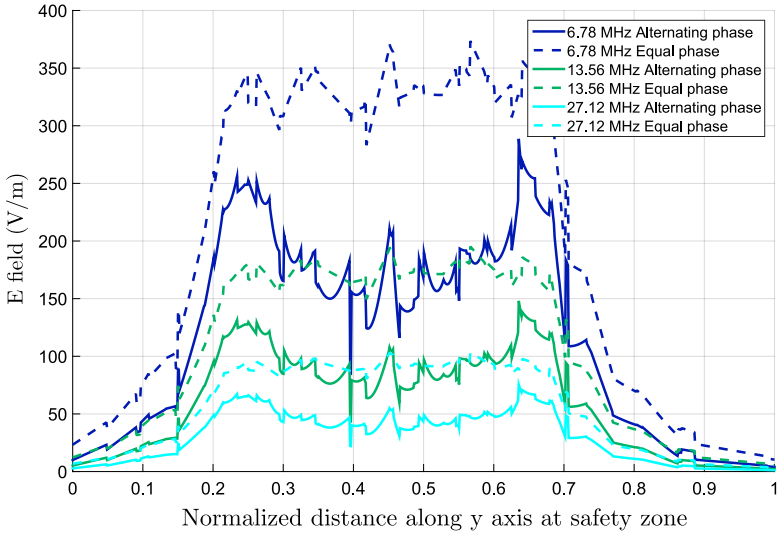
(b)

Figure 6.6: Magnitude of the electric field calculated at the plane of the safety zone for a two-module system at three ISM-band frequencies under consideration. Dashed lines show the E-field with inverter modules in phase, while the solid line shows the E-field with modules having alternating 180° phases.

8-module system is simulated with different alternating phases at 6.78 MHz. Fig. 6.9 shows the E-field as a function of normalized distance for alternating 0 °, 45 °, 90 °, 135 °, and 180 ° phases between adjacent modules. As expected, the magnitude of the E-field decreases in both the energy-transfer and safety zones as the phase difference between adjacent modules increases. Simulations show that a 180° phase difference does indeed results in maximum E-field cancellation at the safety zone with an approximately 60 % field



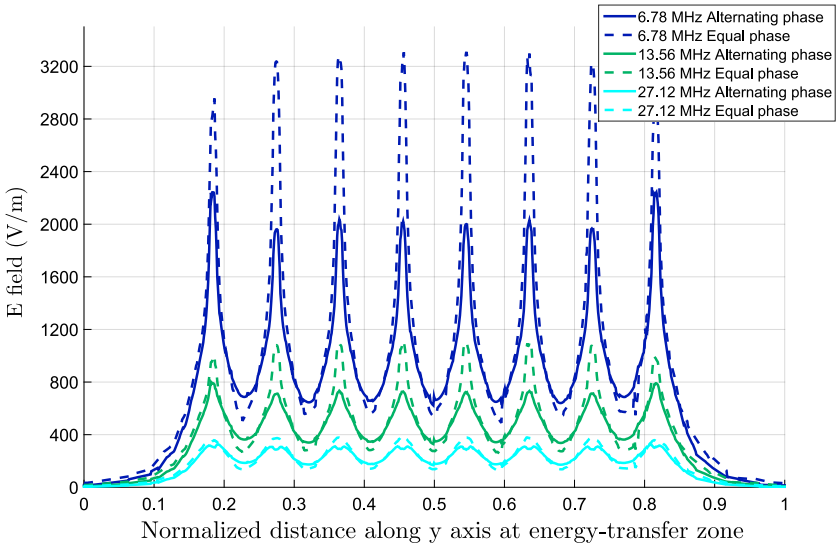
(a)



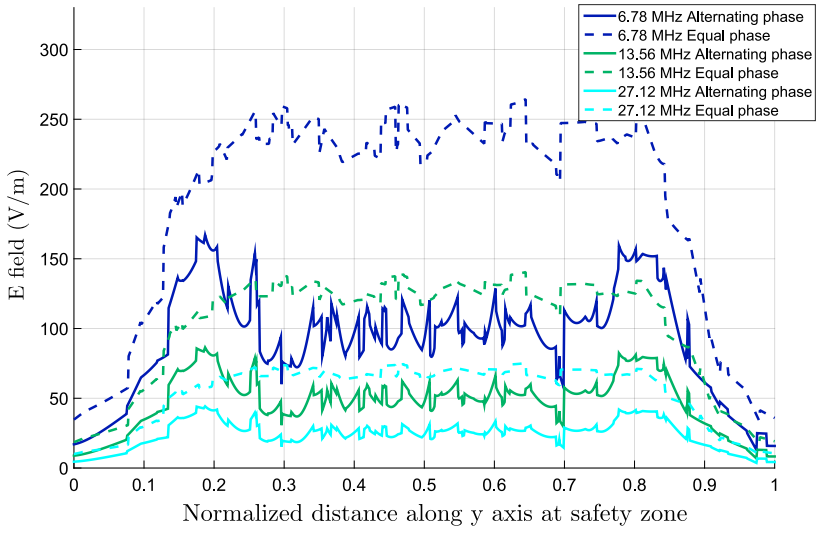
(b)

Figure 6.7: Magnitude of the electric field calculated at the plane of the safety zone for a five-module system at three ISM-band frequencies under consideration. Dashed lines show the E-field with inverter modules in phase, while the solid line shows the E-field with modules having alternating 180° phases.

reduction.

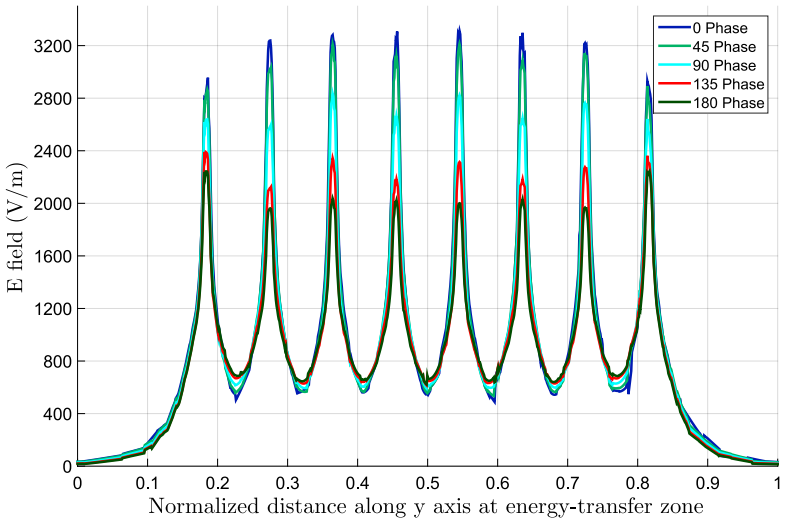


(a)

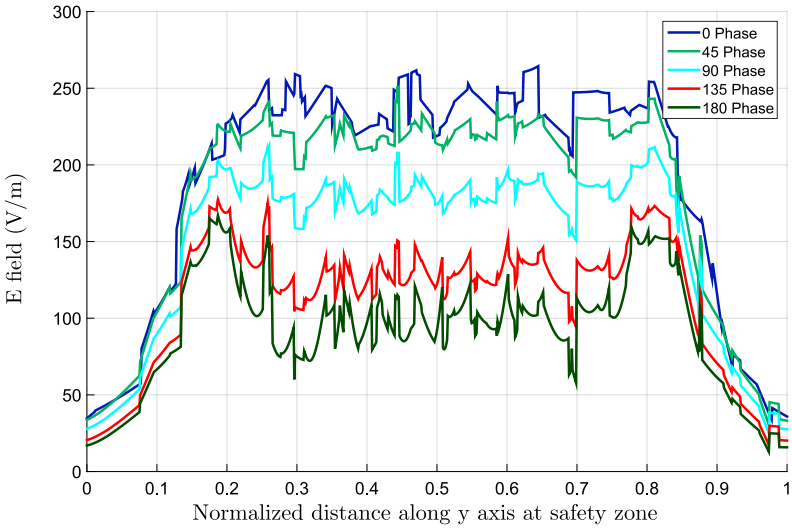


(b)

Figure 6.8: Magnitude of the electric field calculated at the plane of the safety zone for a eight-module system at three ISM-band frequencies under consideration. Dashed lines show the E-field with inverter modules in phase, while the solid line shows the E-field with modules having alternating 180° phases.



(a)



(b)

Figure 6.9: Magnitude of electric field as a function of normalized distance along the body of the car at 6.78 MHz in the energy-transfer zone (a) and safety zone (b) for different alternating phases between modules.

6.4 Conclusion

The simulation results shown in this chapter demonstrate that capacitive power transfer lends itself to an array approach which allows for control of fringing fields for a given power level. A field reduction of approximately 60 % can be achieved with a 8-module system and a 180° alternating phase difference between adjacent modules. A prototype of the system is currently under construction, including inverter and rectifier matching circuits with inductors optimized for efficiency.

Contributions of this chapter include:

- A full-wave electromagnetic model of the near-field capacitive wireless power transfer array. The full-wave simulations demonstrates that a modular near-field array with 8 modules can reduce the magnitude of fringing fields of a capacitive WPT system to approximately 60 %.
- The simulated results obtained in the electromagnetic model are presented at the 2016 IEEE Wireless Power Transfer Conference [26]
- A low power experimental validation of the full-wave electromagnetic model is currently being developed. The measured results could not be ready to include in this thesis, but the results will form part of a subsequent paper.

Chapter 7

Summary and Future Work

Contents

7.1 Summary

The objective of the research presented in this thesis is the application of RF and microwave concepts and techniques to the design of high-frequency power converters, in specific high-frequency dc-dc converters. One of the goals of this approach is to accelerate the development of integrated power supplies by greatly increasing the switching frequency of the converters. The power amplifier-rectifier duality allows for the design of a high-efficiency PA to be used as a high-efficiency rectifier. This is highly beneficial when used at GHz frequencies with wide-bandgap semiconductors such as GaN, due to their high-voltage, high-power capability.

The class-E^2 dc-dc converters presented in this thesis serve as prototypes and as proof-of-concept to the viability of dc-dc converters switching at GHz frequencies. The implementation of self-driving, self-

synchronous rectifiers can be very beneficial in some applications by reducing the complexity of a power system. The elimination of the driver circuitry can significantly reduce the cost, weight and complexity in a system. Furthermore, turning the PA into an oscillator, can completely eliminate the need for RF drivers at the cost of limited control.

By significantly increasing the frequency of operation of a converter, the potential for monolithic integration becomes more accessible due to the requirement of smaller passive components. The proof-of-concept distributed class-E^2 dc-dc converter presented in this thesis investigates the feasibility of a completely distributed design. Although the measured efficiency does not make the converter viable to replace current not-integrated designs for practical applications, the efficiency can be improved by lowering the switching frequency around 1 GHz.

The contributions of each chapter are summarized below.

7.2 Contributions

Chapter 3

In this chapter the implementation of the concept of time-reversal duality was applied to the design of high-efficiency RF power amplifiers and high-efficiency RF rectifiers. It was shown that a high-efficiency PA designed using well known techniques to improve the efficiency, such as harmonic terminations, can change its mode of operation to that of a high-efficiency rectifier. Therefore, the duality between a RF PA and a RF rectifier is introduced. In addition, for the first time, a theoretical analysis of the operation of a self-synchronous rectifier was presented. The theoretical analysis is validated through simulations and experimental measurements and it gives designers sufficient insight to design a self-synchronous rectifier without the need of a load-pull setup. Contributions of this chapter include:

- The application of the concept of time-reversal duality to the design of high-efficiency RF power amplifier and high-efficiency RF rectifiers.
- Investigation of the RF PA-rectifier duality through non-linear simulations using an improved non-linear model of a GaN HEMT that accurately represented the third quadrant of the transistor. The

non-linear simulations are reported in [22].

- Experimental verification of the PA-rectifier duality through Large Signal measurements of a 2.14 GHz PA operating as a high-efficiency power amplifier and a high-efficiency rectifier.
- Demonstration of a RF rectifier operating as a synchronous rectifier without the need of a driver i.e. operating self-synchronously.
- A theoretical analysis of the operation of a class-E self-synchronous rectifier. As well as a theoretical approach to the design of a self-synchronous rectifier instead of a measurement based approach.
- Non-linear simulations validating and expanding the theoretical analysis of a class-E self-synchronous rectifier
- Experimental validation of the analysis presented through the measurement of a GaN class-E self-syncrhonous rectifier as well as a GaN class-B power amplifier operating as a self-synchronous rectifier.
- The work presented in this chapter is published in IEEE Transactions on Microwave Theory & Techniques [21, 24].

Chapter 4

In this chapter two class-E^2 dc-dc converters operating at a switching frequency of 1 and 1.2 GHz are designed, analyzed and characterized. The converters achieve 80 % and 75 % dc-dc efficiency respectively and are among the highest-frequency and highest-efficiency reported in the literature to the best of our knowledge. The application of the concepts established in the analysis of a self-synchronous rectifier to a power amplifier, culminated in the development of an oscillating, self-synchronous class-E^2 dc-dc converter.

Contributions of this chapter include:

- Design and characterization of a 1.2 GHz GaN class-E^2 dc-dc converter.
- Demonstration of a flat 1.2 GHz GaN class-E^2 dc-dc converter with a self-synchronous rectifier.

- A theoretical analysis of a class-E oscillator and a theoretical approach to the design of a class-E oscillator.

- Demonstration of a 900 MHz oscillating, self-synchronous E^2 dc-dc converter with the collaboration of Prof. Jose Angel García and María de las Nieves Ruiz from the university of Cantabria, Spain.

- The work presented in this chapter was presented at the IEEE International Microwave Symposium 2015 [23] and is published in IEEE Transactions on Microwave Theory & Techniques in [24].

Chapter 5

A proof-of-concept fully integrated GaN MMIC dc-dc Converter switching at 4.6 GHz is demonstrated for the first time. The circuit uses two GaN HEMTs, one for the inverter (PA) and one for a synchronous rectifier. The 3.8 mm $\times$ 2.6 mm chip has two RF 50-Ω inputs, a dc input and a dc output, and does not require any external elements. By connecting an external RF tuner to the rectifier gate input, it is demonstrated that the converter can also operate in self-synchronous mode with a single RF input, but with lower efficiency. The efficiency can be increased in this mode of operation by including the appropriate impedance in the rectifier gate on-chip. The maximum end-to-end efficiency is 48 % and can be increased in this particular process by lowering the frequency of operation. It should be noted that the nonlinear device models do not accurately (or at all) predict device behavior for the dynamic load line in the 3^{rd} quadrant of the IV characteristics, making the design only an approximate process since only the inverter (PA) can be simulated.

Contributions of this chapter include:

- The design and characterization of an integrated distributed class-E^2 dc-dc converter switching at 4.6 GHz with a maximum dc-dc efficiency of 48 % at an output power of 0.5 W and a maximum output power of 1.3 W at a dc-dc efficiency of 30 %. All the inductors in the converter are implemented by transmission lines.

- The demonstration of a proof-of-concept of the 4.6 GHz class-E^2 dc-dc converter operating with a self-synchronous rectifier. Terminating the gate of the rectifier and the amplifier on-chip can lead to an integrated distributed class-E^2 dc-dc converter with only dc inputs.

- The work is reported in [25] at the International Microwave Symposium 2016.

Chapter 6

The simulation results shown in this chapter demonstrate that capacitive power transfer lends itself to an array approach which allows for control of fringing fields for a given power level. A field reduction of approximately 60 % can be achieved with a 8-module system and a 180° alternating phase difference between adjacent modules. A prototype of the system is currently under construction, including inverter and rectifier matching circuits with inductors optimized for efficiency. Contributions of this chapter include:

- A full-wave electromagnetic model of the near-field capacitive wireless power transfer array. The full-wave simulations demonstrates that a modular near-field array with 8 modules can reduce the magnitude of fringing fields of a capacitive WPT system to approximately 60 %.

- The simulated results obtained in the electromagnetic model are presented at the 2016 IEEE Wireless Power Transfer Conference.

- A low power experimental validation of the full-wave electromagnetic model is currently being developed. The measured results could not be ready to include in this thesis, but the results will form part of a subsequent paper.

Finally, Appendix A extends the work on rectifiers to ultra-low power diode rectification for wireless energy harvesting. The rectenna shown won 2^{nd} place at the third annual student wireless energy harvesting design competition held at the 2014 IEEE International Microwave Symposium (IMS2014). Appendix B presents a dc-isolated coaxial impedance transformer that is based on guided waves, as opposed to lumped or distributed reactances.

7.3 Future Work

There are numerous opportunities for future work in high-frequency dc-dc converters and wireless energy transfer. The PA-rectifier duality shown in Chapter 3 can be used in the design of high-frequency rectifiers when high-power diodes are not available. The use of a transistor rectifier opens the door for high-power

wireless powering at high-frequencies. However, the inaccuracy of the transistor model in the third quadrant presents a serious problem in the design of high-frequency transistor recitifiers. Hence, there is a need to perform additional research in the modeling of RF transistors in the third quadrant to better understand transistor rectifiers at microwave frequencies. To the best of our knowledge, the model used in this thesis is one of the few reported GaN HEMT transistors that correctly models the third quadrant at high frequencies.

Significant research can be done in high-frequency dc-dc converters as the ones presented in Chapter 4 and Chapter 5. The overall increase in efficiency is of paramount importance and it can be considered the main problem affecting high-frequency converters. As it was shown in Chapter 4, the two main sources of loss in the class-E^2 converter are the inductors in the resonant circuit and the conduction losses due to R_{ON} when the transistor is conducting. Application of topologies such as class-DE amplifiers and rectifiers [115] in converters in the UHF and microwave range can offer an increase in efficiency and should be further investigated.

The dc-dc converters in this thesis do not include voltage regulation. The design of a oscillating, self-synchronous class-E^2 dc-dc converter with a closed-loop voltage regulator control is a clear path for future designs. Currently, two control schemes seem to be the most viable: output voltage control through frequency modulations via the gate-bias voltage of the oscillator, and burst-control modulation by turning the oscillator ON and OFF at a frequency lower than the operating frequency.

The design of a lower frequency integrated resonant converter with the gate impedance terminated on-chip, to transform the PA into an oscillator and operate the rectifier self-synchronously, is also a clear path for future research. Fig. 7.1 shows the proposed layout for the converter. The lower frequency can increase the overall efficiency of the converter and the absence of any RF sources can be an attractive trait for applications where integration is needed and a high-frequency source is not available. Investigating power combining at the transistor level, or at chip level can lead the way to achieving higher power from monolithic integrated dc-dc converters. Integration of a PA and a high-frequency converter in a single chip is also a clear path for future research, given the efficiency of the converter can be improved to be practical in a RF front end.

Additionally, the improvement of inductors in integrated processes such as the 0.15 μm GaN process from Qorvo is an area where significant improvements can be accomplished as shown in [7, 44]. Currently,

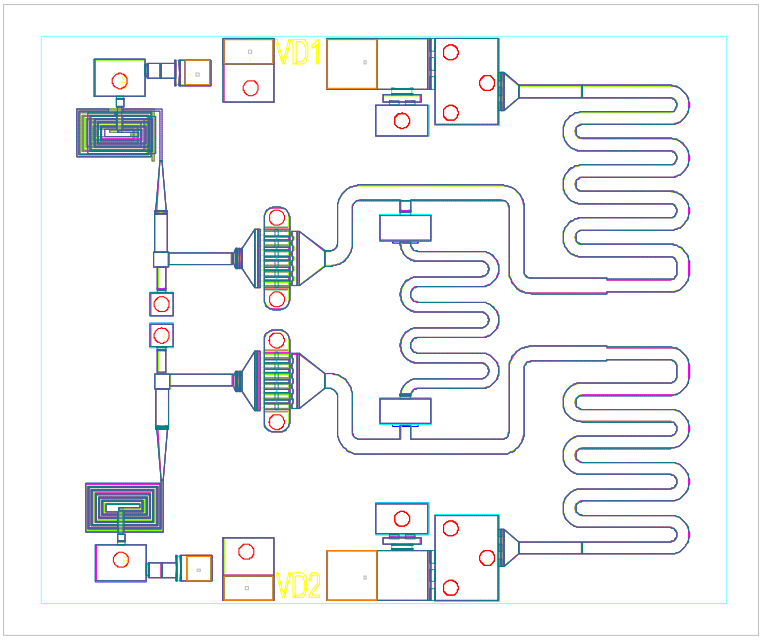


Figure 7.1: Proposed layout for a version of the integrated E^2 dc-dc converter with the gate impedance terminated on-chip. The converter operates without the need of a high-frequency source.

there is interest in thin-film magnetic materials that can be integrated with the GaN process, e.g. Argonne National Lab and Qorvo have tested 100 μm-thick inductor with a $\mu_r \approx 10$. With the improvement of integrated magnetics in the process, integrated dc-dc converters operating at the UHF-1-GHz frequencies can become a viable path toward a power supply on a chip.

With regard to the capacitive WPT system, the project is ongoing with the design and demonstration of a 1 kW prototype consisting of 8 modules spearheaded by Prof. Khurram Afridi and his group at the University of Colorado at Boulder. An independent experimental validation of the full-wave model is currently being developed by measuring the electric field at a distance from the plates using a HI-6005 Electric Field Probe from ETS. The experimental validation of the full-wave model is meant to validate the reduction of the fringing fields by using phase control of the inverters and not the overall efficiency of the system. Therefore the dc-ac and the ac-dc converters are not part of the validation and passive loads and RF amplifiers are used instead.

In summary, the research presented in this thesis addresses fundamental concepts involved in designing dc-dc converter circuits that operate at frequencies that are three orders of magnitude higher than current

high-speed converters in commercial power supplies. The fully integrated MMIC 4.5-GHz dc-dc converter, while functional, exhibited low efficiency and in order to achieve practical efficiencies, a number of directions for future research are identified.

Bibliography

[1] R. Meere, N. Wang, T. O'Donnell, S. Kulkarni, S. Roy, and S. C. O'Mathuna, "Magnetic-Core and Air-Core Inductors on Silicon: A Performance Comparison up to 100 MHz," *IEEE Transactions on Magnetics*, vol. 47, no. 10, pp. 4429–4432, Oct 2011. xii, 13

[2] M. Roberg, J. Hoversten, and Z. Popović, "GaN HEMT PA with over 84% power added efficiency," *Electronics Letters*, vol. 46, no. 23, pp. 1553 –1554, 11 2010. xiii, 33, 34

[3] VTD, "Swap-x402 data sheet." [Online]. Available: http://www.vtd-rf.com/pdf/productpresentation.pdf xiii, 35, 36

[4] O. Jardel, G. Callet, C. Charbonniaud, J. Jacquet, N. Sarazin, E. Morvan, R. Aubry, M.-A. Di Forte Poisson, J. Teyssier, S. Piotrowicz, and R. Quere, "A new nonlinear HEMT model for AlGaN/GaN switch applications," in *2009 European Microwave Integrated Circuits Conference, EuMIC*, Sept 2009, pp. 73–76. xiv, xv, 20, 29, 44, 45, 47

[5] C. Guillaume, J. Faraj, O. Jardel, C. Charbonniaud, J.-C. Jacquet, T. Reveyrand, E. Morvan, S. Piotrowicz, J.-P. Teyssier, and R. Quere, "A new nonlinear HEMT model for AlGaN/GaN switch applications," *International Journal of Microwave and Wireless Technologies*, vol. 2, no. 03, pp. 283–291, 2010. xiv, xv, 20, 29, 44, 45, 47

[6] "ICNIRP Guidelines for Limiting Exposure to Time-Varying Electric, Magnetic and Electromagnetic Fields (up to 300 GHz)." 1998. xix, 96, 98

[7] C. O. Mathúna, N. Wang, S. Kulkarni, and S. Roy, "Review of Integrated Magnetics for Power Supply on Chip (PwrSoC)," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4799–4816, Nov 2012. 1, 13, 111

[8] T. MILLS, "Designing smaller, lighter DC-to-DC converters(DC to DC converters design using HF transistors to achieve high switching speeds while reducing size and weight)," *EEE-THE MAGAZINE OF CIRCUIT DESIGN ENGINEERING*, vol. 17, pp. 76–80, 1969. 2

[9] G. E. Rodriguez, "Circuit considerations for dc to dc conversion above 10 KHZ," NASA, Tech. Rep. TM-X-55667, 1966. 2

[10] S. Y. M. Feng, T. G. Wilson, and W. A. Sander, "Very-high-frequency DC-to-DC conversion and regulation in the low-megahertz range," in *Power Electronics Specialists Conference, 1971 IEEE*, April 1971, pp. 58–65. 2

[11] D. Perreault, J. Hu, J. Rivas, Y. Han, O. Leitermann, R. Pilawa-Podgurski, A. Sagneri, and C. Sullivan, "Opportunities and Challenges in Very High Frequency Power Conversion," in *Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition, 2009. APEC 2009.*, Feb 2009, pp. 1–14. 2, 8, 18, 54

[12] A. Knott, T. M. Andersen, P. Kamby, J. A. Pedersen, M. P. Madsen, M. Kovacevic, and M. A. E. Andersen, "Evolution of very high frequency power supplies," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 3, pp. 386–394, Sept 2014. 2, 8

[13] J. Hu, A. Sagneri, J. Rivas, Y. Han, S. Davis, and D. Perreault, "High-Frequency Resonant SEPIC Converter With Wide Input and Output Voltage Ranges," *IEEE Transactions on Power Electronics*, vol. 27, no. 1, pp. 189–200, Jan 2012. 2, 54

[14] Y. Zhang, M. Rodriguez, and D. Maksimovic, "100 MHz, 20 V, 90% efficient synchronous buck converter with integrated gate driver," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2014, pp. 3664–3671. 2, 54, 55

[15] T. D. Heidel, P. Gradzki, and D. N. Henshall, "Power devices on bulk gallium nitride and diamond substrates: An overview of ARPA-E's SWITCHES program," in *Device Research Conference (DRC), 2015 73rd Annual*, June 2015, pp. 27–28. 2

[16] C. O. Mathuna, N. Wang, S. Kulkarni, R. Anthony, N. Cordero, J. Oliver, P. Alou, V. Svikovic, J. A. Cobos, J. Cortes, F. Neveu, C. Martin, B. Allard, F. Voiron, B. Knott, C. Sandner, G. Maderbacher, J. Pichler, M. Agostinelli, A. Anca, and M. Breig, "Power Supply with Integrated PassivEs - The EU FP7 PowerSwipe Project," in *Integrated Power Systems (CIPS), 2014 8th International Conference on*, Feb 2014, pp. 1–7. 2

[17] F. Neveu, C. Martin, and B. Allard, "Review of high frequency, highly integrated inductive DC-DC converters," in *Integrated Power Systems (CIPS), 2014 8th International Conference on*, Feb 2014, pp. 1–7. 3

[18] M. Roberg, "Analysis & Design of Non-Linear Amplifiers for Efficient Microwave Transmitters," Ph.D. dissertation, University of Colorado at Boulder (CU-Boulder), 2012. 3

[19] J. Hoversten, "Efficient and Linear Microwave Transmitters for High Peak-To-Average Ratio Signals," Ph.D. dissertation, University of Colorado at Boulder (CU-Boulder), 2010. 3, 8

[20] S. Schafer, "Carrier and Envelope Frequency Measurements for Supply-Modulated Microwave Power Amplifiers," Ph.D. dissertation, University of Colorado at Boulder (CU-Boulder), 2016. 3

[21] M. Roberg, T. Reveyrand, I. Ramos, E. Falkenstein, and Z. Popovic, "High-Efficiency Harmonically-Terminated Diode and Transistor Rectifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 12, pp. 1–9, 2012. 6, 40, 52, 108

[22] T. Reveyrand, I. Ramos, and Z. Popovic, "Time-reversal duality of high-efficiency RF power amplifiers," *IET, Electronics Letters*, vol. 48, pp. 1607–1608, 2012. 6, 29, 40, 51, 108

[23] I. Ramos, M. N. Ruiz, J. A. García, and Z. Maksimović, D.and Popović, "A Planar 75 % Efficient 1.2-GHz DC-DC Converter With Self-Synchronous Rectifier," in *2015 IEEE MTT-S International Microwave Symposium (IMS)*, May 2015. 6, 55, 75, 109

[24] I. Ramos, M. N. R. Lavin, J. A. Garcia, D. Maksimovic, and Z. Popovic, "GaN Microwave DC-DC Converters," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 12, pp. 4473–4482, Dec 2015. 6, 52, 55, 75, 108, 109

[25] I. Ramos and Z. Popovic, "A Fully Monolithically Integrated 4.6 GHz DC-DC Converter," in *Microwave Symposium Digest (IMS), 2016 IEEE MTT-S International*, May 2016. 6, 92, 110

[26] I. Ramos, K. Afridi, J. A. Estrada, and Z. Popović, "Near-field Capacitive Wireless Power Transfer Array with External Field Cancellation," in *Wireless Power Transfer Conference (WPTC), 2016 IEEE*, May 2016, p. In press. 6, 105

[27] R. W. Erickson and D. Maksimović, *"Fundamentals of Power Electronics"*, 2nd ed. New York, US: Springer, 2001. 7, 10

[28] S. C. Cripps, *"RF Power Amplifiers for Wireless Communications"*, 2nd ed. Boston, US: ARTECH HOUSE, 2006. 8, 29

[29] M. K. Kazimierczuk, *"RF Power Amplifiers"*, 1st ed. Chichester, UK: Wiley, 2008. 8, 10, 22, 66

[30] "Transistor sine-wave LC oscillators. Some general considerations and new developments," *Proceedings of the IEE - Part B: Electronic and Communication Engineering*, vol. 106, no. 16, pp. 748–758, May 1959. 8

[31] V. Tyler and T. Australia, *A new high-efficiency high-power amplifier*. Telecom Australia, 1958. 8

[32] N. Sokal and A. Sokal, "Class E-A new class of high-efficiency tuned single-ended switching power amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 10, no. 3, pp. 168–176, Jun 1975. 9, 22, 42, 56

[33] T. Mimura, "The early history of the high electron mobility transistor (HEMT)," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 3, pp. 780–782, Mar 2002. 9

[34] A. D. Sagneri, D. I. Anderson, and D. J. Perreault, "Optimization of Integrated Transistors for Very High Frequency DC-DC Converters," *IEEE Transactions on Power Electronics*, vol. 28, no. 7, pp. 3614–3626, July 2013. 10

[35] R. L. Steigerwald, "High-Frequency Resonant Transistor DC-DC Converters," *IEEE Transactions on Industrial Electronics*, vol. IE-31, no. 2, pp. 181–191, May 1984. 11

[36] V. Vorperian and S. Cuk, "A complete DC analysis of the series resonant converter," in *Power Electronics Specialists conference, 1982 IEEE*, June 1982, pp. 85–100. 11

[37] K. D. T. Ngo, "Generalization of resonant switches and quasi-resonant DC-DC converters," in *Power Electronics Specialists Conference, 1987 IEEE*, June 1987, pp. 395–403. 11

[38] D. Maksimovic and S. Cuk, "A general approach to synthesis and analysis of quasi-resonant converters," *IEEE Transactions on Power Electronics*, vol. 6, no. 1, pp. 127–140, Jan 1991. 11

[39] J. M. Rivas, R. S. Wahby, J. S. Shafran, and D. J. Perreault, "New architectures for radio-frequency dc/dc power conversion," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, vol. 5, June 2004, pp. 4074–4084 Vol.5. 11

[40] J. M. Rivas, "Radio Frequency DC-DC Power Conversion," Ph.D. dissertation, Dept. of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA, 2006. 11

[41] T. M. Andersen, S. K. Christensen, A. Knott, and M. A. E. Andersen, "A VHF class E DC-DC converter with self-oscillating gate driver," in *Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE*, March 2011, pp. 885–891. 12

[42] A. J. Hanson, J. A. Belk, S. Lim, D. J. Perreault, and C. R. Sullivan, "Measurements and performance factor comparisons of magnetic materials at high frequency," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2015, pp. 5657–5666. 13

[43] N. Wang, T. O'Donnell, S. Roy, P. McCloskey, and C. O'Mathuna, "Micro-inductors integrated on silicon for power supply on chip," *Journal of Magnetism and Magnetic Materials*, vol. 316, no. 2, pp. e233 – e237, 2007, proceedings of the Joint European Magnetic Symposia. 13

[44] C. R. Sullivan, "Integrating magnetics for on-chip power: Challenges and opportunities," in *Custom Integrated Circuits Conference, 2009. CICC '09. IEEE*, Sept 2009, pp. 291–298. 14, 111

[45] ——, "Optimal choice for number of strands in a litz-wire transformer winding," *IEEE Transactions on Power Electronics*, vol. 14, no. 2, pp. 283–291, Mar 1999. 14

[46] M. E. Dale and C. R. Sullivan, "General Comparison of Power Loss in Single-Layer and Multi-Layer Windings," in *Power Electronics Specialists Conference, 2005. PESC '05. IEEE 36th*, June 2005, pp. 582–589. 14

[47] "Key parameters for selecting rf inductors," 2015, document 671-2. 15

[48] J. R. Warren, K. A. Rosowski, and D. J. Perreault, "Transistor Selection and Design of a VHF DC-DC Power Converter," *IEEE Transactions on Power Electronics*, vol. 23, no. 1, pp. 27–37, Jan 2008. 15

[49] J. Millan, "Wide band-gap power semiconductor devices," *IET Circuits, Devices Systems*, vol. 1, no. 5, pp. 372–379, October 2007. 16

[50] H. Jain, S. Rajawat, and P. Agrawal, "Comparision of wide band gap semiconductors for power electronics applications," in *Recent Advances in Microwave Theory and Applications, 2008. MICROWAVE 2008. International Conference on*, Nov 2008, pp. 878–881. 16, 17

[51] U. K. Mishra, P. Parikh, and Y.-F. Wu, "Algan/gan hemts-an overview of device operation and applications," *Proceedings of the IEEE*, vol. 90, no. 6, pp. 1022–1031, Jun 2002. 17

[52] C. Assad and H. Mureau, "Gan-over-si: The promising technology for power electronics in automotive," in *2012 7th International Conference on Integrated Power Electronics Systems (CIPS)*, March 2012, pp. 1–4. 17

[53] M. Rodríguez, G. Stahl, D. Costinett, and D. Maksimović, "Simulation and characterization of GaN HEMT in high-frequency switched-mode power converters," in *Control and Modeling for Power Electronics (COMPEL), 2012 IEEE 13th Workshop on*, June 2012, pp. 1–6. 17

[54] D. C. Hamill, "Time Reversal Duality and the Synthesis of a Double Class E DC-DC Converter," in *1990 IEEE Power Electronics Specialists Conference PESC*, 1990, pp. 512–521. 21, 42

[55] R. P. Severns and G. Bloom, *"Modern dc-to-dc switchmode power converter circuits"*. New York, NY: Van Nostrand Reinhold, 1985. 21

[56] R. P. Severns, "Switch mode converter topologies - make them work for you!" Intersil Appl. Bull., Tech. Rep. A035, 1980. 21

[57] K.-H. Liu and F. Lee, "Topological constraints on basic pwm converters," in *Power Electronics Specialists Conference, 1988. PESC '88 Record., 19th Annual IEEE*, April 1988, pp. 164–172 vol.1. 21

[58] F. Raab, "Idealized operation of the class e tuned power amplifier," *Circuits and Systems, IEEE Transactions on*, vol. 24, no. 12, pp. 725–735, Dec 1977. 22, 56

[59] T. Mader, "Quasi-Optical Class-E Power Amplifiers," Ph.D. dissertation, University of Colorado at Boulder (CU-Boulder), 1995. 22, 56

[60] M. Kazimierczuk and J. Jozwik, "Resonant DC/DC converter with class-E inverter and class-E rectifier," *Industrial Electronics, IEEE Transactions on*, vol. 36, no. 4, pp. 468–478, Nov 1989. 23, 57

[61] F. Raab, "Maximum efficiency and output of class-f power amplifiers," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 49, no. 6, pp. 1162 –1166, June 2001. 31

[62] J. Hoversten, M. Roberg, and Z. Popovic, "Harmonic load pull of high-power microwave devices using fundamental-only load pull tuners," in *Microwave Measurements Conference (ARFTG), 2010 75th ARFTG*, May 2010, pp. 1–4. 33

[63] J. Verspecht, "Calibration of a measurement system for high frequency nonlinear devices," Ph.D. dissertation, Vrije Universiteit Brussel (VUB), 1995. 35

[64] G. Callet, J. Faraj, O. Jardel, C. Charbonniaud, J.-C. Jacquet, T. Reveyrand, E. Morvan, S. Piotrowicz, J.-P. Teyssier, and R. Quéré, "A new nonlinear hemt model for algan/gan switch applications," *International Journal of Microwave and Wireless Technologies*, vol. 2, no. Special Issue 3-4, pp. 283–291, 2010. 35

[65] J. Faraj, G. Callet, O. Jardel, A. El-Rafei, F. De Groote, R. Quéré, and J. Teyssier, "Time domain large signal characterization of self-biasing phenomena in switch-mode algan/gan hemts," in *74th ARFTG Symposium, International Microwave Symposium Digest*, Montréal, Canada, 2012. 35

[66] M. Nieves Ruiz, R. Marante, and J. A. Garcia, "A class e synchronous rectifier based on an e-phemt device for wireless powering applications," in *IEEE MTT-S International Microwave Symposium Digest*, Montréal, 2012. 35

[67] M. Kazimierczuk and J. Jozwik, "Analysis and design of class E zero-current-switching rectifier," *Circuits and Systems, IEEE Transactions on*, vol. 37, no. 8, pp. 1000 –1009, aug 1990. 35, 57

[68] M. Litchfield, S. Schafer, T. Reveyrand, and Z. Popovic, "High-efficiency X-Band MMIC GaN power amplifiers operating as rectifiers," in *2014 IEEE MTT-S International Microwave Symposium (IMS)*, June 2014, pp. 1–4. 40, 49

[69] M. N. Ruiz and J. A. García, "An E-pHEMT self-biased and self-synchronous class-E rectifier," in *2014 IEEE MTT-S International Microwave Symposium (IMS)*, May 2014, pp. 1–4. 40

[70] P. Cabral, J. Pedro, and N. Carvalho, "Nonlinear device model of microwave power GaN HEMTs for high power-amplifier design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, no. 11, pp. 2585–2592, Nov 2004. 40

[71] T. Mader, E. Bryerton, M. Marković, M. Forman, and Z. Popović, "Switched-Mode High-Efficiency Microwave Power Amplifiers in a Free-Space Power Combiner Array," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 10, pp. 1391–1398, 1998. 42, 57

[72] R. Foley, F. Waldron, J. Slowey, A. Alderman, B. Narveson, and S. C. O. Mathúna, "Technology Roadmapping for Power Supply in Package (PSiP) and Power Supply on Chip (PwrSoC)," in *IEEE 2010 Applied Power Electronics Conference and Exposition (APEC)*, 2010, pp. 525–532. 54

[73] J. M. Rivas, O. Leitermann, H. Yehui, and D. J. Perreault, "A very high frequency dc-dc converter based on a class Φ_2 resonant inverter," in *IEEE Power Electronics Specialists Conference 2008 (PESC)*, 2008, pp. 1657–1666. 54, 55

[74] R. C. N. Pilawa-podgurski, A. D. Sagneri, J. M. Rivas, D. I. Anderson, and D. J. Perreault, "Very-High-Frequency Resonant Boost Converters," *IEEE Transactions on Power Electronics*, vol. 24, no. 6, pp. 1654–1665, 2009. 54, 55

[75] P. Hazucha, G. Schrom, J. Hahn, B. A. Bloechel, P. Hack, G. E. Dermer, S. Narendra, and D. Gardner, "A 233-MHz 80%-87% Efficient Four-Phase DC-DC Converter Utilizing Air-Core Inductors on Package," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 4, pp. 838–845, 2005. 54, 55, 77

[76] J. A. Garcia, R. Marante, and M. N. Ruiz, "GaN HEMT Class E^2 Resonant Topologies for UHF DC/DC Power Conversion," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 12, December 2012, pp. 4220 –4229. 55, 58

[77] J. A. García, R. Marante, M. N. Ruiz, and G. Hernández, "A 1 GHz Frequency-Controlled Class E^2 DC/DC Converter for Efficiently Handling Wideband Signal Envelopes," 2013, pp. 2–5. 55, 68

[78] S. Djukic, D. Maksimović, and Z. Popović, "A planar 4.5-Ghz DC-DC Power Converter," *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 8, pp. 1457–1460, August 1999. 55, 68

[79] J. Jozwik and M. K. Kazimierczuk, "Analysis and design of Class E^2 dc/dc Converter," *IEEE Transactions on Industrial Electronics*, vol. 37, no. 2, pp. 173–183, April 1990. 55, 57

[80] F. Raab, "Class-E, Class-C, and Class-F power amplifiers based upon a finite number of harmonics," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 49, no. 8, pp. 1462 –1468, Aug 2001. 56, 57

[81] R. Gutmann, "Application of rf circuit design principles to distributed power converters," *Industrial Electronics and Control Instrumentation, IEEE Transactions on*, vol. IECI-27, no. 3, pp. 156–164, Aug 1980. 56

[82] R. Gutmann and J. Borrego, "Power Combining in an Array of Microwave Power Rectifiers," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 27, no. 12, pp. 958–968, Dec 1979. 56

[83] R. Redl, B. Molnar, and N. Sokal, "Small-Signal Dynamic Analysis of Regulated Class E DC/DC Converters," *Power Electronics, IEEE Transactions on*, vol. PE-1, no. 2, pp. 121–128, April 1986. 56

[84] ——, "Class E Resonant Regulated DC/DC Power Converters: Analysis of Operations, and Experimental Results at 1.5 MHz," *Power Electronics, IEEE Transactions on*, vol. PE-1, no. 2, pp. 111–120, April 1986. 56

[85] N. Sokal, R. Redl, and B. Molnar, "Class E high-frequency high-efficiency dc/dc power converter," U.S. Patent 4 607 323, 1986. 56

[86] M. Kazimierczuk, "Class E tuned power amplifier with shunt inductor," *Solid-State Circuits, IEEE Journal of*, vol. 16, no. 1, pp. 2–7, Feb 1981. 56

[87] J. Ebert and M. Kazimierczuk, "Class E high-efficiency tuned power oscillator," *Solid-State Circuits, IEEE Journal of*, vol. 16, no. 2, pp. 62–66, Apr 1981. 56

[88] M. Kazimierczuk and J. Jozwik, "Class E zero-voltage-switching rectifier with a series capacitor," *Circuits and Systems, IEEE Transactions on*, vol. 36, no. 6, pp. 926–928, Jun 1989. 57

[89] M. Kazimierczuk, "Class e low dv/sub d//dt rectifier," *Electric Power Applications, IEE Proceedings B*, vol. 136, no. 6, pp. 257–262, Nov 1989. 57

[90] ——, "Analysis of class E zero-voltage-switching rectifier," *Circuits and Systems, IEEE Transactions on*, vol. 37, no. 6, pp. 747–755, Jun 1990. 57

[91] M. Kazimierczuk and J. Jozwik, "Class E2 narrow-band resonant DC/DC converters," *Instrumentation and Measurement, IEEE Transactions on*, vol. 38, no. 6, pp. 1064–1068, Dec 1989. 57

[92] ——, "Optimal topologies of resonant dc/dc converters," *Aerospace and Electronic Systems, IEEE Transactions on*, vol. 25, no. 3, pp. 363–372, May 1989. 57

[93] H. Hase, H. Sekiya, J. Lu, and T. Yahagi, "Resonant dc/dc converter with class E oscillator," in *2005 IEEE International Symposium on Circuits and Systems (ISCAS)*, vol. 1, 2005, pp. 720–723. 67

[94] H. Hase, H. Sekiya, L. Jianming, and T. Yahagi, "Novel design procedure for MOSFET class E oscillator," in *The 2004 47th Midwest Symposium on Circuits and Systems*, vol. 1, July 2004, pp. I–33–6. 68

[95] S. Jeon, A. Suarez, and D. Rutledge, "Nonlinear design technique for high-power switching-mode oscillators," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 10, pp. 3630–3640, Oct 2006. 71

[96] S. Matsumoto, M. Mino, and T. Yachi, "Integration of a power supply system for system-on-chip," *IEICE Trans. Fundamentals*, vol. E80-A, no. 2, pp. 276–282, February 1997. 77

[97] M. Bathily, B. Allard, and F. Hasbani, "A 200-MHz Integrated Buck Converter With Resonant Gate Drivers for an RF Power Amplifier," *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 610–613, Feb 2012. 77

[98] J. Sun, D. Giuliano, S. Devarajan, J. Q. Lu, T. P. Chow, and R. J. Gutmann, "Fully monolithic cellular buck converter design for 3-d power delivery," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 17, no. 3, pp. 447–451, March 2009. 77

[99] V. Kursun, S. G. Narendra, V. K. De, and E. G. Friedman, "Analysis of buck converters for on-chip integration with a dual supply voltage microprocessor," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 11, no. 3, pp. 514–522, June 2003. 77

[100] G. Schrom, P. Hazucha, J.-H. Hahn, V. Kursun, D. Gardner, S. Narendra, T. Karnik, and V. De, "Feasibility of monolithic and 3d-stacked dc-dc converters for microprocessors in 90nm technology generation," in *Low Power Electronics and Design, 2004. ISLPED '04. Proceedings of the 2004 International Symposium on*, Aug 2004, pp. 263–268. 77

[101] J. Chandrasekaran, J. Sun, and V. Mehrotra, "Vertically packaged switched-mode power converter," U.S. Patent 7 012 414, 2006. 77

[102] J. Sun, J. Q. Lu, D. Giuliano, T. P. Chow, and R. J. Gutmann, "3d power delivery for microprocessors and high-performance asics," in *Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE*, Feb 2007, pp. 127–133. 77

[103] G. Patounakis, Y. W. Li, and K. L. Shepard, "A fully integrated on-chip DC-DC conversion and power management system," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 3, pp. 443–451, March 2004. 77

[104] S. Schafer, M. Litchfield, A. Zai, Z. Popovic, and C. Campbell, "X-band mmic gan power amplifiers designed for high-efficiency supply-modulated transmitters," in *Microwave Symposium Digest (IMS), 2013 IEEE MTT-S International*, June 2013, pp. 1–3. 78

[105] J. Dai and D. C. Ludois, "A Survey of Wireless Power Transfer and a Critical Comparison of Inductive and Capacitive Coupling for Small Gap Applications," *IEEE Transactions on Power Electronics*, vol. 30, no. 11, pp. 6017–6029, Nov 2015. 94

[106] G. A. Covic and J. T. Boys, "Modern Trends in Inductive Power Transfer for Transportation Applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 1, pp. 28–41, March 2013. 94

[107] C. T. Rim, "The Deployment and Deployment of On-Line Electric Vehicle (OLEV)." in *2013 IEEE Energy Conversion Congress and Exposition*, Sep 2013. 94

[108] R. D. Fernandes, J. N. Matos, and N. B. Carvalho, "Resonant Electrical Coupling: Circuit Model and First Experimental Results," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 9, pp. 2983–2990, Sept 2015. 94

[109] M. Kline, I. Izyumin, B. Boser, and S. Sanders, "Capacitive power transfer for contactless charging," in *Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE*, March 2011, pp. 1398–1404. 94

[110] T. Ohira, "Via-wheel power transfer to vehicles in motion," in *Wireless Power Transfer (WPT), 2013 IEEE*, May 2013, pp. 242–246. 94

[111] A. Sepahvand, A. Kumar, K. Afridi, and D. Maksimovic, "High power transfer density and high efficiency 100 MHz capacitive wireless power transfer system," in *Control and Modeling for Power Electronics (COMPEL), 2015 IEEE 16th Workshop on*, July 2015, pp. 1–4. 94

[112] F. Lu, H. Zhang, H. Hofmann, and C. Mi, "A Double-Sided LCLC-Compensated Capacitive Power Transfer System for Electric Vehicle Charging," *IEEE Transactions on Power Electronics*, vol. 30, no. 11, pp. 6011–6014, Nov 2015. 94

[113] A. Kumar, S. Pervaiz, C.-K. Chang, S. Korhummel, Z. Popovic, and K. K. Afridi, "Investigation of power transfer density enhancement in large air-gap capacitive wireless power transfer systems," in *Wireless Power Transfer Conference (WPTC), 2015 IEEE*, May 2015, pp. 1–4. 94, 95

[114] "IEEE Standard for Safety Levels with Respect to Human Exposure to Radio Frequency Electromagnetic Fields, 3 KHz to 300 GHz," 1999, iEEE Standard 95.1. 98

[115] T. Suetsugu and M. K. Kazimierczuk, "Integration of class DE inverter for on-chip DC-DC power supplies," in *Circuits and Systems, 2006. ISCAS 2006. Proceedings. 2006 IEEE International Symposium on*, May 2006, pp. 4 pp.–. 111

[116] A. Costanzo, M. Fabiani, A. Romani, D. Masotti, and V. Rizzoli, "Co-design of ultra-low power rf/microwave receivers and converters for rfid and energy harvesting applications," in *Microwave Symposium Digest (MTT), 2010 IEEE MTT-S International*, May 2010, pp. 856–859. 129

[117] E. Falkenstein, M. Roberg, and Z. Popovic, "Low-power wireless power delivery," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 60, no. 7, pp. 2277 –2286, july 2012. 131, 135

[118] C. A. Balanis, *Antenna Theory Analysis and Design*, 3rd ed. John Wiley and Sons, 2005. 131

[119] G. Marrocco, "The art of UHF RFID antenna design: impedance-matching and size-reduction techniques," *IEEE Antennas and Propagation Magazine*, vol. 50, no. 1, pp. 66–79, Feb 2008. 131

[120] R. Scheeler, S. Korhummel, and Z. Popovic, "A Dual-Frequency Ultralow-Power Efficient 0.5-g Rectenna," *IEEE Microwave Magazine*, vol. 15, no. 1, pp. 109–114, Jan 2014. 131, 134

[121] Z. Popović, E. A. Falkenstein, D. Costinett, and R. Zane, "Low-power far-field wireless powering for wireless sensors," *Proceedings of the IEEE*, vol. 101, no. 6, pp. 1397–1409, June 2013. 135

[122] C. L. Ruthroff, "Some broad-band transformers," *Proceedings of the IRE*, vol. 47, no. 8, pp. 1337–1342, Aug 1959. 136

[123] G. Guanella, "New method of impedance matching in radio-frequency circuits," *Brown Boveri Review*, pp. 327–329, September 1944. 136

[124] N. Ehsan, K. J. Vanhille, S. Rondineau, and Z. Popovic, "Micro-Coaxial Impedance Transformers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 11, pp. 2908–2914, Nov 2010. 136, 137, 138, 143

[125] J. E. Post, "Analysis and Design of Planar, Spiral-Shaped, Transmission-Line Transformers," *IEEE Transactions on Advanced Packaging*, vol. 30, no. 1, pp. 104–114, Feb 2007. 136

[126] R. F. Sobrany and I. D. Robertson, "Ruthroff transmission line transformers using multilayer technology," in *Microwave Conference, 2003. 33rd European*, vol. 2, Oct 2003, pp. 559–562 vol.2. 136

[127] P. A. Dalal, H. Y. Yang, and C. Q. Lee, "High frequency transmission line transformer for DC/DC converters," in *Power Electronics Specialists Conference, 1995. PESC '95 Record., 26th Annual IEEE*, vol. 2, Jun 1995, pp. 671–677 vol.2. 137

[128] D. S. Filipovic, M. V. Lukic, Y. Lee, and D. L. Fontaine, "Monolithic Rectangular Coaxial Lines and Resonators With Embedded Dielectric Support," *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 11, pp. 740–742, Nov 2008. 137

Appendix A

Low Power Wireless Energy Harvester

A.1 Introduction

With the increased interest in wireless energy transfer in recent years, bolstered by the ever increasing use of low power sensors and the Internet of Things, there has been a significant interest in the design of compact low power energy harvesters. In environments with no sunlight and vibration, harvesting of very low power densities in the radio frequency of the spectrum is possible for low-power low duty cycle applications [116]. The WEH presented in this paper won second place at the third annual student wireless energy harvesting design competition held at the 2014 IEEE International Microwave Symposium (IMS2014). The competition requires the design of a WEH capable of harvesting a minimum of 10 μW of DC power from a power density of 1 μW/cm^2 at 2.45 GHz. The polarization of the source is specified to be linear vertical, the general location of the source is known, and the DC load is chosen by the designer. The maximum weight of the harvester cannot exceed 20 g and the figure of merit used to evaluate the WEH is defined by

$$FOM = 10\log_{10}\left[\frac{(\frac{P_L(\mu W)}{10(\mu W)})^2}{\frac{D^2(cm^2)}{25(cm^2)}}\right](dB) \tag{A.1}$$

where D refers to the largest dimension of the WEH andP_L is the output DC power across the load.

The figure of merit implies certain specifications and tradeoffs in the design: lightweight materials

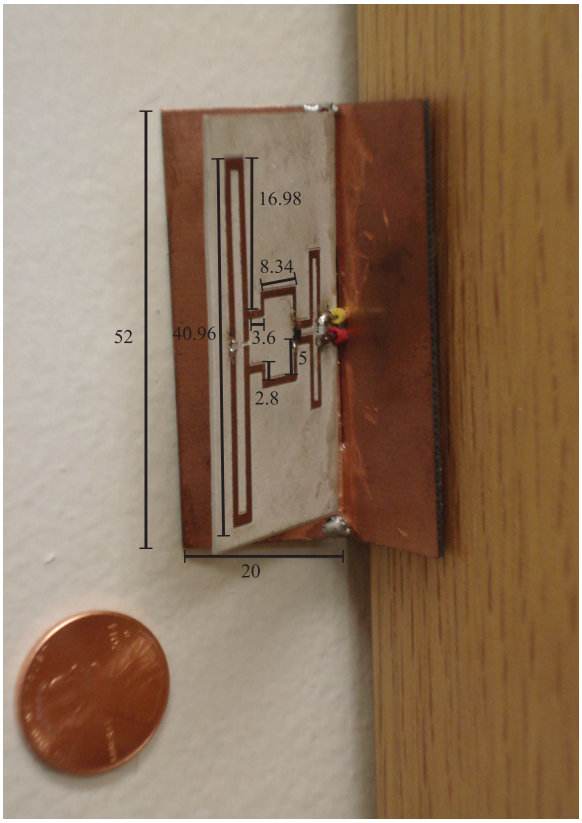


Figure A.1: Photograph of energy harvester prototype wtih a Skyworks SMS7630-079. All dimensions are given in millimeters.

should be used, the antenna and rectifier need to be as compact as possible while providing gain in the direction of the source; the rectifier efficiency needs to be maximized at very low power levels; and the load needs to be chosen to maximize the total rectified power. These constraints motivated the prototype shown in Fig. A.1. A single shunt Schottky diode is chosen as the rectifying element due to the very low power density requirement which would imply reduced efficiency for a rectifier with more diodes, such as a charge pump. The overall dimensions are shown in millimeters and the largest linear dimension in equation A.1 is $D = 52\,\text{mm}$. Additionally, for in-building applications we imposed a form-factor that allows non-obtrusive placement of the harvester in any corner inside a building. The corner reflector shields the rectenna from power management and sensor circuitry that can be placed on the back side of the reflector.

A.2 Design and integration of rectifier and antenna

The RF harvesting component consists of an antenna, rectifier, RF matching circuit and DC collection circuit with DC load. The first step in the design is the characterization of the non-linear rectifying device [117]. Initially, the W-Band ZBD Schottky diode from VDI is chosen. A nonlinear model provided by Modelithics is used to perform a load pull simulation in NI-AWR. The initial load pull is performed with a DC load of 2.2 kΩ and a minimum incident power of -15 dBm. The results of the load pull are shown in Fig. A.2. The simulations show that both the real and imaginary parts of the optimum impedance for maximum efficiency are very large, making matching challenging. Assuming an initial rectifying efficiency of 50 %, a minimum effective area of 20 cm^2 would be required to harvest 10 μW from a 1 $\mu W/cm^2$ power density, which translates to a minimum 2.24 dB antenna gain.To minimize matching circuit size, an antenna with a high impedance is a good choice. A folded dipole with an arm separation $d = 4.2\,\text{mm} \ll \lambda$ is chosen, since its input impedance is on the order of several hundred ohms and given by [118].

$$Z_{in} = N^2 Z_d \tag{A.2}$$

where Z_d is the impedance of a single resonant dipole, and $N = 2$ is the number of elements for a single folded dipole.

An inductive feed [119, 120], is used to match the antenna to the highly reactive diode. An equiavalent schematic of the circuit is shown in Fig. A.3. For reduced size, the circuit was designed on a high-permitivity 25-mil thick RT/duroid 6010.2LM substrate with a ϵ_r= 10.2 ± 0.25. A model of the WEH is created in HFSS for fine tunning with full-wave simulations. To further increase the power received by the diode, a thin metallic corner reflector is added behind the rectenna to increase the gain of the folded dipole. Fig. A.4 shows the simulated circuit, the peak gain of the antenna alone is 7.48 dBi. The inductive match is simulated together with the antenna in HFSS, and results in an impedance presented at the diode of 248.5+j628 Ω, which is slightly off the maximum DC power contour of Fig. A.2. The length of the folded dipole is 39 mm which is approximately 1λ, the length of the reflectors and the distance from the antenna to the reflector is adjusted for maximum gain while maintaining a compact design. Each reflector measures 52 mm ($\approx 1.35\lambda$)

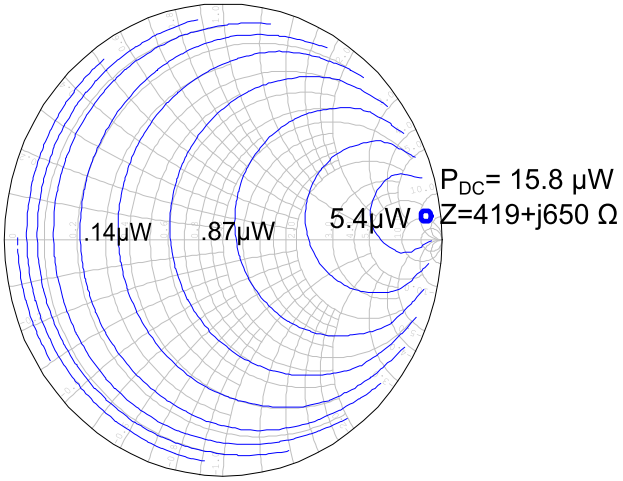


Figure A.2: Simulated load pull contours for the W-band ZBD diode from VDI, performed with an incident power of -15 dBm and a DC load of 2.2 kΩ. Maximum rectified power achieved is 15.8 μW at an impedance of 419+650 Ω. The contours represent constant DC rectified power in μW.

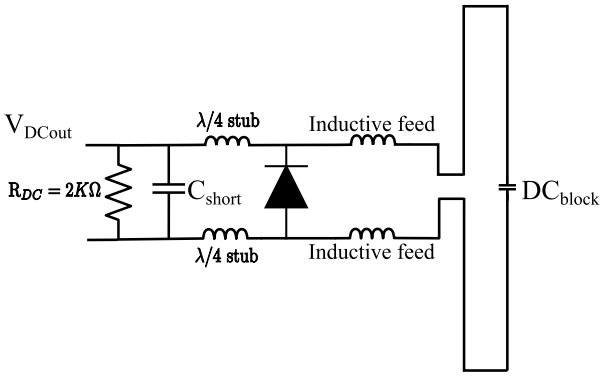


Figure A.3: Simplified schematic of rectenna circuit. C_{short} = 10 pF, a DC blocking capacitor DC_{block} is placed at the symmetry plane of the dipole to behave as a short circuit at 2.45 GHz and avoid short circuiting the diode.

by 20 mm (≈0.5λ) and the two reflectors form an angle between them of 100°. Considering the position of the diode to be the feed, the distance from the reflectors is 11 mm or 0.29 λ.

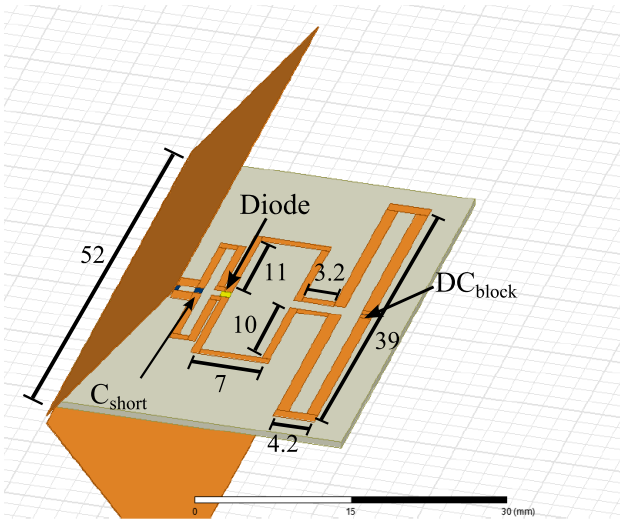


Figure A.4: Layout of the rectenna with the VDI diode match, corresponding to the circuit diagram in the previous figure. The DC load is connected on the back of the reflector though vias. All dimensions are given in mm.

A.3 Measurements and Results

The implemented prototype has a mass of only 7.5 g. The WEH is measured in an anechoic chamber calibrated to provide a power density of approximately 1 μW/cm^2 at the location of the receiver. A low frequency 2.2 kΩ resistor is attached to the DC load terminals and the voltage measured for different azimuth angles. The maximum rectified power is 15.05 μW at approximately 25° from the symmetry plane. Power rectified by the diode seems to be considerably lower than expected, probably due to the high optimal impedance that is difficult to reach with a compact matching circuit. The rectenna design is not symmetrical, resulting in the pattern with a split lobe, which is not a disadvantage for harvesting applications.

A.3.1 Alternate Design with the Skyworks SMS7630-079 Diode

As previously mentioned,the high impedance required for the W-band ZBD diode becomes a problem for high efficiency energy harvesters. A modified version of the WEH using the Skyworks SMS7630-079 GaAs Schottky diode is designed as a modification of the WEH from Fig. A.4. The impedance required for maximum efficiency is lower in this case, about 50+j250 Ω obtained by load-pull simulations with a

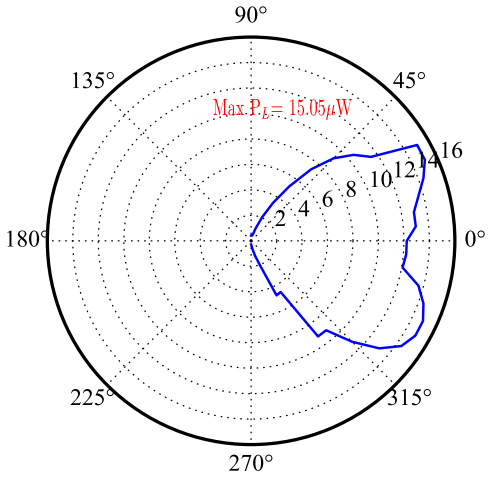


Figure A.5: Measured radiation pattern of the rectenna is obtained by measuring the DC power across the load and includes the efficiency change over angle. The incident power density is 1 μW/cm^2 and the DC load is 2.2 kΩ. The rectified power is shown in μW, with a peak of 15.05 μW.

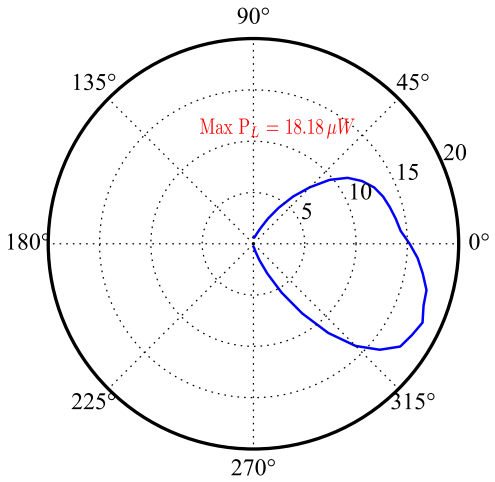


Figure A.6: Pattern of rectified power as a function of azimuth angle for Skyworks SMS7630-079 diode. Measurements are performed with a 1 μW/cm^2 incident power density and a 2.2 kΩ DC load. Rectified power is shown in μW. The maximum rectifed power is 18.05 μW.

Modelithics nonlinear model [120]. The design is modified to maximize gain with different inductive feed dimensions and angle of the corner reflector of 116°, compared to 100° for the first design. The dimensions are shown in Fig. A.1.

The measurements results are shown in Fig. A.6. The rectified power is increased by 20 % compared to the VDI diode prototype, with a maximum rectified power of 18.05 μW at $\approx$ 25° from the symmetry plane.

The following table shows the rectified power for higher power densities, which increases linearly with incident power density while the efficiency remains relatively constant.The efficiency can be estimated from the power density and geometric area of the rectenna as in [117], and the lower bound on efficiency is calculated to be 30% based on the antenna gain of 7.5 dB.

Power density (μW/cm^2)	Maximum rectified power (μW)
1	18.2
1.26	23.22
1.58	29.32
2	35.64
2.5	42
3.16	47.7

The 20 % increase in rectified power results in an increase in the figure of merit from 7.164 dB to 9.07 dB. Because the two designs have similar dimensions and similar gain, it is safe to assume that the increase in rectified power is mainly due to the appropriate impedance matching of the diode.

A.4 Conclusion

The design of two wireless energy harvesting rectennas is presented. Each WEH consists of a folded dipole with an inductive feed and a corner reflector. Two different diodes are used, and the high impedance needed for maximum efficiency for the VDI ZBD diode proves difficult to achieve and therefore matching to the Skyworks SMS7630-079 results in a more efficient design. The WEH can easily be positioned in any corner for harvesting while not being overly intrusive. The WEH presented in this paper won second place in the student wireless energy harvesting design competition held at the 2014 IEEE International Microwave Symposium. The tens of microwatts of available rectified power in an environment that has 1-2 μW/cm^2 incident power density can be used to trickle-charge a storage element for low-energy electronic applications [121].

Appendix B

Micro-coaxial decade-bandwidth dc-isolated transformers

B.1 Introduction

Transmission-line transformers are broadband and compact, and therefore widely used as impedance-matching networks, e.g. in wideband amplifiers and antennas [122]. In TLTs, such as Guanella [123] and Ruthroff [122] transformers, the impedance transformation is realized through transmission lines that are interconnected to form a balanced configuration. In Guanella transformers for example, a pair of coaxial lines are connected in parallel at the low-impedance side and in series at the high-impedance side in order to realize a 1:4 impedance transformation. If the lines have equal electrical length, the transformer is balanced and the currents/voltages add in phase at the low/high impedance ports respectively, so that the impedance transformation is theoretically frequency-independent. At low frequency, TLTs can be fabricated from bifilar lines wound around ferrite cores, while at UHF or higher frequencies coaxial lines are usually employed. In addition, micro-coaxial [124] and monolithic microwave integrated circuit (MMIC) implementations [125], [126] of the Guanella and Ruthroff transformers have been demonstrated up to Ka band. However, despite their decade-wide bandwidths, both Guanella (Fig. B.1(a)) and Ruthroff transformers are

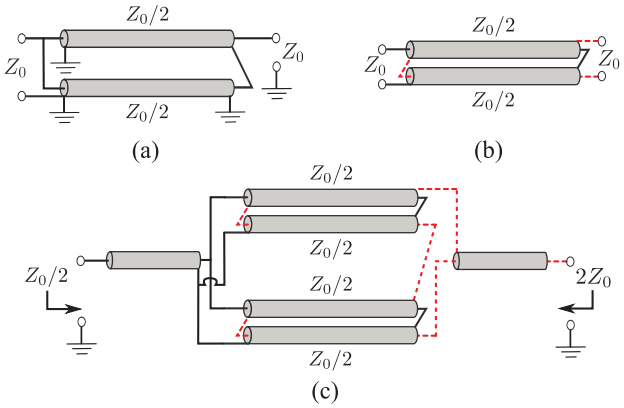


Figure B.1: Circuit schematics of (a) a traditional Guanella, (b) a 1:1 and (c) 4:1 dc-isolated transformers. In the dc-isolated transformers the colors and line types (red dashed/black continuous) identify the separate dc paths.

not dc-isolated, because their input and output ports are shorted to a common ground. This is not desirable in many applications, such as isolated power converter circuits [127].

In this work wideband micro-coaxial dc-isolated TLTs are discussed. Two coaxial transmission lines are connected as in Fig. B.1(b) to create a basic dc-isolated 1:1 transformer, operating from 1 to 10 GHz. The basic 1:1 transformer is then used to implement a 1:4 isolated transformer as in Fig. B.1(c). The transformers are fabricated in PolyStrataTM wafer-scale technology, a sequential layer deposition process suitable to fabricate micro-coaxial lines having low loss (0.1 dB/cm at 38GHz [128]), high isolation and a wide range of characteristic impedances [124]. This section is a collaboration with Dr. Leonardo Ranzani.

B.2 Device design

The basic isolated 1:1 transformer consists of two microcoaxial lines, of equal electrical lengths and characteristic impedances $Z_0/2$, connected as in Fig. B.1(a). If the device is balanced, the currents flowing through the inner and outer conductors of each line are equal and have opposite direction. The voltages at the input and output ports are twice the voltage across each coaxial line and therefore the transformer is electrically equivalent to a single transmission line with impedance Z_0. The bandwidth of operation is determined by the physical layout of the device. At low frequencies the coaxial lines are effectively lumped inductors and the lower frequency limit decreases with increasing lines length. The upper frequency depends

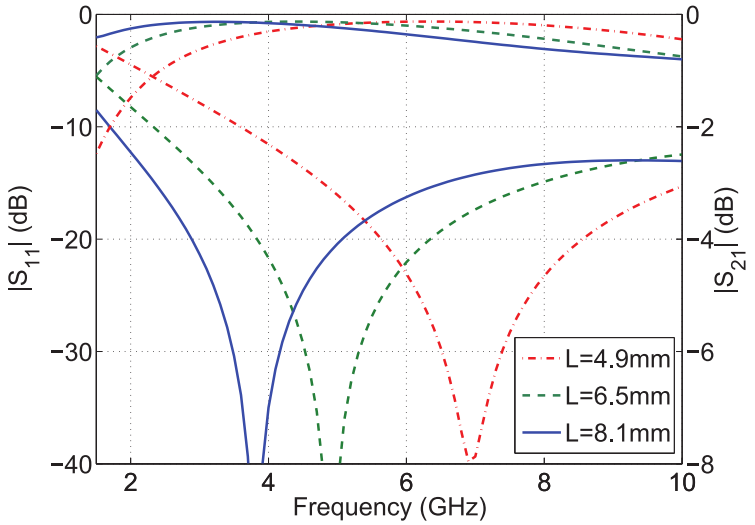


Figure B.2: Simulation of the 1:1 transformer transmission and return loss for different line lengths. The return loss is minimum when the free-space wavelength satisfies $\lambda_0/10$ = L, where L is the length of the coaxial lines

on the amount of unbalanced delay between the coaxial lines, the finite length of interconnections between the micro-coaxial lines and undesired electromagnetic modes in the structure [124]. Therefore, in order to determine the upper frequency limit and optimize the device length and corresponding operating bandwidth, full-wave simulations are required.

The 1:1 subcircuit is designed to be matched to $Z_0 = 50\,\Omega$ and therefore the impedance of the inner coaxial lines is set equal to $25\,\Omega$. Full-wave electromagnetic simulations performed in Ansys HFSS^R showed that optimal impedance match is obtained at the frequency where the coaxial lines are $\lambda_0/10$ long (where λ_0 is the free-space wavelength at minimum return loss), as shown in Fig. B.2.

The PolyStrata^{TM} implementation of the transformer is shown in Figure 3. The micro-coaxial lines are fabricated by sequentially depositing multiple layers of copper and photoresist. The thickness of the copper layers can range from 5 to 100 μm. At the end of the process, the photoresist is removed through 200μm $\times$200μm release holes, to leave two air-filled coaxial lines, in which the inner conductor is supported by 20 μm thick dielectric straps periodically spaced along the line. The straps occupy a small portion of the coaxial line volume and therefore have minimal influence on the microwave performance at the frequencies of interest in this work (below 20 GHz). A photograph of the fabricated transformer is shown in Fig. B.4(a).

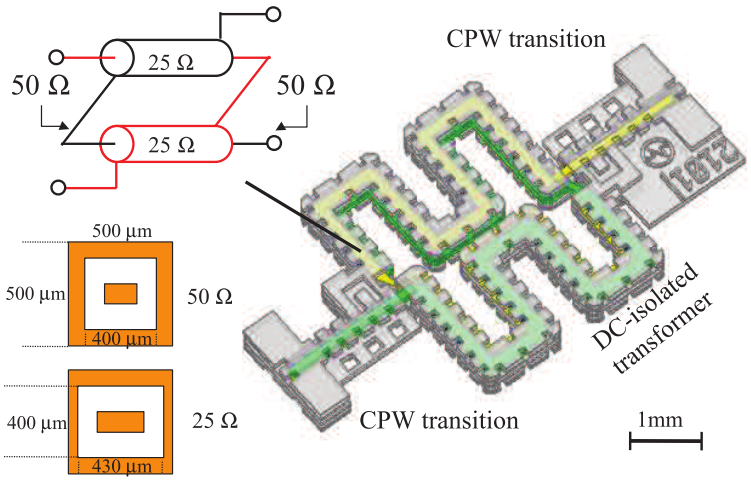


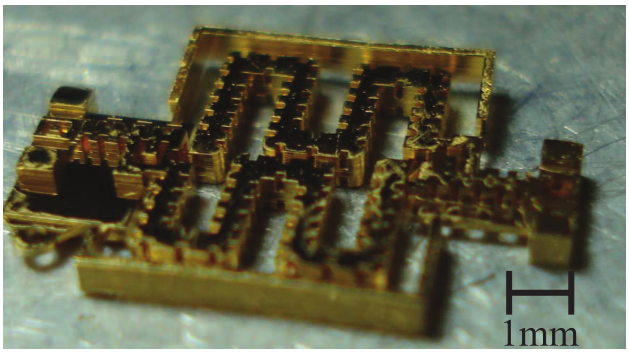
Figure B.3: Layout of the fabricated 1:1 transformer. Two rectangular microcoaxial lines are interconnected as shown in Fig. B.1(b). The coaxial lines have 500 μm × 500 μm cross section. The inner conductor cross section is 200 μm × 155 μm for the 50 Ω lines and 200 μm × 220 μm for the internal 25 Ω lines.

The dimensions of the device are 10.24 mm×5.6 mm. The spacing of the release holes is 600 μm, while the coaxial line cross-section dimensions are described in Fig. B.3.

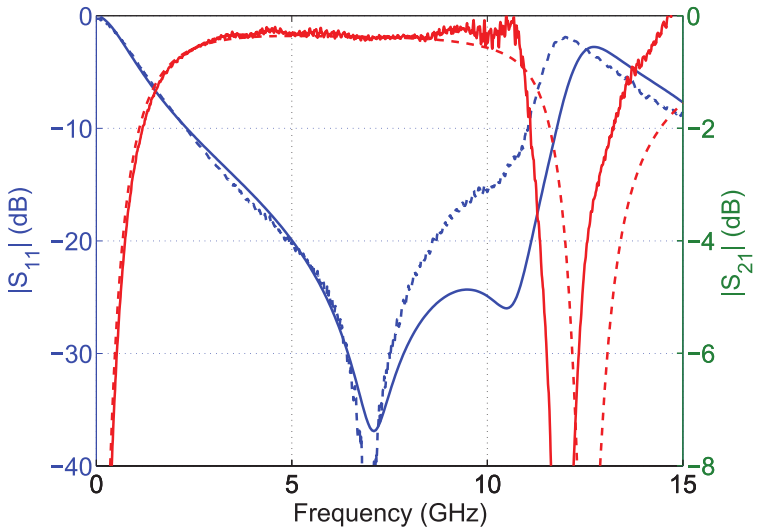
B.3 RF AND DC MEASUREMENTS

Probe transitions (15 GHz bandwidth) compatible with 250 μm-pitch CPW microwave probes are designed as part of the transformer for testing purposes. The transformer is placed onto a 5-mm thick piece of foam ($\epsilon_r \approx 1.005$ at RF) for mechanical support and characterized with a Cascade microwave probe station connected to an Agilent PNA E8364C. Calibration is performed with a set of Short-Open-Load- Thru (SOLT) CPW Alumina standards. Fig. B.4(b) shows the measured and simulated results. The device 3-dB band is over a decade wide, from 0.9 GHz to 11.24 GHz. The insertion loss is below 0.5 dB from 2.8 GHz to 10.8 GHz.

The device dc isolation is tested by applying a dc-voltage across its terminals, while at the same time the dc current is monitored to detect any discharge. No current is detected up to 450 V of dc voltage across the terminals. Above this voltage level the device starts conducting and a nonzero dc current is detected. The minimum air gap in the device is given by the distance between the coaxial lines inner and outer conductor



(a)

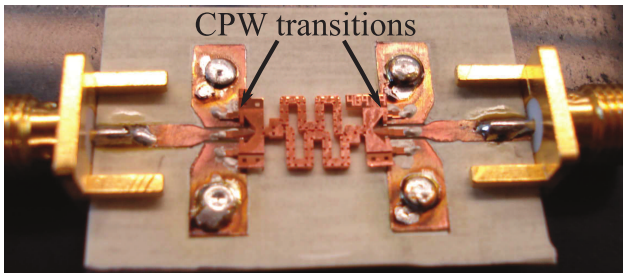


(b)

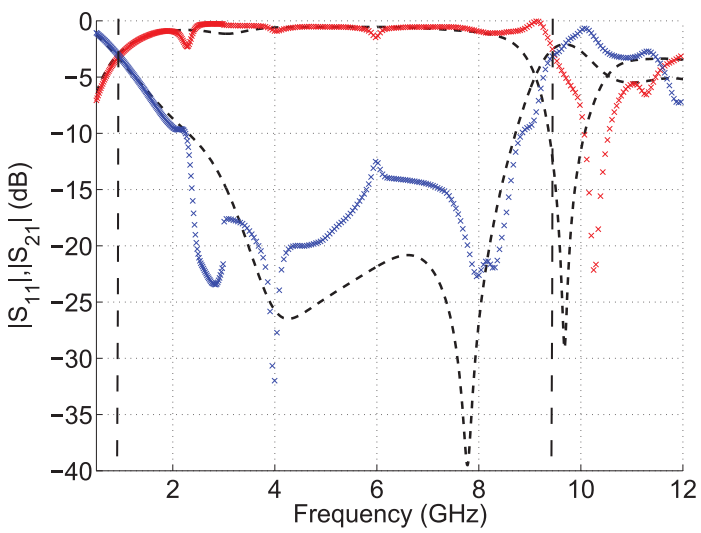
Figure B.4: (a) Photograph of the fabricated 1:1 transformer prototype with a 4.5 mm device width and minimum return loss at 7 GHz. (b) Measured transmission and return loss. Full-wave electromagnetic simulations are plotted in dashed lines.

(150 μm). The measured breakdown voltage is therefore consistent with a value of 3×10^6 V/m for the dielectric strength of air.

In order to use the micro-coaxial transformers as an impedance matching element, it is useful to be able to mount it on a microwave circuit board. For this purpose we developed wideband micro-coaxial-to-CPW transitions, as shown in Fig. B.5, and tested the performance of a mounted device. The transition has three 0.5×1.8 mm contact fingers and a dielectric strap is added between the fingers for structural support. The transition dimensions were optimized in HFSS® and the simulated return loss of the final



(a)

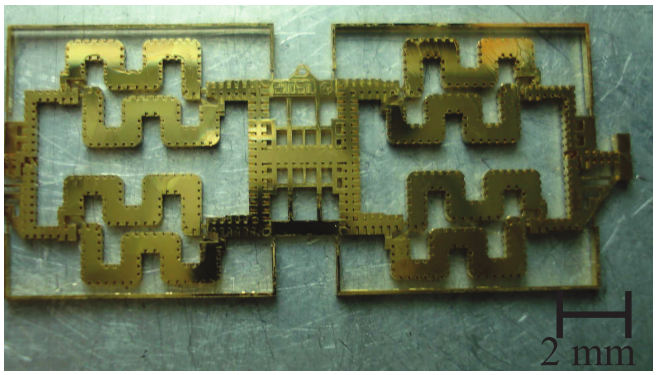


(b)

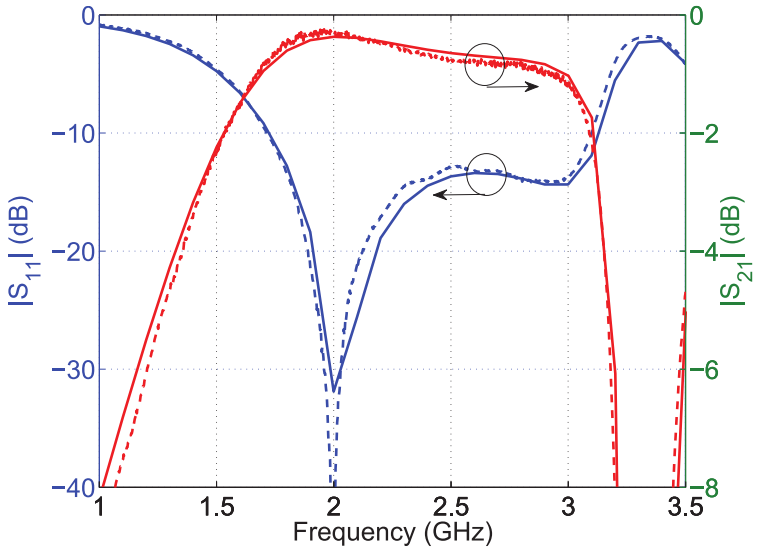
Figure B.5: (a) Photograph of the isolated microfabricated transformer with microcoaxial to CPW transition. A 1 mm wide cut in the center of the microstrip ground plane, so that the input and output microstrip grounds are connected inside the Vector Network Analyzer used for testing. (b) Transmission and return loss. Full-wave simulations are plotted in a dashed line.

CPW-to-microcoaxial transition is less than 20 dB up to 20 GHz.

The device is mounted onto a Rogers 4350 substrate ($\epsilon_r = 3.66$, thickness 790μm) for testing, as shown in Fig. B.5(a), and bonded with a silver epoxy, used here because of the low melting point of the dielectric straps ($\sim 180^\circ$C). The calibration in this case is a TRL set (Thru-Reflect-Line) built on the same microstrip substrate. The measured results are shown in Fig. B.5(b) and compared with full-wave simulations. The electrical contact between the CPW lines and the transformer is not ideal because of misalignment and nonuniformity in the epoxy layer, which caused an increased return loss compared to simulations. The mounted transformer 3-dB bandwidth covers the range from 900 MHz to 9.4 GHz.



(a)



(b)

Figure B.6: (a) Photograph of the fabricated back-to-back 50:25:50 Ω transformer prototype. (b) Measured transmission and return loss. Full-wave electromagnetic simulations are plotted in dashed lines.

B.4 Discussion and conclusion

The isolated transformers demonstrated above have bandwidth extending over a decade, low loss and dc isolation. While the isolated 1:1 transformers are useful for a number of wideband applications, other useful transformation ratios are possible as well. To demonstrate a compact 4:1 transformer with dc isolation, we used the 1:1 transformer as a basis as in Fig. B.1(c). A micro-coaxial back-to-back 50 Ω:25 Ω isolated TLT is shown in Fig. B.6(a) (a back-to-back configuration is used for testing with 50Ω CPW microwave probes). Measured results are shown in Fig. B.6(b) and compared with full-wave simulations. The transformer 3-dB

bandwidth covers more than one octave, from 1.3 GHz to 3.2 GHz. The agreement with simulations is within 0.2 dB. While in this topology miniaturization is achieved at the expense of bandwidth, dc-isolation, impedance transformation and decade-wide bandwidths can still be obtained for example by cascading the 1:1 isolated transformer with a micro-fabricated 1:4 Guanella transformer, such as the one described in [124].