Advanced electrified automotive powertrain with composite DC-DC converter

by

Hua Chen

B.Eng., The Chinese University of Hong Kong, 2010

M.S., University of Colorado Boulder, 2014

A thesis submitted to the

Faculty of the Graduate School of the

University of Colorado in partial fulfillment

of the requirements for the degree of

Doctor of Philosophy

Department of Electrical, Computer, and Energy Engineering

2016

This thesis entitled:
Advanced electrified automotive powertrain
with composite DC-DC converter
written by Hua Chen
has been approved for the Department of Electrical, Computer, and Energy Engineering

_____

Prof. Robert Erickson

_____

Prof. Dragan Maksimovic

Date _____

The final copy of this thesis has been examined by the signatories, and we find that both the content and the form meet acceptable presentation standards of scholarly work in the above mentioned discipline.

Chen, Hua (Ph.D., ECEE)

Advanced electrified automotive powertrain

with composite DC-DC converter

Thesis directed by Prof. Robert Erickson

In an electric vehicle powertrain, a boost dc-dc converter enables size reduction of the electric machine and optimization of the battery system. Design of the powertrain boost converter is challenging because the converter must be rated at high peak power, while efficiency at medium to light load is critical for the vehicle system performance. The previously proposed efficiency improvement approaches only offer limited improvements in size, cost and efficiency trade-offs.

In this work, the concept of composite converter architectures is proposed. By emphasizing the direct / indirect power path explicitly, this approach addresses all dominant loss mechanisms, resulting in fundamental efficiency improvements over wide ranges of operating conditions. The key component of composite converter approach, the DC Transformer (DCX) converter, is extensively discussed in this work, and important improvements are proposed. It enhances the DCX efficiency over full power range, and more than ten times loss reduction is achieved at the no load condition.

Several composite converter prototypes are presented, ranging from 10 kW to 60 kW rated power. They validate the concept of composite converter, as well as demonstrate the scalability of this approach. With peak efficiency of 98.5% to 98.7% recorded, the prototypes show superior efficiency over a wide operation range. Comparing with the conventional approach, it is found that the composite converter results in a decrease in the total loss by a factor of two to four for typical drive cycles. Furthermore, the total system capacitor power rating and energy rating are substantially reduced, which implies potentials for significant reductions in system size and cost.

A novel control algorithm is proposed in this work as well, which proves the controllability of the composite converter approach.

Dedication

To my father

Acknowledgements

The author would like to acknowledge the assistance, guidance, and support from my supervisors Professors Robert Erickson and Dragan Maksimovic. There knowledge in power electronics is unparalleled, and I have learnt invaluable lessons from their style of organizing and presenting technical materials. Without their supervision and encouragement, the completion of this thesis would not be possible.

I would also like to acknowledge the assistance from my committee members, Professors Khurram Afridi, David Jones, and Daniel Costinett, and thank them for agreeing to take their precious time to serve as my thesis committee.

In addition, I would like to thank Professor Alex Leung from the Chinese University of Hong Kong, who first introduced me into the world of electronics, and gave me useful professional advices throughout my career. I would like to thank Dr. Yanqi Zheng from Sun Yat-sen University, who led me to the wonderful field of power electronics. I would also like to thank Professor Lucy Pao from University of Colorado Boulder, who gave me the chance to explore different fields of engineering.

I would like to thank my colleagues in Colorado power electronics center (CoPEC) for their inspiring discussions. I would like to thank Mr. Kamal Sabi and Mr. Tadakazu Harada for their assistance at different stages of my research. I am especially grateful to the assistance from Mr. Hyeokjin Kim, whose diligence sometimes makes me abashed.

Finally, I would like to acknowledge both the financial and emotional support from my family. Especially I would like to thank the support and understanding from my wife Qian Jia throughout the years.

Contents

Chapter

Tables

Table

Figures

Figure

Chapter 1

Electrified Automotive Powertrain Overview

The fossil-based fuel has been the dominant energy source for transportation over the last century. However, as the number of vehicles growing rapidly, the related issues are becoming evident, such as green house gas emission, air pollution, and the danger of oil resources depletion in the near future. One solution is to improve the fuel economy, which include improve the internal combustion engine (ICE) efficiency, reduce the vehicle air drag, improve the transmission and wheel efficiency, and/or utilize the hybrid electric vehicle (HEV) technology. On the other hand, obviously, the more thorough solution is to find alternative sustainable energy sources, such as fuel cell electric vehicle (FCEV). Solutions such as battery-powered electric vehicle (BEV) or plug-in hybrid electric vehicle (PHEV) can either improve the fuel economy or as an alternative energy source solution, depending on how the electricity is generated. Other than improving the efficiency of the existing ICE-powered vehicle, all the other approaches (HEV, PHEV, FCEV, BEV) involves the electrified automotive powertrain, and they are referred as electric vehicle (EV) in general.

Although EV was invented early as in 1834 [17], it was quickly taken over by ICE-powered vehicles in the 19th century, due to the big breakthrough in ICE technology. The research and developments of power train electrification are revived since the 90s [16, 18], mainly due to environmental concerns, and government policies. For example, the California air resource board (CARB) passed the zero emission vehicle (ZEV) mandate in 1990, which required that by 1998, 2% of the vehicles sold in California to be ZEV, and this portion has to be increased to 10% by 2003. Since the late 90s, the modern HEVs debuted the automobile market [73]. HEVs are well accepted by the

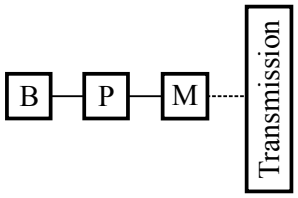
market, and their sales keep growing since then. It is predicted that by 2020, 20% of the annual vehicle sales are comprised by HEVs [81]. Nowadays many major automotive manufacturers such as Toyota, Honda, Ford, GM, and BMW, offer EV options in their production line.

However, there is still a long way to go in the EV development. Comparing with the conventional ICE-powered vehicle, the market share of HEV is still relatively small. On the other hand, in terms of sustainable energy, HEV is only an intermediate solution. The market acceptance of ultimate ZEV solutions, such as BEVs or FCEVs, is still not as good as expected. To further push the EV technology and expand the EV market, the industry is looking for future disruptive technologies that can further extend the vehicle drive range, improve the fuel economy, as well as reduce the production cost [68].

This chapter overviews the EV technology from a general perspective, and discusses about the requirements for the power electronics in the powertrain of EV, from the system point of view. Section 1.1 overviews different type of EV powertrain architectures. Section 1.2 gives brief descriptions on the functions of power electronics in electrified powertrain. In section 1.3, the specific power electronics characteristics in electrified powertrain applications are discussed. In section 1.4, a detailed electric vehicle powertrain model is introduced. Based on this model, several driving profiles in standard vehicle tests are simulated, and the load characteristics of the dc-dc converter for powertrain is extracted. These requirements serve as the basic guidance for all the designs in this work.

1.1 Powertrain architecture overview

Figure 1.1: Battery electric vehicle (BEV) powertrain architecture. B: battery, P: power electronics module, M: motor. Solid lines: electrical connection. Dotted line: mechanical connection.



All the vehicles involves traction systems, energy sources, and the power controls that regulate the power flow. In general, as long as electric system is involved in the powertrain, the vehicle can be regarded as electric vehicle (EV). As mentioned previously, based on different energy sources, the EVs can be categorized into different technologies, such as battery electric vehicles (BEV), hybrid electric vehicles (HEV), and fuel cell electric vehicle (FCEV). Different vehicles can adopt very different powertrain architectures. In this section, some basic architectures are reviewed.

1.1.1 Battery Electric Vehicle (BEV)

BEV utilizes battery as the only energy source, which has to be charged externally. If the charging electricity is generated from renewable energy sources, such as solar or wind power, the use of BEV leaves almost zero carbon footprint. However, even the electricity is generated from fossil-fuel based power plant, its carbon footprint is still much smaller than that of the traditional fossil-fuel based vehicle, because the energy conversion efficiency of the power plant is much higher than that of the vehicular ICE.

Similar to the miles-per-gallon (MPG) metric of the conventional ICE-powered vehicle, to quantify the energy consumption of BEV, the metric of miles-per-gallon-equivalent (MPGe) is introduced by the United States Environmental Protection Agency (EPA). The MPGe counts the vehicle energy consumption from the ac grid, and it is defined as:

$$1\,\text{MPGe} \approx 0.029\,67\,\text{miles/kWh} \tag{1.1}$$

The average combined fuel economy of the conventional ICE-powered vehicle made in 2016 is around 25 MPG, and even the most fuel economic vehicle has under 40 MPG. In contrast, the BEV can easily have more than 100 MPGe.

A typical battery electric vehicle (BEV) power train architecture is sketched in Fig. 1.1. Usually a single battery pack supplies the energy. The energy is processed by some power electronics unit to drive the electric motor. Because the electric motor can operate in a much wider speed / torque range than ICE, fixed gear ratio can be used in the transmission, which simplifies the

transmission design and improves the transmission efficiency. Some BEV uses two motors to drive front and rear wheels separately, which provides extra flexibility and mobility. Ideally four wheels can have independent motor drives, which even eliminates the need for differential gears.

In the early histories of BEV, dc machines are used as the traction motor, because it is very easy to control. In modern BEV, dc motor is rarely used due to the reliability issue of the electric brush. Instead, ac machines such as induction machine (IM) or permanent magnet synchronous machine (PMSM) are used. Comparing PMSM with IM, IM usually has simpler construction therefore costs less to build. However, it exhibits slightly lower efficiency comparing with PMSM, due to extra rotor winding loss. Because PMSM replaces rotor winding with permanent magnet, it usually has higher efficiency and higher power density. However, also because of the permanent magnet, PMSM is more expensive. Since most high performance permanent magnets require the use of rare earth element materials, the PMSM may also have larger price fluctuation in the future. There is also some interests in using switched reluctance machine (SRM) for traction, due to its ruggedness and high power density. However, because of the torque ripple at low speed, and the associating noise problem, currently its use is mainly limited in academic research phase.

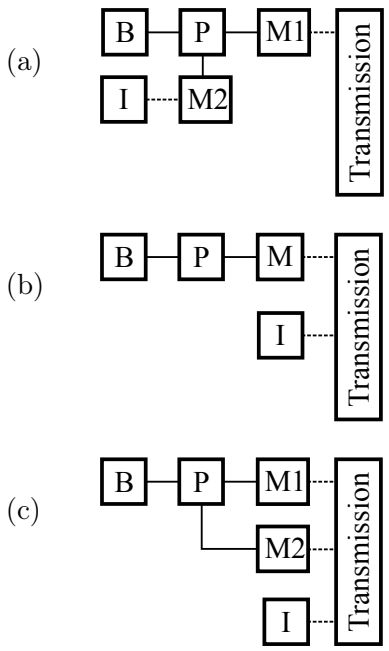
To convert the dc power from the battery pack to three phase ac power, a three-phase inverter is included in the power electronics module. More advanced architectures may incorporate a dc-dc converter to control the dc voltage supplied to the inverter. The advantage of the dc-dc converter is discussed in Section 1.2. Bidirectional power flow is usually required by the power electronics module, so that the vehicle is capable of regenerative brake, which means during the vehicle braking, instead of dissipating the vehicle kinetic energy as heat on the brake pad, the energy is partially or fully recycled back into the battery pack. The regenerative break is a distinctive feature of EV, comparing with ICE-powered vehicle.

The battery pack is composed many small battery cells connected in series and parallel. In contrast to the lead-acid batteries used in ICE-powered vehicles, in early 90s nickel-metal hydride (NiMH) battery was considered for BEV. Most of the modern BEV uses lithium-based battery technologies, such as lithium-ion (Li-ion) battery or lithium-polymer (LiPo) battery. A sophisticated

battery management system is required for safety protection, cell balancing, state-of-charge (SoC) and state-of-health (SoH) monitoring. An alternative technology of BEV is to use supercapacitor to replace the battery. Comparing with battery, supercapacitor has smaller energy capacity, but larger charging / discharging rate. Therefore, it is more suitable for electric bus applications, where the cruising distance from one charging station to another is short, while more acceleration and braking is required.

1.1.2 Hybrid Electric Vehicle (HEV)

Figure 1.2: Hybrid electric vehicle (HEV) powertrain architecture. B: battery, P: power electronics module, M: motor, I: internal combustion engine. Solid lines: electrical connection. Dotted line: mechanical connection.(a) series hybrid, (b) parallel hybrid, (c) series-parallel hybrid system.



Hybrid electric vehicle (HEV) refers to the type of system where the electric traction system is combined with ICE. The energy source of HEV is gasoline, and it is partially or fully converted to electric energy for traction. Comparing with the conventional ICE-powered vehicle, HEV has better fuel economy because:

(1) The ICE in HEV is only required to provide the average traction power, and the power

rating of the ICE is much reduced. Therefore, machines such as Artkinson cycle engine with lower power rating but higher efficiency are used in HEV.

(2) In HEV, the driving dynamics is more or less decoupled from ICE. Ideally ICE is only required to operate at one fixed efficiency-optimized operation point.

(3) HEV is capable of regenerative brake. The vehicle kinetic power is recycled during braking, instead of dissipated.

For example, the Toyota Prius 2016 has 52 combined-MPG.

There are many variations in the HEV powertrain architecture. For example, depending on how much electric power is involved in the traction powertrain, the HEV can be categorized into micro-hybrid, mild-hybrid, and full-hybrid technologies. As a matter of fact, by definition even the existing ICE-powered vehicle can be categorized as HEV, because it has to use the starter motor to start the ICE. Based on similar idea, the micro-hybrid vehicle uses electric motor to reduce the idling time of the ICE. In mild-hybrid vehicle, the electric powertrain is able to handle the regenerative brake. With increased electric traction power, in full-hybrid vehicle the ICE is only required to produce the average driving power, while the peak power is handled by the electric motor. Similar idea has been used in Formula One's race car, where electric motor is used for acceleration. To further increase the portion of the electric traction power to 100% enables the vehicle to operate in electric-only mode. Usually these HEVs allow charging from the grid, which are often referred to as plug-in hybrid electric vehicle (PHEV), or range-extended electric vehicle (REEV).

Depending on how the electric power and mechanical power is mixed, the basic HEV technology can also be categorized into series hybrid, parallel hybrid, and series-parallel hybrid systems. Figure 1.2 depicts different hybrid system structures. Figure 1.2(a) is the series hybrid structure. In series hybrid structure, the ICE provides the average traction power, which is converted to electric power through generator M2. The electric power charges the battery pack, which powers the traction motor M1. All the driving transient peak power and regenerative brake are buffered through M1 to the battery. Since the ICE is mechanically decoupled from the transmission, it can operate in

a fixed operation point with much lower power rating. Therefore, the ICE design is simplified, and its efficiency can be much improved. What is more, the mechanical couples between the ICE, motor, and transmission are also much simplified. However, because all the traction power is provided by the motor M1, the motor, its power electronics driver, and the battery pack have to be rated to the vehicle's peak power. One application of the series hybrid system is hybrid electric bus.

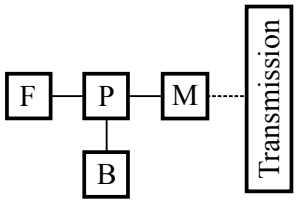
Figure 1.2(b) shows the parallel hybrid structure. In parallel hybrid configuration, both the ICE and the motor are directly coupled to the transmission. The average driving power is directly provided by ICE. While the transient power is lower than the average, the excess power flows from ICE to the motor M, and M operates in the generating mode to charge the battery. While the transient power is higher than the average, the motor M operates in the motoring mode, and the total traction power is the motor and ICE power combined. It is obvious that the parallel hybrid configuration requires a more complicated mechanical connection, usually a set of planetary gear. It also involves more sophisticated control of the power flow. However, comparing with the series hybrid configuration, the paralleled hybrid structure only requires on motor. What is more, the power rating of the motor, power electronics, as well as the battery pack can be reduced. An example of the parallel hybrid architecture is Honda's integrated motor assist (IMA) system.

Figure 1.2(c) shows the series-parallel hybrid system. Both motors / generators M1 and M2, as well as the ICE, are mechanically coupled to the transmission through some complicated mechanical connections, usually two sets of planetary gears. Usually the motor M2 operates in the generating mode, and motor M1 operates in the motoring mode. The system can be configured as either series or parallel hybrid. What is more, the motors M1, M2 and ICE can simultaneously provide driving power as well, leading to extra flexibility of the system. Toyota hybrid system (THS) as well as the GM hybrid system use series-parallel architecture.

1.1.3 Fuel Cell Electric Vehicle (FCEV)

Fuel cell electric vehicle (FCEV) uses electric energy generated from chemical reactions. Usually hydrogen fuel cell is used in FCEV, where the electricity is generated from the reaction of

Figure 1.3: Fuel cell electric vehicle (FCEV) powertrain architecture. F: fuel cell, B: battery, P: power electronics module, M: motor. Solid lines: electrical connection. Dotted line: mechanical connection.



compressed hydrogen with oxygen in the air, via the presence certain catalyst. FCEV only emits water and heat, and therefore is regarded as one type of ZEV. Though FCEV has less emission than HEV, its efficiency is still lower than that of BEV. On the other hand, currently the lack of hydrogen charging infrastructure is the main impediment of FCEV technology.

Figure 1.3 shows a typical FCEV architecture. Because the fuel cell has unidirectional power flow, usually a secondary power storage element, such as battery or supercapacitor, has to be deployed to handle regenerative brake.

1.2 Power electronics in electrified powertrain

Most EVs involve energy storage elements, such as battery, supercapacitor, or fuel cell, that stores the energy in dc. On the other hand, most of the traction motors operate with ac voltages. Therefore, certain power electronics modules have to process the power to perform the conversion between ac and dc. Typically, a three-phase inverter can be used to drive the PMSM or IM motor. Some commercial EVs such as Tesla model S and Chevy Volt directly connects the inverters to the battery pack. However, in this case, the inverter can only produce line-to-line voltages that are less or equal to the input voltage. Therefore, in those vehicles, the motor line-to-line voltages are limited by battery pack voltage, which changes at different operation conditions. On the other hand, the maximum battery pack voltage is physically limited, usually under 400 V.

Recent developments have shown that by inserting a dc-dc converter between the battery pack and inverter, the powertrain performance can be further improved. The motor-drive dc bus

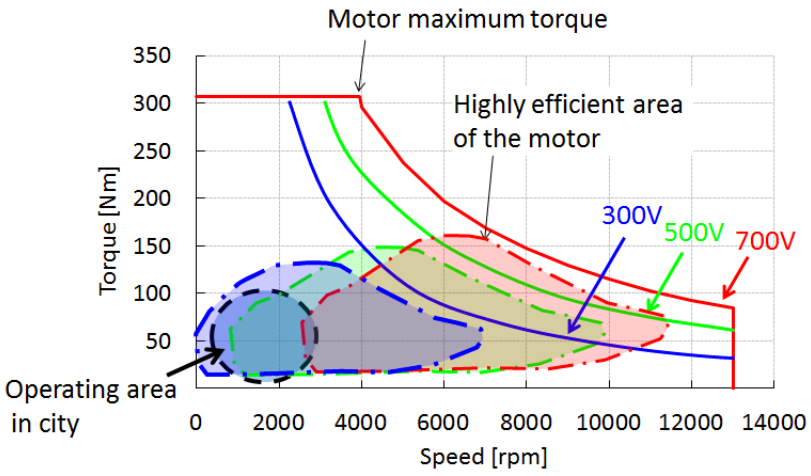
voltage can be increased, which allows extensions of the motor speed range without field weakening. This improves both the motor and the inverter efficiency [14]. It also allows the system to utilize high speed motors with reduced size. For example, the THS II system used in Toyota's 2005 large SUV utilizes boost converter to boost the dc bus voltage from 274 V to 650 V, and adopts high speed motor design. It results in more than four times geometric power density increase, comparing with Prius 2000 which equipped the THS I system [53]. The converter can also dynamically adjust the dc bus voltage, so that the system efficiency can be further optimized [8, 34, 41]. For example, Fig. 1.4 shows the 2014 Honda Accord plug-in high efficiency operation area from [41]. At higher dc bus voltage, the motor is more efficient at higher speed. From the system design perspective, the boost dc-dc converter also enables independent optimization of the battery system and battery pack size and cost reduction [62, 74].

On the other hand, with a varying dc bus voltage provided by the dc-dc converter, the motor driver may also utilize different modulation schemes. For example, the six-step inverter modulation scheme, to which is sometimes also referred as pulse-amplitude modulation (PAM), is well known to improve both the inverter and motor efficiency, because of much reduced switching frequency and current ripple. However, because it lacks one degree of freedom, with a fixed dc bus voltage, it can only operate in high speed where field weakening is applied. If a buck-boost type dc-dc converter is deployed, the operation range of the six-step modulation can be extended all the way to zero speed. Even with a boost type dc-dc converter, the six-step modulation range can be much extended, and the combined powertrain efficiency can be notably improved as well.

The powertrain architecture using a dc-dc converter has been successfully incorporated in commercial vehicle systems from automakers like Toyota, Honda and Ford, which covers over 80% sales of the HEV market. Although manufacturers such as GM and Tesla Motor adopts alternative technology paths, the dc-dc converter in the powertrain is no doubt the dominant technology of the market.

Though the dc-dc converter improves the powertrain performance, the converter itself introduces extra losses as well. The losses associated with the dc-dc converter must be sufficiently low,

Figure 1.4: The high efficiency operation area of the motor in Honda Accord 2014 PHEV, under different bus voltages, from [41].



to not compromise the advantages offered by the boost converter. Designing a high efficiency boost converter in this application is challenging. This work mainly focuses on designing high efficiency boost converter with reduced converter size and cost.

In this work, a typical electric vehicle powertrain architecture as shown in Fig. 1.5 is considered. The battery voltage may vary from 150 V to 300 V, and the boost converter controls the dc bus voltage up to 800 V. For BEV, only single motor inverter is connected at the dc bus. For HEV structures depicted in Fig. 1.2, two inverters are connected at the dc bus for both motor and generator. Some vehicles, such as Toyota Highlander hybrid SUV with 4-wheel-drive, have three inverters connected at dc bus, for two motors and one generator.

1.3 Powertrain application characteristics

In vehicular powertrain applications, the system is typically thermally limited. For example, in BEV, the worst case ambient temperature can be 85 °C, and the worst case coolant temperature of the liquid cooling system can be 75 °C. In HEV, the ambient temperature can be as high as 105 °C to 125 °C, depending on whether the location of concern is close to transmission or not. If the power electronics module in HEV shares the same liquid cooling loop as the ICE, the maximum coolant temperature can be 105 °C. On the other hand, the typical maximum operation

Figure 1.5: Typical electric vehicle powertrain architecture

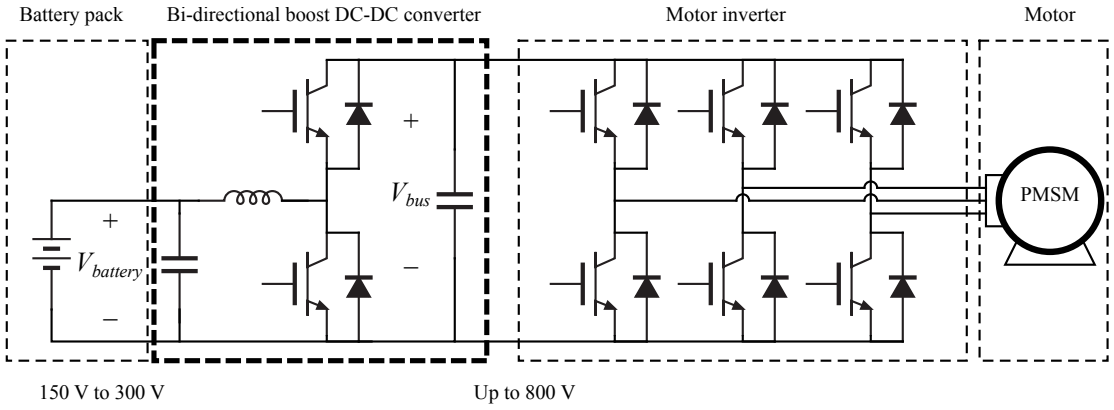
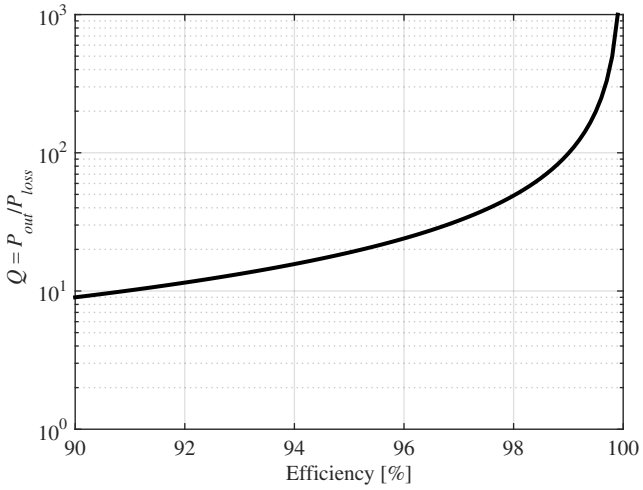


Figure 1.6: Converter quality factor $Q = P_{out}/P_{loss}$ metric vs. efficiency η.



temperature for power electronics components is around 105 °C to 150 °C. Therefore, for a given thermal management design, the allowed average power loss is limited. For such systems, the ratio of output power to power loss

$$Q = \frac{P_{out}}{P_{loss}} = \frac{\eta}{(1-\eta)} \tag{1.2}$$

presents a more meaningful performance metric than efficiency η. By analogy with the quality factor of a reactive element, we define Q of a power converter as the ratio of loss to output power. Fig. 1.6 shows the $Q = P_{out}/P_{loss}$ metric as a function of power efficiency. For example, if the system average efficiency is improved from 96% to 98%, the system average efficiency is improved by just 2%, which appears to be incremental. However, P_{out}/P_{loss} is more than doubled, which means

that the system output power can be doubled given the same thermal management design, or that the same output power can be processed while the system cooling effort can be halved, indicating substantial non-incremental system-level improvements. High efficiency power electronics not only improves the system average efficiency such as MPGe, but also increases the power density and significantly reduces the size and cost of the thermal management system.

In traditional power electronics applications, converter efficiency at full power is often critical. However, in electric powertrain applications, converter efficiency at intermediate and low power levels is actually more important. As an example, Fig. 1.7(a) shows the NREL ADVISOR [101] simulation result for a Ford Focus electric vehicle under different standard Dynamometer Drive Schedules (DDS) specified by the United States Environmental Protection Agency (EPA) [1]. The Urban Dynamometer Drive Schedule (UDDS) is a relatively light load test that represents city driving conditions. The Highway Fuel Economy Test (HWFET) is a highway driving cycle with maximum 60 mph speed. US06 is a supplemental test procedure, which includes fast acceleration events in an aggressive driving cycle. Figure 1.7(b) shows the corresponding distribution of the normalized vehicle power. As shown in Fig. 1.7(b), even in the most aggressive US06 driving profile, most of the time the vehicle operates at less than 40% of its maximum power.

1.4 Modeling of electrified traction systems

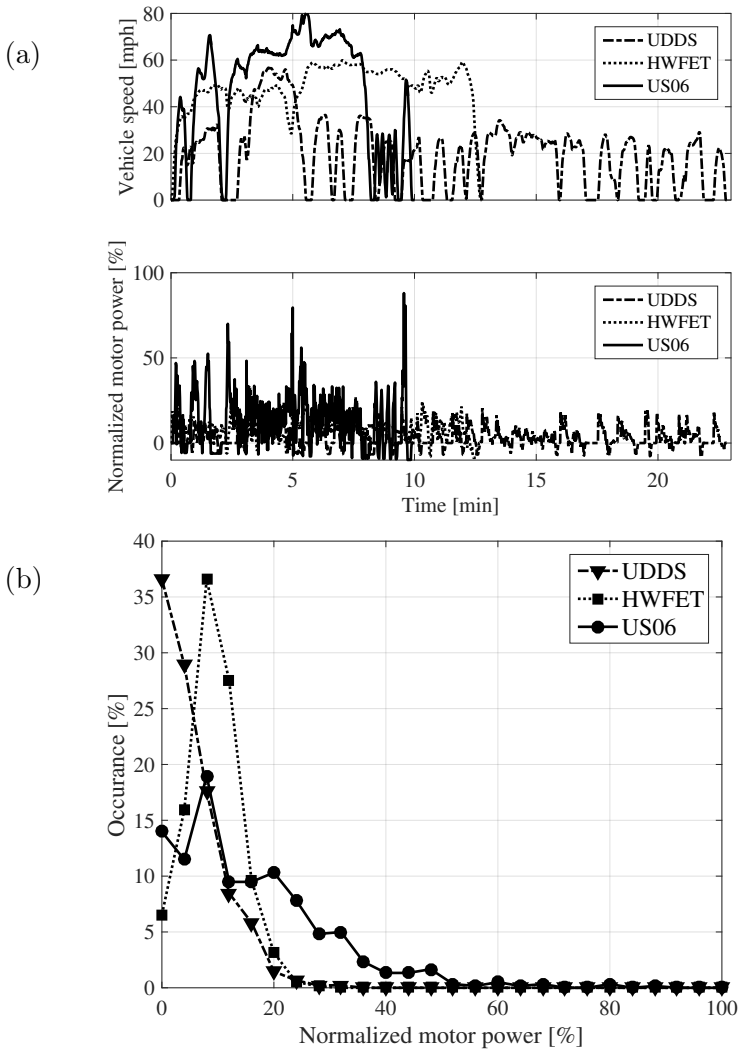
To further understand the load characteristics of the dc-dc converter for powertrain application, it is necessary to model the behavior of the traction system. The model of the traction system, as a load for the dc-dc converter, is composed of three parts: the model of vehicle, motor, and motor drive.

1.4.1 Vehicle model

The basic model of the vehicle follows Newton's second law, that is

$$M_v \dot{v} = F_{drv} - F_{res}, \tag{1.3}$$

Figure 1.7: Simulation of a typical Ford Focus electric vehicle with NREL ADVISOR simulator: (a) vehicle speed and normalized power vs. time; (b) vehicle normalized power histogram.



where M_v is the curb weight of the vehicle, plus the mass of all the cargo and passengers, v is the vehicle speed, and F_{drv} is the driving force. The resistance force F_{res} is composed of several factors. In this work, only three major factors are considered, which are air drag force F_{air}, rolling resistance F_{roll}, and gravity force F_g due to the incline.

$$F_{res} = F_{air} + F_{roll} + F_g. \tag{1.4}$$

The air drag force is approximately proportional to the square of speed v:

$$F_{air} = \frac{1}{2}\rho_{air} C_d A_v v^2, \tag{1.5}$$

where ρ_{air} is the density of air, A_v is the front area of the vehicle, and C_d is the air drag coefficient. The rolling resistance is approximately proportional to the vehicle speed v:

$$F_{roll} = M_v g C_r \left|v\right|, \tag{1.6}$$

where C_r is the rolling resistance coefficient, and g is the gravity acceleration. The gravity force F_g is

$$F_g = M_v g \sin(\theta_g), \tag{1.7}$$

where θ_g is the grade of the road. F_{drv}, the driving force of the vehicle, is linked to the torque on the wheel T_w via:

$$F_{drv} = \frac{T_w}{r_w}, \tag{1.8}$$

where r_w is the radius of the wheel. The wheel is coupled to the electric motor through differential gears and a transmission gear. Unlike ICE, the electric motor is capable of variable speed driving over a wide speed range. Therefore, fixed gear ratio is sufficient for the electric vehicle. With fixed gear ratio $G_r : 1$, and ignoring the loss of the gears, the relationship between wheel and motor is:

$$T_w = T_m G_r \tag{1.9}$$

$$\omega_m = \omega_w G_r, \tag{1.10}$$

where $\omega_w = v/r_w$ is the angular speed of the wheel. T_m and ω_m are the torque and mechanical speed of the motor.

1.4.2 Electric machine model

Permanent Magnet Synchronous Machine (PMSM) is one of the most popular choices as the traction motor for electric vehicles. The PMSM model can be much simplified if modeled from the

d-q axis [59]:

$$\begin{bmatrix} \dot{i_q} \\ \dot{i_d} \end{bmatrix} = \begin{bmatrix} -\frac{R_q}{L_q} & -\omega_e \frac{L_d}{L_q} \\ \omega_e \frac{L_q}{L_d} & -\frac{R_d}{L_d} \end{bmatrix} \begin{bmatrix} i_q \\ i_d \end{bmatrix} + \begin{bmatrix} \frac{v_q - \omega_e \lambda_{af}}{L_q} \\ \frac{v_d}{L_d} \end{bmatrix}. \tag{1.11}$$

Here $R_{q,d}$ and $L_{q,d}$ are the armature winding resistance and inductance, seen from the quadrature-axis and direct-axis, respectively. λ_{af} is the rotor flux linkage due to the presence of the permanent magnets. ω_e is the electrical frequency of the motor, and

$$\omega_e = \frac{P}{2}\omega_m, \tag{1.12}$$

where P is the number of poles of the motor. $i_{q,d}$ and $v_{q,d}$ are the stator current and voltage after the abc–qd0 transform:

$$\boldsymbol{i_{qd0}} = \boldsymbol{T_{abc}} \boldsymbol{i_{abc}} \tag{1.13}$$

$$\boldsymbol{v_{qd0}} = \boldsymbol{T_{abc}} \boldsymbol{v_{abc}}, \tag{1.14}$$

and

$$\boldsymbol{T_{abc}} = \frac{2}{3} \begin{bmatrix} \cos(\theta_e) & \cos\left(\theta_e - \frac{2}{3}\pi\right) & \cos\left(\theta_e + \frac{2}{3}\pi\right) \\ \sin(\theta_e) & \sin\left(\theta_e - \frac{2}{3}\pi\right) & \sin\left(\theta_e + \frac{2}{3}\pi\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}, \tag{1.15}$$

where θ_e is the electrical position of the motor. The torque of the motor is calculated as

$$T_m = \frac{3P}{4} \cdot \left(\lambda_{af} i_q + \left(L_d - L_q\right) i_q i_d\right). \tag{1.16}$$

Notice that the torque equation consists of two terms. The first term indicates the torque contribution from the permanent magnet, while the second term indicates the torque contribution from the reluctance of the rotor. The motor with surface mount (SM) magnets is usually non-salient, which means $L_d = L_q$. Therefore, SM motor does not have reluctance torque. On the contrary, for high speed traction motor, usually interior mount (IM) magnets are preferred, where usually $L_d < L_q$, due to the low permeability of the magnet. Some traction system, such as that in the second generation Chevy Volt design [52], particularly enhances the reluctance torque, thus to reduce the usage of magnets and therefore to lower the cost of the machine.

1.4.3 Motor drive and dc bus voltage control

The inverter controls the motor winding current. There are various motor control algorithms, such as constant torque angle control, constant mutual flux linkage control, optimum torque-per-ampere control, and unity power factor control. In this work, only the constant torque angle control is considered due to its simplicity. With constant torque angle control, $i_d = 0$, therefore the torque angle $\delta = 90°$. For a given speed ω_m, because $i_d = 0$, the inverter output voltage is maximized, and the inverter output current is therefore minimized. Of course, at very high speed, the required inverter output voltage may exceed the maximum bus voltage allowed, and field weakening is required. The field weakening operation increases the torque angle δ, therefore $i_d < 0$, and the required bus voltage is reduced. At the operation of field weakening, the normalized stator voltage amplitude $v_{sn} = \sqrt{v_{dn}^2 + v_{qn}^2}$ is fixed. Here the variables with subscript n are normalized to the per-unit (p.u.) system. Because

$$v_{sn}^2 = \omega_{en}^2 \left(L_{qn}^2 \left(i_{qn}^2 - i_{dn}^2 \right) + \left(1 + L_{dn} i_{dn}^2 \right) \right), \tag{1.17}$$

for a salient machine ($L_d < L_q$), with given stator current amplitude $i_{sn} = \sqrt{i_{dn}^2 + i_{qn}^2}$, the torque angle δ can be solved as

$$\delta = \tan^{-1}\left(\frac{i_{qn}}{i_{dn}}\right) = \cos^{-1}\left(\frac{-1 \pm \sqrt{\left(1 - \left(\frac{L_{qn}}{L_{dn}}\right)^2\right)\left(L_{qn}^2 i_{sn}^2 + 1 - \frac{1}{\omega_{en}^2}\right)}}{\left(1 - \left(\frac{L_{qn}}{L_{dn}}\right)^2\right) L_{dn} i_{sn}} \right). \tag{1.18}$$

The valid result takes either plus or minus sign in the equation, whichever leads to a real angle in the second quadrant.

As shown in Fig. 1.5, the three-phase inverter used in the powertrain is a buck-derived inverter. Therefore, the voltage that can be produced by each phase of the inverter ranges from zero to the dc bus voltage V_{bus}. In another word, there is a lot of freedom in the choice of the dc bus voltage V_{bus}, as long as $V_{bus} \geq \sqrt{3\left(v_d^2 + v_q^2\right)}$, and space-vector pulse width modulation (SVPWM) is assumed. However, in practice, if V_{bus} keeps very high at low speed, the inverter has to operate with small modulation index, where the inverter efficiency is low. To improve the inverter efficiency, in this

work it is assumed that the inverter modulation index is maximized, that is:

$$V_{bus} = \max\left(V_{battery}, \sqrt{3\left(v_d^2 + v_q^2\right)}\right) \tag{1.19}$$

The dc-dc converter is assumed to be a boost converter instead of a buck-boost converter, therefore the minimum dc bus voltage is limited to the battery voltage. With this dc bus voltage control scheme, as long as the dc bus voltage is higher than the battery voltage, the inverter has unity modulation index. In that case, the inverter only requires the degree-of-freedom of two. Therefore, at any time, only two phases are required to switch, and the inverter switching loss is reduced by 33%.

1.4.4 Electrified traction system simulation

Table 1.1: A typical mid-size sedan vehicle model parameters

M_v	A_v	r_w	G_r	C_d	C_r	θ_g	ρ_{air}
2000 kg	2.2 m^2	0.334 m	8.62	0.28	0.01	0°	1.204 kg m^{-3}

To characterize the requirement of the dc-dc converter, a simulation model is built based on equations (1.3) – (1.19). A typical mid-sized sedan is modeled, with the model parameters summarized in Table 1.1. A typical 60 kW 16-pole salient traction motor is modeled, based on parameters extracted from Toyota Prius 2010, as summarized in Table 1.2. This simplified model ignores the copper loss and iron loss of the motor. Comparing to the vehicle mass and rolling resistance, the rotor mass and rotation friction of the motor is ignored as well. The maximum motor voltage is limited by the insulations of the stator winding, which determines the maximum dc bus voltage $V_{bus,max}$ as well. The battery pack is assumed to have a typical voltage of 200 V.

Table 1.2: A typical traction PMSM model parameters

P_{max}	Pole	L_d	L_q	R_d	R_q	λ_{af}	V_{max}
60 kW	16	100 µH	900 µH	0	0	0.633 V s	800 V

Figure 1.8: Modeled traction powertrain with US06 driving profile.

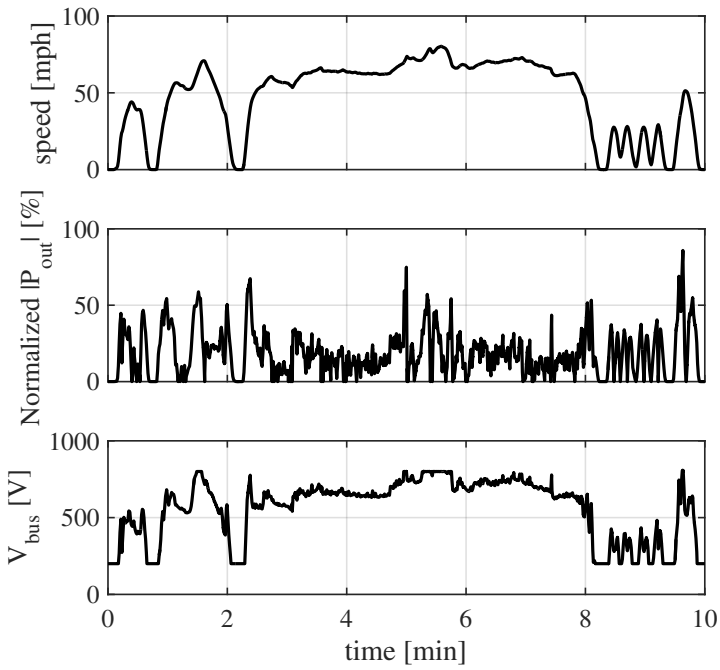


Figure 1.8 plots the simulated powertrain power and dc bus voltage with standard US06 driving profile. Although around 80% peak power is recorded, most of the time the system operates at around 20% power level, which agrees with the simulation results by ADVISOR in Fig. 1.7. At low speed, the bus voltage V_{bus} is at the 200 V battery voltage. As the vehicle speed increases, the bus voltage increases as well. At round $t = 5.5$ min, the bus voltage reaches the maximum 800 V, and the inverter operates in field weakening mode.

To further understand the relationship between system power and dc bus voltage, Fig. 1.9–1.11 show the bus voltage and system power probability distributions for the three simulated driving cycles. The one-dimensional probability density functions (PDF) for the bus voltage and output power are shown as well. In the UDDS driving cycle, the bus voltage is mostly confined to the range 200 V to 300 V, with output power less than 10% of maximum, due to the low-speed urban driving pattern. With the HWFET driving cycle, bus voltage is mostly in the range 400 V to 600 V, with output power approximately 10%; this corresponds to cruising at relatively high speed. Under the US06 driving cycle, the bus voltage is mostly in the range 600 V to 800 V, with output power

Figure 1.9: V_{bus} and normalized $|P_{out}|$ probability distribution in simulated UDDS driving cycle.

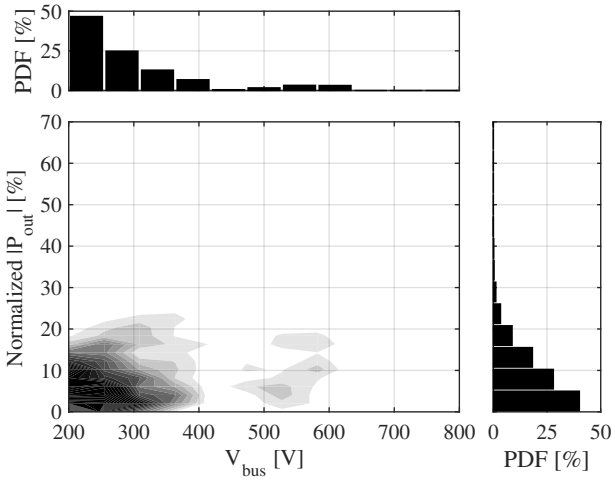
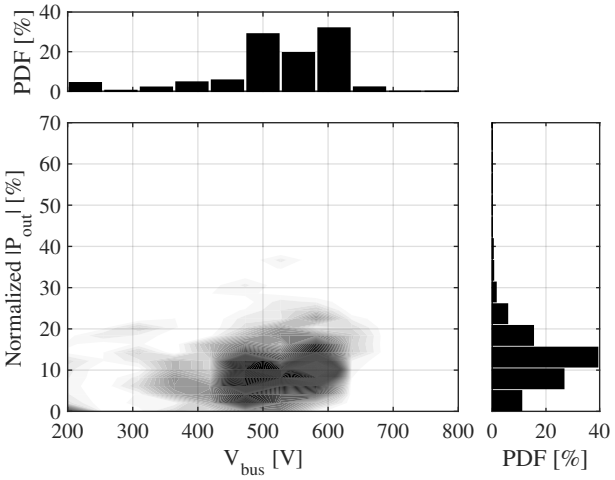


Figure 1.10: V_{bus} and normalized $|P_{out}|$ probability distribution in simulated HWFET driving cycle.



approximately 20%, although a peak power exceeding 70% is recorded, and significant trajectories of proportional bus voltage and output power are caused by the many accelerations and decelerations of the US06 cycle.

The voltage-power relationships illustrated by Fig. 1.9–1.11 serve as design guidelines for the discussion in following chapters.

Figure 1.11: V_{bus} and normalized $|P_{out}|$ probability distribution in simulated US06 driving cycle.

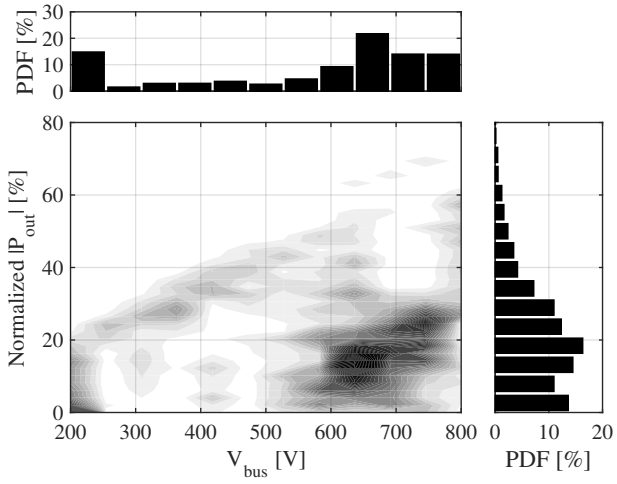


Table 1.3: Converter quality factor Q comparison between the composite D converter and the conventional boost converter, under standard driving cycles

	UDDS	HWFET	US06
Conventional boost	38.6	17.5	21.9
Composite D	74.5	75.2	67.1

This work focuses on novel approaches that significantly improve the electrified powertrain efficiency and size, which eventually will not only improve the vehicle fuel economy, but more importantly, lead to notable vehicle cost reduction. Chapter 2 reviews the conventional boost converter approaches, as well as various existing arts that try to reduce different losses in the conventional approach. It is found that some of them only lead to incremental improvements, while others have to trade performance with the size and cost of the system. Chapter 3 introduces the philosophy of composite converters, which is the main contribution of this work, and talks about several potential architectures. It is found that one of the composite converter structure, composite D converter, can reduce the average loss under standard driving profiles by a factor of two to four, as shown in Table 1.3, while achieving 40% capacitor size reduction at the same time. Chapter 4 gives more details of DC Transformer (DCX) converter, which is the core module in composite converter approach. A novel efficiency-enhanced control algorithm is proposed, which improves the DCX

efficiency over all power range, and ten times loss reduction is achieved at light load conditions. The detailed implementation is documented in Chapter 5, and Chapter 6 discusses some preliminary control ideas of composite converters. This work is concluded in Chapter 7, with possible future directions of composite converter technology.

Chapter 2

Boost DC-DC Converter Technology Overview

This chapter surveys the existing technologies of boost dc-dc converter, for the application of electrified traction powertrain. The conventional boost converter is reviewed in section 2.1, with extensive discussions on the loss mechanisms of the converter. To overcome the limitations of the conventional boost converters, several existing alternative approaches are discussed in section 2.2 – 2.4. Section 2.5 reviews the impedance-source (or Z-source) inverter, which combines the function of the boost converter and inverter into one stage.

2.1 Conventional boost converter

Boost converter is one of the most fundamental switched-mode power converters that can achieve the output voltage higher than the input. The operation principle as well as its loss mechanisms are reviewed in this section.

2.1.1 Conventional boost converter operation

Figure 2.1 shows the power stage of a conventional boost converter, realized with IGBT devices. To handle the bi-directional power flow, which is required in traction powertrain application for regenerative brake, the switches Q_1 and Q_2 are realized with an IGBT device together with an anti-parallel diode. If only unidirectional power flow is required, Q_1 can be realized with a single IGBT device, and Q_2 can be realized with a single diode device.

The switches Q_1 and Q_2 turn on alternatively to chop the inductor current I_{in}, with a switch-

Figure 2.1: Conventional bi-directional boost converter realized with IGBT

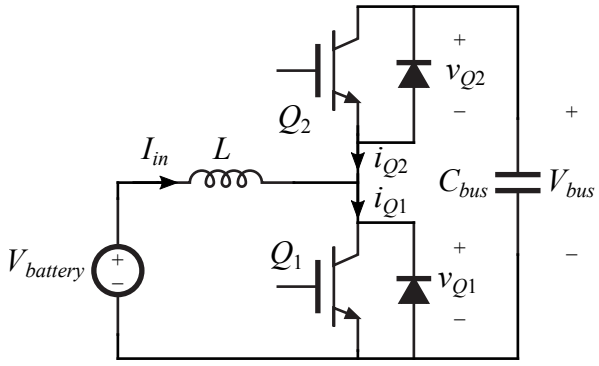
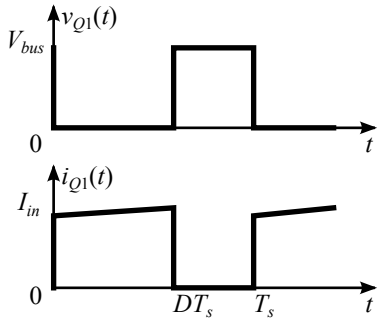


Figure 2.2: Switch Q_1 voltage and current waveforms



ing period T_s. In convention, the turn on duty cycle of switch Q_1 is defined as D. The switch Q_1 voltage and current waveforms are sketched in Fig. 2.2.

If the output capacitor C_{bus} is sufficiently large, one may ignore the output voltage ripple, and assume the output voltage V_{bus} is constant. Under this assumption, the average voltage across the switch Q_1 is:

$$\langle v_{Q_1} \rangle = (1 - D)\, V_{bus} = D' V_{bus}, \tag{2.1}$$

where $D' = 1 - D$. The angle brackets that are around v_{Q1} denote the average operation.

Because at steady-state, the inductor L is equivalent to a short circuit, the averaged voltage across the inductor should be zero. Therefore,

$$V_{battery} = \langle v_{Q_1} \rangle = D' V_{bus}. \tag{2.2}$$

Thus, the voltage conversion ratio M of the boost converter can be derived:

$$M = \frac{V_{bus}}{V_{battery}} = \frac{1}{D'}. \tag{2.3}$$

The voltage conversion ratio M in (2.3) is solely controlled by the duty cycle command D (or D'). The range of duty cycle D is $0 \leq D \leq 1$, therefore the boost converter can achieve $M \geq 1$. To control the output voltage V_{bus}, the pulse-width modulation (PWM) can be used to modify the duty cycle.

Notice that (2.3) is the ideal relationship between voltage conversion ratio and duty cycle, under the assumption that the output voltage ripple is small, and the system is loss-free. In practice, due to the lossy element in the converter, the voltage conversion ratio M is also a function of output power. In practice, usually the duty cycle D is adjusted with some feedback control to reduce the output impedance of the converter. What is more, due to the loss in the system, the maximum voltage conversion ratio that the system can achieve is always limited.

2.1.2 Boost converter loss model

The switched-mode power converters are composed of semiconductor devices, magnetics, and capacitors, and loss is associated with each component.

For semiconductor devices loss is composed of conduction loss and switching loss. The conduction loss is due to the voltage drop across the device, and it is independent of the switching frequency. When minority-carrier devices such as IGBT, BJT, or diode turn on, they can be modeled as a voltage source V_q in series with a resistor R_q, that is,

$$v = V_q + iR_q, \tag{2.4}$$

where v is the voltage across the device, and i is the current flowing through the device. For BJT or IGBT, $V_q = V_{ces}$, which is the collector-to-emitter saturation voltage. For diode, $V_q = V_f$, which is the diode forward drop voltage. The majority-carrier devices such as MOSFETs can be modeled as a resistor R_q when they turn on, that is.

$$v = iR_q \tag{2.5}$$

Given the device current waveform $i(t)$ within a switching period T_s, the conduction loss of the device can be calculated as

$$P_{cond} = \frac{1}{T_s} \int_0^{T_s} v\left(i\left(t\right)\right) i\left(t\right) \mathrm{d}t. \tag{2.6}$$

The semiconductor device switching loss is mainly due to the device output capacitance as well as the diode reverse-recovery charge. Various methods have been proposed to model the device switching loss. For example, in reference [56], the analytical expression of the detailed waveform at the switching instance is derived to calculate the switching loss, in which requires parameters such as the gate driver strength and diode minority-carrier lifetime. On the other hand, many device manufacturers provide the curve of the switching loss in the data sheet, and the switching loss can be approximated with the following equation:

$$P_{sw} = K I_{on}^{a} V_{off}^{b} f_{sw}, \tag{2.7}$$

where I_{on} is the device turn-on current, V_{off} is the device blocking voltage in off-state, and f_{sw} is the switching frequency. Parameters K, a, and b can be obtained by fitting the curve of switching loss in the data sheet.

The magnetic loss is composed of the winding copper loss and the core loss. Copper loss is due to the copper winding resistance. The copper winding dc resistance R_{dc} can be calculated as

$$R_{dc} = \rho_c \frac{N \cdot MLT}{A_w}, \tag{2.8}$$

where ρ_c is the copper resistivity, which is a function of temperature. N is the number of turns, and MLT is the mean-length-per-turn of the given core, and A_w is the wire cross section area. Therefore, the copper loss due to dc resistance in a boost converter is

$$P_{cu,dc} = I_L^2 R_{dc} \tag{2.9}$$

where $I_L = I_{in}$, which is the averaged inductor current.

The inductor in a boost converter carries an ac current ripple as well. The amplitude of the current ripple is

$$\Delta i_L = \frac{V_{battery} D}{2 L f_{sw}}. \tag{2.10}$$

Because of skin effect and proximity effect, the winding of the inductor has higher ac equivalent resistance $R_{ac} = F_R R_{dc}$ [33]. The ac copper loss is calculated as

$$P_{ac} = F_R I_{rms}^2 R_{dc}. \tag{2.11}$$

For non-sinusoidal waveform, the power loss of each harmonic can calculated separately, and the total ac copper loss is the sum of the power loss in each harmonic.

The proximity effect factor F_R can be calculated with Dowell's equation [30, 33], which is the solution of the 1-D Maxwell equation.

$$F_R = \frac{\varphi}{M} \sum_{i=1}^{M} \left(m_i^2 \left(2G_1 \left(\varphi \right) - 4G_2 \left(\varphi \right) \right) - m_i \left(2G_1 \left(\varphi \right) - 4G_2 \left(\varphi \right) \right) + G_1 \left(\varphi \right) \right), \tag{2.12}$$

where

$$G_1 \left(\varphi \right) = \frac{\sinh \left(2\varphi \right) + \sin \left(2\varphi \right)}{\cosh \left(2\varphi \right) - \cos \left(2\varphi \right)}, \tag{2.13}$$

and

$$G_2 \left(\varphi \right) = \frac{\sinh \left(\varphi \right) \cos \left(\varphi \right) + \cosh \left(\varphi \right) \sin \left(\varphi \right)}{\cosh \left(2\varphi \right) - \cos \left(2\varphi \right)}. \tag{2.14}$$

The factor φ is given by

$$\varphi = \sqrt{\eta} \sqrt{\frac{\pi}{4}} \frac{d}{\delta}, \tag{2.15}$$

where d is the wire diameter, and η is winding porosity, which is typically between 0.8 and 1. δ is the skin depth, and

$$\delta = \sqrt{\frac{\rho_c}{\pi \mu_0 f}}, \tag{2.16}$$

where μ_0 is the vacuum permeability, and f is the frequency of the harmonic considered. In equation (2.12), M is the total number of winding layers, and the quantity m_i is the ratio of the ith layer magneto-motive force (MMF) to the ith layer ampere-turns.

In inductor design, to increase the energy capacity of the inductor so that is can handle certain maximum current level I_{max}, it is common to add air gap to the core. The gap length ℓ_g is given by

$$\ell_g = \frac{\mu_0 L I_{max}^2}{B_{max}^2 A_c}, \tag{2.17}$$

where A_c is the cross-section area of the core.

Around the air gap, the magnetic flux is no longer confined in the core. If the air gap is large, or the winding is close to the air gap, the fringing flux may affect the winding current, which further increases the ac copper loss. Since the loss mechanism of fringing effect is essentially the same as that of proximity effect, the ac copper loss of gapped inductor can be calculated as

$$P_{ac} = (1 + F_{fr})\, F_R I_{rms}^2 R_{dc}, \tag{2.18}$$

where F_{fr} is the fringing factor.

Regarding the core loss, in some literature, it is explained by two main loss mechanisms [33]: the hysteresis (static) power loss, and eddy current (dynamic) power loss. The hysteresis power loss is due to the hysteresis behavior of the magnetic material's B-H loop, and it is proportional to frequency f. The eddy current loss is due to the induced eddy current in the magnetic material, and it is proportional to f^n, where usually $n \geq 2$. Combining two loss mechanism, the famous Steinmetz equation [33, 90] is commonly used to model the core loss:

$$P_{fe} = V_e K_{fe0} f^{\alpha} \left(\Delta B\right)^{\beta}, \tag{2.19}$$

where V_e is the equivalent core volume, f is the frequency, ΔB is the ac amplitude of the flux density, and K_{fe0}, α, β are the curve-fitting Steinmetz parameters. The frequency exponent parameter α is usually between 1 and 3, while the flux exponent β is usually between 2 and 3. The Steinmetz equation is preferred in practical power electronics loss modeling, because the parameters can be directly obtained from manufacturer's data sheet.

However, the Steinmetz equation only applies to magnetic flux $B(t)$ with sinusoidal waveform, and which is not the case in the inductor of boost converter. The magnetic flux $B(t)$ of the inductor in boost converter is

$$B(t) = \frac{L i_L(t)}{N A_c}, \tag{2.20}$$

where N is the inductor winding number of turns, and A_c is the inductor core cross section area.

In Steinmetz equation (2.19), $\beta > 2$. Therefore, it is a nonlinear equation, and harmonic superposition with Fourier series (such as in [39]) is not mathematically valid. As demonstrated

in [3], it underestimates the core loss with non-sinusoidal waveform flux density. There have been extensive researches on the core loss prediction with non-sinusoidal waveform flux density. Reference [40] pointed out that "there is no obvious physical distinction to be made between the static or hysteresis loss and the dynamic or eddy-current loss". The core loss is directly related to the magnetization velocity $\mathrm{d}M/\mathrm{d}t$, which is proportional to $\mathrm{d}B/\mathrm{d}t$. Based on this idea, various methods have been proposed, such as Modified Steinmetz Equation (MSE, [82]), Generalized Steinmetz Equation (GSE, [67]), and Improved Generalized Steinmetz Equation (iGSE, [99]). Among these methods, iGSE shows better agreement with measurement over a wide range, and only requires the Steinmetz parameters, which can be directly obtained from the manufacturers' data sheet. The iGSE method predicts that the core loss P_{fe} is:

$$P_{fe} = V_e \frac{1}{T_s} \int_0^{T_s} K_{fei} \left| \frac{\mathrm{d}B}{\mathrm{d}t} \right|^{\alpha} (\Delta B)^{\beta-\alpha} \, \mathrm{d}t, \tag{2.21}$$

and

$$K_{fei} = \frac{K_{fe0}}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^{\alpha} \, 2^{\beta-\alpha} \mathrm{d}\theta}. \tag{2.22}$$

ΔB is the peak-to-peak flux density of the loop. If minor loops exist, each loop has to be calculated separately. In continuous conduction mode (CCM) of the boost converter, only the major loop needs to be considered.

The capacitor power loss is due to the capacitor's equivalent-series-resistance (ESR). In a proper converter design, the capacitor power loss is usually small and can be ignored.

2.1.3 Conventional boost converter efficiency prediction

In this work, a 30 kW boost dc-dc converter is considered. The battery voltage $V_{battery}$ varies from 150 V to 300 V, with a nominal voltage of 200 V. The boost conversion ratio $M = V_{bus}/V_{battery}$ can vary from 1 to 4. With inclusion of all transients, the worst-case dc bus voltage V_{bus} is limited to 800 V. With a 33% voltage derating, which is typically requested by the automotive industry, 1200 V semiconductor devices are required in the conventional boost dc-dc converter. Under the worst-case conditions (30 kW at 150 V battery voltage, with conversion ratio of $M = 1$), the boost

switches conduct 200 A current. 1200 V silicon IGBTs are typically employed. As a representative example, the Fuji Electric 2MBI200VB-120-50 2-pack IGBT module is considered. This half-bridge module is composed of 1200 V 200 A punch-through IGBTs with co-packaged diodes. Curve-fitted device loss models are summarized in Table 2.1.

Table 2.1: 1200 V 200 A 2MBI200VB-120-50 IGBT Module Loss Model

IGBT	Conduction loss	V_{ces} [V]	0.75
		R_q [mΩ]	7
	Turn-on loss	K_{on}	5×10^{-7}
		a_{on}	0.9
		b_{on}	0.84
	Turn-off loss	K_{off}	4.5×10^{-9}
		a_{off}	0.95
		b_{off}	1.63
Diode	Conduction loss	V_f [V]	0.8
		R_d [mΩ]	5.5
	Reverse-recovery loss	K_{rr}	8.9×10^{-7}
		a_{rr}	0.82
		b_{rr}	0.84

The converter switches at 10 kHz. A 200 µH inductor is designed with powdered iron (Kool Mu 60u material from Magnetics Inc.) U-U core. The design parameters are summarized in Table 2.2.

Table 2.2: Conventional Boost Design Summary

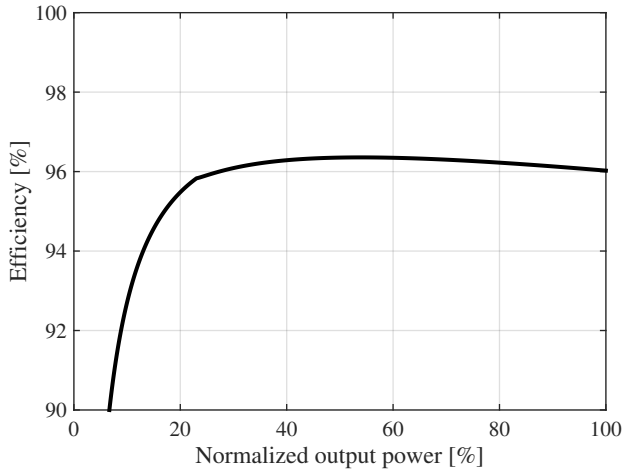
Semiconductor	Part number	2MBI200VB-120-50
	Rating	1200 V / 200 A IGBT
	Switching frequency	10 kHz
Inductor	Inductance	200 µH
	Core material	Kool Mu 60u
	Core size	$A_e = 9\,\text{cm}^2$ $\ell_e = 40\,\text{cm}$
	Number of turns	70
	Wire diameter	4.07 mm

Figure 2.3(a) shows the efficiency of this boost converter at $V_{battery} = 200\,\text{V}$ and $V_{bus} = 650\,\text{V}$. The efficiency is plotted as a function of normalized output power level. The efficiency of this boost

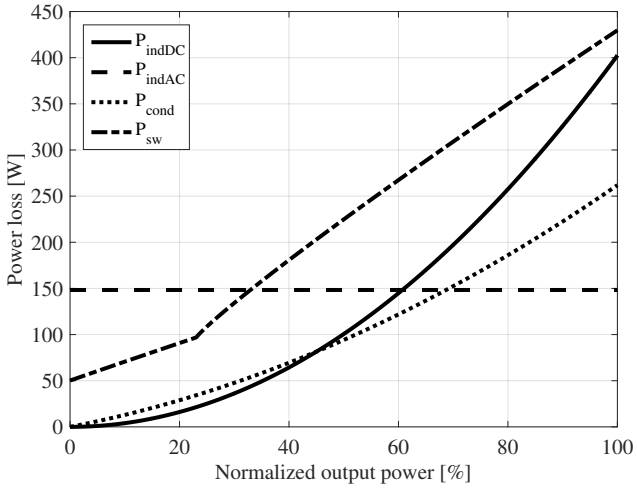
converter is round 96% to 96.4% at medium load to full load, while it drops drastically at light load. Figure 2.3(b) shows the loss breakdown of this boost converter. Ac losses, including semiconductor switching losses P_{sw} and inductor ac losses P_{indAC}, dominate the total loss at light to medium loads. To improve the converter efficiency at medium to light load range, which is crucial for the application of traction powertrain, it is necessary to reduce the converter ac power losses.

Figure 2.3: Typical conventional boost converter design at $V_{battery} = 200\,\mathrm{V}$ and $V_{bus} = 650\,\mathrm{V}$: (a) converter efficiency vs. normalized output power; (b) normalized power loss vs. normalized output power.

(a)



(b)



To further understand the performance of the conventional boost converter, its loss modeled is considered under the standard driving cycles, as discussed in section 1.4. The converter quality

factor of the conventional boost converter is calculated as

$$Q = \frac{\int |P_{out}| \, \mathrm{d}t}{\int P_{loss} \, \mathrm{d}t}, \tag{2.23}$$

and the results are documented in Table 2.3. The converter shows better performance in the low speed urban driving (UDDS), due to lower bus voltage, and therefore lower voltage conversion ratio.

Table 2.3: Converter quality factor Q of the conventional boost converter, under standard driving cycles

	UDDS	HWFET	US06
Q	38.6	17.5	21.9

2.2 Soft switching techniques

Various soft switching techniques, such as zero-voltage switching (ZVS) or zero-current switching (ZCS) have been investigated extensively in power electronics applications. Since the switching loss contributes significantly to the total loss in the conventional boost converter, it is of interest to investigate effectiveness of soft switching approaches. In practice, a soft switching technique may reduce but not completely eliminate switching loss. This is especially the case considering minority carrier devices such as IGBTs, where losses associated with turn-off current tailing can be reduced but not eliminated. Furthermore, auxiliary circuits introduced to facilitate soft switching introduce new additional losses. To evaluate the effectiveness of switching loss reduction, a soft-switching efficiency η_{ss} can be defined as:

$$\eta_{ss} = 1 - \frac{P_{sw,ss}}{P_{sw}} \tag{2.24}$$

where P_{sw} is the switching loss in the original hard-switched converter, and $P_{sw,ss}$ is the remaining switching loss after adopting soft switching. Ideally $\eta_{ss} = 100\%$, meaning that all the switching loss is recovered. In practice, η_{ss} is always less than 100%.

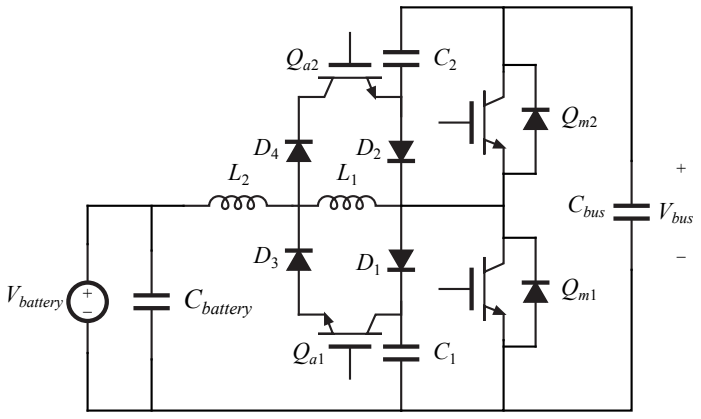
The snubber-assisted zero-voltage transition / zero-current transition (SAZZ) approach [45, 78, 94, 95] is an extension of the well-known auxiliary resonant commutated pole concept [26]. The

SAZZ approach addresses some switching loss mechanisms, including turn-on losses due to diode reverse recovery and, to some extent, turn-off losses due to IGBT current tailing. Its auxiliary circuit is relatively simple, and the converter main switch stresses and conduction losses remain the same as in the original boost converter.

Reference [45] describes a 200 V to 400 V 8 kW SAZZ boost prototype achieving 96% efficiency when operating at 100 kHz using MOSFETs. A 250 V to 390 V 25 kW bi-directional non-inverting SAZZ buck-boost prototype using 600 V IGBTs is presented in [94], achieving 97.4% efficiency at full output power. The SAZZ concept is extended in [78] using a modified snubber configuration and saturable inductors in the snubber circuit. The prototype demonstrates efficiencies exceeding 98.5% at 8 kW to 15 kW output power with 300 V to 420 V conversion, using 600 V MOSFETs operating at 50 kHz. Reference [95] reports another variation of the SAZZ concept, based on three interleaved unidirectional modules connected in parallel. A 200 V to 400 V conversion is demonstrated at up to 15 kW per module, with 30 kHz switching frequency using 1200 V IGBT. According to the efficiencies and the loss results reported in [95], it can be estimated that the SAZZ approach with IGBT devices yields $\eta_{ss} \approx 38\%$.

2.2.1 Operation of SAZZ converter

Figure 2.4: Bi-directional boost SAZZ converter in [45]



The power stage schematic of a bi-directional boost SAZZ converter [45] is shown in Fig. 2.4.

Figure 2.5: Waveforms of boost SAZZ converter with the operation of positive power flow, reproduced from [45]

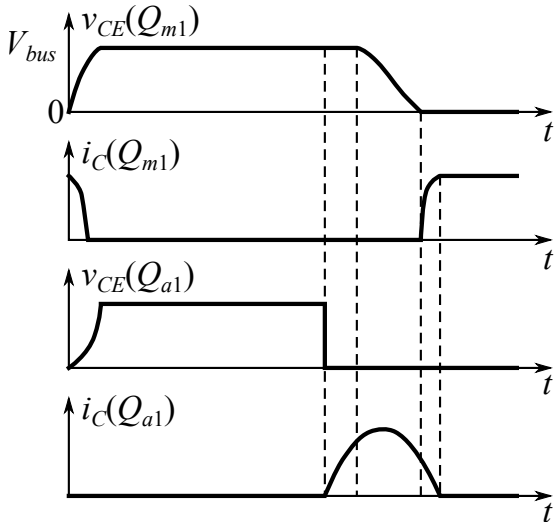
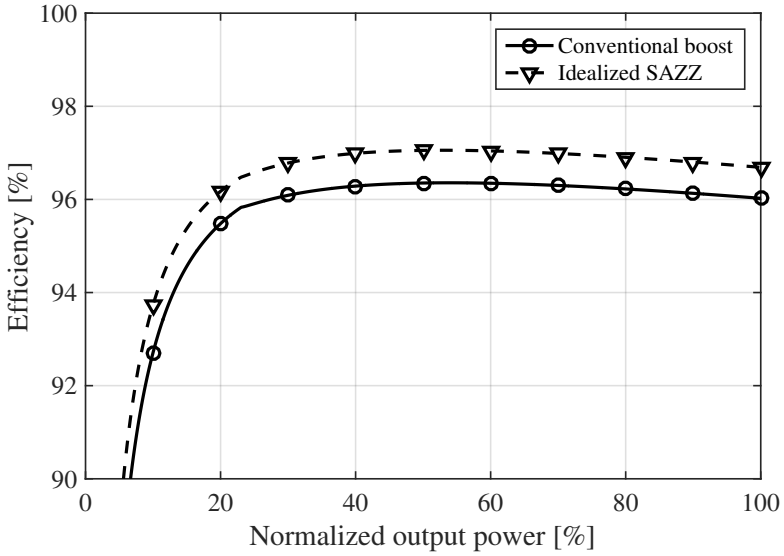


Fig. 2.5 shows the operation waveform during positive power flow. The two main switches Q_{m1}, Q_{m2}, together with the main inductor L_1 resemble a conventional boost converter, where the switch Q_{m1} had to turn on with hard-switching during positive power flow. The resonant components L_2, C_1, with auxiliary switches Q_{a1}, D_1, and D_3, help to achieve ZVS turn on of Q_{m1}. As shown in Fig. 2.5, the auxiliary switch Q_{a1} turns on first with ZCS, shorting the main inductor L_1, so that L_2-C_2 form a resonant tank. The resonant energy helps Q_{m1} to achieve ZVS.

2.2.2 SAZZ converter efficiency prediction

In reference [95], soft switching efficiency $\eta_{ss} \approx 38\%$ has been reported for IGBT devices. The soft switching technique is not very effective for minority-carrier devices such as IGBT, due to the tail current of the device. Figure 2.6 plots the predicted efficiency of an idealized SAZZ converter, where $\eta_{ss} = 50\%$ is assumed, and the rest of the converter losses are the same as the conventional boost converter with design parameters documented in Table 2.2. Notice that this model counts neither the extra switching and driver loss induced by the auxiliary switches, nor the extra magnetic loss. Therefore, the prediction serves as an ideal upper bound of the achievable efficiency by the soft switching techniques. Overall the efficiency improvement is less than 1%. Particularly, the light

Figure 2.6: Idealized SAZZ converter efficiency prediction at fixed 200 V input and 650 V output



load efficiency, which is of great concern in the application of traction powertrain system, is not significantly improved.

Table 2.4 compares the converter quality factor Q of the conventional approach and the SAZZ approach, under standard driving profiles. The reduction of average loss is incremental with SAZZ approach.

Table 2.4: Converter quality factor Q comparison between the SAZZ approach and the conventional approach, under standard driving cycles

	UDDS	HWFET	US06
Conventional boost	38.6	17.5	21.9
SAZZ	44.9	20.2	26.4

2.3 Coupled inductor approach

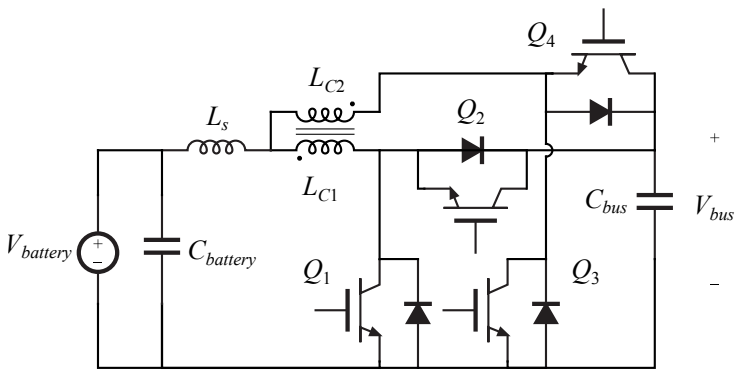
Approaches based on parallel interleaved topologies and coupled inductors can be used to reduce magnetic losses and, to some extent, switching losses [42, 46, 55, 58, 65, 75]. Paralleled boost converters with coupled inductors have been studied in a number of references, including [65].

Interleaving reduces the rms current applied to the output capacitor, and allows operation at reduced switching frequency, which results in reduced switching losses. Furthermore, reference [65] also points out that soft-switching can be achieved with the help of the leakage inductance associated with the coupled inductors.

A particularly interesting coupled-inductor approach is introduced in [42], by engineers from Honda. Figure 2.7 illustrates a bi-directional version of the proposed coupled-inductor boost converter. With this approach, each phase only carries half of the total current, and the switching frequency is equal to one half of the inductor current ripple frequency. Therefore, the device switching loss is reduced. Furthermore, thanks to the 1:1 transformer, the volt-seconds applied to the inductor are reduced so that the inductor loss can be reduced. However, there are additional losses associated with the transformer. In similar approaches and extensions [46, 58, 75] all magnetic components are integrated on the same core, which may lead to a higher power density and a reduction in total magnetics losses.

In reference, [42], the demonstrated unidirectional prototype has an input voltage range of 70 V to 180 V, and an output voltage range of 210 V to 252 V, with a maximum power of 42 kW. The switches are realized using the APTC60DAM18CTG power module composed of one 600 V MOSFET and one 600 V SiC Schottky diode. The switching frequency is 45 kHz. With a fixed boost ratio of 1.4, the experimentally measured peak efficiency is 98.4% at approximately 17 kW output power. Over 98% efficiency is achieved from 8 kW to 32 kW output power.

Figure 2.7: Bi-directional coupled inductor boost converter



The design in [55] adds auxiliary switches and magnetics to achieve soft-switching and mitigate losses associated with diode reverse recovery. A low-power (1 kW) experimental prototype with 100 V to 180 V conversion ratio demonstrates a modest peak efficiency improvement from 96.75% to 97%. It also reported a bi-directional power stage, which requires a relatively complex auxiliary circuitry for four-quadrant switches.

2.3.1 Coupled inductor boost converter operation

Figure 2.8: Waveforms of close-coupled converter in Fig. 2.7, with duty cycle $D \leq 50\%$.

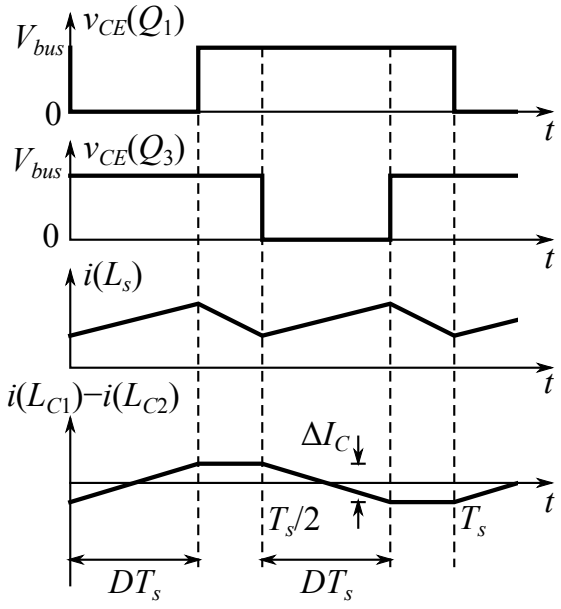


Figure 2.8 shows the operation waveforms of the close-coupled converter in Fig. 2.7, with duty cycle $D \leq 50\%$. The duty cycle D is defined as the on-time of the low-side transistor in one phase, over the switching period T_s. Two half bridges are interleaved with 90° phase shift. They operate with the same duty cycle D, so that the voltage-second applied to the transformer is balanced. Notice that due to the nature of interleaving, the inductor current $i\,(L_s)$ exhibits the ripple with period $T_s/2$.

According to the waveform in Fig. 2.8, when $D \leq 50\%$, the voltage-second balance equation

on the inductor L_s can be written as:

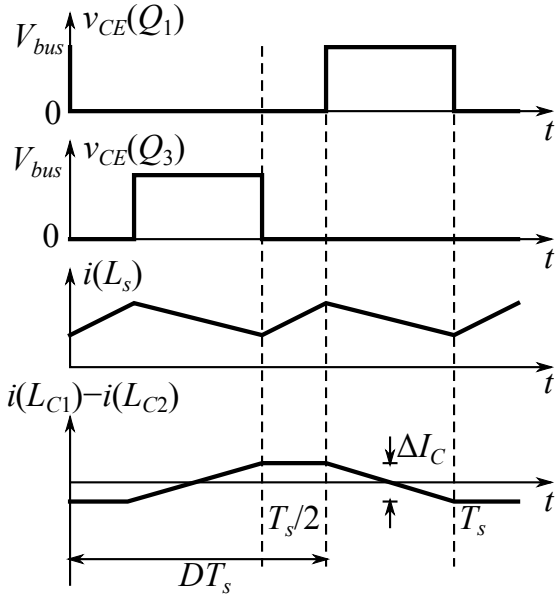
$$\left(V_{battery} - \frac{V_{bus}}{2}\right) DT_s + (V_{battery} - V_{bus}) \left(\frac{T_s}{2} - DT_s\right) = 0. \tag{2.25}$$

Therefore, the voltage conversion ratio M can be derived:

$$M = \frac{V_{bus}}{V_{battery}} = \frac{1}{1-D} \text{ when } D \leq 50\%. \tag{2.26}$$

In this operation mode, $M \leq 2$.

Figure 2.9: Waveforms of close-coupled converter in Fig. 2.7, with duty cycle $D > 50\%$.



Similarly, Fig. 2.9 shows the operation waveforms when $D > 50\%$. In this case, the voltage-second balance equation of L_s is:

$$\left(V_{battery} - \frac{V_{bus}}{2}\right) (T_s - DT_s) + V_{battery} \left(DT_s - \frac{T_s}{2}\right) = 0. \tag{2.27}$$

The voltage conversion ratio M is derived as:

$$M = \frac{1}{1-D} \text{ when } D > 50\%, \tag{2.28}$$

which turns out to be the same as the case when $D \leq 50\%$, with the existing duty cycle definition.

The inductor current $i\left(L_s\right)$ sets the common-mode current in the transformer, that is, $i\left(L_s\right) = i\left(L_{C1}\right) + i\left(L_{C2}\right)$. As sketched in Fig. 2.8, the differential-mode current ripple of the transformer $i\left(L_{C1}\right) - i\left(L_{C2}\right)$ is due to the finite magnetizing inductance of the transformer:

$$i\left(L_{C1}\right) - i\left(L_{C2}\right) = \frac{1}{L'_m}\int_0^t \left(v_{CE}\left(Q_3\right) - v_{CE}\left(Q_1\right)\right)\,\mathrm{d}t', \tag{2.29}$$

where L'_m is the magnetizing inductance of the transformer, seen between two switching nodes.

$$L'_m = \frac{4\mu_c A_c N^2}{\ell_c}, \tag{2.30}$$

where N is the number of turns in each winding of the transformer, A_c and ℓ_c are the cross-section area and magnetic path length of the transformer core, and μ_c is the permeability of the core material, assuming no air gap. When $D \leq 50\%$, the peak-to-peak amplitude, ΔI_C, of the differential-mode current ripple $i\left(L_{C1}\right) - i\left(L_{C2}\right)$ is

$$\Delta I_C = \frac{V_{bus} D T_s}{L'_m} = \frac{V_{battery} T_s}{L'_m} \cdot \frac{D}{1-D}. \tag{2.31}$$

When $D > 50\%$,

$$\Delta I_C = \frac{V_{bus}(1-D) T_s}{L'_m} = \frac{V_{battery} T_s}{L'_m}. \tag{2.32}$$

2.3.2 Coupled inductor boost converter efficiency prediction

To evaluate the performance of the coupled inductor approach, a boost converter is designed. Because the coupled inductor approach is composed of two interleaved phases, each phase only carries half the current. Therefore, the switches are realized with two 2MBI100VA-120-50 modules, which are 1200 V 100 A IGBT half-bridge modules. Its loss model is summarized in Table 2.5.

The design parameters of the coupled inductor boost converter is tabulated in Table 2.6. For fair comparison, the inductor and transformer design is sized so that the total core volume is the same as that of the design of the conventional boost converter in Table 2.2. Because the transformer winding only carries half current in inductor, the winding wire in the transformer has half the cross-section area as that in the inductor. The predicted efficiency is plotted in Fig. 2.10. The converter

Table 2.5: 1200 V 100 A 2MBI100VA-120-50 IGBT Module Loss Model

IGBT	Conduction loss	V_{ces} [V]	0.75
		R_q [mΩ]	14
	Turn-on loss	K_{on}	3.05×10^{-7}
		a_{on}	1.001
		b_{on}	0.84
	Turn-off loss	K_{off}	8.9×10^{-9}
		a_{off}	0.75
		b_{off}	1.63
Diode	Conduction loss	V_f [V]	0.8
		R_d [mΩ]	11
	Reverse-recovery loss	K_{rr}	2.15×10^{-6}
		a_{rr}	0.62
		b_{rr}	0.84

Table 2.6: Coupled Inductor Boost Design Summary

Semiconductor	Part number	2MBI100VB-120-50
	Rating	1200 V / 100 A IGBT
	Switching frequency	10 kHz
Inductor	Inductance	135 µH
	Core material	Kool Mu 60u
	Core size	$A_e = 9\,\text{cm}^2$ $\ell_e = 22.9\,\text{cm}$
	Number of turns	40
	Wire diameter	4.07 mm
Transformer	Core material	Kool Mu 60u
	Core size	$A_e = 9\,\text{cm}^2$ $\ell_e = 17.1\,\text{cm}$
	Number of turns	30
	Wire diameter	2.88 mm

quality factor Q of the coupled inductor approach is tabulated in Table 2.7, in comparison with the conventional approach. The coupled inductor approach does improve the converter efficiency over the whole power range, although the improvement is still incremental.

Figure 2.10: Coupled inductor boost converter efficiency prediction at fixed 200 V input and 650 V output

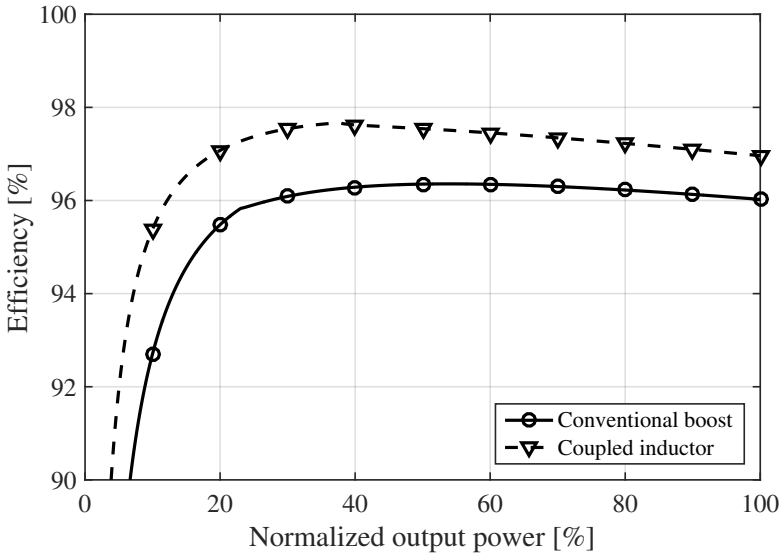


Table 2.7: Converter quality factor Q comparison between the coupled inductor approach and the conventional approach, under standard driving cycles

	UDDS	HWFET	US06
Conventional boost	38.6	17.5	21.9
Coupled inductor	62.4	35.5	34.0

2.4 Three-level converter

Three-level converters [72], such as the bi-directional three-level boost converter using MOSFETs shown in Fig. 2.11, have been introduced to allow use of switches with voltage rating reduced

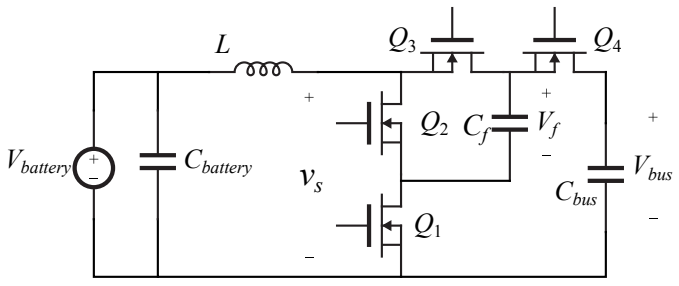


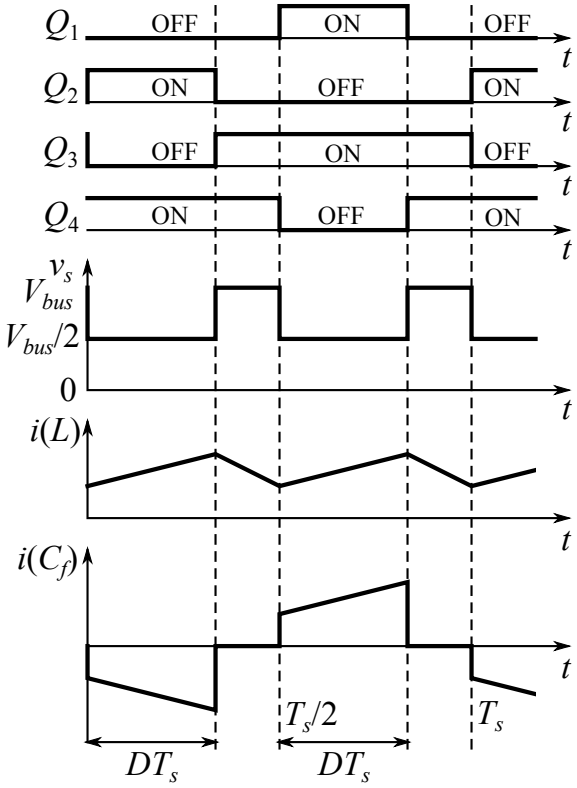
Figure 2.11: Bi-directional three-level boost converter

by a factor of two. Furthermore, similar to the coupled-inductor approach in [42], inductor volt-seconds are reduced and the switching frequency is equal to one half of the inductor current ripple frequency. As a result, the inductor size and inductor losses can be reduced.

The bidirectional three-level boost converter of Fig. 2.11 can be considered a candidate for the automotive powertrain application. Since the device voltage stress equals to one half of the bus voltage, 600 V MOSFETs can be used to allow higher switching frequency, and substantial reductions in the inductor size and losses. With MOSFETs, however, the requirement of bi-directional power flow constraints the design to utilize MOSFETs body diodes, instead of fast external diodes, which raises concerns about switching losses associated with diode reverse recovery. Furthermore, the flying capacitor is exposed to large rms current.

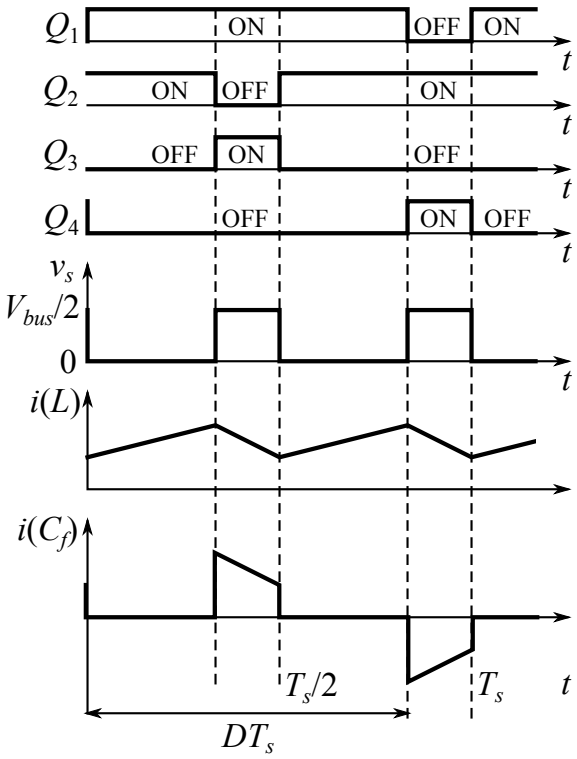
2.4.1 Three-level converter operation

Figure 2.12: Waveforms of three-level boost converter, when the voltage conversion ratio $M \leq 2$.



Similar to the coupled inductor converter, the three-level converter requires different switching sequence when the voltage conversion ratio $M \leq 2$ and $M > 2$. Figure 2.12 shows the operation waveform of the three-level converter when the voltage conversion ratio $M \leq 2$. When Q_1 and Q_3 turn on, the flying capacitor is charged from the inductor L. When Q_2 and Q_4 turn on, the flying capacitor is discharged to the load. If the duty cycles of these two phases are identical, the charge in the flying capacitor C_f is balanced, and thus $V_f = V_{bus}/2$. Therefore, the flying capacitor helps to reduce the voltage-second applied to the inductor L, and the switching node voltage v_s is either $V_{bus}/2$ or V_{bus}. With this operation, the voltage conversion ratio $M \leq 2$, and thus $V_{bus}/2 \leq V_{battery}$. When $v_s = V_{bus}/2$, the inductor current ramps up, and when $v_s = V_{bus}$, the inductor current ramps down. The period of the inductor current ripple is $T_s/2$.

Figure 2.13: Waveforms of three-level boost converter, when the voltage conversion ratio $M > 2$.



The operation waveform of the three-level converter when $M > 2$ is sketched in Fig. 2.13. If the charge in the flying capacitor C_f is balanced, the switching node voltage v_s is either zero or $V_{bus}/2$. Because with this operation $M > 2$, $V_{bus}/2 > V_{battery}$.

If the duty cycle D is defined as the low side transistors (Q_1 and Q_2) turn on time over the switching period T_s, as depicted in Fig. 2.12 & 2.13, one can derive that the voltage conversion ratio is

$$M = \frac{1}{1-D}. \tag{2.33}$$

Notice that this relationship is true for both $M \leq 2$ and $M > 2$.

2.4.2 Three-level converter efficiency prediction

Table 2.8: 600 V 46 A FCH76N60NF Super-Junction MOSFET Loss Model

MOSFET	Conduction loss	R_q [mΩ]	57.4
	Switching loss*	K_q	1.8×10^{-10}
		a_q	1.81
		b_q	1.43
Body diode	Conduction loss	V_f [V]	0.6
		R_d [mΩ]	32
	Reverse-recovery loss†	K_{rr}	1.2×10^{-7}
		a_{rr}	0.96
		b_{rr}	1.16

*: $E_q = K_q I^{a_q} V^{b_q}$.
†: $E_{rr} = K_{rr} I^{a_{rr}} V^{b_{rr}}$.

In three-level converter, if the charge in the flying capacitor C_f is balanced, the rating of the device voltage is halved. Instead of 1200 V devices, 600 V devices can be considered for the three-level converter. Here 600 V MOSFET is considered, which provides both lower conduction loss and lower switching loss than its IGBT counterpart. Table 2.8 documents the loss model of FCH76N60NF 600 V MOSFET from Fairchild. Each MOSFET die is rated to 46 A current, and has 57.4 mΩ on-resistance at 100 °C junction temperature.

To reduce the device on-resistance and increase current capability, several MOSFET dies are connected in parallel for each switch. Twelve MOSFET dies per switch are found to yield a good trade-off between conduction and switching losses. The switching frequency is 10 kHz, which leads to the equivalent frequency of 20 kHz for the current ripple of inductor. Due to the reduced voltage-

Table 2.9: Three-level Boost Design Summary

Semiconductor	Part number	FCH76N60NF
	Rating	600 V / 46 A MOSFET
	Devices per switch	12
	Switching frequency	10 kHz
Inductor	Inductance	85 µH
	Core material	Kool Mu 60u
	Core size	$A_e = 9\,\text{cm}^2$ $\ell_e = 21.7\,\text{cm}$
	Number of turns	25
	Wire diameter	4.07 mm

second on the inductor, the inductance is reduced to 85 µH. The design parameters are summarized in Table 2.9.

Figure 2.14: Three-level boost converter efficiency prediction at fixed 200 V input and 650 V output

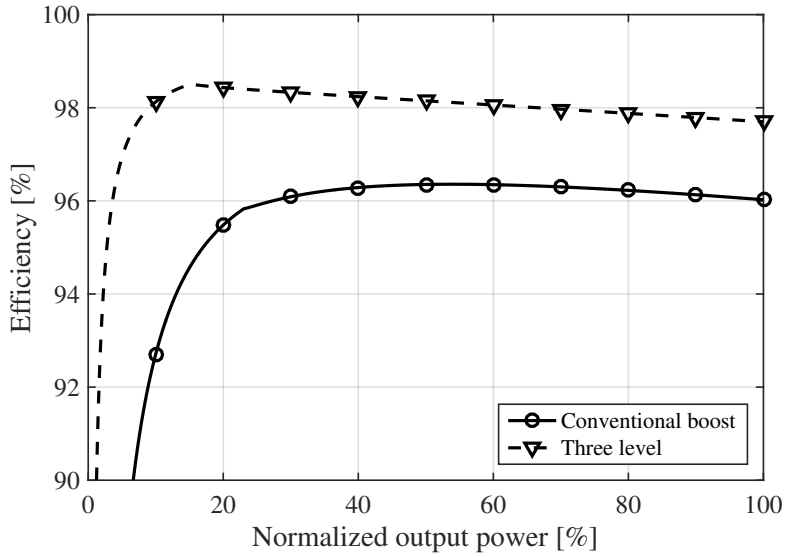


Figure 2.14 plots the predicted three-level converter efficiency. Comparing with the conventional boost converter, the efficiency of three-level converter is much improved. The loss at medium load condition is reduced by half, and the loss reduction in light load is even more significant. The converter quality factor Q of the three-level converter is summarized in Table 2.10. Three-level converter achieves significant average loss reduction comparing with the conventional approach.

Table 2.10: Converter quality factor Q comparison between the three-level converter and the conventional boost converter, under standard driving cycles

	UDDS	HWFET	US06
Conventional boost	38.6	17.5	21.9
Three-level	117.5	71.4	57.7

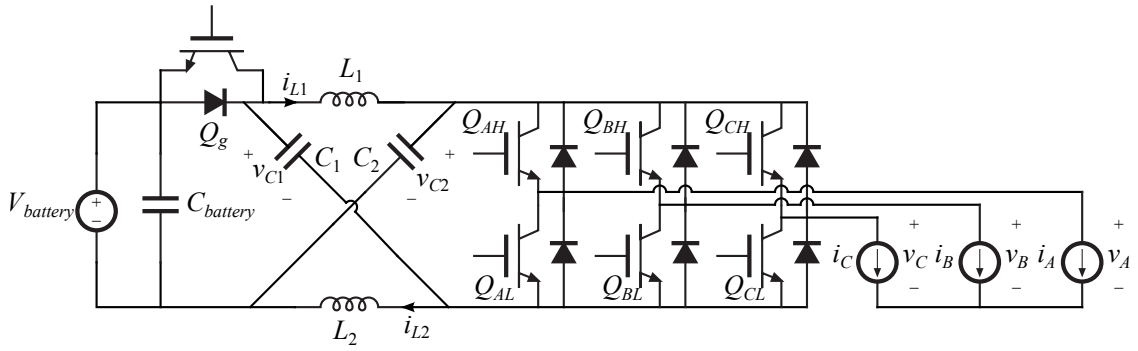
The main drawback of three-level converter is the size of the flying capacitor C_f. As depicted in Fig. 2.12 & 2.13, the flying capacitor C_f is required to carry large amount of ac current. The ac current rating (or power rating) leads to a bulky flying capacitor, and the large ac current leads to extra capacitor power loss as well. The power rating of capacitor modules in different converter topologies will be discussed in detail in section 3.6.

2.5 Impedance-source inverter

The Z-source (or impedance-source) inverter [79] and its many variations such as [5, 88], present an interesting alternative to conventional cascaded converter and inverter approaches shown in Fig. 1.5. Figure 2.15 shows a typical three-phase Z-source inverter with bi-directional power capability. It integrates the functionality of a boost dc-dc converter stage and an inverter stage. While the conventional buck-type voltage-fed inverter is only capable of producing output voltages lower than the input voltage, the Z-source inverter is capable of producing output voltages either higher or lower than the input voltage. Therefore, this approach may be suitable for the considered powertrain application. For example, [80, 87] demonstrated Z-source inverters intended for a fuel cell hybrid electric vehicle (FCHEV) powertrain.

A very interesting feature of the Z-source inverter is that it is immune to shoot-through failures. The shoot-through state when both a high-side and a low-side switch turn on at the same time is in fact utilized to achive the boost function. The buck inverter and the boost functions are effectively time-multiplexed into three-phase PWM signals.

Figure 2.15: Bi-directional three-phase Z-source inverter



2.5.1 Impedance-source inverter operation

Figure 2.16: The equivalent circuit of Z-source inverter at normal chopping phase

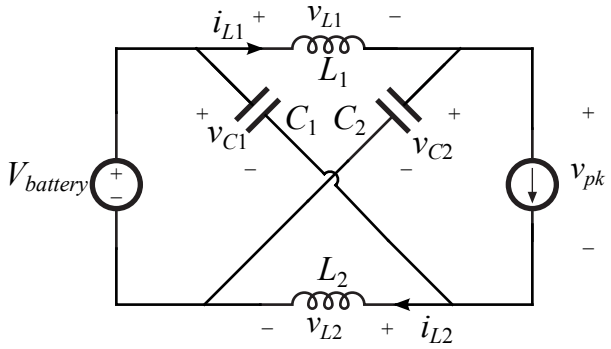


Figure 2.16 illustrates the equivalent circuit of Z-source inverter at the normal chopping phase. At this state, the switch Q_g turns on, and the three-phase chopper can be modeled as a current source. Because of the symmetry of the impedance tank, without the loss of generality, one can assume that $v_{L1} = v_{L2} = v_L$, and $v_{C1} = v_{C2} = V_C$. Here the voltage ripple on the capacitors C_1 and C_2 is ignored, and the voltage across the capacitors is assumed to be constant. The voltage v_{pk} is the instantaneous peak output voltage of a phase if the high-side switch of that phase turns on. v_{pk} is also the blocking voltage of the three-phase chopper device if the device is at off-state. At this phase, it can be derived that

$$v_L = V_{battery} - V_C, \tag{2.34}$$

and

$$v_{pk} = V_C - v_L = 2V_C - V_{battery}. \tag{2.35}$$

Figure 2.17: The equivalent circuit of Z-source inverter at shoot-through phase

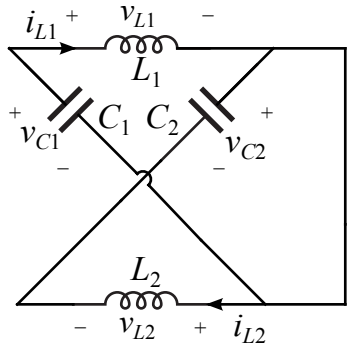


Figure 2.17 shows the equivalent circuit of Z-source inverter at the shoot-through phase. At this phase, the output is short circuit, and the switch Q_g turns off. The voltage across the inductors is

$$v_L = V_C. \tag{2.36}$$

Assume the duty cycle of the shoot-through phase is D_{st}, the voltage-second balance equation on the inductor can be written as

$$(V_{battery} - V_C)(1 - D_{st}) + V_C D_{st} = 0, \tag{2.37}$$

or

$$\frac{V_C}{V_{battery}} = \frac{1 - D_{st}}{1 - 2D_{st}}. \tag{2.38}$$

Therefore, the voltage conversion ratio of the peak voltage is

$$M_{pk} = \frac{v_{pk}}{V_{battery}} = \frac{1}{1 - 2D_{st}}. \tag{2.39}$$

With the given peak voltage v_{pk}, the maximum duty-cycle of one phase is $1 - D_{st}$. Thus, the conversion ratio of maximum peak-to-peak line voltage amplitude is

$$M_{La} = (1 - D_{st}) M_{pk} = \frac{1 - D_{st}}{1 - 2D_{st}}. \tag{2.40}$$

In another word, to achieve a maximum peak-to-peak line voltage amplitude of $V_{La} = V_{battery} M_{La}$, the device blocking voltage is

$$v_{pk} = V_{battery} \left(2M_{La} - 1\right) = 2V_{La} - V_{battery}. \tag{2.41}$$

Considering the powertrain example where the boost dc-dc converter is able to produce 800 V output voltage at 200 V input voltage, 800 V line voltage amplitude can be produced in the conventional architecture of Fig. 1.5. Devices rated at 1200 V can be applied. To produce the same line voltage amplitude at 200 V input with the Z-source inverter, the device voltage stress is 1400 V. Using the same device voltage de-rating, the Z-source inverter would require 2100 V devices.

The time-multiplexing operation also implies that the devices in the Z-source inverter must conduct higher currents resulting in potentially higher conduction losses, even though the Z-source inverter has fewer devices compared to the conventional approach.

Similar considerations and conclusions have been reached in [36] in a wind turbine application. Reference [87] shows that at operating points having very small voltage boost ratios, the Z-source inverter can theoretically offer slight efficiency improvements. In [11], where the Z-source inverter efficiency is evaluated in an electric vehicle powertrain application over a practical driving profile, it was found that the conventional approach results in a slightly higher efficiency.

In this chapter, the conventional boost converter and its loss model is reviewed. The efficiency of the conventional boost converter is high at heavy load, but drops at medium to light load, because of the ac power loss. Several existing approaches to reduce the ac power loss is discussed. Table 2.11 compares the converter quality factor Q of different approaches, under standard driving profiles. The Z-source inverter significantly increases the voltage and current rating of the devices, and is unlikely to achieve better efficiency. The SAZZ converter and coupled inductor converter only achieves incremental loss reduction. The three-level converter does achieve very good efficiency, but it requires large capacitor size, which significantly increases the system size and cost, and is difficult

to implement.

Table 2.11: Converter quality factor Q comparison of existing approaches

	Boost	SAZZ	Coupled inductor	Three-level
UDDS	38.6	44.9	62.4	117.5
HWFET	17.5	20.2	35.5	71.4
US06	21.9	26.4	34.0	57.7

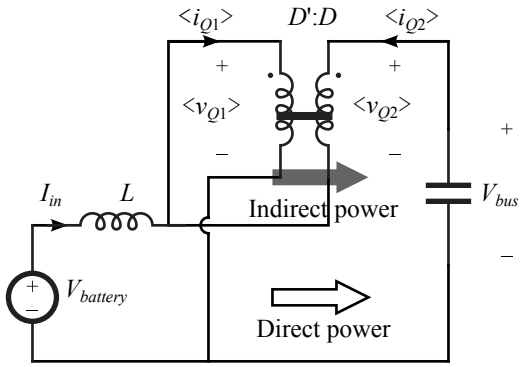
Chapter 3

Composite DC-DC Converter Concept

As discussed in the previous chapter, various existing approaches to converter efficiency improvements partially address some loss mechanisms. As such, they tend to result in incremental or partial improvements in size, cost and efficiency trade-offs. The objectives of this chapter are to first identify the fundamentals of loss mechanisms and then to introduce composite converter configurations where the loss mechanisms are directly addressed, and which can lead to substantial, non-incremental improvements in efficiency and P_{out}/P_{loss} figures of merit.

3.1 Direct / indirect power and power loss

Figure 3.1: Conventional boost converter averaged switch model



Consider again the conventional boost converter shown in Fig. 2.1, with transistor Q_1 voltage and current waveforms shown in Fig. 2.2. The instantaneous switch voltage $v_{Q1}(t)$ can be decomposed into the average dc component $\langle v_{Q1} \rangle$, and the ac component $\tilde{v}_{Q1}(t)$, as shown in Fig. 3.2.

The same can be applied to all switch voltages and currents, as follows:

$$\begin{cases} v_{Q1}(t) &= \langle v_{Q1}\rangle + \tilde{v}_{Q1}(t) \\ i_{Q1}(t) &= \langle i_{Q1}\rangle + \tilde{i}_{Q1}(t) \\ v_{Q2}(t) &= \langle v_{Q2}\rangle + \tilde{v}_{Q2}(t) \\ i_{Q2}(t) &= \langle i_{Q2}\rangle + \tilde{i}_{Q2}(t) \end{cases} \tag{3.1}$$

With the assumption that the switches are lossless, the switch power can be expressed as:

$$p_{Q1}(t) = v_{Q1}(t)\, i_{Q1}(t) = 0 \tag{3.2}$$

By substituting (3.1) into (3.2), and taking the average over one switching period, we obtain

$$\frac{1}{T_s}\int_0^{T_s} \left(\langle v_{Q1}\rangle + \tilde{v}_{Q1}(t)\right)\left(\langle i_{Q1}\rangle + \tilde{i}_{Q1}(t)\right)\, \mathrm{d}t = 0 \tag{3.3}$$

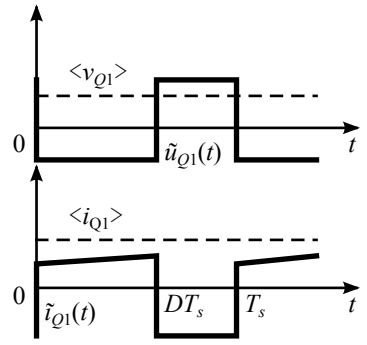
Since the average of each ac component over one switching period is zero, (3.3) can be re-arranged as:

$$\langle v_{Q1}\rangle \langle i_{Q1}\rangle = DV_{battery}I_{in} = -\frac{1}{T_s}\int_0^{T_s} \tilde{v}_{Q1}(t)\,\tilde{i}_{Q1}(t)\, \mathrm{d}t = -\left\langle \tilde{v}_{Q1}(t)\,\tilde{i}_{Q1}(t)\right\rangle \tag{3.4}$$

Similarly, for Q_2:

$$-\langle v_{Q2}\rangle \langle i_{Q2}\rangle = \left\langle \tilde{v}_{Q2}(t)\,\tilde{i}_{Q2}(t)\right\rangle \tag{3.5}$$

Figure 3.2: Average and ac components of transistor Q_1 voltage and current v_{Q1} and i_{Q1}



Equations (3.4) and (3.5) can be interpreted as follows: switch Q_1 converts dc power $\langle v_{Q1}\rangle \langle i_{Q1}\rangle = DV_{in}I_{in}$ into ac average power $\left\langle \tilde{v}_{Q1}(t)\,\tilde{i}_{Q1}(t)\right\rangle$, i.e. Q_1 operates as an inverter. Similarly, Q_2, which

operates as a rectifier, converts the ac average power back into dc power. The effective dc-to-ac-to-dc power conversion associated with the switches Q_1 and Q_2 leads to the notion of ac or *indirect power*, which is fundamental to all dc-dc converters [102]. In the boost converter, the ac power is $P_{indirect} = DV_{battery}I_{in}$. The averaged switch model shown in Fig. 3.1 [33] can be used to examine the voltage step-up and power flow in the converter. The voltage conversion ratio is

$$M = \frac{V_{bus}}{V_{battery}} = 1 + \frac{D}{D'} = \frac{1}{D'}\,. \tag{3.6}$$

The output power can be written as a sum of the ac or *indirect power* $P_{indirect} = V_{battery}(D'I_{in}) = D'P_{out}$ delivered through the ideal dc transformer in the averaged switch model, and the *direct power* $P_{direct} = V_{battery}(DI_{in}) = DP_{out}$ delivered directly from input $V_{battery}$ to output V_{bus},

$$P_{out} = P_{direct} + P_{indirect} = DP_{out} + D'P_{out}\,. \tag{3.7}$$

Combination of (3.6) and (3.7) implies that

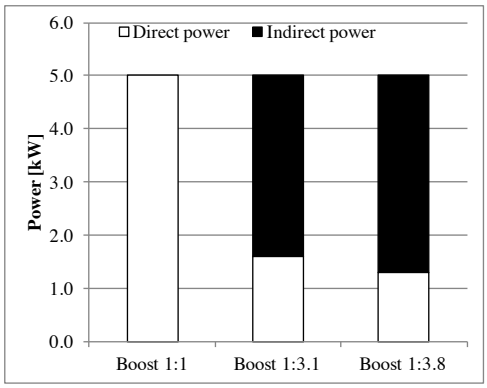
$$P_{indirect} = P_{out}\left(1 - \frac{1}{M}\right) \tag{3.8}$$

Note that $P_{indirect}$ represents the portion of power actively processed by the converter switches, and is therefore subject to both switch and inductor conduction (dc losses) and semiconductor switching losses and inductor ac losses (ac losses). Conversely, P_{direct} is transferred directly and is subject only to dc conduction losses, which can be relatively low. Importantly, it follows that the converter efficiency is *fundamentally limited by the amount of indirect power processed, and by the efficiency of indirect power processing.* In particular, as shown in section 1.3, this is the case in electrified automotive powertrain applications where ac losses dominate and light-to-medium load efficiency is very important.

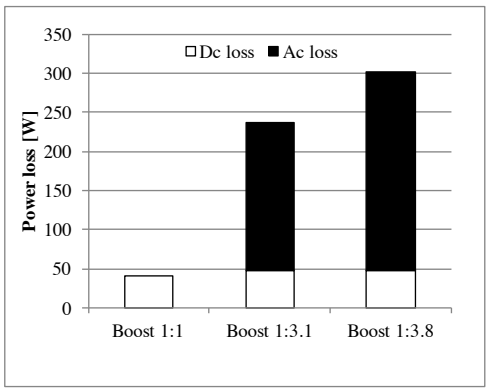
As implied by (3.8) for the boost converter, $P_{indirect}$ is determined by the conversion ratio M. Therefore, as is well understood and confirmed in practice, it is difficult to construct a high-efficiency converter with a large step-up ratio M. An example is given in Fig. 3.3. The direct / indirect power is calculated for a conventional boost converter at fixed 5 kW output power, with different conversion ratios, in Fig. 3.3(a). Fig. 3.3(b) shows the modeled dc and ac power loss.

Figure 3.3: Relationship between direct / indirect power and dc / ac power loss: (a) direct / indirect power distribution; (b) power loss distribution

(a)



(b)



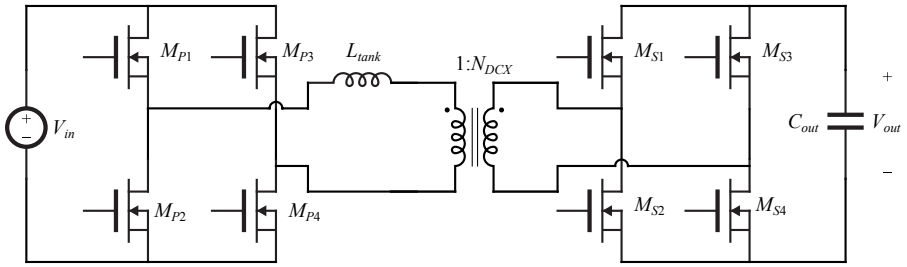
The ac power loss is strongly correlated to indirect power, while the dc power loss increases as indirect power increases as well. While discussed here in the context of the boost converter, these considerations apply to dc-dc converters in general [102].

One may note that various soft-switching techniques and other approaches reviewed in Chapter 2 can be interpreted as attempts to improve efficiency of indirect power processing. A fundamentally different approach is based on *composite* converter architectures consisting of dissimilar partial power processing modules where high conversion ratios can be obtained by stacking modules in series or parallel, and where indirect power processing is delegated to dedicated highly-efficient modules, while regulation is accomplished using modules processing low or no indirect power [20–22, 56].

One approach to improve efficiency of indirect power processing is to utilize an unregulated "DC transformer" (DCX) module, such as the converter shown in Fig. 3.4. If the secondary-side

switches are passive diodes or synchronous rectifiers emulating diode operation, this circuit is a simple DCX, which provides an essentially fixed voltage conversion ratio N_{DCX} at very high efficiency [100]. If the secondary side switches (M_{S1}–M_{S4}) are actively controlled, the circuit is referred to as the Dual-Active Bridge (DAB) [27]. Importantly, the converter can be optimized to achieve soft switching and low conduction losses at operating points where the transformer currents are trapezoidal [25, 44, 49]. Chapter 4 will have an extensive discussion on various details in DCX design.

Figure 3.4: Power stage schematic of DC Transformer (DCX) module



Since the DCX can process the indirect power more efficiently, the indirect power path in the boost converter modeled as shown in Fig. 3.1 can be replaced by the DCX. Replacing the ideal dc transformer with the DCX circuit results in the configuration shown in Fig. 3.5. This converter can be regarded as a DCX connected as an auto-transformer. The modeled efficiency of an example design is shown in Fig. 3.6. Although the DCX is designed with 1200 V IGBTs, a remarkable improvement in efficiency can be observed, compared to the conventional boost converter. The efficiency improvement at medium to light load is more significant, which is because DCX processes indirect power efficiently so that the ac power loss is reduced.

The circuit shown in Fig. 3.5 is not a practical converter, because it only works at one fixed voltage conversion ratio, and the dc bus voltage cannot be regulated. (Being said, one can replace the DCX with a DAB and actively control the phase shift to regulate the output voltage. Although the efficiency of DAB drops if the voltage conversion ratio deviates from transformer ratio N_{DCX}, in some situation it still yields good efficiency, as demonstrated in [7,96].) In the following subsections,

Figure 3.5: DCX connected as an auto-transformer

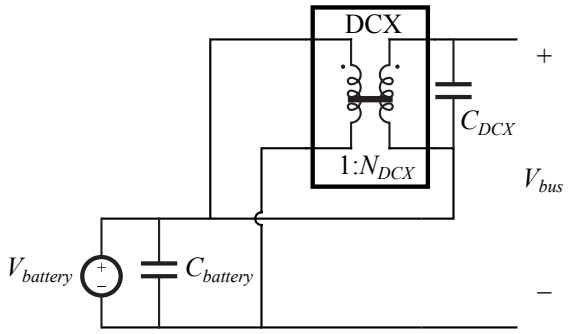
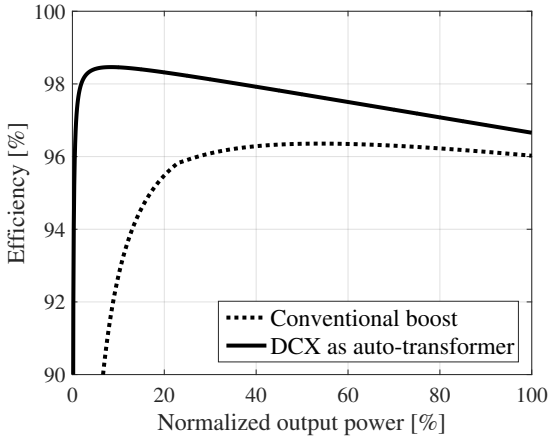


Figure 3.6: Modeled efficiency of DCX module connected as an auto-transformer



several practical composite converter topologies are developed. The composite converters combine a DCX module with other common converter modules such as buck, boost, or non-inverting buck-boost converter. Each converter module is only required to process partial power, and can be operated at higher efficiency. The modules are also designed in a way so that most of the indirect power is processed by the DCX. Therefore, the rest of the modules operate with conversion ratio close to one, at a much higher efficiency. Furthermore, each module can also be optimized independently to enhance efficiency at certain critical operation conditions. The use of lower voltage rating devices allows additional performance improvements, in terms of reduced on-resistance and switching loss. Finally, it is shown that the composite converter approach has potentials to reduce significantly the system capacitor rating, which can result in reduced system volume and reduced cost.

3.2 Composite converter architecture A

Figure 3.7: Boost composite converter A

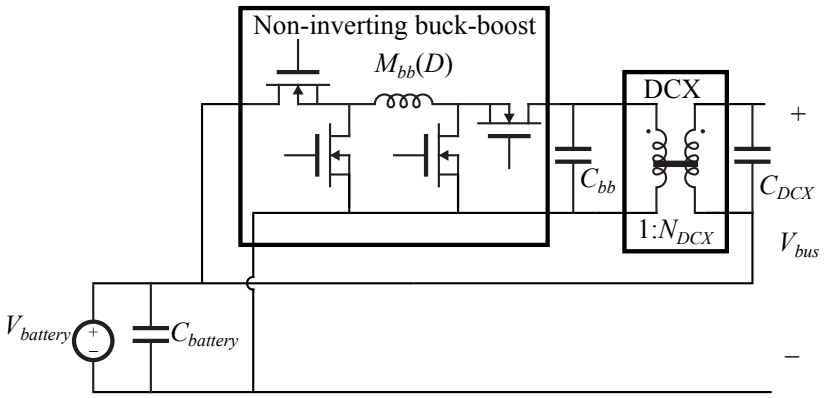
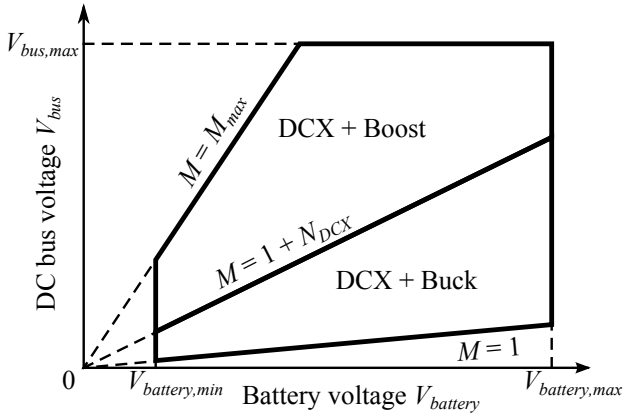


Fig. 3.7 shows a boost composite converter based on Fig. 3.5, but with a non-inverting buck-boost converter module inserted to control the DCX voltage, If we denote the non-inverting buck-boost converter voltage conversion ratio as $M_{bb}(D)$, and DCX turns ratio as N_{DCX}, then the two converters in series have the total voltage conversion ratio of $M_{bb}(D)N_{DCX}$, which emulates the duty cycle controlled ideal dc transformer in Fig. 3.1(b). The overall voltage conversion ratio of this composite converter is:

$$M = \frac{V_{bus}}{V_{battery}} = 1 + M_{bb}(D)N_{DCX} \tag{3.9}$$

Figure 3.8: Composite converter A & B operating modes



The non-inverting buck-boost module is operated as a buck module for $M_{bb} < 1$, and as a

boost module for $M_{bb} > 1$. This results in much higher efficiency than operating the module as a buck-boost with all four devices switching [23, 38, 51]. Fig. 3.8 shows the two operation modes: DCX + buck mode and DCX + boost mode.

The composite converter inherits the merits from the configuration in Fig. 3.5. The direct power path is a direct loss-free short-circuit connection. However, similar to the configuration in Fig. 3.5, although this configuration does reduce the device voltage stress, the reduction is not sufficient to facilitate devices with much lower voltage rating. For example, when the battery voltage is 200 V, if 800 V is desired at the dc bus output, the DCX must produce 600 V output. In this case, 900 V or 1200 V devices would be required. If the DCX turns ratio N_{DCX} is large enough, 600 V devices can be used in the non-inverting buck-boost module. Another drawback of this configuration relates to operation at low system conversion ratios: the non-inverting buck-boost converter must operate with a large step-down ratio. The inductor current equals the output current multiplied by N_{DCX}. As a result, reduced efficiency can be expected at reduced voltage conversion ratio.

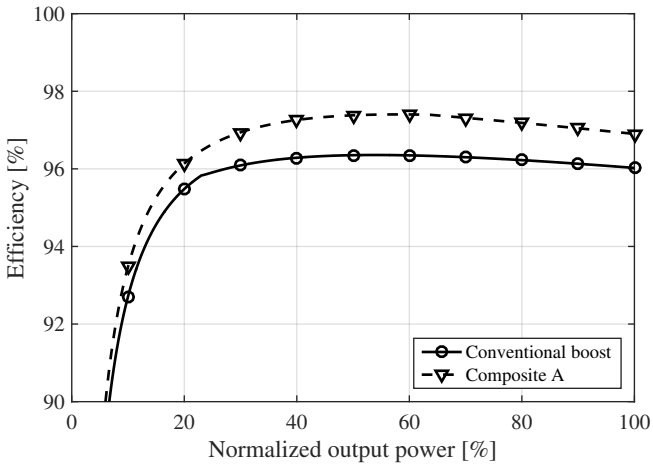
Table 3.1: Composite A Converter Magnetics Design Summary

Inductor	Inductance	25 µH
	Core material	Kool Mu 60u
	Core size	$A_e = 9\,\text{cm}^2$ $l_e = 8\,\text{cm}$
	Number of turns	14
	Wire diameter	4.07 mm
Transformer	Core material	PC95
	Core size	$A_e = 9\,\text{cm}^2$ $l_e = 22.6\,\text{cm}$
	Number of turns	7:11
	Wire diameter	primary: 11.5 mm secondary: 9.4 mm

As an example, a 30 kW composite A converter is designed. The transformer turns ratio in DCX is chosen to be 7:11 ($N_{DCX} \approx 1.5$), so that the voltage stress of the primary side of DCX is limited under 400 V. 600 V MOSFET FCH76N60NF is deployed in the buck-boost module as well as the DCX primary side, where each switch is composed of six MOSFET dies in parallel. Because

the secondary side of DCX needs to handle higher voltage, 1200 V IGBT module 2MBI100VA-120-50 is used there. The loss models of the MOSFET and IGBT used are summarized in Table 2.8 & 2.5. The buck-boost module switches at 20 kHz, with 20 µH inductance. Because of reduced switching loss with soft switching, the DCX module switches at 30 kHz. The magnetics designs are summarized in Table 3.1.

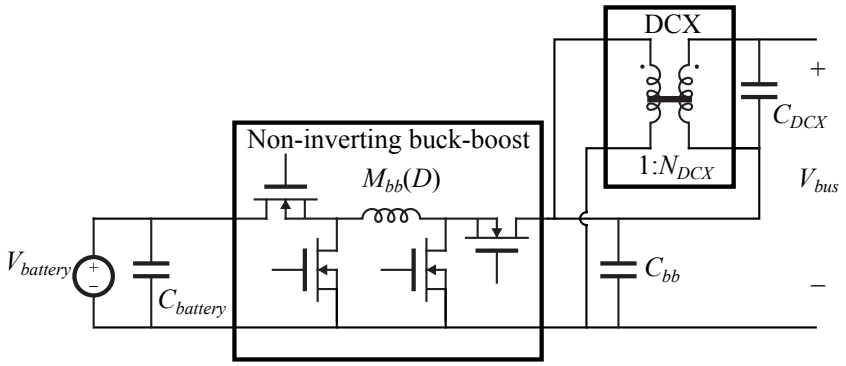
Figure 3.9: Modeled efficiency of composite A converter



The predicted efficiency of composite A converter is plotted in Fig. 3.9, with fixed 200 V input voltage and 650 V output voltage. Comparing with the conventional boost converter, the composite A converter shows more than 1% medium load efficiency improvement, though the light load improvement is not very significant.

Notice that with advanced device technologies, such as SiC device, the performance of composite A converter can be much improved, which will be discussed in section 5.4. Other than powertrain system, the composite A converter may have potential application in other field as well. For example, the "Yeaman topology" [86] for data center power supply can be regarded as a variation of composite A structure, where DCX is replaced by resonant converter.

Figure 3.10: Composite converter topology B



3.3 Composite converter architecture B

To allow 600 V devices in all modules, the boost composite converter B is presented in Fig. 3.10. Instead of inserting the non-inverting buck-boost converter before the DCX, the same converter is inserted on the input side of the system. The system overall voltage conversion ratio is

$$M = \frac{V_{bus}}{V_{battery}} = M_{bb}(D)\,(1 + N_{DCX}) \tag{3.10}$$

Notice that the composite converter B shares the same operating modes as converter A, as shown in Fig. 3.8. If the DCX conversion ratio is chosen to be $N_{DCX} = 1$, the dc bus voltage stress can be shared evenly between the DCX primary side and the secondary side. Therefore, the worst-case device voltage stress is equal to one half of the bus voltage and so 600 V devices can be used in all modules in the application that requires up to 800 V output bus voltage. A drawback of this configuration is that the non-inverting buck-boost module is required to process the full system power.

A composite B converter is designed with 600 V MOSFET FCH76N60NF. The DCX module switches at 30 kHz, and each switch in DCX is composed of three dies in parallel. As a consequence of the increased power rating of the non-inverting buck-boost module, its switch composed of eight dies in parallel. The non-inverting buck-boost module switches at 20 kHz, with an optimized inductor value $L = 63\,\mu\text{H}$. The design parameters of magnetics components are summarized in Table 3.2. Figure 3.11 plots the predicted efficiency at fixed 200 V input and 650 V output. The efficiency

Table 3.2: Composite B Converter Magnetics Design Summary

Inductor	Inductance	63 µH
	Core material	Kool Mu 60u
	Core size	$A_e = 9\,\text{cm}^2$ $l_e = 40\,\text{cm}$
	Number of turns	35
	Wire diameter	8.14 mm
Transformer	Core material	PC95
	Core size	$A_e = 9\,\text{cm}^2$ $l_e = 22.9\,\text{cm}$
	Number of turns	10:10
	Wire diameter	primary: 8.14 mm secondary: 8.14 mm

of composite B converter is slightly worse than the conventional boost converter at full power, which is primarily due to the increased conduction loss of the non-inverting buck-boost module at full power. It is still acceptable in the application of traction powertrain system, because the full power is seldom used. On the other hand, the composite B converter shows significant efficiency improvement at light load conditions.

Figure 3.11: Modeled efficiency of composite B converter

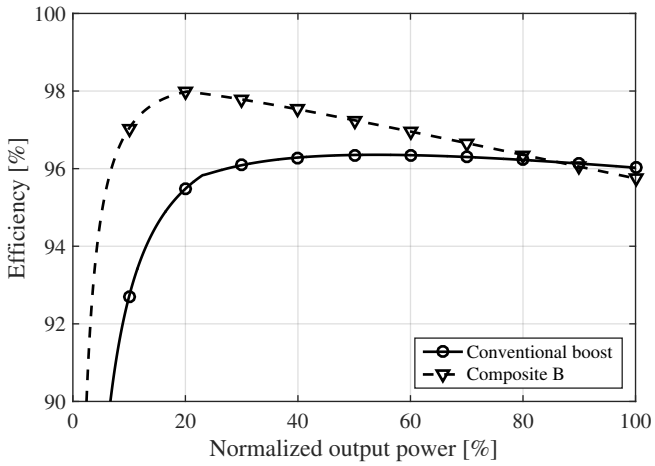
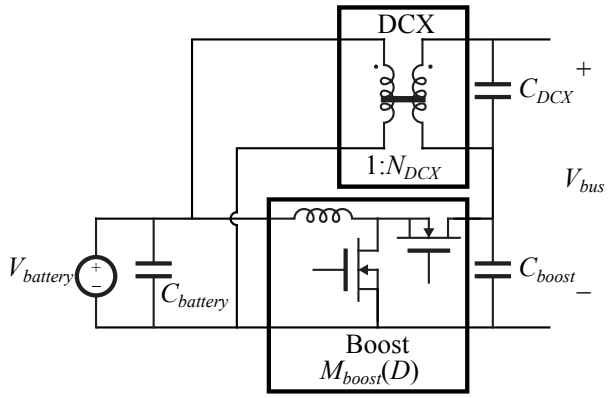


Figure 3.12: Composite converter topology C

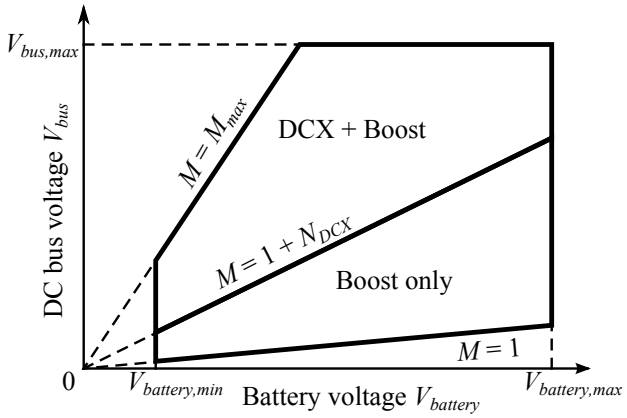


3.4 Composite converter architecture C

Fig. 3.12 shows another composite converter topology. Instead of controlling the DCX output voltage, a boost converter is added in the lower path to regulate the dc bus voltage. If we denote the boost voltage conversion ratio as $M_{boost}(D)$, the system voltage conversion ratio is

$$M = \frac{V_{bus}}{V_{battery}} = M_{boost}(D) + N_{DCX} \tag{3.11}$$

Figure 3.13: Composite converter topology C operation modes



Notice that for boost converter, $M_{boost}(D) \geq 1$. Therefore, to achieve a system conversion ratio $M < 1 + N_{DCX}$, it is required to shut down the DCX (with secondary-side switches shorting the DCX output port) and operate the boost converter alone. This leads to two different operation modes for composite converter C: DCX + boost mode and boost only mode, as depicted in Fig. 3.13.

Comparing with composite converter topology A, the boost module in topology C processes direct power as well as a part of the indirect power. But, in comparison with the conventional boost converter, the boost module processes much less indirect power, with much reduced conversion ratio, and therefore higher efficiency. On the other hand, at low conversion ratios, the boost only mode is more efficient than DCX + buck mode of the composite topologies A and B.

A drawback of composite converter C is that to transition from DCX + boost mode to boost only mode, the DCX module must be shut down abruptly and the boost output voltage must be increased accordingly. This may lead to some difficulties in control. Furthermore, since the DCX output voltage is not controlled, the device voltage stress reduction is relatively small. For the application considered here, the boost module and the DCX module must employ 1200 V devices.

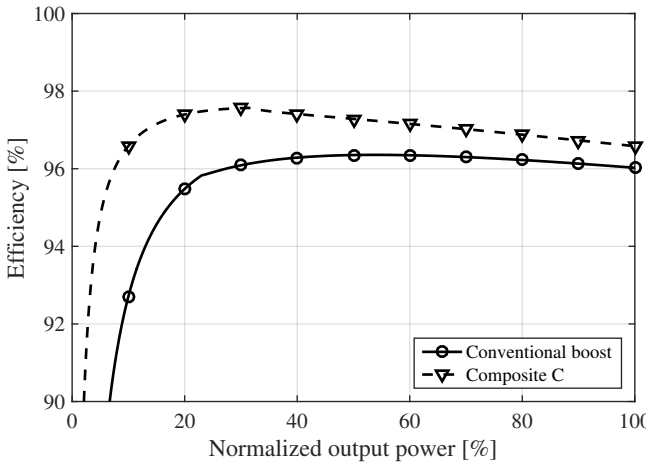
Table 3.3: Composite C Converter Magnetics Design Summary

Inductor	Inductance	108 µH
	Core material	Kool Mu 60u
	Core size	$A_e = 9\,\text{cm}^2$ $l_e = 24.2\,\text{cm}$
	Number of turns	30
	Wire diameter	5.75 mm
Transformer	Core material	PC95
	Core size	$A_e = 9\,\text{cm}^2$ $l_e = 19.4\,\text{cm}$
	Number of turns	6:12
	Wire diameter	primary: 11.51 mm secondary: 8.14 mm

A composite C converter is designed with 1200 V 200 V IGBT modules 2MBI100VA-120-50, because both the DCX and boost module output voltage may exceed 400 V. The transformer turns ratio is chosen to be $N_{DCX} = 2$. The boost module switches at 10 kHz, with $L = 108\,\mu\text{H}$, while the DCX module switches at 30 kHz. Table 3.3 summarizes the magnetics designs. Figure 3.14 plots the predicted efficiency at fixed 200 V input and 650 V output. Though the composite C converter is constructed with all 1200 V IGBT, the efficiency is still higher than that of the conventional boost converter, with significant light load efficiency improvement. It demonstrates that even without

advanced device technology, the composite approach itself can efficiently reduce the ac power loss of the system.

Figure 3.14: Modeled efficiency of composite C converter



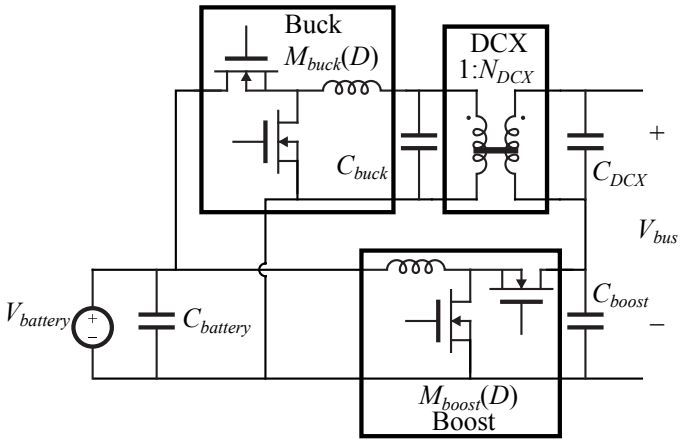
The composite converter C architecture may be attractive in some low-voltage low-power applications where only a narrow input / output voltage range is required. Related configurations, resembling operation with reverse power flow in the modular C architecture, have been reported in [92, 103], where the DCX is implemented using multi-phase LLC resonant converters, and the boost converter is replaced with an isolated PWM converter. The device voltage sharing and the mode transition are less of a concern in the computing or telecommunication applications considered in [92,103] target, with a relatively narrow voltage conversion range, and at lower operating voltages.

3.5 Composite converter architecture D

To address the mode transition problem of composite converter C, the composite converter D is proposed, as shown in Fig. 3.15. A buck converter module is inserted before DCX module to control the DCX output voltage. The buck module output voltage can smoothly ramp down to zero so that the DCX module can be shut down gracefully. If we denote the buck module voltage conversion ratio as $M_{buck}(D_{buck})$, the total system conversion ratio is:

$$M = \frac{V_{bus}}{V_{battery}} = M_{boost}(D_{boost}) + M_{buck}(D_{buck})N_{DCX} \tag{3.12}$$

Figure 3.15: Composite converter topology D



It is not necessary to operate all converter modules together. When the system voltage conversion ratio M is greater than $1+N_{DCX}$, then the buck module can be operated in pass-through with $D_{buck} = 1$, and the system operates in DCX + boost mode. When $M < 1 + N_{DCX}$, the boost module can be operated in pass-through with $D_{boost} = 0$, and the system operates in DCX + buck mode. With the extra buck module, the DCX output voltage can be well controlled, and the dc bus voltage stress can be shared evenly between the DCX and boost modules. Hence, 600 V devices can be employed in all converter modules, with 33% voltage derating. If we define the allowed maximum device voltage stress as $V_{Q,max}$, when the battery voltage $V_{battery} > V_{Q,max}/N_{DCX}$, and bus voltage $V_{bus} > V_{battery} + V_{Q,max}$, the buck module can limit the DCX output voltage stress to $V_{Q,max}$, and the system operates in DCX + buck + boost mode. On the other hand, when $V_{bus} \leq V_{Q,max}$, the system can operate in boost only mode to improve efficiency at low voltage conversion ratios. The operating modes of the composite converter D are depicted in Fig. 3.16.

A 30 kW composite D converter is designed to demonstrate its performance. The transformer turns ratio of DCX is chosen to be $N_{DCX} = 2$, which is the same as that of the composite C converter. Because of the buck module, the voltage stress of all converter modules can be limited to under 400 V. Therefore, the converter is designed with 600 V MOSFET FCH76N60NF. Each switch in the secondary side of DCX module is composed of two MOSFET dies in parallel, while the switches in the rest of the system are composed of five MOSFET dies in parallel each. The

Figure 3.16: Composite converter D operating modes

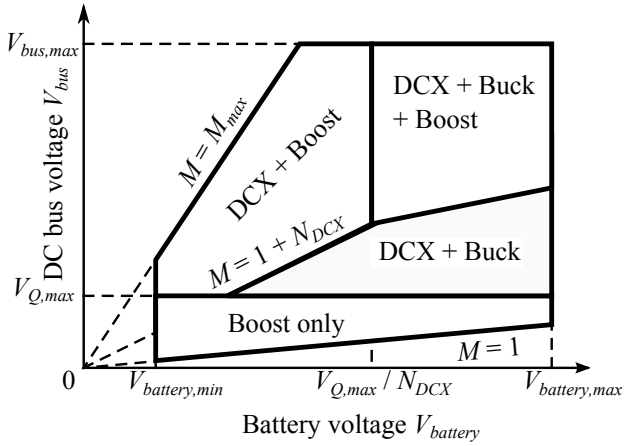


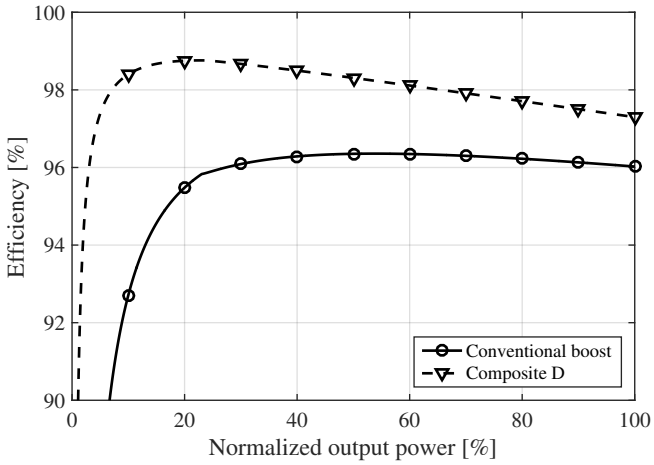
Table 3.4: Composite D Converter Magnetics Design Summary

Inductor	Inductance	72 µH
	Core material	Kool Mu 60u
	Core size	$A_e = 9\,\text{cm}^2$ $l_e = 22.9\,\text{cm}$
	Number of turns	20
	Wire diameter	8.14 mm
Transformer	Core material	PC95
	Core size	$A_e = 9\,\text{cm}^2$ $l_e = 23.4\,\text{cm}$
	Number of turns	6:12
	Wire diameter	primary: 16.27 mm secondary: 5.75 mm

buck and boost modules switch at 20 kHz, both with inductance $L = 72\,\mu\text{H}$, and the DCX module switches at 30 kHz. Table 3.4 summarizes the magnetics design, and Fig. 3.17 plots the efficiency of composite D converter, at fixed 200 V input and 650 V output.

It should be noted that the series combination of the buck and DCX modules of Fig. 3.15 could be replaced by a dual active bridge module. This would lead to a reduced switch count. However, we have observed higher laboratory efficiencies with the configuration shown in Fig. 3.15.

Figure 3.17: Modeled efficiency of composite D converter



3.6 Comparison of converter approaches

In this section, the performance of different composite converter architectures are evaluated and are compared with prior boost converter approaches.

3.6.1 Generic comparison

For a given converter topology, the choices of semiconductor devices, switching frequency, magnetics design, and many other design parameters can result in very different physical designs. Nevertheless, it is beneficial to compare the different converter approaches in a more generalized way, in order to gain higher-level insights that guide design decisions.

To quantify the semiconductor device usage in different converter approaches, a specified device power rating is introduced as

$$P_{Dn} = \frac{\sum I_{device,rms} V_{device,max}}{P_{out,max}} \tag{3.13}$$

which is the sum of all device rms currents multiplied by device voltage ratings, normalized to the converter maximum output power. This can be regarded as a measure of how well the power devices are utilized in a given converter topology.

Table 3.5 shows a comparison of the normalized total specified device power for the converter

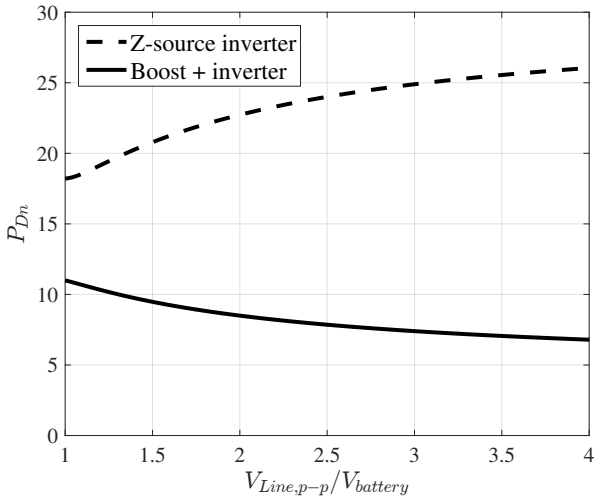
Table 3.5: Converter Specified Device Power Rating P_{Dn} Comparison at fixed Voltage Conversion Ratio $M = 3.25$

	Boost	SAZZ	Coupled inductor	Three-level	Comp. A	Comp. B	Comp. C	Comp. D
N_{DCX}	–	–	–	–	1.5	1	2	2
Specified device power P_{Dn}	5.55	5.55	5.55	5.35	7.84	7.29	5.03	5.13

approaches considered in the previous sections, at a fixed voltage conversion ratio $M = 3.25$. At this voltage conversion ratio, with 200 V battery voltage, the bus voltage is 650 V, which is a typical operating point for the powertrain system. The calculation ignores the inductor current ripple, and therefore it is independent of the choice of magnetics, switching frequency, and device technology. Typical DCX transformer turns ratios N_{DCX} are chosen for the composite converter designs; these are optimized for the powertrain application. The data of Table 3.5 indicates that the soft-switching approach and the coupled inductor approach exhibit the same device power rating as the conventional boost converter, which implies that their designs may require the same total device semiconductor area. The three-level converter device power rating is slightly smaller than in the conventional boost converter. Although the composite approach requires the increased power device component count, composite converter C and composite converter D show even smaller total device power ratings than the other approaches. This implies that the total semiconductor areas for the composite converters C and D could be similar to the other approaches, if not smaller. Table 3.5 also implies that the composite converters A and B may not utilize the semiconductor devices as efficiently as the other approaches.

The Z-source inverter combines the functions of the boost DC-DC converter and the inverter. Therefore, a separate comparison must be made to quantify the performance of the Z-source inverter. Fig. 3.18 compares the total device power rating of Z-source inverter against the conventional boost converter cascaded by a standard inverter. For both cases, it is assumed that sinusoidal pulse-width modulation (SPWM) is employed in the inverter, and the load is assumed to have unity power factor. The normalized total device power rating is plotted against the battery-to-machine voltage

Figure 3.18: Specified device power rating comparison between Z-source inverter and conventional boost cascaded with inverter approach



conversion ratio $V_{Line,p-p}/V_{battery}$. Figure 3.18 implies that the semiconductor device utilization for Z-source inverter is relatively poor. For a given semiconductor device area, the Z-source inverter results in much larger device conduction losses, which agrees with conclusions in [11, 36].

To quantify the capacitor size for a given converter topology, the normalized total capacitor power rating is defined as

$$P_{Cn} = \frac{\sum I_{cap,rms-max} V_{cap,max}}{P_{out,max}} \tag{3.14}$$

which is the sum of all capacitor rms current ratings multiplied by the capacitor voltage ratings, and is normalized to the converter maximum output power. In the electrified vehicle application, film capacitors are usually used, and the converter system is typically thermally limited. Therefore, the capacitor size is usually limited by its rms current rating rather than its capacitance. Additionally, the voltage rating affects the size and cost of the capacitors as well. Therefore, the total capacitor power rating reflects the size and cost of the capacitors in a given converter topology.

For example, in a conventional boost converter, let us assume that the inductor is very large,

Table 3.6: Converter Total Capacitor Power Rating Comparison with $M_{max} = 4$

	Boost	SAZZ	Coupled inductor	Three-level	Comp. A	Comp. B	Comp. C	Comp. D
N_{DCX}	–	–	–	–	1.5	1	2	2
Normalized total capacitor power P_{Cn}	2	2	1	4	0.75	1	1.5	1

and the inductor current ripple is ignored. The output capacitor rms current is

$$I_{Cout,rms} = I_{in}\sqrt{D\left(1-D\right)} \leq \begin{cases} \dfrac{P_{out,max}}{2V_{in}} & \text{for } M_{max} \geq 2 \\ \dfrac{P_{out,max}\sqrt{M_{max}-1}}{M_{max}V_{in}} & \text{for } 1 \leq M_{max} < 2 \end{cases} \tag{3.15}$$

The output capacitor voltage is

$$V_{Cout} = V_{out} \leq V_{in}M_{max} \tag{3.16}$$

Therefore the normalized total capacitor power rating of the conventional boost converter is

$$P_{Cn} = \frac{I_{Cout,rms-max}V_{Cout,max}}{P_{out,max}} = \begin{cases} \dfrac{M_{max}}{2} & \text{for } M_{max} \geq 2 \\ \sqrt{M_{max}-1} & \text{for } 1 \leq M_{max} < 2 \end{cases} \tag{3.17}$$

With the maximum voltage conversion ratio of $M_{max} = 4$ specified, the conventional boost converter exhibits $P_{Cn} = 2$. Since the inductor current ripple is ignored in this analysis, the result is independent of inductor design, switching frequency, or device technology: it is simply the property of the converter topology itself. The normalized total capacitor power ratings of different converter approaches with maximum voltage conversion ratio $M_{max} = 4$ are compared in Table 3.6. The capacitor power rating is reduced by a factor of two in the coupled-inductor approach, because it is basically an interleaved two-phase boost converter. Although the composite approach requires an increased capacitor component count, the composite converters A, B, and D can achieve a factor of two reduction in capacitor power rating reduction. Composite converter C requires a slightly larger capacitor power rating, although it is still 25% smaller than for the conventional boost converter. It is important to note that the capacitor power rating of the three-level converter is two times larger

than for the conventional boost approach, because of the high current stress in the additional flying capacitor. This is a significant disadvantage of the three-level boost converter in the electrified vehicle application.

These generic comparisons illustrate some fundamental properties of the considered converter approaches, which are independent of switching frequency and device technology. However, other factors such as device switching loss, and magnetics loss and size should also be considered in a practical design as well. Therefore, it is useful to compare different converter approaches using example physical designs, as described in the following sections.

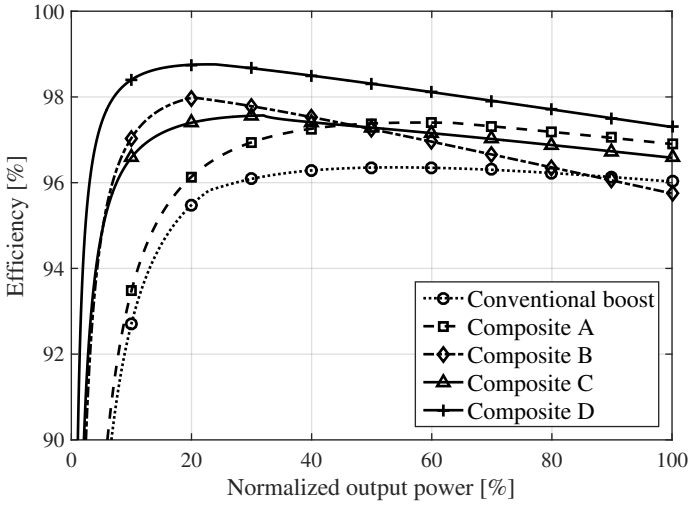
3.6.2 Composite converter comparisons

To evaluate the performance of different composite converter topologies, the efficiencies of the physical designs, as documented in section 3.2 – 3.5, are compared. The efficiencies of different converters are plotted in Fig. 3.19, with fixed 200 V input and 650 V output, which is a typical operation point for powertrain application. Because of different worst-case voltage stresses in different converters, the composite B & D converters are designed with 600 V MOSFETs, the composite C converter is designed with 1200 V IGBTs, and the composite A is a hybrid of 600 V MOSFETs and 1200 V IGBT.

In general, composite topology A shows better efficiency than the conventional boost converter, though the improvements at light loads are not very significant. The composite converter B shows a significant efficiency improvement over the conventional boost converter at light load, although the heavy load efficiency is worse. This is primarily a consequence of the increased conduction loss of the non-inverting buck-boost module. The composite converter C efficiency curve in Fig. 3.19 achieves a substantial efficiency improvement over the conventional boost approach, in spite of the need to employ 1200 V Si IGBTs. The predicted efficiency curve of composite converter D achieves the best efficiency among all composite converter architectures, with a loss reduction of approximately 50% at medium load. Therefore, the rest of this work mainly focus on the design of composite D converter, though the other composite converters still have potential applications in

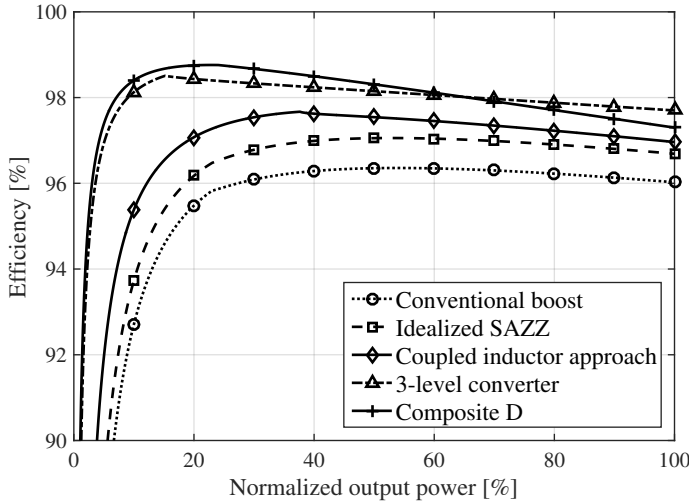
other areas.

Figure 3.19: Comparison of predicted composite converter efficiencies at fixed 200 V input voltage and 650 V output voltage.



3.6.3 Comparison with efficiencies of prior approaches

Figure 3.20: Boost converter efficiency comparison of different approaches with fixed 200 V input and 650 V output



The efficiencies of the prior-art SAZZ, coupled-inductor, and three-level approaches, as documented in section 2.2 – 2.4, are compared with the conventional boost approach as well as with the proposed composite D converter approach. For the application of powertrain system concerned

in this work, where relatively large boost ratio with maximum 800 V output voltage is required, the Z-source inverter requires 2100 V devices. It is concluded that the Z-source inverter is not a competitive solution for this application. Figure 3.20 plots the efficiency vs. power for the different approaches at a fixed 200 V input and 650 V output.

The SAZZ approach efficiency curve is generated by assuming the soft-switching efficiency is $\eta_{ss} = 50\%$. This is an optimistic assumption, since the previously reported η_{ss} was less than 40% [95], and the increased losses in the added magnetics and semiconductor devices are ignored. However, even with these idealized assumptions, the overall system efficiency improvement is modest: approximately 0.7% at medium load, as compared against the conventional boost approach.

The coupled inductor approach improves the medium to heavy load efficiency by approximately 1.2% relative to the conventional approach. Even with additional transformer loss, the total magnetics loss is nonetheless slightly reduced. However, the predicted efficiency is still much lower than the results reported in [42]. This is because in [42], operating voltages are lower, and 600 V MOSFETs with SiC Schottky diode were therefore used. The switching frequency is increased to 45 kHz, and the magnetics can be designed with ferrite cores and substantially reduced magnetics loss. For the operating voltages considered here, silicon 1200 V IGBTs exhibit much higher switching losses, the switching frequency is limited to 10 kHz, and the magnetics loss is substantially increased. It can be concluded that the coupled inductor approach is more advantageous in relatively low voltage applications. These advantages could extend to higher voltages based on emerging higher voltage SiC MOSFET devices.

The efficiency of the three-level converter is substantially improved relative to the conventional boost approach. The ability to employ 600 V MOSFETs enables lower conduction and switching losses compared to IGBTs. Because of the higher switching frequency and reduced volt-seconds applied to the inductor by the three-level switching waveform, the magnetics loss is also further reduced. Compared with the conventional boost, the three-level converter efficiency at medium to heavy load is improved by approximately 1.8% with 600 V MOSFETs, and the loss is reduced by a factor of approximately two. It can be observed that the three-level converter efficiency is very

close to the efficiency of the composite converter D. Composite converter D shows slightly higher efficiency at medium to light load, while the three-level converter shows slightly higher efficiency at heavy load. It should be noted, however, that the three level converter requires substantially larger capacitors, as shown in Table 3.6, and discussed further in the next section.

3.6.4 Comparison of average efficiency over standard driving test cycles

Improvement of the efficiency of indirect power conversion, via the composite converter approach, can lead to significant mission-related performance improvements. In the electrified vehicle application, the composite converter approach can lead to substantial improvements in efficiency and total power loss under actual driving conditions. Especially noteworthy is the improvement in low-power efficiency and its influence on the total loss. In this section, the impact of the composite converter approach is estimated for three standard US EPA drive cycles: UDDS (city driving), HWFET (highway driving), and US06 (aggressive driving). Significant and non-incremental improvements in total loss and in converter quality factor Q are predicted; these could lead to improvements in MPGe, in cooling system size and weight, and in system cost.

Based on the electric vehicle model developed in section 1.4.1, and the voltage-power relationships illustrated in Fig. 1.9 – 1.11, the performances of different converter approaches under different driving cycles are simulated. Table 3.7 documents the simulated drive cycle converter quality factor

$$Q = \frac{\int |P_{out}| \, \mathrm{d}t}{\int P_{loss} \, \mathrm{d}t} \tag{3.18}$$

for the different converter approaches. The loss and power throughput are integrated over each drive cycle to compute an average Q. In all three different driving profiles, both the three-level converter

Table 3.7: Converter Quality Factor Q For Standard Driving Cycles

	Boost	SAZZ	Coupled inductor	Three-level	Composite D
UDDS	38.6	44.9	62.4	117.5	74.5
HWFET	17.5	20.2	35.5	71.4	75.2
US06	21.9	26.4	34.0	57.7	67.1

Table 3.8: Converter Size Comparison

	Boost / SAZZ	Coupled inductor	Three-level	Composite D
Semiconductor devices	2×(1200 V 200 A IGBT + 1200 V 200 A diode)	4×(1200 V 100 A IGBT + 1200 V 100 A diode)	48×(600 V 46 A MOSFET die)	48×(600 V 46 A MOSFET die)
Total magnetics core volume	360 cm^3	360 cm^3	195 cm^3	360 cm^3
Total capacitor power rating	85 kVA	45 kVA	160 kVA	51 kVA
Total capacitor energy rating*	162 J	42 J	242 J	25 J

*assume worst-case ±5 V output voltage ripple.

and composite converter D show significant efficiency improvements over the conventional boost converter. In the UDDS urban driving test, the converter quality factor of composite converter D is almost twice of that of conventional boost converter, which means the power throughput per unit loss of composite converter D is almost doubled. With the HWFET highway driving test, the converter quality factor of composite converter D is increased by more than a factor of four relative to the conventional boost converter. Under the US06 driving test, the converter quality factor is increased by more than a factor of three as well. The three-level converter out-performs composite D converter in the low speed UDDS driving test, while the composite converter D shows higher converter quality factor in high speed HWFET and US06 driving tests. However, as illustrated in the following section, the three-level converter requires much larger capacitor modules, which are challenging to implement, and can significantly increase the system size and cost.

3.6.5 Converter size comparison

Table 3.8 compares composite converter D with prior approaches in terms of total semiconductor devices, total magnetics core volume, total capacitor power rating, and total capacitor energy rating. In terms of semiconductor devices, the boost converter uses two silicon 1200 V 200 A IGBT modules. The SAZZ approach will use roughly the same semiconductor devices, if the extra aux-

iliary switch elements are ignored. The coupled inductor approach uses four silicon 1200 V 100 A IGBT modules, and is similar to the conventional approach in total device area. Both the three-level converter and composite converter D use silicon 600 V 46 A MOSFETs, and both employ a total of 48 MOSFET dies. The semiconductor utilization in all approaches is similar.

Regarding the total magnetic core volume, the total core volume of the SAZZ approach can be taken to be the same as in the conventional boost approach, if the magnetics of the active snubber is ignored. The coupled inductor approach basically takes the conventional boost inductor, and splits it into one smaller inductor and one transformer. Therefore, the total magnetics size is unchanged. Because the three-level converter reduces the applied inductor volt-seconds, the inductor size is reduced by 65%. The composite converter D total magnetic core volume is designed to be the same as in the conventional boost approach.

As noted previously, the capacitor rms current rating typically is the dominant constraint limiting the size of the capacitors in electrified vehicle applications. The total capacitor power rating ($I_{cap,rms-max}V_{cap,max}$ summed over all capacitors) is a good measure of the volume and cost of the capacitor module. The power ratings listed in Table 3.8 include details such as inductor current ripple and DCX non-trapezoidal transformer current waveforms, which cause the data in Table 3.8 to be somewhat higher than the idealized data of Table 3.6. In Table 3.8, the total capacitor energy rating is also calculated, based on designs that result in ± 5 V worst-case output voltage ripple. The snubber capacitor of the SAZZ approach is ignored. Therefore, the SAZZ approach requires roughly the same capacitor power and energy rating as the conventional boost converter. The coupled inductor approach is basically a two-phase interleaved converter, and therefore the capacitor power rating is reduced by 47%, while the energy rating is only a quarter of that in the conventional boost approach. The three-level converter requires a flying capacitor which carries a large rms current at a voltage rated half of the output bus voltage. For the 30 kW design considered here, a 200 Arms 400 V capacitor is required. This may substantially increase the system size and cost. Relative to the conventional boost, the capacitor power rating is increased by 91%, while the energy rating is increased by 49%, even though it switches at a higher frequency. In contrast,

although the composite converter D increases the number of capacitors required, the capacitor voltage rating is much reduced. Further, because the indirect power path is processed with a DCX module having a quasi-square wave converter with very small current ripple, the capacitor rms current rating and voltage ripple can both be reduced. This leads to a 40% reduction in the total capacitor power rating. The composite converter D also achieves an 85% reduction in the total capacitor energy rating.

In a typical electrified drive train system, the film capacitor modules exhibit higher volume and cost than the magnetics. For example, the capacitor module of the Prius 2004 has volume larger than 6 L, while the remainder of the converter module has volume of 1.1 L [89]. Therefore, although the three-level converter approach achieves excellent efficiency, it leads to significantly increased system size and cost because of the large flying capacitor. Other multi-level approaches such as [29] suffer from this issue as well. It should be noted that deployment of more advanced device technologies, such as GaN or SiC transistors [77] with higher switching frequencies, does not address the issue of capacitor rms current rating, and therefore would not lead to reduced capacitor size and cost. Hence, the composite converter approach achieves a combination of substantially reduced loss and substantially reduced capacitor size and cost. Non-incremental improvements can be achieved, relative not only to the conventional boost converter but also relative to other candidate approaches such as the three-level, SAZZ, and coupled-inductor circuits.

Chapter 4

DC Transformer and Efficiency-Enhanced Dual Active Bridge

DC Transformer (DCX) is the key component in the composite converter approach, which processes most of the indirect power efficiently. This chapter is dedicated to various technical details of the DCX, including its operation, modeling, and efficiency improvements.

Physically a transformer only works with AC voltages. If the primary / secondary voltages and currents in a two-winding transformer are denoted as v_1, v_2, i_1, and i_2, the relationship between the primary and secondary port is:

$$v_1 N_2 = v_2 N_1 \tag{4.1}$$

$$i_1 N_1 = i_2 N_2 \tag{4.2}$$

where N_1 and N_2 are the transformer turns ratio of primary and secondary side.

The mathematical model of the transformer can be extended to "generalized transformer [4]" to describe a large family of power electronics converters. In particular, the DC transformer is widely used to model the behavior of a DC-DC converter [33]. Basically all the isolated DC-DC converters can be regarded as a DC transformers with variable turns ratio.

In modern literature the term "DC Transformer" (or DCX) often refers to the type of intermediate isolated converter stage with fixed voltage conversion ratio. The DCX is usually designed to achieve very high efficiency, with unregulated voltage. For example, in [47], the DCX is implemented as a parallel resonant converter (PRC). An *LLC* resonant converter based DCX is proposed in [35], while the realization with class-E resonant converter is reported in [85]. Other different res-

onant converters [2, 83] can be utilized as DCX as well. DCX is a popular choice as an unregulated intermediate bus converter for data-center, computer and telecommunication systems [92, 97, 100]. In combination with regulating converter stages, such as buck, boost, or non-inverting buck-boost, the DCX can also be applied as a system module in applications such as photovoltaic systems [51].

Instead of realizing the DCX with resonant converters, in this work DCX is implemented as quasi-square wave converter. In specific, the Dual Active Bridge (DAB) converter [27] operated unregulated at 50% duty cycle and with passive secondary-side rectification is considered. Its conversion ratio approximately equals to the transformer turns ratio [49]. With proper design, DAB can achieve zero-voltage switching (ZVS) in both primary and secondary sides, with much reduced switching loss. Comparing to resonant converters, the voltage and current stresses in DAB is also much reduced. As a matter of fact, with proper design, the DAB can have minimum possible voltage and current stresses on all components. Therefore, it is more appropriate for high power applications such as in electrified automotive powertrain. When operating with trapezoidal transformer current waveform and zero voltage switching (ZVS) of all devices, the DAB based DCX can achieve very high efficiencies [25].

The DCX design is the crucial part of the composite converter design. In this chapter, the detailed DAB based DCX operation is modeled. Similar to many other soft-switching converters, at the light load condition the DCX primary side may lose ZVS, due to reduced tank inductor energy [19,44]. This issue is addressed in section 4.4. Section 4.5 discusses synchronous rectification. A novel efficiency-enhanced DAB control algorithm is proposed in section 4.6, which improves the DCX efficiency over all power range, and reduces the power loss at light load by a factor of ten.

4.1 DCX operation and simplified model

In this section, the simplified DCX operation will be discussed. In Section 4.1.1 we will start from the case of ideal active rectification to introduce the phase-shift controlled operation of DCX. Then a more sophisticated case with passive rectification will be analysed in Section 4.1.2.

4.1.1 Ideal active rectification

Figure 4.1: The DC Transformer (DCX) converter schematic, with implementation as Dual Active Bridge (DAB).

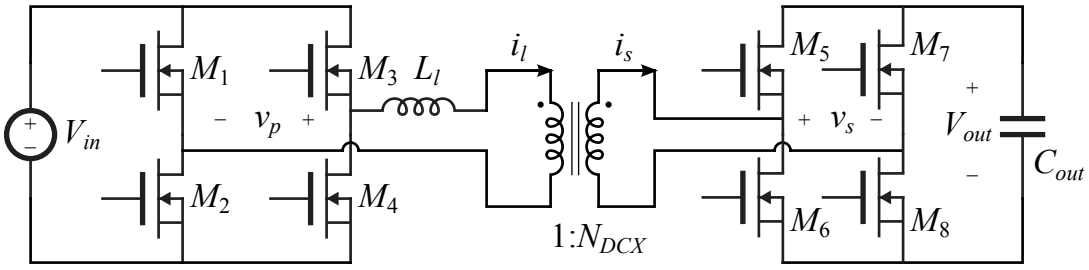
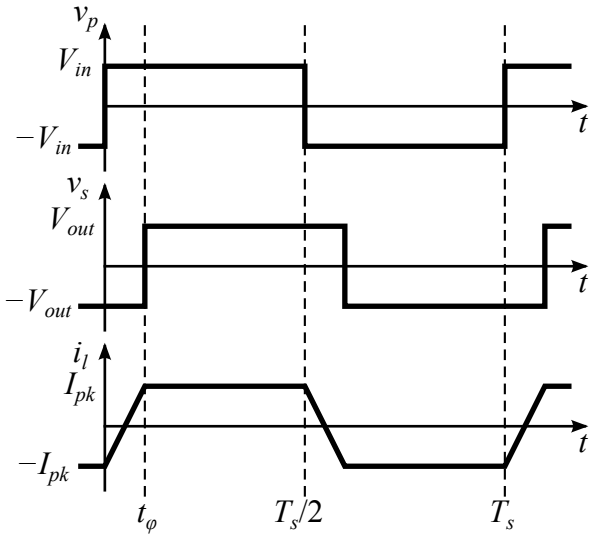


Figure 4.1 illustrates one of the DCX realization as a Dual Active Bridge (DAB) converter. The primary side full bridge (M_1 – M_4) chop the input DC voltage V_{in} with 50% duty cycle. v_p is the AC voltage with symmetric rectangular waveform, which can pass through the transformer. The secondary side full bridge (M_5 – M_8) rectify the AC voltage back to DC voltage V_{out}. L_ℓ is the tank inductor that assists the soft switching and limits the $\mathrm{d}i/\mathrm{d}t$ of the transformer current. It can be realized as either a separate inductor, or integrated into the transformer as leakage inductance. If the DAB is properly controlled, it can achieve $V_{out} = N_{DCX}V_{in}$, where N_{DCX} is the transformer turns ratio. At this condition, the simplified operation waveform is sketched in Fig. 4.2.

Figure 4.2: Simplified DAB operation waveform, assuming it is controlled so that $V_{out} = N_{DCX}V_{in}$.



In Fig. 4.2, T_s is the switching period. t_φ is the phase shift duration between primary and secondary sides. If we denote $\varphi \triangleq 2t_\varphi/T_s$, which is the relative phase shift, then

$$I_{pk} \approx \frac{N_{DCX} I_{out}}{1-\varphi}, \tag{4.3}$$

where I_{out} is the output current. Therefore, as long as $\varphi \ll 1$, the components current stresses are close to minimum, and very small conduction loss is expected. On the other hand, it is easy to verify that

$$I_{out} \approx \frac{V_{in} T_s}{2 N_{DCX} L_\ell} \cdot \varphi\,(1-\varphi)\,. \tag{4.4}$$

The output power is controlled by the phase shift, and the maximum output current is approximately

$$I_{out,max} \approx \frac{V_{in} T_s}{8 N_{DCX} L_\ell}. \tag{4.5}$$

4.1.2 Passive rectification

Instead of actively controlling the phase shift, the DAB converter operation can be simplified with secondary side passive rectification, as illustrated in Fig. 4.3. In this case, the phase shift is passively determined by the secondary side diodes.

Figure 4.3: The DC Transformer (DCX) converter schematic, with implementation as Dual Active Bridge (DAB) with secondary side passive rectification.

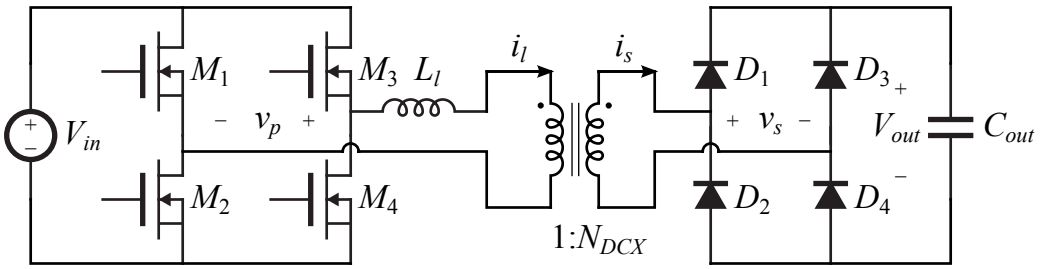


Figure 4.4 sketches half switching period of the simplified tank inductor current waveform of the converter in Fig. 4.3, in a more general scenario where $V_{out} \neq N_{DCX} V_{in}$. It is convenient to define the normalized voltage conversion ratio

$$M \triangleq \frac{V_{out}}{N_{DCX} V_{in}}. \tag{4.6}$$

With secondary side passive rectification, the phase shift t_φ is composed of two durations: t_0 where the tank inductor current ramps from $-I_{pk}$ to zero, and the diode reverse recovery time t_{rr} [12,57,64], which is a property of the device. Same as in previous case, during the phase shift, the voltage-second applied to the tank inductor is $\lambda_\ell = V_{in}\,(M+1)\,t_\varphi$. The current I_{pk} and I_{rr} thus can be derived as

$$I_{pk} = t_0 \cdot \frac{V_{in}\,(M+1)}{L_\ell} \tag{4.7}$$

$$I_{rr} = t_{rr} \cdot \frac{V_{in}\,(M+1)}{L_\ell}. \tag{4.8}$$

Since $V_{out} \neq N_{DCX} V_{in}$, the voltage-second applied to the tank inductor during the main conduction period is no longer zero. The tank inductor current ramps up or down with the slope $V_{in}\,(1-M)\,/L_\ell$. To guarantee that the inductor current waveform is continuous, it is required that

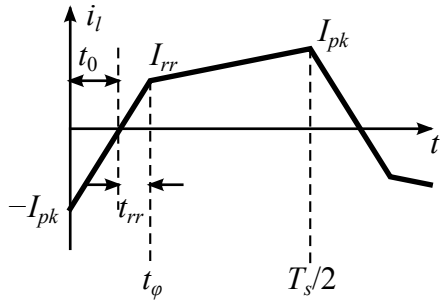
$$I_{pk} - I_{rr} = \frac{V_{in}\,(1-M)}{L_\ell} \cdot \left(\frac{T_s}{2} - t_0 - t_{rr}\right). \tag{4.9}$$

On the other hand, the converter output capacitor charge should be balanced. Therefore,

$$Q = \frac{1}{2} t_0 I_{pk} - \frac{1}{2} t_{rr} I_{rr} + \frac{1}{2}\,(I_{pk} + I_{rr}) \cdot \left(\frac{T_s}{2} - t_0 - t_{rr}\right) = N_{DCX} I_{out} \frac{T_s}{2} \tag{4.10}$$

Solving equations (4.7) – (4.10) together allows M to be found, and the converter steady state operation point is obtained.

Figure 4.4: Simplified tank inductor current waveform of DAB operation with secondary side passive rectification.



The solutions of equations (4.7) – (4.10) require the knowledge of diode reverse recovery time t_{rr}. The device data sheet usually provides a typical value of the diode reverse recovery time.

However, the actual diode reverse recovery time is governed by the diode charge equation [54, 63]:

$$\frac{\mathrm{d}q_D}{\mathrm{d}t} = -\frac{q_D}{\tau} + i_D, \tag{4.11}$$

where q_D is the junction charge, i_D is the diode current, and τ is the diode minority carrier lifetime. The diode turns off when $q_D = 0$. If the diode current has a ramp waveform as in Fig. 4.4, and with the assumption that $q_D(0) = i_D(0)\,\tau_L$, the reverse recovery time is approximately described by the equation [49]

$$t_{rr} = \tau \cdot \left(1 - e^{-\frac{t_0 + t_{rr}}{\tau}}\right). \tag{4.12}$$

Notice that equation (4.12) has the explicit solution

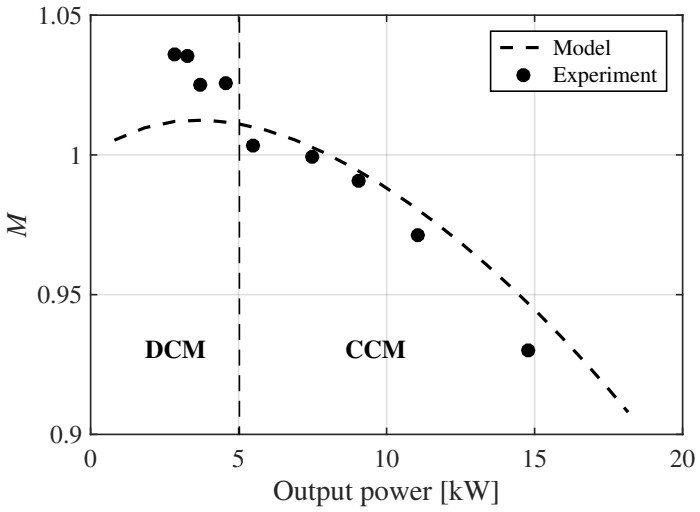
$$t_{rr} = \tau \cdot \left(1 - W_0\left(-e^{-\left(\frac{t_0}{\tau}+1\right)}\right)\right) \tag{4.13}$$

where W_0 is the main branch of the Lambert W-function [24]. The complete converter steady state solution requires solving equations (4.7) – (4.10) and (4.13) altogether. It is obvious that the solution requires the knowledge of diode minority carrier lifetime τ. For a given diode, usually the data sheet provides the typical reverse recovery time together with the test conditions. Based on this information $t_{rr,typ}$ and $t_{0,typ}$ can be obtained, and the device minority carrier lifetime can be solved by substituting $t_{rr,typ}$ and $t_{0,typ}$ into equation (4.12):

$$\tau = \frac{t_{rr,typ}}{1 + \frac{t_{rr,typ}}{t_{0,typ}+t_{rr,typ}} \cdot W_0\left(-\left(1 + \frac{t_{0,typ}}{t_{rr,typ}}\right) e^{-\left(1+\frac{t_{0,typ}}{t_{rr,typ}}\right)}\right)} \tag{4.14}$$

Figure 4.5 shows the modeled DCX voltage conversion ratio plotted with the measurement data. This is a 20 kW DCX implemented as DAB converter with secondary side passive rectification, and the transformer turns ratio $N_{DCX} = 2$. The normalized voltage conversion ratio M is modeled and measured at different output power level, with fixed 200 V input voltage. The model matches measurement data well at medium to heavy load, but deviate from the experimental result at light load. This is because this model only considers the continuous conduction mode (CCM), while the DCX actually enters discontinuous conduction mode (DCM) at light load. As pointed out in [49], at

Figure 4.5: Normalized DCX voltage conversion ratio model and measurement at different output power level, with fixed 200 V input voltage. The transformer turns ratio $N_{DCX} = 2$.



DCM the initial condition assumption $q_D(0) = i_D(0)\tau_L$ of the charge equation (4.11) is no longer valid, and equations (4.12) & (4.13) are no longer appropriate as well.

As shown in Fig. 4.5, the DCX normalized voltage conversion ratio M becomes greater than one at light load, and smaller than one at heavy load. When $M = 1$, $I_{pk} = I_{rr} \approx N_{DCX} I_{out} / (1 - \varphi)$. Therefore, at $M = 1$, the tank inductor rms current is minimized, and very small conduction loss is expected. On the other hand, at $M = 1$, the tank inductor voltage-second at main conduction period is zero, and the tank inductor core loss is much reduced. In general, it is expected that DCX exhibits very good efficiency at $M = 1$. In this specific design, the tank inductor is chosen so that $M = 1$ occurs around 7 kW – 10 kW, where the peak efficiency is achieved.

Comparing to regulated DAB ([9, 48, 61, 76]), where M can significantly deviate from unity, the unregulated (or efficiency-regulated [25]) DAB always has M close to one. The unregulated DAB exhibits much reduced conduction loss comparing to regulated DAB. On the other hand, to achieve certain voltage ratio, the regulated DAB has to sacrifice ZVS with increased switching loss [60]. Therefore, the unregulated DAB or DCX always demonstrates much higher efficiency than the regulated DAB.

4.2 DCX soft switching analysis

A very important property of DCX is that it is capable of soft switching on both primary and secondary sides, which significantly reduces the switching loss. There are two types of soft switching: zero voltage switching (ZVS) and zero current switching (ZCS). In this section, the detailed DCX soft switching behavior is analyzed. In Section 4.2.1, with the assumption of linear device output capacitance, the technique of state plane analysis is deployed to illustrate the ZVS operation. However, since in practice the device output capacitance is always nonlinear, Section 4.2.2 discusses the method that can be applied to nonlinear systems.

4.2.1 Ideal resonance analysis

Figure 4.6: Detailed DCX operation waveform with resonant transitions considered.

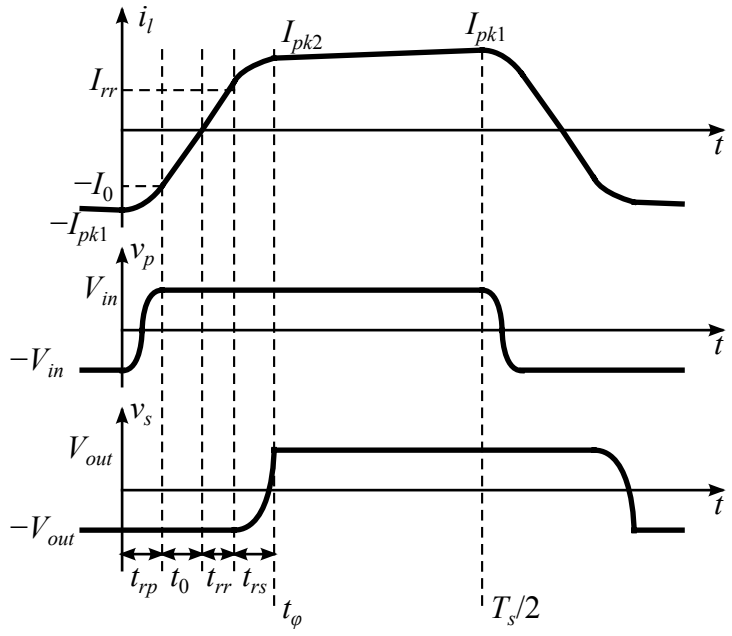
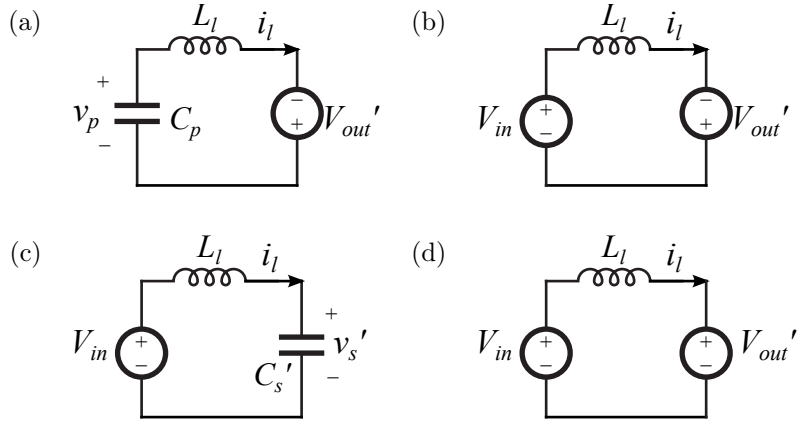


Figure 4.6 sketches the detailed DCX operation waveform. Comparing with Fig. 4.4, Fig. 4.6 include the resonant transitions during switch commutation.

When $t < 0$, M_1, M_4, D_2, and D_3 are on. $v_p = -V_{in}$, and $v_s = -V_{out}$. At $t = 0$, M_1 and M_4 turn off. The equivalent circuit at this moment is shown in Fig. 4.7(a). Here C_p is the equivalent

Figure 4.7: DCX equivalent circuits during commutation: (a) during t_{rp}, the primary-side resonant commutation; (b) during t_0 and t_{rr}; (c) during t_{rs} , the secondary-side resonant commutation; and (d) the main conduction period.



capacitance seen between the primary side switching nodes. It is composed of device output capacitance, package and printed circuit board stray capacitance, as well as any extra capacitance added to slow down the switching nodes $\mathrm{d}v/\mathrm{d}t$ during commutation. $V'_{out} \triangleq V_{out}/N_{DCX} = MV_{in}$, which is the output voltage reflected to primary side. Therefore, during t_{rp}, L_ℓ and C_p form a resonant circuit. The state equation of this circuit can be written as:

$$\begin{bmatrix} \dot{v}_p \\ \dot{i}_\ell \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{C_p} \\ \frac{1}{L_\ell} & 0 \end{bmatrix} \begin{bmatrix} v_p \\ i_\ell \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{MV_{in}}{L_\ell} \end{bmatrix}. \tag{4.15}$$

At t_{rp}, v_p reaches V_{in}, the body diodes in M_2 and M_3 turns on, and clamps v_p to V_{in}. After that, M_2 and M_3 can turn on with ZVS, which is free of switching loss. During t_0 and t_{rr}, $v_p = V_{in}$ and $v'_s = MV_{in}$, where $v'_s \triangleq v_s/N_{DCX}$, which is v_s reflected to primary side. The equivalent circuit is shown in Fig. 4.7(b). Therefore, the inductor current ramps up with the slope of $(M+1)\,V_{in}/L_\ell$, until D_2 and D_3 turn off after t_{rr}.

The equivalent circuit during t_{rs} is shown in Fig. 4.7(c), where $C'_s \triangleq C_s N_{DCX}^2$, which is the equivalent capacitance seen between the secondary switching nodes, reflected to primary side. The

state equation during this transition can be written as:

$$\begin{bmatrix} \dot{v}'_s \\ \dot{i}_\ell \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{C'_s} \\ -\frac{1}{L_\ell} & 0 \end{bmatrix} \begin{bmatrix} v'_s \\ i_\ell \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{V_{in}}{L_\ell} \end{bmatrix}. \tag{4.16}$$

After t_{rs}, v_s reaches V_{out}, and D_1 and D_4 turn on. The equivalent circuit is shown in Fig. 4.7(d). The tank inductor current ramps with the slope $(1 - M)\, V_{in}/L_\ell$.

Therefore, the DCX commutation is a multi-resonant process, which involves the resonance of C_p–L_ℓ and C'_s–L_ℓ. If C_p and C'_s are constant capacitance, the states in equations (4.15) & (4.16) can be plotted in the normalized state planes as those in Fig. 4.8.

Figure 4.8: DCX state plane plots: (a) the m_p–j_ℓ plane; (b) the m'_s–j_ℓ plane.

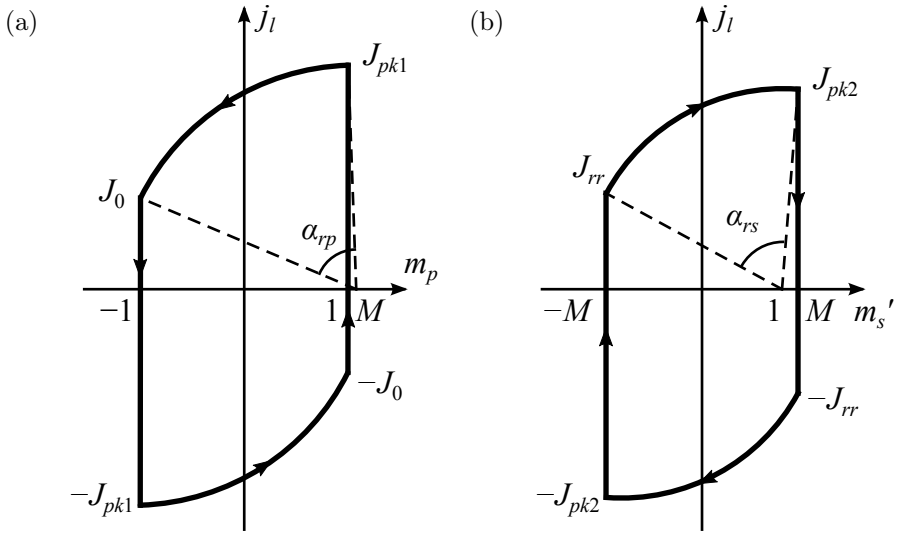
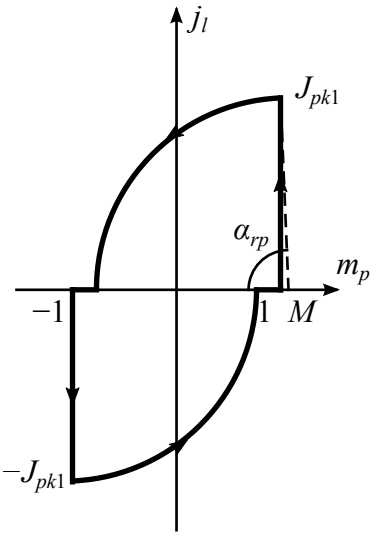


Figure 4.8 is sketched under the condition that $M > 1$. In Fig. 4.8(a), v_p and i_ℓ are normalized into m_p and j_ℓ. According to equation (4.15), $Z_{0p} = \sqrt{L_\ell/C_p}$, and $\omega_{0p} = 1/\sqrt{L_\ell C_p}$. It is chosen that $V_{base} = V_{in}$, therefore $m_p = v_p/V_{in}$, and $j_\ell = i_\ell Z_{0p}/V_{in}$. Similarly, $J_{pk1} = I_{pk1} Z_{0p}/V_{in}$, and $J_0 = I_0 Z_{0p}/V_{in}$. During the primary side resonant transition, the m_p–j_ℓ trajectory is an arc from $(1, J_{pk1})$ to $(-1, J_0)$. The arc has the center at $(M, 0)$, with angle $\alpha_{rp} = t_{rp}/\omega_{0p}$. The m_p–j_ℓ trajectory circles counter-clockwise. This is because with positive power flow, the primary side is an active chopper (inverter).

In Fig. 4.8(b), v'_s and i_ℓ are normalized into m'_s and j_ℓ, according to equation (4.16). $Z_{0s} = \sqrt{L_\ell/C'_s}$, and $\omega_{0s} = 1/\sqrt{L_\ell C'_s}$. The chosen base voltage $V_{base} = V_{in}$ keeps the same. $m'_s = v'_s/V_{in}$,

and $j_\ell = i_\ell Z_{0s}/V_{in}$. Similarly, $J_{pk2} = I_{pk2}Z_{0s}/V_{in}$, and $J_{rr} = I_{rr}Z_{0s}/V_{in}$. During the secondary side resonant transition, the m_s'–j_ℓ trajectory is an arc from $(-M, J_{rr})$ to (M, J_{pk2}). The arc has the center at $(1, 0)$, with angle $\alpha_{rs} = t_{rs}/\omega_{0s}$. The m_s–j_ℓ trajectory circles clockwise. This is because with positive power flow, the secondary side is a passive rectifier.

Figure 4.9: DCX m_p–j_ℓ state plane trajectory at zero current switching (ZCS).



According to Fig. 4.8(b), it is obvious that the secondary side commutation is always ZVS. However, in Fig. 4.8(a), the primary side ZVS condition is not always valid. Figure 4.9 sketches the m_p–j_ℓ plane trajectory where primary side ZVS is lost. The primary side switches have to actively turn on before the switch voltage reaches zero. Although after turn on the switch current is zero, which is zero current switching (ZCS). During ZCS, the switch still exhibits switching loss, though comparing to hard switching, the switching parasitic ringing is smaller due to zero current.

Based on the geometry relationship in Fig. 4.8(a), it is not difficult to figure out the primary side ZVS condition:

$$\sqrt{J_{pk1}^2 + (M-1)^2} \geq M + 1, \tag{4.17}$$

or $J_{pk1} \geq 2\sqrt{M}$. If it is assumed that $M \approx 1$, then $I_{pk1} \approx I_{pk2} \approx N_{DCX} I_{out}/(1-\varphi)$. Therefore, the primary side ZVS requires that

$$I_{out} \geq \frac{2V_{in}}{N_{DCX}} \cdot \sqrt{\frac{C_p}{L_\ell}}. \tag{4.18}$$

It can be interpreted that to achieve a wide ZVS range, it prefers small C_p, which means less required resonance energy, and large L_ℓ, which means more available resonance energy. However, according to equation (4.5), large L_ℓ also limits the maximum output current. It is interesting to define the converter ZVS range as

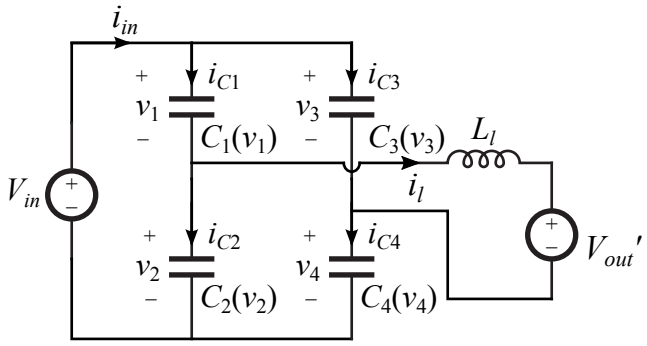
$$\frac{I_{out,max}}{I_{out,ZVS-min}} = \frac{T_s}{16\sqrt{L_\ell C_p}} = \frac{\pi}{8} \cdot \frac{f_{0p}}{f_s}, \tag{4.19}$$

where $f_s = 1/T_s$ is the converter switching frequency, and $f_{0p} = \omega_{0p}/2/\pi$, is the primary side resonance frequency. Therefore, to design a high frequency DCX, it is beneficial to use small tank inductance and device with small output capacitance.

It should be noticed that equation (4.18) is just an approximate solution with the assumption that $M \approx 1$. The complete solution requires solving the whole state plane equations, together with the diode reverse recovery behavior governed by equation (4.11). As demonstrated in [49], there is a large set of transcendental equations and it is computational intensive.

4.2.2 Nonlinear capacitance treatment

Figure 4.10: DCX detailed equivalent circuit at primary side commutation



In practice, it is well known that the MOSFET device output capacitance is highly nonlinear. The whole state plane analysis requires linear transformation of equations (4.15) & (4.16), which assumes they are linear systems. Therefore, even the exact state plane solution may not accurately reflect the real circuit behavior.

Figure 4.10 illustrates a more detailed DCX equivalent circuit during primary side commu-

tation, with nonlinear device output capacitance. C_1 – C_4 are the device output capacitance of switches M_1 – M_4, and they are the functions of switch voltages v_1 – v_4. Assume that at the beginning of the resonance, $v_1(0) = v_4(0) = 0$, and $v_2(0) = v_3(0) = V_{in}$ At the end of the resonance, $v_1(t_{rp}) = v_4(t_{rp}) = V_{in}$, and $v_2(t_{rp}) = v_3(t_{rp}) = V_{in}$ During the resonant interval, the total energy supplied by voltage source V_{in} is:

$$E_{in} = \int_0^{t_{rp}} V_{in} i_{in} \mathrm{d}t = \int_0^{t_{rp}} V_{in} \left(i_{C1} + i_{C3}\right) \mathrm{d}t = V_{in} \left(\int_0^{V_{in}} C_1 \left(v_1\right) \mathrm{d}v_1 + \int_{V_{in}}^0 C_3 \left(v_3\right) \mathrm{d}v_3 \right)$$
$$= V_{in} \left(Q_1|_0^{V_{in}} + Q_3|_{V_{in}}^0 \right) = V_{in} \left(\Delta Q_1 + \Delta Q_3\right) \tag{4.20}$$

Similarly, the energy supplied by voltage source V'_{out} is:

$$E_{out} = \int_0^{t_{rp}} -V'_{out} i_\ell \mathrm{d}t = MV_{in} \int_0^{t_{rp}} \left(i_{C2} - i_{C1}\right) \mathrm{d}t = MV_{in} \left(\int_{V_{in}}^0 C_2 \left(v_2\right) \mathrm{d}v_2 - \int_0^{V_{in}} C_1 \left(v_1\right) \mathrm{d}v_1 \right)$$
$$= MV_{in} \left(\Delta Q_2 - \Delta Q_1\right) \tag{4.21}$$

Therefore the total energy supplied to the system during resonance is:

$$E_{tot} = E_{in} + E_{out} = V_{in} \left(\left(1 - M\right) \Delta Q_1 + \Delta Q_3 + M \Delta Q_2 \right) \tag{4.22}$$

If M_1 – M_4 use the same type of device, $\Delta Q_1 = -\Delta Q_2 = -\Delta Q_3 = Q_{oss}\left(V_{in}\right) = Q_0$. Then

$$E_{tot} = -2MV_{in}Q_0. \tag{4.23}$$

Notice that the total energy stored in the capacitors is the same at the beginning and the end of the resonance. The total change of energy must be applied to the tank inductor. The initial inductor energy at the beginning of the resonance is:

$$E_L = \frac{1}{2} L_\ell i_\ell \left(0\right)^2 = \frac{1}{2} L_\ell I_{pk1}^2. \tag{4.24}$$

If

$$E_L + E_{tot} \geq 0, \tag{4.25}$$

the system has enough energy to achieve ZVS for the primary side switches. Otherwise, the primary side switches operate with ZCS. During ZCS, the energy that cannot be supplied by the tank

inductor is dissipated in the MOSFET on-resistance. The corresponding switching energy loss is

$$E_{loss} = -\left(E_L + E_{tot}\right). \tag{4.26}$$

In this way, the ZVS condition as well as the ZCS switching loss can be solved without solving the actual nonlinear differential equations. The only parameter required is the device output charge $Q_{oss}(v)$. Usually the device manufacturers provide the plot of device capacitance $C_{oss}(v)$, and $Q_{oss}(v)$ can be simply obtained as:

$$Q_{oss}(v) = \int_0^v C_{oss}\left(v'\right) \mathrm{d}v'. \tag{4.27}$$

4.3 DCX loss model

With the modeled DCX behavior in previous sections, it is possible to develop an accurate DCX loss model. In section 2.1.2, the general switched mode power converter loss model is discussed, with emphasis on conventional boost converter. Most of the loss mechanisms mentioned in section 2.1.2 applies to DCX converter as well. This section discusses about the specific loss modeling techniques that applies to the DCX.

4.3.1 Semiconductor loss

With the model developed in section 4.1, the DCX operation current waveforms can be obtained. Equation (2.6) can be applied to calculate the device conduction loss. In specific, for a DCX realized with MOSFET device, the MOSFET can be modeled as constant on-resistance R_{on}. Therefore, the primary side MOSFET conduction loss is calculated as

$$P_{Qcond} = \frac{2}{T_s} \int_0^{T_s/2} 2i_Q(t)^2 R_{on} \mathrm{d}t. \tag{4.28}$$

Similarly, the diode can be modeled as a constant voltage source V_D in series with a resistor R_D, that is,

$$v_D = V_D + i_D R_D. \tag{4.29}$$

The secondary side diode conduction loss is

$$P_{Dcond} = \frac{2}{T_s}\int_0^{T_s/2} 2\left(i_D\left(t\right)^2 R_D + i_D\left(t\right) V_D\right) \mathrm{d}t. \tag{4.30}$$

A more accurate method is to model the diode current using the complete diode model. Ideally the diode current follows the equation

$$i_D = I_s\left(e^{\frac{v_D}{nV_T}} - 1\right) \tag{4.31}$$

where I_s is the saturation current, $V_T = kT/q$ is the thermal voltage, and n is the diode ideality factory. For power diode, at high current level, the diode resistance also appear to affect the diode current significantly. The complete model should also include the diode resistance R_D, and the complete model should be

$$i_D = \frac{nV_T}{R_D} W_0\left(\frac{I_s R_D}{nV_T} e^{\frac{v_D + I_s R_D}{nV_T}}\right) - I_s \tag{4.32}$$

where W_0 is the main branch of the Lambert-W function [24].

Figure 4.11: Comparison of different diode models for the Infinoeon IPW65R041CFD 650 V 41 mΩ CoolMOS body diode at 25 °C temperature

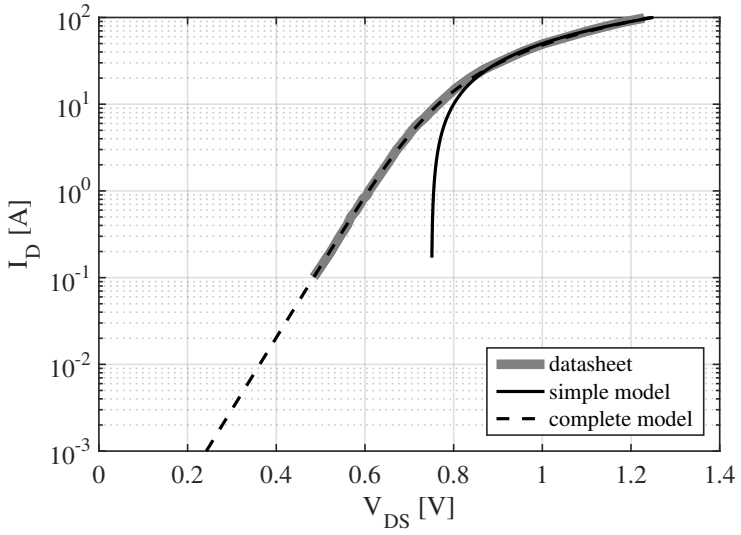


Figure 4.11 plots the nominal body diode characteristics of Infineon IPW65R041CFD 650 V 41 mΩ CoolMOS at 25 °C temperature. The data extracted from data sheet is compared with the simplified as well as complete models, with the model parameters documented in Table 4.11. The

Table 4.1: Infineon IPW65R041CFD 650 V 41 mΩ CoolMOS body diode model parameters at 25 °C

Parameter	Simple model	Complete model
V_D [V]	0.75	–
R_D [mΩ]	5	4
I_S [µA]	–	10
n	–	2.1

complete model matches perfectly with data sheet, while the simplified model over estimates the voltage drop at medium to low current level. Once the $v_D\left(i_D\right)$ data is known, the power loss can be calculated as

$$P_{Dcond} = \frac{2}{T_s}\int_0^{T_s/2} 2i_D\left(t\right)v_D\left(i_D\left(t\right)\right)\mathrm{d}t. \tag{4.33}$$

The MOSFET on-resistance is a function of temperature. Especially for silicon device, the on-resistance may increase significantly at higher temperature. To reduce the modeling error, after calculating the device conduction and switching loss, it is preferred to estimate the device junction temperature, and iterate the conduction loss calculation with temperature coefficient correction factor [56].

Figure 4.12: Simple device thermal circuit model

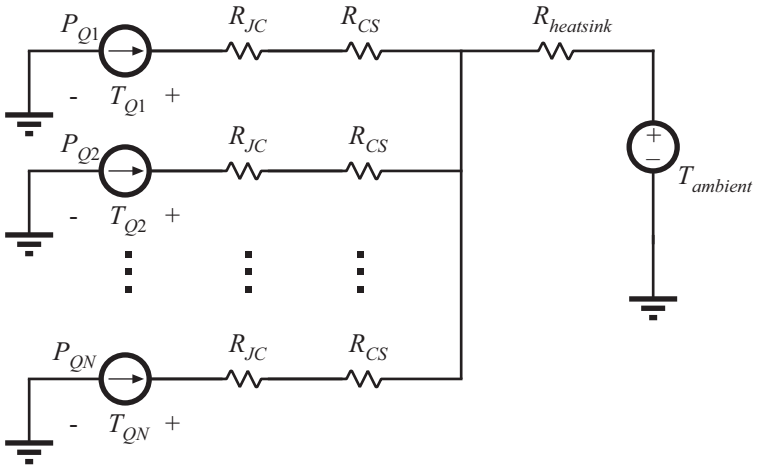


Figure 4.12 shows a simple device thermal circuit model. R_{JC} and R_{CS} are the junction-

to-case and case-to-heat-sink thermal resistance, and $R_{heatsink}$ is the heat sink to ambient thermal resistance. P_{Qn} is the power dissipation of the nth device, and T_{Qn} is its junction temperature. More accurate thermal model also considers thermal dynamic behavior. It requires more characterization process and more accurate measurement methods, which are beyond the scope of this work.

Although the model used in section 4.1 is not accurate at light load, it is still usable for the purpose of loss modeling. This is because the model developed in section 4.1 mainly affects the conduction loss model. At light load, the conduction loss is relatively small, and the device switching loss is the dominant loss mechanism.

Unlike the conventional boost converter where the device hard-switches, the switches in DCX exhibits soft-switching behavior. Therefore, the estimated switching loss equation (2.7) does not apply for DCX. In DCX, with ZVS, the primary side MOSFETs exhibit very small switching loss, and it is typically ineligible. At light load, the primary side MOSFETs may enter ZCS, and switching loss can be calculated with equation (4.26).

The secondary side always achieves ZVS. However, due to the diode reverse recovery, certain switching loss still exists. The diode switching loss can be modeled with the empirical model

$$P_{Dsw} = 4\alpha f_s \tau V_{out} I_{out}, \tag{4.34}$$

where τ is the diode minority carrier lifetime, and can be obtained from equation (4.14). α is an empirical curve-fitting parameter, and it is typically between 0.1 and 0.3.

4.3.2 Magnetic loss

Regarding the magnetic core loss, the iGSE method in equation (2.21) & (2.22) applies in the transformer and tank inductor of DCX as well. The DCX transformer magnetic flux $B_x(t)$ is a triangular waveform with peak

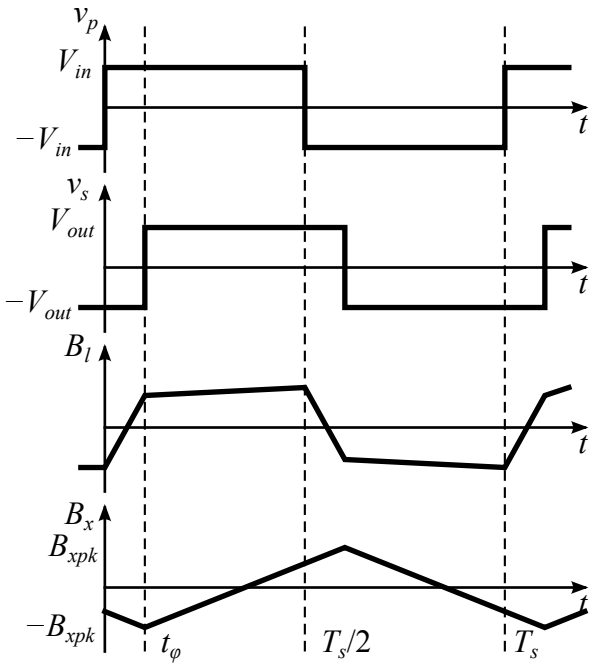
$$B_{xpk} = \frac{MV_{in}}{4 f_s N_p A_{cx}}, \tag{4.35}$$

where N_p is the transformer primary side winding number of turns, and A_{cx} is the transformer core cross section area. The DCX tank inductor magnetic flux $B_\ell(t)$ is

$$B_\ell(t) = \frac{L_\ell i_\ell(t)}{N_\ell A_{c\ell}}, \tag{4.36}$$

where N_ℓ is the inductor winding number of turns, and $A_{c\ell}$ is the inductor core cross section area. It has large $\mathrm{d}B/\mathrm{d}t$ over a short period, and small $\mathrm{d}B/\mathrm{d}t$ over a long period. Both the inductor and transformer flux density is sketched in Fig. 4.13.

Figure 4.13: DCX inductor and transformer flux density sketch



The copper loss model discussed in section 2.1.2 also can apply to the DCX transformer and tank inductor. To reduce the ac copper loss, the transformer windings can be interleaved to cancel MMF. Foil or Litz wire can also be used to reduce φ. If Litz wire is used, the proximity effect between the strands in each bundle has to be considered as well. To model this effect, the Litz wire with n_s strands can be considered to be packed in a square, and therefore equivalent to $\sqrt{n_s}$ layers. Therefore, the M in equation (2.12) has to be replaced with equivalent number of layers M_e

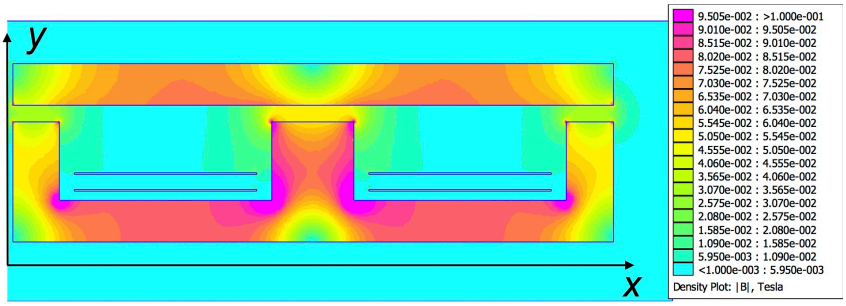
$$M_e = M\sqrt{n_s}. \tag{4.37}$$

Reference [91] also suggests that in Litz wire case, it is more accurate to calculate the factor φ in equation (2.12) as

$$\varphi = \sqrt{\eta}\frac{\sqrt[4]{3\pi}}{2}\frac{d_s}{\delta}, \tag{4.38}$$

where d_s is the diameter of the strand.

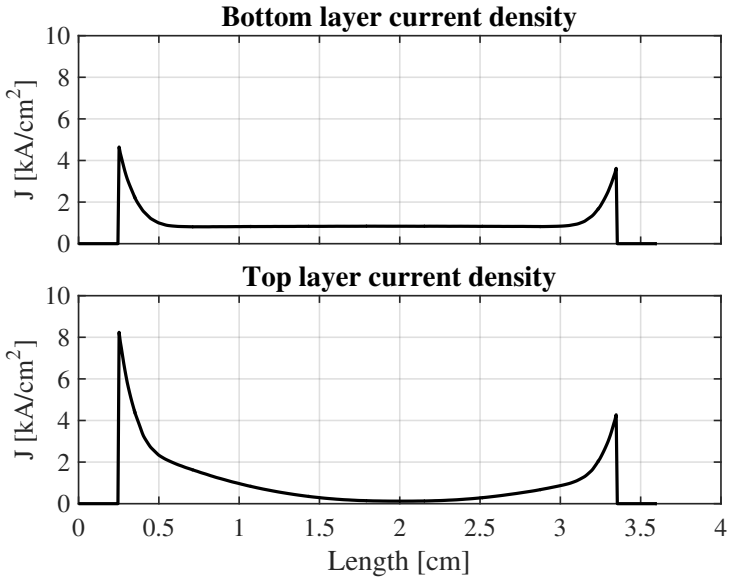
Figure 4.14: DCX planar tank inductor magnetic flux density plot in 2D finite element analysis (FEA), with 33 kHz 100 A peak sinusoidal current excitation. Two EPCOS EILP102 cores are used, with 2.88 mm air gap. 2-layer 9-ounce printed circuit board is designed as the winding.



In the tank inductor loss model, to determine the fringing loss factor F_{fr} due to the air gap, 2-D finite element analysis (FEA) can be performed. As an example, a 4 µH planar tank inductor is designed, with two EPCOS EILP102 cores [32]. Two-layer 9 ounce printed circuit board (PCB) is used as the winding. To handle peak current of around 200 A, 2.88 mm air gap is designed. The cross-section 2D FEA is done with Finite Element Method Magnetics (FEMM [71]) software, and the magnetic flux density is plotted in Fig. 4.14. Because of 2.88 mm air gap, significant fringing flux is observed outside of air gap. The fringing flux diffuses all the way to the top winding conductor, despite the fact that the conductor is more than 8 mm away from the air gap.

Figure 4.15 plots the winding conductor current density of the inductor simulation in Fig. 4.14. The bottom and top layer conductor current density is plotted respectively, along x-direction, and at the center of each conductor in y-direction. The directions are labeled in Fig. 4.14. Because of fringing flux, more current crowds around the edge of the top layer conductor than the bottom layer conductor, and little current is carried at the center of the top conductor. It implies the top conductor exhibits higher ac resistance than the bottom conductor. The Dowell's equation

Figure 4.15: The winding current density plot of the inductor simulation in Fig. 4.14. The current density is plotted along x-direction, at the center of each conductor in y-direction. The directions are labeled in Fig. 4.14.



predicts that $F_R = R_{ac}/R_{dc} = 1.15$, while the FEA shows that $R_{ac}/R_{dc} = 2.15$. Therefore, one can determine that in this case the fringing factor is $K_{fr} = 0.87$.

4.3.3 Loss model and measurement comparison

To validate the DCX loss model, a 20 kW 1 : 2 DCX prototype is designed, constructed and tested. The design parameters are documented in Table 4.2.

The input voltage range is from 100 V to 200 V, while the output voltage should not exceed 420 V. Infineon 650 V 43 A superjunction [37] MOSFET (CoolMOS [69]) with fast body diode technology (CFD2 [43, 84]) is used. To accommodate worst-case 200 A input current, on primary side each switch is composed of 5 MOSFET dies connected in parallel. In the case of bi-directional power flow, each secondary switch is composed of two MOSFET dies connected in parallel. With positive power flow, on the secondary side only the MOSFET body diodes are used with passive rectification. The superjunction MOSFET exhibits highly nonlinear output capacitance [15, 28], which may lead to large $\mathrm{d}v/\mathrm{d}t$ during ZVS. To improve the converter reliability, an extra 2.5 nF

Table 4.2: 20 kW 1 : 2 DCX prototype design parameters

Input voltage	$100\,\text{V} \leq V_{in} \leq 200\,\text{V}$
Output voltage	$V_{out} \leq 420\,\text{V}$
Output power	$P_{out} \leq 20\,\text{kW}$
Switching frequency	$f_s = 33\,\text{kHz}$
Switching device	Infineon IPW65R041CFD 650 V 43 A super-junction MOSFET, 5 in parallel on primary side. 2 in parallel on secondary side (only body diode is used under positive power flow). Each device has extra 2.5 nF external output capacitance.
Transformer	two EILP102 cores, N97 ferrite, 6:12 turns, 12-layer 9-Oz winding, $L_m \approx 450\,\mu\text{H}$, $N_{DCX} = 2$.
Tank inductor	two EILP102 cores, N97 ferrite, 2 turns, 2-layer 9-Oz winding, $L_\ell = 4\,\mu\text{H}$.

capacitance is externally added to the output of each device.

A 20 kVA planar transformer is designed with two EPCOS EILP102 cores [32] in parallel. The core is casted with N97 ferrite [31]. 12-layer 9 ounce PCB winding is designed, with 6:12 turns interleaved. The tank inductor is designed with same core shape and material, with 2-layer 9 ounce 2-turn winding. According to the loss model, 33 kHz switching frequency appears to be the optimum switching frequency with the best converter efficiency at medium load.

The designed DCX converter efficiency is predicted with the loss modeled discussed in this section. The DCX converter prototype efficiency is also measured in experiment. At 33 kHz switching frequency, the driver, control and sensing circuitry power consumption combined is around 10 W, and they are not included in the efficiency calculations. Calibrated current shunts are used to measure the input and output current, and $\pm 0.2\%$ accuracy is guaranteed in the efficiency measurement. Figure 4.16 plots the measured and predicted efficiencies at different output power levels. Figure 4.16(a) operates at fixed 100 V input, and Fig. 4.16(b) operates at fixed 200 V input. The measurement agrees with the theoretical prediction very well over a wide operation range. The DCX converter exhibits good efficiency at medium load, and the efficiency drops steeply at light load.

Figure 4.16: DCX loss model and measurement comparison: (a) at fixed 100 V input; (b) at fixed 200 V input.

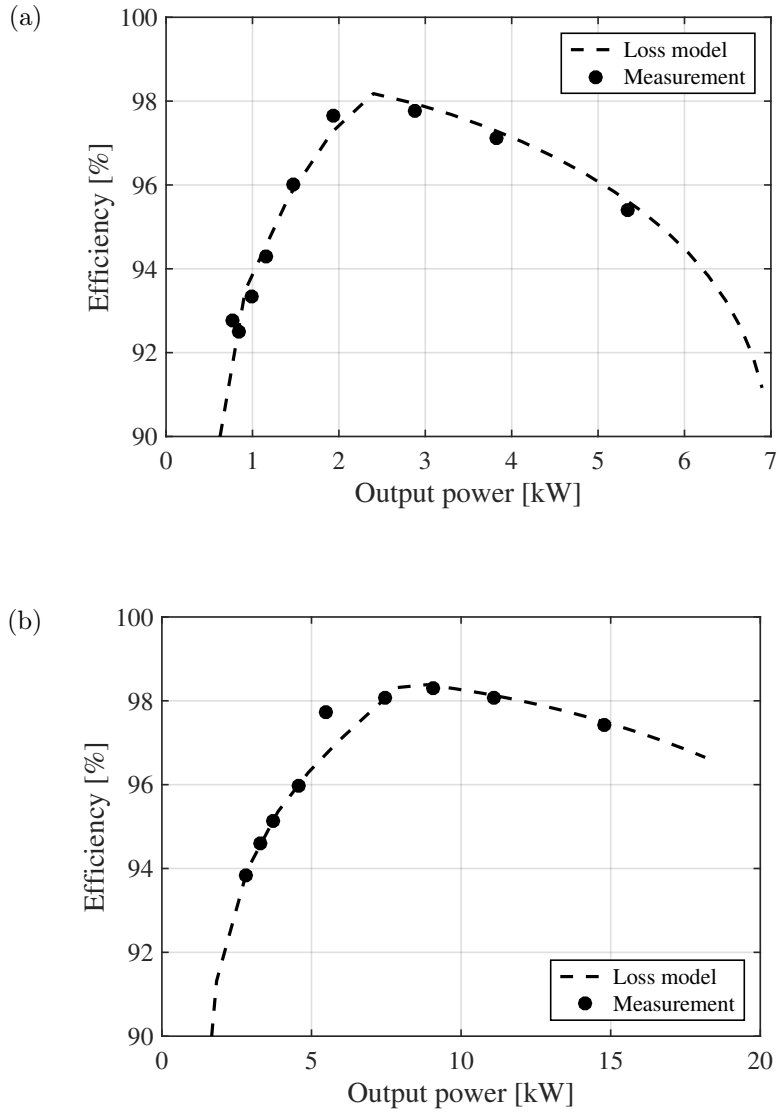
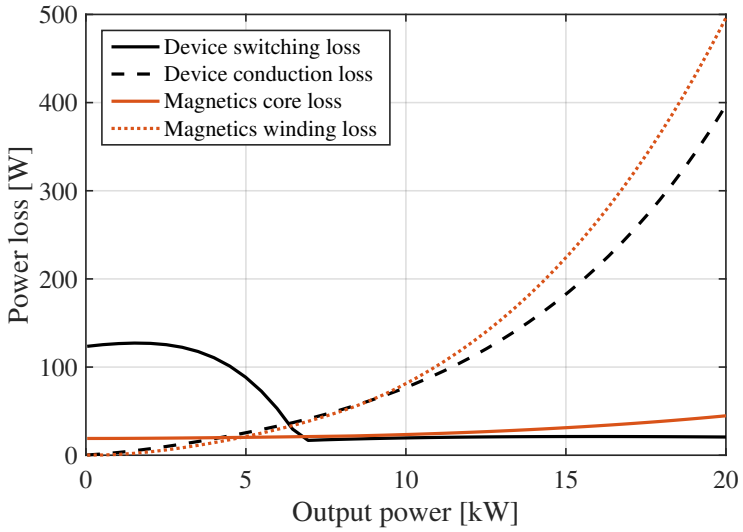


Figure 4.17: Modeled DCX prototype loss breakdown at fixed 200 V input.



To understand the dominant loss mechanism of DCX at different operation conditions, the modeled DCX loss breakdown is plotted at fixed 200 V input in Fig. 4.17. At heavy load, the device conduction loss and magnetics winding copper loss increases significantly as the power increases, which leads to the efficiency drop at heavy load. On the other hand, at light load, since the primary side switches lose ZVS, the device switching loss increases significantly, and it contributes to the sharp efficiency decline at light load.

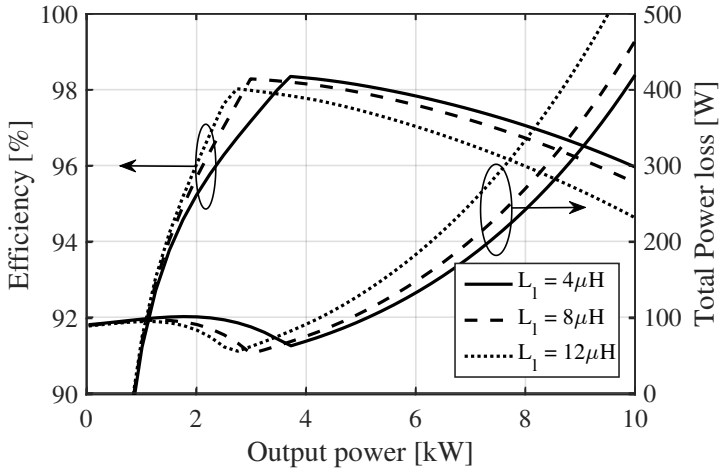
4.4 DCX light load efficiency improvement

As indicated in the previous section, at light load, the DCX primary side may lose ZVS. The DCX efficiency may drop significantly at light load, due to increased switching loss, such as the example shown in Fig. 4.16. However, in vehicle application, most of the time the powertrain system operates at light load. In this section, several conventional approaches to improve DCX light load efficiency are studied, and their limitations are discussed as well. After that a novel resonant transition operation mode is introduced, which theoretically can extend the ZVS range all the way to no load condition. It significantly improves the DCX light load efficiency, and it has other benefits such as improved open loop voltage regulation at light load.

4.4.1 Conventional approaches

As analyzed in Section 4.2, during primary side resonant transition, the tank inductor L_ℓ resonates with the primary side device output capacitance. The ZVS condition given in equation (4.25) suggests that it requires sufficient tank inductor energy to complete the ZVS resonant transition. As given in equation (4.24), the tank inductor energy is $E_L = 1/2 \times L_\ell I_{pk1}^2$. At light load, as the current decreases, the tank inductor energy is reduced, and the part of device output capacitor energy that cannot be recovered by tank inductor has to be dissipated in the device.

Figure 4.18: Modeled DCX efficiency and loss with varying tank inductance, at fixed 150 V input.



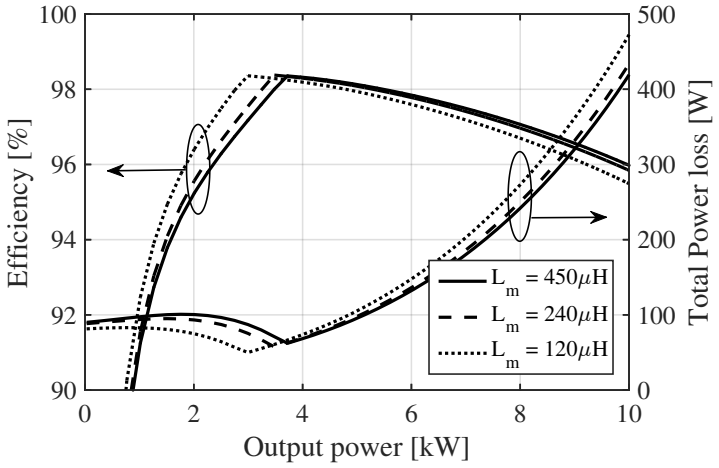
A straightforward approach to improve the light load efficiency is to simply increase the tank inductance. Since $E_L = 1/2 \times L_\ell I_{pk1}^2$, increasing tank inductance L_ℓ increases the stored energy E_L as well, and thus extending the ZVS range. To increase the tank inductance, the inductor number of turns has to be increased. With fixed inductor core design, and same current rating,

$$\frac{L_\ell}{N_\ell} = \frac{B_{max} A_{c\ell}}{I_{max}}. \tag{4.39}$$

In another word, the inductor winding number of turns is proportional to inductance. As discussed in Section 4.3.2, increased winding number of turns increases the inductor copper loss. The impact of different tank inductances on efficiency is modeled and shown in Fig. 4.18. Because the inductor energy is proportional to inductor current square, increasing tank inductance shows very limited loss

reduction at light load. On the other hand, the loss at medium to heavy load increases significantly, due to increased inductor winding turns and copper losses.

Figure 4.19: Modeled DCX efficiency and loss with varying magnetizing inductance, at fixed 150 V input.

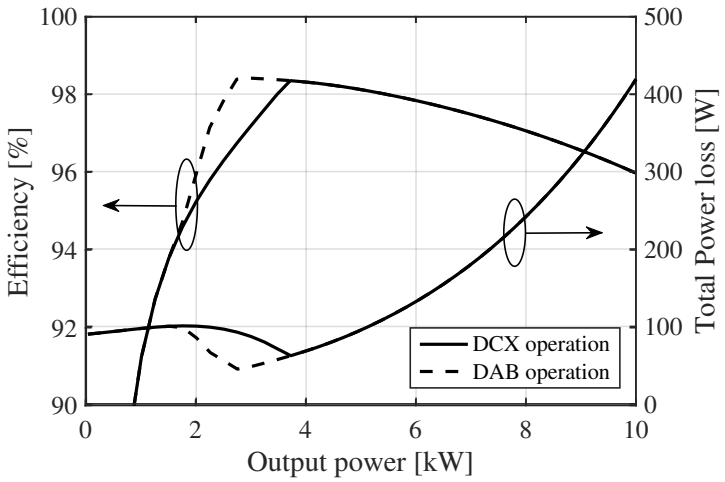


Another possibility is to gap the transformer core to reduce the magnetizing inductance. The magnetizing current is independent of the converter output power level, and it ensures that a minimum tank inductor energy is available. Fig. 4.19 shows the loss model based results. With the magnetizing inductance reduced to one half, no significant efficiency improvements can be observed. With the magnetizing inductance reduced to one quarter of the original value, switching loss at light load is slightly reduced, but at the expense of slightly increased conduction losses at heavy loads.

A third previously considered method is to operate the converter as a DAB at light load, which requires MOSFETs instead of diodes on the secondary side. The phase shift between the primary-side and the secondary-side bridge is controlled so that the tank inductor current at the moment of commutation can be increased to extend the primary side ZVS range. However, this primary side ZVS range extension comes ultimately at the expense of a secondary-side ZVS condition. As shown in Fig. 4.20, to ensure secondary-side ZVS, the DAB operation cannot result in the primary-side ZVS for loads smaller than about 2.8 kW (14% of maximum power).

A slight variation of the DAB operation is to combine the phase shift control with PWM

Figure 4.20: Modeled DCX efficiency and loss with DAB operation at light load, with fixed 150 V input.



control. As demonstrated in [9, 61], the PWM control reduces the rms current in the magnetics when $M \neq 1$, in a voltage-regulated DAB. It helps to further extend the ZVS range when $M \neq 1$, as well. However, as far as the unregulated DAB converter is concerned, where $M \approx 1$, the usually PWM control does not bring extra benefits. References [93, 98] introduce a different modulation scheme, where negative phase shift is applied to a PWM modulated DAB with positive power flow. With this modulation scheme, the tank inductor current may have several zero crossings, which greatly extends the ZVS operation range in light load. However, it requires fairly complicated control scheme with zero current detection. What is more, the ZVS range is extended only if $M < 1$ and the primary side H-bridge is PWM modulated, or $M > 1$ and the secondary H-bridge is PWM modulated. When $M \approx 1$, it is unlikely to guarantee ZVS operation on both primary and secondary sides. According to [48], even with the very sophisticated dual PWM modulation with phase-shift control, at light load with $M \approx 1$, at least one half bridge has to hard switch or ZCS.

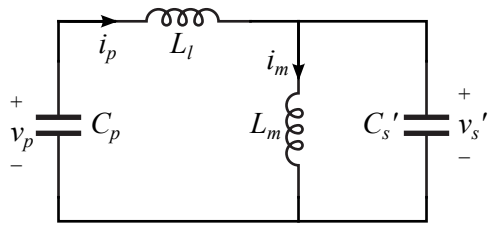
4.4.2 Extended *LLCC* resonant transition

It is clear that DCX primary side loses ZVS at light load because the energy stored in the tank inductor is not sufficient to complete the resonant commutation. Actually the transformer

magnetizing inductance L_m could potentially become another reactive energy source to assist ZVS, similar to the scenario in LLC resonant converter [70]. The reason that the energy stored in L_m cannot be exploited in DCX is because the transformer secondary side voltage is clamped by the diode during primary side commutation, as shown in Fig. 4.7(a). The only exception is during DCM that the secondary diodes are off due to zero current. On the other hand, at light load condition, if the primary side dead time is longer than the optimum value to achieve ZCS, after the tank inductor current i_p reverses its polarity, the secondary diodes will eventually turn off. In both cases, if the primary side switches do not turn on during this interval, the magnetizing inductance L_m will appear in the resonant tank, and its energy can be utilized.

4.4.2.1 State plane analysis

Figure 4.21: Equivalent resonant tank circuit during the proposed resonant transition



During the interval where all the switches in DCX are off, the equivalent resonant tank circuit is shown in Fig. 4.4.2.1, which is a fourth-order $LLCC$ resonant circuit. It has four state variables: v_s', v_p, i_p, and i_m. This system can be described the state equation:

$$\begin{bmatrix} \dot{v_s'} \\ \dot{v_p} \\ \dot{i_p} \\ \dot{i_m} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{1}{C_s'} & -\frac{1}{C_s'} \\ 0 & 0 & -\frac{1}{C_p} & 0 \\ -\frac{1}{L_l} & \frac{1}{L_l} & 0 & 0 \\ \frac{1}{L_m} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_s' \\ v_p \\ i_p \\ i_m \end{bmatrix} \tag{4.40}$$

With certain matrix transformation [10], the four state variables can be transformed into two pairs of independent states. In normal design, usually $L_l \ll L_m$. With this assumption, the

decoupled state equations can be approximately simplified as

$$\begin{bmatrix} \dot{q_1} \\ \dot{\lambda_1} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{C_p}{(C_s'+C_p)L_m} \\ \frac{1}{C_p} & 0 \end{bmatrix} \begin{bmatrix} q_1 \\ \lambda_1 \end{bmatrix} \tag{4.41}$$

$$\begin{bmatrix} \dot{v_2} \\ \dot{i_2} \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{C_s'||C_p} \\ -\frac{1}{L_l} & 0 \end{bmatrix} \begin{bmatrix} v_2 \\ i_2 \end{bmatrix} \tag{4.42}$$

where $q_1 \approx v_s' C_s' + v_p C_p$, $\lambda_1 \approx i_p L_l + \left(\frac{C_s'}{C_p} + 1\right) i_m L_m$, $v_2 \approx v_s' - v_p$, and $i_2 \approx i_p - \frac{C_p}{C_s'+C_p} i_m$. The details of the derivation are documented in the Appendix A.1.

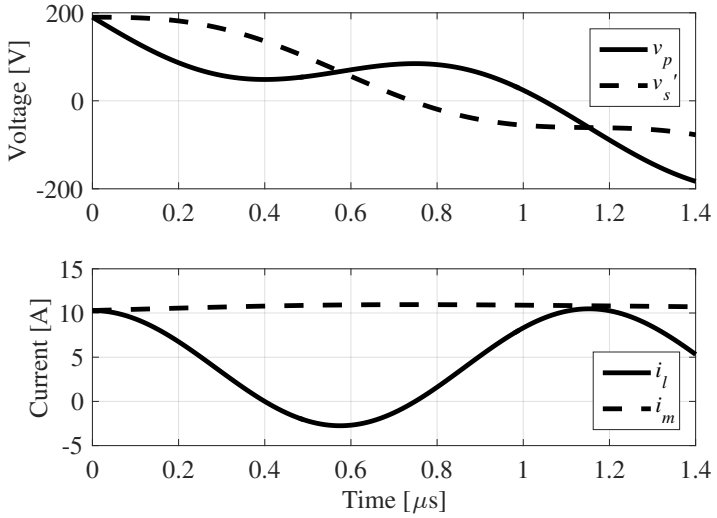
In equation (4.41), $\langle q_1, \lambda_1 \rangle$ can be interpreted as the system total charge resonates with (scaled) system total flux. In equation (4.42), $\langle v_2, i_2 \rangle$ can be interpreted as the tank inductor L_l resonates with C_s' and C_p in series, with some dc offset (i_m is approximated as a constant during this resonance, due to large L_m).

Fig. 4.22 shows the simulated tank resonant waveform. At the end of the resonance, v_p completes the commutation in full ZVS. After that, the primary side switch turns on, and the secondary side completes ZVS commutation as before.

Fig. 4.23 plots the simulated and analytically approximated state plane trajectory of the transient waveform in Fig. 4.22. The approximation is shown to be close enough to the simulation. It is worth noticing that on the state plane trajectory of $\langle q_1, \lambda_1 \rangle$ in Fig. 4.23(a), the center of the trajectory is at $(0, 0)$, where the start point is at $(1, \lambda_{n10})$. It implies that the trajectory can always reach the point $(-1, \lambda_{n10})$, which means the systems total charge can always be inverted, and the ZVS condition for both primary side and secondary side can always be satisfied, even at no-load condition.

The final note is that although the proposed resonance transition can always achieve ZVS, if L_m is too large, the resonant transition time may be too long to be desired. To solve this problem, the transformer core can be gapped to slightly reduce L_m. As modeled in Fig. 4.19, slight reduction of L_m may not affect the total efficiency much.

Figure 4.22: Simulated $LLCC$ resonance transient



4.4.2.2 Operations and modes of extended $LLCC$ resonant transition

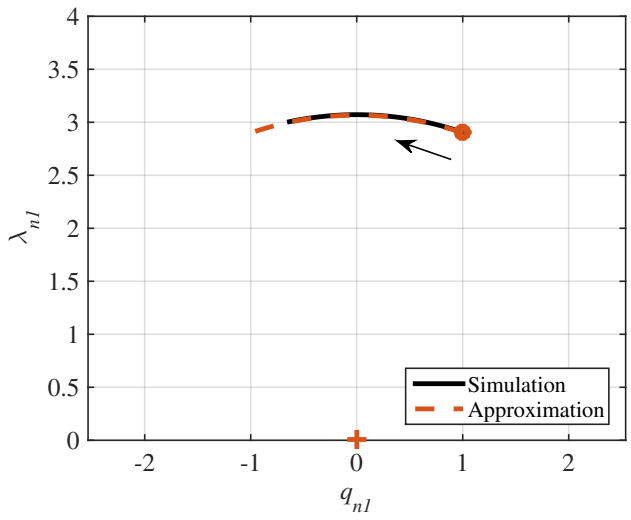
The state-plane analysis proofs that the extended $LLCC$ resonant transition can always achieve ZVS. Further analysis is required to evaluate the effect of extended resonant transition on the converter operation, and to determine the duration of dead time that achieves optimum efficiency.

Figure 4.24 – 4.26 show the SPICE simulation waveform of DCX at light load, with fixed load resistance, and different dead time durations. With long dead time duration, the $LLCC$ tank may resonate on $\langle v_2, i_2 \rangle$ plane for more than one cycle. The resonance operation of DCX can be categorized into different modes, where mode N indicates that the dead time resonance duration is between N and $N + 1$ periods. Fig. 4.24 shows the mode 0 operation, which is the conventional mode. The primary side is hard-switching, with almost all parasitic capacitor energy dissipated. Fig. 4.25 shows the mode 1 operation, where the resonance lasts more than one resonance cycle. The primary side is partial ZVS, with approximately half the capacitor energy restored. Fig. 4.26 shows the mode 2 operation, where the resonance lasts more than two resonance cycles. The primary side is full ZVS with almost zero switching loss.

On the other hand, notice that by changing the dead time duration, the DCX exhibits slightly

Figure 4.23: Simulated and analytically approximated state plane trajectory of the $LLCC$ resonance tank: (a) normalized state plane of $\langle q_1, \lambda_1 \rangle$, (b) normalized state plane of $\langle v_2, i_2 \rangle$.

(a)



(b)

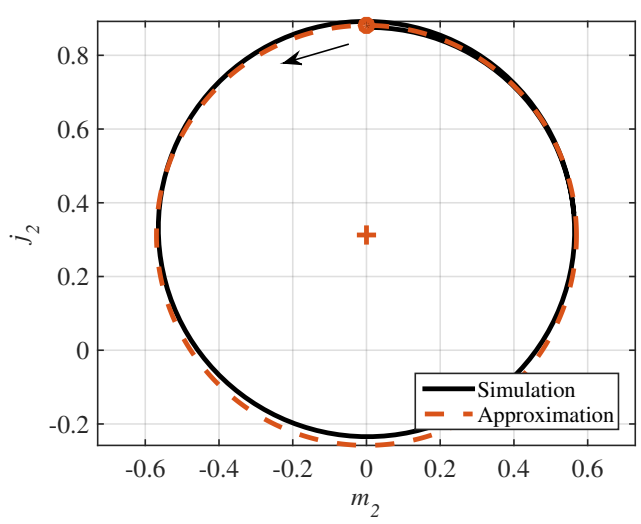


Figure 4.24: SPICE simulation of DCX in resonant mode 0, with 0.5 µs dead time. Load resistance is $R_L = 96\,\Omega$. With 150 V input voltage, the output is 317.3 V.

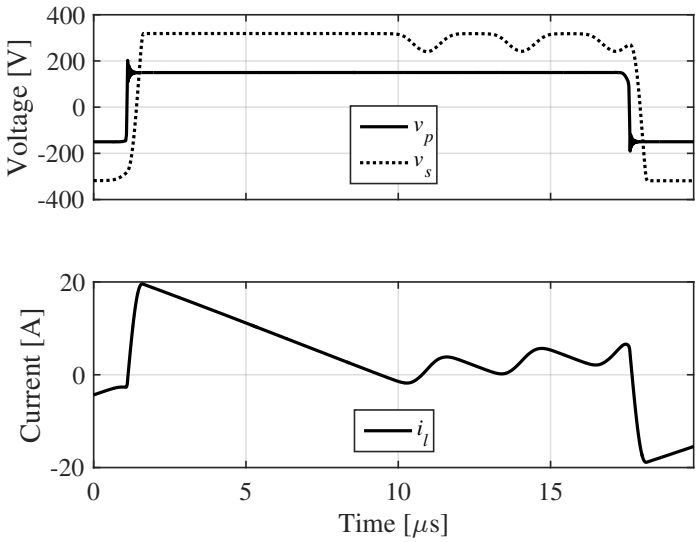


Figure 4.25: SPICE simulation of DCX in resonant mode 1 with 2 µs dead time. Load resistance is $R_L = 96\,\Omega$. With 150 V input voltage, the output is 302.5 V.

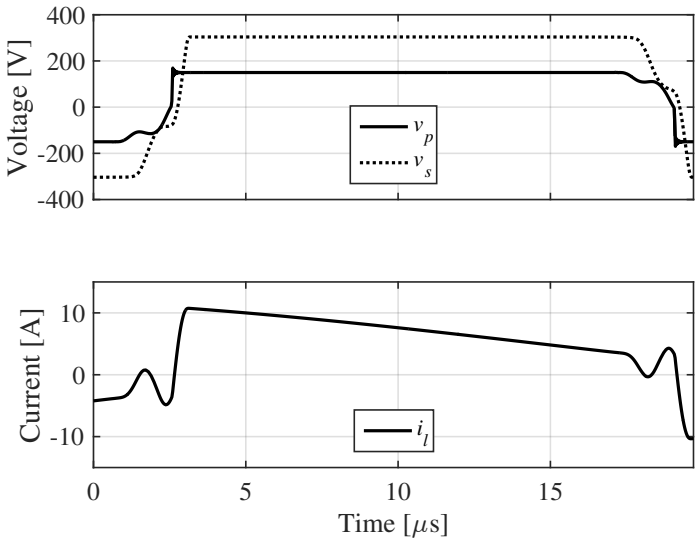
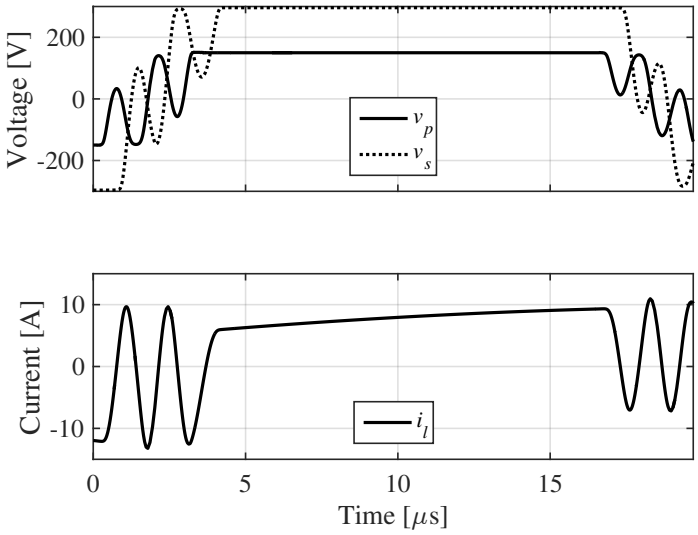


Figure 4.26: SPICE simulation of DCX in resonant mode 2 with 3.5 µs dead time. Load resistance is $R_L = 96\,\Omega$. With 150 V input voltage, the output is 294.8 V.



different voltage conversion ratios in different modes. In mode 0 operation of Fig. 4.24, $M = 1.06 > 1$. The waveform in Fig. 4.24 indicates that the DCX operates in DCM. In mode 1 operation as in Fig. 4.25, $M = 1.01$, and the DCX operates around the boundary between CCM and DCM. In mode 2 operation as in Fig. 4.26, $M = 0.98$, and the DCX operates in CCM.

During the dead time resonance duration, the energy only cycles back and forth between the tank elements, and no energy is delivered through the secondary diodes to the output. Therefore, the effective conduction period of the diodes is reduces, while the total charge delivered to the output in each cycle should still be balanced. The voltage-second on the tank inductor has to be adjusted to affect the shape of the tank current. The longer the dead time, the shorter the diode conduction period, thus the output voltage has to be lower to ramp up the tank inductor current more.

This phenomenon is favorable in extremely light load operation. Ideally, if no load is present at the DCX output (open circuit), the DCX operates in deep DCM with output voltage shoot up to infinity. In real circuit, because of various loss mechanism, the output voltage can boost to some finite but unreasonably high voltage level, which can exceed the device voltage ratings. In

practice, usually extra protection mechanisms are required, such as lowering input voltage at no-load condition, or add bleeder resistors to avoid no-load condition. With proper extended $LLCC$ resonant transitions, the output voltage variation can be much reduced, and no extra protection mechanism is required.

What is more, despite of reducing the switching loss, the resonant mode also has the potential to reduce other losses such as conduction loss and tank inductor core loss. For example, in Fig. 4.24, the inductor peak current is around 20 A, while with similar output power, in Fig. 4.25 & 4.26 the inductor peak currents are reduced to around 10 A. The inductor current slope in Fig. 4.25 & 4.26 is also much reduced comparing to that in Fig. 4.24, which implies a reduced inductor voltage-second, therefore reduced core loss. Of course, if the dead time further increases to introduce extra unnecessary resonance, the output voltage further drops, and it is expected that the conduction loss as well as inductor core loss will increase again. There exists an optimum dead time that yields the best efficiency at given load condition.

4.4.3 Experimental validation

In order to verify the DCX extended resonant transition at light load, the 20 kW converter prototype mentioned in Section 4.3.3 is operated at light load with different operation modes. The design parameters of the prototype are documented in Table 4.2.

4.4.3.1 Open loop operation

Figure 4.27 shows the prototype light load operation at mode 0, which is the conventional operation mode. The DCX operates in DCM. Fig. 4.27(b) indicates that the primary side switch (driven by v_{gsL}) actively switches v_p, resulting in hard-switching losses and low efficiency. In Fig. 4.28, the converter operates in the resonant transition mode 1 at the same condition. Partial ZVS is achieved, and around 30% device output capacitor energy is recovered. The measurement shows that the efficiency is improved from 94.6% to 96.6%. In Fig. 4.29, the converter operates in the resonant transition mode 2. With more partial ZVS, more than 80% of the device output

Figure 4.27: 20 kW DCX prototype light load measurement in mode 0 (conventional approach), with around 0.4 µs dead time. At $V_{in} = 150$ V and around 1.5 kW output power (8% of maximum power), measured efficiency is 94.6%, and $M = 1.04$. (a): waveform of one switching period; (b) zoom in at switching interval.

(a)

(b)

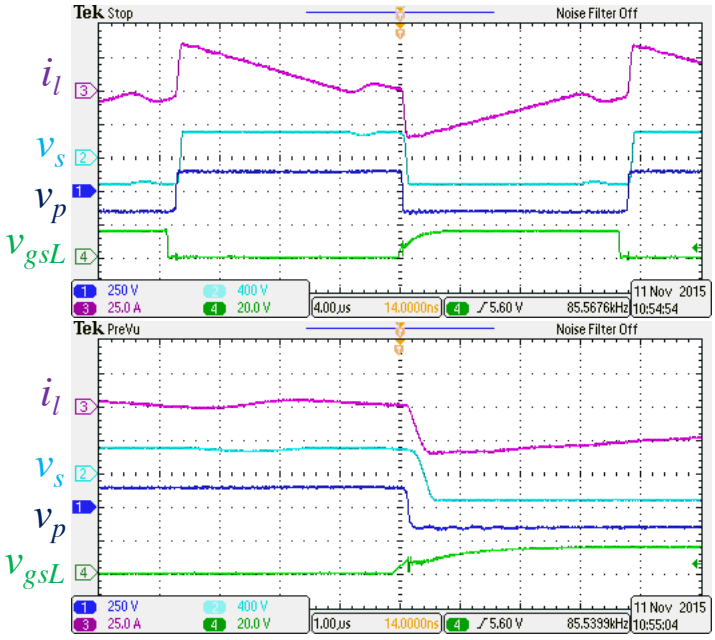


Figure 4.28: 20 kW prototype measurement in mode 1, with around 1.7 µs dead time. At $V_{in} = 150$ V and around 1.5 kW output power (8% of maximum power), measured efficiency is 96.6%, and $M = 1.02$. (a): waveform of one switching period; (b) zoom in at switching interval.

(a)

(b)

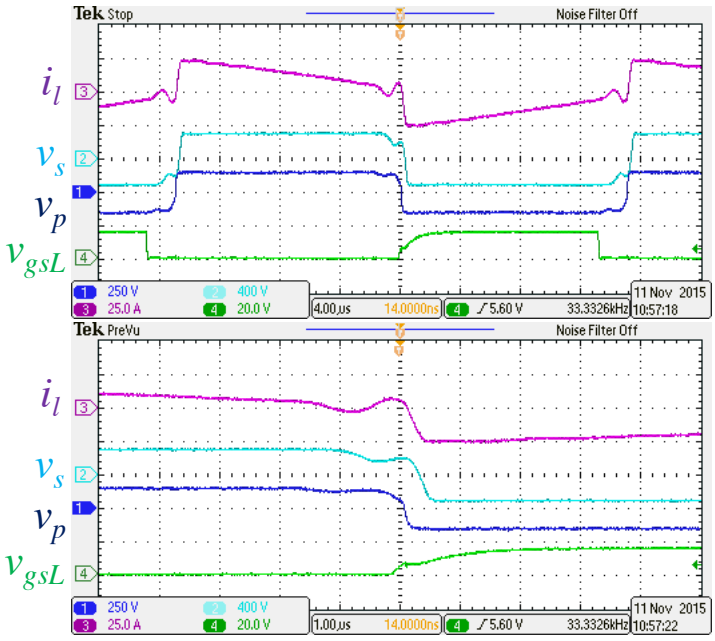


Figure 4.29: 20 kW prototype measurement in mode 2, with around 2.6 µs dead time. At $V_{in} = 150$ V and around 1.5 kW output power (8% of maximum power), measured efficiency is 97.4%, and $M = 1$. (a): waveform of one switching period; (b) zoom in at switching interval.

(a)

(b)

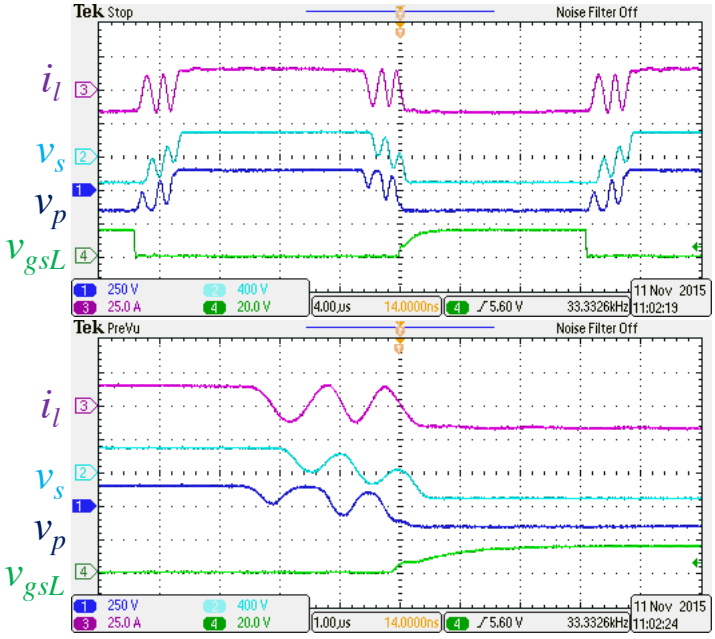
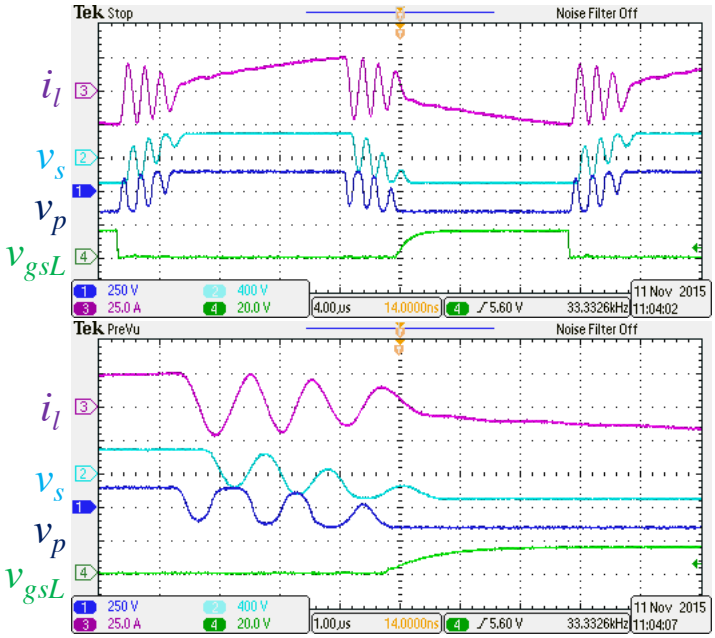


Figure 4.30: 20 kW prototype measurement in mode 3, with around 3.6 µs dead time. At $V_{in} = 150$ V and around 1.5 kW output power (8% of maximum power), measured efficiency is 96.6%, and $M = 0.97$. (a): waveform of one switching period; (b) zoom in at switching interval.

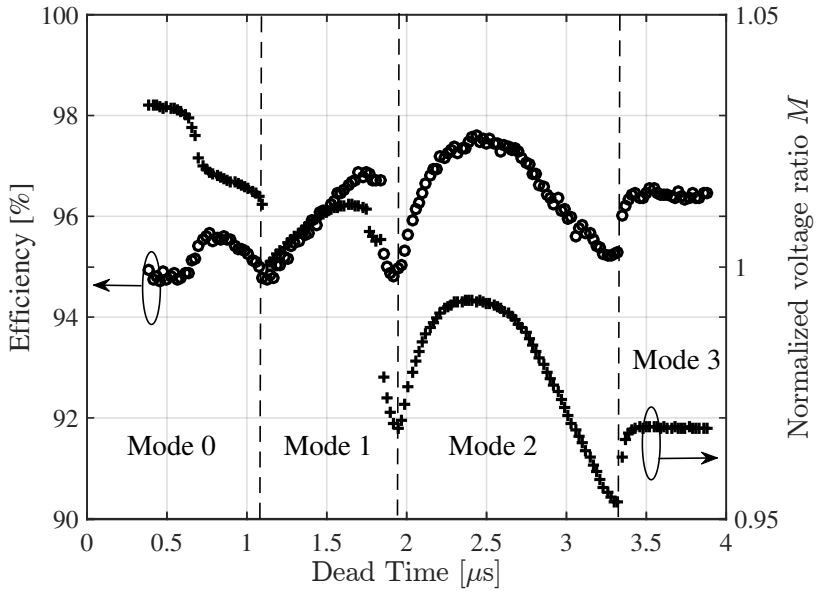
(a)

(b)



capacitor energy is recovered. At this mode $M = 1$, which also indicates that the conduction loss as well as tank inductor core loss are minimized. The resulting efficiency is 97.4%, which is higher than that in both mode 0 and mode 1. The converter achieves full ZVS in mode 3, as shown in Fig. 4.30. However, since at mode 3, $M < 1$, the conduction and tank inductor core losses increase again. The measured efficiency is 96.6%, lower than that in mode 2, though still higher than the conventional approach.

Figure 4.31: Measured DCX voltage conversion ratio and efficiency versus dead time, at around 1.5 kW output power, with 150 V input voltage.

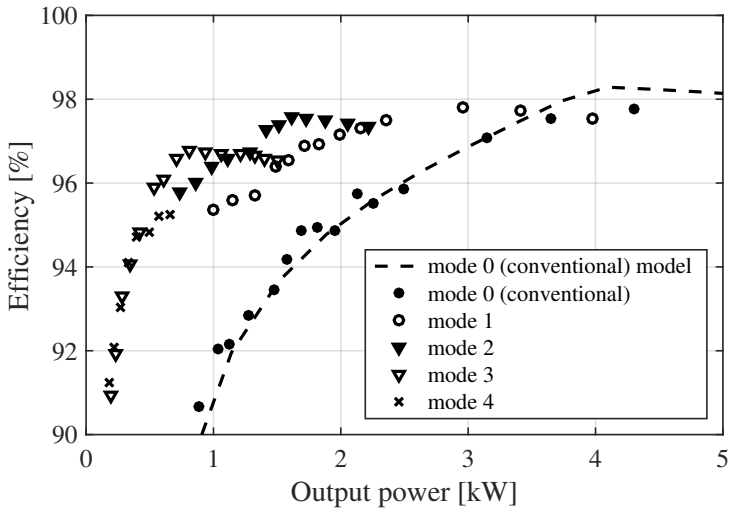


The extended resonant transition affects not only the switching loss, but the conduction loss and magnetic core loss as well. Therefore, the best efficiency point is not necessary the operation point that achieves full ZVS. To illustrate how the efficiency changes with resonant time, Fig. 4.31 plots the measured voltage conversion ratio and converter efficiency at different dead time. It is measured with fixed 150 V input voltage, and around 1.5 kW output power (7.5% rated power). At this specific load condition, the voltage conversion ratio stays constant in mode 3. It indicates that in mode 3 full ZVS is achieved, and the dead time no longer affects the converter operation.

Within each mode, different dead time lead to different efficiencies, and there's a best dead

time that yields the minimum switching loss and the best efficiency. On the other hand, the peak efficiency in each mode also varies. For example, although in mode 3 full ZVS is achieved with minimum switching loss, the peak efficiency is somehow lower than that in mode 2 due to increased conduction and core losses.

Figure 4.32: Measured DCX peak efficiency versus output power at different modes, with fixed 150 V nominal input voltage.

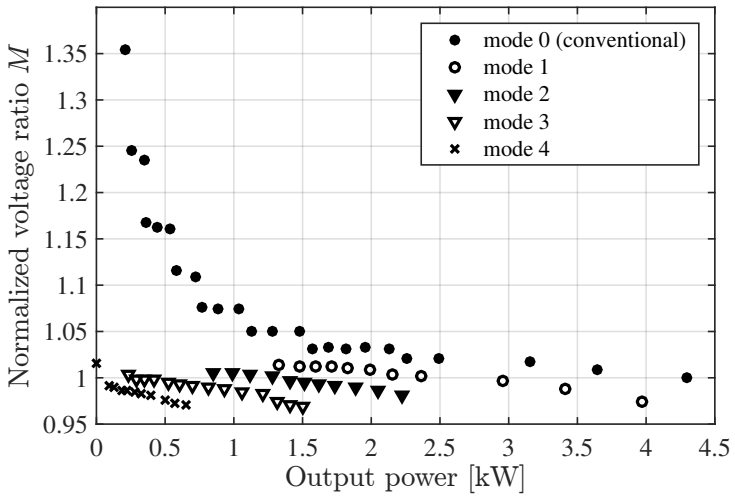


In order to understand which mode exhibits optimum efficiency with given load, the measured peak efficiency at each mode is plotted against output power as in Fig. 4.32, with fixed 150 V nominal input voltage. The predicted efficiency with conventional mode 0 loss model is also plotted for comparison. The loss model used in previous calculations shows good agreement with the measured efficiency at mode 0.

At medium load, the conventional mode 0 shows the best efficiency, since it can achieve ZVS with minimum conduction loss. As load decreases, mode 0 loses ZVS and switching loss increases. Then mode 1 shows better efficiency, until the switching loss in mode 1 significantly increases, where the next mode yields optimum efficiency.

Figure 4.4.3.1 shows the measured voltage conversion ratio at each efficiency points of Fig. 4.32. In the conventional operation of mode 0, the output voltage goes up significantly at light load. To

Figure 4.33: Measured normalized voltage conversion ratio versus output power at the optimum efficiency points in different modes, with fixed 150 V nominal input voltage.



limit the output voltage under 420 V, the conventional approach is unable to process output power less than 200 W. On the contrary, with the extended resonant transitions, the converter normalized voltage conversion ratio stays close to unity. In specific, mode 4 can operate at no-load condition with $M = 1.015$, and no extra protection mechanism is required.

Figure 4.34: No-load operation in mode 0 (conventional approach). With 90 V input, $M = 1.91$. 61.7 W loss is measured.

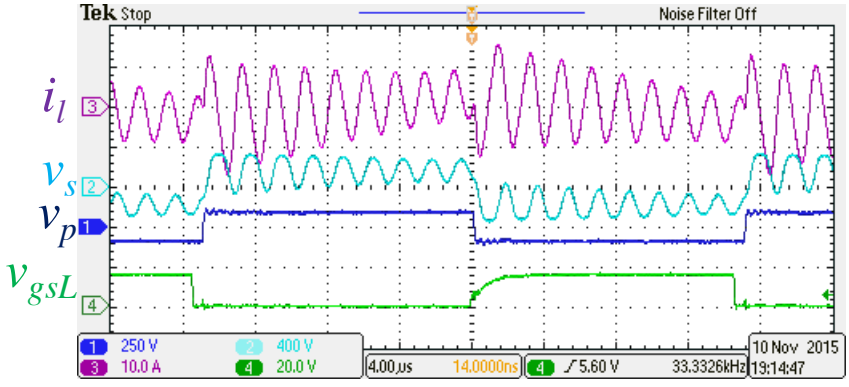
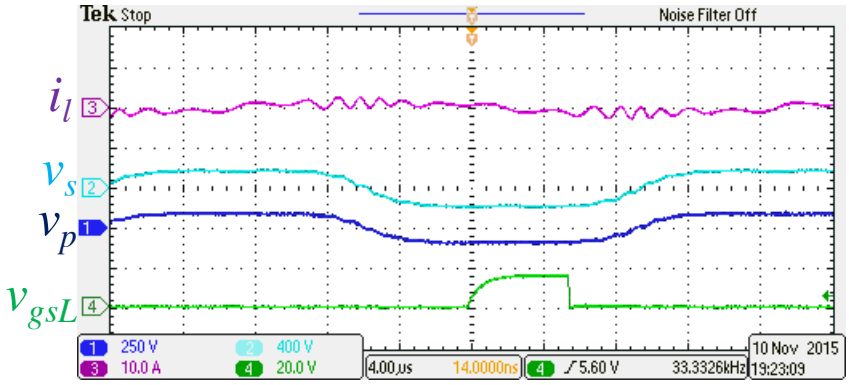


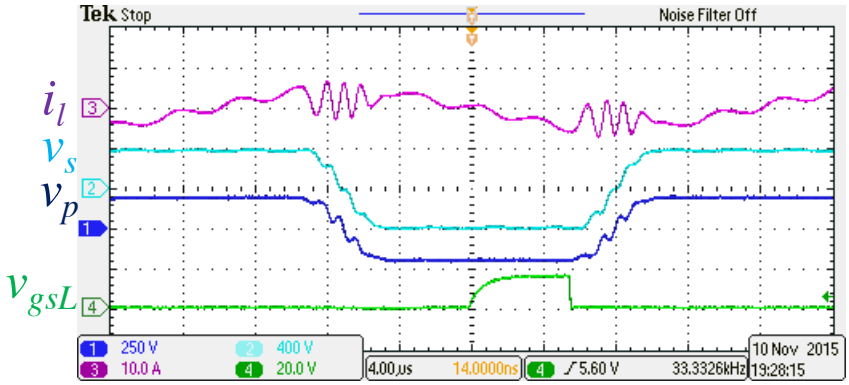
Fig. 4.4.3.1 & 4.4.3.1 shows the no-load operation waveforms in mode 0 (conventional approach) and mode 5. In mode 0, the tank inductor current amplitude is more than 12 A, with significant ringings on v_s. In mode 5, the tank inductor current amplitude is only around 2 A, and

Figure 4.35: No-load operation in mode 5. With 90 V input, $M = 1.02$. 6.2 W loss is measured.



the ringings on v_s are much reduced. The power loss in mode 5 is 10 times smaller than that in mode 0. Fig. 4.4.3.1 shows that with resonant transition operation, the designed DCX is capable to operate at maximum 200 V input voltage safely, without extra protection mechanisms.

Figure 4.36: No-load operation in resonant transition operation, with maximum 200 V input, $M = 1.02$. 27.3 W loss is measured.



4.4.3.2 Approximate optimum efficiency trajectory control

To utilize the extended resonant transition in real application, a controller has to be designed so that the converter can automatically adjust the dead time to achieve good efficiency. Ideally the most straight forward solution is to sense both the input current and voltage, and use a 2-D look up table (LUT) to achieve the optimum efficiency trajectory (that is, the envelop of the best efficiency

points) in Fig. 4.32. However, to implement an accurate current sensor with good resolution and low noise level may impose extra cost to the system, and a 2-D LUT may be too complicated for some applications. In this section, a simple current sensorless approximate optimum efficiency trajectory control is proposed.

The purpose of the controller is to improve the converter steady state light load efficiency, any sub-optimal dead time during the transients is acceptable. On the other hand, as shown in Fig. 4.31, slight deviation from the optimum dead time value does not significantly degenerate the efficiency, and therefore can be tolerated as well.

Figure 4.37: Dead time that yields peak efficiency in each mode, at 150 V nominal input voltage. The optimum efficiency trajectory points are highlighted in red dashed line boxes, where the blue dotted line indicates the approximate optimum dead time in each mode.

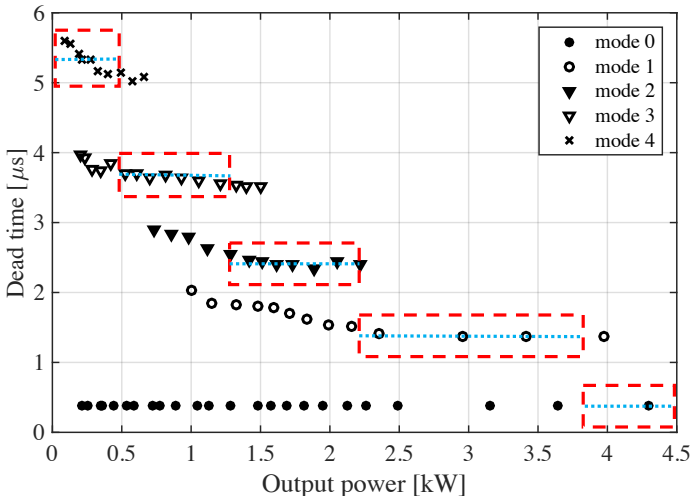
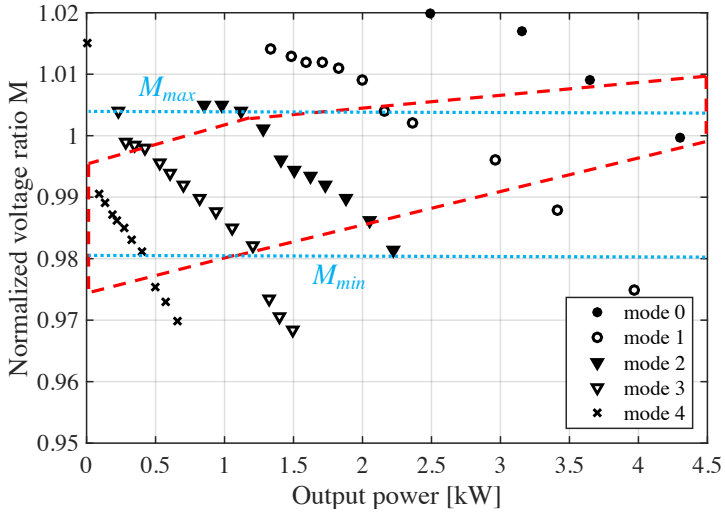


Figure 4.4.3.2 plots the dead time in each mode that produces the peak efficiency points in each mode in Fig. 4.32 (except that constant dead time is used in mode 0, to be compatible with conventional operation). The points that falls into the optimum efficiency trajectory are highlighted in red dashed line boxes. The optimum dead time in each mode stays almost flat inside the boxes, and therefore can be approximated as constants which are independent of the current. In each mode, just one fixed dead time value is sufficient. This eliminates the need of LUT.

Figure 4.4.3.2 shows the zoom in of Fig. 4.4.3.1. The optimum efficiency trajectory points

Figure 4.38: Zoom in of Fig. 4.4.3.1, with the optimum efficiency trajectory points in red dash line regions. Blue dot line indicates the approximate optimum efficiency trajectory boundary.



are highlighted in the red dashed line area. All these points are around the region where M is close to unity. Because in this area, not only the switching loss is significantly reduced, the conduction and tank inductor core losses are also minimized. This region can be approximated as regions within the boundaries M_{max} and M_{min}, as highlighted in Fig. 4.4.3.2. If the controller can select the appropriate mode, so that M lies in between M_{max} and M_{min}, the converter efficiency should be very close to the optimum efficiency trajectory. A simple approximate optimum efficiency trajectory control algorithm is proposed in Fig. 4.39. The controller simply increase or decrease the mode number if the voltage conversion ratio lies outside the predefined boundary, and no current sensor information is required. Notice that in Fig. 4.4.3.2, inside the given boundary, one output power may correspond to two neighbouring modes. This guarantees hysteresis behavior during mode transition, therefore the instability at mode boundary is eliminated.

Figure 4.40 shows the measured performance with proposed controller, at fixed 150 V nominal input voltage. Fig. 4.40(a) plots the close loop efficiency, compared with the open loop efficiency of different modes as in Fig. 4.32. The proposed control algorithm yields the efficiency that follows the optimum efficiency trajectory at most conditions. Though at some points the close loop effi-

Figure 4.39: Proposed simple approximate optimum efficiency trajectory control decision diagram.

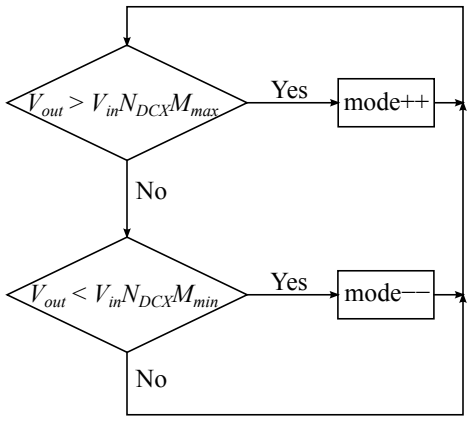
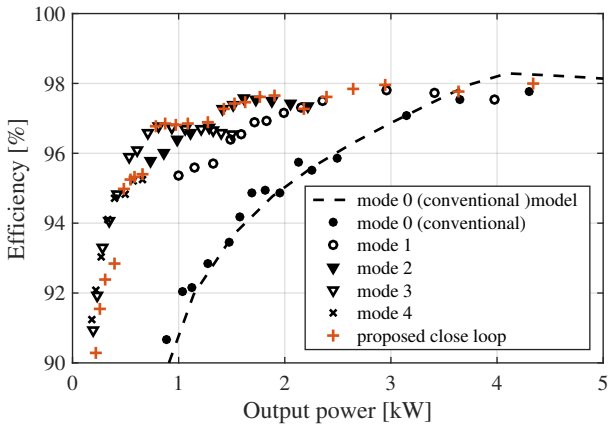
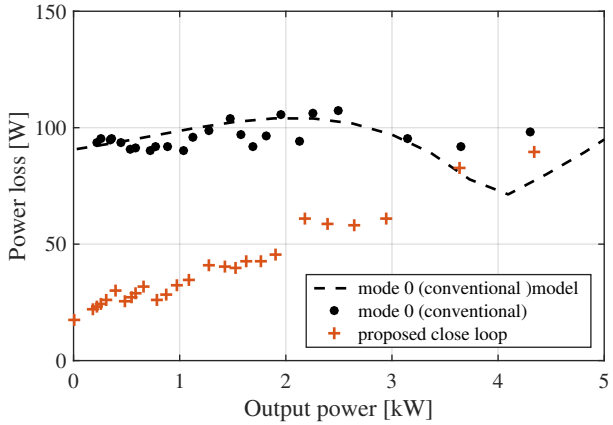


Figure 4.40: Measured DCX close loop operation at nominal 150 V input: (a) efficiency; (b) power loss.

(a)

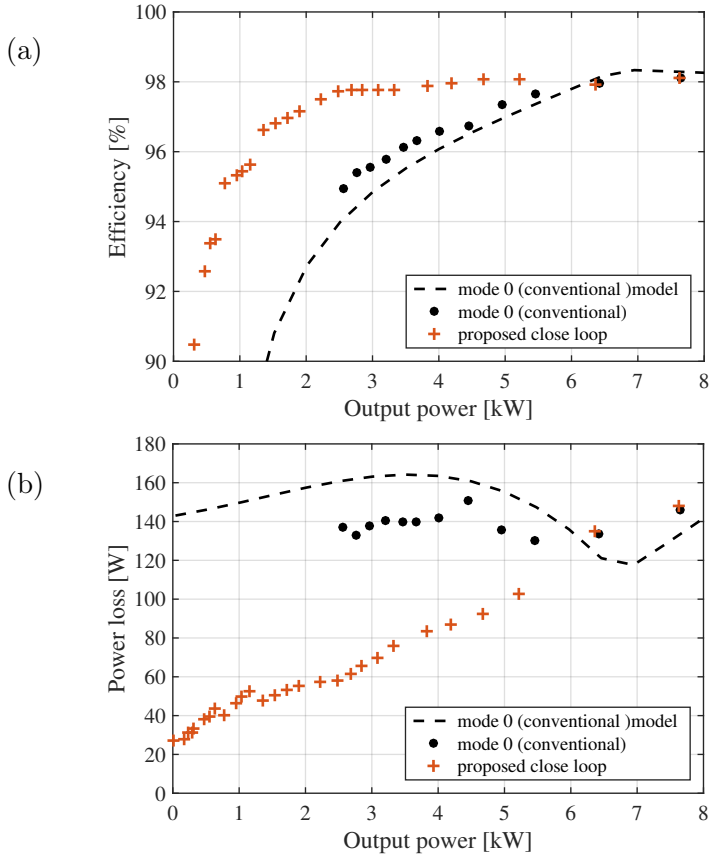


(b)



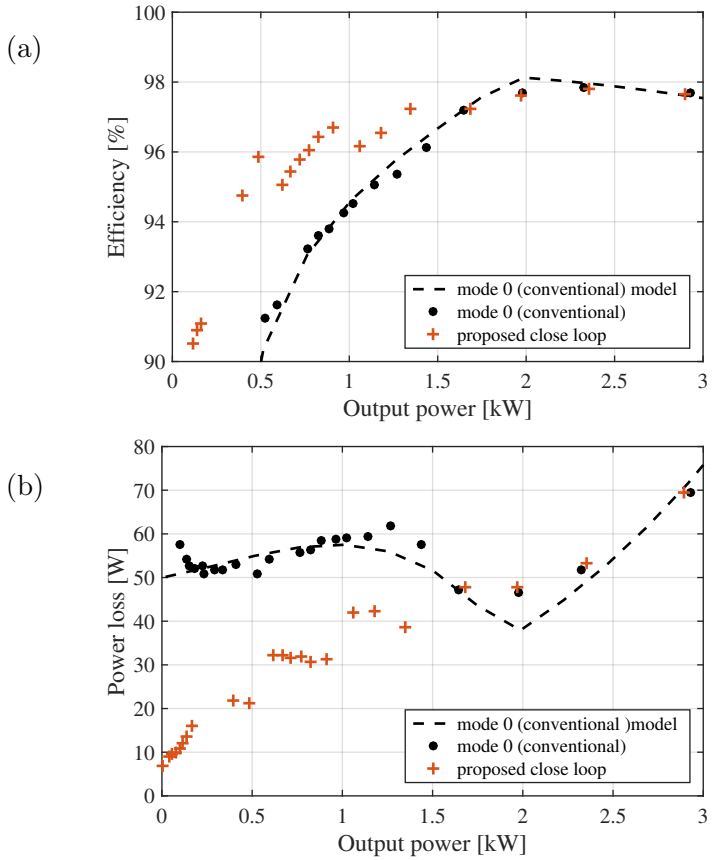
ciency deviates from the optimum trajectory, it still shows much higher efficiency than that in the conventional approach. Fig. 4.40(b) plots the measured converter loss. At open load condition, the power loss is reduced by more than 5 times.

Figure 4.41: Measured DCX close loop operation at maximum 200 V input: (a) efficiency; (b) power loss.



One concern of the proposed control algorithm is that the optimum dead time in each mode as well as the voltage conversion ratio boundary may vary with input voltage. If the input voltage deviates from the nominal 150 V value, the proposed control algorithm may lead to sub-optimal operation. To verify the control parameter sensitivity to voltage, Fig. 4.41 measures the close loop operation at maximum 200 V input, and Fig. 4.42 measures the close loop operation at minimum 100 V input, both with the same fixed parameters as those used in Fig. 4.40. They show that the control algorithm is not very sensitive to input voltage. At maximum input voltage, the close loop

Figure 4.42: Measured DCX close loop operation at minimum 100 V input: (a) efficiency; (b) power loss.



operation shows very good efficiency. Greater than 97% efficiency is measured for load larger than 10% of the rated power. At minimum input voltage, though the efficiency is slightly lowered, it is still much better than the conventional approach. What is more, notice that at maximum 200 V input voltage, the conventional operation is unable to operate for output power less than 2.5 kW without exceeding the maximum 420 V output voltage limit. With the close loop operation, the converter can safely operate down to zero watt output.

4.5 DCX heavy load efficiency improvement

In most of the DCX discussion so far, it is mainly focused on the case of passive rectification operation, due to its simplified control scheme and robustness. However, in the application where

the bi-directional power flow is required, on DCX secondary side actually MOSFETs are deployed. Therefore, for bi-directional power flow application, both passive and active rectification (DAB) operation can be realized, without hardware modification.

Notice that with secondary side active rectification, extra gate driver power is consumed. In the case of the 20 kW DCX prototype concerned, the active rectification requires extra 4 W driver loss, which is not included in our following discussions.

As indicated in Section 4.3.3, at heavy load, the device conduction loss and magnetics copper loss dominates the total loss. The active rectification has the potential to reduce some of these losses. There are many active rectification control methods proposed in literature, addressing different technical issues. In the application of this work, the voltage regulation is not required, while efficiency consideration is of first priority. On the other hand, at heavy load, the ZVS operation is desired, since it exhibits better robustness comparing to hard switching.

The easiest way to implement active rectification without losing ZVS is to keep the passive phase control operation of DCX. Therefore, the MOSFETs only turns on after the body diodes turn on, and turn off before the body diodes turn off. The phase shift is still passively determined by the body diodes, as in the case of passive rectification, and the active rectification only reduces the device conduction loss.

Figure 4.43: DAB operation with passive phase shift control at 18 kW output power. The channel 4 signal (green) is the secondary side low-side MOSFET gate-to-source voltage (v_{gsLS}).

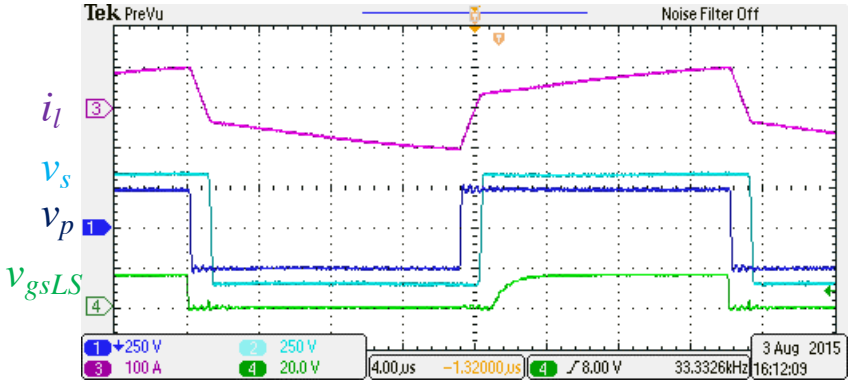
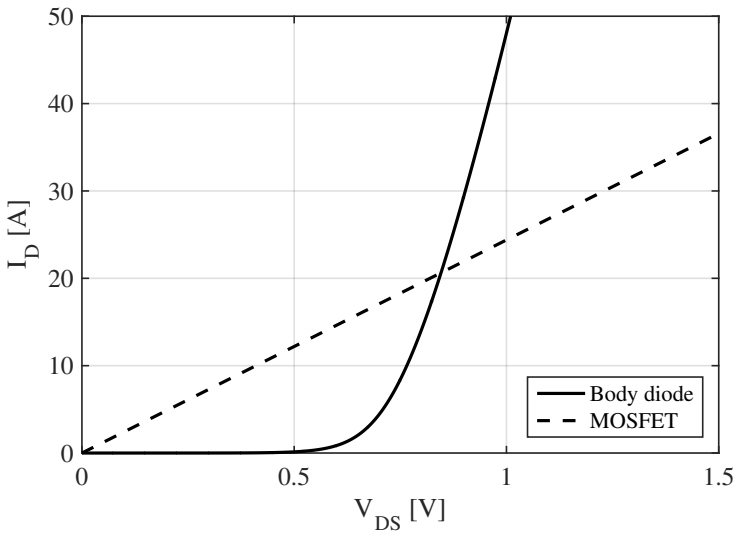


Figure 4.43 shows the measured waveform of the DAB operation with passive phase shift

control, at 18 kW output power. Channel 4 signal (green) is the secondary side low-side MOSFET gate-to-source voltage (v_{gsLS}). The gate voltage does not rise until the secondary side commutation (v_s) is complete where diodes conduct, and the gate voltage falls before the next secondary side commutation begins where diodes turn off. The tank inductor current shows the same waveform as that with passive rectification.

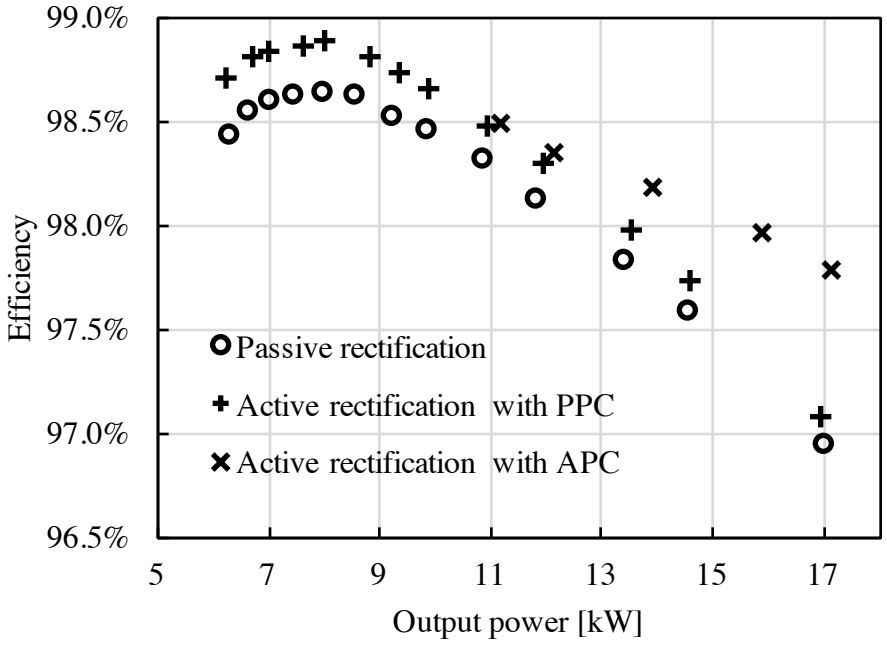
Figure 4.44: Infineon IPW65R041CFD 650 V 41 mΩ CoolMOS channel conduction versus body diode conduction.



Therefore, this operation does not affect the converter operation. It only turns on the MOSFET channel, which is in parallel with the body diode. Figure 4.5 plots the MOSFET channel conduction versus body diode conduction. Because the MOSFET channel can be modeled as a constant resistance, at low current level, the MOSFET channel conduction shows much lower voltage drop, therefore much smaller conduction loss. However, as the current level increases, the body diode voltage drop does not increase much, and it is expected that turning on the MOSFET will not significantly reduce conduction loss. Figure 4.5 plots the measured efficiency of passive rectification and active rectification with passive phase control. It is as expected that the efficiency improvements at light to medium load is more significant than heavy load.

Figure 4.46 shows another type of active rectification, where the phase shift is actively con-

Figure 4.45: Efficiency comparison of passive rectification, active rectification with passive phase control (PPC), and active rectification with active phase control (APC), at fixed 250 V input voltage.

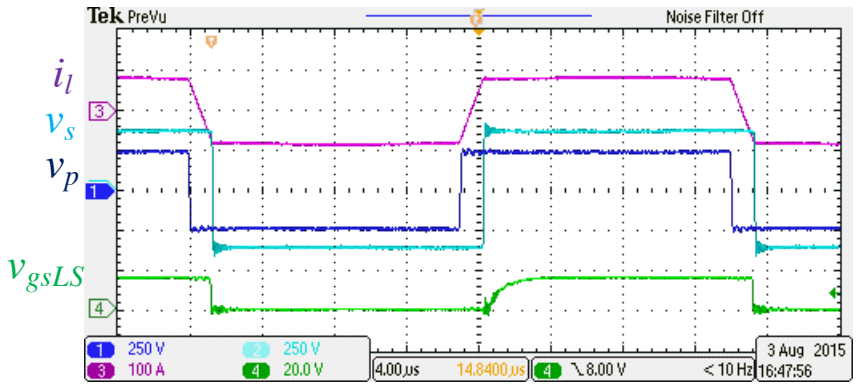


trolled by the secondary MOSFETs. The secondary side MOSFET does not turn on until the body diode turns on, but it turns off after the body diode turns off. Therefore, a larger phase shift can be achieved. In the case shown in Fig. 4.46, the phase shift is controlled so that $M = 1$. Therefore, the tank inductor current i_ℓ exhibits trapezoidal waveform, with reduced peak and rms current level than that in Fig. 4.43. Therefore, both the conduction loss and magnetic copper loss can be reduced. Because of the trapezoidal current waveform in tank inductor, it is expected that the $\mathrm{d}B_\ell/\mathrm{d}t$ in tank inductor is also reduced, resulting in reduced tank inductor core loss as well. Finally, since the MOSFET still conducts when the diode turns off, the diode switching loss due to diode reverse recovery is eliminated too.

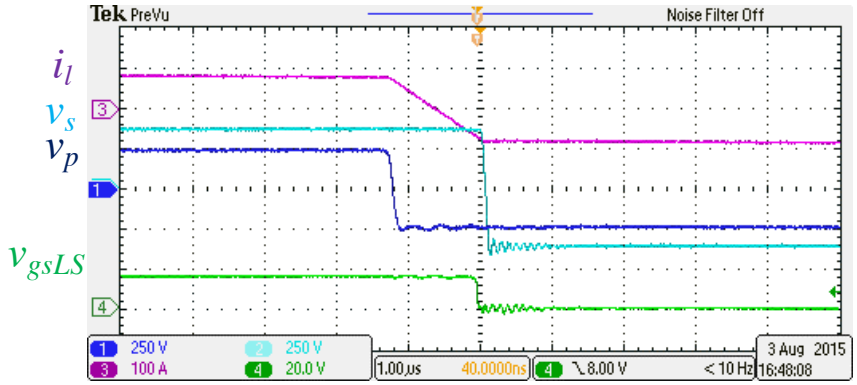
As shown in Fig. 4.5, the active rectification with active phase shift control show significant efficiency improvements at heavy load. In specific, at 17 kW, nearly 30% total loss reduction is achieved. This is because when the phase shift is controlled to $M = 1$, several loss reduction mechanisms are addressed.

Figure 4.46: DAB operation with active phase shift control at 18 kW output power. The channel 4 signal (green) is the secondary side low-side MOSFET gate-to-source voltage (v_{gsLS}). The phase shift is controlled so that $M = 1$. (a) operation waveform of one switching period; (b) zoom in at commutation transition.

(a)



(b)



However, with active phase control, without losing secondary side ZVS, it requires turning off the MOSFET after the diode turns off. Therefore, the phase shift can only be actively controlled to be larger than the phase shift defined by the passive phase control. In other word, without losing secondary side ZVS, it is only allowed to control the voltage conversion ratio M to be larger than that in passive rectification case, not smaller. At light load with $M > 1$, it is impossible to operate with active phase control without losing ZVS. Therefore, to achieve optimum efficiency Ideally the optimum efficiency can be achieved by operating with active phase control of $M = 1$ at heavy load, and transit to passive phase control at medium to light load.

4.6 Efficiency-enhanced Dual Active Bridge control

The purpose of efficiency-enhanced DAB control is to combine the light load and heavy load efficiency improvements introduced in previous sections, so that:

(1) Synchronized rectification is achieved, and the secondary side conduction loss is reduced.

(2) The rms current is minimized at heavy load, the associated conduction and magnetics losses are reduced.

(3) Proposed resonant operation is achieved at light load, so that switching loss is much reduced.

(4) The variation of voltage conversion ratio M is reduced, and the effort of voltage regulation by other modules in the composite architecture is relieved.

For a given DAB power stage design, the efficiency-enhanced DAB control should be able to exploit the best achievable efficiency over the full load range.

The efficiency-enhanced DAB control algorithm utilizes three control variables: the primary side dead-time t_{Dp}, the secondary side dead-time t_{Ds}, and the phase-shift between primary side and secondary side t_{ps}, as illustrated in Fig. 4.47.

At heavy load, it is expected that the phase-shift control variable t_{ps} will actively control the effective phase-shift t_{φ}, so that the voltage conversion ratio M is regulated to unity. This is referred as active phase control (APC) in the previous section. In this mode, the dead-times t_{Dp} and t_{Ds} are kept at minimum value, as long as they are longer than the resonant commutation time, and ZVS is achieved. As the output power decreases, t_{ps} keeps decreasing, until it is smaller than the diode reverse recovery time. From that point, t_{ps} no longer controls the effective phase-shift t_{φ}, and the voltage conversion ratio deviates from unity. This is previously referred as passive phase control (PPC). As the output power further decreases, the primary side of the DAB may lose ZVS in the conventional operation mode, and the DAB should begin to operate in the resonant mode, where the dead-times t_{Dp} and t_{Ds} significantly increases. Figure 4.48 illustrates these different modes in the efficiency-enhanced DAB control.

Figure 4.47: Timing diagram of efficiency-enhanced DAB control

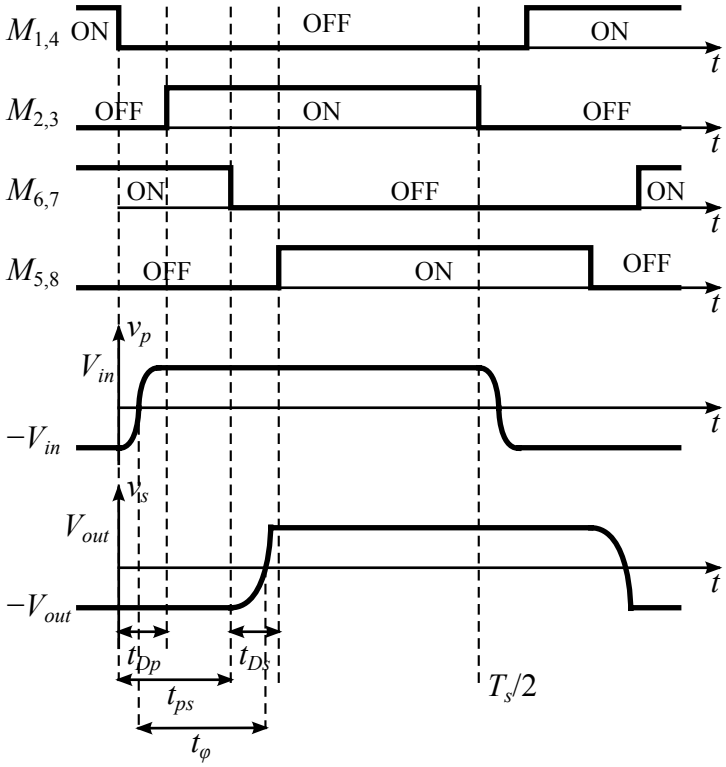


Figure 4.48: Modes in efficiency-enhanced DAB control

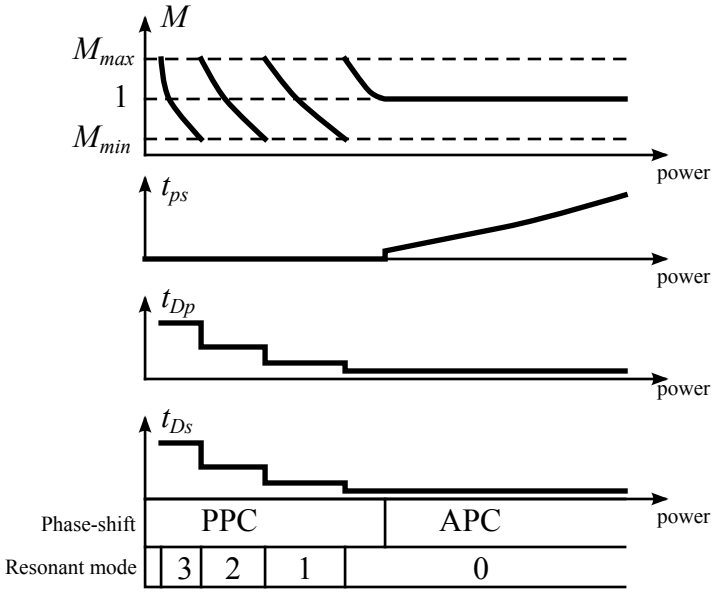
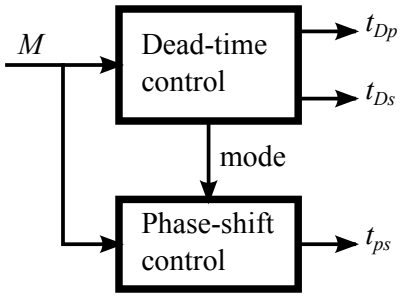


Figure 4.49: Efficiency-enhanced DAB control block diagram



The controller behavior described by Fig. 4.48 can be realized by the control block diagram in Fig. 4.49. It is composed of two sub-systems: the dead-time control block and the phase-shift control block. The dead-time control block implements the algorithm described in Fig. 4.39. It hops between different resonant modes with different dead-times t_{Dp} and t_{Ds}, to keep the voltage conversion ratio M between the boundaries M_{min} and M_{max}. The phase-shift control can be a simple PI controller that regulates the voltage conversion ratio M to unity at heavy load. At medium to light load, the integrator inside the phase-shift control will naturally saturate to zero, so that the system can smoothly transit from APC to PPC. As the output power further decreases, the dead-time control block freezes the phase-shift control, and enters the resonant operation mode.

Although the control algorithm in Fig. 4.49 may seem complicated, the purpose of the control is to enhance the efficiency of the system, therefore, it is not necessary to perform the calculation and adjust the control variables in a fast update rate. The controller only needs to follow the rate of change of the system power, and slight efficiency drop during transients is tolerable. For electrified traction system application, even 10 Hz update rate is sufficient.

A 20 kW DAB prototype with 1:1.5 turns ratio is implemented, with the efficiency-enhanced DAB control algorithm. The details of the implementation is documented in appendix B. The experimental results are shown in Fig. 4.50 – 4.53. Figures 4.50 & 4.51 show the measured efficiency and power loss at different output level, with fixed minimum 100 V input. Figures 4.52 & 4.53 show the measured efficiency and power loss at different output level, with fixed maximum 250 V input.

At both minimum and maximum input voltage, the DAB control improves the converter

Figure 4.50: Measured efficiency comparison of open loop operation and DAB close loop operation, at fixed 100 V input voltage.

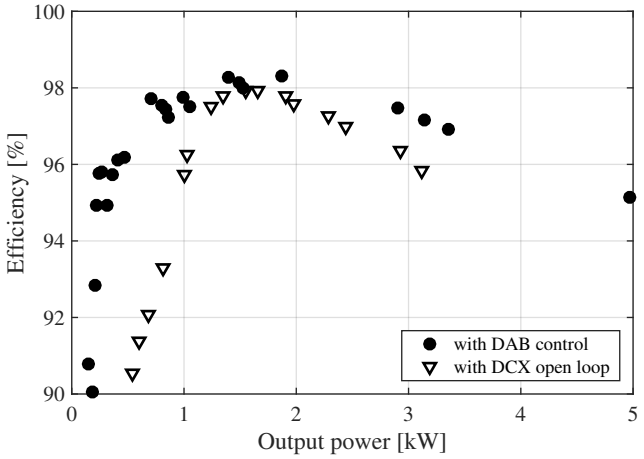


Figure 4.51: Measured power loss comparison of open loop operation and DAB loop operation, at fixed 100 V input voltage.

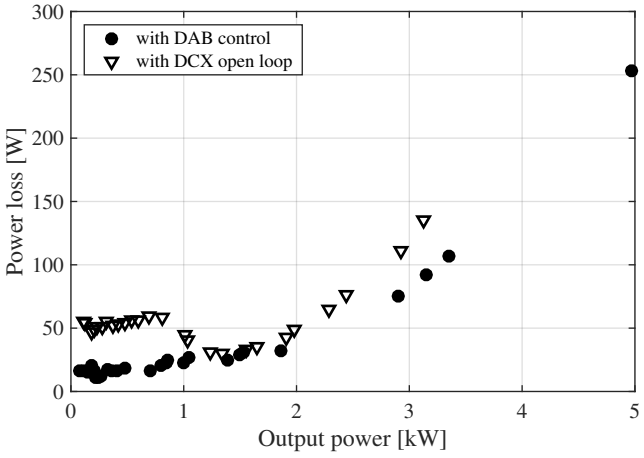


Figure 4.52: Measured efficiency comparison of open loop operation and DAB close loop operation, at fixed 250 V input voltage.

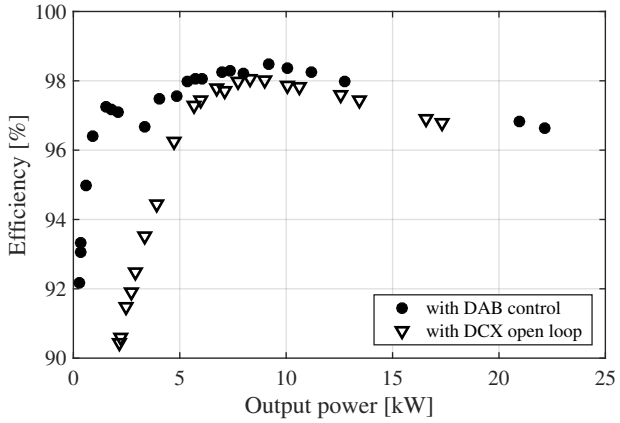
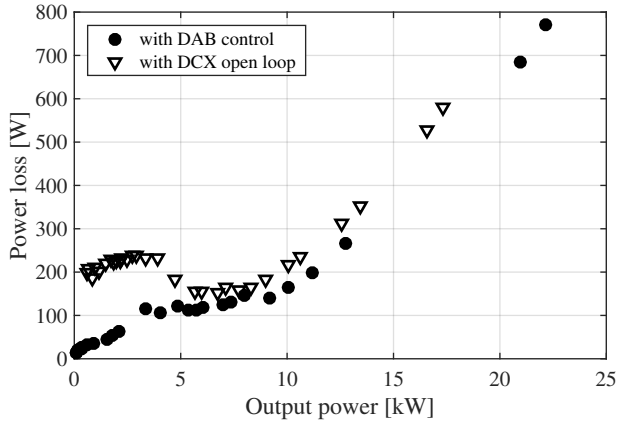


Figure 4.53: Measured power loss comparison of open loop operation and DAB loop operation, at fixed 250 V input voltage.



efficiency over the full load range. Particularly, the power loss at light load operation is significantly reduced, which is favorable for the powertrain application. Because of the switching loss, the power loss in DCX operation keeps almost constant at light load, which is around 50 W for 100 V input, and 200 W for 250 V input. In contrast, with efficiency-enhanced DAB control, the power loss decreases as the output power decreases, and reaches the minimum of around 16 W for both 100 V input and 250 V input. At 250 V input, with efficiency-enhanced DAB control, the efficiency stays above 96% with the output power range from 900 W to 22 kW, and the peak efficiency of 98.5% is recorded

at 9 kW output. It is almost the highest achievable efficiency for the given converter power stage design.

Table 4.3: Predicted converter quality factor Q of the 20 kW DCX module prototype within a composite D converter, under different driving profiles (with 250 V battery voltage).

	UDDS	HWFET	US06
open loop	8.11	9.59	13.96
with efficiency-enhanced DAB control	56.47	108.16	88.42

Table 4.3 compares the converter quality factor Q of the DCX converter module, assuming that it is within a composite D converter, under different driving profiles. With a constant 250 V battery voltage, it shows that with the efficiency-enhanced DAB control, the average loss of the DCX module can be reduced by a factor of six to eleven, with the proposed efficiency-enhanced DAB control.

Chapter 5

Implementation Examples of Composite DC-DC Converter

In this chapter, the concept of composite converter is verified experimentally with several prototypes. Section 5.1 – 5.3 demonstrate composite converters realized with silicon-based device, which currently is still the dominant technology in the electrified traction powertrain application. Three composite D converter prototypes are designed and manufactured, with different power levels, which also illustrates the scalability of the composite converter approach. Based on the comparisons in Chapter 3, the composite D converter is chosen because it predicts the best efficiency among the others. Section 5.1 documents a 10 kW pilot design as a preliminary validation. The design of a 30 kW prototype is shown in section 5.2, whose power level is appropriate for a medium-sized hybrid electric vehicle. A 60 kW prototype is demonstrated in section 5.3, which is applicable in a medium-sized electric vehicle or plug-in hybrid electric vehicle. In section 5.4, the composite converter architectures are reassessed in the context of wide bandgap device, which is the future trend of the power device technology. It demonstrates how composite converter can enhance the wide bandgap technology to achieve very high power density design.

5.1 10 kW silicon-device-based prototype

In this section, a 10 kW converter prototype is designed, and the composite D converter architecture is considered, which shows the best efficiency in the comparison in section 3.6. The input voltage is allowed to vary between 150 V and 300 V. The boost ratio is between 1 and 3.8, while the maximum output voltage is limited to 800 V. However, most of the time, the converter is

operated at neither maximum power nor maximum voltage.

5.1.1 Design optimization

It is desired to reduce the DCX and boost module voltage rating to 400 V, so that 600 V semiconductor devices can be utilized, according to the 33% de-rating rule of our specified application. Therefore, at $V_{out} = 800\,\text{V}$, the output voltages of both the DCX and boost modules must be exactly 400 V, regardless of input voltage.

Since the system conversion ratio $M \leq 3.8$, at $V_{out} = 800\,\text{V}$, $V_{in} \geq 211\,\text{V}$. The DCX output voltage is limited to $V_{DCX,out} = V_{in} M_{buck} N_{DCX} = 400\,\text{V}$. Since $M_{buck} \leq 1$, this implies that $N_{DCX} \geq 400/211 = 1.9$.

It is desired to maximize the boost plus DCX operating area to achieve lower DCX primary side transformer current and lower inductor current. Since the lowest conversion ratio the boost plus DCX mode can achieve is $M = N_{DCX} + 1$, maximizing boost plus DCX operating area requires minimization of N_{DCX}. At the same time, minimizing N_{DCX} also minimizes the operating area where the buck and boost modules operate simultaneously. Hence, switching loss is reduced as well.

Therefore, the minimum value $N_{DCX} = 1.9$ is chosen. The operating modes of each converter module still follow the segmentation illustrated in Fig. 3.16. When the output voltage is lower than 400 V, the boost module can operate alone, with DCX and buck modules shut down. When the output voltage is higher than 400 V, either the buck or the boost module is in the pass-through mode, depending on whether the system conversion ratio M is greater or less than $1 + N_{DCX}$. If the input voltage is higher than 211 V, the buck converter will limit the DCX output to 400 V, and all three modules operate simultaneously.

For $N_{DCX} = 1.9$, the rated operating conditions of each module are listed in Table 5.1. With the module output voltage stress limited to 400 V, derated 600 V devices can be utilized. In the experimental prototype, Fairchild FCH76N60NF 650 V 43 A super-junction MOSFET with fast-recovery body diode is used. To meet the worst-case current rating, the buck and boost modules use two MOSFETs in parallel for each switch. The DCX module uses two MOSFETs in parallel for

Table 5.1: Module specification summary

DCX	Max. Input Voltage [V]	211
	Max. Output Voltage [V]	400
	Max. Output Current [A]	25
	Max. Input Current [A]	47.5
Boost	Max. Input Voltage [V]	300
	Max. Output Voltage [V]	400
	Max. Conversion Ratio	2.7
	Max. Input Current [A]	67
Buck	Max. Input Voltage [V]	300
	Max. Output Voltage [V]	211
	Min. Conversion Ratio	0.18
	Max. Output Current [A]	47.5

each switch at the primary side, and one MOSFET for each switch at the secondary side.

The detailed design of each module can now be optimized numerically, according to specified operating condition distribution. In section 4.3, the DCX loss model has been discussed, while the loss model of buck and boost converter modules has been derived in section 2.1.2. For semiconductor loss, the conduction loss model is extracted from the device data sheet. The empirical switching loss model is curve fitted according to simulation models provided by the manufacturer. The core loss model is curve fitted according to material data sheet, while the inductor copper loss is calculated using Dowell's equation [30].

Partial power efficiency can be further optimized by use of the inductor current ripple to achieve zero-voltage switching at moderate-to-low currents. The body diodes of the super-junction MOSFETs exhibit significant reverse-recovery losses [13]. To optimize partial-power efficiency, the boost and the buck modules can be designed with negative instantaneous transistor current at the turn-on transitions to achieve zero-voltage switching at low to moderate power.

Due to the soft-switching behavior, the DCX module exhibits low switching loss. Therefore, the DCX module is able to operate at higher switching frequency, and ferrite core materials are employed for the DCX transformer and tank inductor. The tank inductor value is chosen to achieve

Table 5.2: Composite converter design summary

Buck / Boost	Number of MOSFET dies	4
	Estimated total silicon area	265 mm^2
	Switching frequency	15 kHz
	Inductance	120 µH
	Inductor peak current	80 A
	Inductor winding	#44 Litz wire, 1000 strands
	Inductor core material	metal powder
	Inductor core volume	51 cm^3
DCX	Number of MOSFET dies	12
	Estimated total silicon area	794 mm^2
	Switching frequency	33 kHz
	Transformer turns ratio	22:42
	Transformer winding	#44 Litz wire, 1500 strands on primary, 880 strands on secondary
	Transformer core material	ferrite
	Transformer core volume	72 cm^3

zero-voltage switching of the MOSFET body diodes [49] and to minimize the transformer rms current at an intermediate power such that the system efficiency is optimized.

The resulting composite converter design parameters are summarized for this 10 kW prototype in Table 5.2.

5.1.2 Comparison with Conventional Boost Converter

In this section, the design of the 10 kW composite converter D prototype is compared with the conventional boost converter approach, in terms of power efficiency, silicon device usage and capacitor size. The capacitor size is compared as total capacitor energy storage rating and power rating. The silicon device usage is quantified in terms of device rms current rating at full load.

Table 5.3: Switch rms current comparison at 210 V input, 650 V output with 5 kW output power

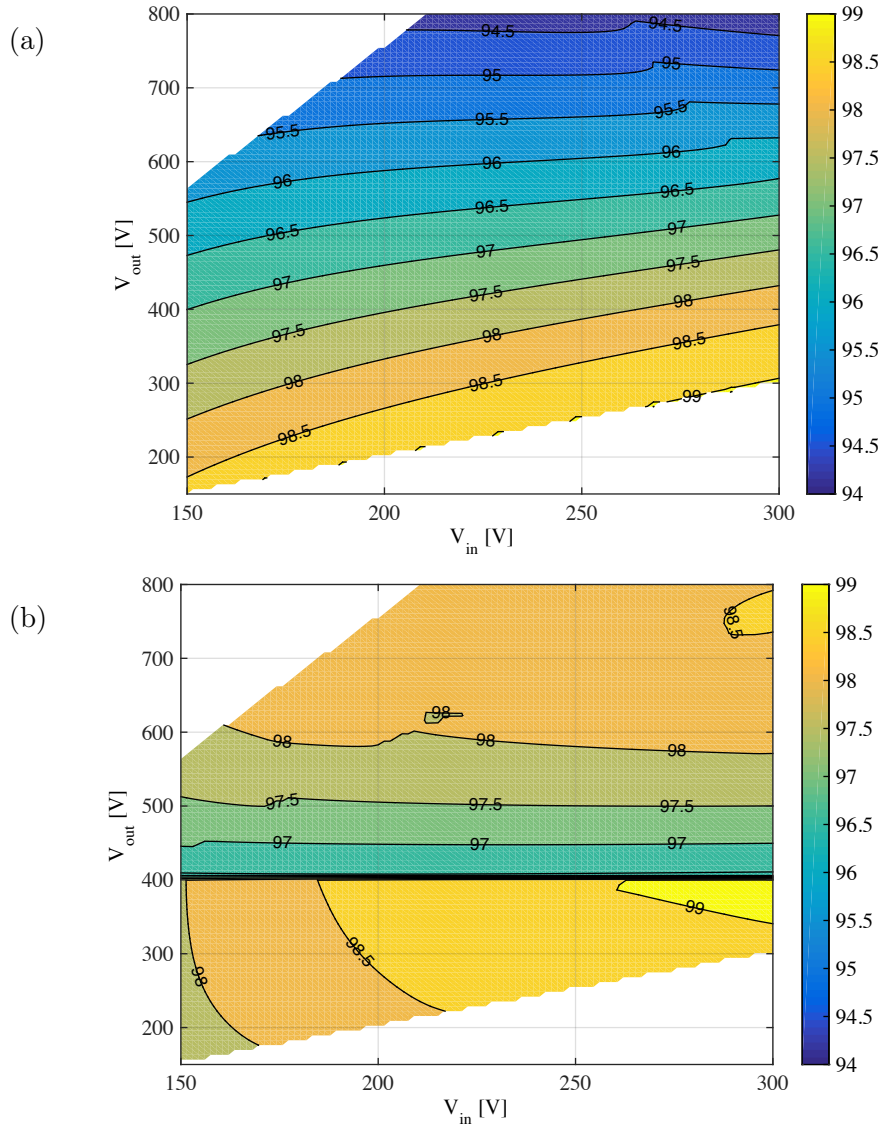
	System input current	23.8 A
	System output current	7.7 A
Conventional	Low-side switch	19.6 Arms
	High-side switch	13.5 Arms
Composite	Boost low-side switch	3.7 Arms
	Boost high-side switch	8.4 Arms
	Buck low-side switch	0 A
	Buck high-side switch	14.6 A (DC)
	DCX primary switch	14.6 Arms
	DCX secondary switch	7.7 Arms

5.1.2.1 Switch Rms Current Comparison

To illustrate the benefits of reduction of indirect power achieved by the proposed composite converter architecture, the ideal switch rms currents in the composite converter are compared with those of a conventional boost converter, at a typical partial-power operating point, where V_{in} = 210 V, V_{out} = 650 V, at a 5 kW load. The comparison is summarized in Table 5.3. The inductor current ripple is ignored in this comparison. Therefore, the data listed in the table is independent of the choice of devices, switching frequency, and magnetics design.

The switch rms current in the boost module of the composite design is much reduced, relative to the conventional boost converter, while the buck module in pass-through mode only carries dc current. The DCX module can handle the trapezoidal current with ZVS at very high efficiency. Therefore, the proposed composite design has the potential to greatly reduce system ac power loss, and improve system efficiency. An additional benefit of the composite architecture is the ability to employ devices having lower voltage ratings and hence faster switching speed and lower switching loss.

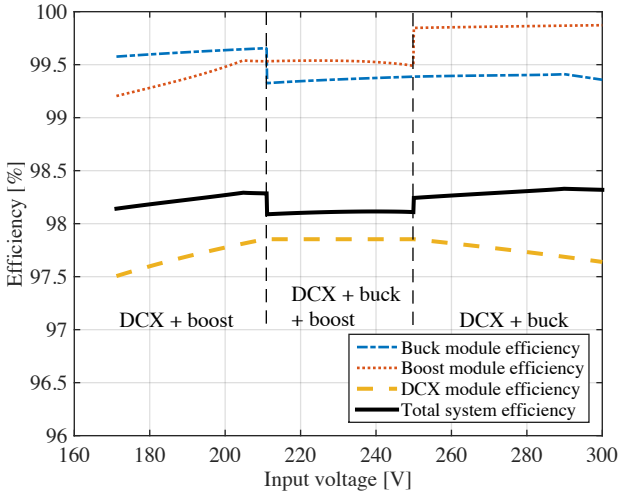
Figure 5.1: Converter efficiency comparison: (a) predicted conventional boost converter efficiency vs. V_{in} & V_{out}, at $P_{out} = 5\,\text{kW}$, (b) predicted composite converter efficiency vs. V_{in} & V_{out}, at $P_{out} = 5\,\text{kW}$



5.1.2.2 Theoretical Efficiency Comparison

To compare the performance of the composite converter with a conventional approach, a similar 10 kW boost converter is designed using 1200 V IGBTs. The IGBT total silicon area is chosen to be the same as that of the composite converter design. The inductor core size is also chosen to have the same volume as the total magnetics core volume in the composite converter

Figure 5.2: Calculated converter module efficiency and total system efficiency as functions of the input voltage, at $V_{out} = 650\,\text{V}$, $P_{out} = 5\,\text{kW}$.



design. Owing to the high switching loss of the IGBT, the switching frequency is limited to 10 kHz. The calculated efficiency is plotted versus input and output voltage at fixed 5 kW output power, as shown in Figure 5.1(a). It can be seen that the converter efficiency significantly drops as conversion ratio increases. For a fixed input / output voltage combination, the converter efficiency improves as output power increases, and it reaches peak efficiency at full power. At a typical partial-power operating point where $V_{in} = 210\,\text{V}$, $V_{out} = 650\,\text{V}$, at a 5 kW load, the efficiency is slightly less than 96%.

The calculated efficiency of proposed composite converter is plotted in Figure 5.1(b), at 5 kW. The efficiency is generally higher than that of conventional boost converter, and the efficiency does not degrade significantly as conversion ratio increases. For fixed input / output voltage combination, the system peak efficiency occurs at some intermediate power level rather than at full power. At operating point where $V_{in} = 210\,\text{V}$, $V_{out} = 650\,\text{V}$, at a 5 kW load, the efficiency is approximately 98.5%.

Figure 5.2 shows efficiency of each converter module in different operation modes as functions of the input voltage, at fixed 650 V output voltage, 5 kW output power. Since the buck and the boost module process only partial power with conversion ratios close to one, their efficiencies are

Table 5.4: Capacitor rating for conventional and composite converters

		Voltage rating [V]	RMS current rating [A]	Minimum capacitance required [μF]
Conventional	Input	300	6	100
	Output	800	57.3	300
Composite	Input	300	40	100
	Buck output	210	21	300
	DCX output	400	5	100
	Boost output	400	34	222

Table 5.5: Total capacitor energy and power rating comparison

	Total capacitor energy storage rating [J]	Total capacitor power rating [kW]
Conventional	100.5	47.7
Composite	36.2	37.1

very high.

5.1.2.3 Capacitor Rating Comparison

With reduced module voltage stress, the capacitor voltage ratings in the composite converter can also be reduced. In comparison to the conventional boost converter, the modules of the composite converter employ higher switching frequencies and therefore the capacitances can be reduced as well, while maintaining the same output voltage ripple. Therefore, although the composite converter employs an increased number of individual capacitor elements, the total capacitor energy storage rating can be lower than conventional boost converter.

In a typical boost converter, the output capacitor rms current rating typically constrains the capacitor size and cost, rather than the capacitance itself. Since rms capacitor current is independent of the switching frequency, simply increasing the switching frequency will not reduce the capacitor size. In pass-through mode, the buck or boost modules do not apply ac currents to their capacitors,

and operating points near pass-through mode exhibit low rms capacitor currents. The DCX module exhibits relatively low capacitor rms currents as well, particularly when the transformer winding currents are trapezoidal. Hence, the capacitor rms current requirements are substantially lower than in the conventional boost converter operating at high duty cycle.

The minimum capacitance required to achieve the worst case ±5 V output voltage ripple is calculated, for both the conventional boost converter and the proposed composite converter. The rms current rating for each capacitor is calculated as well, and the results are listed in Table 5.4, for the specific 10 kW application. It is assumed that a fixed 100 µF input capacitor is used for both cases.

The energy storage rating is calculated as $0.5CV_{rate}^2$, while the power rating is calculated as $V_{rated}I_{rms,rated}$. Table 5.5 summarizes the total capacitor energy storage ratings and power ratings. The composite converter requires both lower energy and power ratings, which can lead to reduced capacitor cost.

5.1.3 Experimental Results

The 10 kW composite converter example described earlier has been built. Its open-loop operation has been demonstrated and tested in all operating modes.

Figure 5.3 shows the operation in DCX plus Boost mode. The DCX waveforms are shown in the upper half of the figure, operating at 210 V input and 400 V output. Both the primary and secondary side devices of the DCX operate with ZVS, as implied by the smooth transition of switching node voltages. The secondary side switching node voltage is measured with a differential probe, with reference to the negative output of the DCX. The buck and boost module waveforms are shown in the lower half of the figure. With high-side MOSFET constantly on, the buck module operates in pass-through mode, and only DC current flows through its inductor. The boost module operates with 210 V input and 250 V output, and therefore the total output voltage is 650 V. At this operating point, the output power is approximately 5 kW, and the boost module operates in boundary conduction mode.

Figure 5.3: Composite converter operation in DCX + Boost mode

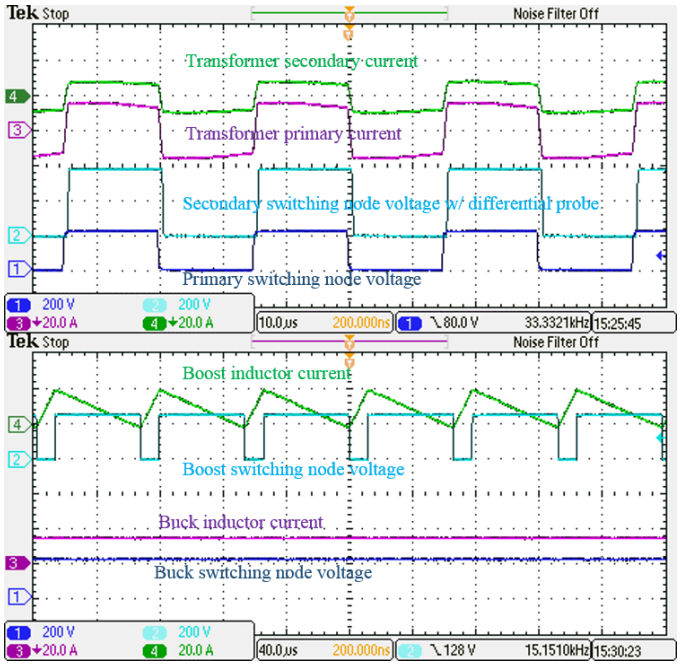


Figure 5.4 shows operation in DCX plus Buck mode, where the system input voltage is approximately 210 V. The buck module operates with approximately 50% duty cycle, while the boost module operates in pass-through mode. The DCX operates at approximately 100 V input and 190 V output. As a result, the total system output voltage is 410 V.

Figure 5.5 illustrates operation in DCX plus Buck plus Boost mode, where the system input voltage is 230 V. The buck module output is 210 V, while both the boost and DCX module outputs are 400 V. The total system output is 800 V.

Figure 5.6 plots the measured efficiency with different input / output voltages, at fixed 5 kW output power. The highest efficiency recorded is 98.7%, at approximately 210 V input and 650 V output. All points with output voltage greater than 500 V achieve measured efficiency higher than 98%. When the output voltage is slightly above 400 V, and the system operates in DCX plus Buck mode, the efficiency slightly drops to 97.2%, due to the small buck module conversion ratio. However, when the output voltage is below 400 V, the system can operate in Boost only mode, and the measured efficiency is higher.

Figure 5.4: Composite converter operation in DCX + Buck mode

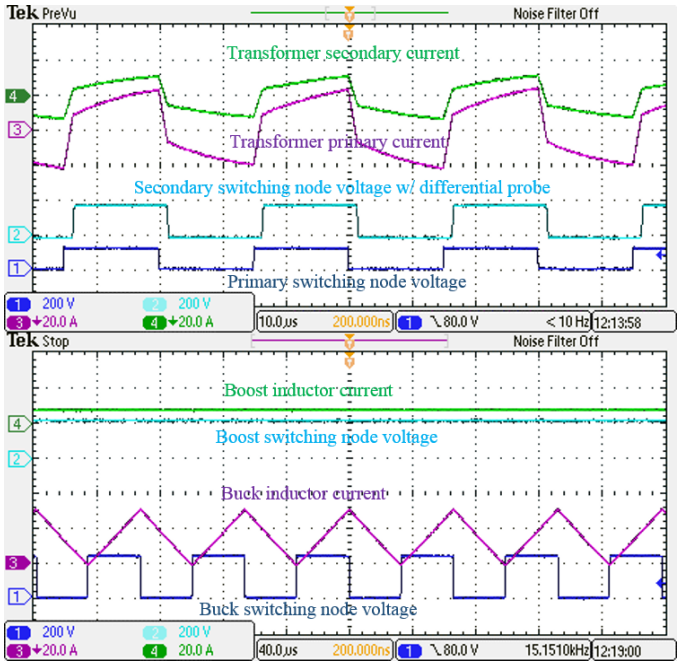


Figure 5.5: Composite converter operation in DCX + Buck + Boost mode

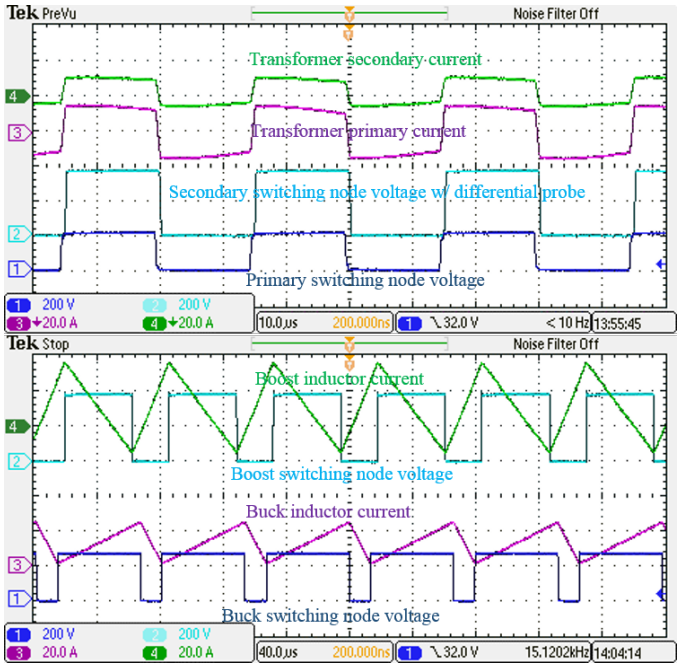
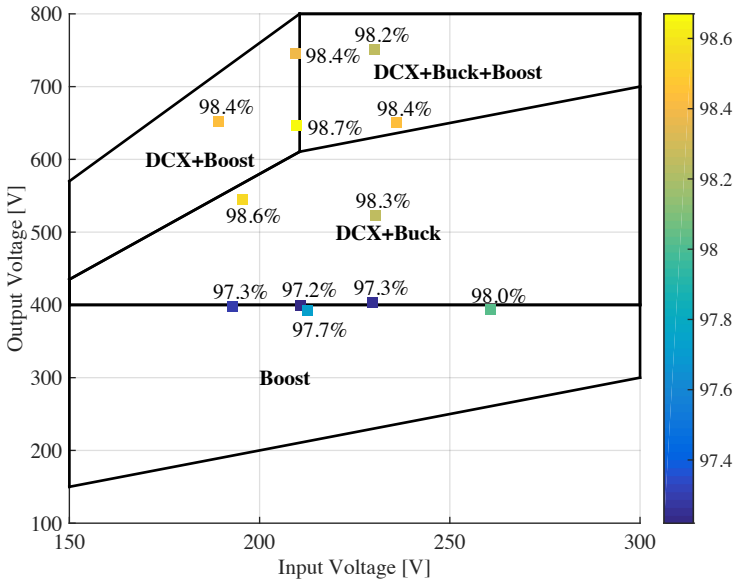


Figure 5.7 shows the measured efficiency versus output power at different input / output voltages and different operating modes. The measured results are compared with theoretical model

Figure 5.6: Measured composite converter efficiency vs. V_{in} & V_{out}, at $P_{out} = 5\,\text{kW}$



used in design. The measurements show slightly higher efficiency than theoretical calculation. This is mainly because the actual semiconductor junction and copper winding temperatures in the experiment are lower compared to the worst-case values assumed in the theoretical model. As a result, the actual conduction losses are slightly lower compared to the model.

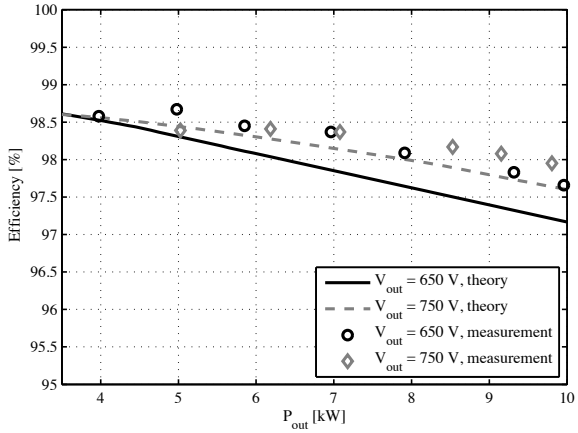
The 10 kW prototype proofs that the concept of composite converter works, and the composite converter D does significantly improve the efficiency and achieves capacitor module size reduction. The prototype also validates that the loss model used in the design phase is sufficiently accurate. However, 10 kW is a scaled-down power rating for the electric vehicle specification. In the following section, a second prototype is designed with extended power rating to meet the realistic vehicle traction power requirement.

5.2 30 kW silicon-device-based prototype

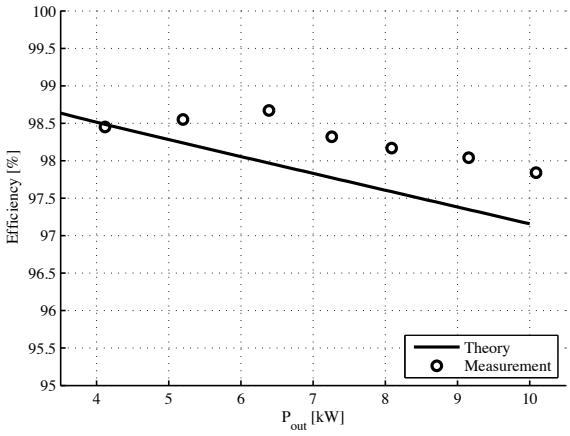
In this section, a 30 kW composite D converter prototype is considered. The voltage requirement keeps the same as that of the 10 kW prototype, that is, the input voltage range is from 150 V to 300 V, while the maximum output voltage is 800 V. The maximum voltage conversion ratio is

Figure 5.7: Measured converter efficiency vs. output power: (a) $V_{in} = 210\,\mathrm{V}$. Converter operates at DCX + boost mode; (b) $V_{in} = 260\,\mathrm{V}$, $V_{out} = 650\,\mathrm{V}$. Converter operates at DCX + buck mode; (c) $V_{in} = 260\,\mathrm{V}$, $V_{out} = 750\,\mathrm{V}$. Converter operates at DCX + buck + boost mode.

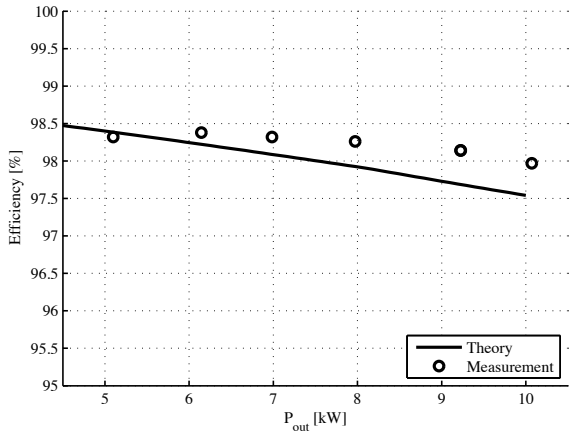
(a)



(b)



(c)



limited to 3.8. This power rating is suitable for a medium-sized full-hybrid electric vehicle. For example, in Toyota Prius 2012, with a 60 kW traction motor and a 30 kW generator, the maximum power required from the battery pack via the dc-dc converter is 30 kW.

Because the voltage rating of the 30 kW prototype keeps the same as that of the 10 kW one, the same device voltage rating can be used, but more paralleled devices should be used to handle the increased current level. In the 30 kW prototype, Infineon IPW65R045CFD 650 V 41 mΩ CoolMOS with fast-recovery body diode is used, due to its excellent ruggedness. Five MOSFETs are connected in parallel for each switch in buck module, boost module, as well as the primary side of DCX module. The switches in DCX secondary side are composed of two MOSFETs in parallel each.

With the loss model of the device, the optimum switching frequency for DCX module is 33 kHz. Although the optimum switching frequency for the buck and boost module is below 20 kHz, to avoid the human audible frequency range, the switching frequency of the buck and boost module is set to 20 kHz. The magnetics of the converter have to be redesign, with the same voltage level and frequency, but scaled current level.

5.2.1 Magnetics design

Ways to increase the magnetics current rating include:

(1) Use thicker winding wires to reduce the winding resistance. The increased skin effect and proximity effect should be considered.

(2) Increase the magnetics core size so that there is sufficient winding window area for the increased wire size. On the other hand, enlarging the core cross-section area can reduce the number of winding turns, which also reduces the winding resistance. However, increasing the core cross-section area also increases the mean-length-per-turn (MLT) of the winding. Therefore, the winding resistance is only approximately inversely proportional to the square root of the cross-section area.

(3) Utilize core materials with higher flux density saturation level, therefore the number of

winding turns can be reduced. On the other hand, these materials usually exhibit higher core loss, and there are balances between core loss and copper loss.

The prototype fabrication is done in the research lab, where the manufacturing resources are limited. Therefore, there exist trade-offs between the performance of the magnetics and the availability of the components.

5.2.1.1 Litz wire vs. planar winding

In the 10 kW composite D converter prototype, the 7 kVA DCX transformer was designed using Litz wire windings on a ferrite EE core. For the 30 kW design, the DCX transformer power rating is increased to 20 kVA, while keep the same voltages and frequency. The first question that should be addressed, in the design of the scaled-up prototype, is that whether direct scaling of the 7 kVA transformer is feasible.

The DCX module switches at 33 kHz, which presents a challenge with respect to the choice of the core material. The switching frequency can be considered high for powered iron core materials, and low for ferrite materials. In the 10 kW prototype, it was found that a ferrite core was better suited for the transformer design. However, ferrite material has lower magnetic flux density saturation level (typically $B_{sat} \leq 0.3\,\mathrm{T}$). Note that

$$\Delta B = \frac{\lambda}{2NA_c} \tag{5.1}$$

where λ is the flux-linkage, N is the number is turns and A_c is the core cross section area. To keep the transformer magnetic flux density below saturation, a sufficiently large number of turns N is required, with the result that the winding losses dominate, for the ferrite core. In consequence, direct scaling of the 7 kVA transformer to 20 kVA is not feasible, because the design ends up having very large winding copper loss. The copper loss can be reduced by simply adding more strands in the Litz wire bundle. However, this is not very effective, because similar to skin-effect of solid wire, as the Litz wire bundle grows bigger, ac current tends to crowd in the stands at the surface of the bundle. As a result, doubling the number of strands does not reduce the ac resistance by two times.

As indicated by (5.1), another approach is to choose a larger core with a larger cross section area A_c, which leads to a design with a fewer number of turns and therefore less copper resistance. However, the core volume may become prohibitively large. For example, if one directly doubles the 7 kVA transformer dimensions, the cross-section area is multiplied by four, but the core volume is multiplied by eight.

Planar magnetics is an alternative technology that uses relatively flat core shapes, with PCB traces as windings. This approach reduces the height of magnetic components, which is especially important for applications where total thickness is important. PCB traces serve as copper foil windings, which are well suited to conduct high frequency ac currents without significant skin effect. For high current, making wide PCB traces is much easier and more effective than making large Litz wire bundles. Furthermore, compared to core shapes such as E core, to achieve the same cross section area, a flat planar core ends up with less core volume.

A practical challenge in the 30 kW design is that the choice of large planar cores is very limited. One of the largest cores currently available commercially is the EPCOS ELP102 core. This size is still not sufficient for the 20 kVA transformer design. To achieve the required core size, two ELP102 cores are placed together.

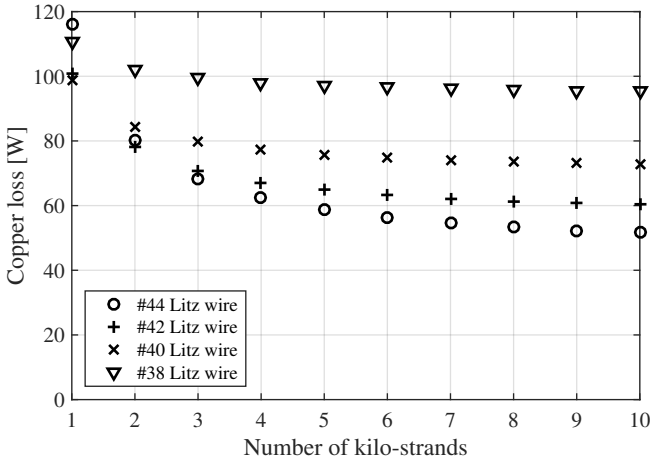
Fig. 5.8 shows a comparison of transformers designed using (a) Litz wire and (b) planar technology. The winding copper loss is compared at a typical operation point where the input voltage is 200 V, and the output power is 10 kW. The Litz wire design uses EPCOS U141/78/30 core, which has approximately the same cross-section area as two ELP102 cores, but with much larger volume, which also leads to larger core loss. It can be seen that using finer Litz wire strands or increasing the number of strands are not very effective, while the planar transformer design ends up with a much smaller loss.

5.2.1.2 Planar transformer design

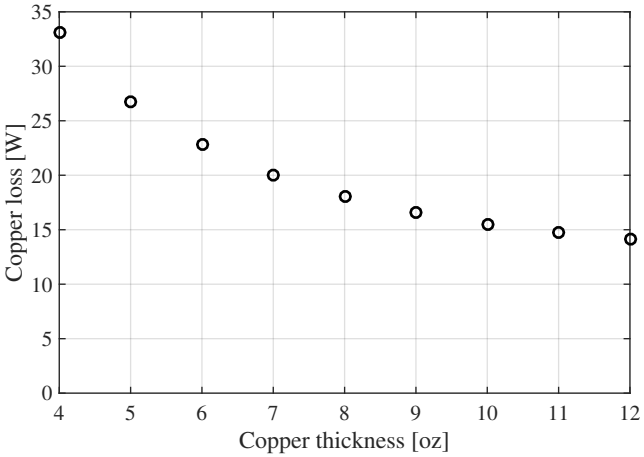
Fig. 5.9 shows the modeled transformer and inductor loss at different copper thicknesses. The transformer has 6 turns on the primary and 12 turns on the secondary. To interleave windings, the

Figure 5.8: Comparison of 20 kVA DCX transformer designs: (a) Litz wire winding on EPCOS U141/78/30 core (core volume: 255 cm^3) vs. (b) planar winding on two EPCOS ELP102 core (total core volume 136 cm^3), both at 33 kHz switching frequency, and keep worst-case $B_{max} = 0.3$ T.

(a)



(b)



primary winding has one turn per layer, while the secondary winding has two turns per layer. It can be seen that the tank inductor copper loss is minimized with 9 oz copper. Transformer copper loss is minimized with thicker copper, but copper thicker than 9 oz does not show significant loss reduction. Furthermore, due to PCB manufacturing limitations, a PCB with copper thicker than 9 oz is difficult to fabricate. Therefore, a 9 oz PCB is used for both the DCX transformer and the DCX tank inductor. The distance between copper layers is maximized to minimize inter-winding capacitance. The total board thickness is approximately 7 mm, which is at the limit of the capability of our selected PCB manufacturer.

Figure 5.9: DCX magnetics loss versus copper thickness at typical 200 V input and 10 kW output power. The scale factor to obtain the copper thickness in metric units is 0.0347 mm/oz.

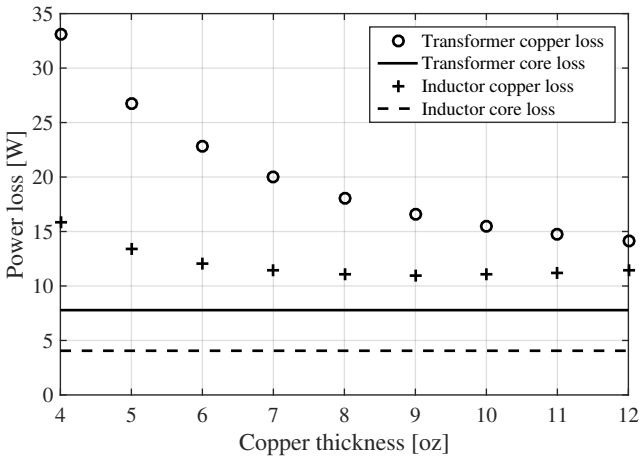


Figure 5.10: Magnetic flux density plot of the 2-D Finite Element Analysis (FEA) on the designed planar DCX transformer

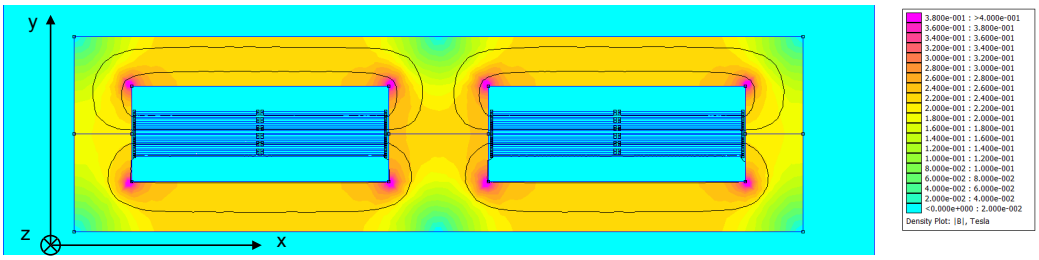
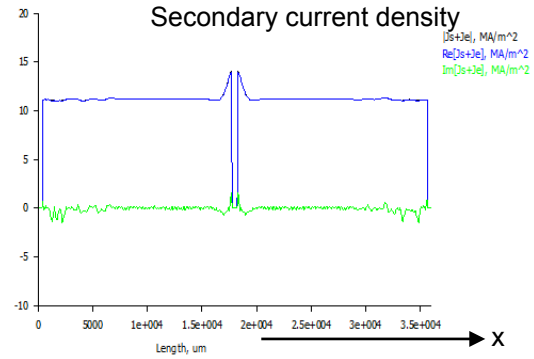


Figure 5.10 & 5.11 show the 2-D finite element analysis performed on the planar transformer cross section. Due to the interleaved structure, the proximity effects are minimized. The current distribution along x-axis direction is slightly uneven, due to the gap between the two secondary windings, which is not modeled by the Dowell's one-dimensional model. However, the difference is small. In terms of ac resistance, the difference between calculation from Dowell's equation and FEA simulation is within 4%. Therefore, the magnetics loss model still has sufficient accuracy.

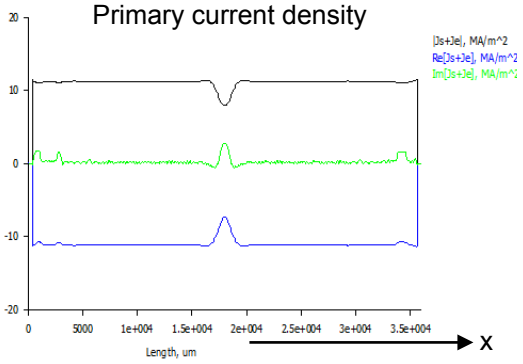
The detailed DCX planar transformer design is summarized in Table 5.6, and the tank inductor design is given in Table 5.7. Notice that to reduce DCX common mode currents, the tank inductor winding actually splits into two (one per leg of the primary transformer winding), as described in following.

Figure 5.11: Current density plots of the 2-D Finite Element Analysis (FEA) on the designed planar DCX transformer: (a) secondary winding current density along x-axis; (b) primary winding current density along x-axis; (c) both primary and secondary winding current density along y-axis.

(a)



(b)



(c)

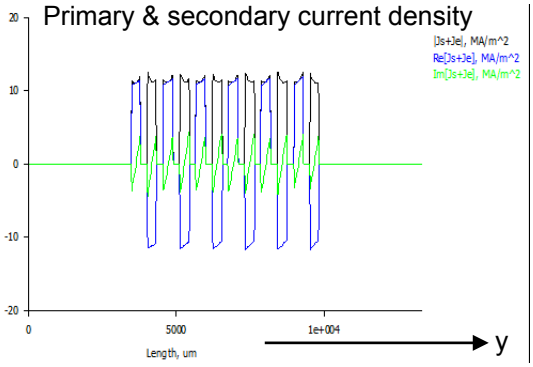


Table 5.6: DCX planar transformer parameters

Core Material	EPCOS N97
Core Shape	ELP102 × 2
Winding	12-layer 9-oz PCB
Turns ratio	6:12
Magnetizing inductance	264 µH from primary
Leakage inductance	70 nH from primary
Inter-winding capacitance	18 nF

Table 5.7: DCX planar tank inductor parameters

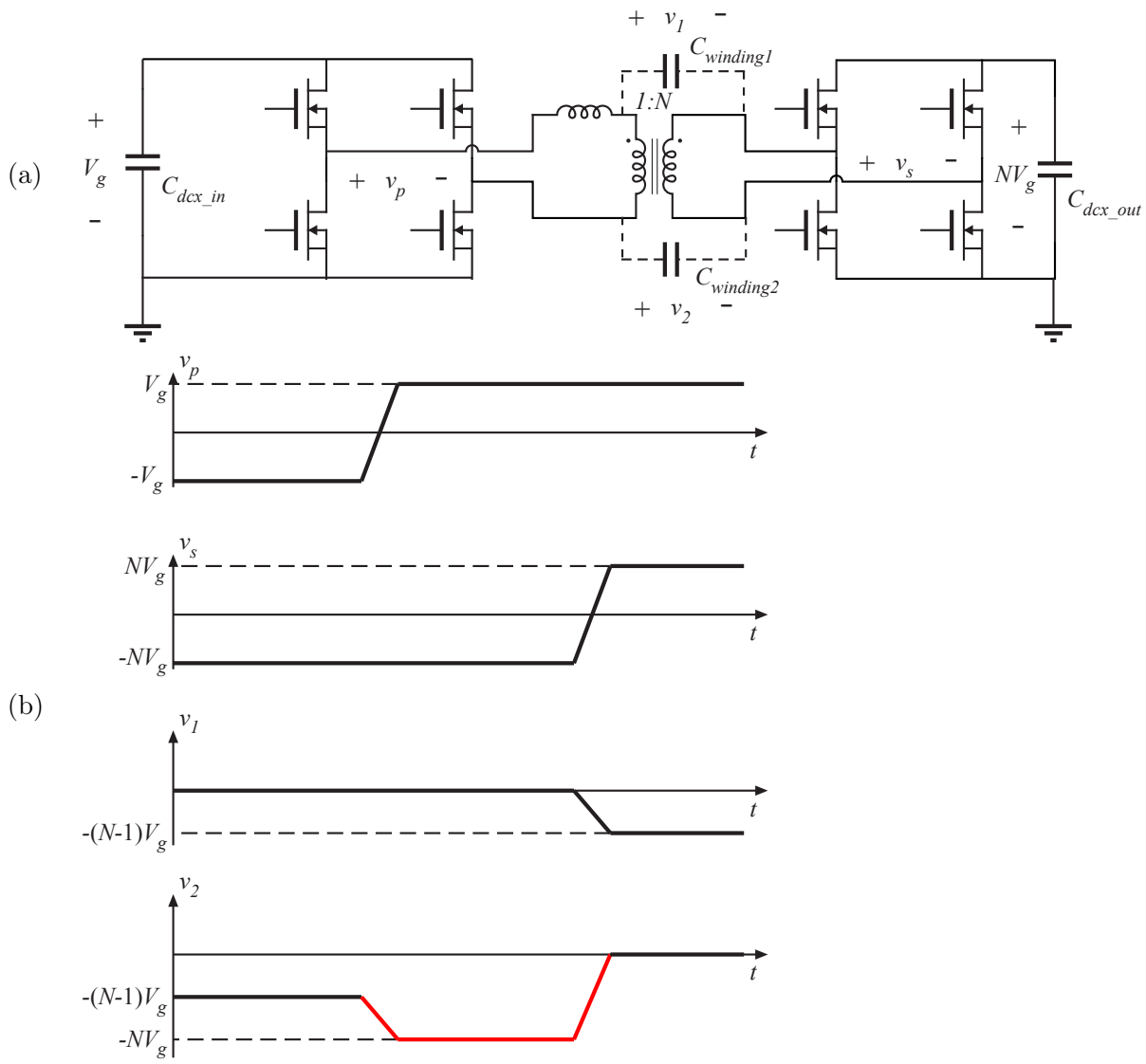
Core Material	EPCOS N97
Core Shape	ELP102 × 2
Winding	2-layer 9-oz PCB
Number of turns	2
Inductance	2.7 µH

5.2.1.3 DCX common-mode current reduction

Compared to a conventional transformer, the planar transformer has significantly smaller leakage inductance, but much larger inter-winding capacitance. For the existing design, an inter-winding capacitance of 18 nF is measured.

The large inter-winding capacitance may lead to transformer self-resonance, as well as increased common-mode current, which is explained with the aid of Fig. 5.12. There is a phase shift between DCX primary side and secondary side switching. During this phase shift, the voltage difference between primary and secondary is applied to the tank inductor. However, because the tank inductor is inserted in only one side of the primary winding, the voltage waveforms applied to the transformer primary terminals are not symmetric, as illustrated in Fig. 5.12(b). The current through the winding capacitance is $i_C = C\mathrm{d}v_C/\mathrm{d}t$, which is proportional to the rate of voltage changes applied to the capacitor. According to the parasitic capacitor voltage waveforms, the currents flowing into and out of the transformer are not symmetric. This results in common-mode current flowing through the transformer. Theoretically one expects this common-mode current to circulate within

Figure 5.12: (a) Schematic of DCX with asymmetrical tank inductor. (b) Transformer inter-winding capacitor voltage waveforms.



the DCX power stage only. In practice, however, it is difficult to identify and characterize the return path for the common-mode current. Spurious system latch ups or test equipment shut downs were attributed to the common-mode currents affecting the system controller or controllers in the test equipment.

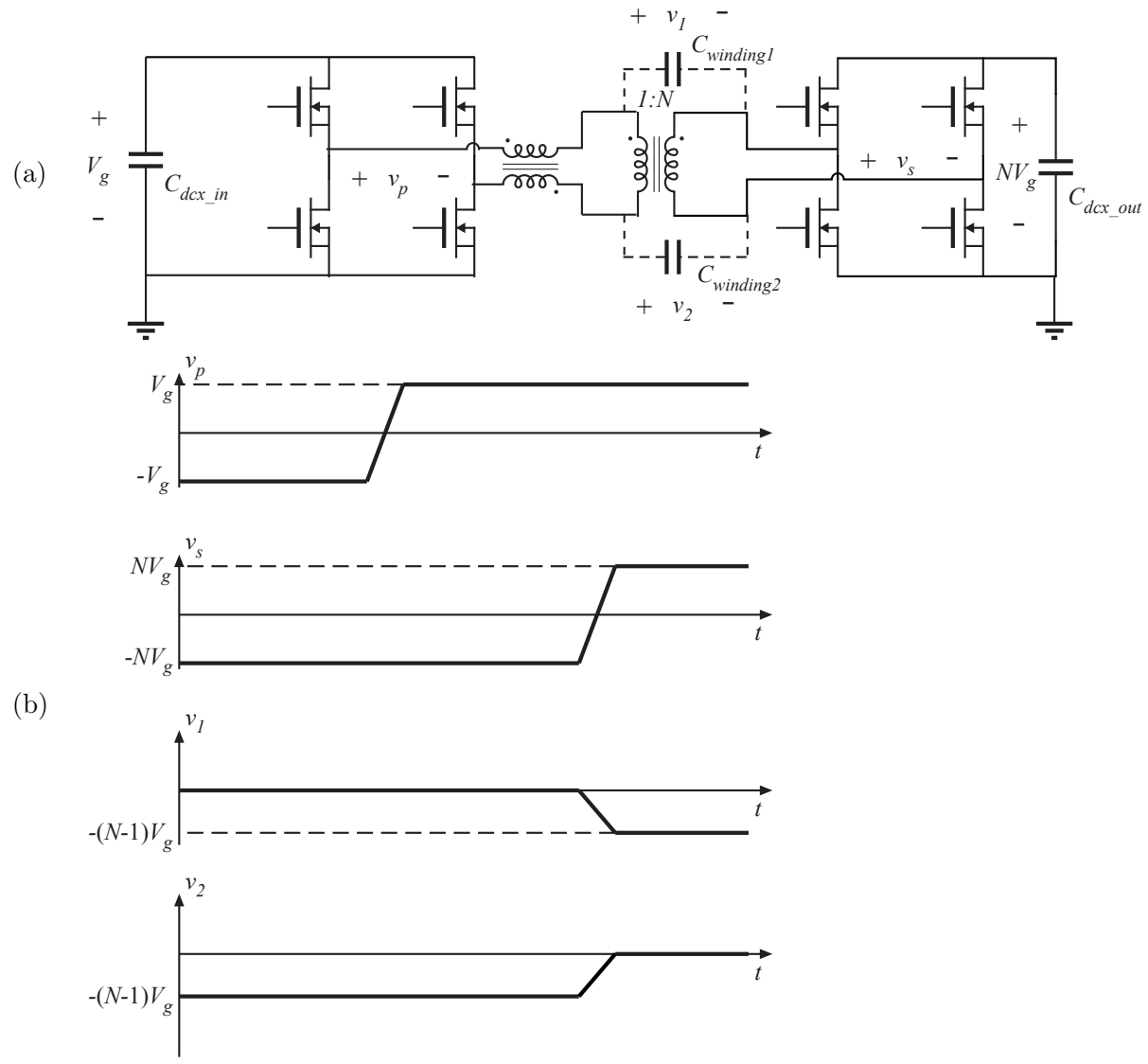


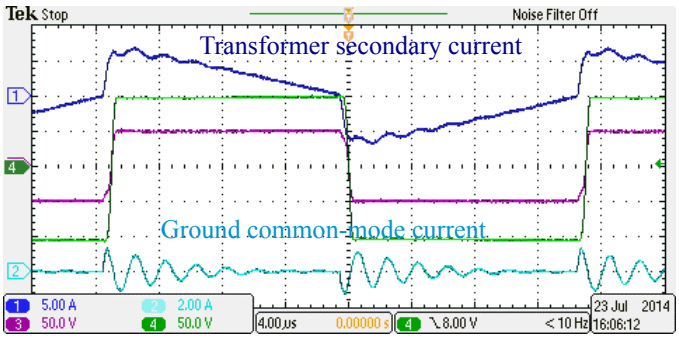
Figure 5.13: A symmetrical tank inductor: (a) DCX schematic; (b) transformer inter-winding capacitor voltage waveform.

To mitigate this type of undesirable interference, several approaches were considered, including common-mode filters, or including an additional primary-to-secondary side capacitor to confine the

common-mode current loop to the DCX module power stage. The most effective approach found was to minimize generation of the common-mode current by rearranging the tank inductor as shown in Fig. 5.13. Simply splitting the tank inductor into two inductors, each with half inductance and placing the two tank inductors each in series with a transformer lead makes the tank and transformer circuit symmetric, thus significantly reducing the common-mode current. With this modification, there is still current flowing through the transformer parasitic capacitances, but the current becomes symmetric. As a result, there is only differential mode current confined to the DCX power stage, instead of common-mode current with an uncertain return path. In practice, the two tank inductors can be coupled to minimize the core volume, as shown in Fig. 5.13.

Figure 5.14: Experimental DCX waveforms with (a) asymmetrical tank inductor as shown in Fig. 5.12; (b) symmetrical tank inductor as shown in Fig. 5.13

(a)



(b)

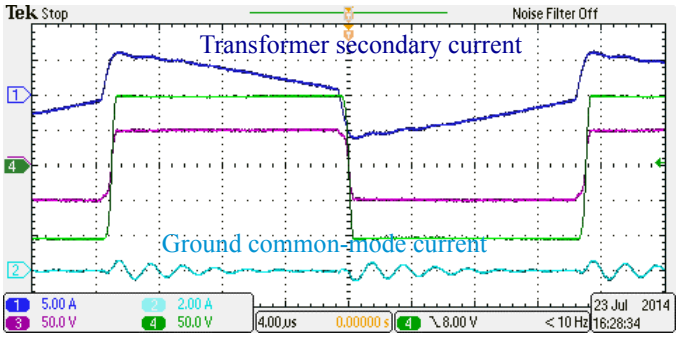


Fig. 5.14 shows the experimental waveforms recorded with (a) asymmetrical tank inductor as shown in Fig. 5.12 and (b) symmetrical tank inductor as shown in Fig. 5.13. It can be seen that with the symmetric tank inductor, the ground common-mode current magnitude is much reduced,

Table 5.8: Boost Inductor Design

Core Material	Metglas Powerlite
Core Shape	AMCC016A
Winding	#38 Litz wire, 1000 strands × 2
Inductance	17 µH
Turns	11
Air gap	2.1 mm

Table 5.9: Buck inductor Design

Core Material	Metglas Powerlite
Core Shape	AMCC010
Winding	#36 Litz wire, 500 strands × 2
Inductance	32 µH
Turns	16
Air gap	1.8 mm

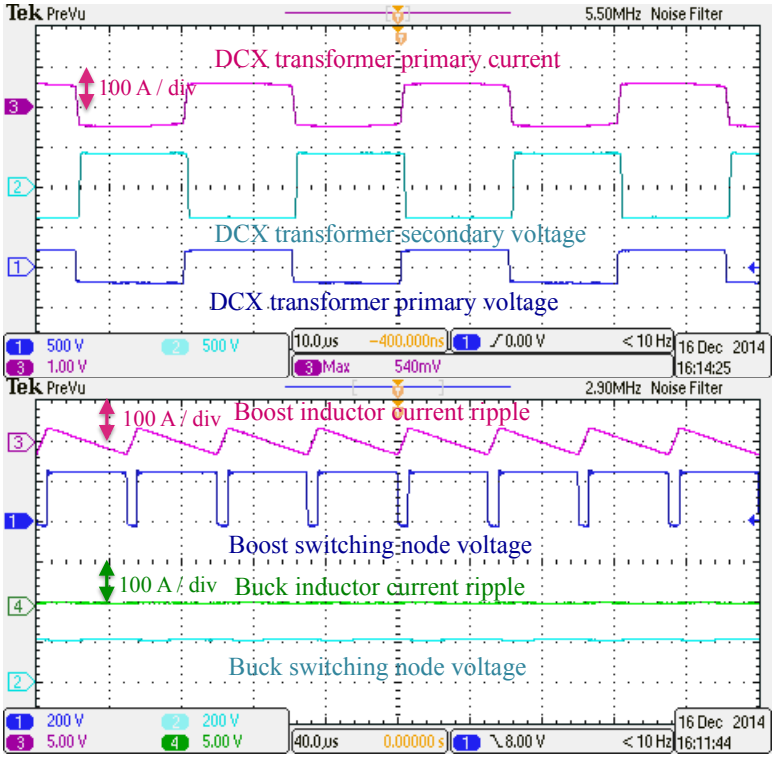
and the transformer self-resonance is much reduced as well. With the symmetric tank inductor, spurious controller latch-ups have been completely eliminated.

5.2.1.4 Inductor design

In the 30 kW prototype, the buck and boost module inductors are re-designed as well. To accommodate the scaled current level on the winding, amorphous metal (such as Metglas) is chosen as the core material. With higher magnetic flux density saturation level ($B_{max} \geq 1.5\,\mathrm{T}$), the winding number of turns is greatly reduced, which results in much reduced copper loss.

Comparing with the 10 kW prototype, where the buck and boost module utilize the same inductor design, the 30 kW prototype optimizes the buck and boost module inductor separately. Table 5.8 & 5.9 documents the boost and buck module inductor designs respectively.

Figure 5.15: 30 kW prototype waveforms in DCX + boost mode, with 15 kW output power.

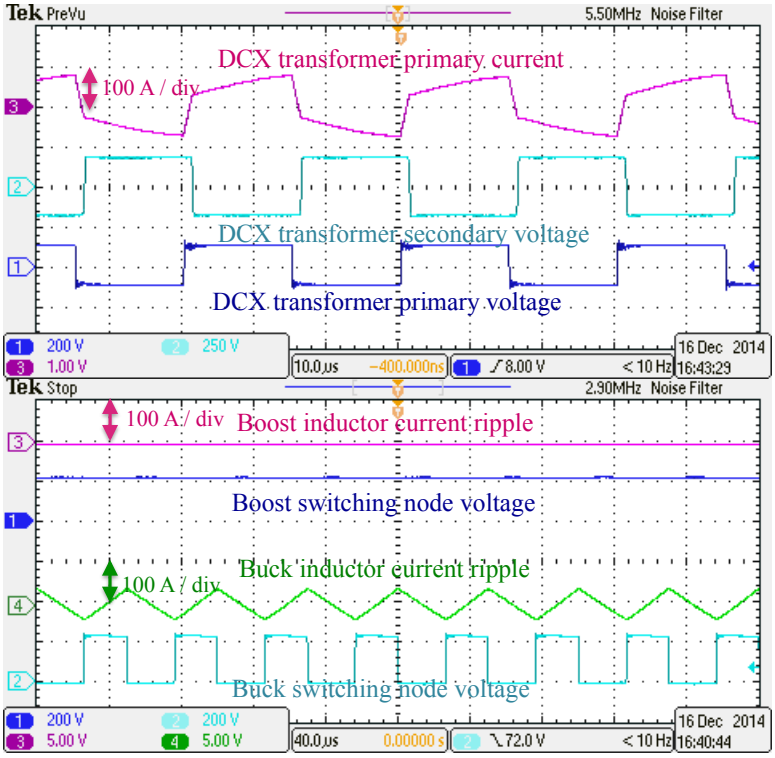


5.2.2 Measurement results

Fig. 5.15 shows operating waveforms of the 30 kW composite converter D prototype system at medium power level. The system operates in the DCX + boost mode. The top graph shows the DCX operating waveforms. It can be seen that both primary and secondary sides exhibit ZVS transitions at this point. The DCX transformer current waveform has a trapezoidal shape, with minimized RMS current and optimized efficiency. The bottom graph shows the buck and the boost module operating waveforms. Because the current rating at this point exceeds the available current probe rating, only the ac components of inductor currents are measured, through current transformers. The boost module switches with small duty cycle, while the buck module is in the pass-through mode.

Figs. 5.16 and 5.17 show the waveforms at light load and full load, respectively. In Fig. 5.16,

Figure 5.16: 30 kW system waveforms in DCX + buck mode, with 10 kW output power.



the system is in the DCX + buck mode, with the boost module in pass-through, while in Fig. 5.17 the system is in the DCX + boost mode, with the buck module in pass-through.

Fig. 5.18 shows the measured system efficiency in the DCX + boost mode, over a range of output power, at fixed 210 V input and 650 V output.

Fig. 5.19 shows the measured efficiency at fixed 15 kW (50%) output power, in the output voltage versus input voltage plane, demonstrating efficiency performance in different operating modes. At most of the operating points, the measured efficiency exceeds 97%. The efficiency measurement results are consistent with the model predictions shown in Fig. 5.26.

The system has also been tested under reverse power flow conditions. To measure reverse power flow operation, the power supply is connected at the DC bus port, and a load resistor is connected at the battery port. Due to the limitations of the laboratory power supply, the bus voltage can only be applied up to 500 V. Table 5.10 summarizes the measured efficiency for both

Figure 5.17: 30 kW system waveforms in DCX + boost mode, with 30 kW output power.

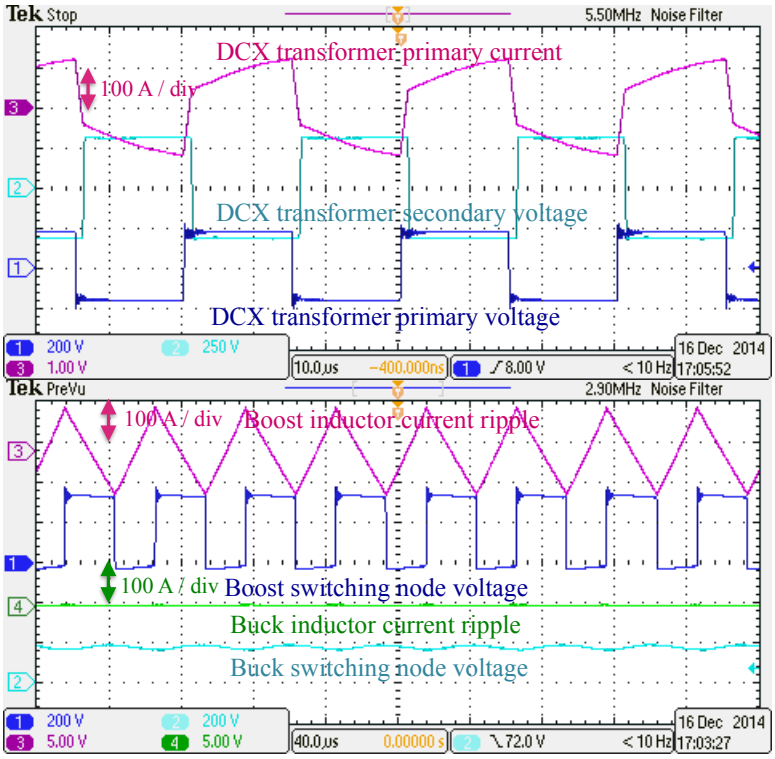


Figure 5.18: 30 kW system measured efficiency as a function of output power, at fixed $V_{in} = 210$ V, $V_{out} = 650$ V in the DCX + boost mode

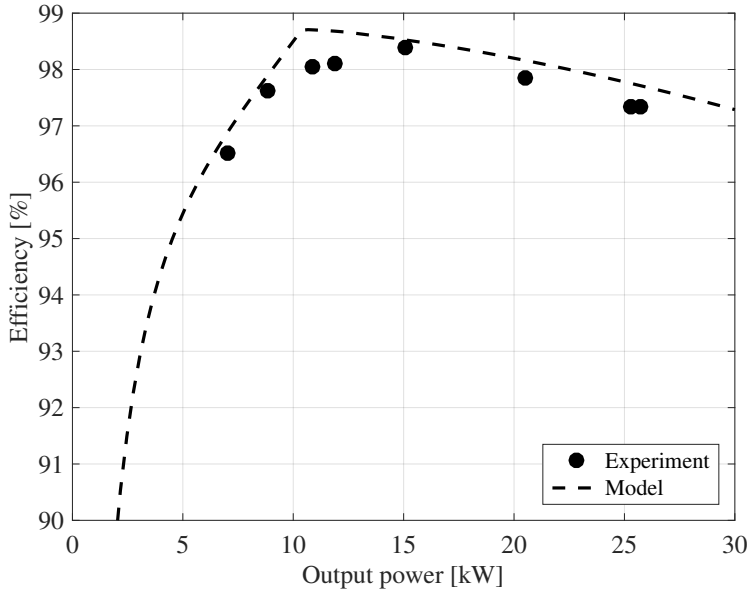


Figure 5.19: 30 kW module measured efficiency at different input / output voltages in different mode, with fixed 15 kW output power

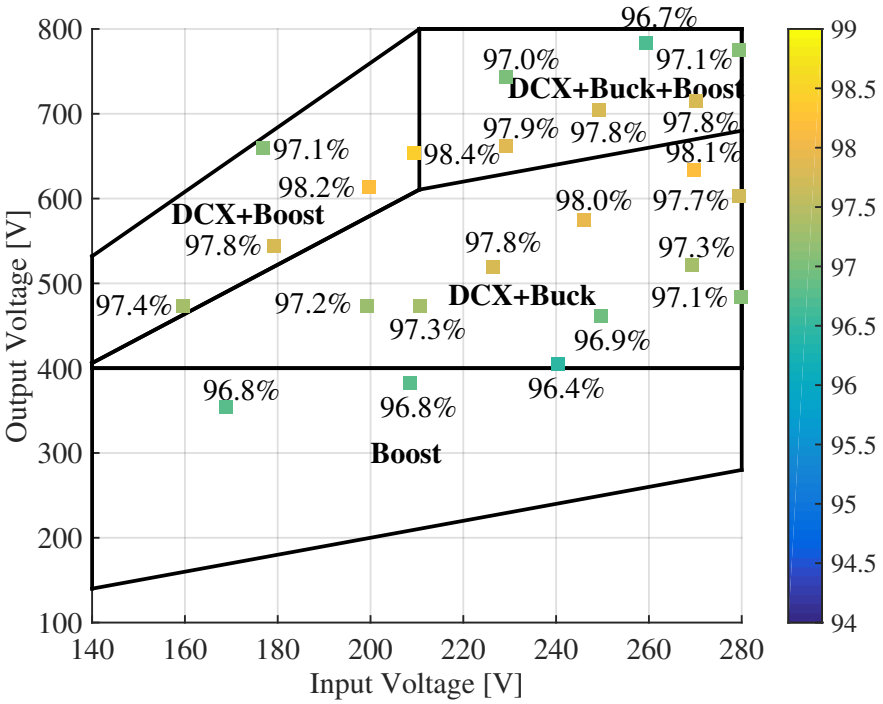


Table 5.10: Measured 30 kW system efficiency for forward and reverse power flow

Power flow	$V_{battery}$ [V]	V_{bus} [V]	P [kW]	Efficiency
forward	199.9	501.9	4.8	97.2%
reverse	200.4	500.6	-5.3	97.2%
forward	199.6	472.4	10	98.0%
reverse	190.5	500.6	-10	97.9%

forward and reverse power flow at 200 V battery voltage and 500 V bus voltage. It can be seen that the measured efficiency for reverse power flow is the same or very close to the measured efficiency for forward power flow.

5.2.3 30 kW prototype second revision

The 30 kW prototype is improved with a second revision. In this revision, the battery input voltage is assumed to be 250 V typical. Therefore the transformer is re-designed with 8:12 turns ratio. The design parameters of the magnetics are summarized in Table 5.11.

Table 5.11: Magnetics design summary of 30 kW prototype second revision

Buck inductor	Inductance	64 µH
	Core material	Powerlite Metglas
	Core shape	AMCC50
	Number of turns	36
	Wire	AWG36 Litz wire, 1000 strands
Boost inductor	Inductance	80 µH
	Core material	Powerlite Metglas
	Core shape	AMCC50
	Number of turns	40
	Wire	AWG40 Litz wire, 1500 strands
Transformer	Core material	3C95 ferrite
	Core shape	Two EILP102
	Number of turns	8:12
	PCB stacking	9-oz 14-layer
Tank inductor	Inductance	2.7 µH
	Core material	N87 ferrite
	Core shape	EILP64
	Number of turns	2
	PCB stacking	9-oz 2-layer

The three converter modules in the composite D converter are integrated into one single power stage printed circuit board. The PCB has 2-layer 13-ounce heavy copper to handle around 200 A peak current. Because of the heavy copper clearance rule which is determined by the PCB manufacturer, it is impossible to mount small surface-mount components onto the heavy copper

power stage board. Therefore, a second 4-layer 2-oz driver PCB is designed to accommodate all the driver and sensor circuitry. Between two boards, a 1/32 inch fiber glass, which is cut by water jet, is used as a spacer between the power stage PCB and the driver PCB, for voltage isolation. Fig. 5.20 shows the CAD illustration of the physical assembly of the system. The photo of the fabricated prototype is shown in Fig. 5.21.

Figure 5.20: 30 kW prototype second revision PCB stacking

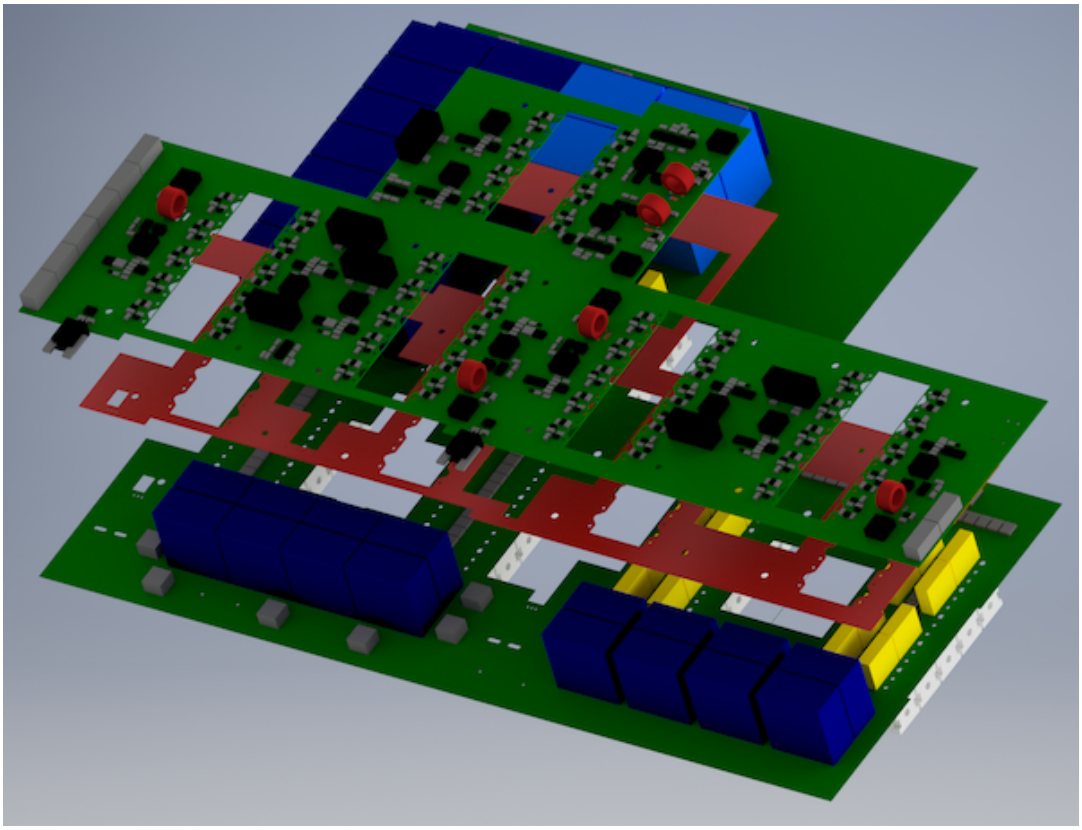
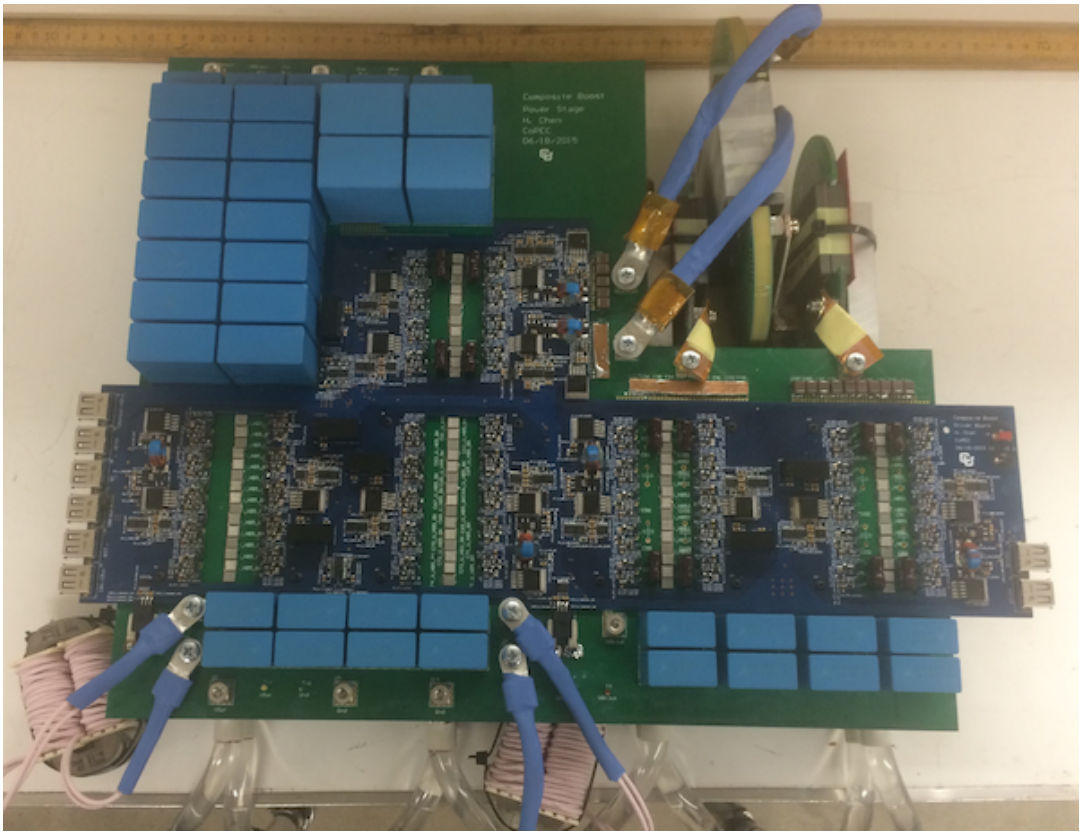


Fig. 5.22 shows the measured efficiency of this prototype, at fixed 250 V input and 650 V output. The converter reduces the power loss by half at medium to heavy load, in comparison with the conventional boost converter. With the efficiency-enhanced DAB control, the efficiency at light load is significantly improved. The converter efficiency stays above 97% for output power greater than 1 kW. Fig. 5.23 shows the measured power loss of this prototype. With the efficiency-enhanced DAB control, the power loss almost decreases linearly as the output power decreases,

Figure 5.21: 30 kW prototype second revision photo



which is preferred for the traction powertrain system, where most of the time the system operates at medium to light load conditions.

The performance of the 30 kW prototype in the actual driving conditions is predicted with standard driving cycles. It is assumed that the battery pack stays at a typical voltage of 250 V. Fig. 5.24 plots the energy loss of the three converter modules inside composite converter D, with different driving profiles. In Fig. 5.24(a), the DCX module is operated in open loop. Under all three driving profiles, the DCX energy loss is dominated. This is because of the switching loss of DCX module at light load conditions, as discussed in section 4.4, and this problem is solved by the efficiency-enhanced DAB control. With the proposed control algorithms, the predicted energy loss distribution is plotted in Fig. 5.24(b), where the energy loss is more evenly distributed. Under the urban driving condition (UDDS), because the average speed is low, most of the time the system

Figure 5.22: Measured efficiency of the 30 kW prototype, with efficiency-enhanced DAB control enabled, at fixed 250 V input and 650 V output.

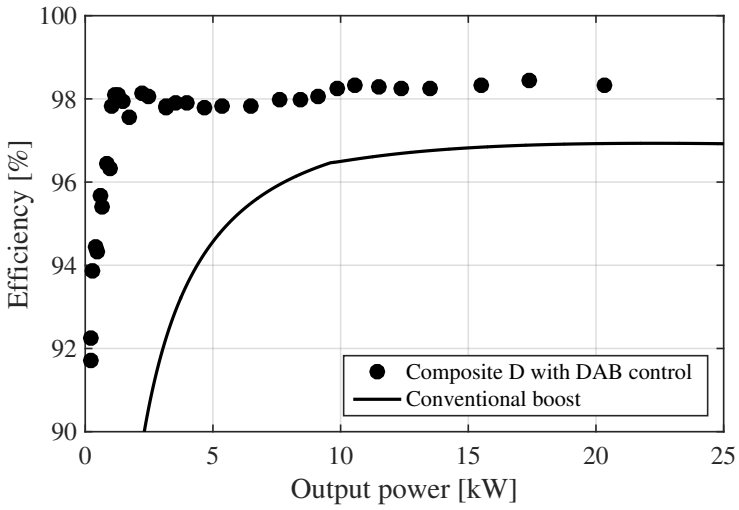


Figure 5.23: Measured power loss of the 30 kW prototype, with efficiency-enhanced DAB control enabled, at fixed 250 V input and 650 V output.

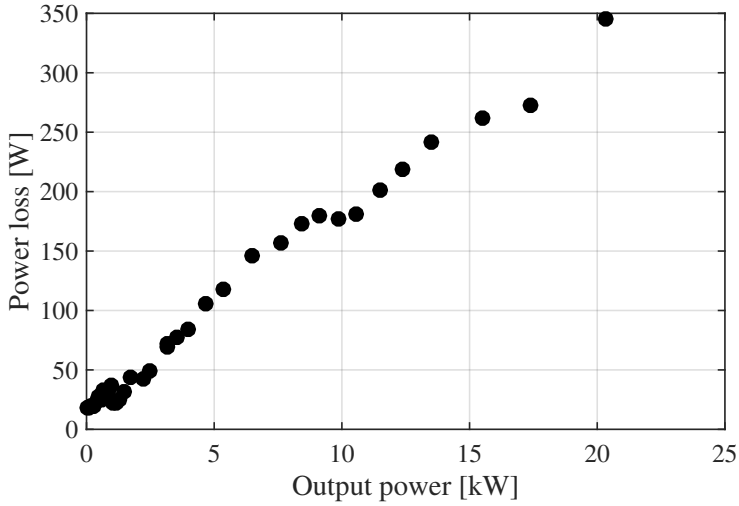
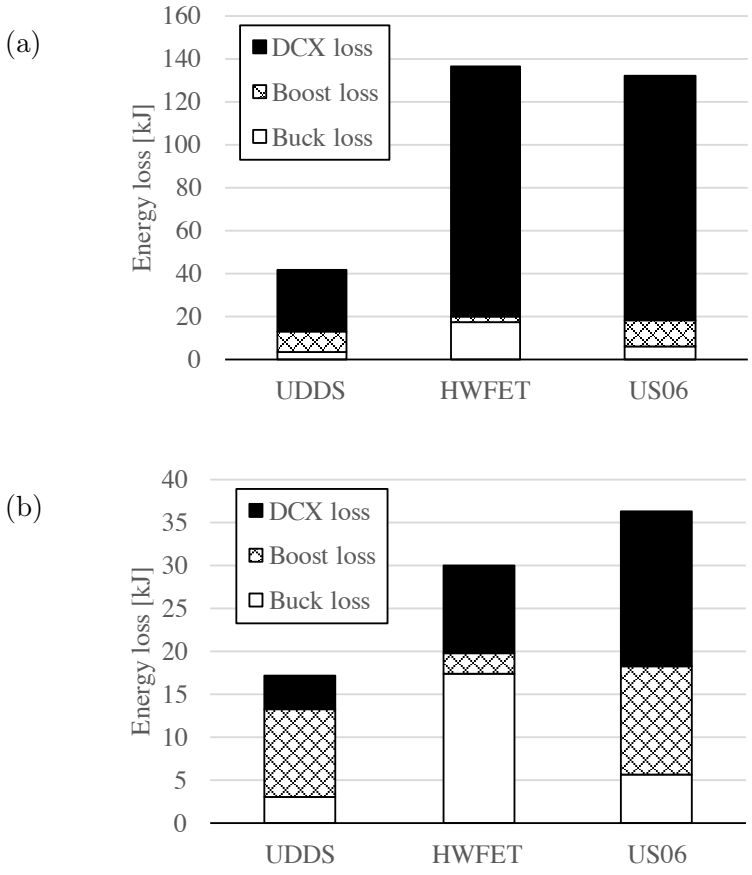


Figure 5.24: Predicted composite converter energy loss distribution under different driving profiles (with 250 V battery voltage): (a) with DCX module operated in open loop; (b) with efficiency-enhanced DAB control algorithm enabled on DCX module.



operates in boost-only mode, and the boost module loss is dominated. With the highway driving profile (HWFET), with 48 mph average speed, most of the time the system operates in DCX + buck mode, and thus the buck module loss is dominated. In the aggressive driving cycle (US06), because of high speed (85 mph peak), the system spends significant portion of time in the DCX + boost mode, and the DCX module loss is dominated.

The converter quality factor Q as well as the corresponding average efficiency η of the prototype is predicted in Table 5.12, with different driving profiles. The converter quality factor Q here is defined as:

$$Q = \frac{\int |P_{out}| \, \mathrm{d}t}{P_{loss} \, \mathrm{d}t}, \tag{5.2}$$

Table 5.12: Predicted converter quality factor Q and average efficiency η of 30 kW composite converter prototype under different driving profiles (with 250 V battery voltage).

		UDDS	HWFET	US06
Conventional boost	Q	53.80	17.20	22.17
	η	98.18%	94.51%	95.68%
Composite D with open loop DCX	Q	61.31	16.97	26.09
	η	98.40%	94.44%	96.31%
Composite D with efficiency-enhanced DAB control	Q	146.83	76.94	95.14
	η	99.32%	98.72%	98.96%

and the average efficiency η is calculated as

$$\eta = \frac{Q}{Q+1}. \tag{5.3}$$

Because of the DCX switching loss at light load conditions, the loss reduction provided by composite converter with open-loop DCX module is limited. However, after the switching loss problem being fixed by the efficiency-enhanced DAB control, the composite D converter offers two to four times loss reduction, under all three different driving conditions.

5.3 60 kW silicon-device-based prototype

In this section, the idea of composite D converter is further extended to a 60 kW prototype. This power level is suitable for mid-sized PHEV or BEV powertrain application.

For the 60 kW experimental prototype, two 30 kW composite D converters are interleaved. Therefore, it also demonstrates the scalability of the composite converter approach. As illustrated in Fig. 5.25, each of the converter modules is realized using two half-power parallel-connected modules. The controller ensures that the module currents are balanced, and additionally it phase-shifts the module gate drive signals to minimize the rms capacitor currents. Hence, the requirements of the system film capacitors are further reduced.

Fig. 5.26 plots the modeled 60 kW composite converter D system efficiency at fixed 30 kW output power, at different input/output voltages and across different modes of operation. For most

Figure 5.25: 60 kW module system configuration, using parallel phase-shifted modules

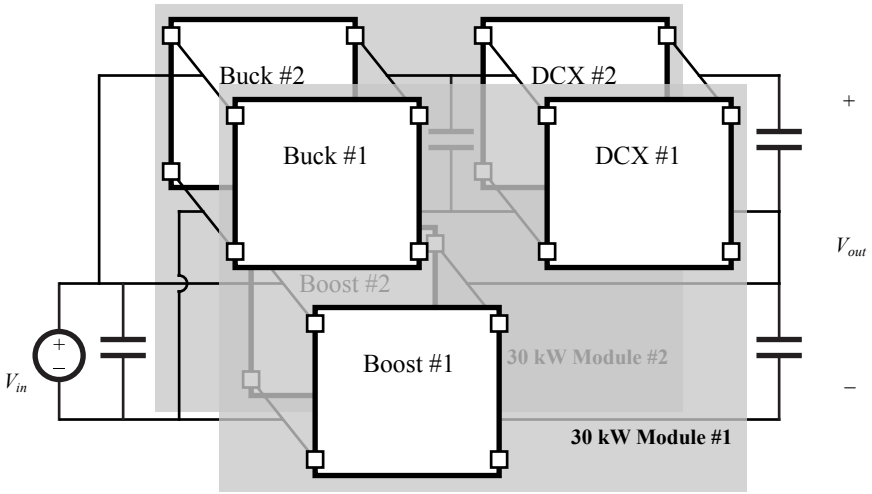
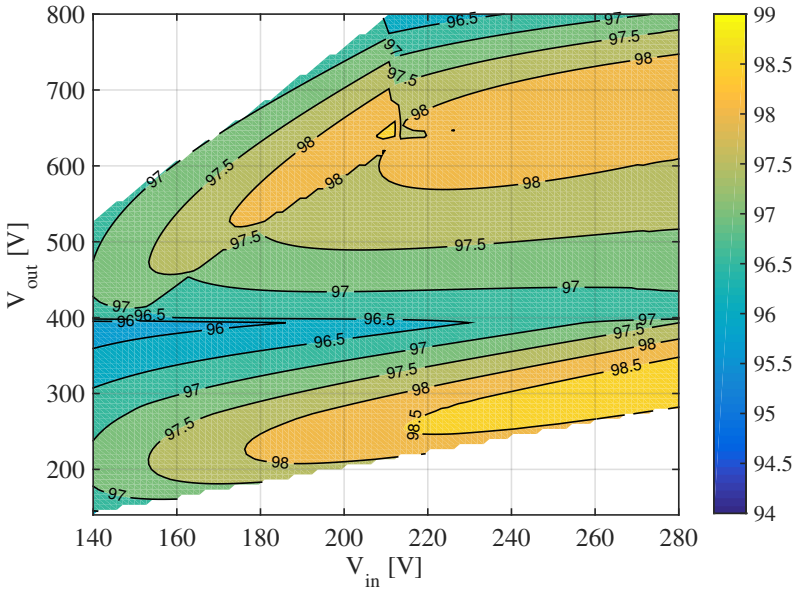


Figure 5.26: Modeled 60 kW system efficiency at fixed 30 kW output power, with different input / output voltages

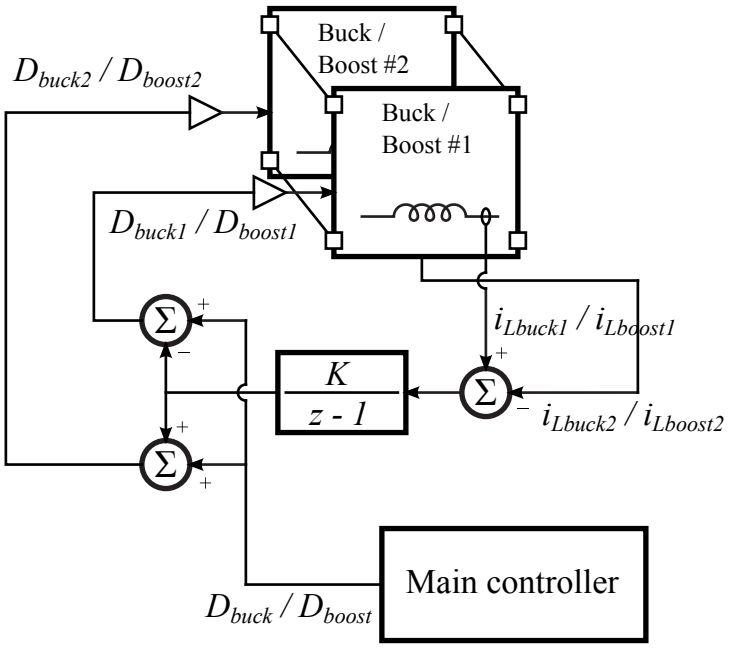


of the operating region, the system efficiency is maintained above 97%, except for a relatively narrow region close to the boundary between boost-only and DCX + buck modes. The system efficiency is above 98% for output voltages between 600 V and 700 V, with input voltages greater than 200 V.

5.3.1 Current balancing control

Since the 60-kW system is composed of modules arranged in parallel, as shown in Fig. 5.25, current sharing among the paralleled modules must be addressed. Due to component mismatches, if the same duty cycle is applied to two modules operating in parallel, the modules may not share the current equally. This may lead to reduced system efficiency, or even system failure if the current in one module exceeds its safe current rating. To address this problem, a simple current balancing control approach is developed for the 60-kW prototype.

Figure 5.27: Block diagram of the current balancing control algorithm



A block diagram of the current sharing controller around two paralleled modules (buck or boost) is shown in Fig. 5.27. The same approach applies to both the two paralleled buck modules, and the two paralleled boost modules in the completed phase 3 system shown in Fig. 5.25. Inductor

currents of the two modules are sensed and compared. The difference is fed into a discrete-time integrator ($K/(z-1)$ block). The output of the integrator generates an offset correction between the duty cycle commands for the two paralleled modules. For example, if $I_{Lbuck1} > I_{Lbuck2}$, the integrator increases its output. As result, the duty cycle D_{buck1} is reduced, while the duty cycle D_{buck2} is increased, to counteract the error in current sharing between the two modules. Because of the integral action in the current-sharing control loop, the steady-state error between the two sensed module currents is forced to zero, ideally resulting in perfect current balancing, i.e. equal steady-state current sharing between the two modules. In practice, some current mismatches may still occur due to mismatches in current sensing, current sampling and A/D conversion. To make sure this additional current sharing control does not affect the existing control algorithms, the speed of the current balancing loop, which is set by the integrator gain K, is kept slow compared to the main control loop.

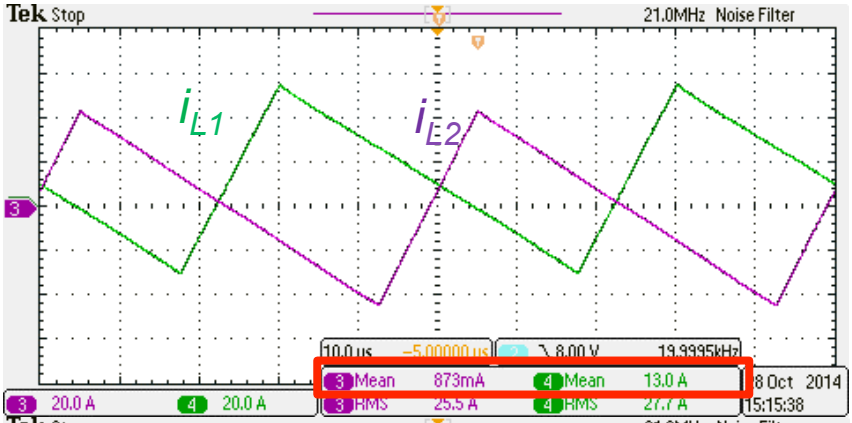
It should be noted that current balancing is necessary even in open loop operation of the 60-kW system with paralleled modules, i.e., with the main control duty cycle (D_{buck} or D_{boost}) set independently to a fixed value, not by the system controller. The results presented in Section 5.3.2 are in fact obtained with the current balancing control applied in open-loop operation of the system. In the rest of this section, additional experimental verification of the effectiveness of the developed current balancing approach is provided.

Fig. 5.28 illustrates effects of the current balancing algorithm. The waveforms in Fig. 5.28(a) are obtained when the same duty cycle $D_{boost1} = D_{boost2} = D_{boost}$ is applied to two interleaved boost modules operating in parallel. The two modules are operated in an interleaved manner, phase shifted by 180°. Because of a small inductance mismatch between the two modules, the average inductor currents in the two modules are not well balanced. One module average current is significantly larger than the other. This can lead to reduced efficiency and increased component current stresses.

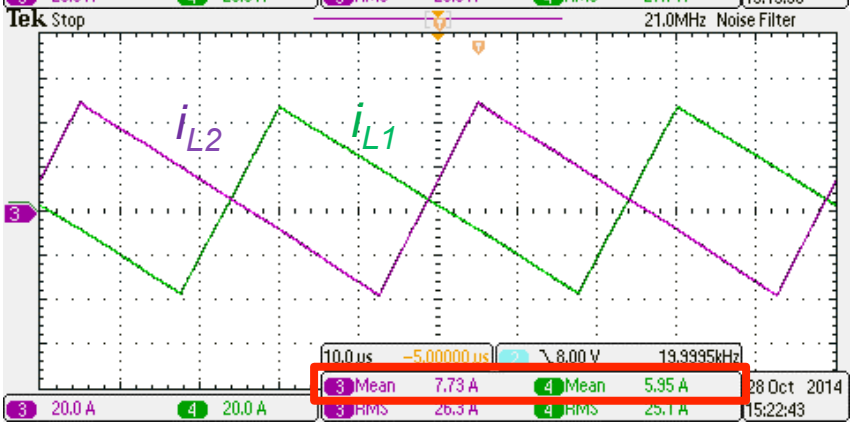
Fig. 5.28(b) shows the effect of current balancing. The current balancing algorithm is applied, and the module currents are balanced much better. The small remaining mismatch between the

Figure 5.28: Two interleaved boost converters operating at $V_{in} = 250\,\text{V}$, $V_{out} = 330\,\text{V}$, with slightly mismatched inductances: (a) without the current balancing algorithm; (b) after applying the current balancing algorithm.

(a)



(b)



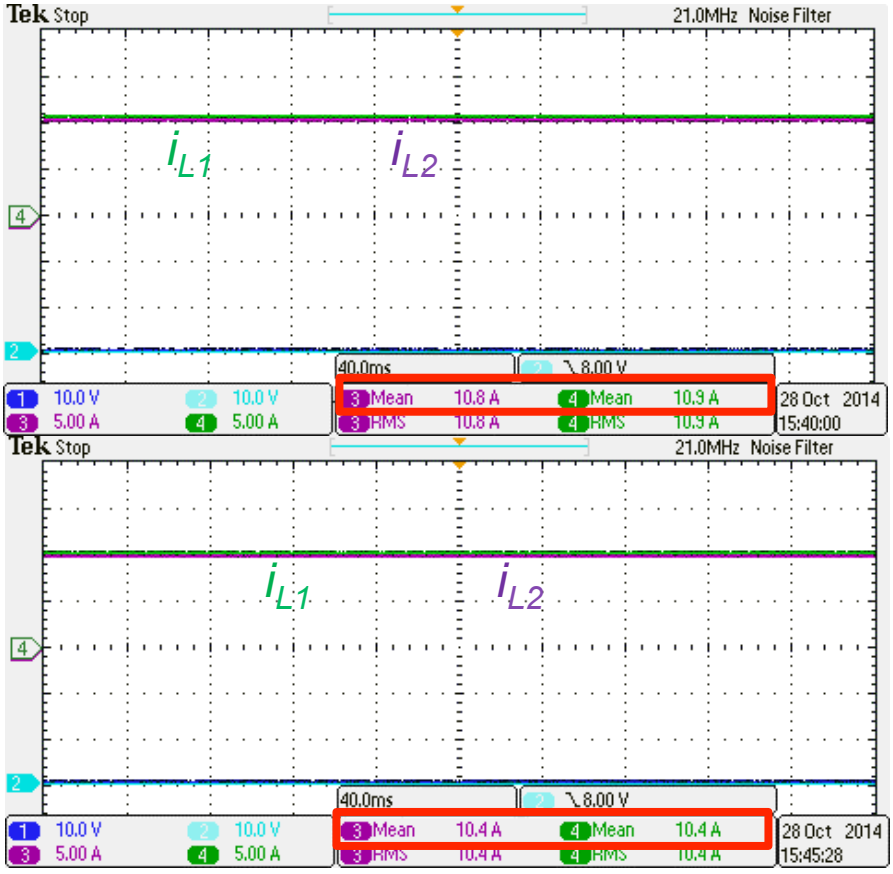
two averaged inductor currents is a result of mismatches in current probes used to perform the measurements, as well as any current sensing and sampling mismatches.

It should be noted that the developed current balancing algorithm works only if the two paralleled modules are actively controlled, i.e., if the two modules are switching and not in pass-through mode. If the two modules are in the pass-through mode, current balancing depends on DC matching and DC characteristics of the devices in the current path through each of the two modules. The 60-kW prototype utilizes MOSFETs as power switches, which are majority carrier devices, with on-resistance that exhibits a positive temperature coefficient. Similarly, the dc resistance of a copper-wire inductor also has a positive temperature coefficient. Because of the inherent negative-feedback effect due to positive temperature coefficients, it is expected that current balancing occurs naturally

Figure 5.29: Two boost converters operating in parallel in pass-through mode, with 2.8 kW output power: (a) initial inductor currents; (b) inductor currents after 5 minutes of operation.

(a)

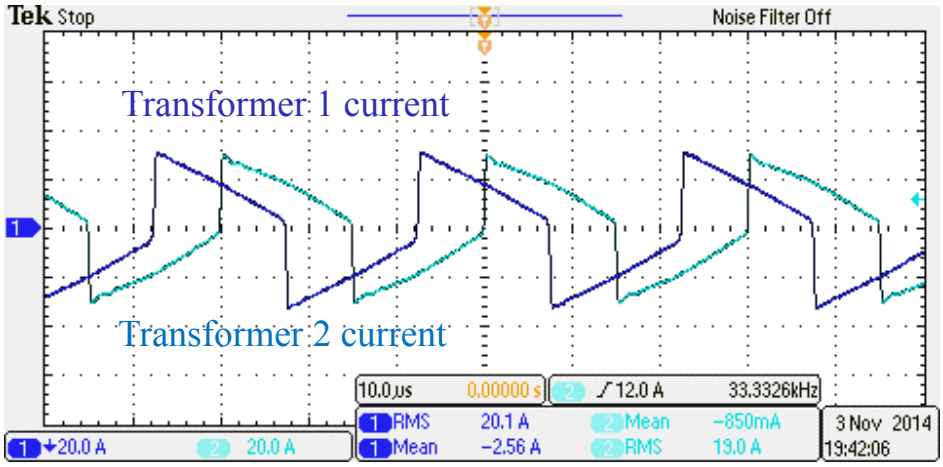
(b)



in paralleled modules operating in the pass-through mode. This has been confirmed in experiments. Fig. 5.29 shows DC inductor currents in two paralleled boost converters operating in pass-through mode: (a) at the start of operation immediately after turn-on, and (b) after 5 minutes, at elevated temperature. It can be observed that the module DC currents are essentially the same, i.e., remain nearly perfectly balanced at all times.

It remains to consider current balancing in the two DCX modules operating in parallel. It has been found that effective current balancing in the paralleled DCX modules occurs naturally, without the need for any additional active control. This is consistent with the published work on natural current balancing for soft-switching converters such as DCX, which exhibit quasi-square-waveform converters. As an example, Fig. 5.30 shows how the currents between two DCX modules are well

Figure 5.30: Two interleaved DCXs naturally balance their transformer current.



balanced naturally. In the waveforms of Fig. 5.30 one may also note that the two DCX modules are properly interleaved with a phase shift of 90° instead of 180°. The diode bridge rectification on the DCX secondary side then results in the lowest output current ripple for this 90° interleaving.

5.3.2 60 kW system measurement results

This section documents steady-state operation and efficiency performance of the full 60 kW composite converter D system. The system consists of two interleaved boost modules, two interleaved buck modules, and two interleaved DCX modules, as shown in Fig. 5.25. The system is tested in open loop. However, the current balancing algorithm described in Section 5.3.1 is employed to ensure current balancing between the interleaved modules.

Fig. 5.31 contains a plot of the measured efficiency as a function of output power, at fixed 210 V input and 650 V output, in the DCX + boost mode. The maximum output power is limited to up to 35 kW due to the limitations of the laboratory facilities. One may note that the shape of the efficiency curve in Fig. 5.31 is almost the same as the curve shown in Fig. 5.18 for the 30 kW system. This is not surprising, since the 60 kW system is constructed by interleaving and operating in parallel the same modules used in the 30 kW system.

Fig. 5.32 contains a plot of the measured efficiency as a function of output power at fixed

Figure 5.31: 60 kW system measured efficiency as a function of output power, at fixed $V_{in} = 210\,\text{V}$, $V_{out} = 650\,\text{V}$ in DCX + boost mode

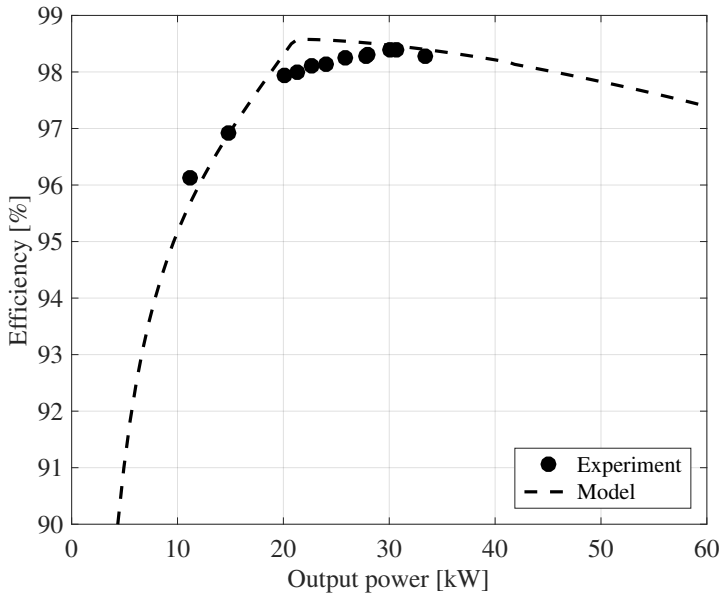
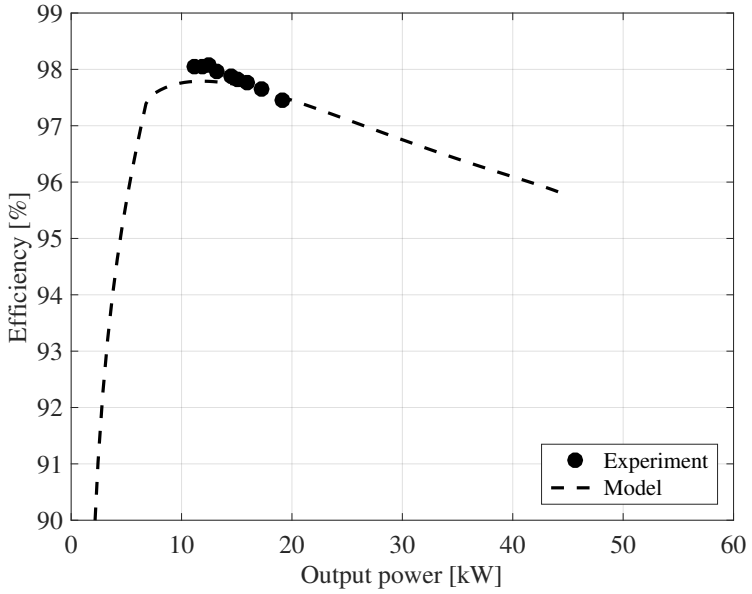


Figure 5.32: 60 kW system measured efficiency as a function of output power, at fixed $V_{in} = 218\,\text{V}$, $V_{out} = 401\,\text{V}$ in the DCX + buck mode



218 V input and 401 V output, in the DCX + buck mode. The maximum output power is limited to up to 20 kW due to limitations of the laboratory equipment.

Figure 5.33: 60 kW system measured efficiency as a function of output power, at fixed $V_{in} = 177$ V, $V_{out} = 540$ V in the DCX + boost mode

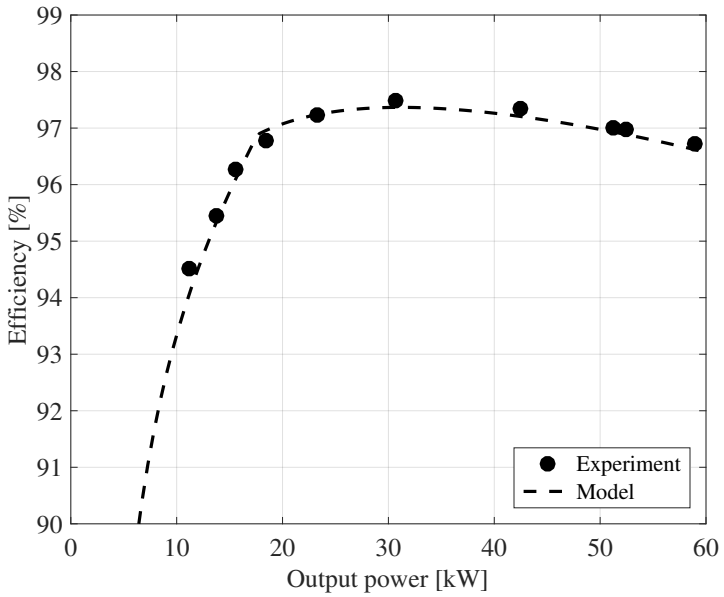
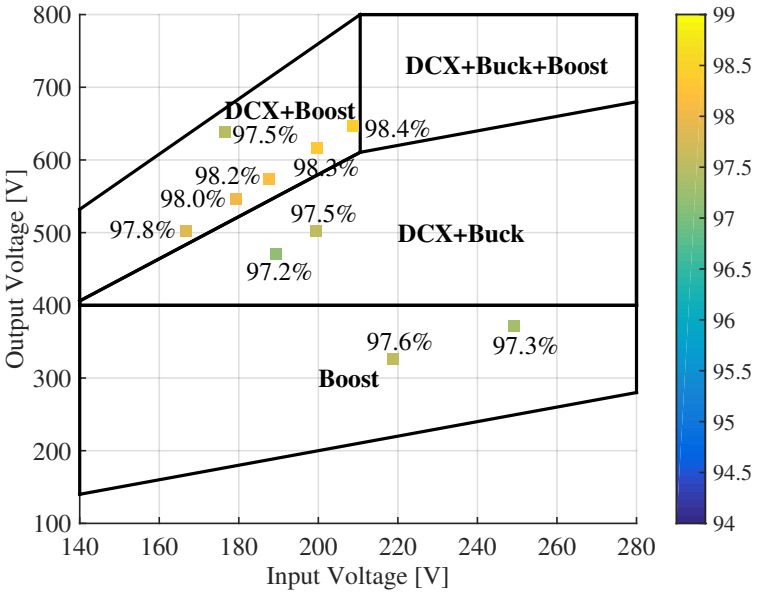


Fig. 5.33 contains a plot of the measured efficiency as a function of output power at fixed 177 V input and 650 V output, in the DCX + boost mode.

Fig. 5.34 shows the system measured efficiency at fixed 30 kW (50%) output power, over different input and output voltages, and under different operating modes. Due to equipment laboratory limitations, some points cannot be measured. Based on the measured points, the efficiency results obtained for the 60 kW system follow the same distribution as the results shown in Fig. 5.19 for the 30 kW system. This is expected, as the 60 kW system is constructed simply by interleaving and operating in parallel the same module prototypes used in the 30 kW system. Furthermore, the measured efficiency results are consistent with the model predictions shown in Fig. 5.26.

Figure 5.34: 60 kW system measured efficiency at different input / output voltages in different modes, with fixed 30 kW output power



5.4 High power density design with wide bandgap devices

Converter size and weight reduction is preferred in the application of electric vehicle. The composite converter with silicon devices can significantly reduce the size of the capacitor module, but not much reduction of size of the magnetics modules, as shown in Table 3.8. On the other hand, wide bandgap devices such as SiC devices represent the future trend of power devices, which provide better on-resistance with much reduced switching loss. With wide bandgap devices, the switching frequency of composite converter modules can be increased, which will reduce the size of magnetic components. Therefore, very high power density design is possible for composite converters with wide bandgap devices.

One particular device of interest is a 900 V SiC MOSFET H-bridge module with 10 mΩ on-resistance, whose parameters are, unfortunately, not for disclosure at the time of this work. Its much reduced device capacitance enables the design of converter modules at the switching frequency of 200 kHz or higher, which significantly reduces the size of magnetic components. What is more, with the well-packaged H-bridge module, the power stage and driver circuitry design can be much

simplified, which saves extra space.

On the other hand, applying the same 33% device de-rating rule, the 900 V devices allows operation at 600 V. If the dc-dc converter input and output voltage specifications keep the same, there is more freedom in the choice of composite converter architectures. Revisiting various composite converter topologies introduced in chapter 3, one particular architecture of interest is composite converter A. The DCX module in composite A converter is required to output maximum voltage of 600 V. Because in chapter 3, only silicon devices are considered, the secondary side of the DCX has to be implemented with 1200 V IGBT. Here 900 V SiC MOSFET is suitable for composite converter A as well.

What makes composite A converter even more attractive for high power density design, is that, as shown in Table 3.6, the composite A converter exhibits the smallest total capacitor power rating: half of that of composite D converter. This is because in composite A converter, part of the output capacitor is shared with the input capacitor, and the output current flowing through that part of the capacitor is purely dc, because it is the direct power path. Therefore, composite A converter may end up with even smaller capacitor size than that of the composite D converter. What is more, the composite A converter may have simpler magnetics design, due to reduced magnetic components count.

Table 5.13: 30 kW Composite A converter with SiC devices magnetics component design

Inductor	Switching frequency	200 kHz
	Inductance	2 µH
	Core material	N49
	Core shape	ELP43
	Number of turns	4
	PCB stacking	2-oz, 4-layer
Transformer	Switching frequency	240 kHz
	Core material	N87
	Core shape	ELP43
	Number of turns	8:12
	PCB stacking	7-oz, 8-layer

To demonstrate the potential of high power density design with composite converter A topology, a 30 kW composite A converter is designed. Two H-bridge modules are used for the non-inverting buck-boost module, each with two half-bridges connected in parallel. The DCX module uses two H-bridge modules as well: one for the primary side, and one for the secondary side. Totally four H-bridge modules are used. With 2 µH inductance, the optimum switching frequency for the non-inverting buck-boost module is 200 kHz. The optimum DCX switching frequency is 240 kHz. The design parameters for the magnetics components are summarized in Table 5.13, and Table 5.14 documents the capacitor design.

Table 5.14: 30 kW Composite A converter with SiC devices capacitor design

	rms current [A]	capacitance [µF]	volume [cm^3]
Input cap	73	17	66
DCX input cap	76	25	72
DCX output cap	30	10	51

The efficiency of the SiC version of composite A design is predicted in Fig. 5.35. Comparing with the silicon version in Fig. 3.9, the efficiency of SiC version is much improved, not only because of reduced semiconductor device loss, but also because of much reduced magnetic loss thanks to higher switching frequency.

One significant drawback of composite converter A is that its efficiency may drop considerably at lower output voltage, because in that case the non-inverting buck-boost module operates with very small buck ratio. On the other hand, from the system point of view, low output bus voltage implies that the vehicle cruises at low speed, where high power consumption is unlikely to happen. Therefore, to fully quantify the performance of composite converter A, its quality factor Q over standard driving cycles should be modeled.

Table 5.15 summarizes the simulated converter quality factor Q of composite converter A design with SiC devices, under different standard driving cycles. Although the improvement with low speed urban driving (UDDS) is incremental, the composite converter A shows more than three times

Figure 5.35: Predicted efficiency of composite converter A with 900 V, at fixed 250 V input and 650 V output.

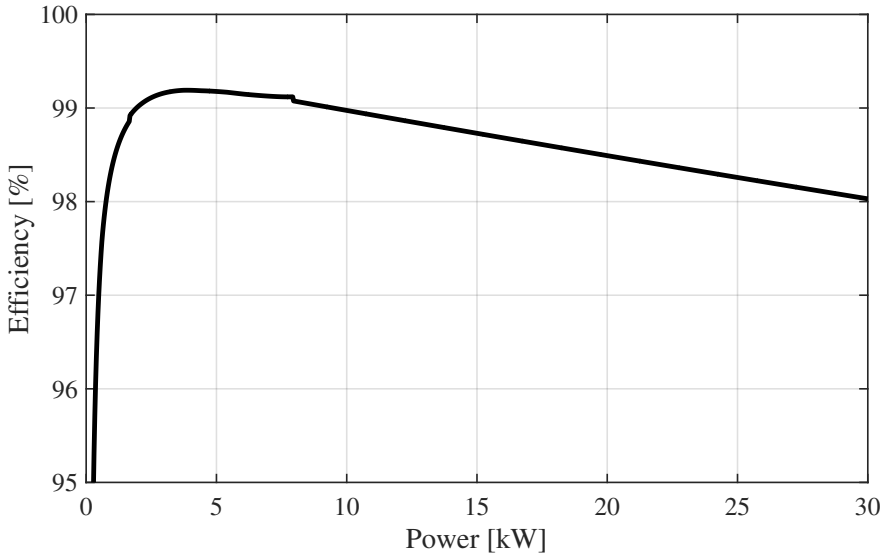


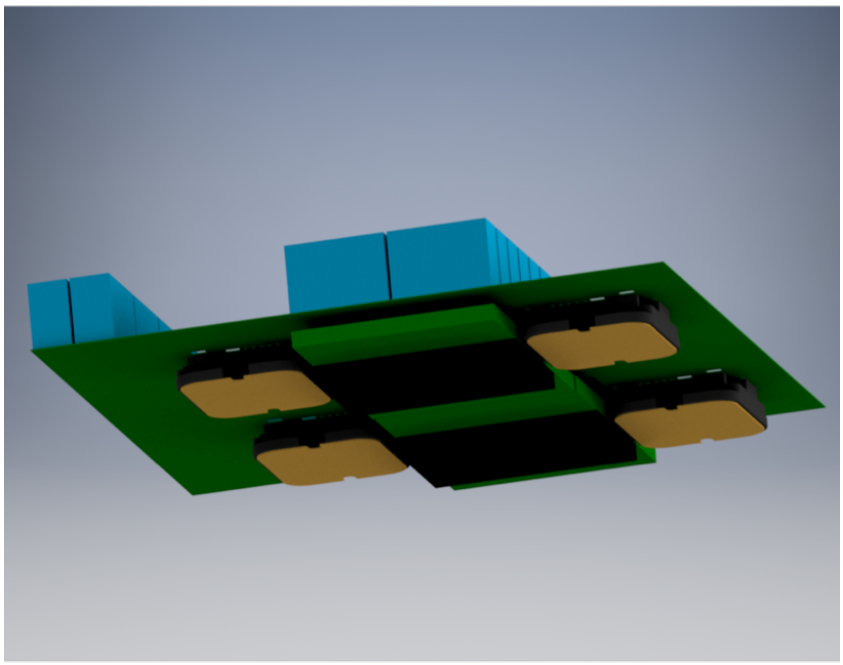
Table 5.15: Converter quality factor Q comparison between composite A converter with SiC devices and the conventional boost converter

	UDDS	HWFET	US06
Composite A	48.0	58.9	69.9
Conventional boost	38.6	17.5	21.9

loss reduction in highway driving profiles (HWFET and US06). Therefore, composite converter A with SiC devices is still an attractive solution for EV application, plus it shows significant power density improvement.

Figure 5.36 shows the CAD rendering of the power stage of the composite A converter design with SiC devices. The board size is 20.1 cm by 21.2 cm, with 3.88 cm height. If a 1.4 cm cold plate is assumed, with 30 kW rated power, the power density of the composite A converter is 13.3 $\mathrm{kW\,L^{-1}}$, or 218 $\mathrm{W/in^3}$.

Figure 5.36: CAD rendering of the composite A converter power stage design with SiC devices



Chapter 6

Control of Composite DC-DC Converter

The previous chapter verifies the efficiency improvements of the composite converter architecture, with open-loop operation. This chapter introduces a possible control architecture for the composite converter, which verifies its controllability.

Because the composite architecture requires controlling several converter modules at the same time, the conventional control architectures no longer apply. On the other hand, to further enhance the system efficiency, each module may operate at pass-through or shut-down mode at certain operating conditions, resulting several system operation modes. In this chapter, a novel centralized control algorithm is proposed. It is able to regulate system output voltage, while optimizing the system efficiency by automatically and smoothly transits the system into corresponding operating mode that yields the best efficiency. It also protects the converter modules from over voltage or over current stress. This control method combines several conventional control techniques, such as average current control and PI compensator. Therefore, it is relatively simple, and can be implemented into some inexpensive hardwares.

In this chapter, Section 6.1 describes the proposed controller, and Section 4.4.3 shows some experimental results.

6.1 Proposed Control Algorithm

The main system control objective is to regulate the output voltage V_{out} at a reference voltage level. The closed-loop control system is expected to achieve high-performance static and dynamic

regulation with respect to variations in commanded reference level, and in the presence of disturbances such as load or input voltage variations. The controller should further automatically adjust the system operating mode to optimize the system efficiency, and to ensure that all devices operate within safe operating limits. Therefore, the controller should be able to control the system so that the steady-state mode is the same as illustrated in Fig. 3.16.

Although the composite converter system is composed of several converter modules, a centralized control algorithm that can be implemented onto a single micro-controller unit is preferred, to reduce control complexity.

The composite converter system has several operation modes. To achieve mode transitions, look-up table or logic-basic mode decision methods may be employed. However, such approaches can easily lead to discontinuities across mode boundaries and undesirable mode-transition disturbances. The control architecture and the control algorithm developed are instead designed to achieve smooth mode transitions.

The control signals available to the composite converter system controller are:

- Buck module duty cycle D_{buck}, $0 \leq D_{buck} \leq 1$, where $D_{buck} = 1$ corresponds to pass-through operation of the buck module, and $D_{buck} = 0$ corresponds to shut-down operation of the buck module.

- Boost module duty cycle D_{boost}, $0 \leq D_{boost} < 1$, where $D_{boost} = 0$ corresponds to pass-through operation of the boost module.

- DCX module on/off control signal DCX enable. When DCX module turns on, it is only operated in open-loop with fixed 50% duty cycle. Therefore, DCX will not operate in those regions that the voltage conversion ratio significantly deviates from transformer turns ratio, which results in much lower efficiency.

To achieve the closed-loop control objectives, the following signals are sensed by the controller:

- The output voltage v_{out}, to achieve the main voltage regulation control objective.

- The buck and the boost module inductor currents i_{Lbuck} and i_{Lboost}, to achieve current protection.
- The boost module output voltage v_{boost} is sensed, and the DCX output voltage is calculated as $v_{DCX} = v_{bus} - v_{boost}$.

The output voltages of the boost and DCX modules are limited to a maximum of $V_{Q,max}$, to ensure that the voltage stresses applied to devices remain within safe derated levels.

6.1.1 Main control loop

Figure 6.1: The block diagram of the main control loop using average current control structure

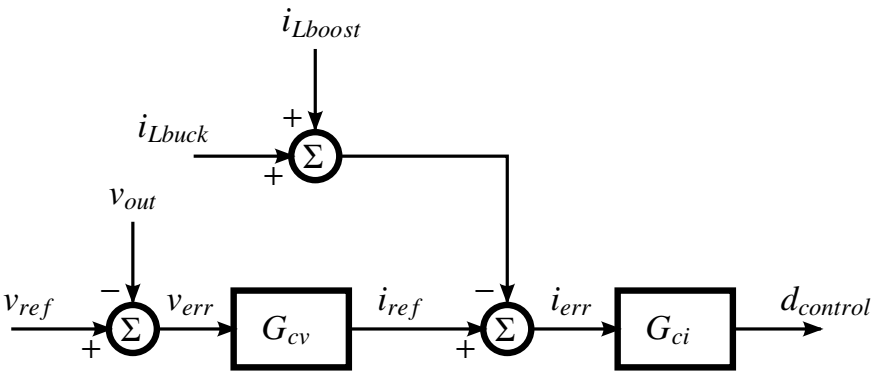


Fig. 6.1 shows a block diagram of the main control loop, which is based on an inner average current control loop and an outer voltage control loop. In the outer loop, the sensed output voltage v_{out} is compared with the voltage reference v_{ref}. The error voltage v_{err} is fed into the voltage loop compensator G_{cv} to generate a reference current i_{ref}. In the inner loop, the sensed inductor currents i_{Lbuck} and i_{Lboost} are summed together, and compared with the reference current i_{ref}. The error current i_{err} is passed to the current loop compensator G_{ci} to generate a control command $d_{control}$.

The main control loop architecture is very similar to the conventional average current control architecture. It also inherits several benefits of average current control. For example, with the inner current loop, the power stage complex poles are well damped and separated. In this design, both

G_{cv} and G_{ci} are implemented as simple PI compensators. Furthermore, by imposing limits to the dynamic range of i_{ref}, the current limiting and therefore current protection are naturally achieved in the system.

In the conventional average current control, only a single inductor current is sensed and controlled. In contrast, in the main control loop shown in Fig. 6.1, there are two inductors currents, which present two state variables, and both of them should be controlled. This is accomplished by summing i_{Lbuck} and i_{Lboost} together. When one of the modules is in the pass-through or shut-down mode, its inductor current has only a DC component. This DC component represents a DC offset that does not affect the control loop dynamics at all because G_{cv} includes an integral controller. Therefore, the summation of i_{Lbuck} and i_{Lboost} can also be regarded as signal multiplexing, which enables the main control loop to exist and operate smoothly in different operating modes, and to ensure that the main control loop is always continuous, without any mode-transition discontinuities.

Another important difference between the main control loop show in Fig. 6.1 and the conventional average current control is that in average current control the current loop output is a duty cycle command that directly controls the power stage, while in the main control loop $d_{control}$ serves as an intermediate control variable that must be resolved into the buck and the boost module duty cycles, respectively. The buck and the boost module duty cycles are generated based on $d_{control}$ using the following algorithm:

$$D_{buck} = \begin{cases} d_{control}, & \text{when } d_{control} < 1 \\ 1, & \text{when } d_{control} \geq 1 \end{cases} \tag{6.1}$$

$$D_{boost} = \begin{cases} 0, & \text{when } d_{control} < 1 \\ d_{control} - 1, & \text{when } d_{control} \geq 1 \end{cases} \tag{6.2}$$

With this algorithm, when $d_{control} < 1$, $D_{boost} = 0$. In this case, the boost module operates in the pass-through mode, and the main controller controls the output voltage through the DCX + buck mode of operation. Similarly, when $d_{control} > 1$, $D_{buck} = 1$. In this case, the buck module operates in the pass-through mode, and the system is in the DCX + boost mode. One may note that

a similar technique has previously been applied in control of four-switch non-inverting buck-boost converters [38, 66]. Fig. 6.2 shows simulation results that illustrates operation of this algorithm. A small hysteresis band is applied at $d_{control} = 1$ to mitigate any jitter at the mode boundary. Other more advanced techniques such as Dead Zone Avoidance and Mitigation (DZAM) [50] possibly could be applied to further improve the system performance around the mode boundaries.

6.1.2 DCX voltage limit

With the control algorithm described in the previous section, the output voltage can be well regulated. However, because DCX is operated in open-loop, when the input voltage is high (or DCX operates in DCM at very light load), there are chances that the DCX output voltage may exceed the safe voltage limits of one or more semiconductor devices. To prevent this, an additional controller algorithm is needed to limit the DCX output voltage. This is accomplished by activating the DCX + buck + boost mode of operation.

Figure 6.2: Simulated DCX + buck to DCX + boost mode transition

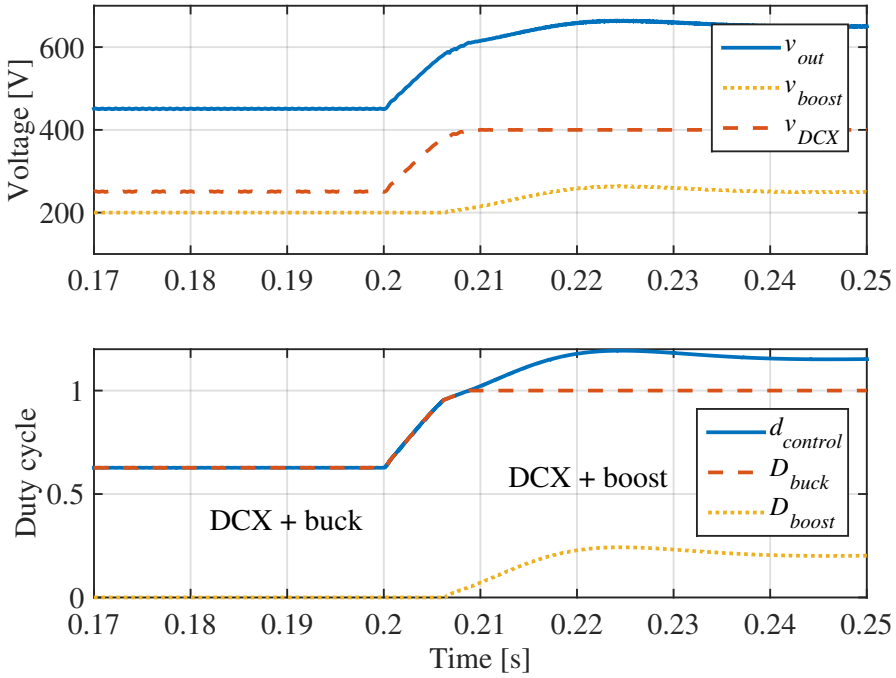


Figure 6.3: The block diagram of the DCX voltage limit block, which leads to DCX + buck + boost mode of operation

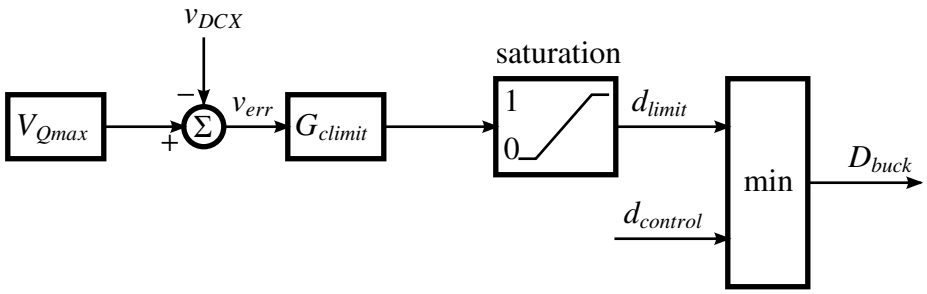


Fig. 6.3 shows a block diagram of the DCX voltage limit controller. The DCX output voltage v_{DCX} is calculated as $v_{DCX} = v_{bus} - v_{boost}$. It is compared with the device safe voltage rating V_{Qmax}. The error is passed to a voltage loop compensator G_{climit} to generate a command d_{limit}, which has a dynamic range between 0 and 1.

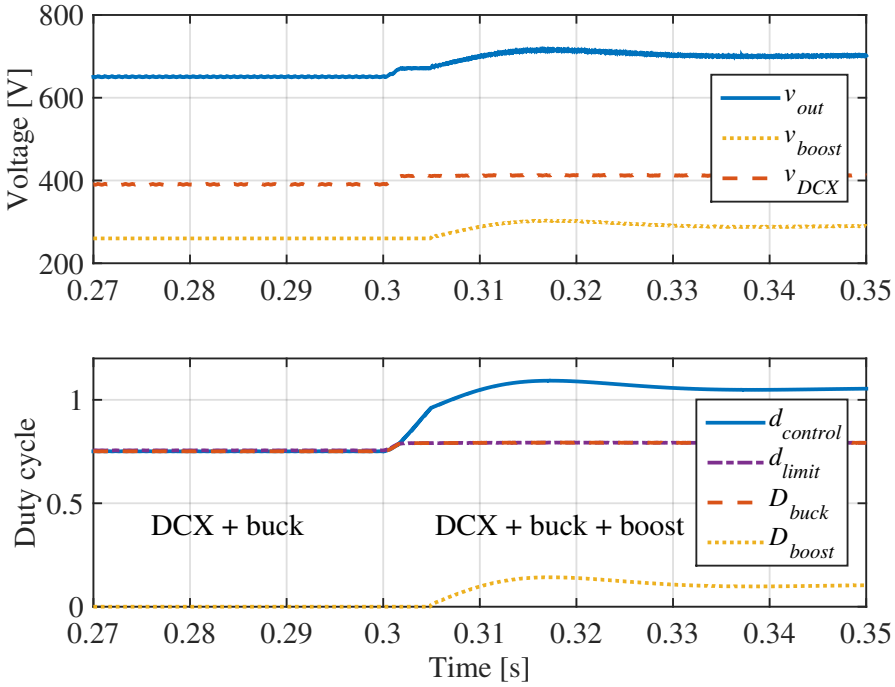
In this design, G_{climit} is implemented as a simple PID compensator. Because of the presence of the integrator inside G_{climit}, when $v_{DCX} < V_{Qmax}$, d_{limit} will always be saturated at 1. Applying

$$D_{buck} = \min\left(d_{limit}, d_{control}\right), \tag{6.3}$$

becomes equivalent to (6.1) in the case when $d_{limit} = 1$. On the other hand, when $v_{DCX} > V_{Qmax}$, the integrator inside G_{climit} will decrease d_{limit} until $d_{limit} < d_{control}$, and the DCX output voltage will be regulated to be equal to V_{Qmax} through this voltage limit control loop. If the system was previously in the DCX + boost mode, the main control loop will keep regulating the bus voltage through the boost module. Otherwise, the main control loop will automatically increase $d_{control}$ until it is becomes greater than 1, and will continue regulating the bus voltage through the boost module.

Fig. 6.4 shows a simulated transition from DCX + buck to DCX + buck + boost mode. In this simulation, DCX output voltage is limited to $V_{Qmax} = 420\,\mathrm{V}$. To improve the DCX voltage limit loop transient performance, the actual d_{limit} range is limited between 0 and $d_{control} + \Delta d$ when $d_{control} < 1$. In this way, once v_{DCX} is slightly higher than V_{Qmax}, the buck converter will

Figure 6.4: Simulated DCX + buck to DCX + buck + boost transition



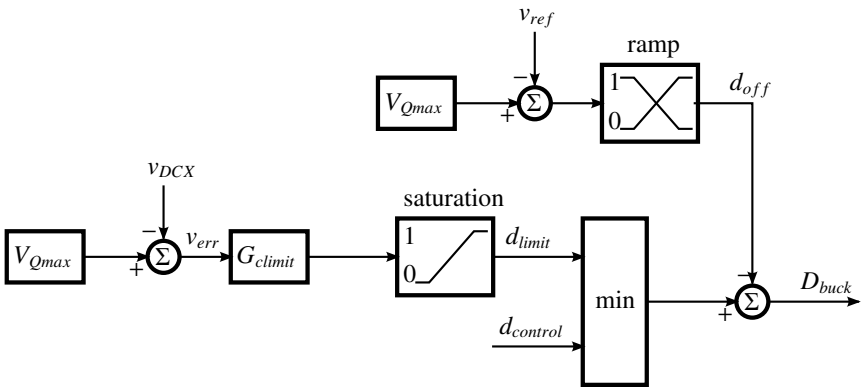
immediately limit v_{DCX} down to V_{Qmax}.

6.1.3 Boost-only mode

With the controller described in the previous sections, the output voltage is well-regulated, and the controller guarantees that all modules operates under their safe voltage ratings. However, when the conversion ratio is small, operating the system in DCX + buck mode may lead to low system efficiency. To improve system efficiency, it is desired to operate the system in boost-only mode, whenever the required output voltage is lower than the device safe voltage rating V_{Qmax}.

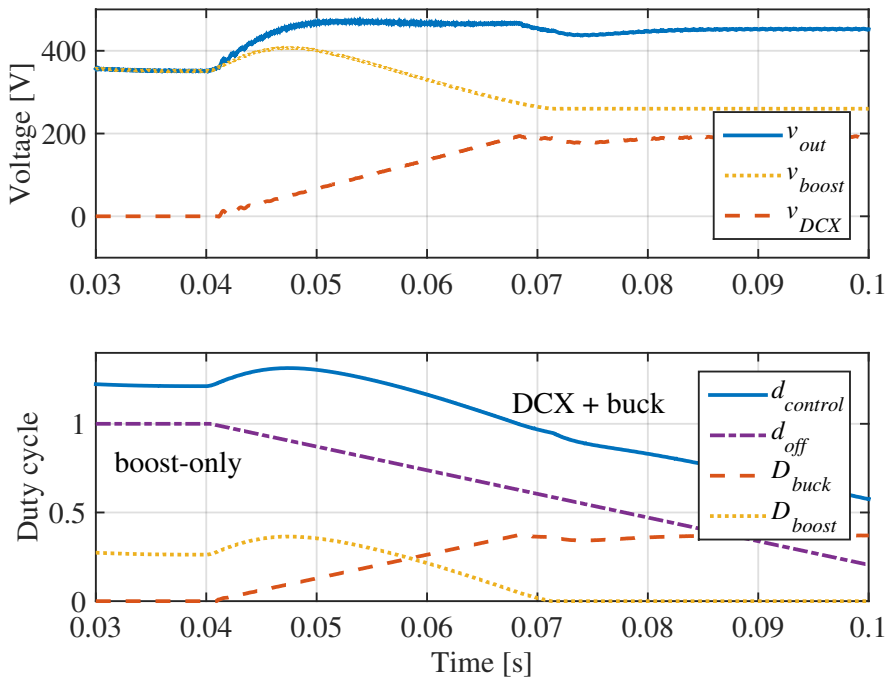
Fig. 6.5 shows the extra buck-off control block added to the DCX voltage limit block. This block compares the reference voltage with the device safe voltage rating V_{Qmax}. If $v_{ref} < V_{Qmax}$, it sends a command d_{off} to turn off the buck module. Notice that there is no feedback path in this block. It is a simple feed-forward path. After it turns the buck module on or off, the main control loop automatically turns the boost module off or on, respectively, to regulate the bus voltage. To

Figure 6.5: The block diagram of DCX voltage limit block with added buck-off block, which forces the system into the Boost-only mode



prevent a discontinuity of abruptly turning the buck module on or off, the d_{off} command ramps up or down smoothly instead of using a step function.

Figure 6.6: Simulated boost-only to DCX + buck transition



To illustrate operation of the extra buck-off control block, Fig. 6.6 shows a simulated transition from boost-only mode to DCX + buck mode. At the start of simulation, the output voltage reference

is low, and the system is in the boost-only mode. In this mode, the buck module and the DCX module are turned off. As a higher output voltage is requested, exceeding the safe voltage rating capabilities of the boost module, the DCX module is turned on, and the buck module is gradually activated. The system smoothly transitions to the DCX + buck mode of operation. Note also that the output voltage remains well regulated throughout the transition, while the boost module output voltage stays below the safe voltage limit.

6.1.4 Auxiliary current loop with band-pass filter

When the buck or the boost module is in the pass-through or off mode, it is operating with duty cycle of 0 or 1, which is in fact a form of open-loop (uncontrolled) operation. If there is a system disturbance, such as load change or input voltage change, an undesirable undamped inductor current resonance can be excited in the pass-through (or off) module.

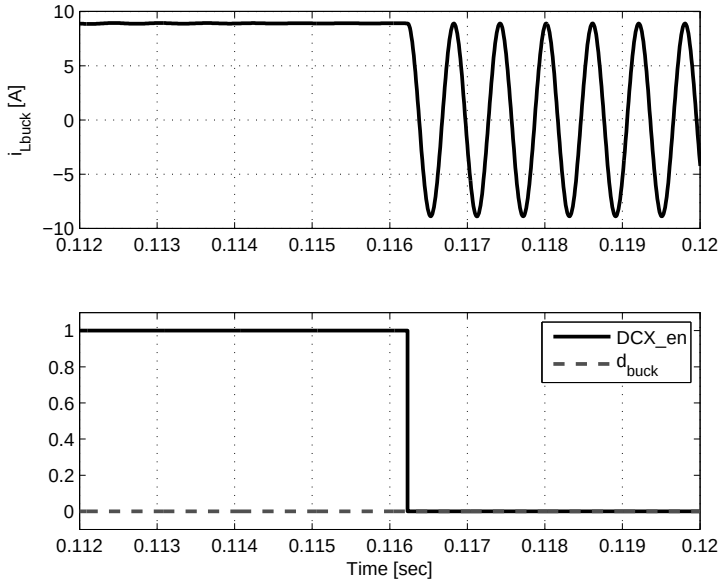
This can also be explained by a simple state-space model of the composite architecture. If the DCX is treated as ideal DC transformer, then the composite system can be modeled as

$$\begin{cases} s\begin{bmatrix} v_{DCX} \\ i_{buck} \\ v_{boost} \\ i_{boost} \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{C'_{DCX}N_{DCX}} & 0 & 0 \\ -\frac{1}{L_{buck}N_{DCX}} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{D'_{boost}}{C_{boost}} \\ 0 & 0 & -\frac{D'_{boost}}{L_{boost}} & 0 \end{bmatrix} \begin{bmatrix} v_{DCX} \\ i_{buck} \\ v_{boost} \\ i_{boost} \end{bmatrix} + \begin{bmatrix} 0 & -\frac{1}{C'_{DCX}} \\ \frac{D_{buck}}{L_{buck}} & 0 \\ 0 & -\frac{1}{C_{boost}} \\ \frac{1}{L_{boost}} & 0 \end{bmatrix} \begin{bmatrix} v_{in} \\ i_{out} \end{bmatrix} \\ v_{out} = \begin{bmatrix} 1 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_{DCX} \\ i_{buck} \\ v_{boost} \\ i_{boost} \end{bmatrix} \end{cases} \tag{6.4}$$

Here the C'_{DCX} is an equivalent capacitance, which equals to the actual DCX output capacitance C_{DCX} plus the buck module output capacitance C_{buck} reflected to DCX output side. For example, when the buck module operates with $D_{buck} = 1$, the system state v_{DCX} and i_{buck} can still be affected

by the system inputs v_{in} and i_{out}. However, these two states are not controllable by D_{boost}.

Figure 6.7: Buck inductor current ringing after DCX turns off

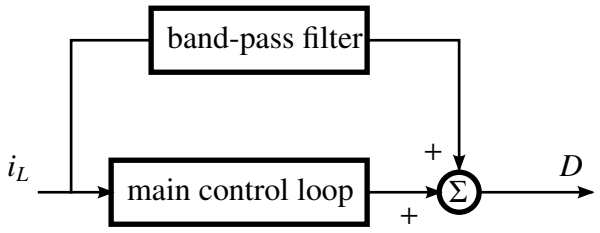


As a specific situation, consider the case when DCX module is turned off shortly after the buck module shuts down, as shown in Fig. 6.7. After the buck module shuts down, the DCX module input and output voltages are ideally zero. However, if the DCX module still operates, its output current, which is actually the load current, is not zero. The DCX input current is then equal to approximately N_{DCX} times the load current. As a result, the buck inductor carries a significant amount of DC current. When DCX finally shuts down, its input current becomes zero. This sharp transition results in the buck module inductor current experiencing a step from around $N_{DCX}I_{out}$ to zero. With the buck converter shut down and not actively controlled, this step can cause significant undamped inductor current ringings, as illustrated in the simulated waveforms shown in Fig. 6.7.

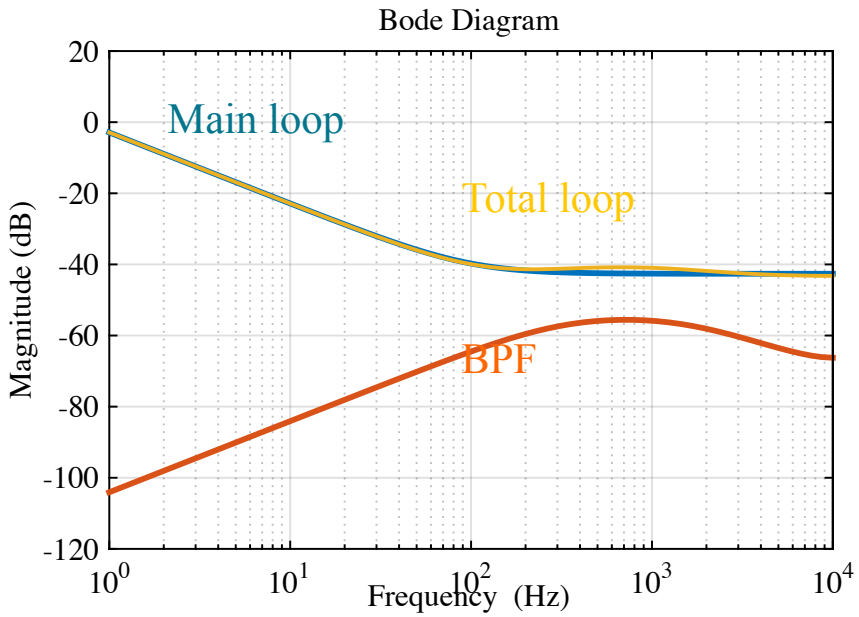
To mitigate this problem, an auxiliary current loop with a band-pass filter can maintain the feedback loop during pass-through or off mode operation in system transients, to damp out the undesirable inductor current resonances, as shown in Fig. 6.8. The band-pass filter should have the pass-band around the converter module natural resonant frequency determined by the module inductance and output capacitance. The magnitude of the filter gain should be much smaller than

Figure 6.8: (a) Extra band-pass-filter current feedback loop that damps out the converter module in pass-through or shut-down mode. (b) The total current loop controller gain frequency response, with the presence of extra band-pass-filter.

(a)



(b)



that of main controller, so that the normal operation of the controller is not affected. Because the DC gain of band-pass filter is zero, the auxiliary loop does not affect the steady-state operation of the modules in shut-down or pass-through modes.

The simulation results shown in Fig. 6.9 illustrate how the buck inductor current ringing is suppressed using the auxiliary band-pass filter current loop.

6.1.5 Summary of controller architecture

Fig. 6.10 shows the complete composite system controller architecture, including all components described in the previous sections. The controller combines the main control loop, the voltage

Figure 6.9: With auxiliary band-pass filter current loop, the buck inductor current ringing is suppressed.

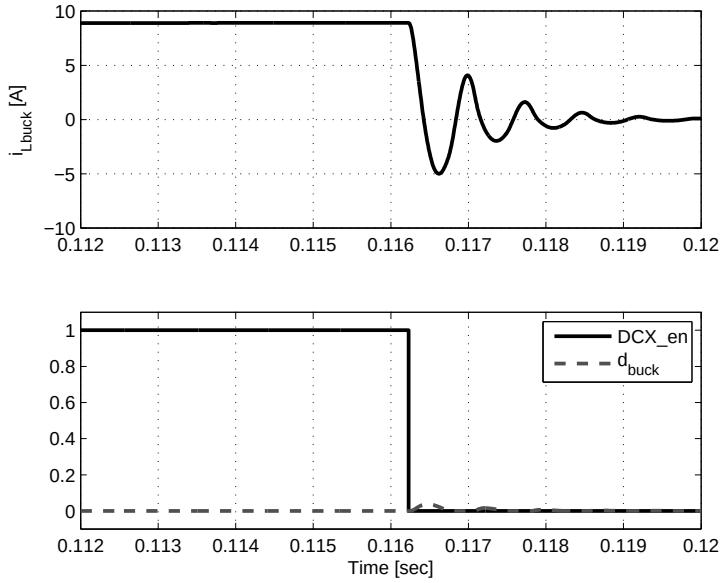
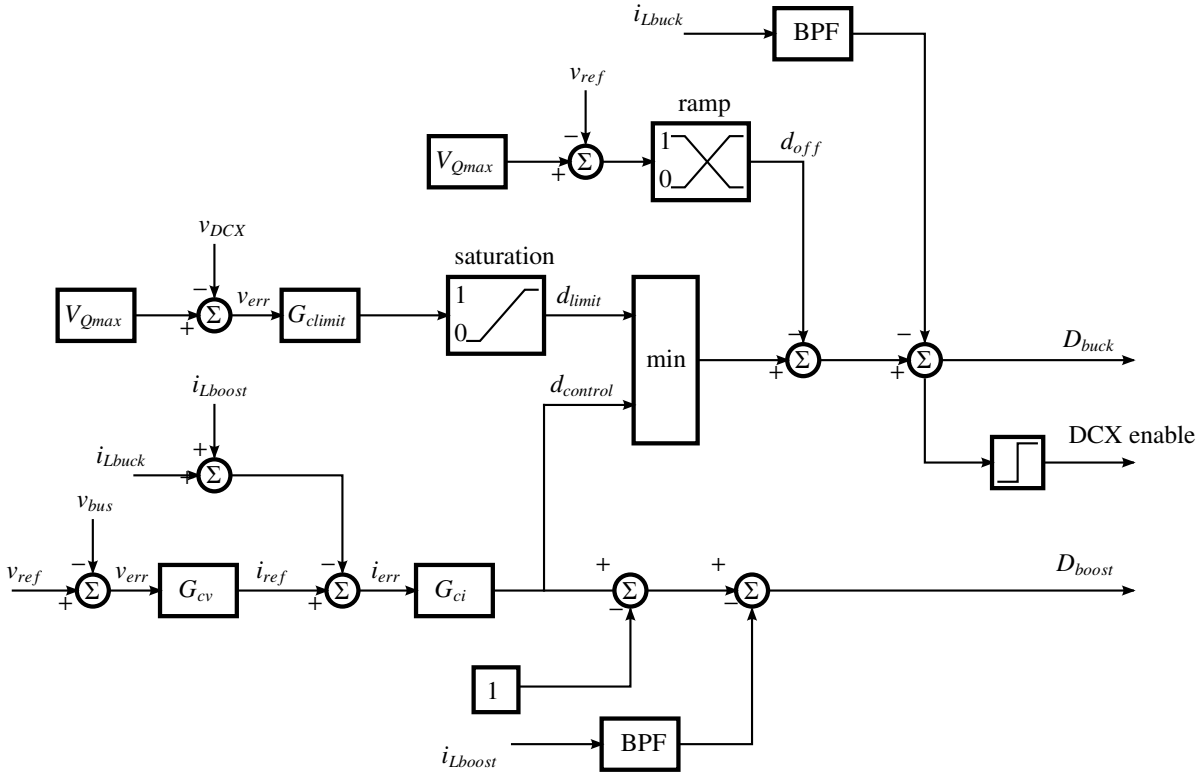


Figure 6.10: The block diagram of the full controller



loop that limits the DCX output voltage, and the feed-forward block that turns the buck module on or off, as well as the auxiliary band-pass current control loops to suppress spurious inductor current oscillations. The DCX enable command is determined simply based on the buck module duty cycle: DCX turns off when $D_{buck} = 0$.

The novel controller architecture shown in Fig. 6.10 and the control algorithms described in this section achieve all control objectives: high-performance voltage regulation, current and voltage protection, as well as smooth mode transitions. The controller is centralized and is relatively simple so that it can be practically implemented on a single micro-controller.

6.2 Experimental result of proposed controller operation

To verify the performance of the proposed control algorithm, it is implemented to control the 30 kW composite converter reported in section 5.2. The control algorithm is coded into TI MSP430F28069 Piccolo 32-bit micro-controller. The inductors currents are sensed with Hall sensor, and on-chip 12-bit ADCs are used to digitize the sensed signals.

With a resistive load, the system is exposed to step changes in reference voltage. The voltage references are selected so that during transients the system remains in one of the operating modes, or so that the system transitions between two operating modes. In the experimental waveforms, the buck and boost module switching node voltages are measured instead of the corresponding module inductor currents, because the currents in the prototype exceed the current rating of the current probes available in the laboratory.

Figs. 6.11 – 6.14 show the system responses to a reference voltage step, for the cases when the system operates within a single operating mode throughout the transient.

The waveforms in Fig. 6.11 show the system closed-loop response to a step reference transient when the system operates in the boost-only mode. In this case, the buck module and the DCX module are off, and the system operation is essentially the same as in a conventional average-current-controlled boost converter. Since the buck module is off, the buck module switch node voltage is always zero. The boost output voltage is almost the same as the output bus voltage, the only

Figure 6.11: Transient waveforms with the output voltage reference step from 300 V to 350 V, at $V_{in} = 180$ V, and approximately 1.9 kW output power. The system is in the boost-only mode.

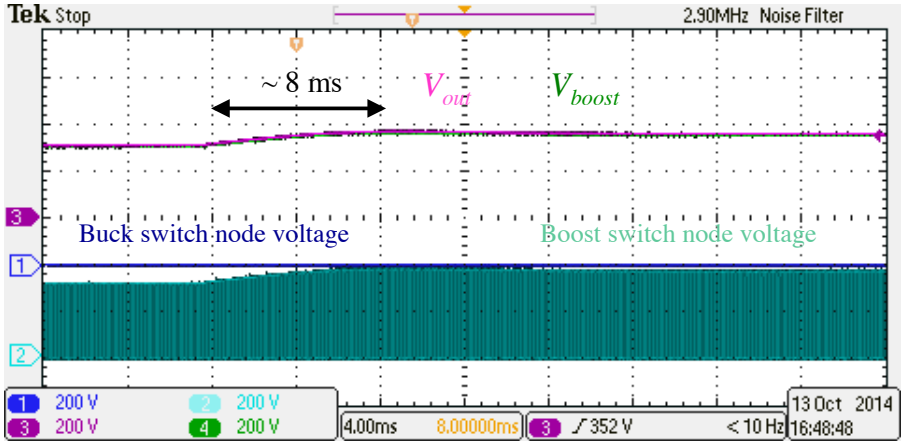
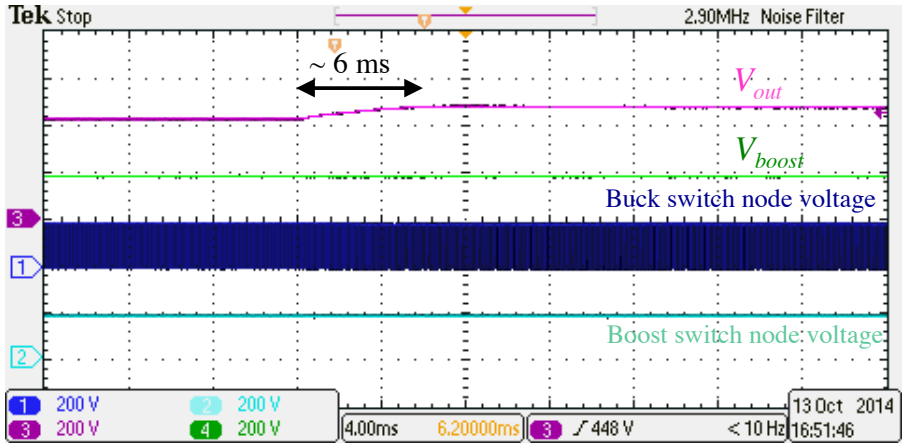


Figure 6.12: Transient waveforms with the output voltage reference step from 420 V to 470 V, at $V_{in} = 180$ V, and approximately 4.3 kW output power. The system is in the DCX + buck mode.



difference being due to the voltage drops across the DCX diodes. The output voltage V_{out} responds to the step reference within 8 ms, with a negligibly small overshoot.

Fig. 6.12 illustrates closed-loop operation of the system in the DCX + buck mode, when the reference steps from 420 V to 470 V. In this case, the boost converter is in pass-through mode, which is why the boost switch node voltage remains equal to the boost output voltage at all times. The boost DC output voltage is very close to the DC input voltage $V_{in} = 180$ V, except for small DC voltage drops across the inductor DC resistance and the MOSFET on-resistance. The buck

Figure 6.13: Transient waveforms with the output voltage reference step from 600 V to 650 V, at $V_{in} = 180$ V, and approximately 9.5 kW output power. The system is in the DCX + boost mode.

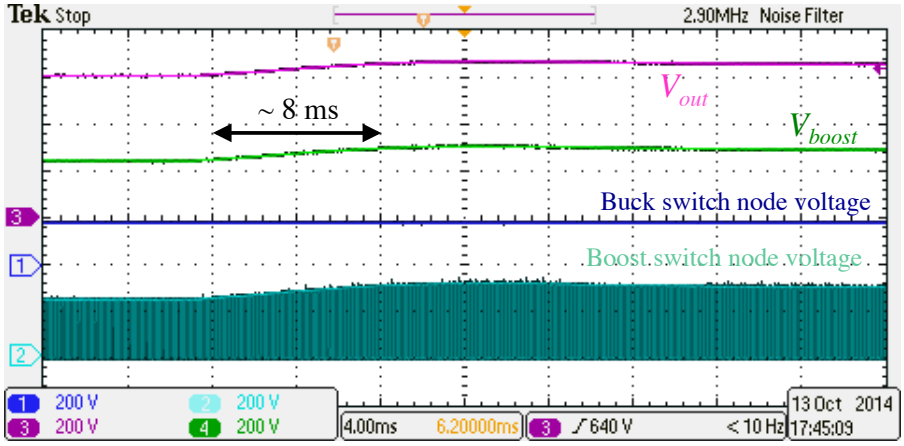
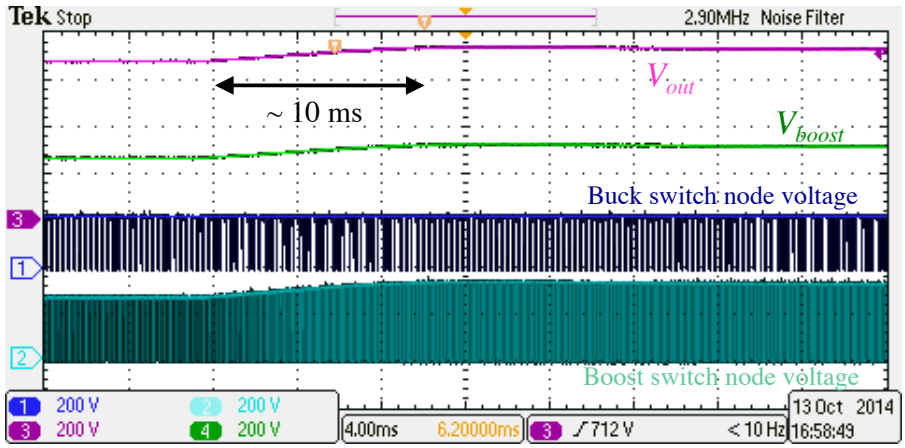


Figure 6.14: Transient waveforms with the output voltage reference step from 670 V to 720 V, at $V_{in} = 220$ V, and approximately 11.3 kW output power. The system is in the DCX + buck + boost mode.

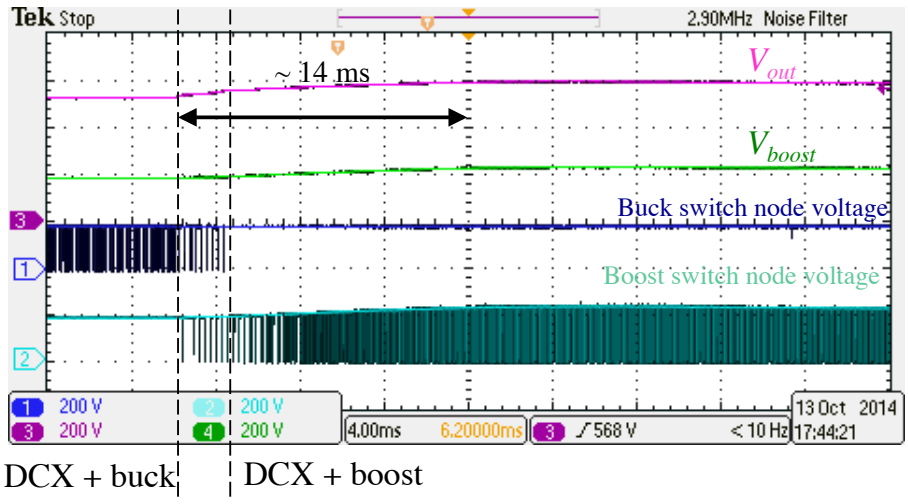


modules are controlled to regulate the output voltage. The output voltage V_{out} responds to the step reference in approximately 6 ms, with a negligibly small overshoot.

The waveforms in Fig. 6.12 show the system closed-loop operation in the DCX + boost mode. The buck modules are in the pass-through mode, which is why the buck switch node voltage is a DC value very close to the input voltage V_{in} = 180 V, except for small DC voltage drops across the buck inductor DC resistance and the buck MOSFET on-resistance. The boost modules are controlled to regulate the output voltage. The output voltage V_{out} responds to the step reference in approximately 8 ms, with a negligibly small overshoot.

Fig. 6.14 shows waveforms illustrating a step reference transient of the system operating in the DCX + buck + boost mode. In this case, both buck and boost modules are active and switching. The voltage reference steps between two relatively high values, 670 V to 720 V. The boost modules are controlled to regulate the output voltage, while the buck modules adjust the DCX input voltage so that the DCX output voltage remains within the safe operating limit (420 V). The output voltage V_{out} responds to the step reference within approximately 10 ms, with no overshoot.

Figure 6.15: Transient waveforms for an output voltage reference step from 520 V to 580 V, at V_{in} = 180 V, and around 7.3 kW output power. The system transitions from DCX + buck mode to DCX + boost mode.



Figs. 6.15 – 6.18 show experimental waveforms in the closed-loop controlled system when the

Figure 6.16: Transient waveforms for a output voltage reference step from 620 V to 670 V, at $V_{in} = 220$ V, and around 9.4 kW output power. The system transitions from DCX + buck mode to DCX + buck + boost mode.

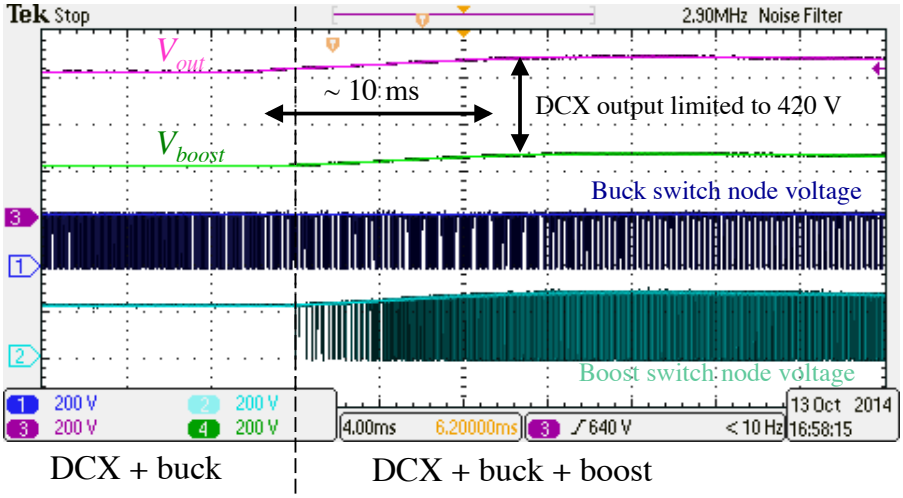
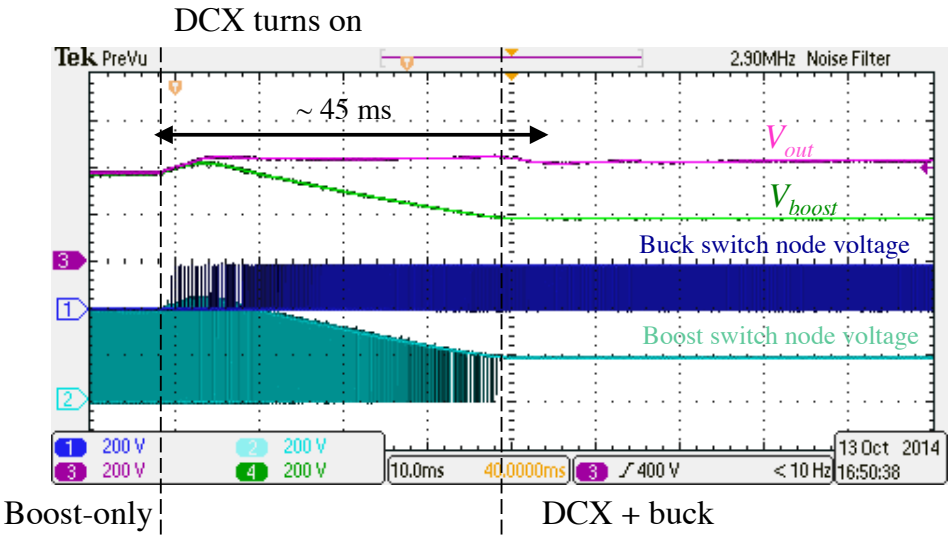


Figure 6.17: Transient waveforms for the output voltage reference step from 370 V to 420 V, at $V_{in} = 180$ V, and around 3.2 kW output power. The system transitions from boost-only mode to DCX + buck mode.



step voltage references are such that the system transitions between two different operating modes.

A system transition from DCX + buck mode to DCX + boost mode is illustrated by the waveforms shown in Fig. 6.15. Initially, the system is in the DCX + Buck mode. The boost modules are in the pass-through mode, and the boost output voltage V_{boost} starts from a value very close to the input voltage $V_{in} = 180$ V. The reference steps from 520 V to 580 V. As the output voltage increases, the buck modules transition to pass-through operation with $D_{buck} = 1$, while the boost modules smoothly take over control of the output voltage. This transient involves only the main control loop. The output voltage V_{out} responds to the step reference within approximately 14 ms, with essentially no overshoot.

A system transition from DCX + buck mode to DCX + buck + boost mode is illustrated by the waveforms shown in Fig. 6.16. In this case, the system starts with the boost module in pass-through mode, while the buck converter duty cycle is controlled to regulate the output voltage at 620 V. Upon a step in the reference to 670 V, as the output voltage increases, the DCX voltage limit control block is activated to limit the DCX output voltage to the safe operating limit, as described in Section 6.1.2. The buck module duty cycle is decreased to limit the DCX output voltage to within the safe operating limit (420 V). To achieve higher regulated output voltage, the boost module duty cycle is increased to increase the boost output voltage. The output voltage V_{out} responds to the reference step in about 10 ms, with essentially no overshoot.

Fig. 6.17 illustrates a system transition from the boost-only mode to the DCX + buck mode. This transition involves the feed-forward control of the buck-off controller block described in Section 6.1.3. Initially, with input $V_{in} = 180$ V, and output $V_{bus} = 370$ V, the system operates in the boost-only mode. The output voltage is very close to the boost output voltage. The buck module and the DCX module are off, and the boost module alone is sufficient to regulate the output voltage. As the reference is stepped to a new, higher value of 420 V, the system must activate the buck and DCX modules, while transitioning the boost module to pass-through operation. To achieve a smooth transition, the DCX module is turned on, and the buck module is gradually activated. At the same time, the boost module duty cycle is initially increased to maintain regulation of the

output voltage, followed by decreasing D_{boost} towards zero, which corresponds to the boost module pass-through operation at the end of the transient. The controller ensures that the boost module output voltage stays below the safe voltage limit. The smooth transition is tuned to minimize transient disturbances in the output voltage. The complete transient takes approximately 45 ms, with a very small overshoot in V_{out}.

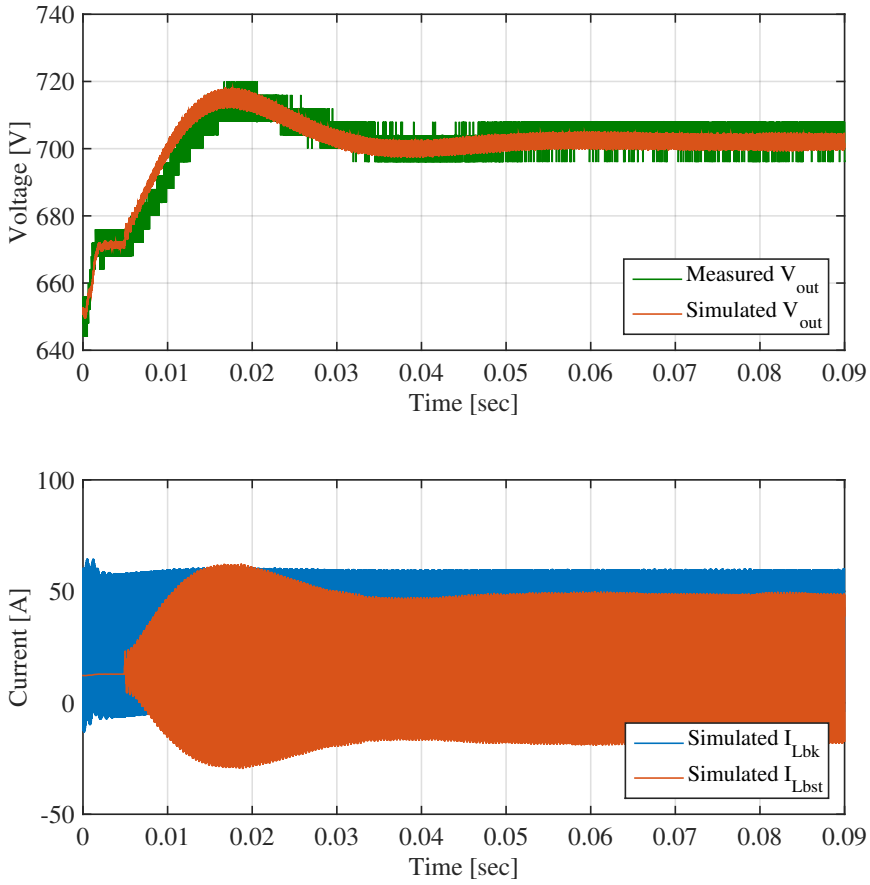


Figure 6.18: Simulation vs. experimental results for the output voltage reference step from 650 V to 700 V, with 260 V input voltage, and around 9.6 kW output power. The measured oscilloscope data (green waveform) is affected by the oscilloscope limited resolution.

To verify validity of the dynamic models and simulation models employed to design the controller parameters, Fig. 6.18 compares waveforms measured on the experimental prototype with waveforms obtained by simulation, when the system is exposed to a 650 V-to-700 V step reference

transient, at V_{in} = 260 V input. In this case, the system transitions from the DCX + buck mode to the DCX + buck + boost mode. The green waveform in the upper (V_{out}) plot is based on the data extracted from the oscilloscope. The glitches are due to the oscilloscope resolution (Tektronix DPO2014B, which has 8-bit resolution). It can be observed that the experimental waveform matches the simulation model waveform very well. The system responds in approximately 30 ms, with overshoot of less than 20 V, or less than 3% of the final regulated DC output voltage.

Chapter 7

Conclusion and extension of the work

In a hybrid or electric vehicle powertrain, a boost dc-dc converter enables reduction of the size of the electric machine and optimization of the battery system. In this work, the composite dc-dc architecture is proposed, which has fundamental efficiency improvements over wide ranges of operating conditions. It results in a decrease in the total loss by a factor of two to four for typical drive cycles. Furthermore, the total system capacitor power rating and energy rating are substantially reduced, which implies potentials for significant reductions in system size and cost.

In chapter 1, a complete mathematical model of the electric vehicle powertrain is derived, which helps to extract the load characteristics of the dc-dc converter for powertrain application. It is identified that, although the converter must be rated at high peak power, the efficiency at medium to light load is critical for the vehicle system performance.

The loss model of the conventional boost converter is reviewed in chapter 2. Though the conventional boost converter can achieve good efficiency at full power, its efficiency at light to medium load is low, because of ac power loss. Various approaches in the existing literature that helps to reduce the ac power loss have been reviewed. They either only achieve incremental improvements, or have to trade efficiency with size and cost of the system.

The concept of composite converter is introduced in chapter 3, with the emphasis of direct / indirect power path. By processing the indirect power efficiently with the DCX module, the composite converter addresses all the loss mechanism in switched mode power converters, and substantial efficiency improvements can be made. Four different composite converter architectures

are proposed, and the composite converter D exhibits superior performance over various previous approaches. Because of the dedicated indirect power path, the composite converter can significantly reduce the capacitor rms current rating as well, which leads remarkable capacitor module size and cost reduction. Table 7.1 compares the converter quality factor Q

$$Q = \frac{\int |P_{out}| \, \mathrm{d}t}{\int P_{loss} \, \mathrm{d}t} \tag{7.1}$$

under standard driving cycles for the composite D converter and the conventional boost converter. The composite D converter reduces the average loss by a factor of three to four in the highway driving profile, and a factor of two in the urban driving profile.

Table 7.1: Converter quality factor Q comparison between the composite D converter and the conventional boost converter, under standard driving cycles

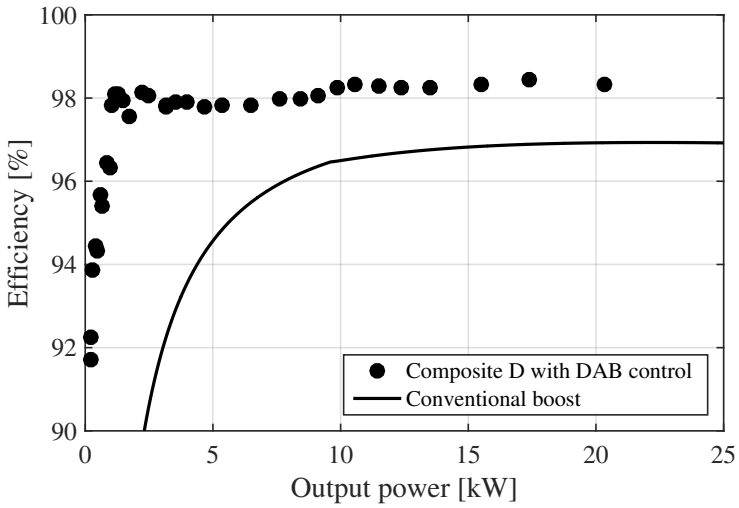
	UDDS	HWFET	US06
Conventional boost	38.6	17.5	21.9
Composite D	74.5	75.2	67.1

As the key component in the composite converter architecture, the DCX is studied extensively in chapter 4. The model of steady-state operation, soft-switching, and loss mechanisms are discussed. A novel resonant mode operation is introduced at light load, to reduce the switching loss, as well as to mitigate the output voltage shoot up at extremely light load condition. With the proposed efficiency-enhanced DAB control, the DCX module efficiency is improved over the full power range, with almost the best possible efficiency, for a given converter power stage design. In particular, the light load efficiency is significantly improved, with more than ten times no-load power loss reduction.

Three different composite converter prototypes are demonstrated in chapter 5, with the power rated at 10 kW, 30 kW, and 60 kW. They validate the composite converter concept, and demonstrate the scalability of this approach. With recorded peak efficiency of 98.5% – 98.7% at medium power level, the composite converters exhibit high efficiency over a wide operation range. Fig. 7.1 shows the measured efficiency of one of the 30 kW prototype, which shows significant efficiency improvement at medium to light load conditions. A compact composite converter design with SiC devices is

discussed as well, which predicts 219 W/in^3 power density.

Figure 7.1: Measured efficiency of the 30 kW prototype, with efficiency-enhanced DAB control enabled, at fixed 250 V input and 650 V output.



In chapter 6, a novel centralized control algorithm is proposed, which verifies the controllability of the composite converter approach. The controller is demonstrated on the 30 kW converter prototype. It not only regulates the output bus voltage, but also can autonomously operate the system at different operation modes, to protect the power devices, as well as improving the system efficiency.

At the current stage, the control algorithm proposed in chapter 6 only considers the resistive load. When the composite converter is integrated into the powertrain, it is loaded by the inverter, whose input impedance is no longer resistive. As the future work of the composite converter, the control algorithm can be improved to accommodate the inverter as the load. After that, the composite converter can be tested in a real powertrain system with the standard driving profiles. Other nonlinear control techniques can also be applied to improve the performance of the existing control algorithm. For example, the DZAM operation [50] can be integrated into the controller to further smooth the boundary transitions.

The future design of composite converter can be extended into the full powertrain system

level optimizations, which includes the design of inverter, motor, and battery pack. For example, with 900 V or 1200 V SiC device available, the composite converter approach may provide the dc bus voltage of 1200 V to 1600 V. It enables the design of ultra high voltage ultra high speed motors, which may achieve better efficiency and power density. With the deeper understanding of the motor loss mechanism, the bus voltage control algorithm can also be improved to further reduce the motor loss. For example, in the HEV system where more than one motor / generator is connected to the dc bus, the choice of dc bus voltage should consider the efficiency of all the motors / generators connected. Regarding the inverter design, inverter architecture such as three-level inverter achieves good balance between system efficiency and motor torque ripple, but requires extra power stage circuitry to generate a neutral voltage point. In the composite converter approach, possibly some internal converter module output voltage can be re-used to help the inverter module. With the concept of composite converter, the battery pack can be re-designed as well. For example, the battery pack can be separated into smaller modules to address the direct / indirect path of the system (reference [96] as an example). The functionality of the composite converter can be augmented as well. For example, the battery charger can be integrated by re-using some converter modules in the composite converter, as proposed in [6].

Bibliography

[1] "Dynamometer Drive Schedules," http://www.epa.gov/nvfel/testing/dynamometer.htm, accessed: 2015-08-24.

[2] A. Abramovitz and K. Smedley, "A resonant dc-dc transformer with zero current ripple," in *IEEE 36th Power Electronics Specialists Conference, 2005. PESC '05.*, June 2005, pp. 1299–1305.

[3] M. Albach, T. Durbaum, and A. Brockmeyer, "Calculating core losses in transformers for arbitrary magnetizing currents a comparison of different approaches," in *27th Annual IEEE Power Electronics Specialists Conference, 1996. PESC '96 Record.,*, vol. 2, Jun 1996, pp. 1463–1468 vol.2.

[4] A. Alesina and M. Venturini, "Solid-state power conversion: A fourier analysis approach to generalized transformer synthesis," *IEEE Transactions on Circuits and Systems*, vol. 28, no. 4, pp. 319–330, Apr 1981.

[5] J. Anderson and F. Peng, "Four quasi-Z-source inverters," in *IEEE Power Electronics Specialists Conference, 2008. PESC 2008.*, June 2008, pp. 2743–2749.

[6] U. Anwar, H. Kim, H. Chen, R. Erickson, D. Maksimovic, and K. Afridi, "A high power density drivetrain-integrated electric vehicle charger," in *submitted to 2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016.

[7] K. Aoyama, N. Motoi, Y. Tsuruta, and A. Kawamura, "High efficiency energy conversion system for decreaces in electric vehicle battery terminal voltage," *IEEJ Journal of Industry Applications*, vol. 5, no. 1, pp. 12–19, 2016.

[8] K. Asano, Y. Inaguma, H. Ohtani, E. Sato, M. Okamura, and S. Sasaki, "High performance motor drive technologies for hybrid vehicles," in *2007 Power Conversion Conference-Nagoya*, 2007.

[9] H. Bai and C. Mi, "Eliminate reactive power and increase system efficiency of isolated bidirectional dual-active-bridge dc-dc converters using novel dual-phase-shift control," *IEEE Transactions on Power Electronics*, vol. 23, no. 6, pp. 2905–2914, Nov 2008.

[10] I. Batarseh and C. Lee, "Steady-state analysis of the parallel resonant converter with LLCC-type commutation network," *IEEE Transactions on Power Electronics*, vol. 6, no. 3, pp. 525–538, Jul 1991.

[11] A. Battiston, J.-P. Martin, E.-H. Miliani, B. Nahid-Mobarakeh, S. Pierfederici, and F. Meibody-Tabar, "Comparison criteria for electric traction system using Z-source/Quasi Z-source inverter and conventional architectures," *IEEE Transactions on Emerging and Selected Topics in Power Electronics*, vol. 2, no. 3, pp. 467–476, Sept 2014.

[12] H. Benda and E. Spenke, "Reverse recovery processes in silicon power rectifiers," *Proceedings of the IEEE*, vol. 55, no. 8, pp. 1331–1354, Aug 1967.

[13] R. Burra and K. Shenai, "CoolMOS integral diode: a simple analytical reverse recovery model," in *2003 IEEE 34th Annual Power Electronics Specialist Conference, 2003. PESC '03.*, vol. 2, 2003, pp. 834–838.

[14] F. Caricchi, F. Crescimbini, G. Noia, and D. Pirolo, "Experimental study of a bidirectional DC-DC converter for the DC link voltage control and the regenerative braking in PM motor drives devoted to electrical vehicles," in *Ninth Annual Applied Power Electronics Conference and Exposition, 1994. APEC '94. Conference Proceedings 1994.,*, Feb 1994, pp. 381–386 vol.1.

[15] I. Castro, D. Lamar, J. Roig, and F. Bauwens, "Modeling capacitive non-linearities and displacement currents of high-voltage SuperJunction MOSFET in a novel analytical switching loss model," in *2014 IEEE 15th Workshop on Control and Modeling for Power Electronics (COMPEL),*, June 2014, pp. 1–9.

[16] C. Chan, "An overview of electric vehicle technology," *Proceedings of the IEEE*, vol. 81, no. 9, pp. 1202–1213, Sep 1993.

[17] ——, "The state of the art of electric and hybrid vehicles," *Proceedings of the IEEE*, vol. 90, no. 2, pp. 247–275, Feb 2002.

[18] ——, "The state of the art of electric, hybrid, and fuel cell vehicles," *Proceedings of the IEEE*, vol. 95, no. 4, pp. 704–718, April 2007.

[19] H. Chan, K. Cheng, and D. Sutanto, "ZCS-ZVS bi-directional phase-shifted DC-DC converter with extended load range," *IEE Proceedings - Electric Power Applications,*, vol. 150, no. 3, pp. 269–277, May 2003.

[20] H. Chen, H. Kim, R. Erickson, and D. Maksimovic, "Electrified automotive powertrain architecture using composite dc-dc converters," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1–1, 2016.

[21] H. Chen, K. Sabi, H. Kim, T. Harada, R. Erickson, and D. Maksimovic, "A 98.7% efficient composite converter architecture with application-tailored efficiency characteristic," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 101–110, Jan 2016.

[22] ——, "A 98.7% efficient composite converter architecture with application-tailored efficiency characteristic," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE),*, Sept 2014, pp. 5774–5781.

[23] J. Chen, D. Maksimovic, and R. Erickson, "Buck-boost PWM converters having two independently controlled switches," in *2001 IEEE 32nd Annual Power Electronics Specialists Conference, 2001. PESC.*, vol. 2, 2001, pp. 736–741 vol.2.

[24] R. M. Corless, G. H. Gonnet, D. E. Hare, D. J. Jeffrey, and D. E. Knuth, "On the Lambert W function," *Advances in Computational mathematics*, vol. 5, no. 1, pp. 329–359, 1996.

[25] D. Costinett, D. Maksimovic, and R. Zane, "Design and control for high efficiency in high step-down dual active bridge converters operating at high switching frequency," *IEEE Trans. on Power Electron.*, vol. 28, no. 8, pp. 3931–3940, 2013.

[26] R. De Doncker and J. Lyons, "The auxiliary resonant commutated pole converter," in *Conference Record of the 1990 IEEE Industry Applications Society Annual Meeting, 1990.,*, Oct 1990, pp. 1228–1235 vol.2.

[27] R. De Doncker, D. Divan, and M. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power applications," *IEEE Trans. on Ind. Applicat.*, vol. 27, no. 1, pp. 63–73, 1991.

[28] G. Deboy, N. Marz, J.-P. Stengl, H. Strack, J. Tihanyi, and H. Weber, "A new generation of high voltage MOSFETs breaks the limit line of silicon," in *International Electron Devices Meeting, 1998. IEDM '98. Technical Digest.,*, 1998, pp. 683–685.

[29] E. Deschamps and I. Barbi, "A flying-capacitor ZVS PWM 1.5 kW DC-to-DC converter with half of the input voltage across the switches," *IEEE Trans. on Power Electronics*, vol. 15, no. 5, pp. 855–860, Sep 2000.

[30] P. Dowell, "Effects of eddy currents in transformer windings," *Proceedings of the Institution of Electrical Engineers,*, vol. 113, no. 8, pp. 1387–1394, August 1966.

[31] EPCOS AG, "Ferrites and accessories: SIFERRIT material N97," Sep. 2006.

[32] ——, "Ferrites and accessories: EELP 102, EILP102 core set (without clamp recess)," June 2013.

[33] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Springer Science+Business, 2001.

[34] J. Estima and A. Marques Cardoso, "Efficiency analysis of drive train topologies applied to electric/hybrid vehicles," *IEEE Transactions on Vehicular Technology*, vol. 61, no. 3, pp. 1021–1031, March 2012.

[35] W. Feng, P. Mattavelli, and F. C. Lee, "Pulsewidth Locked Loop (PWLL) for Automatic Resonant Frequency Tracking in LLC DC-DC Transformer (LLC-DCX)," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1862–1869, April 2013.

[36] W.-T. Franke, M. Mohr, and F. Fuchs, "Comparison of a Z-source inverter and a voltage-source inverter linked with a DC/DC-boost-converter for wind turbines concerning their efficiency and installed semiconductor power," in *IEEE Power Electronics Specialists Conference, 2008. PESC 2008.*, June 2008, pp. 1814–1820.

[37] T. Fujihira, "Theory of semiconductor superjunction devices," *Japanese Journal of Applied Physics*, vol. 36, no. Part 1, No. 10, pp. 6254–6262, 1997. [Online]. Available: http://jjap.jsap.jp/link?JJAP/36/6254/

[38] M. Gaboriault and A. Notman, "A high efficiency, noninverting, buck-boost dc-dc converter," in *Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2004. APEC '04.*, vol. 3, 2004, pp. 1411–1415 Vol.3.

[39] P. Gradzki, M. Jovanovic, and F. Lee, "Computer-aided design for high-frequency power transformers," in *Fifth Annual Applied Power Electronics Conference and Exposition, 1990. APEC '90, Conference Proceedings 1990.,*, March 1990, pp. 336–343.

[40] C. D. Graham, "Physical origin of losses in conducting ferromagnetic materials (invited)," *Journal of Applied Physics*, vol. 53, no. 11, pp. 8276–8280, 1982. [Online]. Available: http://scitation.aip.org/content/aip/journal/jap/53/11/10.1063/1.330306

[41] N. Higuchi and H. Shimada, "Efficiency enhancement of a new two-motor hybrid system," in *2013 World Electric Vehicle Symposium and Exhibition (EVS27),*. IEEE, 2013, pp. 1–11.

[42] M. Hirakawa, M. Nagano, Y. Watanabe, K. Andoh, S. Nakatomi, and S. Hashino, "High power density DC/DC converter using the close-coupled inductors," in *IEEE Energy Conversion Congress and Exposition, 2009. ECCE 2009.*, 2009, pp. 1760–1767.

[43] Infineon AG, "650 V CoolMOS CFD2 power transistor IPW65R041CFD data sheet," Oct. 2011.

[44] S. Inoue and H. Akagi, "A bi-directional isolated DC/DC converter as a core circuit of the next-generation medium-voltage power conversion system," in *37th IEEE Power Electronics Specialists Conference, 2006. PESC '06.*, 2006, pp. 1–7.

[45] Y. Ito, Y. Tsuruta, M. Bando, and A. Kawamura, "Bilateral SAZZ chopper circuit for HEV," in *37th IEEE Power Electronics Specialists Conference, 2006. PESC '06.*, June 2006, pp. 1–6.

[46] Y. Itoh, S. Kimura, J. Imaoka, and M. Yamamoto, "Inductor loss analysis of various materials in interleaved boost converters," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE),*. IEEE, 2014, pp. 980–987.

[47] G. Ivensky, A. Abramovitz, M. Gulko, and S. Ben-Yaakov, "A resonant dc-dc transformer," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 29, no. 3, pp. 926–934, Jul 1993.

[48] A. K. Jain and R. Ayyanar, "PWM control of dual active bridge: Comprehensive analysis and experimental verification," *IEEE Transactions on Power Electronics*, vol. 26, no. 4, pp. 1215–1227, April 2011.

[49] D. Jones and R. Erickson, "Analysis of switching circuits through incorporation of a generalized diode reverse recovery model into state plane analysis," *IEEE Trans. on Circuits Syst. I*, vol. 60, no. 2, pp. 479–490, Feb 2013.

[50] ——, "A nonlinear state machine for dead zone avoidance and mitigation in a synchronous noninverting buck-boost converter," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 467–480, Jan 2013.

[51] ——, "Probabilistic analysis of a generalized perturb and observe algorithm featuring robust operation in the presence of power curve traps," *IEEE Transactions on Power Electronics*, vol. 28, no. 6, pp. 2912–2926, June 2013.

[52] S. Jurkovic, K. Rahman, B. Bae, N. Patel, and P. Savagian, "Next generation chevy volt electric machines; design, optimization and control for performance and rare-earth mitigation," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE),*, Sept 2015, pp. 5219–5226.

[53] M. Kamiya, "Development of Traction Drive Motors for the Toyota Hybrid System," *IEEJ Transactions on Industry Applications*, vol. 126, pp. 473–479, 2006.

[54] Y. Kao and J. Davis, "Correlations between reverse recovery time and lifetime of p-n junction driven by a current ramp," *IEEE Transactions on Electron Devices*, vol. 17, no. 9, pp. 652–657, Sep 1970.

[55] T. Kawashima, S. Funabiki, and M. Yamamoto, "Recovery-less boost converter for electric vehicle," in *13th European Conference on Power Electronics and Applications, 2009. EPE '09.*, 2009, pp. 1–10.

[56] H. Kim, H. Chen, D. Maksimovic, and R. Erickson, "Design of a high efficiency 30 kW boost composite converter," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE),*, Sept 2015, pp. 4243–4250.

[57] R. H. Kingston, "Switching time in junction diodes and junction transistors," *Proceedings of the IRE*, vol. 42, no. 5, pp. 829–834, May 1954.

[58] K. Kono, Y. Nakamura, and M. Yamamoto, "Optimal design of digital control system for interleaved boost chopper circuit with the coupled inductor," in *2011 IEEE Ninth International Conference on Power Electronics and Drive Systems (PEDS),*, Dec 2011, pp. 995–998.

[59] R. Krishnan, *Electric Motor Drives, Modeling and Analysis.* Prentice Hall, Inc, 2001.

[60] F. Krismer and J. Kolar, "Accurate power loss model derivation of a high-current dual active bridge converter for an automotive application," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 3, pp. 881–891, March 2010.

[61] F. Krismer, S. Round, and J. W. Kolar, "Performance optimization of a high current dual active bridge with a wide operating voltage range," in *37th IEEE Power Electronics Specialists Conference, 2006. PESC '06.*, June 2006, pp. 1–7.

[62] J.-S. Lai and D. Nelson, "Energy management power converters in hybrid electric and fuel cell vehicles," *Proceedings of the IEEE*, vol. 95, no. 4, pp. 766–777, April 2007.

[63] P. O. Lauritzen and C. Ma, "A simple diode model with reverse recovery," *IEEE Transactions on Power Electronics*, vol. 6, no. 2, pp. 188–191, Apr 1991.

[64] B. Lax and S. Neustadter, "Transient response of a p-n junction," *Journal of Applied Physics*, vol. 25, no. 9, pp. 1148–1154, 1954.

[65] P.-W. Lee, Y.-S. Lee, D. K. Cheng, and X.-C. Liu, "Steady-state analysis of an interleaved boost converter with coupled inductors," *IEEE Transactions on Industrial Electronics*, vol. 47, no. 4, pp. 787–795, 2000.

[66] Y.-J. Lee, A. Khaligh, and A. Emadi, "A compensation technique for smooth transitions in non-inverting buck-boost converter," in *Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition, 2009. APEC 2009.*, Feb 2009, pp. 608–614.

[67] J. Li, T. Abdallah, and C. Sullivan, "Improved calculation of core loss with nonsinusoidal waveforms," in *Conference Record of the 2001 IEEE Industry Applications Conference, 2001. Thirty-Sixth IAS Annual Meeting.*, vol. 4, Sept 2001, pp. 2203–2210 vol.4.

[68] V. R. H. Lorentz, M. M. Wenger, R. John, M. Marz, and G. Meyer, *Electric Vehicle Business Models: Global Perspectives.* Cham: Springer International Publishing, 2015, ch. Electrification of the Powertrain in Automotive Applications: "Technology Push" or "Market Pull"?, pp. 35–51. [Online]. Available: http://dx.doi.org/10.1007/978-3-319-12244-1_3

[69] L. Lorenz, G. Deboy, A. Knapp, and N. Marz, "COOLMOS^{TM} — a new milestone in high voltage power MOS," in *The 11th International Symposium on Power Semiconductor Devices and ICs, 1999. ISPSD '99. Proceedings.*,, 1999, pp. 3–10.

[70] B. Lu, W. Liu, Y. Liang, F. C. Lee, and J. D. Van Wyk, "Optimal design methodology for LLC resonant converter," in *Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, 2006. APEC '06.*, March 2006, pp. 6 pp.–.

[71] D. Meeker, "Finite element method magnetics version 4.2 user's manual," http://www.femm.info/, 2015.

[72] T. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in *23rd Annual IEEE Power Electronics Specialists Conference, 1992. PESC '92 Record.*,, Jun 1992, pp. 397–403 vol.1.

[73] C. Mi, M. A. Masrur, and D. W. Gao, *Hybrid electric vehicles: principles and applications with practical perspectives.* John Wiley & Sons, 2011.

[74] K. Muta, M. Yamazaki, and J. Tokieda, "Development of new-generation hybrid system THS II – Drastic improvement of power performance and fuel economy," in *SAE paper 2004-01*, 2004.

[75] Y. Nakamura and M. Yamamoto, "Optimal control design method for trans-linked type multi-phase boost converter," in *2011 IEEE Ninth International Conference on Power Electronics and Drive Systems (PEDS)*,, Dec 2011, pp. 991–994.

[76] G. Oggier, G. Garcia, and A. Oliva, "Switching control strategy to minimize dual active bridge converter losses," *IEEE Transactions on Power Electronics*, vol. 24, no. 7, pp. 1826–1838, July 2009.

[77] B. Ozpineci and L. Tolbert, "Comparison of wide-bandgap semiconductors for power electronics applications," Oak Ridge National Laboratory (ORNL), Tech. Rep., 2004.

[78] M. Pavlovsky, Y. Tsuruta, and A. Kawamura, "Bi-directional buck/boost dc-dc converter with ultra high efficiency based on improved SAZZ topology," in *IEEE Energy Conversion Congress and Exposition, 2009. ECCE 2009.*, Sept 2009, pp. 1783–1790.

[79] F. Z. Peng, "Z-source inverter," *IEEE Transactions on Industry Applications*, vol. 39, no. 2, pp. 504–510, Mar 2003.

[80] F. Z. Peng, M. Shen, and K. Holland, "Application of Z-source inverter for traction drive of fuel cell mdash;battery hybrid electric vehicles," *IEEE Transactions on Power Electronics*, vol. 22, no. 3, pp. 1054–1061, May 2007.

[81] J. Power *et al.*, "Drive green 2020: more hope than reality," *A Special Report by JD Power and Associates, November*, 2010.

[82] J. Reinert, A. Brockmeyer, and R. De Doncker, "Calculation of losses in ferro- and ferrimagnetic materials based on the modified steinmetz equation," *IEEE Transactions on Industry Applications*, vol. 37, no. 4, pp. 1055–1061, Jul 2001.

[83] Y. Ren, M. Xu, J. Sun, and F. C. Lee, "A family of high power density unregulated bus converters," *IEEE Transactions on Power Electronics*, vol. 20, no. 5, pp. 1045–1054, Sept 2005.

[84] M. René, D. D. Francesco, K. Matteo-Alessandro, and S. Alois, "CoolMOS^{TM} CFD2: first 650 V rated super junction MOSFET with fast body diode suitable for resonant topologies," Infineon Technologies AG, Tech. Rep., Feb. 2011.

[85] J. Rivas, R. Wahby, J. Shafran, and D. Perreault, "New architectures for radio-frequency dc/dc power conversion," in *2004 IEEE 35th Annual Power Electronics Specialists Conference, 2004. PESC 04.*, vol. 5, June 2004, pp. 4074–4084 Vol.5.

[86] A. T. Russell and E. M. A. Oliveira, "Sine amplitude converters for efficient datacenter power distribution," in *2012 International Conference on Renewable Energy Research and Applications (ICRERA),*, Nov 2012, pp. 1–6.

[87] M. Shen, A. Joseph, J. Wang, F. Peng, and D. Adams, "Comparison of traditional inverters and Z-source inverter for fuel cell vehicles," *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1453–1463, July 2007.

[88] Y. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, and G. Town, "Impedance-source networks for electric power conversion part I: A topological review," *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 699–716, Feb 2015.

[89] R. H. Staunton, C. W. Ayers, J. N. Chiasson, T. A. Burress, and L. D. Marlino, "Evaluation of 2004 toyota prius hybrid electric drive system," Oak Ridge National Laboratory (ORNL); Power Electronics and Electric Machinery Research Facility, Tech. Rep., 2006.

[90] C. Steinmetz, "On the law of hysteresis," *Proceedings of the IEEE*, vol. 72, no. 2, pp. 197–221, Feb 1984.

[91] C. Sullivan, "Optimal choice for number of strands in a litz-wire transformer winding," *IEEE Transactions on Power Electronics*, vol. 14, no. 2, pp. 283–291, Mar 1999.

[92] J. Sun, M. Xu, D. Reusch, and F. Lee, "High efficiency quasi-parallel voltage regulators," in *Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition, 2008. APEC 2008.*, Feb 2008, pp. 811–817.

[93] H. Tao, A. Kotsopoulos, J. L. Duarte, and M. A. M. Hendrix, "Transformer-coupled multiport ZVS bidirectional dc-dc converter with wide input range," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 771–781, March 2008.

[94] Y. Tsuruta, Y. Ito, and A. Kawamura, "Snubber-assisted zero-voltage and zero-current transition bilateral buck and boost chopper for EV drive application and test evaluation at 25 kW," *IEEE Trans. on Ind. Electron.*, vol. 56, no. 1, pp. 4–11, 2009.

[95] Y. Tsuruta and A. Kawamura, "Verification of efficient operation for high power dc chopper," in *Power Electronics and ECCE Asia (ICPE ECCE), 2011 IEEE 8th International Conference on*, May 2011, pp. 1286–1293.

[96] ——, "Principle verification prototype chopper using SiC MOSFET module developed for partial boost circuit system," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE),*, Sept 2015, pp. 1421–1426.

[97] J. D. van Wyk and F. C. Lee, "On a future for power electronics," *IEEE Transactions on Emerging and Selected Topics in Power Electronics*, vol. 1, no. 2, pp. 59–72, June 2013.

[98] K. Vangen, T. Melaa, S. Bergsmark, and R. Nilsen, "Efficient high-frequency soft-switched power converter with signal processor control," in *13th International Telecommunications Energy Conference, 1991. INTELEC '91.*, Nov 1991, pp. 631–639.

[99] K. Venkatachalam, C. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters," in *2002 IEEE Workshop on Computers in Power Electronics, 2002. Proceedings.*, June 2002, pp. 36–41.

[100] R. White, "Emerging on-board power architectures," in *IEEE Applied Power Electronics Conference (APEC '03)*, 2003, pp. 799–804.

[101] K. Wipke, M. Cuddy, and S. Burch, "ADVISOR 2.1: a user-friendly advanced powertrain simulation using a combined backward/forward approach," *IEEE Transactions on Vehicular Technology*, vol. 48, no. 6, pp. 1751–1761, Nov 1999.

[102] D. Wollaver, "Fundamental study of dc to dc conversion system," Ph.D. dissertation, Massachusetts Institute of Technology, 1969.

[103] M. Xu, Y. Liu, J. Sun, and F. Lee, "Σ/sigma DC/DC conversion for computing and telecom applications," in *IEEE Power Electronics Specialists Conference, 2008. PESC 2008.*, June 2008, pp. 1190–1195.

Appendix A

DCX Extended $LLCC$ Resonance Modeling

A.1 Derivation of fourth-order state plane transformation

Equation(4.40) can be rewritten as:

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} \tag{A.1}$$

where

$$\mathbf{x} = \begin{bmatrix} v_s \\ v_p \\ i_l \\ i_m \end{bmatrix} \tag{A.2}$$

and

$$\mathbf{A} = \begin{bmatrix} 0 & 0 & \frac{1}{C_s} & -\frac{1}{C_s} \\ 0 & 0 & -\frac{1}{C_p} & 0 \\ -\frac{1}{L_l} & \frac{1}{L_l} & 0 & 0 \\ \frac{1}{L_m} & 0 & 0 & 0 \end{bmatrix} \tag{A.3}$$

The state space representation of (A.1) can be transformed by matrix $\mathbf{T}$ so that

$$\dot{\bar{\mathbf{x}}} = \bar{\mathbf{A}}\bar{\mathbf{x}} \tag{A.4}$$

where

$$\bar{\mathbf{x}} = \begin{bmatrix} v_1 \\ v_2 \\ i_1 \\ i_2 \end{bmatrix} = \mathbf{T}\mathbf{x} \tag{A.5}$$

and

$$\bar{\mathbf{A}} = \mathbf{T}\mathbf{A}\mathbf{T}^{-1} \tag{A.6}$$

Let

$$\mathbf{T} = \begin{bmatrix} 1 & K_1 & 0 & 0 \\ 1 & K_2 & 0 & 0 \\ 0 & 0 & 1 & K_3 \\ 0 & 0 & 1 & K_4 \end{bmatrix} \tag{A.7}$$

Therefore

$$\bar{\mathbf{A}} = \mathbf{T}\mathbf{A}\mathbf{T}^{-1} = \begin{bmatrix} 0 & 0 & \frac{1}{C_s} - \frac{K_1}{C_p} & -\frac{1}{C_s} \\ 0 & 0 & \frac{1}{C_s} - \frac{K_2}{C_p} & -\frac{1}{C_s} \\ \frac{K_3}{L_m} - \frac{1}{L_l} & \frac{1}{L_l} & 0 & 0 \\ \frac{K_4}{L_m} - \frac{1}{L_l} & \frac{1}{L_l} & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} \frac{-K_2}{K_1-K_2} & \frac{K_1}{K_1-K_2} & 0 & 0 \\ \frac{1}{K_1-K_2} & \frac{-1}{K_1-K_2} & 0 & 0 \\ 0 & 0 & \frac{-K_4}{K_3-K_4} & \frac{K_3}{K_3-K_4} \\ 0 & 0 & \frac{1}{K_3-K_4} & \frac{-1}{K_3-K_4} \end{bmatrix} \tag{A.8}$$

To decouple the states, it is expected that $\bar{\mathbf{A}}$ is in the form of

$$\bar{\mathbf{A}} = \begin{bmatrix} 0 & 0 & * & 0 \\ 0 & 0 & 0 & * \\ * & 0 & 0 & 0 \\ 0 & * & 0 & 0 \end{bmatrix} \tag{A.9}$$

We can define $\xi = C_s/C_p$, and $\psi = L_l/L_m$. To ensure that $\bar{\mathbf{A}}$ conforms to the form of (A.9), it can be solved that

$$K_{1,2} = \frac{\psi + 1 - \xi \pm \sqrt{\Delta}}{2\xi} \tag{A.10}$$

$$K_{3,4} = \frac{\xi + 1 - \psi \pm \sqrt{\Delta}}{2\psi} \tag{A.11}$$

where $\Delta = \xi^2 + \psi^2 + 1 - 2\xi\psi + 2\xi + 2\psi$.

$$\bar{\mathbf{A}} = \begin{bmatrix} 0 & 0 & \frac{\psi K_4}{C_s} & 0 \\ 0 & 0 & 0 & \frac{\psi K_3}{C_s} \\ -\frac{\xi K_2}{L_l} & 0 & 0 & 0 \\ 0 & -\frac{\xi K_1}{L_l} & 0 & 0 \end{bmatrix} \tag{A.12}$$

Therefore, the system can be decoupled as

$$\begin{bmatrix} \dot{v}_1 \\ \dot{i}_1 \end{bmatrix} = \begin{bmatrix} 0 & \frac{\psi K_4}{C_s} \\ -\frac{\xi K_2}{L_l} & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ i_1 \end{bmatrix} \tag{A.13}$$

$$\begin{bmatrix} \dot{v}_2 \\ \dot{i}_2 \end{bmatrix} = \begin{bmatrix} 0 & \frac{\psi K_3}{C_s} \\ -\frac{\xi K_1}{L_l} & 0 \end{bmatrix} \begin{bmatrix} v_2 \\ i_2 \end{bmatrix} \tag{A.14}$$

On $\langle v_1, i_1 \rangle$ state plane, the expressions of the characteristic impedance Z_{01} and natural resonance frequency ω_{01} are:

$$Z_{01} = \sqrt{\frac{\xi + 1 - \psi - \sqrt{\Delta}}{\psi + 1 - \xi - \sqrt{\Delta}} \frac{L_l}{C_s}} \tag{A.15}$$

$$\omega_{01} = \sqrt{\frac{1 + \xi + \psi - \sqrt{\Delta}}{2C_s L_l}} \tag{A.16}$$

Similarly, on $\langle v_2, i_2 \rangle$ state plane:

$$Z_{02} = \sqrt{\frac{\xi + 1 - \psi + \sqrt{\Delta}}{\psi + 1 - \xi + \sqrt{\Delta}} \frac{L_l}{C_s}} \tag{A.17}$$

$$\omega_{02} = \sqrt{\frac{1 + \xi + \psi + \sqrt{\Delta}}{2C_s L_l}} \tag{A.18}$$

Equations (A.13) – (A.18) are the exact state plane solution of the $LLCC$ resonant tank. They are complicated "high entropy" expressions that do not help much to understand the physical insight of the system. In the sense of design oriented analysis, certain reasonable approximations can be applied to simplify the model.

In normal design, usually $L_l \ll L_m$. That is, $\psi \ll 1$. Then equation (A.10) & (A.11) can be approximated as $K_1 \approx 1/\xi$, $K_2 \approx -1$, $K_3 \approx (\xi + 1)/\psi$, and $K_4 \approx -1/(\xi + 1)$. Therefore on $\langle v_2, i_2 \rangle$

plane:

$$v_2 \approx v_s - v_p \tag{A.19}$$

$$i_2 \approx i_l - \frac{C_p}{C_s + C_p} i_m \tag{A.20}$$

$$Z_{02} \approx \sqrt{\frac{L_l}{C_s \parallel C_p}} \tag{A.21}$$

$$\omega_{02} \approx \frac{1}{\sqrt{L_l \left(C_s \parallel C_p\right)}} \tag{A.22}$$

$\langle v_2, i_2 \rangle$ approximately describes that L_l resonates with C_p and C_s in series, with some offsets by i_m. On $\langle v_1, i_1 \rangle$ plane:

$$v_1 \approx v_s + \frac{C_p}{C_s} v_p \tag{A.23}$$

$$i_1 \approx i_l + \frac{L_m}{L_l} \left(\xi + 1\right) i_m \tag{A.24}$$

The $\langle v_1, i_1 \rangle$ plane can be transformed to the $\langle q_1, \lambda_1 \rangle$ plane, which has more physical senses:

$$q_1 = v_1 C_s \approx v_s C_s + v_p C_p \tag{A.25}$$

$$\lambda_1 = i_1 L_l \approx i_l L_l + \left(\xi + 1\right) i_m L_m \tag{A.26}$$

then

$$\begin{bmatrix} \dot{q}_1 \\ \dot{\lambda}_1 \end{bmatrix} = \begin{bmatrix} 0 & \frac{\psi K_4}{L_l} \\ -\frac{\xi K_2}{C_s} & 0 \end{bmatrix} \begin{bmatrix} q_1 \\ \lambda_1 \end{bmatrix} \tag{A.27}$$

and

$$Y_{01} \approx \sqrt{\frac{C_p}{L_m \left(\xi + 1\right)}} \tag{A.28}$$

$$\omega_{01} \approx \frac{1}{\sqrt{L_m \left(C_s + C_p\right)}} \tag{A.29}$$

The $\langle q_1, \lambda_1 \rangle$ plane roughly describes the system's (scaled) total flux resonates with total charge.

A.2 Complete DCX resonant model

The DCX resonant operation includes complicated transitions, where several switch on/off status may occur, which end up with different resonant circuitries. Here each switch on/off status

combination is referred as a 'state'. To model the complete DCX resonant operation, all the possible states are explored and solved. Then a state machine diagram is used to find all the possible state transitions. With each possible state transition, the solution of each individual states are combined to find the total system solution. Finally, each solution is verified to rule out the unreasonable transitions.

Figure A.1: State A

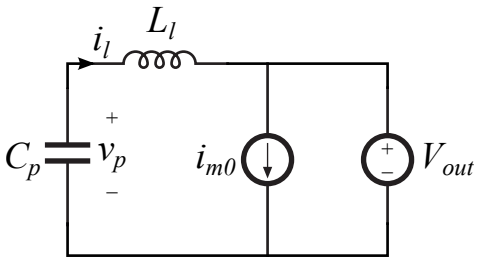


Fig. A.1 shows the equivalent circuit of state A, where only the switches M_5 and M_8 in Fig. 4.1 are on. The state equations of this state is:

$$\begin{cases} L_l \dot{i_l} = v_p - V_{out} \\ C_p \dot{v_p} = -i_l \end{cases} \tag{A.30}$$

The solution is:

$$i_l = i_{lA0} \cos(\omega_A t) + \frac{v_{pA0} - V_{out}}{Z_A} \sin(\omega_A t) \tag{A.31}$$

$$v_p = V_{out} - i_{lA0} Z_A \sin(\omega_A t) + (v_{pA0} - V_{out}) \cos(\omega_A t) \tag{A.32}$$

$$v_s = V_{out} \tag{A.33}$$

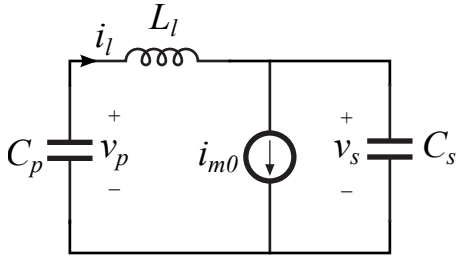
where

$$\omega_A = \frac{1}{\sqrt{C_p L_l}} \tag{A.34}$$

$$Z_A = \sqrt{\frac{L_l}{C_p}} \tag{A.35}$$

Fig. A.2 shows the equivalent circuit of state B, where all the switches are off. The state

Figure A.2: State B



equations of this state is:

$$\begin{cases} L_l \dot{i_l} = v_p - v_s \\ C_p \dot{v_p} = -i_l \\ C_s \dot{v_s} = i_l - i_{m0} \end{cases} \tag{A.36}$$

The solution is:

$$i_l = \left(i_{lB0} - i_{m0} \cdot \frac{C_p}{C_s + C_p} \right) \cos(\omega_B t) + \frac{v_{pB0} - v_{sB0}}{Z_B} \sin(\omega_B t) + i_{m0} \cdot \frac{C_p}{C_s + C_p} \tag{A.37}$$

$$v_p = v_{pB0} - \frac{1}{C_p \omega_B} \cdot \left(i_{lB0} - i_{m0} \cdot \frac{C_p}{C_s + C_p} \right) \sin(\omega_B t) + \frac{(v_{pB0} - v_{sB0}) C_s}{C_s + C_p} (\cos(\omega_B t) - 1) - \frac{i_{m0} t}{C_s + C_p} \tag{A.38}$$

$$v_s = v_{sB0} + \frac{1}{C_s \omega_B} \cdot \left(i_{lB0} - i_{m0} \cdot \frac{C_p}{C_s + C_p} \right) \sin(\omega_B t) - \frac{(v_{pB0} - v_{sB0}) C_p}{C_s + C_p} (\cos(\omega_B t) - 1) - \frac{i_{m0} t}{C_s + C_p} \tag{A.39}$$

where

$$\omega_B = \frac{1}{\sqrt{L_l (C_s \parallel C_p)}} \tag{A.40}$$

$$Z_B = \sqrt{\frac{L_l}{C_s \parallel C_p}} \tag{A.41}$$

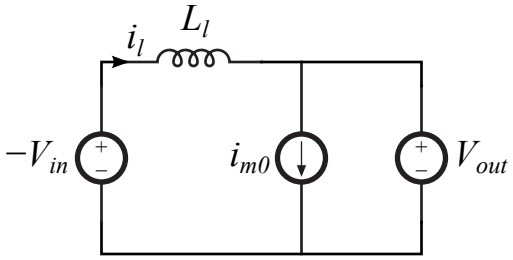
Fig. A.3 shows the equivalent circuit of state C, where the switches M_1, M_4, M_5 and M_8 in Fig. 4.1 are on. The state equations of this state is:

$$L_l \dot{i_l} = -V_{in} - V_{out} \tag{A.42}$$

The solution is:

$$i_l = i_{lC0} - \frac{V_{in} + V_{out}}{L_l} \cdot t \tag{A.43}$$

Figure A.3: State C



$$v_p = -V_{in} \tag{A.44}$$

$$v_s = V_{out} \tag{A.45}$$

Figure A.4: State D

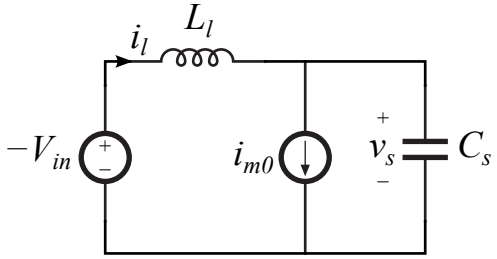


Fig. A.4 shows the equivalent circuit of state D, where the switches M_1 and M_4 in Fig. 4.1 are on. The state equations of this state is:

$$\begin{cases} L_l \dot{i_l} = -V_{in} - v_s \\ C_s \dot{v_s} = i_l - i_{m0} \end{cases} \tag{A.46}$$

The solution is:

$$i_l = (i_{lD0} - i_{m0}) \cos(\omega_D t) - \frac{V_{in} + v_{sD0}}{Z_D} \cdot \sin(\omega_D t) + i_{m0} \tag{A.47}$$

$$v_s = (i_{lD0} - i_{m0}) Z_D \sin(\omega_D t) + (V_{in} + v_{sD0}) \cos(\omega_D t) - V_{in} \tag{A.48}$$

$$v_p = -V_{in} \tag{A.49}$$

where

$$\omega_D = \frac{1}{\sqrt{L_l C_s}} \tag{A.50}$$

$$Z_D = \sqrt{\frac{L_l}{C_s}} \tag{A.51}$$

Figure A.5: State E

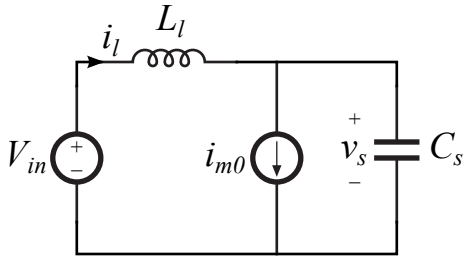


Fig. A.5 shows the equivalent circuit of state E, where the switches M_2 and M_3 in Fig. 4.1 are on. The state equations of this state is:

$$\begin{cases} L_l \dot{i_l} = V_{in} - v_s \\ C_s \dot{v_s} = i_l - i_{m0} \end{cases} \tag{A.52}$$

The solution is:

$$i_l = (i_{lE0} - i_{m0}) \cos(\omega_D t) + \frac{V_{in} - v_{sE0}}{Z_D} \cdot \sin(\omega_D t) + i_{m0} \tag{A.53}$$

$$v_s = (i_{lE0} - i_{m0}) Z_D \sin(\omega_D t) + (-V_{in} + v_{sE0}) \cos(\omega_D t) + V_{in} \tag{A.54}$$

$$v_p = V_{in} \tag{A.55}$$

Figure A.6: State F

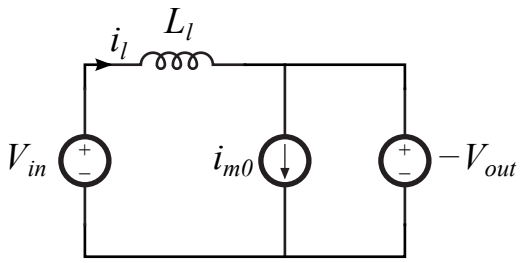


Fig. A.6 shows the equivalent circuit of state F, where the switches M_2, M_3, M_6 and M_7 in Fig. 4.1 are on. The state equations of this state is:

$$L_l \dot{i_l} = V_{in} + V_{out} \tag{A.56}$$

The solution is:

$$i_l = i_{lF0} + \frac{V_{in} + V_{out}}{L_l} \cdot t \tag{A.57}$$

$$v_p = V_{in} \tag{A.58}$$

$$v_s = -V_{out} \tag{A.59}$$

Figure A.7: State G

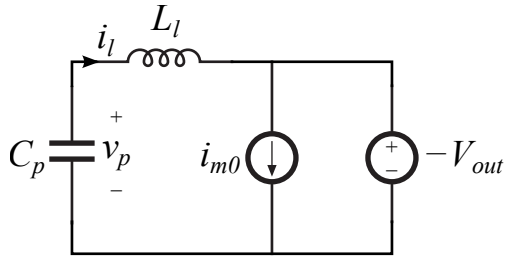


Fig. A.7 shows the equivalent circuit of state G, where the switches M_6 and M_7 in Fig. 4.1 are on. The state equations of this state is:

$$\begin{cases} L_l \dot{i_l} = v_p + V_{out} \\ C_p \dot{v_p} = -i_l \end{cases} \tag{A.60}$$

The solution is:

$$i_l = i_{Gl0} \cos(\omega_A t) + \frac{v_{pG0} + V_{out}}{Z_A} \sin(\omega_A t) \tag{A.61}$$

$$v_p = -V_{out} - i_{lG0} Z_A \sin(\omega_A t) + (v_{pG0} + V_{out}) \cos(\omega_A t) \tag{A.62}$$

$$v_s = -V_{out} \tag{A.63}$$

State H and I shown in Fig. A.8 & A.9 are the two main conduction states.

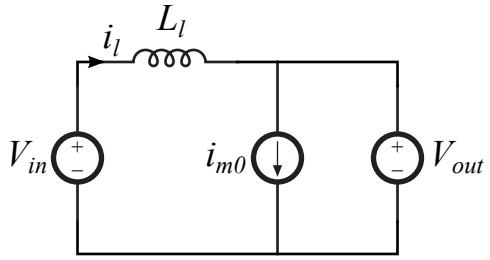


Figure A.8: State H

Figure A.10 sketches the state transition diagram, with all the possible state transition between the two main conduction states H and I. The state transition conditions are labeled in

Figure A.9: State I

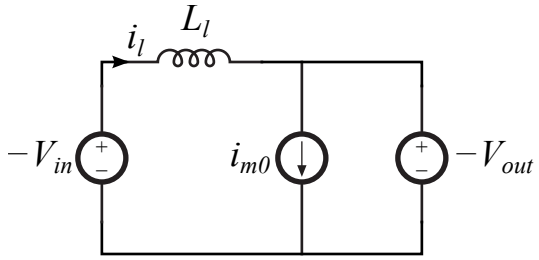


Fig. A.10 as well. The 'H.S.' is short-term for hard-switching. With this state transition diagram, different state transitions can be found solved. For example, the transition (H)-A-B-D-(I) requires solving equations (A.31) – (A.35), (A.37) – (A.41), (A.47) – (A.51), together with the voltage-second balance equation and the charge balance equation. After the solution is found, the state transition conditions along the (H)-A-B-D-(I) path are verified to rule out the non-physical solutions.

Figure A.10: State transition diagram

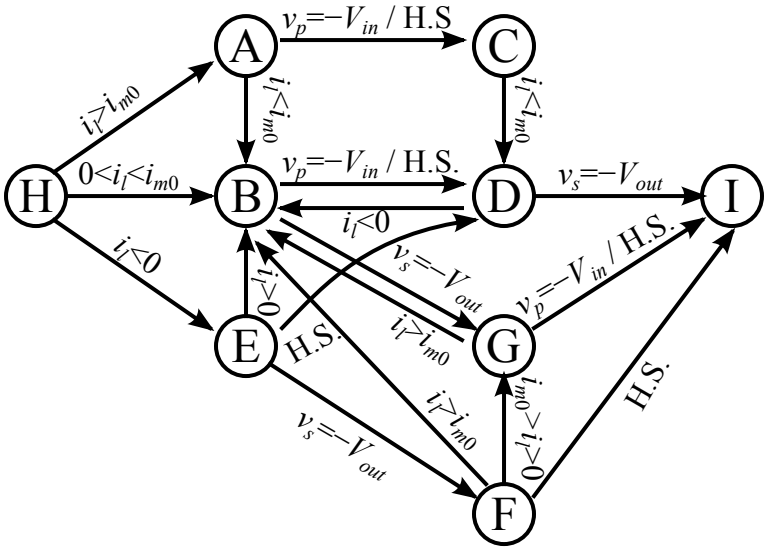
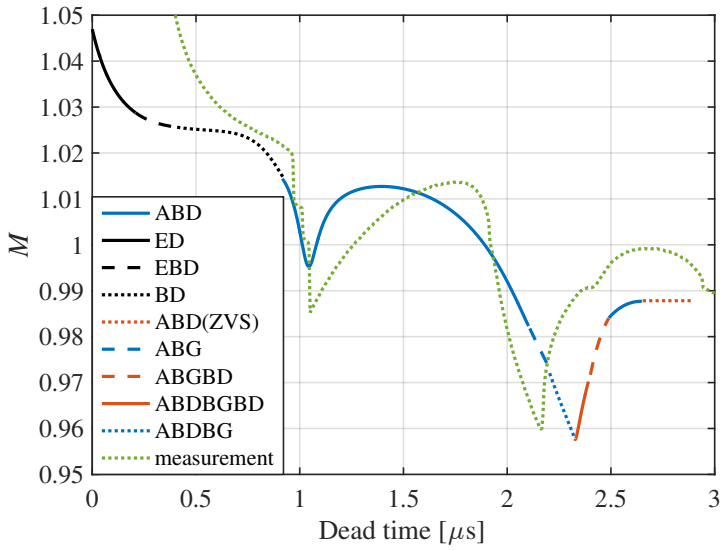


Figure A.11 plots the analytical solutions of the resonant transition. At each point, different state transitions are guessed and tried, until a physical solution is found. The calculated analytical solution is compared with the measurement results. Generally the model predicts the trend in the measurement, although detailed discrepancies can be found. The discrepancy mainly comes from two sources: 1) in the analytical model, ideal diode is assumed, and the diode reverse-recovery

behavior is not modeled; 2) the nonlinearity of device output capacitance is not considered.

Figure A.11: Resonant transition analytical model and measurement comparison.



Appendix B

Implementation of efficiency-enhanced DAB control

The details of the implementation of the efficiency-enhanced DAB control, which is discussed in section 4.6, is documented in this chapter.

The controller is implemented in Texas Instrument's C2000 Piccolo 32-bit micro-controller TMS320F28069. It is a 90 MHz micro-controller, with 16 channels of 12-bit ADC, and 8 modules of enhanced pulse-width modulator (ePWM).

In the DCX prototype hardware, the DCX primary-side H-bridge switches are controlled by two PWM commands: one for each half-bridge; and the DCX secondary-side H-bridge switches are controller by one PWM command: two half-bridges operate in complimentary manner. Therefore, totally three ePWM modules are used to control the DCX converter. Table B.1 documents the designation of these PWM channels. The ePWM1 and ePWM2 channels are reserved for the PWM commands of buck and boost module in the composite D converter.

Table B.1: Micro-controller ePWM channel designation

ePWM3	ePWM4	ePWM5
primary-side half-bridge 1	primary-side half-bridge 2	secondary-side H-bridge

The following code segment demonstrates the initialization for ePWM modules.

```
131 void epwm3(void) // DCX P1
132 {
133   EALLOW;
```

```
134   EPwm3Regs.TBPRD = 1350; // Set timer period 33 kHz (2700 period)
135   EPwm3Regs.TBPHS.half.TBPHS = 0x0000; // Phase is 0
136   EPwm3Regs.TBCTR = 0x0000; // Clear counter
137   EPwm3Regs.TBCTL.bit.SYNCOSEL = TB_CTR_ZERO;
138
139   // Setup TBCLK
140   EPwm3Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // triangular
          modulation
141   EPwm3Regs.TBCTL.bit.PHSEN = TB_DISABLE; // Disable phase loading
142   EPwm3Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1; // Clock ratio to SYSCLKOUT
143   EPwm3Regs.TBCTL.bit.CLKDIV = TB_DIV1;
144
145   // Setup compare
146   EPwm3Regs.CMPA.half.CMPA = 675; // 50% duty cycle
147
148   // Set actions
149   EPwm3Regs.AQCTLA.bit.CAU = AQ_SET;
150   EPwm3Regs.AQCTLB.bit.CAU = AQ_CLEAR;
151   EPwm3Regs.AQCTLA.bit.CAD = AQ_CLEAR;
152   EPwm3Regs.AQCTLB.bit.CAD = AQ_SET;
153
154   // Active high complementary PWMs - Setup the deadband
155   EPwm3Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;
156   EPwm3Regs.DBCTL.bit.HALFCYCLE = 0; // disable high resolution DB
157   EPwm3Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
158   EPwm3Regs.DBCTL.bit.IN_MODE = DBA_ALL;
159
160   // Set default dead time
161   EPwm3Regs.DBRED = 37;
162   EPwm3Regs.DBFED = 37;
163
164   EPwm3Regs.ETSEL.bit.SOCAEN  = 1; // Enable SOC on A group
165   EPwm3Regs.ETSEL.bit.SOCASEL = 1; // Select SOC from equal to zero
166   EPwm3Regs.ETPS.bit.SOCAPRD  = 1; // Generate pulse on 1st event
167
168   EDIS;
169 }
170
171 void epwm4(void) // DCX P2
172 {
173   EALLOW;
174   EPwm4Regs.TBPRD = 1350; // Set timer period
175   EPwm4Regs.TBPHS.half.TBPHS = 1350; // 180 degree phase shift
176   EPwm4Regs.TBCTR = 0x0000; // Clear counter
177   EPwm4Regs.TBCTL.bit.SYNCOSEL = TB_CTR_ZERO;
178
179   // Setup TBCLK
```

```
180   EPwm4Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // triangular
          modulation
181   EPwm4Regs.TBCTL.bit.PHSEN = TB_ENABLE; // Enable phase loading
182   EPwm4Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1; // Clock ratio to SYSCLKOUT
183   EPwm4Regs.TBCTL.bit.CLKDIV = TB_DIV1;
184
185   // Setup compare
186   EPwm4Regs.CMPA.half.CMPA = 675; // 50% duty cycle
187
188   // Set actions
189   EPwm4Regs.AQCTLA.bit.CAU = AQ_SET;
190   EPwm4Regs.AQCTLB.bit.CAU = AQ_CLEAR;
191   EPwm4Regs.AQCTLA.bit.CAD = AQ_CLEAR;
192   EPwm4Regs.AQCTLB.bit.CAD = AQ_SET;
193
194   // Active high complementary PWMs - Setup the deadband
195   EPwm4Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;
196   EPwm4Regs.DBCTL.bit.HALFCYCLE = 0; // disable high resolution DB
197   EPwm4Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
198   EPwm4Regs.DBCTL.bit.IN_MODE = DBA_ALL;
199
200   // Set default dead time
201   EPwm4Regs.DBRED = 37;
202   EPwm4Regs.DBFED = 37;
203   EDIS;
204 }
205
206 void epwm5(void) // DCX S
207 {
208   EALLOW;
209   EPwm5Regs.TBPRD = 1350; // Set timer period, 33 kHz
210   EPwm5Regs.TBPHS.half.TBPHS = 0; // Phase is 0
211   EPwm5Regs.TBCTR = 0x0000; // Clear counter
212
213   // Setup TBCLK
214   EPwm5Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // triangular
          modulation
215   EPwm5Regs.TBCTL.bit.PHSEN = TB_ENABLE; // Enable phase loading
216   EPwm5Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1; // Clock ratio to SYSCLKOUT
217   EPwm5Regs.TBCTL.bit.CLKDIV = TB_DIV1;
218
219   // Setup compare
220   EPwm5Regs.CMPA.half.CMPA = 675; // 50% duty cycle
221
222   // Set actions
223   EPwm5Regs.AQCTLA.bit.CAU = AQ_SET;
224   EPwm5Regs.AQCTLB.bit.CAU = AQ_CLEAR;
```

```
225   EPwm5Regs.AQCTLA.bit.CAD = AQ_CLEAR;
226   EPwm5Regs.AQCTLB.bit.CAD = AQ_SET;
227
228   // Active high complementary PWMs - Setup the deadband
229   EPwm5Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;
230   EPwm5Regs.DBCTL.bit.HALFCYCLE = 0; // disable high resolution DB
231   EPwm5Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC; // for phase 3
232   EPwm5Regs.DBCTL.bit.IN_MODE = DBA_ALL;
233
234   // Set default dead time
235   EPwm5Regs.DBRED = 127;
236   EPwm5Regs.DBFED = 127;
237
238   EDIS;
239 }
```

In this configuration, the ePWM4 channel is synchronized to ePWM3 channel, with 180° phase shift, and the ePWM5 channel is synchronized to ePWM4 channel, with 0° phase shift. Notice that the registers that controls the dead-time, DBRED and DBRED, are both 10-bit registers. It means the counter for dead-time cannot exceed $2^{10} - 1 = 1023$ counts. To achieve sufficient dead-time for the resonant mode operation, the high-resolution dead-time function is disabled.

What is more, the channel A of the triggering signal for the start-of-conversion (SOCA) is enabled in ePWM3, which is used to synchronize the ADC sampling.

In the efficiency-enhanced DAB control, two input signals are required: the DCX input voltage V_{DCXin} and output voltage V_{DCXout}. While the DCX module is used in the composite D converter, its output is stacked on top of a boost converter. Therefore, the direct measurement of V_{DCXout} is difficult. Instead, the total bus voltage V_{bus}, and the boost converter module output voltage V_{boost} are measured. Together with the buck converter module output voltage V_{buck}, the input signals are derived as:

$$V_{DCXin} = V_{buck} \tag{B.1}$$

$$V_{DCXout} = V_{bus} - V_{boost}. \tag{B.2}$$

Table B.2 documents the ADC channel configurations for these signals.

The following code segments implements the documented ADC configuration:

Table B.2: Micro-controller ADC channel configuration

	Channel	start-of-conversion	interrupt	CLA trigger
V_{bus}	A1	SOC2	ADCINT2	Task 2
V_{boost}	A2	SOC3	ADCINT3	Task 3
V_{buck}	B2	SOC5	ADCINT1	Task 1

```
87  EALLOW;
88  AdcRegs.INTSEL1N2.bit.INT1E     = 1;  // Enabled ADCINT1
89  AdcRegs.INTSEL1N2.bit.INT1CONT  = 0;  // Disable ADCINT1 Continuous
       mode
90  AdcRegs.INTSEL1N2.bit.INT1SEL   = 5;  // setup EOC5 to trigger
       ADCINT1 to fire
91
92  AdcRegs.INTSEL1N2.bit.INT2E     = 1;  // Enabled ADCINT2
93  AdcRegs.INTSEL1N2.bit.INT2CONT  = 0;  // Disable ADCINT2 Continuous
       mode
94  AdcRegs.INTSEL1N2.bit.INT2SEL   = 2;  // setup EOC2 to trigger
       ADCINT2 to fire
95
96  AdcRegs.INTSEL3N4.bit.INT3E     = 1;  // Enabled ADCINT3
97  AdcRegs.INTSEL3N4.bit.INT3CONT  = 0;  // Disable ADCINT3 Continuous
       mode
98  AdcRegs.INTSEL3N4.bit.INT3SEL   = 3;  // setup EOC3 to trigger
       ADCINT3 to fire
99
100 AdcRegs.ADCSOC2CTL.bit.CHSEL  = 1;    // set SOC2 channel select to
       ADCINA1, Vbus
101 AdcRegs.ADCSOC3CTL.bit.CHSEL  = 2;    // set SOC3 channel select to
       ADCINA2, Vbst
102 AdcRegs.ADCSOC5CTL.bit.CHSEL  = 0x0a; // set SOC5 channel select to
       ADCINB2, Vbk
103
104 AdcRegs.ADCSOC2CTL.bit.TRIGSEL  = 0x09; // set SOC2 start trigger on
       EPWM3A
105 AdcRegs.ADCSOC3CTL.bit.TRIGSEL  = 0x09; // set SOC3 start trigger on
       EPWM3A
106 AdcRegs.ADCSOC5CTL.bit.TRIGSEL  = 0x09; // set SOC5 start trigger on
       EPWM3A
107 AdcRegs.ADCSOC2CTL.bit.ACQPS  = ADC_ACQ; // set SOC2 S/H Window
108 AdcRegs.ADCSOC3CTL.bit.ACQPS  = ADC_ACQ; // set SOC3 S/H Window
109 AdcRegs.ADCSOC5CTL.bit.ACQPS  = ADC_ACQ; // set SOC5 S/H Window
110 EDIS;
```

The code of the main body of the program is shown as following.

```
// Efficiency-enhanced DAB control with F28069
// H. Chen
// ver. 1.2
// March 2016
// File name: main.c
// Description: main program file

#include "DSP28x_Project.h" // Device Headerfile from controlSUITE
#include "F28069_example.h" // Main include file from controlSUITE
#include "Serial_comm.h" // communication with computer for debug
#include "ModE_P3.h" // header file of the project
#include "CLAshared.h" // shared variables with CLA
#include <string.h>

// mode boundaries
#define DCXBH 1.5
#define DCXBL 1.44

// the time-critical interrupts run from ram
#pragma CODE_SECTION(cpu_timer0_isr,  "ramfuncs");
#pragma CODE_SECTION(adc1_isr,        "ramfuncs");
#pragma CODE_SECTION(adc2_isr,        "ramfuncs");
#pragma CODE_SECTION(adc3_isr,        "ramfuncs");

// Prototype statements for functions found within this file.
interrupt void adc1_isr(void);
interrupt void adc2_isr(void);
interrupt void adc3_isr(void);
interrupt void cpu_timer0_isr(void);

// Global variables
// buffers for communication
volatile Uint16 Vbstoutbuf[BUF_SIZE];
volatile Uint16 Vbkoutbuf[BUF_SIZE];
volatile Uint16 Voutbuf[BUF_SIZE];

Uint16 Sampleno, Samplecnt;

// variables CPU writes to CLA
#pragma DATA_SECTION(mode,   "CpuToCla1MsgRAM");
#pragma DATA_SECTION(DCXmode,   "CpuToCla1MsgRAM");
int32 mode, DCXmode;

```

```
44 //variables CLA writes to CPU
45 #pragma DATA_SECTION(Vbusf, "Cla1ToCpuMsgRAM");
46 #pragma DATA_SECTION(Vbuckf, "Cla1ToCpuMsgRAM");
47 #pragma DATA_SECTION(Vboostf, "Cla1ToCpuMsgRAM");
48 float32 Vbusf, Vbuckf, Vboostf;
49
50 void main(void) // entry function
51 {
52   Uint16 cmd; // for communication
53
54   // initialization
55   InitSysCtrl();
56   InitGpio();
57
58   DINT;
59   InitPieCtrl();
60   IER = 0x0000;
61   IFR = 0x0000;
62   InitPieVectTable();
63
64   // copy the time-critical code from flash to ram
65   memcpy(&RamfuncsRunStart, &RamfuncsLoadStart, (Uint32)&
        RamfuncsLoadSize);
66   InitFlash();
67
68   // Interrupts that are used in this example are re-mapped to
69   // ISR functions found within this file.
70   EALLOW; // This is needed to write to EALLOW protected register
71   PieVectTable.TINT0 = &cpu_timer0_isr;
72   PieVectTable.ADCINT1 = &adc1_isr;
73   PieVectTable.ADCINT2 = &adc2_isr;
74   PieVectTable.ADCINT3 = &adc3_isr;
75   EDIS; // This is needed to disable write to EALLOW protected
        registers
76
77   InitEPwmGpio_OL(); // initialize PWM IO
78
79   InitSci(); // initialize communication module
80
81   InitCpuTimers(); // initialize timer0
82   // Configure CPU-Timer 0 to interrupt every 100 milliseconds:
83   ConfigCpuTimer(&CpuTimer0, 90, (int32)100000);
84
85   PieCtrlRegs.PIEIER1.bit.INTx1 = 1;  // Enable INT 10.1 in the PIE
        ADCINT1
86   PieCtrlRegs.PIEIER1.bit.INTx2 = 1;  // Enable INT 10.2 in the PIE
        ADCINT2
```

```
87    PieCtrlRegs.PIEIER10.bit.INTx3 = 1; // Enable INT 10.3 in the PIE
          ADCINT3
88    PieCtrlRegs.PIEIER1.bit.INTx7 = 1;  // Enable INT 1.7 in the PIE
          TINT0
89
90    init_cla(); // initialize CLA
91    InitAdc();  // Configure ADC
92
93    IER |= M_INT1;  // Enable CPU Interrupt 1
94    IER |= M_INT10; // Enable CPU Interrupt 10
95    SetDBGIER(IER); // Configure the DBGIER for realtime debug
96    asm("␣CLRC␣INTM,␣DBGM"); // Enable global interrupts and realtime
          debug
97
98    // Use write-only instruction to set TSS bit = 0, start Timer0
99    CpuTimer0Regs.TCR.all = 0x4000;
100
101   Sampleno = BUF_SIZE;
102   Samplecnt = 0;
103   memset((void*)Voutbuf, 0, BUF_SIZE);
104   memset((void*)Vbstoutbuf, 0, BUF_SIZE);
105   memset((void*)Vbkoutbuf, 0, BUF_SIZE);
106
107   Vin = 0;
108   mode = 1;
109   DCXmode = 0;
110   start_cla();
111
112   while(1){ // main loop for communication
113     cmd = get_cmd16();
114     parse_cmd(cmd);
115   }
116 }
117
118 // timer0 ISR for resonant mode control
119 interrupt void cpu_timer0_isr(void)
120 {
121   float32 VDCXin, VDCXout;
122   Uint16 DCXDBp, DCXDBs;
123
124   // calculate DCX input / output voltages
125   VDCXin = Vbuckf;
126   VDCXout = Vbusf*G1 - Vboostf;
127
128   // adjust modes
129   if (DCXmode == 0) {
130     // mode 0 uses a different mode boundary
```

```
131     if (VDCXout > VDCXin * 1.51)
132       DCXmode++;
133   }
134   else {
135     if (VDCXout > VDCXin * DCXBH) {
136       if (DCXmode < 5)
137         DCXmode++;
138     }
139     else {
140       if (VDCXout < VDCXin * DCXBL) {
141         DCXmode--;
142       }
143     }
144   }
145
146   // determine dead-time
147   switch(DCXmode) {
148     case 0:
149       DCXDBp = 37;
150       DCXDBs = 127;
151       break;
152     case 1:
153       DCXDBp = 161;
154       DCXDBs = 251;
155       break;
156     case 2:
157       DCXDBp = 268;
158       DCXDBs = 358;
159       break;
160     case 3:
161       DCXDBp = 406;
162       DCXDBs = 496;
163       break;
164     case 4:
165       DCXDBp = 581;
166       DCXDBs = 671;
167       break;
168     case 5:
169       DCXDBp = 834;
170       DCXDBs = 924;
171       break;
172     default:
173       DCXDBp = 37;
174       DCXDBs = 127;
175   }
176
177   // write dead-time to PWM channels
```

```
178   if (mode == 1) {
179     EALLOW;
180     EPwm3Regs.DBRED = DCXDBp;
181     EPwm3Regs.DBFED = DCXDBp;
182     EPwm4Regs.DBRED = DCXDBp;
183     EPwm4Regs.DBFED = DCXDBp;
184     EPwm5Regs.DBRED = DCXDBs;
185     EPwm5Regs.DBFED = DCXDBs;
186     EDIS;
187   }
188   // Acknowledge this interrupt to receive more interrupts from group 1
189   PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;
190 }
191
192 // ADC1 ISR stores readings for communication
193 interrupt void  adc1_isr(void)
194 {
195   if (Sampleno > 0) {
196     Samplecnt++;
197     if (Samplecnt > Sampleno) {
198       Samplecnt = 0;
199       Sampleno = 0;
200     }
201     else {
202       Vbstoutbuf[Samplecnt-1] = (Uint16)Vboostf;
203       Vbkoutbuf[Samplecnt-1] = (Uint16)Vbuckf;
204       Voutbuf[Samplecnt-1] = (Uint16)Vbusf;
205     }
206   }
207   AdcRegs.ADCINTFLGCLR.bit.ADCINT1 = 1;   //Clear ADCINT1 flag
        reinitialize for next SOC
208   PieCtrlRegs.PIEACK.all = PIEACK_GROUP1; // Acknowledge interrupt to
        PIE
209 }
210
211 interrupt void  adc2_isr(void)
212 {
213   AdcRegs.ADCINTFLGCLR.bit.ADCINT2 = 1;   //Clear ADCINT2 flag
        reinitialize for next SOC
214   PieCtrlRegs.PIEACK.all = PIEACK_GROUP1; // Acknowledge interrupt to
        PIE
215 }
216
217 interrupt void  adc3_isr(void)
218 {
219   AdcRegs.ADCINTFLGCLR.bit.ADCINT3 = 1;   //Clear ADCINT3 flag
        reinitialize for next SOC
```

```
220   PieCtrlRegs.PIEACK.all = PIEACK_GROUP10; // Acknowledge interrupt to
          PIE
221 }
```

The entry function `main()` initializes various peripherals and variables, and then enters an infinite polling loop, which waits for commands from the serial communication interface (SCI) for debug purpose. The global variable `mode` controls the behavior of the controller: when `mode` = 0, the controller operates in open loop, and when `mode` = 1, the controller operates in close loop.

The light load resonant mode control is implemented in the interrupt service routing (ISR) of timer0 `cpu_timer0_isr()`. (The three ISRs for ADCs are only for debug purpose, and does not affect the operation of the controller.) This ISR is triggered every 100 ms. It checks the converter voltage conversion ratio, updates the resonant mode number `DCXmode` and its corresponding dead-time for each PWM channels. The mode boundary is defined by constants `DCXBH` and `DCXBL`, except the boundary that transits from mode 0 to mode 1 is defined separately. If found to be necessary, it is possible to define different boundaries for each mode transition.

The input signals used by `cpu_timer0_isr` are not directly read from the ADC. To eliminate the mode jitter due to the noise in ADC, all ADC signals are digitally filtered at first. These digital filters are implemented in the control law accelerator (CLA) module, which is an auxiliary 32-bit float-point DSP inside the micro-controller. In the TMS320F28069, the CLA module supports up to eight tasks. Each task is a segment of code that is executed once triggered by software or by external events. In this controller, the CLA task 1 – 3 are configured to be triggered by the ADC interrupts 1 – 3, as tabulated in Table B.2. It is implemented in the following code segments:

```
68   Cla1Regs.MPISRCSEL1.bit.PERINT1SEL  = CLA_INT1_ADCINT1;
69   Cla1Regs.MPISRCSEL1.bit.PERINT2SEL  = CLA_INT2_ADCINT2;
70   Cla1Regs.MPISRCSEL1.bit.PERINT3SEL  = CLA_INT3_ADCINT3;
71   Cla1Regs.MPISRCSEL1.bit.PERINT4SEL  = CLA_INT4_NONE;
72   Cla1Regs.MPISRCSEL1.bit.PERINT5SEL  = CLA_INT5_NONE;
73   Cla1Regs.MPISRCSEL1.bit.PERINT6SEL  = CLA_INT6_NONE;
74   Cla1Regs.MPISRCSEL1.bit.PERINT7SEL  = CLA_INT7_NONE;
75   Cla1Regs.MPISRCSEL1.bit.PERINT8SEL  = CLA_INT8_NONE;
```

Because the internal variables used by CLA cannot be directly accessed from the CPU, the

CLA task 8 is reserved to reset these internal variables. Therefore, to start the CLA module, the following code is executed:

```
109 void start_cla(void) {
110   EALLOW;
111   Cla1Regs.MIER.all = (M_INT8 | M_INT1 | M_INT2 | M_INT3);
112   EDIS;
113   Cla1ForceTask8();
114 }
```

The complete code which is executed in the CLA module is documented as following.

```
1  /*
2   * File name: control.cla
3   *
4   *      Author: H. Chen
5   *      March 2016
6   */
7
8  #include "DSP28x_Project.h"
9  #include "CLAshared.h"
10
11 #pragma DATA_SECTION(Vbus,     "ClaDataRam0");
12 #pragma DATA_SECTION(Vbuck,    "ClaDataRam0");
13 #pragma DATA_SECTION(Vboost,   "ClaDataRam0");
14 #pragma DATA_SECTION(Verr,     "ClaDataRam0");
15 #pragma DATA_SECTION(phi,      "ClaDataRam0");
16 #pragma DATA_SECTION(Vbusf1,   "ClaDataRam0");
17 #pragma DATA_SECTION(Vbusf2,   "ClaDataRam0");
18 #pragma DATA_SECTION(Vbus1,    "ClaDataRam0");
19 #pragma DATA_SECTION(Vbus2,    "ClaDataRam0");
20 #pragma DATA_SECTION(Vbuckf1,  "ClaDataRam0");
21 #pragma DATA_SECTION(Vbuckf2,  "ClaDataRam0");
22 #pragma DATA_SECTION(Vbuck1,   "ClaDataRam0");
23 #pragma DATA_SECTION(Vbuck2,   "ClaDataRam0");
24 #pragma DATA_SECTION(Vboostf1, "ClaDataRam0");
25 #pragma DATA_SECTION(Vboostf2, "ClaDataRam0");
26 #pragma DATA_SECTION(Vboost1,  "ClaDataRam0");
27 #pragma DATA_SECTION(Vboost2,  "ClaDataRam0");
28
29 volatile float32 Vbus, Vbusf1, Vbusf2, Vbus1, Vbus2;
30 volatile float32 Vbuck, Vbuckf1, Vbuckf2, Vbuck1, Vbuck2;
31 volatile float32 Vboost, Vboostf1, Vboostf2, Vboost1, Vboost2;
32 volatile float32 Verr, phi;
33
34 __interrupt void Cla1Task1 ( void )
35 {
```

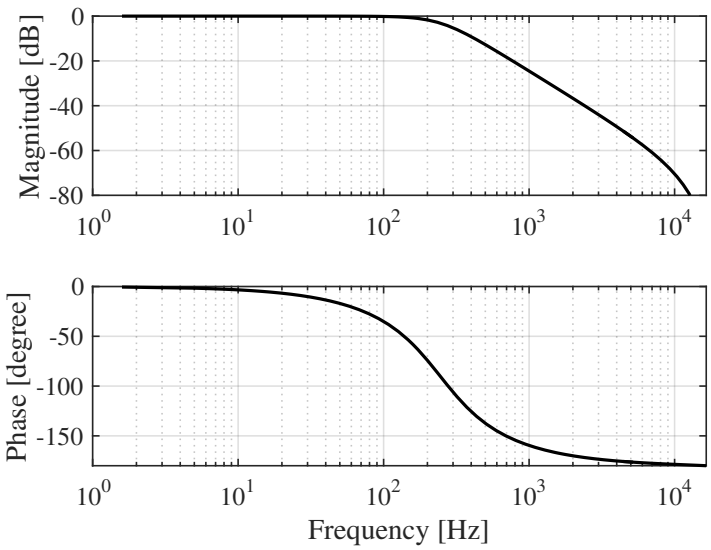
```
36 // filter for Vbuck
37   Vbuck = (float32)AdcResult.ADCRESULT5;
38   Vbuckf = 0.0005*Vbuck2 + 0.0011*Vbuck1 + 0.0005*Vbuck - 0.9355*
        Vbuckf2 + 1.9334*Vbuckf1;
39   Vbuck2 = Vbuck1;
40   Vbuck1 = Vbuck;
41   Vbuckf2 = Vbuckf1;
42   Vbuckf1 = Vbuckf;
43 }
44
45 __interrupt void Cla1Task2 ( void )
46 {
47 // filter for Vbus
48   Vbus = (float32)AdcResult.ADCRESULT2;
49   Vbusf = 0.0005*Vbus2 + 0.0011*Vbus1 + 0.0005*Vbus - 0.9355*Vbusf2 +
        1.9334*Vbusf1;
50   Vbus2 = Vbus1;
51   Vbus1 = Vbus;
52   Vbusf2 = Vbusf1;
53   Vbusf1 = Vbusf;
54 }
55 __interrupt void Cla1Task3 ( void )
56 {
57   float32 Verr2, Vout1;
58
59 // filter for Vboost
60   Vboost = (float32)AdcResult.ADCRESULT3;
61   Vboostf = 0.0005*Vboost2 + 0.0011*Vboost1 + 0.0005*Vboost - 0.9355*
        Vboostf2 + 1.9334*Vboostf1;
62   Vboost2 = Vboost1;
63   Vboost1 = Vboost;
64   Vboostf2 = Vboostf1;
65   Vboostf1 = Vboostf;
66
67   Vout1 = Vbus*G1 - Vboost;
68   Verr2 = Verr;
69   Verr = Vbuck * VGAIN - Vout1;
70
71 // phase-shift control
72   if (mode == 1) {
73     if (DCXmode == 0) {
74       // PI compensator
75       phi = K1 * Verr + K2 * Verr2 + phi;
76       // saturation
77       if (phi < 0L)
78         phi = 0L;
79       else {
```

```
80          if (phi > 500L)
81            phi = 500L;
82        }
83        EPwm5Regs.TBPHS.half.TBPHS = (Uint16)(phi);
84      }
85      else {
86        EPwm5Regs.TBPHS.half.TBPHS = 0;
87      }
88    }
89  }
90  __interrupt void Cla1Task4 ( void ) { }
91  __interrupt void Cla1Task5 ( void ) { }
92  __interrupt void Cla1Task6 ( void ) { }
93  __interrupt void Cla1Task7 ( void ) { }
94
95  __interrupt void Cla1Task8 ( void )
96  {
97  // initialization
98    Vbus = 0;
99    Vbus1 = 0;
100   Vbus2 = 0;
101   Vbusf1 = 0;
102   Vbusf2 = 0;
103   Vbuck = 0;
104   Vbuck1 = 0;
105   Vbuck2 = 0;
106   Vbuckf1 = 0;
107   Vbuckf2 = 0;
108   Vboost = 0;
109   Vboost1 = 0;
110   Vboost2 = 0;
111   Vboostf1 = 0;
112   Vboostf2 = 0;
113   Verr = 0;
114   phi = 0;
115 }
```

The CLA Task 1, 2, and the first nine lines in Task 3 implement three digital filters to filter the ADC signals. Based on the observation on the frequency spectrum of the ADC noise, the filters are designed as second order Butterworth filters. Fig. B.1 plots the frequency response of the filter. At the 10 Hz update rate of the timer0, the digital filter has flat frequency response with almost 0° phase lag.

The other half of the CLA task 3 implements the phase-shift controller, which regulates the

Figure B.1: Frequency response of the digital filter



voltage conversion ratio to `VGAIN`. The controller is only active when `DCXmode` = 0, otherwise it is frozen with constant phase shift `TBPHS` = 0. The phase-shift controller is implemented as a PI compensator with saturation. Because CLA task 3 is triggered after every ADC conversion in channel A2, the update rate of the phase-shift controller is the same as the converter switching frequency. Because of the large phase lag at high frequency, the filtered signals are not suitable for the PI compensator in the phase-shift controller. Therefore, the phase-shift controller uses the raw ADC input signals, and relies on its internal integrator to attenuate the ADC noise. The saturation block limits the phase shift between zero and an arbitrary upper bound 500. Notice that because the saturation function is implemented inside the PI compensator, it naturally achieves the anti-windup function.

The CLA task 8 is a simple initialization task that resets all the internal variables which have memory.