

Optimization of Active-Bridge Based Modular Power Converters

by

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Thesis directed by Prof. Prof. Dragan Maksimović

Modularization is one of the essential concepts used in today's power electronics integration. Modular converters are often realized based on active bridges, arranged around high-frequency passive components. Due to soft-switching properties, these converters feature high efficiency and high power density, especially at the nominal conversion ratio. This thesis covers optimization of the aforementioned converters from different angles, including topology configuration, selection of semiconductor devices, modulation strategies, as well as optimization and integration of magnetic components. The thesis is organized into two parts based on different target applications.

The first part of the thesis considers the design and optimization of stacked active bridge (SAB) converters for high-conversion ratio dc-to-dc applications. Firstly, a transformerless high step-down SAB dc-dc converter is introduced. The SAB converter consists of series-stacked, capacitively coupled inverter modules and parallel-connected rectifier modules. The nominal step-down conversion ratio is determined by the number of inverter modules, while the output current capability scales with the number of paralleled rectifier modules. SAB operating principles, including phase-shift control and soft switching, achieved through series inductors, are similar to those of transformer-isolated dual active bridge (DAB) converters. It is found that the best size-versus-loss trade-off is achieved by the integration of the series inductors on a custom core. Furthermore, it is shown how soft switching contributes to natural voltage sharing among the series-stacked inverter modules. The approach is verified by experimental results on a 400-to-48 V, 3 kW SAB prototype using GaN devices and featuring 400 W/in³ power density. A flat efficiency curve is obtained, with 99% peak efficiency, 97.5% full-load efficiency, and 98% efficiency at 20% load. Second, a galvanic isolated version of the SAB converter is discussed. To achieve galvanic isolation, transformers are inserted between the inverters and rectifier bridges. The nominal step-down conversion ratio is

determined by the number of inverter modules and the turns ratio of the transformer. In order to reduce the footprint of the magnetic components, the transformers are coupled on a single core, and the series inductances are realized as controllable leakage inductances within the same magnetic structure using a novel custom core and planar winding arrangement, a solution unique to the iSAB configuration. The approach is verified by experimental results on a 400-to-48 V, 3 kW, 400 kHz iSAB prototype using GaN devices and having 96.7% peak efficiency.

The second part of the thesis is centered around the topic of modular SiC-based string inverters for medium-voltage transformer-less photovoltaic (PV) systems. The interface of low-voltage (LV) DC to medium-voltage (MV) three-phase AC grid is often based on series-stackable modular converter architectures. To minimize energy storage requirements, it is advantageous to employ a quadruple active bridge (QAB) stage operating as a “dc transformer” (DCX) in each stackable module. The QAB stage offers three isolated dc link voltages, which then allow flexible stacking of three single-phase dc-to-ac inverter stages. Each of the module phases processes a pulsating power having a component at twice the line frequency. This presents a challenge in maintaining zero-voltage switching (ZVS) on the secondary sides of the QAB during low-power portions of the line cycle. The design of the QAB stage is covered in this thesis. A detailed analysis of ZVS switching waveforms is presented, including the effects of nonlinear device capacitances. It is shown how ZVS can be achieved at all times using a relatively small circulating current provided by the magnetizing inductance of the high-frequency transformer. Analytical expressions are given for the optimal values of the magnetizing inductance and the dead times of the QAB primary and secondary bridges. The approach is verified by experimental results on a 1 kV, 10 kW SiC-based prototype, demonstrating a relatively flat efficiency curve with a peak efficiency of 97.1% at 75% load.

Dedication

To my parents.

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Contents

Chapter

1	Introduction	1
1.1	Trends and Challenges in Advanced Power Electronics Converters	1
1.2	DC Transformers in Power Electronics	2
1.3	Introduction to Stacked Active Bridge Converters (Part I)	6
1.4	Introduction to Modular SiC Based String Inverters for Medium-voltage Transformer-less PV Systems (Part II)	8
1.5	Thesis Outline	12
 Part I - Gallium Nitride (GaN) based High Step-Down Stacked Active Bridge Converters		
2	Scaling of Semiconductor devices in Stacked Active Bridges	15
2.1	Modularization of active-bridge based dc-transformers	15
2.2	Voltage Scaling of Semiconductor Devices with Splitting the High-Voltage Side with SAB - Theoretical Perspective	17
2.3	Voltage Scaling of Semiconductor Devices with Splitting the High- Voltage Side with SAB - Revisited	18
2.4	Energy stored in SAB	20
2.5	Chapter Summary and Conclusions	21

3	400 V-to-48 V Stacked Active Bridge Converter	22
3.1	SAB converter operation	24
3.2	Capacitor voltage balancing	26
3.3	Realization of the series inductors	31
3.3.1	Loss modeling, design optimization, and comparison of inductor realizations .	33
3.3.2	Magnetic structure with four coupled inductors	35
3.3.3	Effects of inductor coupling on the capacitor voltage balancing	38
3.4	Experimental results	38
3.5	Chapter Summary and Conclusions	48
4	400 V-to-48 V Transformer-Isolated Stacked Active Bridge Converter with Integrated Mag-	
	netics	50
4.1	iSAB Integrated Magnetics Structure	52
4.1.1	Core Geometry	52
4.1.2	Primary Side Winding Arrangement and the Magnetizing Flux	52
4.1.3	Secondary-Side Winding Arrangement and the Magnetizing Flux	55
4.2	Integrated Magnetics Design using Finite Element Analysis (FEA)	56
4.3	Experimental Results	57
4.4	Chapter Summary and Conclusions	57
 Part II - Modular Silicon Carbide (SiC) Based String Inverters for Medium-voltage Transformerless PV Systems		
5	Design and Optimization of a Quadruple Active Bridge DCX Stage in a DC to Three-Phase AC Module for Medium-Voltage Grid Integration	62
5.1	Introduction	62
5.1.1	Control Signals for Zero Voltage Switching at Zero Instantaneous Power Transfer in One Phase	66

5.2	ZVS Sequence Analysis Neglecting the Parasitic Capacitance of the Series Inductor .	67
5.2.1	Zero Voltage Switching at Zero Instantaneous Power Transfer in One Phase .	67
5.2.2	Experimental results	75
5.2.3	Summary of the Section	80
5.3	ZVS Sequence Analysis Considering the Parasitic Capacitance of the Series Inductor	80
5.3.1	Zero voltage switching at zero instantaneous power transfer in one phase . . .	80
5.3.2	Parameter Selection for Minimum Peak Magnetizing Current	83
5.3.3	Sensitivity to parameter variations	90
5.4	Design optimization	91
5.4.1	Active-bridge conduction losses	93
5.4.2	Loss in the magnetic components	94
5.4.3	Total modeled loss	97
5.5	Experimental results	98
5.5.1	Design validation	100
5.5.2	Efficiency comparison against a conventional design using a large magnetizing inductance	105
5.5.3	Efficiency and loss breakdown	108
5.6	Conclusions	109
6	Conclusions and Future Work	111
6.1	Thesis Summary and Conclusions	111
6.2	Future Work Directions	113

Bibliography	117
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Appendix

A	Derivation of Relations Between Parameters Mismatch and Voltage Imbalance Between The Modules in SAB	125
B	Loss Modelling in SAB	127
B.1	Inductor loss	127
B.1.1	Copper loss	127
B.1.2	Core loss	127
B.2	Semiconductor device losses	128
B.2.1	Conduction loss	128
B.2.2	Turn-on loss	128
B.2.3	Turn-off loss	128
B.3	PCB losses	129

Tables

Table

3.1	Components and parameter values in the 400-to-48 V, 3 kW SAB prototype	39
3.2	Experimentally measured imbalance of the inverter input dc voltages with respect to the nominal value of $V_{IN}/4 = 100$ V	43
3.3	Delay mismatch introduced by the gate driver (LMG1210RVRT) and the digital isolator (SN74LVC2G17DBVT)	43
3.4	Comparison of 400-to-48 V, 3 kW prototypes	48
5.1	Time instants of the switching sequence during ZVS transition	67
5.2	Time intervals of the switching sequence during ZVS transition	67
5.3	System specifications and circuit parameters	69
5.4	Time instants of the approximated switching sequence	73
5.5	Time intervals of the approximated switching sequence	73
5.6	Experimental prototype parameters	75
5.7	Design parameters	76
5.8	Time instants of the switching sequence during ZVS transition	82
5.9	Time intervals of the switching sequence during ZVS transition	82
5.10	Experimental prototype parameters	90
5.11	Capacitances in the experimental prototype	91
5.12	Components used in the hardware prototype	100

5.13 Dead times, magnetizing inductance, and maximum phase shift in the experimental prototype	105
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Figures

Figure

1.1	Applications with high demand of advanced power electronics systems: data centers, smart homes, solar farms, and electric vehicle charging stations [12].	2
1.2	Turn-on and turn-off trajectory in drain to source current vs. voltage plane for hard and soft switching transitions.	3
1.3	Topology that represents an example of a galvanically-isolated high step-down “dc transformer”.	4
1.4	DAB and SRC ac currents at nominal conversion ratio.	5
1.5	Topology that represents a non-isolated example of a high step-down “dc transformer”.	6
1.6	Stacked active bridge (SAB) dc-dc converter comprising of 4 series-stacked, capacitively coupled half-bridge inverter modules and 2 parallel-connected full-bridge rectifier modules.	7
1.7	Traditional LVDC to MVAC architecture using line frequency transformer.	9
1.8	Modular multilevel architectures for interfacing LVDC to MVAC [16].	10
1.9	Modular multilevel architecture for interfacing LVDC to MVAC based on a three-phase module. The module is based on QAB dc-dc converter that provides galvanic isolation between the phases.	11
2.1	Modular connection of active bridges.	16
2.2	Voltage scaling of the RSP.	19

2.3	Scaling of the normalized conduction loss of the SAB with blocking voltage of the devices used in the stack.	20
3.1	Stacked active bridge (SAB) dc-dc converter comprising $n = 4$ series-stacked, capacitively coupled half-bridge inverter modules and $m = 2$ parallel-connected full-bridge rectifier modules.	23
3.2	Control signals c_I , $\overline{c_I}$ for the inverter modules, and c_R , $\overline{c_R}$, for the rectifier modules, together with the inductor currents $i_{1..4}$ in the SAB converter of Fig. 3.1.	25
3.3	SAB converter with two inverter modules having a timing mismatch between the control signals $c_{I,1}$ and $c_{I,2}$	26
3.4	Control signals $c_{I,1}$, $\overline{c_{I,1}}$ and $c_{I,2}$, $\overline{c_{I,2}}$ for the inverter modules, and c_R , $\overline{c_R}$, for the rectifier modules, together with the input currents $i_{IN,1}$, $i_{IN,2}$, and the switching node voltages $v_{sw,1}$, $v_{sw,2}$ in the SAB converter of Fig. 3.3 under imbalanced conditions due to timing mismatches.	27
3.5	State-plane diagrams for the normalized switching node voltages $v_{sw,1}$, $v_{sw,2}$, and inductor currents i_1 , i_2 , corresponding to the waveforms under imbalanced condition shown in Fig. 3.4. The state-plane trajectories when the voltages are perfectly balanced are shown in light-gray color.	28
3.6	Voltage imbalance ΔV as a function of the timing mismatch $t_{\Delta\beta}$ between the control signals $c_{I,1}$ and $c_{I,2}$ in the SAB converter of Fig. 3.3, for different values of the half-bridge switch node capacitance C_{HB}	29
3.7	Voltage imbalance ΔV as a function of the inductance mismatch $\Delta L/L$, for different values of the half-bridge switch-node capacitance C_{HB}	30
3.8	Voltage imbalance ΔV as a function of the half-bridge switch-node capacitance mismatch $\Delta C_{HB}/C_{HB}$, where $C_{HB} = 2.4 \text{ nF}$	30
3.9	Four different realizations of the series inductors.	31

3.10	Four planar magnetic structures for implementation of the series inductors, corresponding to the realizations shown in Fig. 3.9. In the comparison, the total box volume of the magnetic structures is kept the same.	32
3.11	Single planar inductor dimensions.	33
3.12	Comparison of the magnetic structures in Fig. 3.10: total inductor loss as a function of the core center-post area A in the 400-to-48 V, 3 kW SAB converter operating at full power. The switching frequency is $f_{sw} = 400$ kHz.	34
3.13	Loss optimization of the magnetic structure with four coupled inductors (option (B)), shown in Fig. 3.10b: conduction and core losses are shown as functions of the core center-post area A , under the constraints that the total boxed volume and the aspect ratio W/H are fixed.	35
3.14	Flux density obtained using 3D FEA simulation in the magnetic structure with four coupled inductors operating at full load in the 3 kW, 400-to-48 V SAB converter. . .	36
3.15	Magnetic circuit models. Each winding has a single turn.	37
3.16	Photograph (top view) of the 3 kW, 400-to-48 V SAB prototype. The prototype box dimensions, including heat sinks, are $125 \text{ mm} \times 65 \text{ mm} \times 15 \text{ mm}$, which yields 400 W/in^3 power density.	39
3.17	A 3D model showing how the custom heat sinks are mounted on the SAB prototype PCB. The base of the heat sink is trimmed such that the heat-sink protrusions are in direct thermal contact with the top of the GaN devices.	40
3.18	Experimental waveforms in the 400-to-48 V SAB prototype operating at 3 kW: inverter 1 switch-node voltage $v_{1,sw}$, rectifier 1 switch-node voltage $v_{1,sw,out}$, and series inductor current i_1	40
3.19	Module voltages $v_{1..n}$, during the input power supply turn-on/off transients.	41
3.20	Experimental waveforms showing the switch-node voltages $v_{1..3,sw}$, and the series inductor current i_1 . Amplitudes of the switch-node voltages are the same, demonstrating that the inverter capacitor voltages are well balanced.	42

3.21	Theoretically predicted voltage imbalance ΔV as a function of the timing mismatch $t_{\Delta\beta}$ between the control signals $c_{I,1}$ and $c_{I,2}$ in the SAB converter with the half-bridge switch node capacitance $C_{HB} = 2.4nF$. The predicted range of ΔV is determined based on the maximum time delay mismatch given in Table 3.3.	42
3.22	Measured efficiency of the experimental SAB prototype, together with a model-predicted efficiency curve, as functions of the output power from 10% to 100%. . . .	43
3.23	Model-predicted loss budget and the total measured loss in the 3 kW SAB prototype operating from 10% to 100% of load.	44
3.24	Measured efficiency of the experimental SAB prototype, as a function of the output voltage from -20% to +20% of the nominal voltage, at fixed output power of 3 kW. . . .	45
3.25	Experimental waveforms in the SAB prototype operating at $\pm 20\%$ of the nominal output voltage at 3 kW: inverter 1 switch-node voltage $v_{1,sw}$, rectifier 1 switch-node voltage $v_{1,sw,out}$, and series inductor current i_1	46
3.26	Thermal images of the SAB prototype taken at 3 kW output power. The ambient temperature is 25°C	47
4.1	Isolated stacked active bridge (iSAB) dc-dc converter comprising $n = 4$ series-stacked, half-bridge inverters and $m = 2$ parallel-connected full-bridge rectifier modules. All transformers and series inductors are integrated on the same custom magnetic core with planar windings.	51
4.2	Integrated magnetics core and primary winding arrangement, together with illustration of the magnetizing flux path.	53
4.3	Winding arrangement of the secondary-side planar windings.	54
4.4	Leakage flux path.	55
4.5	FEA simulation of the integrated magnetics structure and iSAB current waveforms.	56
4.6	Photograph of the 3 kW, 400-to-48 V iSAB prototype.	58

4.7	Experimental waveforms in the 400-to-48 V iSAB prototype operating at 3 kW: inverter 1 switch-node voltage $v_{1,sw}$, rectifier 1 switch-node voltage $v_{1,sw,out}$, and series inductor current i_1	59
4.8	Measured efficiency of the experimental iSAB prototype as a functions of the output power from 10% to 100%.	59
5.1	System architecture with cascaded isolated inverter modules [4].The module configuration is shown in Fig. 5.2.	63
5.2	Transformer-isolated inverter module using a quadruple active bridge (QAB) dc-dc converter operated as a fixed-ratio “dc transformer” (DCX).	64
5.3	QAB switch control signals at the time when the secondary Phase A processes zero power.	66
5.4	Model-based waveforms of the ZVS transition at the zero power transfer instant for Phase A. Referring to Fig. 5.3, $T_3 = t_{ds}$ and $T_2 - T_1 = t_{dp}$	68
5.5	Equivalent circuits during ZVS transition at the zero power transfer instant for one of the phases.	71
5.6	Approximate equivalent circuits during ZVS transition.	72
5.7	Exact and approximate waveforms of the primary side switching-node voltage $nv_p(t)$ during Interval II.	72
5.8	State plane trajectory during interval I'.	73
5.9	600 V, 4 kW SiC-based experimental prototype.	75
5.10	State plane trajectory at the time Phase A power is zero. Experimental results are overlapped with solutions based on accurate and approximate models.	76
5.11	Quadruple active bridge primary and secondary currents.	77
5.12	Quadruple active bridge primary and secondary currents.	78
5.13	Efficiency measurements.	79

5.14	Model-based waveforms of the ZVS transition at the zero power transfer instant for Phase A. Referring to Fig. 5.3, $T_3 = t_{ds}$ and $T_2 - T_1 = t_{dp}$	81
5.15	Equivalent circuits during ZVS transition at the zero power transfer instant for one of the phases.	82
5.16	Half-bridge switching node device capacitance.	84
5.17	Approximate equivalent circuits during ZVS transition.	85
5.18	Exact and approximate waveforms of the primary-side switching-node voltage $nv_p(t)$ during Interval II.	87
5.19	State plane trajectory during intervals I' and II'.	88
5.20	Effects of the variation in the series inductance on the changes Δt_{sd} and ΔL_M in the design parameters.	91
5.21	Theoretical currents waveforms during a switching period.	92
5.22	Peak magnetizing current dependence on φ_m	92
5.23	RMS primary and secondary currents as functions of φ_m	93
5.24	H field magnitude in the planar high frequency transformer along y axis at one instant during a line cycle.	95
5.25	2D FEA simulation showing H field distribution in the planar high frequency transformer at a point of the line cycle.	96
5.26	3D model of the MV high frequency transformer used for finite-element analysis in Ansys Maxwell.	97
5.27	Component losses as functions of the maximum phase shift φ_m	98
5.28	Total loss as a function of φ_m	99
5.29	1 kV, 10 kW SiC-based prototype of the isolated DC to three-phase AC module. . . .	100
5.30	Phase A dc-link voltage V_A and the inverter output current $i_{A,LOAD}$, during a step change from 50% to 100% of load.	101
5.31	Quadruple active bridge primary and secondary currents.	102
5.32	Waveforms illustrating zero voltage switching at the zero power instant for phase A. .	103

5.33	State plane trajectory at the time Phase A power is zero. Experimental results are overlapped with solutions based on accurate and approximate models.	104
5.34	Experimentally measured loss for designs around the optimum φ_m together with the model-predicted optimization curve.	104
5.35	Model-predicted efficiency curves for the design with the optimized maximum phase shift, magnetizing inductance, and dead times, and for the conventional design with ungapped transformers.	105
5.36	Model-predicted loss breakdown of the QAB prototype using conventional design with ungapped transformers.	106
5.37	Loss of the experimental QAB prototype operating at 500 V dc link voltages using conventional design with ungapped transformers, together with a model-predicted loss breakdown.	106
5.38	Efficiency of the experimental QAB prototype using the optimized maximum phase shift, magnetizing inductance, and dead times, together with a model-predicted efficiency curve.	107
5.39	Loss of the experimental QAB prototype using the optimized maximum phase shift, magnetizing inductance, and dead times, together with a model-predicted loss breakdown.	108
5.40	Thermal images of the devices and one of the transformers in the experimental prototype operating at full power (10 kW) and at room ambient temperature, without any forced-air cooling.	109
6.1	Direct Power Converter (DPx).	114
6.2	Equivalent circuits and operating waveforms of DPx over the switching period. . . .	115
6.3	Modular, stacked active bridge direct power converter (SABDPx).	116

Chapter 1

Introduction

1.1 Trends and Challenges in Advanced Power Electronics Converters

Power Electronics (PE) is responsible for converting electric power from one form to another, which makes it an essential part of every electric system. Over 70% of electrical energy, today is processed by PE. This trend will continue to grow over the next few decades [1]. Moreover, it is projected that 40% of the overall worldwide energy consumption will be in the form of electricity by 2030. As illustrated in Fig. 1.1, some of the areas where the PE is exceedingly expanding include: data centers, telecommunication systems, smart homes, renewable energy systems, electrified vehicles etc.

Improvements in efficiency, and power density, as well as cost reduction, are the main factors that drive innovations in the design and optimization of power converters. Miniaturization of power converters is mainly driven by the rise in switching frequency, which leads to a reduction of energy stored in the passive components, namely inductors and capacitors [70]. The size reduction and high-frequency content further impose challenges in loss reduction and thermal management of passive components. The rise in the operating switching frequency also imposes challenges in the thermal management of semiconductor devices. Switching loss, which is caused by the overlap of drain to source voltage and current, as well as stored charge in the power device, proportionally increases with switching frequency. Power devices based on wide-bandgap (WBG) materials such as Gallium Nitride (GaN), and Silicon Carbide (SiC) have recently gained massive attention due to their high critical electric field, which leads to several orders of magnitude smaller specific

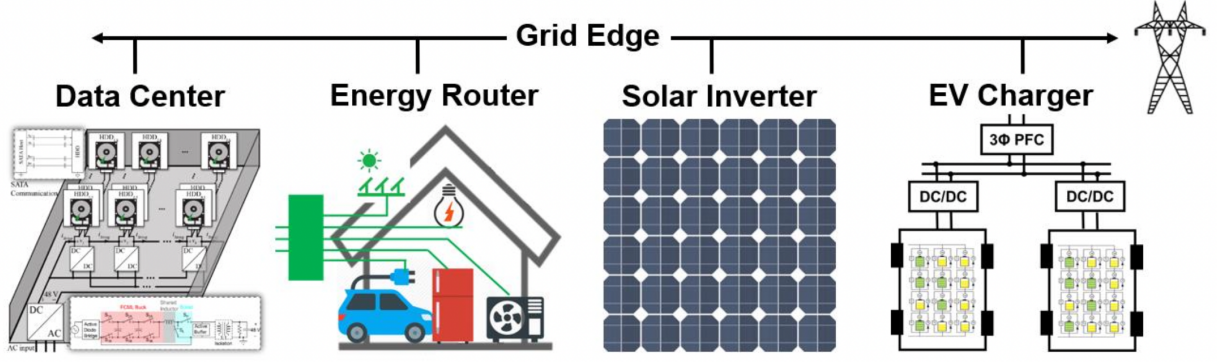


Figure 1.1: Applications with high demand of advanced power electronics systems: data centers, smart homes, solar farms, and electric vehicle charging stations [12].

on-resistance (RSP), compared to traditionally used silicon-based devices, greatly increasing the overall wafer yield. Reduction in RSP means that the same resistance of the channel can be achieved with a smaller die area, which reduces parasitic capacitances of the device, and therefore reduces switching loss [30]. Nevertheless, simply replacing the silicon devices with wide-bandgap devices does not fully utilize the potential benefits. Instead, proper selection of topology, together with devices, and design of passives results in a competent design for a particular application. Traditionally used hard-switched, pulse-width-modulated (PWM) converters have fundamentally limited efficiency with the amount of indirect power that is being processed. The amount of indirect power is directly proportional to the conversion ratio [91]. More indirect power results in larger ac losses in the converter. The ac losses scale up with higher operating frequencies, placing constraints on the miniaturization of the power converters, especially for high step-up/down applications.

1.2 DC Transformers in Power Electronics

The class of converters known as “dc transformer,” or “DCX” features superior performance in fixed, high conversion ratio applications [85, 97], in terms of efficiency and power density. Their main property is processing indirect power efficiently. This is achieved thanks to:

- **Soft-switching** of semiconductor devices. Soft-switching can take two major forms: zero-

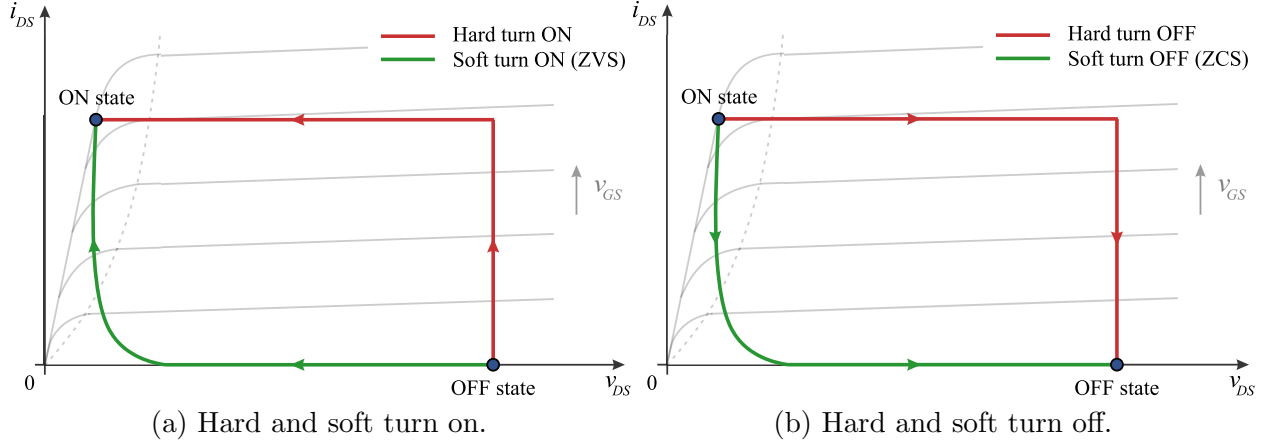


Figure 1.2: Turn-on and turn-off trajectory in drain to source current vs. voltage plane for hard and soft switching transitions.

voltage-switching (ZVS), or zero-current-switching (ZCS). ZVS event happens when drain to source voltage of the device drops to zero before the device starts turning on, i.e. before the current in the channel starts rising. Similarly, ZCS event occurs with the current falling down to zero, before turning the device off. Fig. 1.2 represents turn-on and turn-off trajectories in drain to source current vs. voltage plane for hard and soft switching transitions. Both ZVS and ZCS greatly reduce the overlap between the voltage and current of the device, compared to a hard-switching event. High voltage and low to moderate current applications can greatly benefit from ZVS, while ZCS is beneficial in low voltage high currents applications. Loss reduction offered by soft switching enables semiconductor devices to switch at higher frequencies, without significant loss increase.

- **AC inductors.** Inductors in traditional PWM converters carry both DC + AC components. A higher conversion ratio imposes higher volt-seconds across the inductor, which means that the value of the inductance needs to be increased, in order to keep the current ripple within the specified limits. Increased inductance leads to larger energy stored in the inductor $E_{ind} = \frac{LI_{ind}^2}{2}$. Contrary, ac inductors only need to store as much energy, as it is needed to charge/discharge parasitic capacitance of the switching node of the active

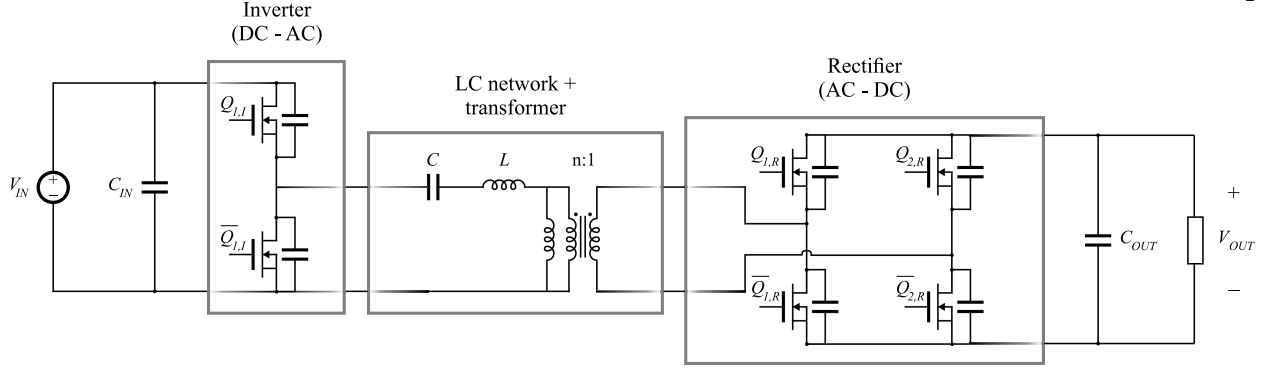


Figure 1.3: Topology that represents an example of a galvanically-isolated high step-down “dc transformer”.

bridge, to accommodate for the soft-switching of the devices. Storing less energy is in direct correlation with reduced loss, and size of the inductor.

A commonly used transformer-isolated DCX is presented in Fig. 1.3. The converter consists of three major parts:

- **Inverter** - converts DC power to AC power. To achieve ZVS of the inverter bridge, it is essential that the current coming out of the switching node, lags behind the switching node voltage, i.e. that the input impedance seen from the inverter needs to look inductive at the operating frequency. For example, at the turn-off event of the bottom switch, the direction of the current coming out of the switch node needs to be negative, so that the inductor current naturally charges up the parasitic capacitance of the switching node.
- **LC network + transformer** - determines the conversion ratio of the converter, together with the operating switching frequency, the phase shift between the active bridges, and the load. Aside from the current direction, it is necessary that inductive energy stored in the LC network is greater than the energy stored in the parasitic capacitance of the switching node of the active bridge, in order to complete ZVT.
- **Rectifier** - converts AC power back to DC power. Unlike in the case of the inverter bridge, the current entering the switching node of the rectifier bridge needs to lead the switching

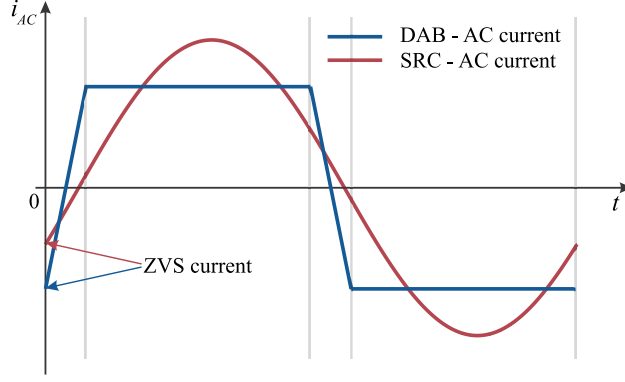


Figure 1.4: DAB and SRC ac currents at nominal conversion ratio.

node voltage in order to achieve ZVS.

Based on the control of active bridges, and LC network design, DCX could be realized as: Series-Resonant-Converter (SRC) [88, 90], Dual-Active-Bridge (DAB) [24, 20], LLC [92], etc. The DCX can be operated as an SRC if the resonant frequency of the series inductor L and capacitor C is relatively close to the switching frequency. If the resonant frequency is well below the switching frequency, the converter operates as a DAB. Fig. 1.4 shows ac currents through the series inductors in DAB and SRC converters. It can be noted that for the same power transfer, the DAB has smaller RMS currents and larger currents at ZVS transitions. Because the resonant frequency of SRC is higher compared to that of DAB, the inductance can be reduced, resulting in a smaller magnetic flux density (B). However, this further reduces the energy available for ZVS in the SRC. The efficiency can be optimized by running the converter between SRC and DAB operation, as discussed in [97]. By reducing the magnetizing inductance, DCX can be operated as an LLC. The ac currents in the LLC converter have a shape similar to the SRC current, shown in Fig.1.4, with superimposed circulating currents on the primary side, caused by the smaller magnetizing inductance. The circulating current in LLC greatly improves the ZVS range compared to SRC. On the other hand, the imbalance between the primary and secondary currents increases the loss in the transformer.

This thesis is focused on the design and optimization of modular converters based on active

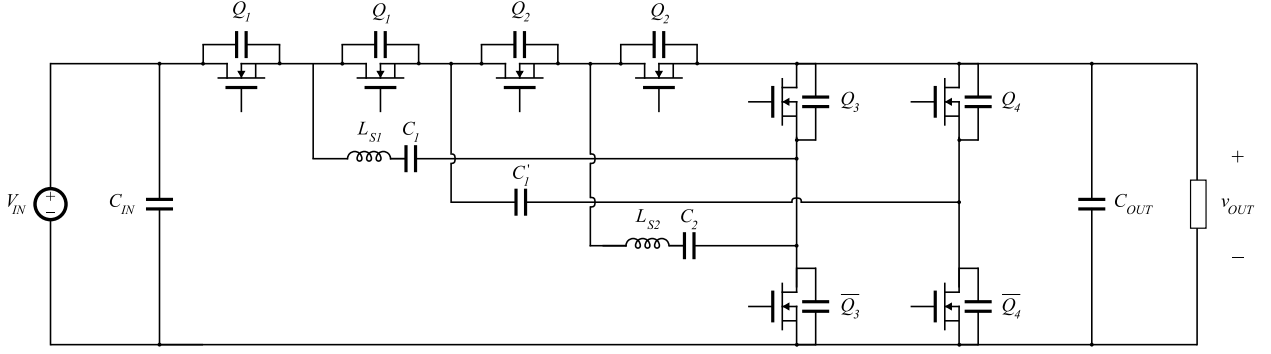


Figure 1.5: Topology that represents a non-isolated example of a high step-down “dc transformer”.

bridges that operate well above the resonance frequency. When operated as DCX, the converters feature trapezoidal flat-top ac currents, analogous to DAB current waveforms in Fig. 1.4. This mode of operation features major advantages such as ratio of mean to rms current close to one, wide ZVS range, and simple phase shift control with fixed switching frequency.

1.3 Introduction to Stacked Active Bridge Converters (Part I)

High-step-down or high-step-up dc-dc converters are usually based on transformer-isolated converters, shown in Fig. 1.3, such as dual active bridge (DAB) [20, 22, 95], or resonant LLC converters [92]. The high step-down or step-up transformer is one of the most significant contributors to the overall converter loss and size, which has prompted approaches based on splitting the transformer into stacked units [34, 33, 89, 36].

As an alternative to transformer-isolated converters, various hybrid switched capacitor (SC) based topologies, presented in Fig. 1.5, with inductive elements added to achieve soft charging and soft switching, have been considered for high step-down or step-up conversion applications. For example, switched tank converters [47, 57, 51] are hybrid SC-based converters that operate near the resonant frequency of the LC tank, similar to series resonant converters (SRC). Similar converter architectures, but operating at a switching frequency well above the resonance and with operating and control characteristics similar to DAB converters, are transformerless stacked active bridge (TSAB) converters [99, 98, 100]. Advantages of the above-resonance operation include a

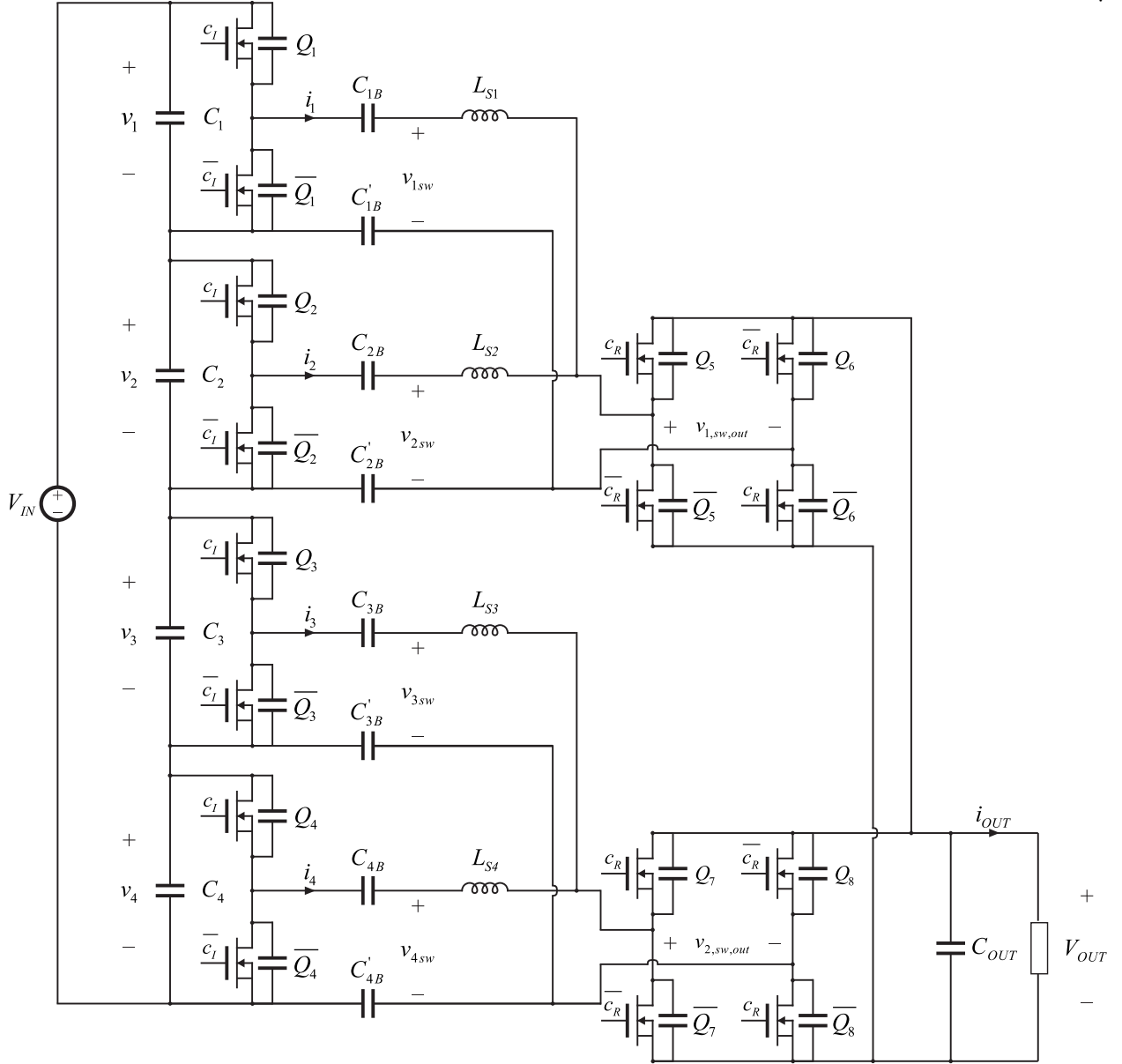


Figure 1.6: Stacked active bridge (SAB) dc-dc converter comprising of 4 series-stacked, capacitively coupled half-bridge inverter modules and 2 parallel-connected full-bridge rectifier modules.

wider ZVS range, reduced RMS currents, regulation capability through simple phase-shift control, and reduced sensitivity to LC parameter variations. On the other hand, operation near resonance leads to zero current switching (ZCS), which can be advantageous in high-current applications. Both switched-tank and TSAB converters exhibit partial hard switching of the inverter devices. An approach based on capacitively coupled active-bridge modules following the input-series output-

parallel (ISOP) architecture is shown in Fig. 1.6. This architecture inherently eliminates the partial hard switching problem by capacitively isolating the inverter from the rectifier bridges. Conduction losses on the rectifier devices present a challenge in high-current, high step-down converters. The ISOP architecture further enables paralleling the rectifier modules on the output dc side, which has advantages in terms of built-in current sharing and the absence of potentials for undesired parasitic oscillations compared to brute-force device paralleling [50].

Capacitively coupled ISOP converter configurations have been considered in telecom rectifier systems, employing SRC modules [5]. The work presented in [40] takes a similar approach for data center applications, using capacitively coupled LLC modules. In general, input-series configurations are realized by stacking the inverter active bridges, as shown in Fig. 3.1. Compared to traditional, single-module inverters, the stacked configuration requires a larger number of switching devices. However, the switching devices used in the stacked inverter configuration are rated at a lower voltage, allowing devices with a much-improved figure of merit (FOM). Splitting the input voltage has a fundamental advantage over single-module inverters in terms of the energy required for zero-voltage switching (ZVS). One may note that stacked inverter configurations can also be combined with isolation transformers, splitting the conversion task between the two stages, as shown in [3] and [42].

1.4 Introduction to Modular SiC Based String Inverters for Medium-voltage Transformer-less PV Systems (Part II)

Low-voltage (LV) dc to medium-voltage (MV) ac connection has traditionally been done by paralleling three-phase inverters at LVAC side and stepping the voltage up through line frequency MV transformer, as shown in Fig. 1.7. Hefty line frequency transformer, and considerable conduction loss on LVAC side in this configuration present motivation for looking into alternative approaches to LVDC to MVDC connection.

Modular power electronics architectures [43] have lately gained increased attention in electric vehicle (EV) dc charges [86, 54, 41, 15], power distribution for data centers [96], photovoltaic (PV)

power systems [39, 45, 4], and other applications. Fig. 1.8 shows the advancement of modular architectures. Fig. 1.8a consists of an MVDC bus and a modular inverter. The MV isolation is done on the DCDC side, using input-parallel-output-series (IPOS) configuration of isolated dc to dc converters. The isolated converters operate at medium to relatively high switching frequencies and therefore achieve a significant reduction in size compared to the line frequency transformer in the conventional design [44]. A popular choice for the MV inverter is Modular-Multilevel-Converter (MMC) [35, 53]. Each leg of the inverter is comprised of multiple submodules. The submodules are phase-shifted so that the effective switching frequency is increased, therefore reducing the filter size requirements [62, 63]. Various implementations of the modular inverter are presented in [76, 75]. However, the main disadvantage of this topology is that each of the submodules in the inverter leg contains a capacitor that has to store energy at twice the line frequency, which significantly impacts the size of the converter.

Another option is to avoid creating MV dc bus, by bringing the output of each individual isolated dc to dc converter directly to the submodule, as shown in Fig. 1.8b. This approach relaxes the requirements on the DC capacitance in the submodule. The pulsating power propagates through the isolated converter to the LVDC side. At the LVDC, the three-phase pulsating power cancels,

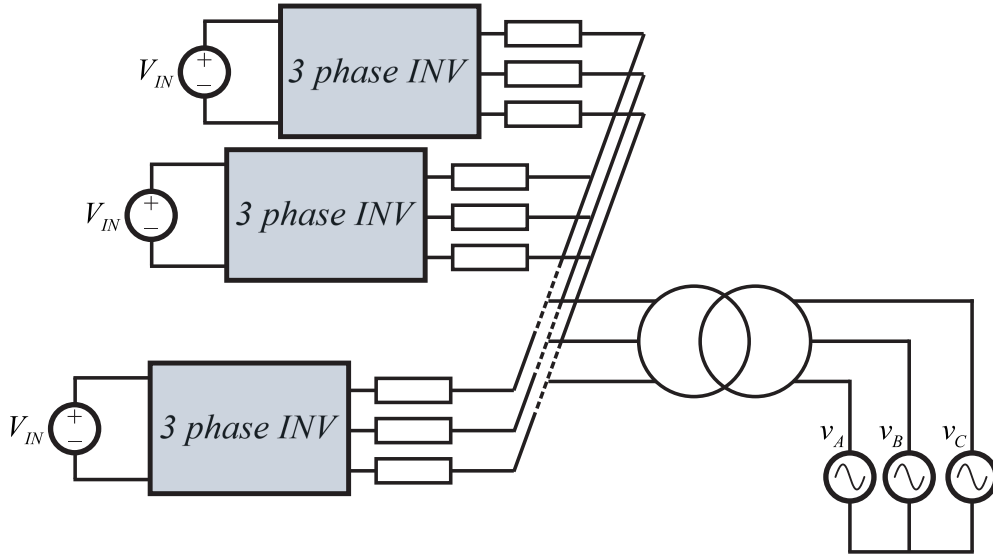
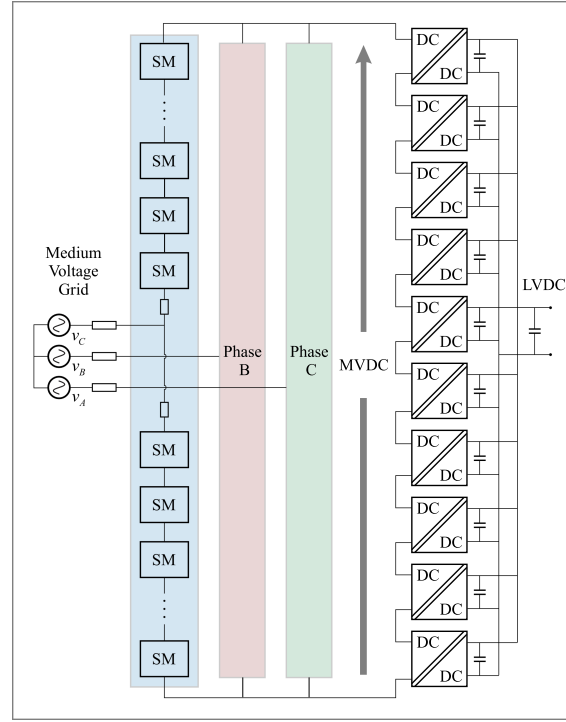
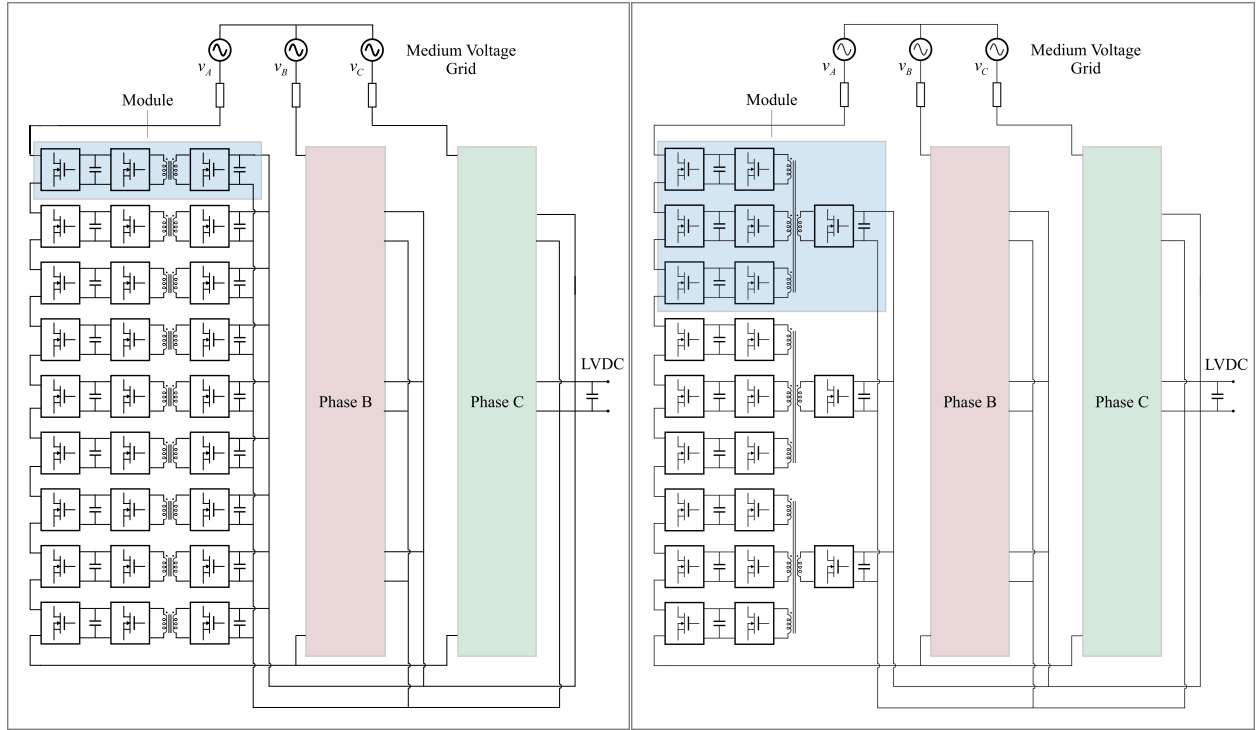


Figure 1.7: Traditional LVDC to MVAC architecture using line frequency transformer.



(a) LVDC to MVAC architecture 1.



(b) LVDC to MVAC architecture 2.

(c) LVDC to MVAC architecture 3.

Figure 1.8: Modular multilevel architectures for interfacing LVDC to MVAC [16].

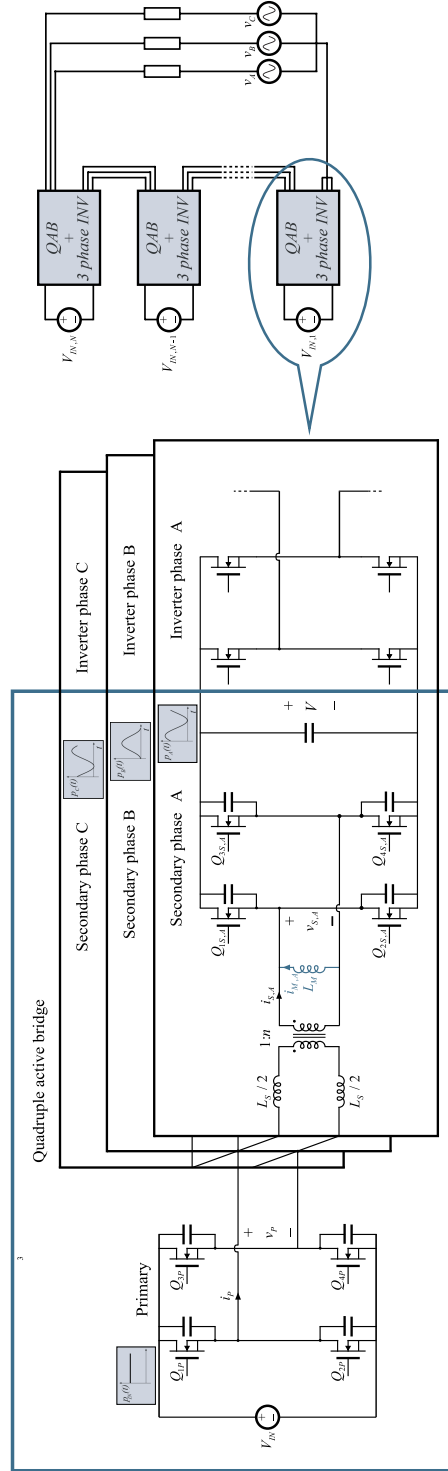


Figure 1.9: Modular multilevel architecture for interfacing LVDC to MVAC based on a three-phase module. The module is based on QAB dc/dc converter that provides galvanic isolation between the phases.

leaving only DC power.

The architecture can be further simplified by connecting multiple secondaries of the isolated dc to dc converter to one primary, as presented in Fig. 1.8c, reducing the component count.

The architecture can be further improved by coupling the secondaries from different phases to the same primary as presented in Fig. 1.9. This topology leverages the three-phase AC power cancelation within a module. The pulsating power propagates through the secondary sides of the isolated converter, but it cancels at the primary, therefore, the primary side bridge processes only DC power.

1.5 Thesis Outline

The thesis is divided into two parts, and it is organized as follows:

- **Part I** is focused on Gallium Nitride (GaN) based high step-down Stacked Active Bridge converters.

Chapter 2 examines voltage scaling of specific on-resistance (RSP) of semiconductor devices within SAB. It is shown how splitting the DC bus voltage across multiple modules in SAB, using lower voltage-rated devices, can be beneficial from the RSP standpoint. It is also shown how using a too large number of stacked modules can have detrimental effects on the overall conduction loss. This implies that an optimum number of stacked modules can be determined, to minimize the conduction loss.

Chapter 3 presents design optimization and analysis of a 400V to 48V, 3kW capacitively coupled (CC) SAB converter. The SAB configuration with CC enables elimination of the high step-down transformer. The only magnetic components in the converter are series inductors that are used for soft charging of blocking capacitors and soft switching of the semiconductor devices. Various implementations of the series inductors are compared in terms of loss and size. Effects of timing mismatch between gate pulses, and other parameters' tolerances in the circuit, on the amount of imbalance among the voltages of the

blocking capacitors, are determined considering zero-voltage transitions (ZVTs).

Chapter 4 discusses design of a 400V to 48V, 3kW galvanically isolated SAB converter. The SAB configuration is utilized to achieve the conversion ratio, while the transformer only needs to provide galvanic isolation. All the transformers and the inductors are integrated together into a single magnetic structure to shrink the footprint of the magnetic components.

- **Part II** is focused on Modular Silicon Carbide (SiC) Based String Inverters for Medium-voltage Transformer-less PV Systems.

Chapter 5 discusses a stackable modular architecture, where each module has a dc port and three isolated single-phase ac ports [4]. The MV isolation within the module is achieved through Quadruple Active Bridge (QAB) dc to dc converter. The QAB is comprised of one primary and three secondary active bridges arranged around three high-frequency transformers with MV isolation. Power through each of the secondary active bridges consists of both DC and AC components, while the three-phase AC components cancel out at the primary bridge. The pulsating component through the secondary bridges makes ZVS of the devices during low power transfer intervals challenging. The work presented in the thesis focuses on design optimization of the QAB with reduced magnetizing inductance for achieving ZVS of the secondary side devices throughout the line cycle.

Part I

Gallium Nitride (GaN) based High Step-Down Stacked Active Bridge Converters

Chapter 2

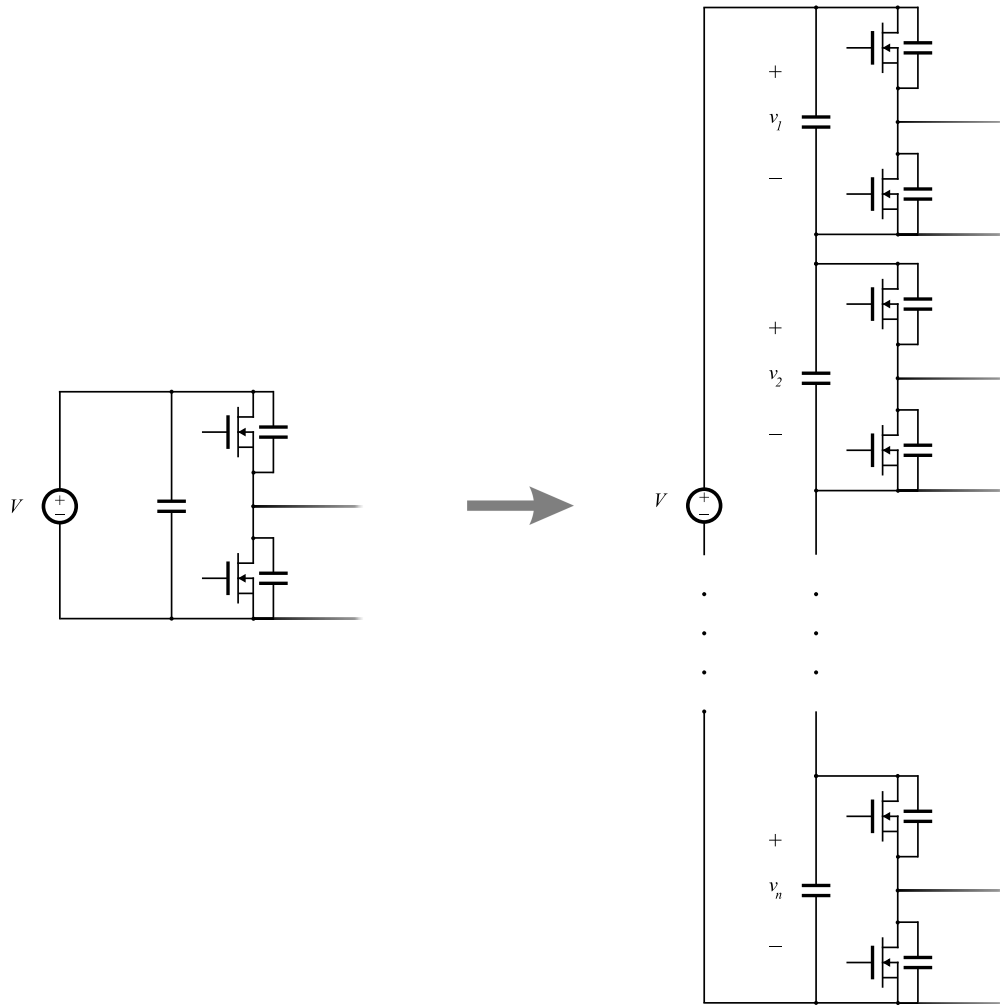
Scaling of Semiconductor devices in Stacked Active Bridges

This chapter introduces modular active-bridge based dc-transformers. The main focus is on the scaling of the semiconductor devices with a different number of series-stacked modules. Splitting the high-voltage side of the converter between a different number of modules enables the use of different voltage-rated devices. The effect of the number of modules on the performance of the stacked-active-bridge is discussed in this chapter.

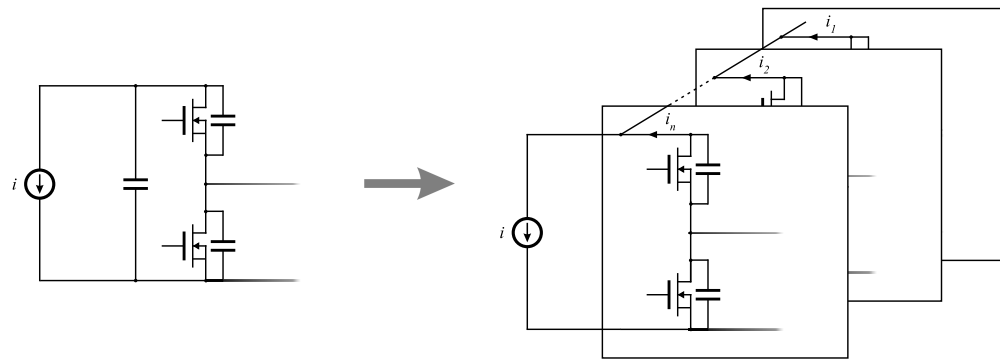
2.1 Modularization of active-bridge based dc-transformers

It can be observed from Fig. 1.3 that the converter is comprised of two distinguishable parts: active bridges (inverter and rectifier), and passive components.

- **Active Bridges** - are composed of semiconductor devices. In high conversion ratio applications, the high-voltage side is normally arranged in a half-bridge configuration, while the low-voltage side is normally arranged in a full-bridge configuration, as shown in Fig. 1.3. In order to maximize the utilization of semiconductor devices, the high voltage side can be split into multiple "modules" connected in series - Fig. 2.1a. This configuration is referred to as Stacked-Active-Bridge (SAB) further in the text. Similarly, the low voltage side can be split into multiple parallel connected modules - Fig. 2.1b.
- **Passive Components** - are connected between the active bridges. The optimization of passives is dependent on the converter mode of operation (SRC, DAB, LLC, etc.). Mod-



(a) Series stacking of high-voltage side active bridge.



(b) Parallel connection of low-voltage side active bridges.

Figure 2.1: Modular connection of active bridges.

ularization of active bridges can also lead to improvements in the design of passives. For example, integration of the magnetic components, or elimination of the transformer.

2.2 Voltage Scaling of Semiconductor Devices with Splitting the High-Voltage Side with SAB - Theoretical Perspective

The specific on-resistance (RSP) of a semiconductor device is typically described with (2.1) [30, 58].

$$AR_{ON} = \frac{k}{\mu_n \epsilon_S E^3} V_B^2. \quad (2.1)$$

Product of R_{ON} (resistance of the drift region), and A (active area of the device), in (2.1) represents RSP. The RSP is dependent on:

- **Semiconductor property related parameters:**

- * k - a constant dependent on the process,
- * μ_n - the electron mobility,
- * ϵ_S - the semiconductor permittivity,
- * E_c - the critical field for avalanche breakdown.

- V_B - the device breakdown voltage.

Assuming fixed semiconductor property and process related parameters, it is of interest to investigate how does the RSP scales with the blocking voltage of the device. Using different blocking voltage devices is possible by staking multiple modules in series. The blocking voltage scaling analysis is normalized to a fixed total semiconductor area, and the total conduction loss of the stacked active bridge is compared for different number of modules n .

According to (2.1), the conduction loss of a single module blocking the entire DC bus voltage is directly proportional to:

$$P_{cond,1} \sim \frac{1}{A} \frac{k}{\mu_n \epsilon_S E^3} V_B^2. \quad (2.2)$$

Considering the same total active semiconductor area A , the conduction loss of n series-sacked modules that block the same DC bus voltage is proportional to:

$$P_{cond,1} \sim n \frac{1}{\left(\frac{A}{n}\right)} \frac{k}{\mu_n \epsilon_S E^3} \left(\frac{V_B}{n}\right)^2. \quad (2.3)$$

Which leads to conclusion that the total conduction loss is unaffected by the number of modules:

$$\frac{P_{cond,n}}{P_{cond,1}} = 1. \quad (2.4)$$

This conclusion is based on theoretical relation given in (2.1), which only approximately relates the blocking voltage to RSP of a device. Further investigation is presented in the following subsection, to revisit equation (2.1), which will give a more accurate insight in the voltage scaling of the devices.

2.3 Voltage Scaling of Semiconductor Devices with Splitting the High-Voltage Side with SAB - Revisited

Gallium Nitride (GaN) has been emerging technology over the past years, and it is continuing to grow. Wide band-gap (WBG) of GaN results in increased critical electric field by an order-of-magnitude. This leads to three orders-of-magnitude reduction in RSP [30]. RSP in lateral GaN devices is further reduced thanks to higher electron mobility in the two-dimensional electron gas (2DEG).

Efficient power conversion (EPC) has a wide portfolio of GaN devices ranging from 30V to 350V, in various sizes. Fig. 2.2 shows $R_{ON}Q_{GS}$ dependence on blocking voltage V_B . The data-points plotted with dots is pulled from EPC website [2]. Q_{GS} in the figure represents the gate-source charge. Since the information about active die area of the device is not easily accessible, it is assumed that $Q_{GS} \sim A$. Considering quadratic dependence of RSP to V_B , and a constant K , shown in (2.5), the curve-fit overlapped with the data is shown in Fig. 2.2a.

$$Q_{gs}R_{on} = KV_B^2, \quad (2.5)$$

One can note that the curve-fit given with (2.5) does not accurately reflect the data. The curve fit

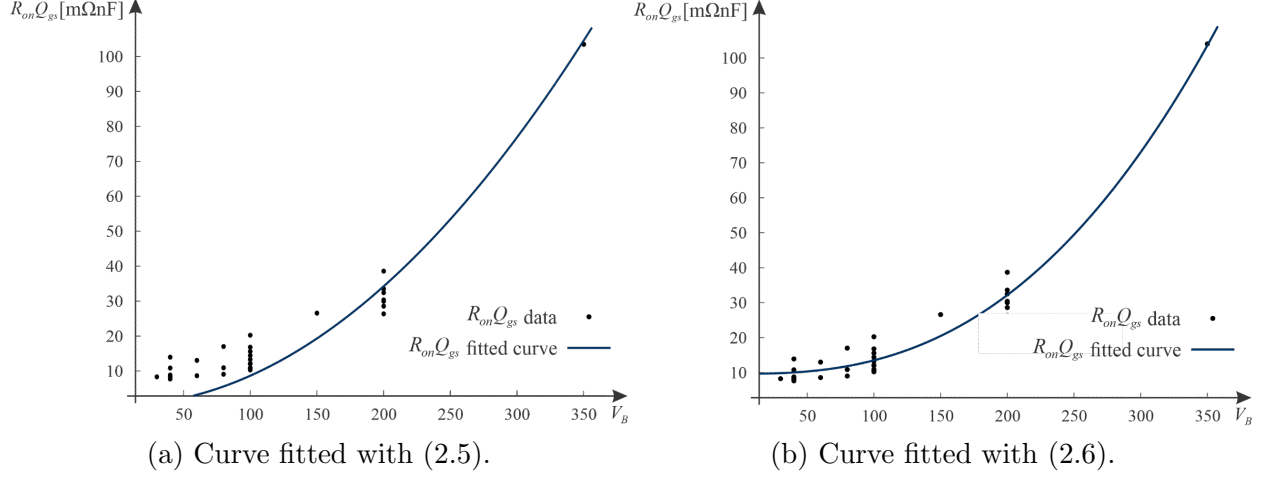


Figure 2.2: Voltage scaling of the RSP.

equation can be expanded to a more generalized exponential form:

$$Q_{gs}R_{on} = KV_B^\alpha + C, \quad (2.6)$$

where K , α and C are parameters determined by fitting the data. The curve-fit, overlapped with the data is presented in Fig.2.2b, showing very good matching. Interestingly, the exponent of the fitted curve is given with:

$$\alpha = 2.55, \quad (2.7)$$

contrary to quadratic dependence, assumed in (2.1). Fig. 2.3 shows the normalized conduction loss dependence of a SAB on the blocking voltage of the devices used. A lower blocking voltage device on the x-axis implies a higher number of modules, while the total active semiconductor area is kept constant. The two regions of the curve can be distinguished:

- **Low blocking voltage region** - dominated by constant C term in (2.6). This phenomenon happens due to metalization and die-to-pin interconnects. In smaller voltage-rated devices this effect dominates the conduction loss over the loss in the channel of the semiconductor. Therefore, using a large number of smaller voltage-rated devices in series, increases the total conduction loss in SAB.

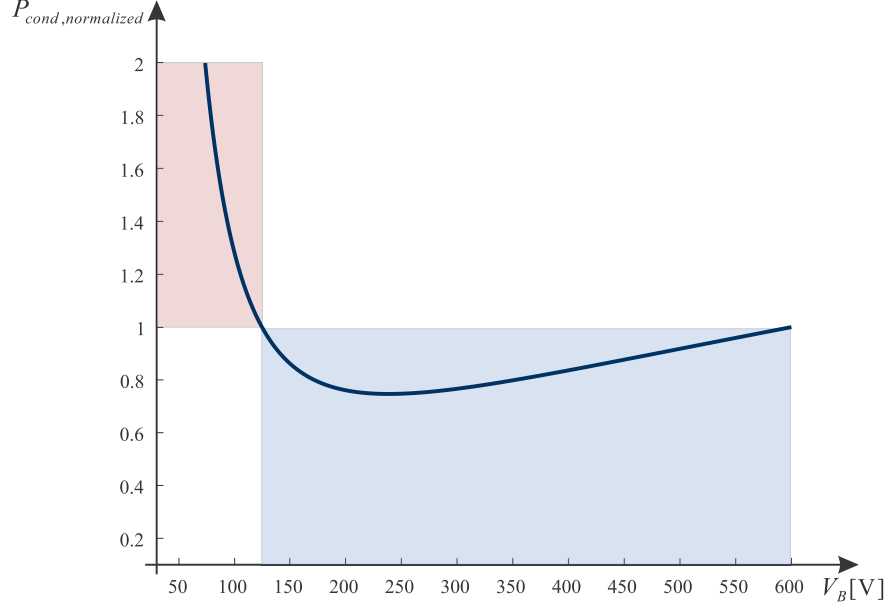


Figure 2.3: Scaling of the normalized conduction loss of the SAB with blocking voltage of the devices used in the stack.

- **High blocking voltage region** is dominated by the exponential term in (2.6). As it was shown previously with (2.4), if the exponent $\alpha = 2$, the total conduction loss in the channel does not change with the voltage rating of the devices used in the stacked active bridge. However, if $\alpha > 2$, as in the case of (2.7), the overall conduction loss reduces, with using a bigger number of smaller voltage-rated devices in SAB.

As illustrated in Fig. 2.3 with the blue region, splitting the DC bus voltage in multiple modules can be beneficial from the conduction loss point of view. Contrary, using too many modules can have a detrimental effect on the overall conduction loss, as shown in the red region in Fig. 2.3.

2.4 Energy stored in SAB

Aside from voltage scaling in terms of conduction loss, which has been discussed in the previous section, scaling of the total energy stored in a SAB is an important aspect. Even though the energy stored in an active bridge does not directly impact loss in the devices when soft-switched topologies are considered, it is directly proportional to the amount of inductive energy, that needs

to be stored in the circuit, to achieve soft switching. Energy stored in a single module active bridge is given with:

$$E_{C_{oss,1}} = C_{oss,1}V_{IN}^2, \quad (2.8)$$

where $C_{oss,1}$ is a parasitic drain to source capacitance of a device in a single module active bridge.

Now, considering a SAB with n modules, the total energy stored is:

$$E_{C_{oss,n}} = \frac{C_{oss,n}V_{IN}^2}{2n}, \quad (2.9)$$

where $C_{oss,n}$ is a parasitic drain to source capacitance of a device in an n -module SAB. Therefore, the ratio of stored energy using n modules, and stored energy using a single module is given with:

$$\frac{E_{C_{oss,n}}}{E_{C_{oss,1}}} = \frac{C_{oss,n}}{nC_{oss,n}}, \quad (2.10)$$

In order to benefit from using an n -module SAB, in terms of total stored energy, the parasitic capacitance of a device used in the SAB, needs to be smaller than n times parasitic capacitance of a device used in a single module AB.

$$C_{oss,n} < nC_{oss,1} \quad (2.11)$$

2.5 Chapter Summary and Conclusions

Scaling of the semiconductor devices with a different number of series-stacked modules is discussed in this chapter. Different voltage-rated devices can be used by splitting the high-voltage side of the converter between different number of modules. It is shown how the total specific on-resistance (RSP) of the stack can be reduced with the number of modules. However, a too large number of modules can lead to significant increase in RSP. Therefore an optimum number of modules in the stacked-active-bridge can be selected to minimize RSP.

Chapter 3

400 V-to-48 V Stacked Active Bridge Converter

This chapter is focused on the capacitively coupled Stacket-Active-Bridge (SAB) converter shown in Fig. 3.1. The converter is comprised of $n = 4$ series-stacked, capacitively coupled half-bridge inverter modules and $m = 2$ parallel-connected full-bridge rectifier modules. As opposed to the similar approaches reported in [5, 40], the converter is operated well above the series resonance so that the operating waveforms and the control characteristics are similar to the DAB converter. All of the inverter modules are controlled with the same square-wave control signals, and all the output rectifier modules are controlled with the same square-wave control signals, while the power flow through the converter is controlled by the phase-shift between the inverter and the rectifier control signals. In addition to the simple, DAB-like operation of the SAB configuration shown in Fig. 3.1, the key contributions of this chapter include an analysis of the natural voltage-sharing property of the converter in the presence of timing mismatches, and a novel realization of the series inductors integrated on a custom magnetic core.

A detailed analysis is conducted to examine the effects of timing mismatches among the gate-driver control signals on the voltage sharing among the stacked inverter modules. Similar to [6], the analysis is carried out considering ZVTs of the inverter bridges. It is shown that in practice the converter does not require an active control to ensure voltage balancing.

Four options are considered for the series inductors placement and implementation, and the options are compared in terms of loss, while keeping the same boxed volume. The most effective solution, which is based on integration of the inductors on a custom core, is selected and

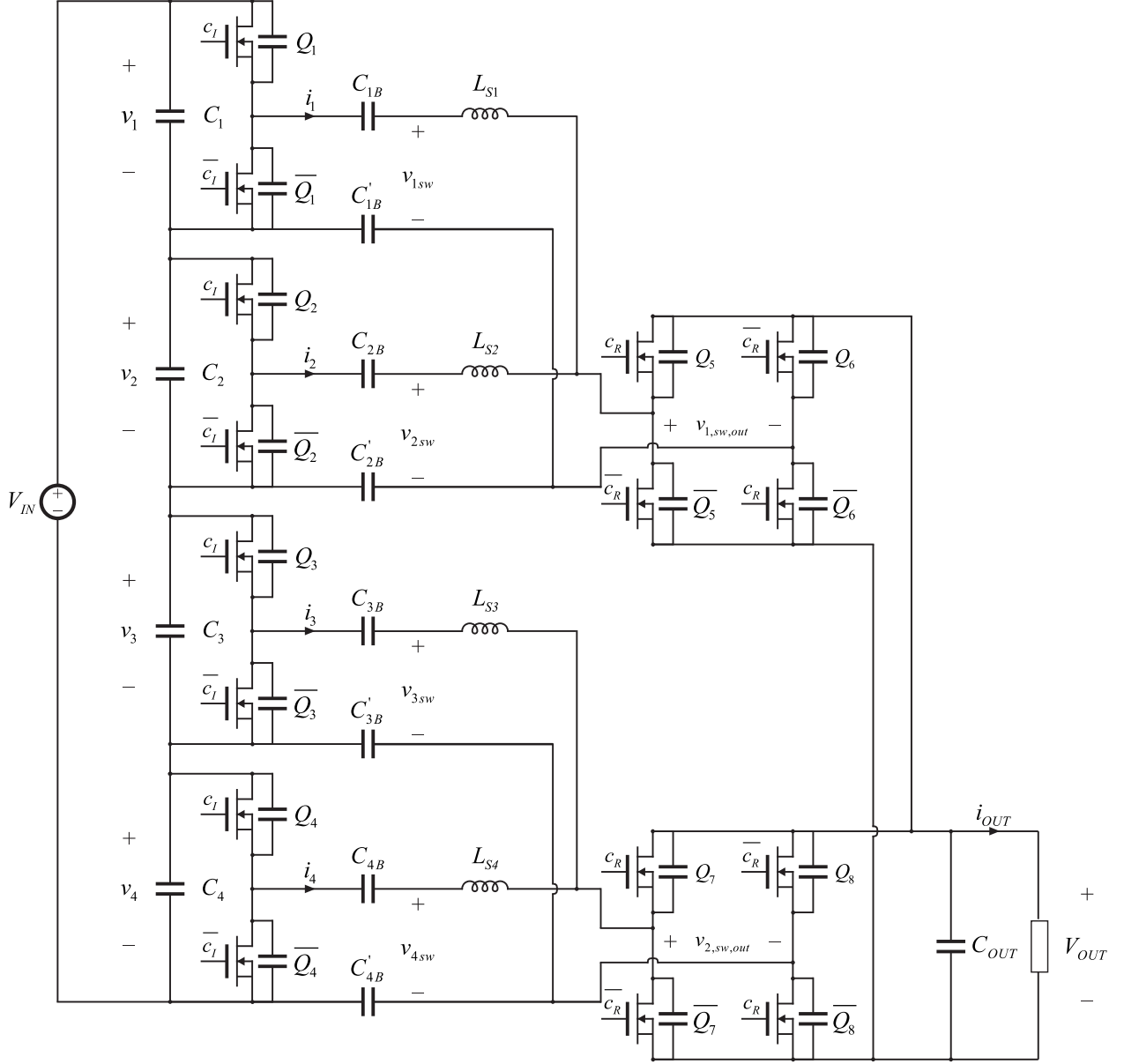


Figure 3.1: Stacked active bridge (SAB) dc-dc converter comprising $n = 4$ series-stacked, capacitively coupled half-bridge inverter modules and $m = 2$ parallel-connected full-bridge rectifier modules.

implemented in a hardware prototype.

The chapter is organized as follows. Section 3.1 describes operation of the SAB converter shown in Fig. 3.1. Section 3.2 focuses on the analysis of the input capacitor voltage balancing in the presence of timing mismatches among control signals. Various options for the realization of the

series inductors are discussed and compared in Section 3.3. Experimental results for a 400-to-48 V, 3 kW, 400 W/in³ SAB prototype operating at 400 kHz using GaN devices, and demonstrating a flat efficiency curve with 99% peak efficiency, are presented in Section 3.4. Section 3.5 concludes this chapter.

3.1 SAB converter operation

In steady-state operation of the SAB converter shown in Fig. 3.1, the input voltage is ideally equally shared among the inverter modules, $v_{1..n} = V_{in}/n$. Similarly, the output current is equally shared among the rectifier modules. As shown in Fig. 3.2, complementary square-wave signals c_I and $\overline{c_I}$ control the top and the bottom devices, respectively, in all the inverter active-bridges, while similarly c_R and $\overline{c_R}$ control the rectifier active-bridge devices. Similar to the standard phase-shift control of DAB converters, there are only four control signals regardless of the numbers of inverter or rectifier modules, and the phase shift between the inverter and the rectifier bridges controls the power flow through the converter [20, 73]. It would also be possible to operate the inverter bridges with interleaved gate pulses, potentially allowing for reduced switching frequency or reduced ripples, but at the expense of increased number of control signals and complexity. Fig. 3.2 also shows a series inductor current waveform, where t_α represents the inverter-side zero voltage transition (ZVT) interval of the inverter bridges, t_β is the ramp-up interval of the inductor current, t_δ is the ZVT interval of the rectifier bridges, and t_ξ is the current flat-top interval.

Similar to a DAB converter, the power transfer characteristic is given by

$$P = \frac{nV_{OUT}^2}{2\pi f_{sw}L_S} \varphi \left(1 - \frac{\varphi}{\pi}\right), \quad (3.1)$$

where $\varphi = t_\varphi 2\pi f_{sw}$ is the phase shift, and n is the number of inverter modules. With an appropriately controlled phase shift, the nominal conversion ratio is simply

$$M = \frac{V_{OUT}}{V_{IN}} = \frac{1}{2n}. \quad (3.2)$$

The steady-state characteristics (3.1), (3.2) are shown for the SAB converter of Fig. 3.1 where the inverter modules employ half-bridge stages and the rectifier modules are based on full-bridge

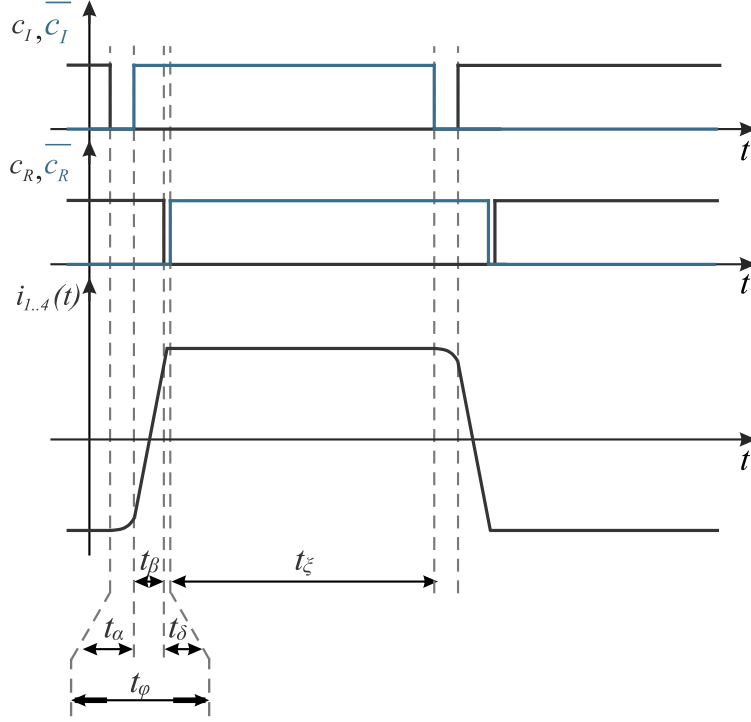


Figure 3.2: Control signals $c_I, \overline{c_I}$ for the inverter modules, and $c_R, \overline{c_R}$, for the rectifier modules, together with the inductor currents $i_{1..4}$ in the SAB converter of Fig. 3.1.

stages. Variations of the SAB converter topology can be constructed where the inverter or the rectifier modules are based on either half-bridge or full-bridge stages.

A minimum power needed to achieve ZVS of the inverter-side devices can be found approximately as

$$P_{crit} \approx \frac{V_{IN}^2}{2n} \sqrt{\frac{C_{HB}}{L_S}}, \quad (3.3)$$

where C_{HB} is the equivalent half-bridge switch-node capacitance [21], which is due to the device output capacitance and parasitic PCB capacitance, and L_S is the series inductance, which can be selected based on the ZVS condition in (3.3). A larger inductance leads to ZVS operation over a wider range of loads, but a larger size is required to realize the series inductor. This trade-off is exemplified in the experimental prototype addressed in Sections 3.3 and 3.4.

It is of interest to compare (3.3) to the ZVS condition expressed as the minimum power $P_{crit,conv}$ for a conventional DAB configuration with a single inverter module and an $n : 1$ step-

down transformer. Assuming the same C_{HB} capacitance, and the same switching frequency and phase shift for the same power transfer,

$$\frac{P_{crit}}{P_{crit,conv}} \approx \frac{1}{\sqrt{n}}, \quad (3.4)$$

which shows an advantage of the stacked inverters in terms of the power required to achieve ZVS. This advantage can be utilized either to achieve an extended ZVS range, or to reduce the total energy stored in the series inductors. Furthermore, upon loss of ZVS, the hard-switching losses at light loads are reduced in the stacked-inverter configuration.

3.2 Capacitor voltage balancing

As mentioned in the previous section, all the inverter modules are controlled with the same control signals, and the input voltage is shared equally among the modules, $v_{1..n} = V_{IN}/n$. The control signals propagate from a controller through PCB traces, isolators and gate drivers. Any mismatches among propagation delays result in effective on/off timing mismatches among the inverter modules, which in turn may lead to an imbalance among the capacitor voltages $v_{1..n}$. Additionally, a mismatch between the inductances $L_{1..n}$, as well as halfbridge switch-node capacitances C_{HB} ,

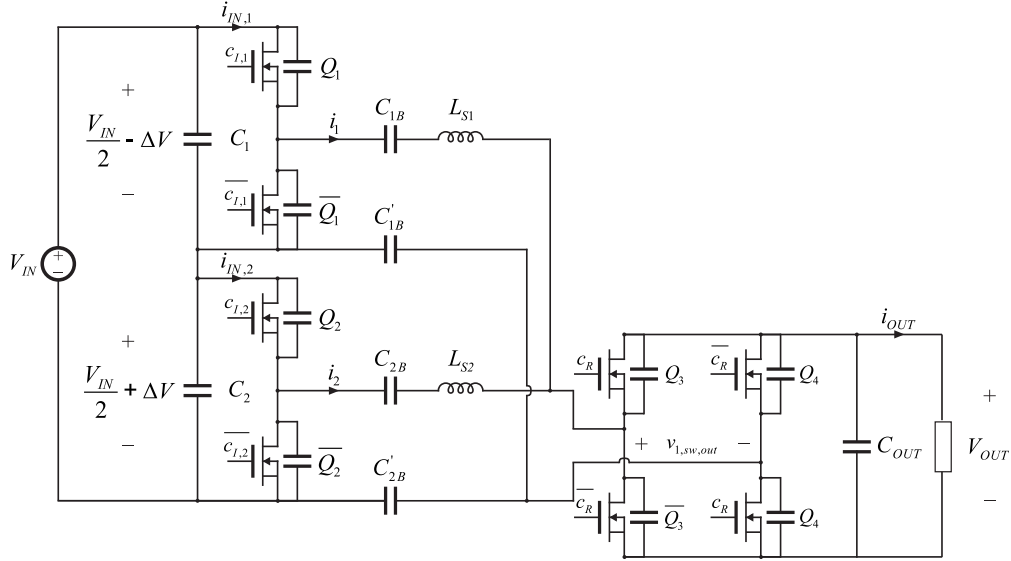


Figure 3.3: SAB converter with two inverter modules having a timing mismatch between the control signals $c_{I,1}$ and $c_{I,2}$.

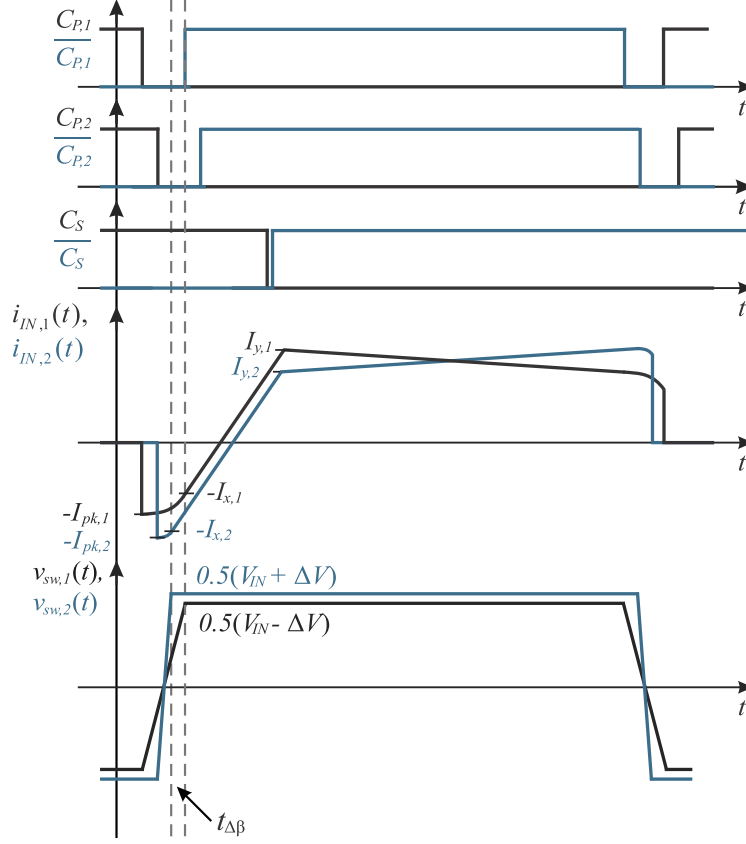


Figure 3.4: Control signals $c_{I,1}$, $\overline{c_{I,1}}$ and $c_{I,2}$, $\overline{c_{I,2}}$ for the inverter modules, and c_R , $\overline{c_R}$, for the rectifier modules, together with the input currents $i_{IN,1}$, $i_{IN,2}$, and the switching node voltages $v_{sw,1}$, $v_{sw,2}$ in the SAB converter of Fig. 3.3 under imbalanced conditions due to timing mismatches.

cause imbalance among the voltages. In order to investigate the effects of these nonidealities, a simplified configuration with two inverter modules, as shown in Fig. 3.3, is considered for simplicity.

Fig. 3.4 shows theoretical waveforms of the mismatched gate pulses, and their effect on the switch-node voltages and the inductor currents. The timing mismatch acts as a mismatch between phase shifts of the modules with respect to the rectifier, which can be viewed as a difference between the t_β intervals of the two modules, shown as $t_{\Delta\beta}$ in Fig. 3.4. Considering idealized waveforms, without taking into account the inverter-side zero-voltage transition (ZVT) intervals, the timing mismatch would result in diverging capacitor voltages. However, taking the resonant transitions into account, it is found that the capacitor voltages converge to steady-state values only slightly away from the ideal, balanced conditions.

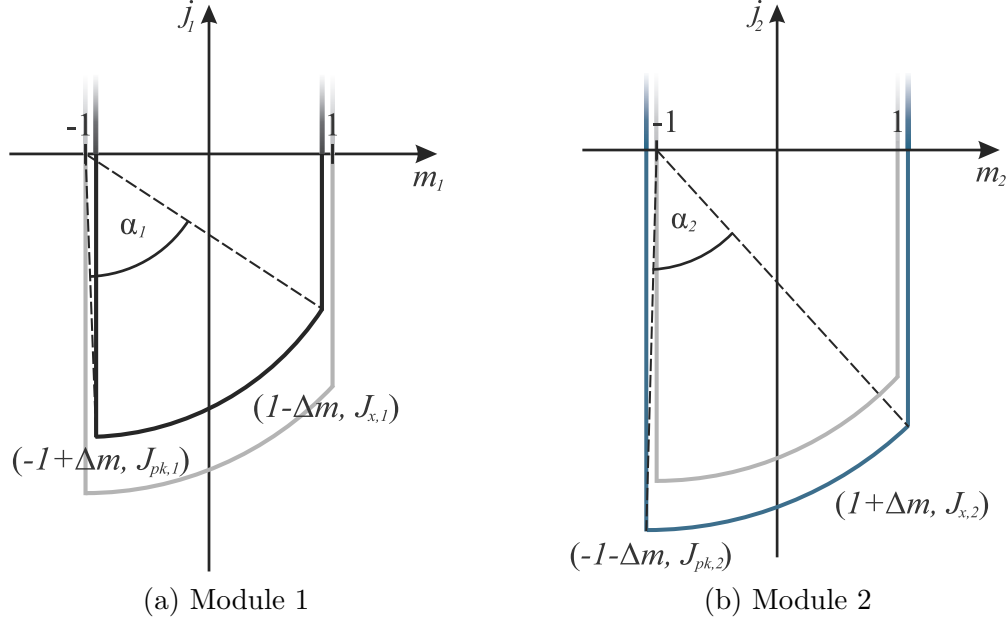


Figure 3.5: State-plane diagrams for the normalized switching node voltages $v_{sw,1}$, $v_{sw,2}$, and inductor currents i_1 , i_2 , corresponding to the waveforms under imbalanced condition shown in Fig. 3.4. The state-plane trajectories when the voltages are perfectly balanced are shown in light-gray color.

In order to find a steady-state solution for the imbalance ΔV as a function of the timing mismatch Δt_β , each module can be considered separately using state-plane analysis, as shown in Fig. 3.5. In the state-plane analysis, a standard normalization is applied using the base values $V_{base} = 2V_{OUT}$ and $I_{base} = \frac{V_{base}}{R_0}$, where $R_0 = \sqrt{L_S/C_{HB}}$.

A set of expressions derived from the state-plane diagrams is provided in Appendix A. For a given $t_{\Delta\beta}$, ΔV can be found from the charge balance conditions for the inverter input capacitors, i.e., by equating the average input currents of the two inverter modules,

$$I_{IN,1} = I_{IN,2}. \quad (3.5)$$

The solution can be found using numerical iterations, as described in Appendix A.

The analysis results are presented in Fig. 3.6 where $\Delta V/(2V_{OUT})$ is shown as a function of the timing mismatch in nanoseconds, for several different values of the half-bridge switch-node capacitance C_{HB} . As expected, a longer mismatch results in a larger voltage imbalance. A larger

C_{HB} capacitance results in a longer resonant transition interval, which in turn means that a larger timing mismatch can be tolerated.

The effect of the mismatch between the inductances on the imbalance among the voltages can be analyzed by setting $t_{\Delta\beta} = 0$ and using different characteristic impedances for normalizing the currents in the two cases, $R_{0,1} = \sqrt{L_{S1}/C_{HB}}$ and $R_{0,2} = \sqrt{L_{S2}/C_{HB}}$, where $L_{S1} = L_S + \Delta L_S/2$ and $L_{S2} = L_S - \Delta L_S/2$. Fig. 3.7 shows the results of the inductance mismatch analysis, where $\Delta V/(2V_{OUT})$ is shown as a function of the percentage inductance mismatch $\Delta L_S/L_S$, for several different values of the half-bridge switch-node capacitance C_{HB} . Similar to the timing mismatch results, a larger half-bridge capacitance implies a larger tolerance to inductance mismatch.

Similarly, the effect of the mismatch between the half-bridge switch-node capacitances on the imbalance among the voltages can be analyzed using different characteristic impedances for normalizing the currents, $R_{0,1} = \sqrt{L/C_{HB1}}$ and $R_{0,2} = \sqrt{L/C_{HB2}}$, where $C_{HB1} = C_{HB} - \Delta C_{HB}/2$ and $C_{HB2} = C_{HB} + \Delta C_{HB}/2$. The results are shown in Fig. 3.8 where $\Delta V/(2V_{OUT})$ is shown as a function of the capacitance percent mismatch $\Delta C_{HB}/C_{HB}$.

In practice, as discussed further in the context of the experimental prototype described in

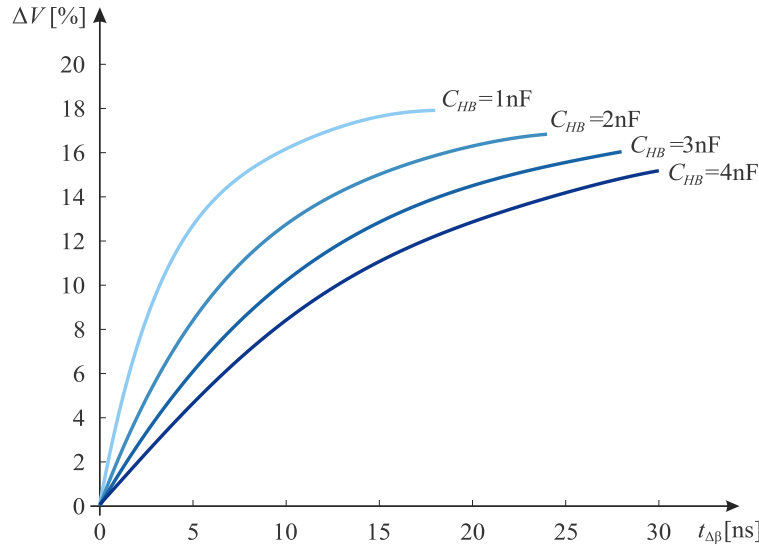


Figure 3.6: Voltage imbalance ΔV as a function of the timing mismatch $t_{\Delta\beta}$ between the control signals $c_{I,1}$ and $c_{I,2}$ in the SAB converter of Fig. 3.3, for different values of the half-bridge switch node capacitance C_{HB} .

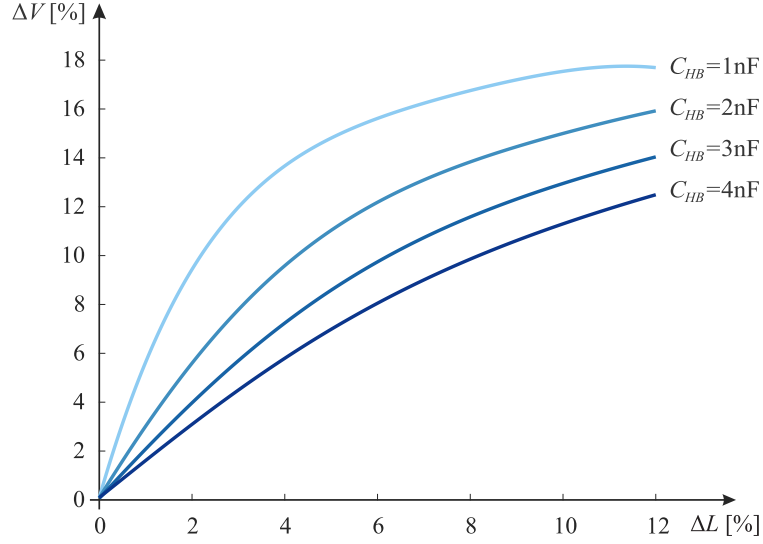


Figure 3.7: Voltage imbalance ΔV as a function of the inductance mismatch $\Delta L/L$, for different values of the half-bridge switch-node capacitance C_{HB} .

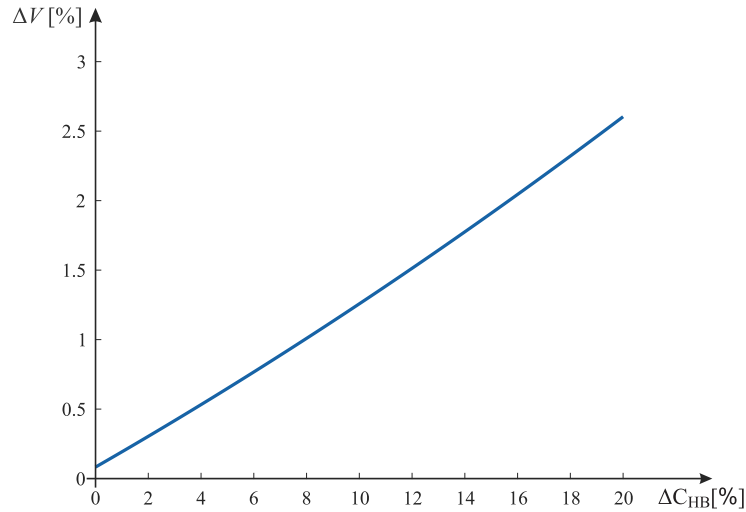


Figure 3.8: Voltage imbalance ΔV as a function of the half-bridge switch-node capacitance mismatch $\Delta C_{HB}/C_{HB}$, where $C_{HB} = 2.4\text{ nF}$.

Section 3.4, the results in Figs. 3.6, 3.7 and 3.8 suggest that no active balancing is necessary to achieve input capacitor voltage sharing in the SAB converter.

3.3 Realization of the series inductors

The SAB modular structure offers several possibilities for realization of the series inductors, as shown in Fig. 3.9. In all cases, a planar implementation is assumed. The four options considered

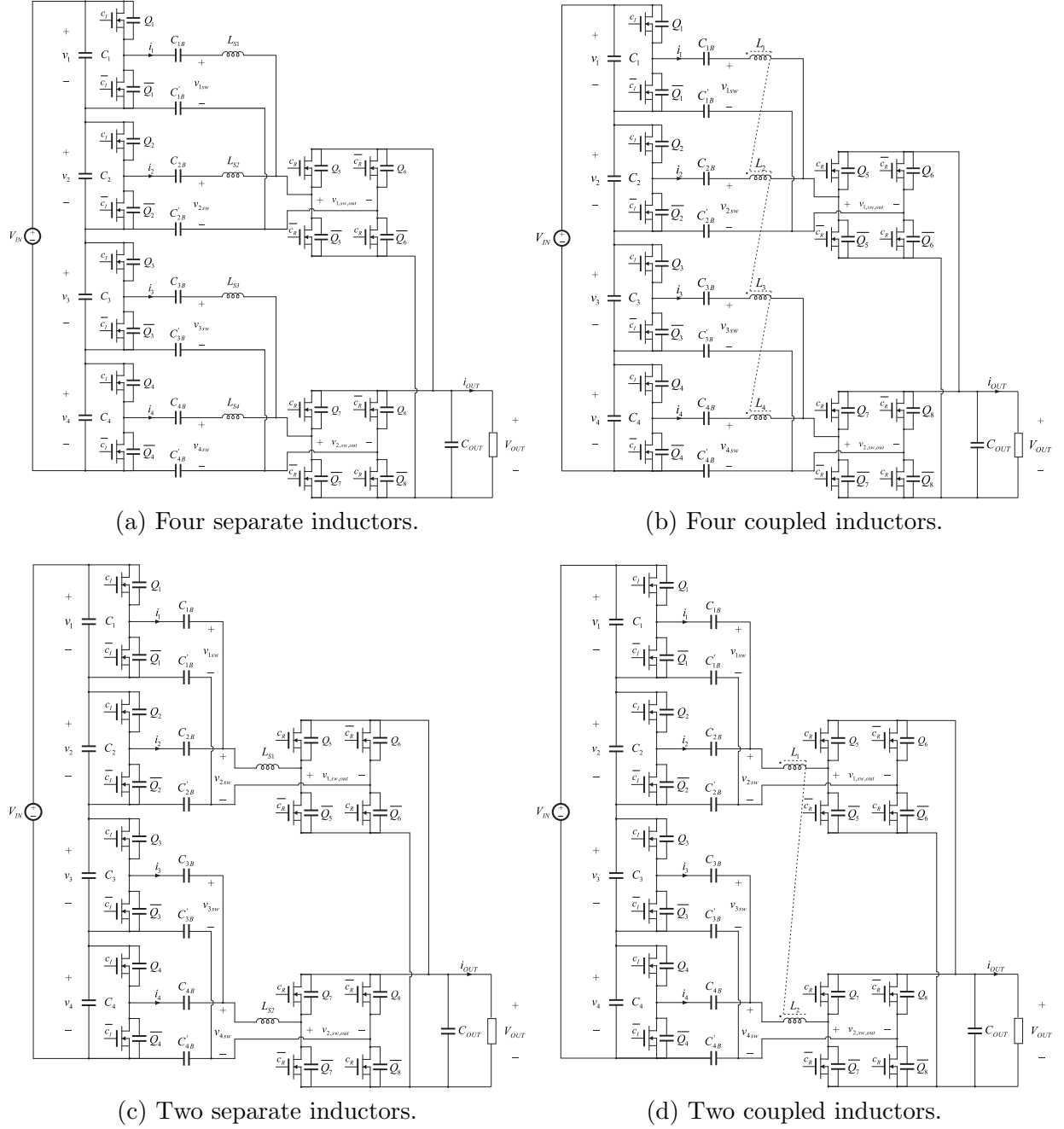
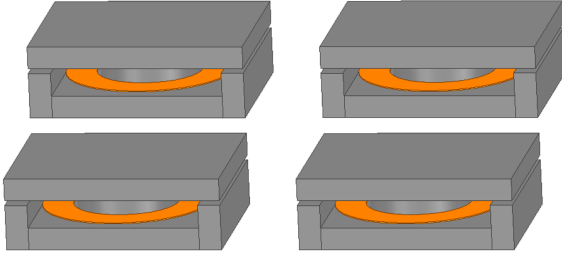
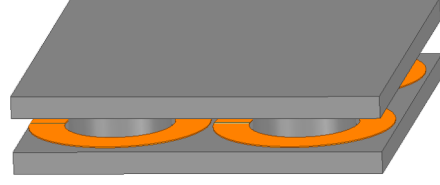


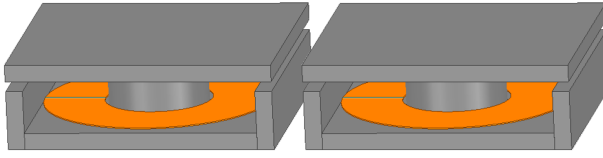
Figure 3.9: Four different realizations of the series inductors.



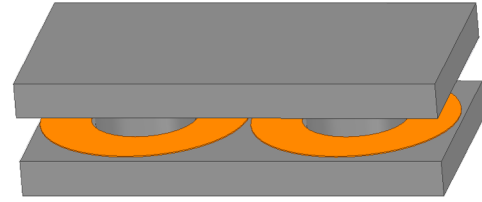
(a) Four separate inductors.



(b) Four coupled inductors.



(c) Two separate inductors.



(d) Two coupled inductors.

Figure 3.10: Four planar magnetic structures for implementation of the series inductors, corresponding to the realizations shown in Fig. 3.9. In the comparison, the total box volume of the magnetic structures is kept the same.

are as follows:

- (A) Fig. 3.9a - An inductor is placed in one of the two branches of each inverter module. This approach requires four separate inductors using EI cores, as shown in Fig. 3.10a.
- (B) Fig. 3.9b - The inductors in option (A) can be coupled on a single core. The core structure shown in Fig. 3.10b allows the flux from one of the center posts to close through the two adjacent posts, which eliminates the need for side posts. This can be utilized to reduce the magnetics size or to reduce the losses.
- (C) Fig. 3.9c - Two capacitively coupled inverter stages can be connected in parallel at their outputs. In this case, an inductor is placed between the parallel connection of the inverters and a rectifier switching node. This option requires two separate inductors using EI cores,

as shown in Fig. 3.10c.

- (D) Fig. 3.9d - The inductors in option (C) can be coupled on a single core, as shown in Fig. 3.10d.

3.3.1 Loss modeling, design optimization, and comparison of inductor realizations

Since the series inductor currents are relatively high, only single layer, single turn inductor designs are considered, to eliminate the proximity effect between the layers. Three core geometry parameters are considered as the design variables: the center post area A , the winding area width W and the winding area height H , as illustrated in Fig. 3.11 for a single inductor.

In order to reduce the effect of the fringing field on the conduction loss, the winding layer is kept relatively far away from the gap. This can be controlled through aspect ratio W/H . Decreasing W/H , results in underutilized window area, which leads to larger copper and core losses. Conversely, increasing W/H , results in better utilization of the window area, and smaller loss up to the point where the winding becomes too close to the air gap, and the fringing-field induced eddy currents result in increased conduction loss [79]. For a fair comparison, the same aspect ratio $W/H = 1.5$ is

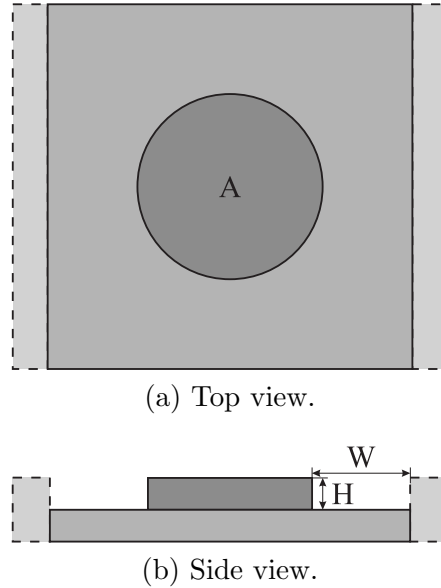


Figure 3.11: Single planar inductor dimensions.

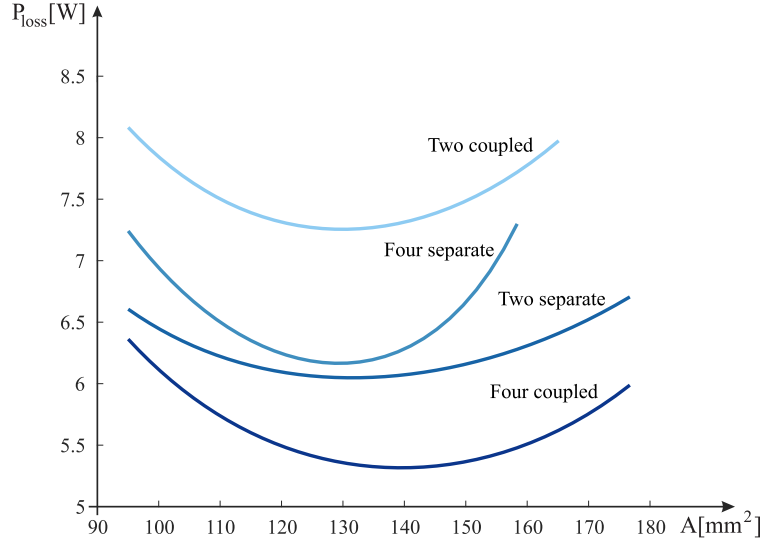


Figure 3.12: Comparison of the magnetic structures in Fig. 3.10: total inductor loss as a function of the core center-post area A in the 400-to-48 V, 3 kW SAB converter operating at full power. The switching frequency is $f_{sw} = 400$ kHz.

kept in all considered designs and the same total boxed volume is kept for all inductor realization options shown in Fig. 3.10. This simplifies the optimization problem, narrowing the design space down to only one independent variable. The center-post cross section area A is chosen to be the independent input variable.

For each design, the conduction loss is calculated using Dowell's equations [26]. Keeping the winding away from the gap makes this approach fairly accurate, since the fringing field effect is relatively small. The core loss is estimated using the improved generalized Steinmetz equation (iGSE) [87]. The total loss as a function of A is plotted in Fig. 3.12 for the four options considered in a 400-to-48 V, 3 kW SAB converter operating at full power, and at $f_{sw} = 400$ kHz switching frequency. One may observe that option (D) results in the highest losses. This is due to the fact that the flux, when entering from the main post to the top/bottom plate of the core does not split in two, which is the case in all other considered options. As a result, in option (D) the area of the plates has to be the same as the center post area A , whereas it can be reduced by half in all other options. The second worst performing are options (A) and (C), which have comparable losses.

Option (B) offers the lowest losses. In the case when the four inductors are coupled on the

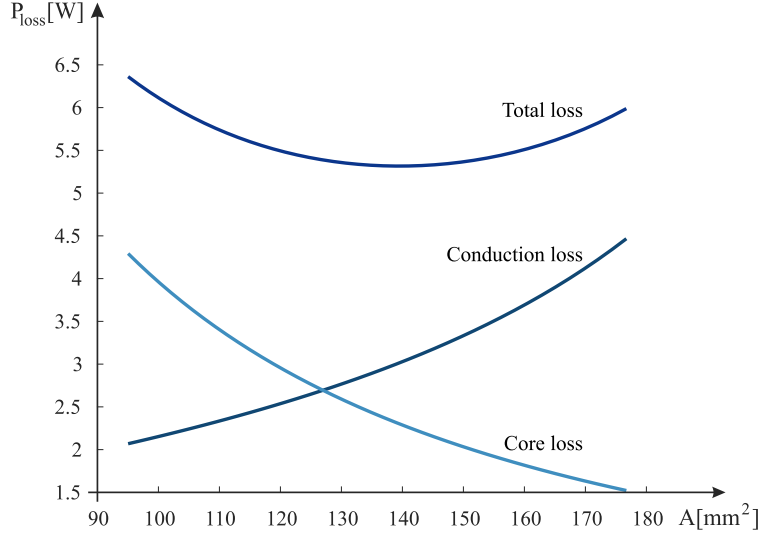
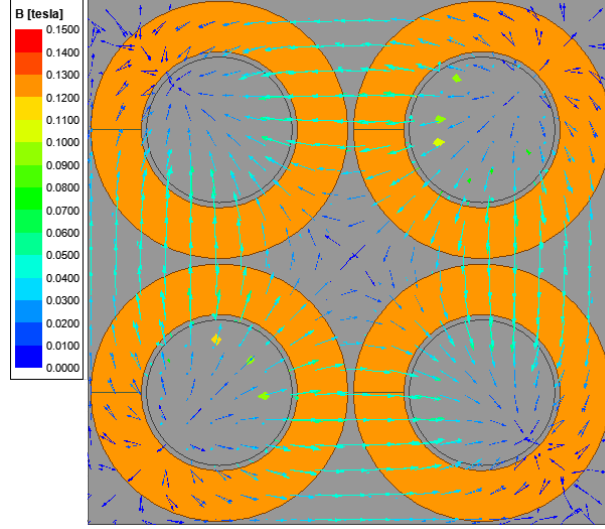


Figure 3.13: Loss optimization of the magnetic structure with four coupled inductors (option (B)), shown in Fig. 3.10b: conduction and core losses are shown as functions of the core center-post area A , under the constraints that the total boxed volume and the aspect ratio W/H are fixed.

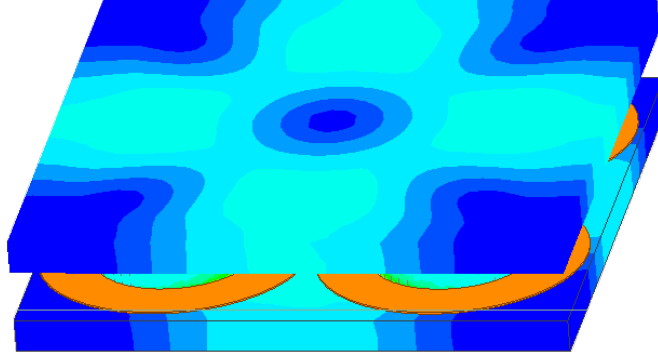
same core, the side posts can be removed, which is a fundamental advantage of option (B). Fig. 3.13 presents conduction and core loss for option (B) as functions of A . It can be noted that the optimum design gives nearly equal loss distribution between the two. Fig. 3.14 shows results of a finite element analysis (FEA) simulation for a near optimum design ($A = 125 \text{ mm}^2$) for option (B). It can be observed how the magnetic flux flows out of one post and into the two adjacent posts. The area of the I segment can therefore be equal to one half of the center post area A . Together with the removal of the side posts, this is the reason option (B) results in the lowest losses, and is the option selected for implementation in the experimental prototype.

3.3.2 Magnetic structure with four coupled inductors

The SAB steady-state characteristic (3.1) is derived based on inductance L_S of the four separate inductors (option (A)). To maintain the same power flow with the same phase shift φ , it is necessary to find the equivalent series inductance $L_{S,eq}$ that results in the same di/dt during the current ramp-up interval when all windings in the structure with four coupled inductors (option (B)) are energized and carry the same current i .



(a) Flux density vector diagram.



(b) Magnitude of the flux density.

Figure 3.14: Flux density obtained using 3D FEA simulation in the magnetic structure with four coupled inductors operating at full load in the 3 kW, 400-to-48 V SAB converter.

The equivalent series inductance $L_{S,eq}$ for option (B) follows from the equivalent magnetic circuits shown in Fig. 3.15(a) for the separate inductors and in Fig. 3.15(b) for the coupled inductors. It should be noted that the equivalent magnetic circuit model in Fig. 3.15(b) assumes a coupling coefficient of $k = 1/3$, neglecting any stray leakage flux.

By solving the magnetic circuit model in Fig. 3.15(b), the total flux Φ_B through a center

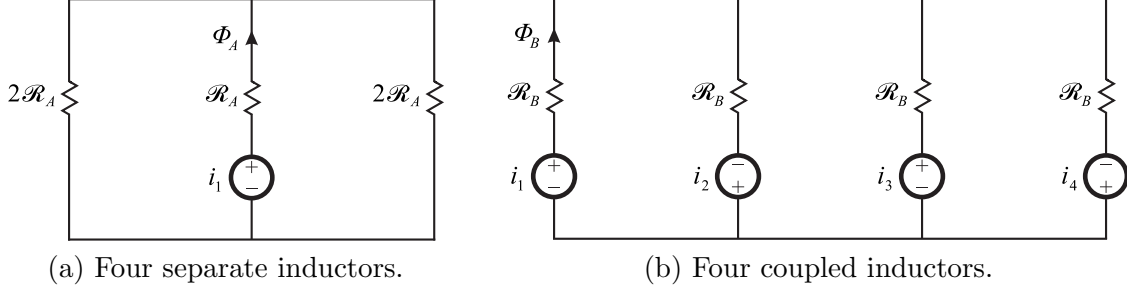


Figure 3.15: Magnetic circuit models. Each winding has a single turn.

post in the coupled-inductor structure is

$$\Phi_B = \frac{i}{\mathcal{R}_B}, \quad (3.6)$$

To get $L_{S,eq} = L_S$, Φ_B should be equal to the total flux Φ_A through the center post of a single separate inductor,

$$\Phi_A = \frac{i}{2\mathcal{R}_A}. \quad (3.7)$$

Equating (3.6) and (3.7) yields a relationship between the center-post reluctances:

$$\mathcal{R}_B = 2\mathcal{R}_A. \quad (3.8)$$

Consequently, in order to maintain the same steady-state characteristic with $L_{S,eq} = L_S$ in (3.1), the air-gap $l_{g,B}$ for the coupled-inductor structure should be selected as follows:

$$l_{g,B} = \frac{\mu_0 A}{L_S}. \quad (3.9)$$

If (3.8) is satisfied, it further follows that the self inductance L of each winding in the coupled-inductor structure is related to inductance L_S ,

$$L = \frac{3}{4}L_S. \quad (3.10)$$

For a given L_S , the relationship (3.10) can be used to verify or adjust the air-gap $l_{g,B}$ by measuring the winding self inductance L in the coupled-inductor structure (option (B)).

3.3.3 Effects of inductor coupling on the capacitor voltage balancing

The voltage balancing analysis in Section 3.2 considers uncoupled inductors (option A). Given that the implementation with coupled inductors (option B) is the best performing option, it is of interest to qualitatively consider the impact of coupling on the balancing performance. Assume, for simplicity, perfect coupling $k = 1$ between the inductors in two inverter modules. If the switch in module 1 turns off, while the switch in module 2 is still on, the switch-node voltage of module 1 remains unchanged, i.e., the resonant transition does not start, because the voltage across the inductor winding in module 1 is set by the voltage in module 2. Turning the switch in module 2 off, the resonant transitions starts simultaneously in both modules, effectively eliminating the effects of any timing mismatches. This implies that inductor coupling tends to improve the voltage balancing performance. In conclusion, given $k = 1/3$ in the practical coupled inductor realization, the analysis presented in the Section 3.2 can be considered somewhat conservative with respect to voltage balancing performance.

3.4 Experimental results

A photograph of the 400-to-48 V, 3 kW SAB prototype is shown in Fig. 3.16, and the converter parameters are provided in Table 3.1. 150 V GaN devices (EPC2033) are used in the inverter half-bridges, and 80 V GaN devices (EPC2021) are used in the rectifier bridges. Following the optimized coupled inductor design described in Section 3.3 (option (B)), a custom ferrite core with four posts is made using DMR96 material from DMEGC. The core dimensions are 50 mm \times 50 mm \times 10 mm. The coupled inductor windings are terminated with four pins at each connecting point. Similarly, the main power board has receptacles that connect to the pins. Custom heat sinks are designed to improve thermal management of the GaN devices. As illustrated in Fig. 3.17, the base of the heat sink is trimmed such that the protrusions touch the devices, while the other components are kept away from the heat sink. The box dimensions of the prototype, including the heat sinks, are 125 mm \times 65 mm \times 15 mm, which results in 400 W/in³ power density.

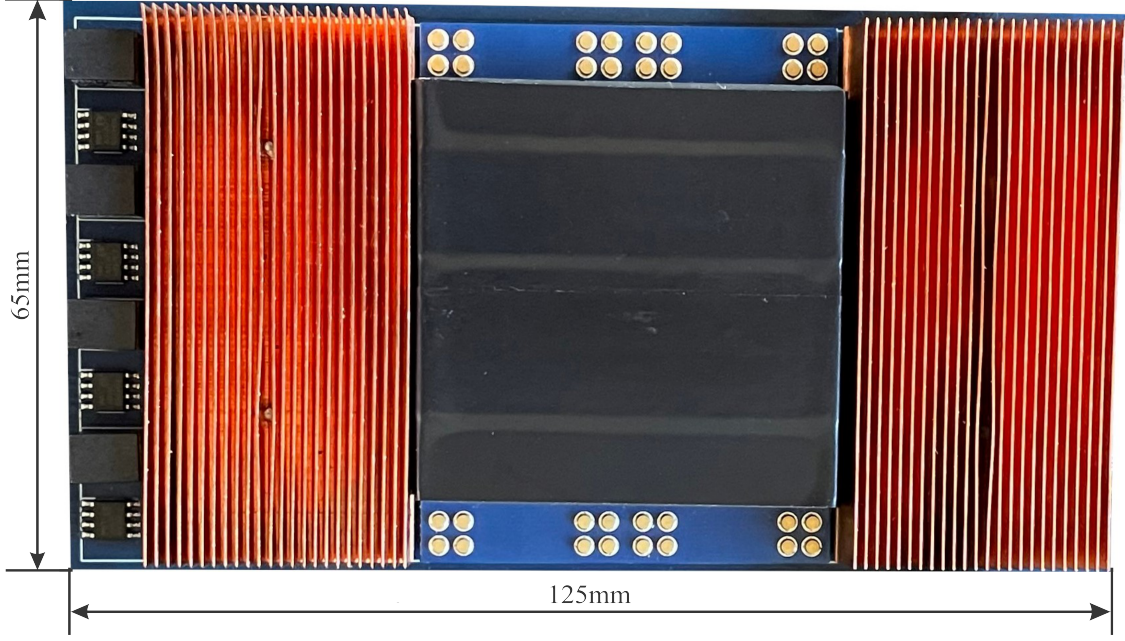


Figure 3.16: Photograph (top view) of the 3 kW, 400-to-48 V SAB prototype. The prototype box dimensions, including heat sinks, are 125 mm \times 65 mm \times 15 mm, which yields 400 W/in³ power density.

Table 3.1: Components and parameter values in the 400-to-48 V, 3 kW SAB prototype

$Q_{1..4}, \overline{Q}_{1..4}$	EPC2033
$Q_{5..8}, \overline{Q}_{5..8}$	EPC2021
L	330 nH
$C_{1B..4B}, C'_{1B..4B}$	8.8 μ F
f_{sw}	400 kHz

Fig. 3.18 shows waveforms of the inverter and the rectifier switch-node voltages, as well as one of the series inductor currents measured at the rated power. Both switching nodes achieve ZVS, while the current has the expected low-rms flat-top shape.

Fig. 3.20 shows three inverter switch-node voltages. This experimental result shows that the input voltages across the modules are well balanced, indicating that there is no significant timing mismatch between the gate pulses of the inverter modules.

The analysis in Section 3.2 is verified by measuring the input dc voltages $v_{1..4}$ of the input

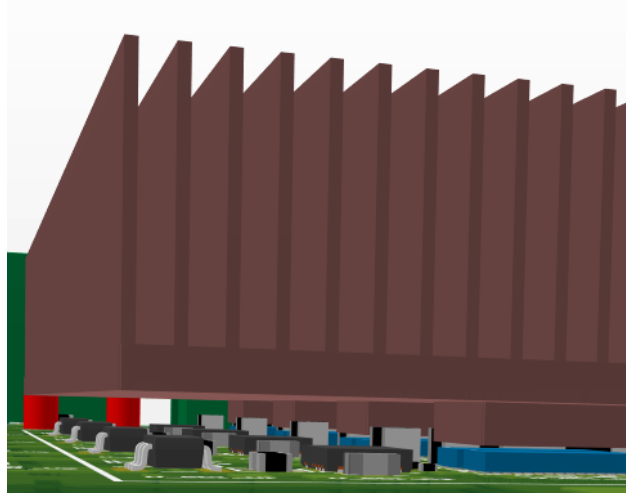


Figure 3.17: A 3D model showing how the custom heat sinks are mounted on the SAB prototype PCB. The base of the heat sink is trimmed such that the heat-sink protrusions are in direct thermal contact with the top of the GaN devices.

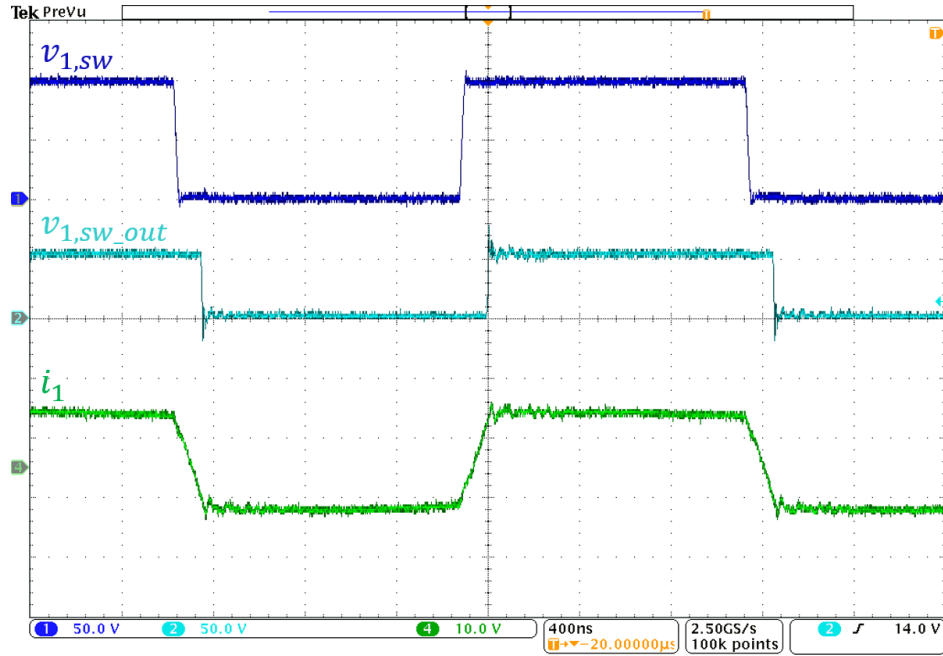
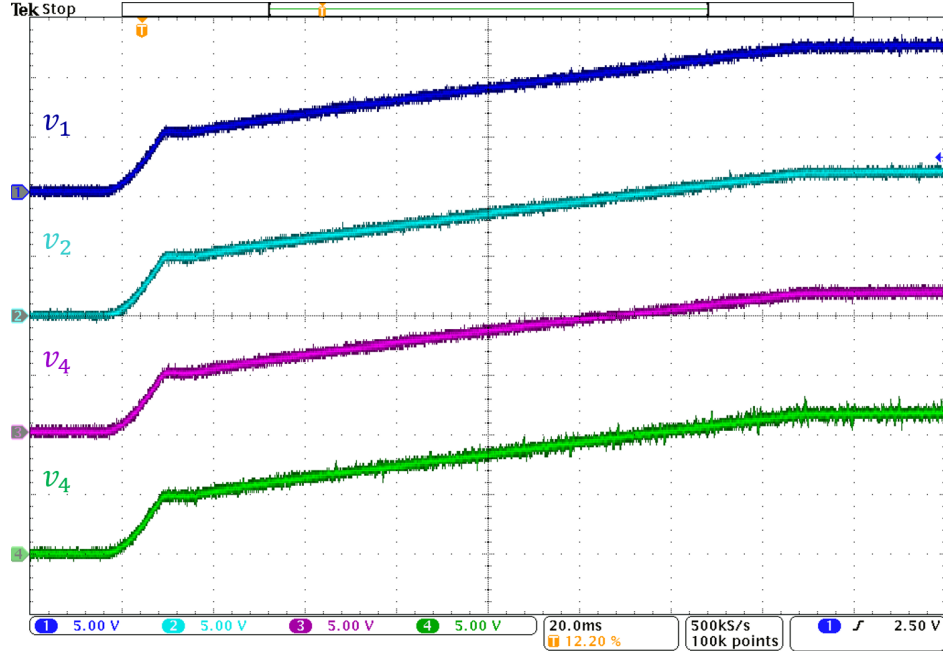
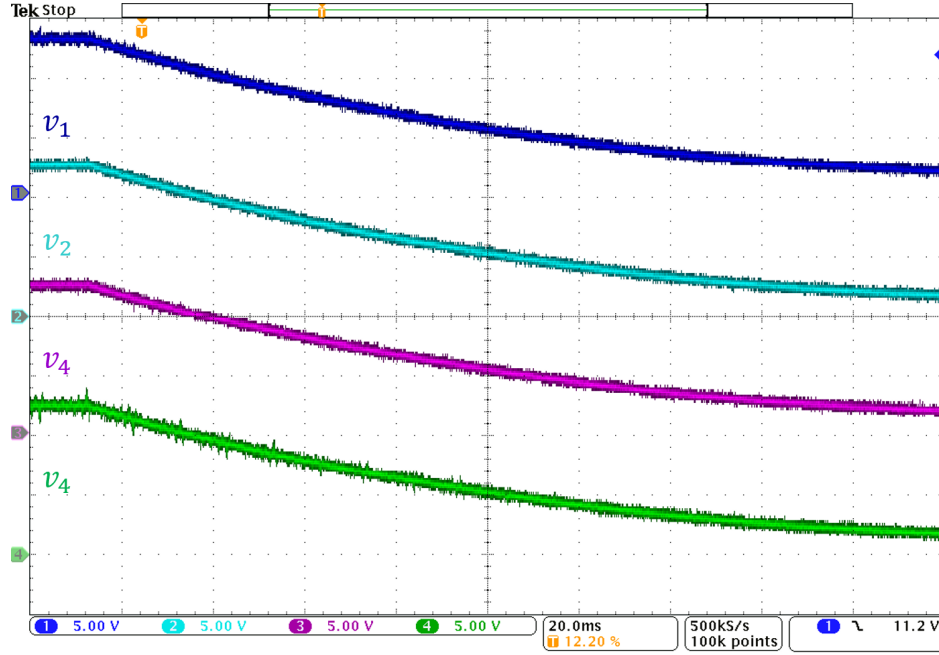


Figure 3.18: Experimental waveforms in the 400-to-48 V SAB prototype operating at 3 kW: inverter 1 switch-node voltage $v_{1,sw}$, rectifier 1 switch-node voltage $v_{1,sw,out}$, and series inductor current i_1 .

modules. A theoretical maximum voltage deviation is calculated based on the analysis in Section 3.2 and the timing mismatch parameters shown in Table 3.3 for the gate driver and the digital isolator. Measured inductance mismatch in the prototype is below 1%, and can therefore be neglected,



(a) Power-up transient.



(b) Power-down transient.

Figure 3.19: Module voltages $v_{1..n}$, during the input power supply turn-on/off transients.

according to the results in Fig. 3.7. Measured mismatch between the switch-node capacitances in the prototype is below 6%. According to Fig. 3.8, the maximum voltage deviation caused by this

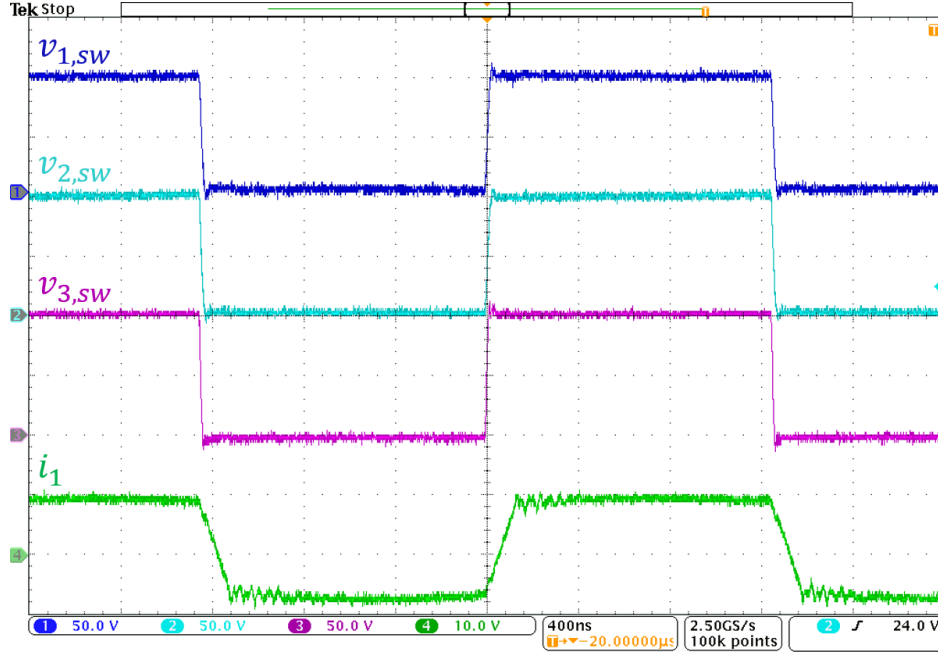


Figure 3.20: Experimental waveforms showing the switch-node voltages $v_{1..3,sw}$, and the series inductor current i_1 . Amplitudes of the switch-node voltages are the same, demonstrating that the inverter capacitor voltages are well balanced.

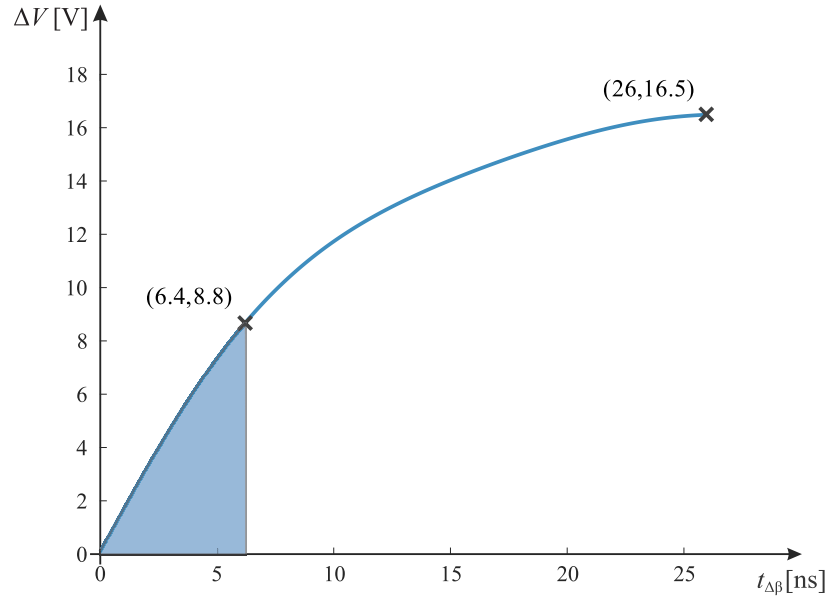


Figure 3.21: Theoretically predicted voltage imbalance ΔV as a function of the timing mismatch $t_{\Delta\beta}$ between the control signals $c_{I,1}$ and $c_{I,2}$ in the SAB converter with the half-bridge switch node capacitance $C_{HB} = 2.4 \text{ nF}$. The predicted range of ΔV is determined based on the maximum time delay mismatch given in Table 3.3.

Table 3.2: Experimentally measured imbalance of the inverter input dc voltages with respect to the nominal value of $V_{IN}/4 = 100\text{ V}$

	$v_1 = 108\text{V}$	$v_2 = 102\text{V}$	$v_3 = 93\text{V}$	$v_4 = 97\text{V}$
ΔV	8V	2V	7V	3V

Table 3.3: Delay mismatch introduced by the gate driver (LMG1210RVRT) and the digital isolator (SN74LVC2G17DBVT)

	Gate driver	Digital isolator	Total
Maximum delay mismatch	3.4ns	3ns	6.4ns

mismatch is less than 0.75%. As presented in Fig. 3.21 the analysis predicts a maximum voltage deviation of around 8.8 V for the maximum time-delay mismatch of 6.4 ns, and the equivalent half-bridge capacitance $C_{HB} = 2.4\text{ nF}$. Based on the measured dc voltages noted in Table 3.2, all the voltages are within the limits predicted by the analysis. Furthermore, as indicated in Fig. 3.21,

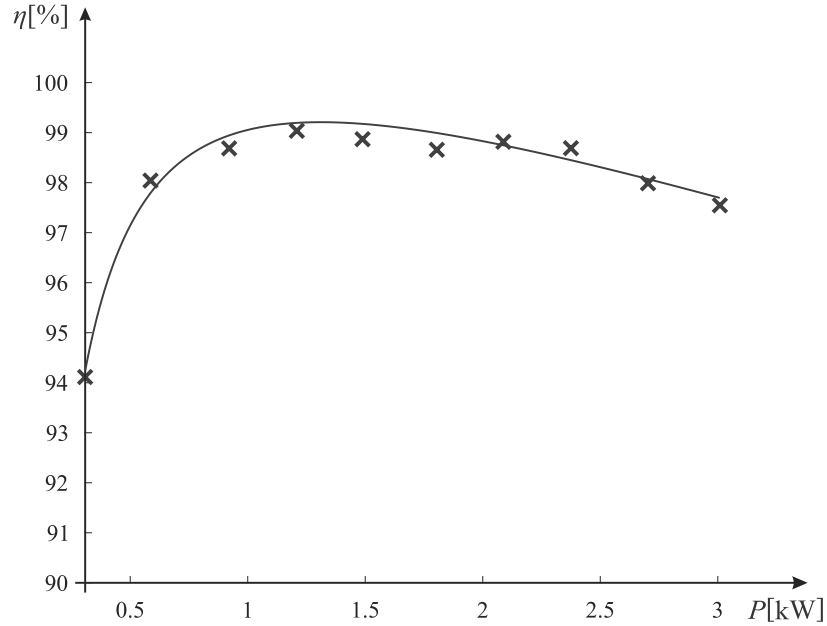


Figure 3.22: Measured efficiency of the experimental SAB prototype, together with a model-predicted efficiency curve, as functions of the output power from 10% to 100%.

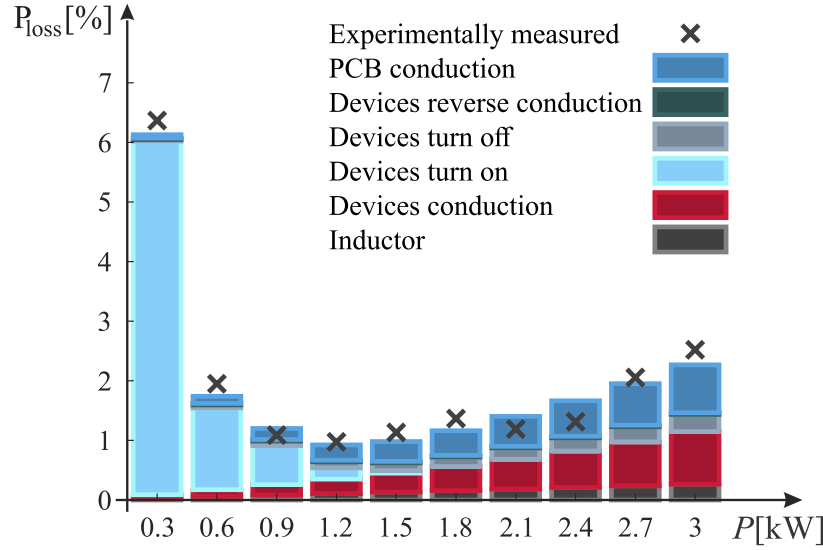


Figure 3.23: Model-predicted loss budget and the total measured loss in the 3 kW SAB prototype operating from 10% to 100% of load.

there is a substantial margin between the time delay mismatch in the prototype, and the mismatch that the circuit could tolerate before the inverter input voltages would start to diverge.

Fig. 3.19 shows how the voltages $v_{1..n}$ vary during input power supply turn on/off transients. The input voltage, in this experiment, is set to a scaled value of 50 V, for demonstration purposes. The phase shift is kept constant throughout the transient. The results show that the voltages remain well balanced during both power-on and power-off transients.

According to (3.3), the converter starts partially hard switching for power levels below $P_{crit} = 1.7$ kW. Even when operating with partial ZVS, the switching loss is reduced due to the fact that the input voltage is split among the inverter modules. Furthermore, since the transformer is eliminated, the loss in the SAB magnetic component scales down with power. These favorable characteristics can be seen in the relatively flat experimentally measured efficiency curve shown in Fig. 3.22. The peak efficiency of 99% is measured at 40% of load, and the full-load efficiency is 97.5%. At 20% load, the measured efficiency is 98%. Fig. 3.23 shows the loss budget at various power levels and an

excellent match between the loss model and the experimentally measured loss. One may note that conduction losses associated with PCB traces are significant at intermediate and high loads, while the inductor losses are relatively low at all power levels, both indicating that there are potentials for further improvements in efficiency and power density.

Fig. 3.24 shows the efficiency at full power, for $\pm 20\%$ of output voltage variation from the nominal voltage, while keeping the input voltage fixed. As expected, the highest efficiency is obtained at the nominal output voltage of 50 V, where the converter operates with flat-top shaped currents, as shown in Fig. 3.18. Operating away from the nominal conversion ratio, the series-inductor current deviates from the flat-top shape, as shown in Fig. 3.25. This results in larger RMS currents and loss of ZVS, leading to reduced efficiency.

Thermal images of the inductor and the rectifier devices at full power, at the nominal conversion ratio, are presented in Fig. 3.26a and Fig. 3.26b, respectively. Fig. 3.26a shows a temperature pattern in the ferrite core, which coincides with the flux distribution shown in Fig. 3.14. At room ambient temperature, the converter operates continuously at the maximum temperature below 60°C with forced air flow of around 10 cubic feet per minute (CFM).

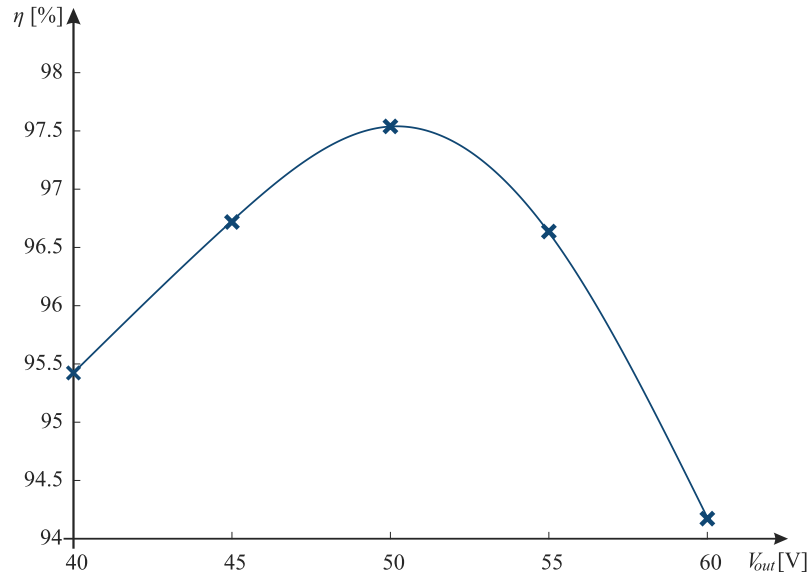
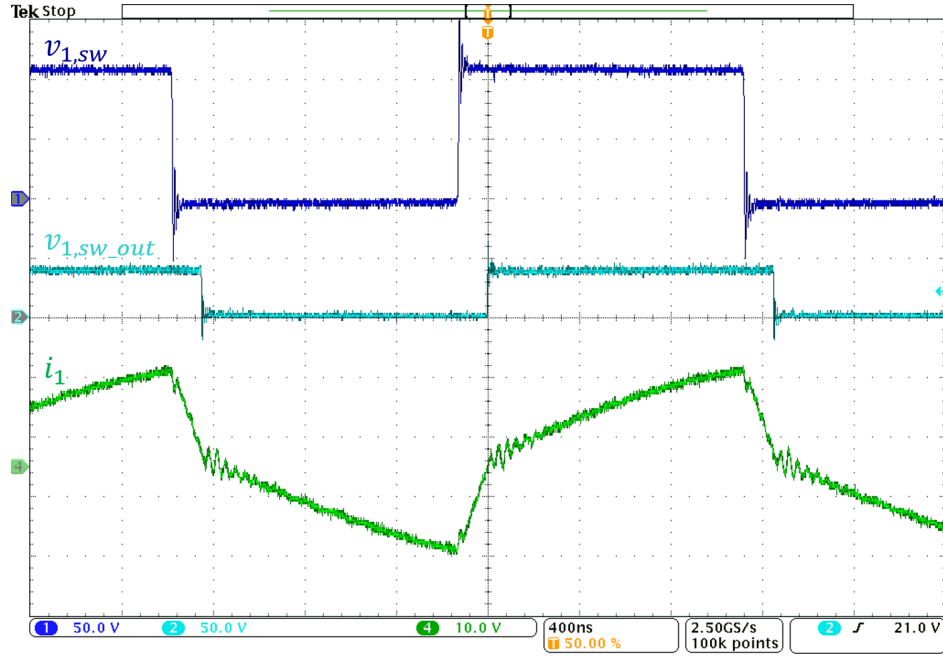
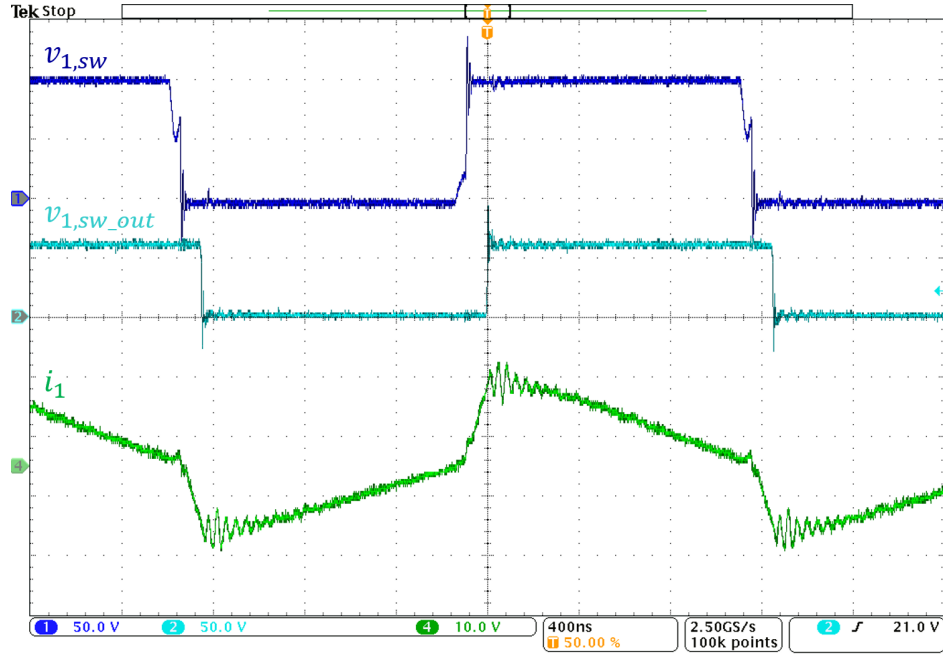


Figure 3.24: Measured efficiency of the experimental SAB prototype, as a function of the output voltage from -20% to $+20\%$ of the nominal voltage, at fixed output power of 3 kW.



(a) 400-to-40 V.

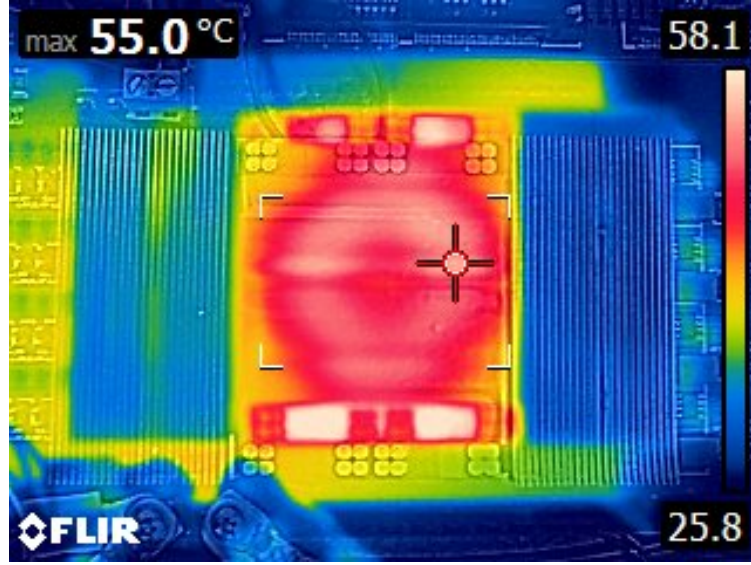


(b) 400-to-60 V.

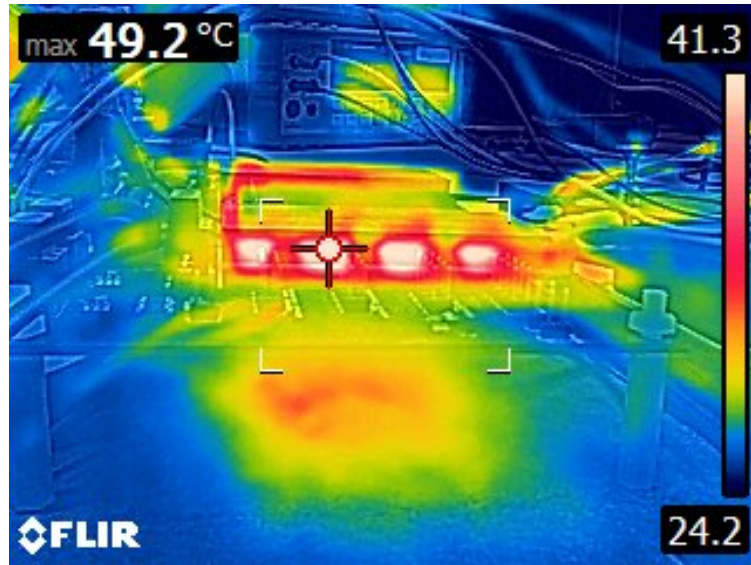
Figure 3.25: Experimental waveforms in the SAB prototype operating at $\pm 20\%$ of the nominal output voltage at 3 kW: inverter 1 switch-node voltage $v_{1,sw}$, rectifier 1 switch-node voltage $v_{1,sw,out}$, and series inductor current i_1 .

Table 3.4 shows a comparison between the transformerless SAB prototype and several best

performing designs based on LLC converters with integrated matrix transformers [33, 89, 36], as well as the designs presented in [42] and [25]. Although the SAB prototype operates at almost the lowest switching frequency, a competitive power density is achieved, while the light-load and peak



(a) Thermal image of the SAB prototype (top view) showing temperature of the coupled-inductor core.



(b) Thermal image of the SAB prototype (side view) showing temperature of the rectifier devices.

Figure 3.26: Thermal images of the SAB prototype taken at 3kW output power. The ambient temperature is 25°C.

Table 3.4: Comparison of 400-to-48 V, 3 kW prototypes

	Power density	f_{sw}	$\eta_{20\%}$	η_{pk}	$\eta_{100\%}$
[33]	$600 \frac{W}{in^3}$	1 MHz	95.0%	97.7%	97.2%
[89]	$400 \frac{W}{in^3}$	500 kHz	96.0%	98.5%	98.3%
[36]	$450 \frac{W}{in^3}$	1 MHz	94.5%	97.4%	97.0%
[42]	$522 \frac{W}{in^3}$	1 MHz	96.8%	98.6%	98.5%
[25]	$140 \frac{W}{in^3}$	350 kHz	97.3%	98.3%	98%
This work	$400 \frac{W}{in^3}$	400 kHz	98.0%	99.0%	97.5%

efficiencies are notably higher. At 20% load, losses in the SAB converter are more than two times lower compared to the transformer-isolated designs.

3.5 Chapter Summary and Conclusions

A stacked active bridge (SAB) modular dc-dc converter is presented as an alternative to transformer-isolated approaches in high step-down applications. The SAB inverter stage is composed of series stacked, capacitively coupled half-bridge modules, while the output consists of parallel connected rectifier stages. The SAB converter exhibits operating and control characteristics similar to the dual active bridge converter (DAB). Soft charging of dc capacitors, as well as zero voltage switching of both inverter and rectifier devices are facilitated by series inductors. Given the stacked transformerless architecture, losses in the magnetics scale with load and light-load partial-ZVS losses are reduced.

In addition to the simple DAB-like operation of the stackable converter architecture, which does not require an isolation transformer, the main contributions of the work include two new modeling and design aspects. Firstly, effects of timing mismatch and switch node parasitic capacitances on the input capacitor voltage balancing are analyzed. It is shown that natural voltage balancing can easily be achieved in practice. Secondly, four possible realizations of the series inductors are analyzed and compared in terms of losses while keeping the same boxed volume. It is found that the realization with four inductors coupled on the same custom ferrite core results in the minimum

loss among the considered candidates.

A 400-to-48 V, 3 kW experimental SAB prototype is constructed using low-voltage GaN devices. Operating at 400 kHz, the prototype features a power density of 400 W/in³, while the efficiency curve remains relatively flat over a wide load range, with 99% peak efficiency, 97.5% full-load efficiency, and 98% efficiency at 20% load.

Chapter 4

400 V-to-48 V Transformer-Isolated Stacked Active Bridge Converter with Integrated Magnetics

In contrast to the capacitively coupled SAB converter presented in the previous chapter, this chapter discusses a transformer-isolated SAB converter for applications that require galvanic isolation between the input and the output of the converter. To reduce the transformer size and losses, substantial advances have been made using matrix-transformer configurations in LLC converters [34, 33, 89]. To further reduce the size of the passives, the series inductance can be integrated with the transformer, by utilizing its leakage flux [36]. Transformers implemented in planar technology, with interleaved windings, inherently have very low leakage inductance. Recent work presented a solution with a modified winding arrangement and an additional center post in a matrix transformer to provide a leakage-flux path [66].

This chapter presents a novel approach to combining hybrid conversion with transformer isolation in an isolated stacked active bridge (iSAB) converter shown in Fig. 4.1. The conversion ratio is effectively realized through capacitively coupled series-stacked inverters, while the 1:1 transformers are used only for galvanic isolation purposes. Splitting the voltage on the primary side results in less volt-seconds across the transformer, which makes the transformer design less challenging compared to solutions with high turns-ratio transformers [20, 92]. Additionally, splitting the input voltage across the inverter stages allows for lower-voltage-rated, better-FOM devices. The series-stacked inverters also require less energy stored in the series inductors for soft switching of the semiconductor devices, therefore allowing a reduction in the size of passives [59]. Similar to the

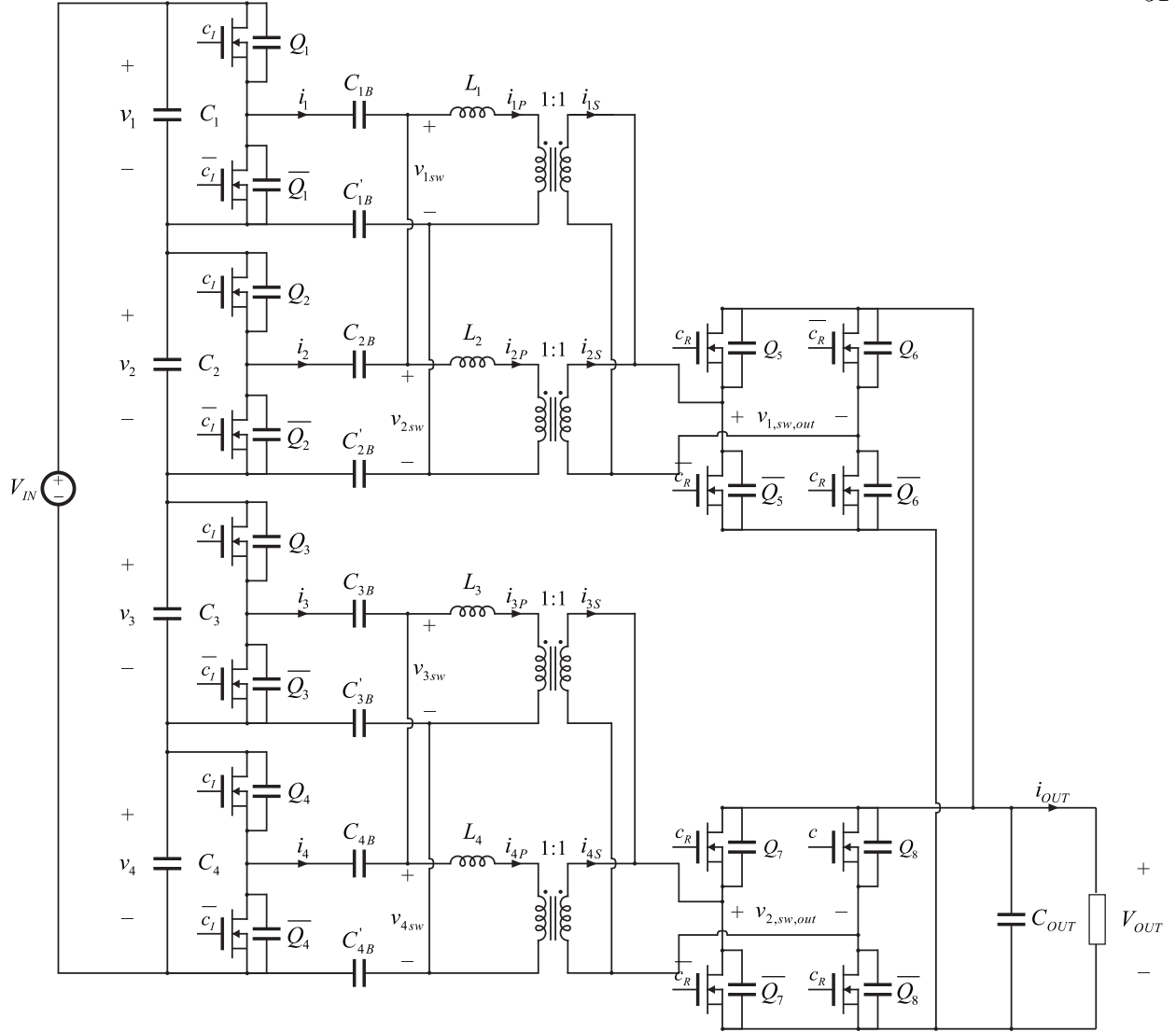


Figure 4.1: Isolated stacked active bridge (iSAB) dc-dc converter comprising $n = 4$ series-stacked, half-bridge inverters and $m = 2$ parallel-connected full-bridge rectifier modules. All transformers and series inductors are integrated on the same custom magnetic core with planar windings.

transformerless capacitively-coupled SAB in Chapter 3 [59], the iSAB operates well above the series resonance, with current waveforms and phase-shift control similar to the dual active bridge (DAB) converter. Unlike the matrix transformer used in LLC converters, which has a single primary winding, the iSAB transformer has a set of four primary-side windings. Additionally, the iSAB transformer features a large magnetizing inductance, making the phase displacement between the primary and secondary currents negligible, contrary to the LLC transformer. As the main contri-

bution, we show how all four transformers and series inductances can be effectively integrated on a custom core with novel planar winding arrangement featuring controllable leakage inductance and high magnetizing inductance, eliminating the need for air gaps in the magnetizing flux path.

The chapter is organized as follows. Section 4.1 presents the proposed core geometry and the planar winding arrangements of both primary and secondary windings, followed by the integrated magnetics design and model extraction through finite-element analysis (FEA) simulations in Section 4.2. Section 4.3 shows experimental results for a 400-to-48 V, 3 kW iSAB prototype operating at 400 kHz using low-voltage GaN devices.

4.1 iSAB Integrated Magnetics Structure

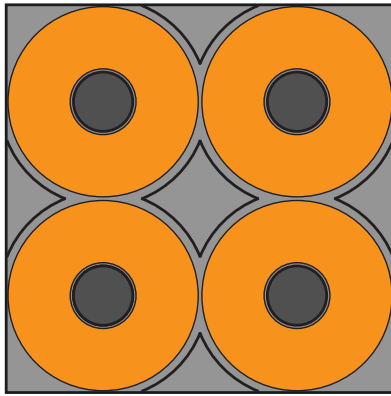
4.1.1 Core Geometry

The proposed integrated magnetics core geometry is shown in Fig. 4.2a. The core has four main posts (dark-gray highlighted in the figure), which do not have air-gaps, and their primary purpose is to carry the magnetizing flux. The center post and four auxiliary side posts are added to provide the path for the leakage flux. These posts are gapped, and the length of the gaps determines the leakage inductance.

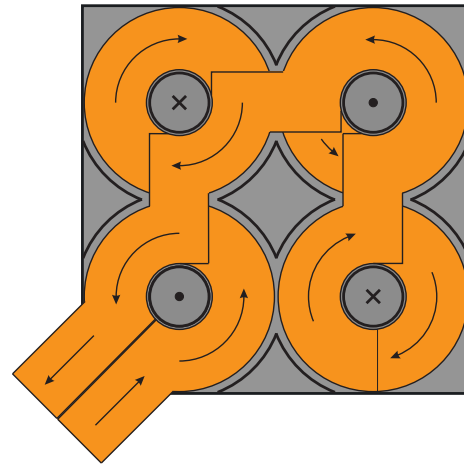
4.1.2 Primary Side Winding Arrangement and the Magnetizing Flux

Figure 4.2b shows the planar winding arrangement of a primary winding. A winding is wound around all four main posts, resulting in effectively four turns per layer. All four primary windings are wound in the same manner, each on a different PCB layer. This winding arrangement keeps the primary windings tightly coupled. As a result, the voltages among the stacked inverter modules are well balanced.

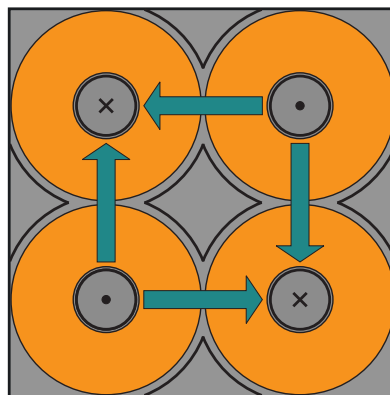
Figure 4.2c shows the path of the magnetizing flux. The flux that comes out of one of the main posts splits into two directions, and closes through the two adjacent main posts. The flux between two diagonal posts cancels out, which is why the magnetizing flux does not go through



(a) Cross-section view of the core geometry with four main posts dark-grey highlighted.

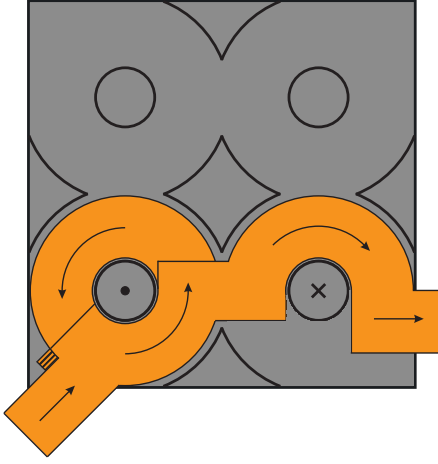


(b) Arrangement of a primary planar winding.

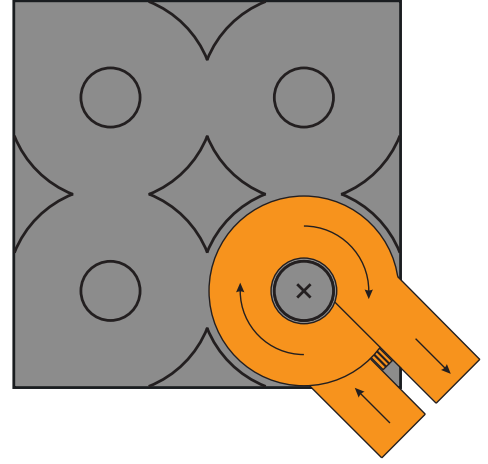


(c) Magnetizing flux path.

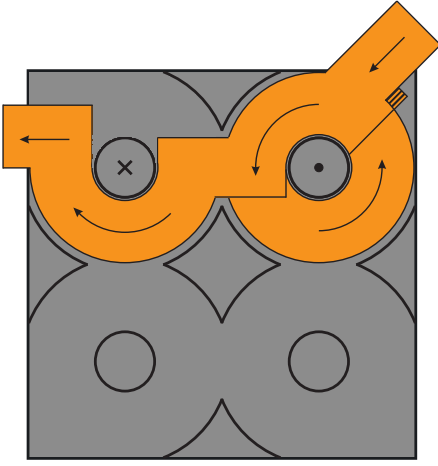
Figure 4.2: Integrated magnetics core and primary winding arrangement, together with illustration of the magnetizing flux path.



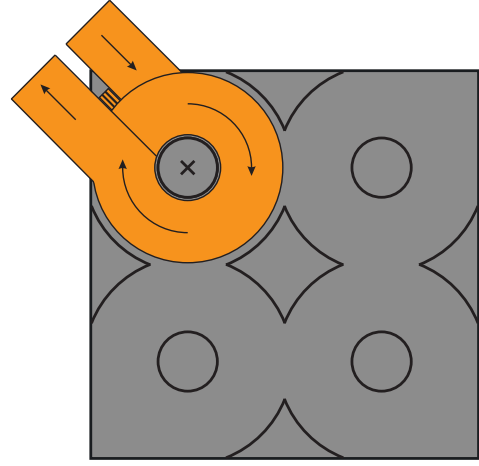
(a) Secondary winding 1.



(b) Secondary winding 2.



(c) Secondary winding 3.



(d) Secondary winding 4.

Figure 4.3: Winding arrangement of the secondary-side planar windings.

the center post. Instead, the magnetizing flux is shared exclusively between the main posts. The main posts do not have air gaps and the resulting magnetizing inductance is large.

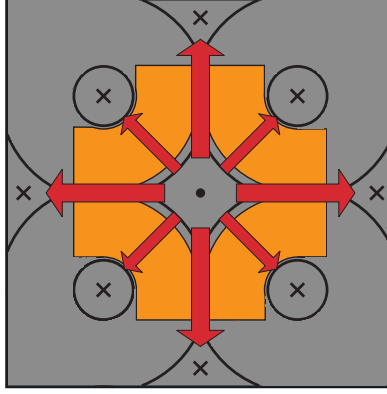


Figure 4.4: Leakage flux path.

4.1.3 Secondary-Side Winding Arrangement and the Magnetizing Flux

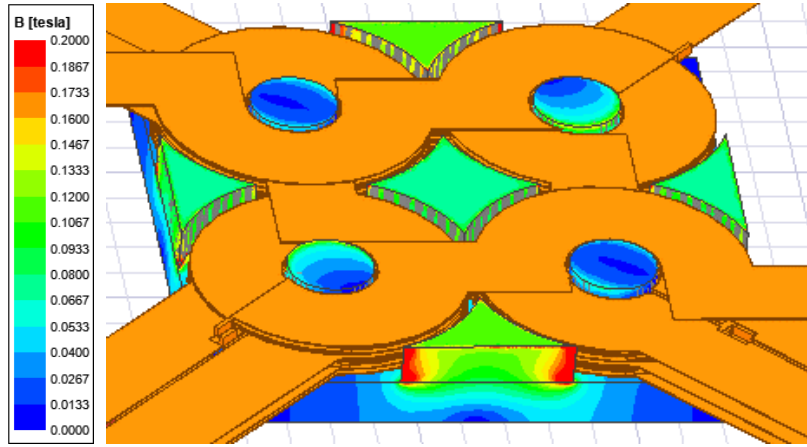
Figure 4.3 shows the winding arrangement for each of the secondary windings. Winding 1 has three turns wound around the first main post. The fourth turn extends around the second main post (Fig. 4.3a). Winding 2 has all of the four turns wound around the second main post (Fig. 4.3b). Both windings still have four turns each, but there are three turns around the first main post and five turns around the second main post, which creates an imbalance in the flux. Winding 3 and Winding 4 are symmetrical to Winding 1 and Winding 2, as can be seen from Fig. 4.3c and Fig. 4.3d.

The described arrangement of the secondary-side windings results in an equivalent single turn around the center post, as shown in Fig. 4.4. The leakage flux, excited by the equivalent single turn, comes out of the center post and closes through the auxiliary posts as well as the main posts. The center post and the four auxiliary posts are air-gapped, and the value of the leakage inductance can be tuned by adjusting the length of the airgaps.

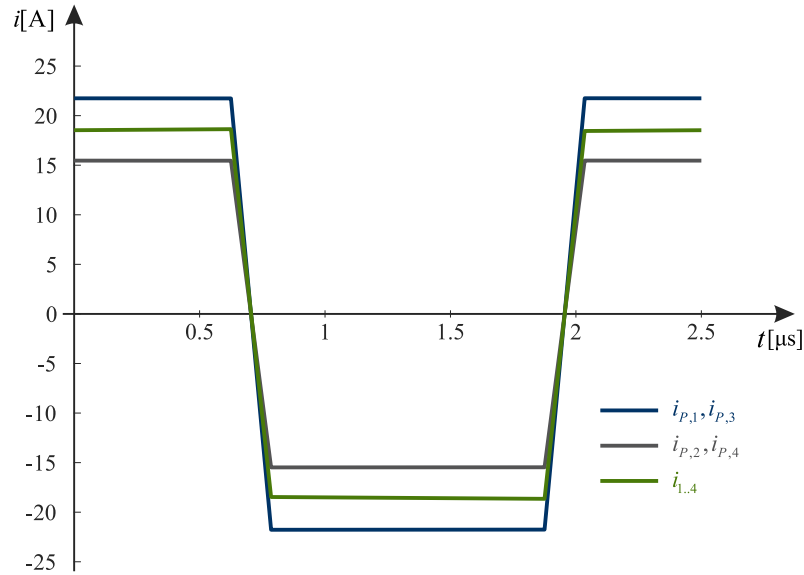
4.2 Integrated Magnetics Design using Finite Element Analysis (FEA)

Since the center post and the four auxiliary posts have airgaps, while the main posts do not, it is essential to accurately predict the needed length of the airgaps before manufacturing the custom core.

Figure 4.5a presents the results of FEA simulation using Ansys Maxwell. The software outputs an inductance matrix, which can be used with excitation waveform to verify the value of



(a) Illustration of FEA simulation of the integrated magnetics.



(b) Transformer and switch-node current waveforms.

Figure 4.5: FEA simulation of the integrated magnetics structure and iSAB current waveforms.

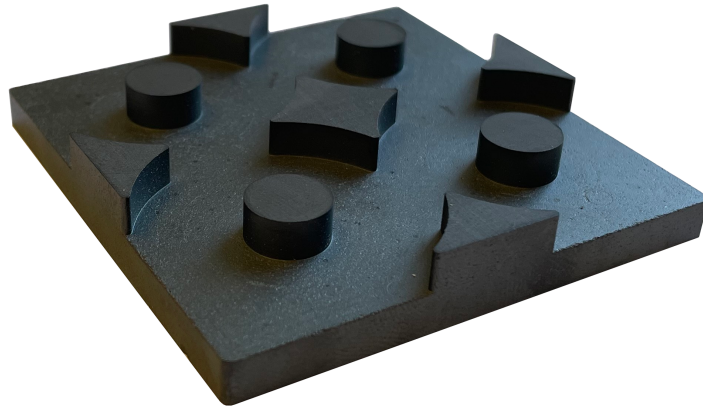
the equivalent series inductances. Airgaps are adjusted in an iterative manner until a desired value of the series inductance is obtained. Due to asymmetry in flux, the equivalent series inductance in Winding 1 and Winding 3 differs from the one in Winding 2 and Winding 4, as can be seen in Fig. 4.5b. This results in a slight imbalance between the amplitudes of the transformer currents. Unique to the iSAB topology, two windings with different currents can be connected in parallel. Parallel connection on the inverter side is possible due to the capacitive coupling of the stacked inverter modules. The parallel connections result in equal currents through all semiconductor devices, even though the current amplitudes in the individual windings are slightly out of balance.

4.3 Experimental Results

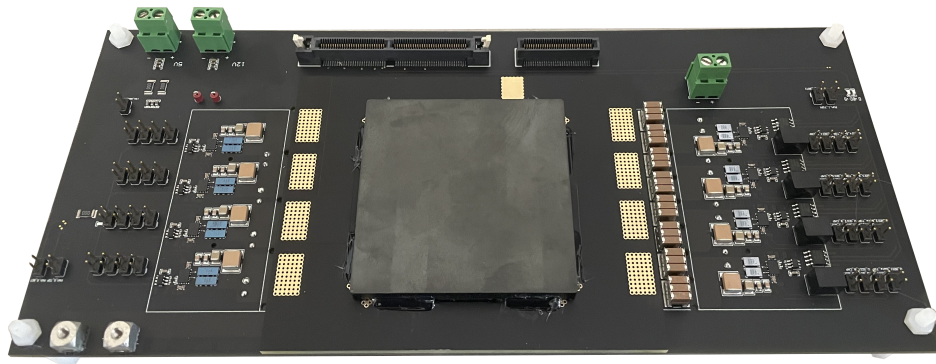
Figure 4.6a shows the custom core using DMR96 material from DMEGC. The core dimensions are $65\text{ mm} \times 65\text{ mm} \times 15.9\text{ mm}$. A photograph of the 400-to-48 V, 3 kW iSAB prototype is shown in Fig. 4.6b. 150 V GaN devices (EPC2033) are used in the inverter half-bridges, and 80 V GaN devices (EPC2021) are used in the rectifier bridges. Figure 4.7 shows waveforms of the inverter and the rectifier switch-node voltages, as well as one of the series inductor currents measured at the rated power. Both switching nodes achieve ZVS, while the current has the expected low-RMS flat-top shape. Fig. 4.8 shows an experimentally measured efficiency curve, which is relatively flat over a wide range of load, with a peak efficiency of 96.7%.

4.4 Chapter Summary and Conclusions

An isolated stacked active bridge (iSAB) dc-dc converter is presented in this chapter. The iSAB converter is suitable for high step-down applications that require galvanic isolation. The iSAB inverter stage is composed of series-stacked capacitively coupled half-bridge modules, whereas the output consists of parallel connected rectifier stages. The iSAB converter features operating waveforms and phase-shift control similar to the dual active bridge (DAB) converter. The soft charging of dc capacitors, as well as zero voltage switching of both inverter and rectifier devices, is facilitated by the series inductors. The burden of attaining a high conversion ratio is shifted from



(a) “E” part of the custom ferrite core.



(b) iSAB prototype board with the planar integrated magnetics assembled.

Figure 4.6: Photograph of the 3 kW, 400-to-48 V iSAB prototype.

the transformer to the series-stacked active bridges at the input.

The main contribution of this chapter is the integrated magnetics structure, which combines the transformers and the series inductances. A novel winding arrangement for the primary and

secondary planar windings is described. The primary winding arrangement results in strong coupling between the four primaries and, therefore, good voltage balancing among the series-stacked inverter modules. The secondary winding arrangement results in an equivalent single turn around

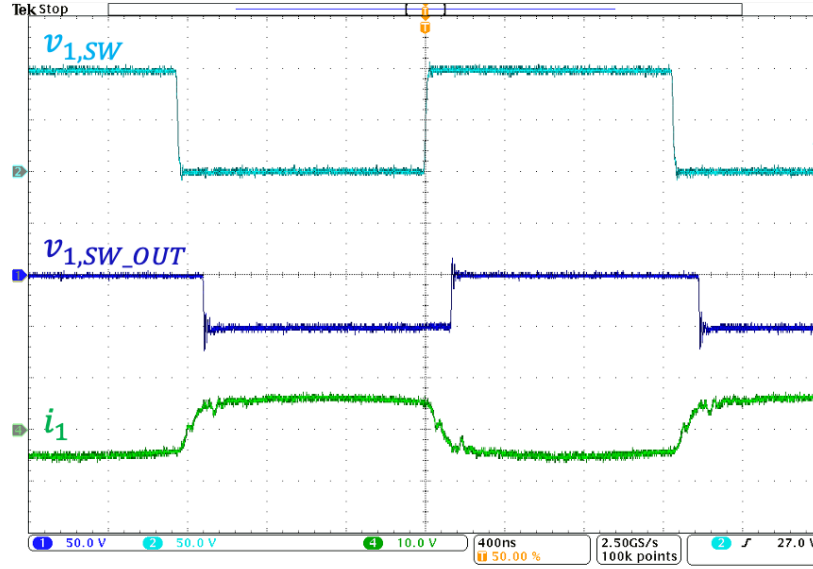


Figure 4.7: Experimental waveforms in the 400-to-48 V iSAB prototype operating at 3 kW: inverter 1 switch-node voltage $v_{1,sw}$, rectifier 1 switch-node voltage $v_{1,sw,out}$, and series inductor current i_1 .

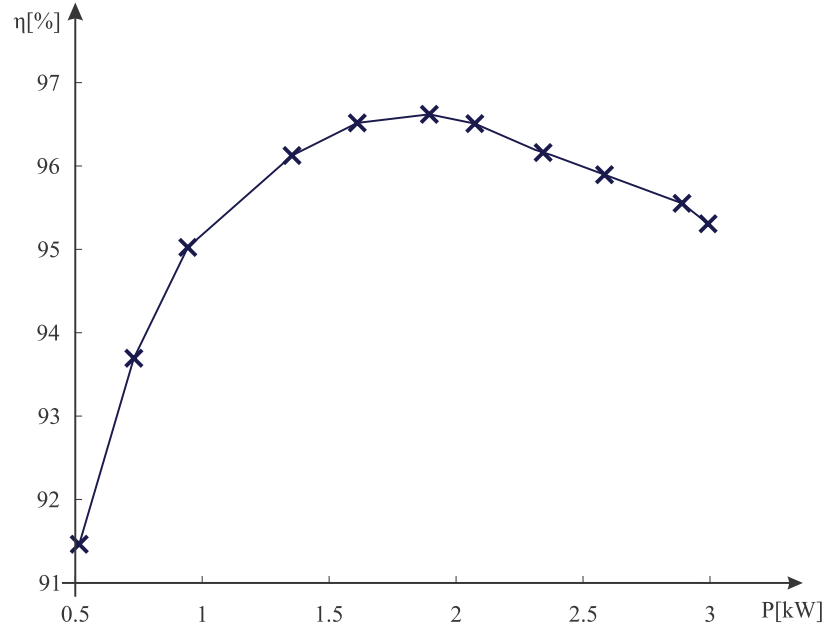


Figure 4.8: Measured efficiency of the experimental iSAB prototype as a functions of the output power from 10% to 100%.

the center post, which provides excitation of the leakage flux. Four auxiliary posts are added, to provide an additional path for the leakage flux to close, reducing the imbalance of the flux in the main posts.

A 400-to-48 V, 3 kW experimental iSAB prototype is constructed using low-voltage GaN devices. Switching at 400 kHz, the prototype features a relatively flat efficiency curve over a wide load range, with a peak efficiency of 96.7%.

Part II

Modular Silicon Carbide (SiC) Based String Inverters for Medium-voltage Transformerless PV Systems

Chapter 5

Design and Optimization of a Quadruple Active Bridge DCX Stage in a DC to Three-Phase AC Module for Medium-Voltage Grid Integration

5.1 Introduction

Fig. 5.1 shows a stackable modular architecture, where each module has a dc port and three isolated single-phase ac ports [4]. The module dc port and the ac ports can be used independently, or stacked in parallel or in series. For example, in the architecture shown in Fig. 5.1, the dc ports are tied to LV dc sources such as PV strings, while ac ports stacked in series are connected to an MV three-phase grid. The architecture features an interesting property of eliminating twice the line frequency pulsating power on the dc port of each module, thus eliminating the need for bulky energy storage. As shown in Fig. 5.2, each module contains a quadruple active bridge (QAB) creating three isolated dc link voltages, each followed by a single-phase dc-ac inverter bridge. The QAB, which operates as a fixed-ratio converter, *i.e.*, as “dc transformer” (DCX), provides galvanic isolation between the primary and each of the individual ac phases, so the modules can be flexibly stacked on the ac side.

The QAB outputs connected to phases A , B , and C deliver time-varying power $p_A(t)$, $p_B(t)$, and $p_C(t)$, respectively, each having a dc and twice-line-frequency ac component. The three currents add up on the primary side, such that dc power is transferred from the input, and the dc-link capacitance requirements are relaxed. This is an advantage compared to single-phase systems where the dc-link capacitors are sized for energy storage at twice the line frequency [82, 94]. In contrast, the dc-link capacitors are sized here to filter the switching ripple in the secondary-bridge

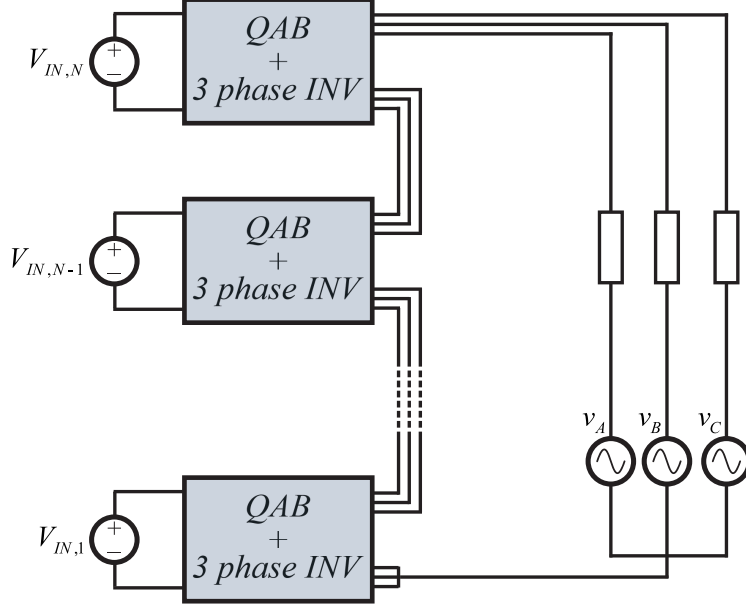


Figure 5.1: System architecture with cascaded isolated inverter modules [4]. The module configuration is shown in Fig. 5.2.

output current and the inverter input current.

The fact that the power fluctuates from zero to twice the average power on each secondary side during a line cycle presents challenges with respect to soft-switching of the secondary side bridges. This is similar to the loss of zero-voltage switching (ZVS) in lightly loaded dual-active-bridge dc-dc converters where inductively stored energy is insufficient to achieve soft charging and discharging of the switching-node capacitance [52, 49]. This capacitance consists of power MOSFET capacitances, inductor and transformer winding capacitance, and printed circuit board (PCB) parasitic capacitance.

Dual active bridge (DAB) converters have been used in applications that process ac power, such as ac-dc rectifiers [32, 31, 83] and ac-ac converters [71]. A modulation strategy for operating DABs under soft switching conditions throughout the entire operating range was proposed in [67], but the effects of the device output capacitances were not fully taken into account. The work in [52] showed that a reduced magnetizing inductance can lead to an extended ZVS range, but interactions between the magnetizing inductance and the device output capacitances were not

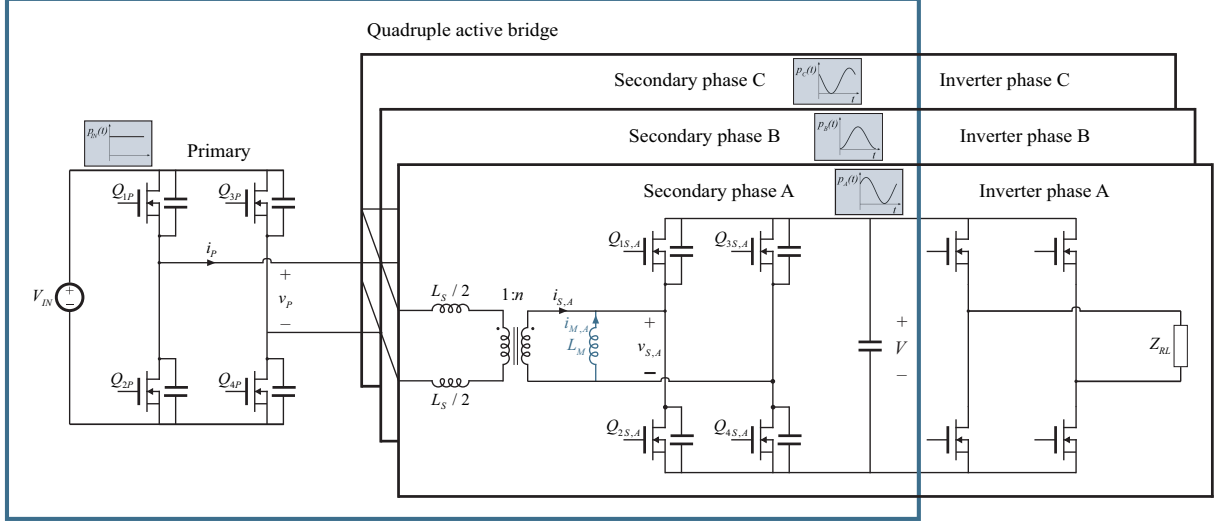


Figure 5.2: Transformer-isolated inverter module using a quadruple active bridge (QAB) dc-dc converter operated as a fixed-ratio “dc transformer” (DCX).

addressed. Utilization of the transformer magnetizing current to extend ZVS to light load region was also proposed in [11, 78]. This approach relies on relatively complex high-resolution dead-time control to account for multiple resonant periods, which in practice may result in the loss of ZVS. Facilitating ZVS transitions by utilizing magnetizing current was also discussed in [38] for a DCX based on a series resonant converter (SRC).

Switching transitions and ZVS conditions in the QAB stage shown in Fig. 5.2 differ from the conditions in DAB converters, so that aforementioned previously reported analysis and mitigation techniques do not directly apply. Unique to the QAB stage in Fig. 5.2 is that, assuming a balanced three-phase system, the primary-side power is dc, which means that ZVS can be accomplished throughout the line cycle on the primary bridge. However, the loss of ZVS on the secondary side during low-power intervals of an ac line period results in reduced system efficiency. This work proposes a solution for ZVS operation of the QAB over the entire ac line cycle by optimally utilizing the magnetizing currents of the transformers (or separate auxiliary inductors), as illustrated in Fig. 5.2 [60]. By reducing the magnetizing inductance of the transformer, circulating currents are introduced through the secondary sides of the QAB. The circulating currents greatly reduce switching loss at the cost of slightly increased conduction loss.

The reduced magnetizing inductance is not needed to achieve ZVS at all points during the line cycle at full load. However, while operating at lower average power levels, the energy provided by the series inductance becomes insufficient to achieve ZVS over a larger portion of the line cycle, which is why the circulating current due to the reduced magnetizing inductance helps with ZVS and results in improved efficiency. As an alternative, a larger series inductance could be used, but this approach would result in reduced efficiency at full load.

A detailed analysis of the switching sequence during primary and secondary dead-time intervals and the ZVS transition at zero power transfer is given in Sections 5.2 and 5.3. Analysis presented in Section 5.2 neglects effects of the parasitic capacitance across the series inductors on the ZVS transition. The results of this analysis are validated on a lower power rated, proof of concept prototype, where the magnetic components are implemented with litz-wire based windings, that inherently have low winding capacitance. Section 5.3 shows a more complex version of the analysis, considering parasitic capacitance across the series inductors. The results are validated on a lower power rated prototype for the design procedure described in Section 5.2. The design procedure described in Section 5.3 is validated on a full power rated prototype, with the windings of the magnetic components implemented in planar technology with more pronounced stray winding capacitance. The procedure of selecting the converter parameters to minimize the circulating currents, while maintaining ZVS at all times is developed in Sections 5.2.1.1, and 5.3.2 for the two scenarios, respectively. The critical zero-power operating point is discussed in detail, including parasitic capacitance effects, and approximate closed form expressions are found for choosing the magnetizing inductance and the dead times. The nonlinear nature of the device parasitic capacitance is taken into account based on the approach described in [17]. Section 5.4 investigates how the choice of the maximum phase shift, for a given power level, affects losses in the converter, assuming the design discussed in Section 5.3.1. The loss analysis addresses major loss mechanisms, including semiconductor conduction losses, as well as core and conduction losses in the magnetics. The optimal values of the maximum phase shift and thereby the series inductance are chosen to minimize the losses. Experimental verification results on a 1 kV, 10 kW SiC-based prototype are

presented in Section 5.5, while Section 5.6 concludes the chapter.

5.1.1 Control Signals for Zero Voltage Switching at Zero Instantaneous Power Transfer in One Phase

To guarantee ZVS operation of a particular phase over the entire line cycle, it is sufficient to show how ZVS can be achieved at the zero power transfer instant.

Over a line cycle, the power processed by each secondary is determined by the corresponding phase shift between the secondary and the primary full bridge:

$$\begin{aligned}\varphi_A(t) &= \varphi_m \sin^2(\omega_0 t) \\ \varphi_B(t) &= \varphi_m \sin^2\left(\omega_0 t + \frac{2\pi}{3}\right) \\ \varphi_C(t) &= \varphi_m \sin^2\left(\omega_0 t - \frac{2\pi}{3}\right),\end{aligned}\tag{5.1}$$

where φ_m is the maximum phase shift, and ω_0 is the angular line frequency.

Consider the time instant when the power processed by phase A is zero, while phases B and

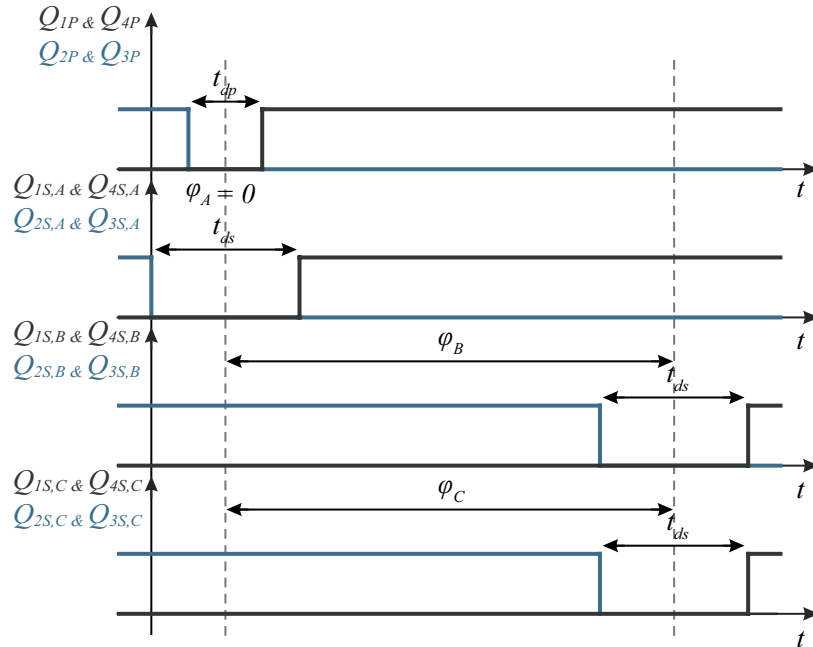


Figure 5.3: QAB switch control signals at the time when the secondary Phase A processes zero power.

C contribute non-zero instantaneous power levels to maintain constant overall power in the three-phase module. The corresponding switch control signals are shown in Fig. 5.3. The phase shift φ_A between the primary bridge and the phase A secondary bridge is zero, so that the corresponding control pulses are centered around the same instant.

The solution presented in this section is based on sizing the magnetizing inductance and a proper combination of the primary and secondary-side dead times.

5.2 ZVS Sequence Analysis Neglecting the Parasitic Capacitance of the Series Inductor

5.2.1 Zero Voltage Switching at Zero Instantaneous Power Transfer in One Phase

Theoretical, model-based waveforms during the rise-time transition of the secondary switching node are shown in Fig. 5.4. Definitions of the time instants and the time intervals during the transition are given in Tables 5.1 and 5.2, while the corresponding equivalent circuit models for the switching sequence consisting of Intervals I, II and III are shown in Fig. 5.5.

At the beginning of time Interval I (Fig. 5.5(a)), the secondary side switches $Q_{2S,A}$ and $Q_{3S,A}$ are turned off. The magnetizing inductance current $i_{M,A}$ starts charging voltage dependent switching-node capacitance $C_S(v)$ of the phase A secondary bridge, and the switching node voltage $v_{S,A}$ starts increasing. As $v_{S,A}$ increases, a negative voltage is applied across the series inductance, and the current $i_{S,A}$ starts decreasing.

The primary-side switches Q_{2P} and Q_{3P} turn off at the beginning of Interval II. The equivalent

Table 5.1:
Time instants of the
switching sequence
during ZVS
transition

T_1	$0.5(t_{ds} - t_{dp})$
T_2	$0.5(t_{ds} + t_{dp})$
T_3	t_{ds}

Table 5.2:
Time intervals of the
switching sequence
during ZVS
transition

Interval I	$0 \leq t < T_1$
Interval II	$T_1 \leq t < T_2$
Interval III	$T_2 \leq t < T_3$

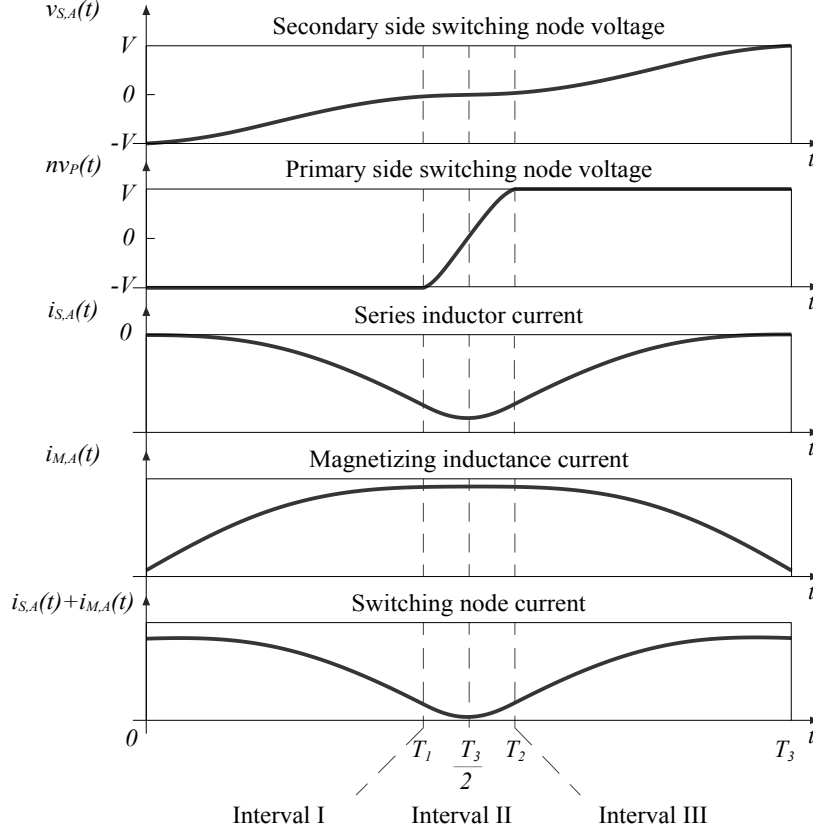


Figure 5.4: Model-based waveforms of the ZVS transition at the zero power transfer instant for Phase A. Referring to Fig. 5.3, $T_3 = t_{ds}$ and $T_2 - T_1 = t_{dp}$.

circuit in Interval II is shown in Fig. 5.5(b). During this interval, phases B and C are charging the switching-node capacitance $C_P(v)$ on the primary side. It is assumed that the QAB is closed-loop controlled to operate as a DCX, so that $v_{S,B}$ and $v_{S,C}$ can be considered constant voltage sources. The rise time of the primary side switching node v_P is faster than $v_{S,A}$, because the sum of the currents $i_{S,B}$ and $i_{S,C}$ is much higher than the peak of the magnetizing current. At the mid-point of Interval II, nv_P becomes higher than $v_{S,A}$, and $i_{S,A}$ changes polarity. Interval II ends, completing the ZVS transition of v_P , at the end of the primary-side dead time t_{dp} .

Interval III starts with turning on switches Q_{1P} and Q_{4P} of the primary full bridge. The corresponding equivalent circuit is shown in Fig. 5.5(c). During this interval, current $i_{S,A}$ is increasing until $v_{S,A}$ reaches the end of the ZVS transition. At that instant, $Q_{1S,A}$ and $Q_{4S,A}$ are turned on, which ends Interval III and the secondary phase A dead time t_{ds} .

Table 5.3: System specifications and circuit parameters

P	Rated power
V	DC link voltage
n	Transformer turns ratio
f_{sw}	Switching frequency
φ_m	Maximum phase shift

It should be noted that the sum of the magnetizing and series inductance current ($i_{M,A} + i_{S,A}$) reaches a minimum in the middle of Interval II. If this current becomes negative, it will start discharging the secondary side switching-node capacitance $C_S(v)$, which means that it would not be possible to complete the ZVS switching sequence as described above. Fig. 5.4 shows theoretical waveforms for the case when the minimum of ($i_{M,A} + i_{S,A}$) is zero. This represents the optimal design, in the sense of achieving ZVS operation while minimizing peak of the magnetizing inductance current, and therefore minimizing the conduction losses introduced by the circulating current.

5.2.1.1 Parameter Selection for Minimum Peak Magnetizing Current

In order to achieve ZVS at zero power transfer, the following circuit parameters need to be determined:

- Primary dead time: t_{dp}
- Secondary dead time: t_{ds}
- Magnetizing inductance referred to the secondary side: L_M .

In the design approach detailed in this section, all the parameters are expressed in terms of the specifications and the circuit parameters shown in Table 5.3.

The series inductance

$$L_S = \frac{3V^2\varphi_m\left(1 - \frac{\varphi_m}{\pi}\right)}{4\pi n^2 f_{sw} P} \quad (5.2)$$

and the peak value of the primary side current

$$I_{P,pk} \approx \frac{nP}{V \left(1 - \frac{\varphi_m}{\pi}\right)} \quad (5.3)$$

are found using the standard steady-state solution for the active-bridge converters [4].

5.2.1.2 Primary side dead time

Since the sum of the currents $i_{S,B}$ and $i_{S,C}$ is much greater than $i_{M,A}$, the rise time of the primary side switching node can be analyzed neglecting the effect of the phase A secondary side current $i_{S,A}$. Therefore, the equivalent circuit in Fig. 5.5(b) can be reduced to a simple LC circuit. Charge equivalent capacitance can be used to accurately calculate the switching-node voltage rise time, under the assumption that the energy stored in the series inductor is much higher than the energy used for charging the switching-node capacitance

$$I_{P,pk} \gg \frac{2V}{n} \sqrt{\frac{C_{P,E}}{L_S}}. \quad (5.4)$$

Consequently, primary-side dead time can be found as

$$t_{dp} = \frac{2VC_{P,Q}}{nI_{P,pk}} = \frac{2C_{P,Q}V^2}{n^2P} \left(1 - \frac{\varphi_m}{\pi}\right). \quad (5.5)$$

5.2.1.3 Magnetizing inductance and secondary-side dead time

The switching sequence, described in Section 5.3.1, involves equivalent circuits shown in Fig. 5.5. Exact solution is complicated for two reasons: nonlinear nature of the switching node capacitances, and multi-resonant responses, especially in Interval II. An approximate, design-oriented analytical approach is developed in this section to arrive at relatively simple, yet accurate design guidelines for selection of the magnetizing inductance L_M and the secondary-side dead time t_{ds} .

Two approximations are applied in order to simplify the equivalent circuits in Fig. 5.5:

- The primary-side switching-node voltage v_P is approximated by a stair-step waveform during Interval II, as shown in Fig. 5.7. The approximation is justified by the fact that Interval

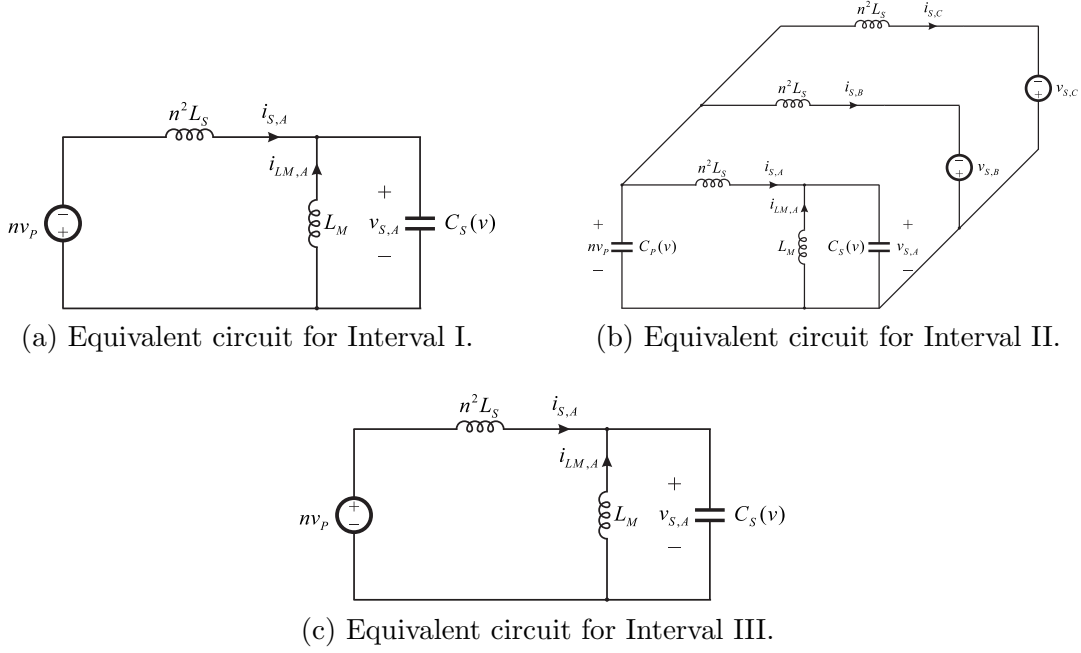


Figure 5.5: Equivalent circuits during ZVS transition at the zero power transfer instant for one of the phases.

II is relatively short compared to the overall ZVS transition time, and details of $nv_p(t)$ transitioning from 0 to V have little impact on the secondary-side ZVS transition waveforms. Furthermore, the approximate stair-step waveform is symmetric around the mid-point of the transition, which simplifies the analysis.

- The magnetizing inductance current is considered constant and equal to I_M during the ZVS transition. This is justified by the fact that the magnetizing inductance is much larger than the series inductance, so that variations in i_M are relatively small during the ZVS transition.

The approximate equivalent circuits of the ZVS switching sequence are shown in Fig. 5.6. Definitions of the time instants and time intervals corresponding to the approximate switching sequence are given in Tables 5.4 and 5.5. The approximations greatly reduce complexity of the analysis, simplifying the switching sequence states to second-order circuits well suited for state-

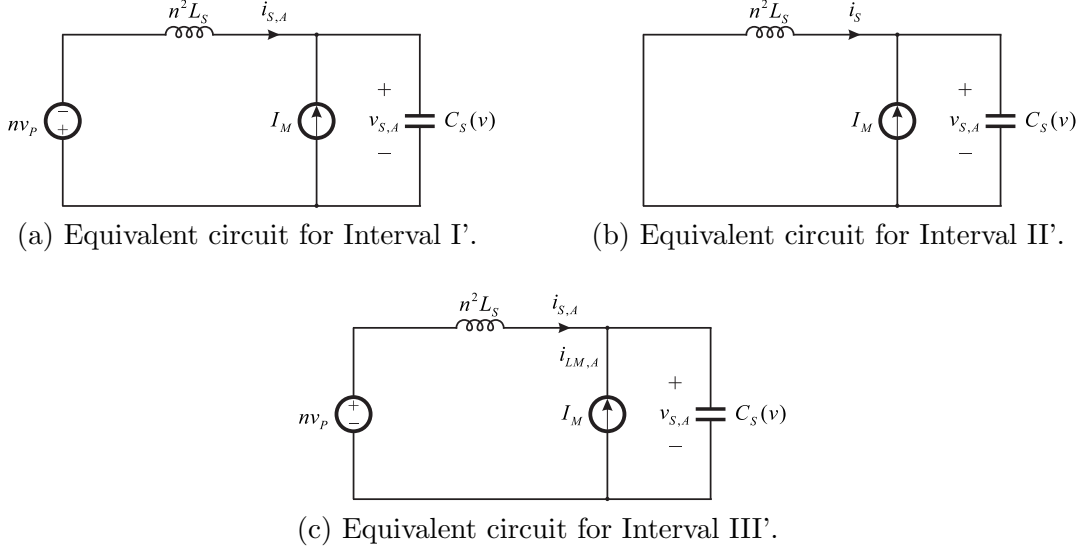


Figure 5.6: Approximate equivalent circuits during ZVS transition.

plane analysis. Since the switching sequence and the waveforms are symmetrical around $T_3/2$, as shown in Fig. 5.4, it is sufficient to perform the analysis over one half of the ZVS transition, from 0 to $T_3/2$.

In order to achieve ZVS with a minimum magnetizing current, $i_{S,A} + i_{M,A}$ should drop to zero at $T_3/2$, as discussed in Section 5.3.1. Equivalently, $i_{S,A}$ should drop to $-I_M$. From the approximate

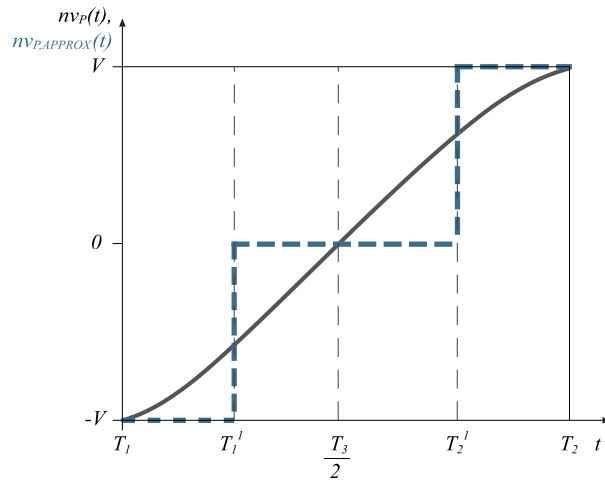


Figure 5.7: Exact and approximate waveforms of the primary side switching-node voltage $nv_p(t)$ during Interval II.

Table 5.4:
Time instants of the
approximated
switching sequence

T'_1	$0.5(t_{ds} - 0.5t_{dp})$
T'_2	$0.5(t_{ds} + 0.5t_{dp})$
T'_3	t_{ds}

Table 5.5:
Time intervals of the
approximated switching
sequence

Interval I'	$0 \leq t < T'_1$
Interval II'	$T'_1 \leq t < T'_2$
Interval III'	$T'_2 \leq t < T'_3$

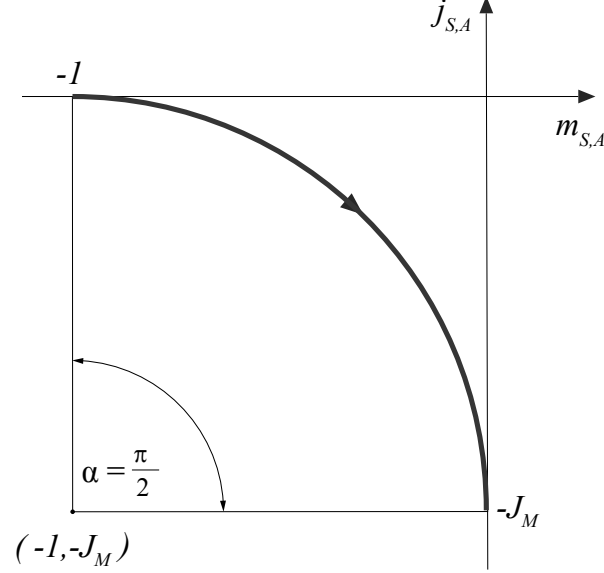


Figure 5.8: State plane trajectory during interval I'.

model in Fig. 5.7, it can be seen that the primary-side voltage becomes zero at T'_1 . Therefore, in order to keep $i_{S,A}$ constant and equal to $-I_M$, the secondary side switching node must drop to zero at T'_1 as well. Following this sequence of events, the entire half-transition is described by the circuit shown in Fig. 5.6(a), which further simplifies the analysis.

For state-plane analysis of the circuit in Fig. 5.6(a), a standard normalization is applied using the base values $V_{base} = V$ and $I_{base} = \frac{V_{base}}{R_0}$, where $R_0 = n\sqrt{\frac{L_S}{C_{S,EH}}}$. Since the analysis involves only one half of the ZVS transition, $C_{S,EH}$ is obtained by integrating the nonlinear $C_{S,hb}(v)$ curve up to one half of the full dc link voltage V . The normalized voltage and current can be written as $m_{S,A} = \frac{v_{S,A}}{V_{base}}$ and $j_{S,A} = \frac{i_{S,A}}{I_{base}}$.

Fig. 5.8 illustrates the state-plane trajectory during Interval I'. In order for the normalized

voltage to reach zero while the normalized current drops to $-J_M$, the following condition must be met

$$J_M = 1. \quad (5.6)$$

Denormalizing (5.6), the required amplitude of the magnetizing current can be found as

$$I_M = \frac{V}{n} \sqrt{\frac{C_{S,EH}}{L_S}} = 2 \sqrt{\frac{\pi f_{sw} C_{S,EH} P}{3 \varphi_m (1 - \frac{\varphi_m}{\pi})}} \quad (5.7)$$

and the required magnetizing inductance is

$$L_M = \frac{V}{4I_M} \left(\frac{1}{f_{sw}} - t_{ds} - t_{dp} \right) \quad (5.8)$$

where t_{dp} can be found from (5.5). It remains to determine the secondary-side dead time t_{ds} .

Since the energy stored in the magnetizing inductance is just enough to discharge the switching node capacitance, the charge equivalent linear capacitance cannot be used to determine the secondary-side dead time. The rise time of the secondary side switching node can be estimated more accurately by solving the circuit in Fig. 5.6(a)

$$t_{ds} = \frac{t_{dp}}{2} + 2 \int_0^{\frac{V}{2}} \frac{C_{S,hb}(v) dv}{\sqrt{I_M^2 - \frac{4}{n^2 L_s} \int_0^v C_{S,hb}(v_x) v_x dv_x}}. \quad (5.9)$$

This result for the secondary dead time is accurate, and can be used to properly set the dead time in a practical implementation. With the goal of arriving at a simpler, closed-form solution for the required magnetizing inductance, it should be noted that the impact of t_{ds} in (5.8) is relatively small. An approximate expression for t_{ds} can be found from state-plane analysis illustrated in Fig. 5.8 by noting that T'_1 interval corresponds to angle $\alpha = \pi/2$

$$\alpha = \frac{T'_1}{n \sqrt{L_S C_{S,EH}}} = \frac{\pi}{2}, \quad (5.10)$$

using the energy-equivalent secondary-side capacitance $C_{S,EH}$ evaluated over one half of the dc link voltage. Given that $T'_1 = 0.5(t_{ds} - 0.5t_{dp})$, (5.10) yields an approximate expression for the secondary-side dead time

$$t_{ds,approx} = \frac{t_{dp}}{2} + \pi n \sqrt{L_S C_{S,EH}} \quad (5.11)$$

where L_S and t_{dp} can be found from (5.2) and (5.5), respectively.

Finally, a closed-form expression for the required magnetizing inductance L_M follows from (5.8)

$$L_M \approx \frac{V}{4I_M} \left(\frac{1}{f_{sw}} - t_{ds,approx} - t_{dp} \right) \quad (5.12)$$

where, in terms of the circuit specifications and parameter values, t_{dp} can be found from (5.5), I_M from (5.7), and $t_{ds,approx}$ from (5.11).

5.2.2 Experimental results

The experimental setup of the isolated dc-to-3-phase ac module, using 900 V SiC MOSFETs (Wolfspeed Cree C3M0030090K) is shown in Fig. 5.9. The parameters of the converter are given in Table 5.6.

Primary-side dead time is calculated from (5.5), while secondary-side dead time and the magnetizing inductance are calculated according to (5.9) and (5.12), respectively, and the results are summarized in Table 5.7.

Table 5.6: Experimental prototype parameters

P	V	n	f_{sw}	φ_m	$C_{P,Q}$	$C_{S,EH}$
4 kW	600 V	1	100 kHz	20°	408 pF	312 pF

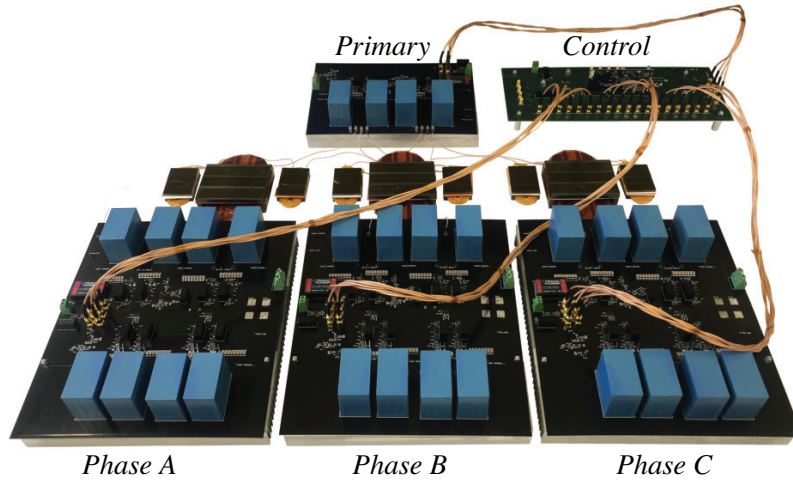


Figure 5.9: 600 V, 4 kW SiC-based experimental prototype.

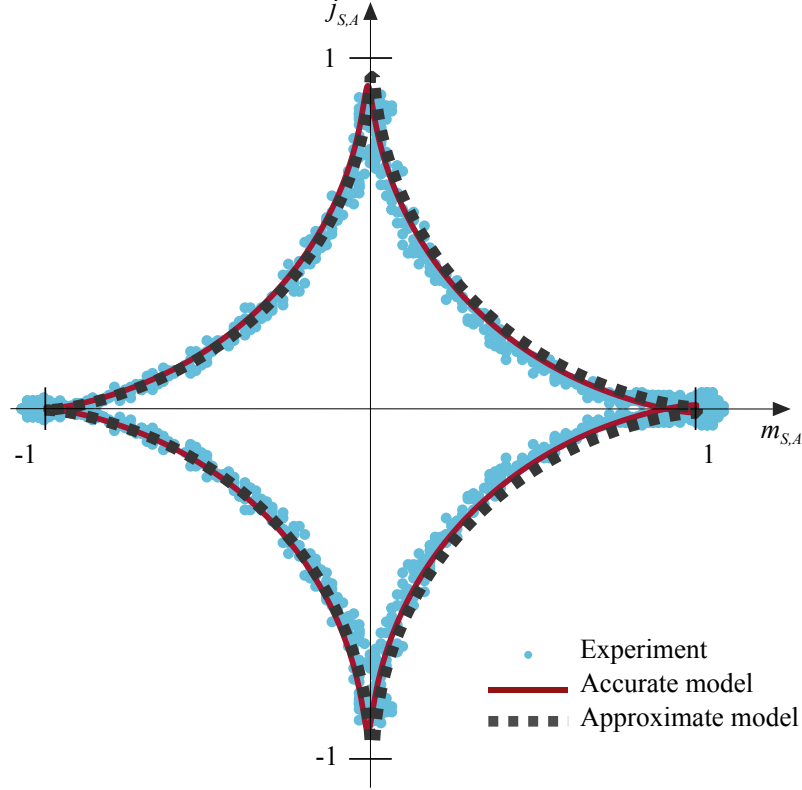


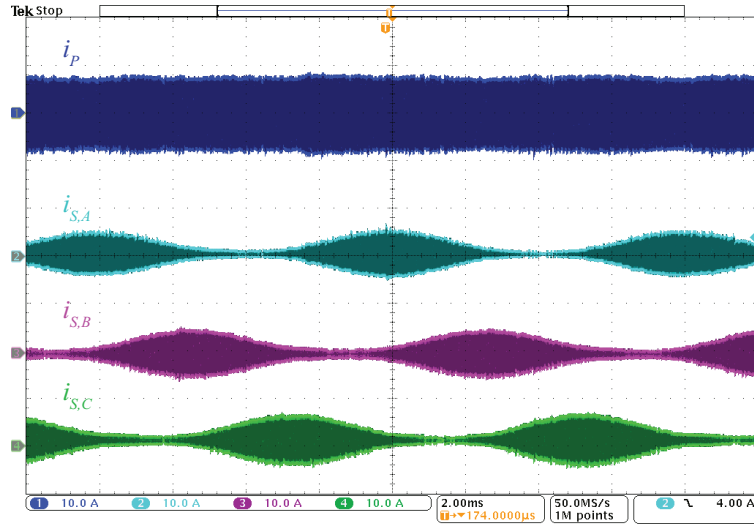
Figure 5.10: State plane trajectory at the time Phase A power is zero. Experimental results are overlapped with solutions based on accurate and approximate models.

Fig. 5.11 shows how the three-phase secondary QAB currents are summing up to a constant-envelope current on the primary side. The waveforms are shown for the currents $i_{S,A}$, $i_{S,B}$ and $i_{S,C}$ in Fig. 5.11(a), and the currents including the magnetizing currents in Fig. 5.11(b), which illustrate how the additional circulating currents are relatively small. Fig. 5.12(a) shows ZVS operation at the zero power crossing of phase A, while Fig. 5.12(b) confirms that the measured waveforms closely match the theoretical waveforms shown in Fig. 5.4.

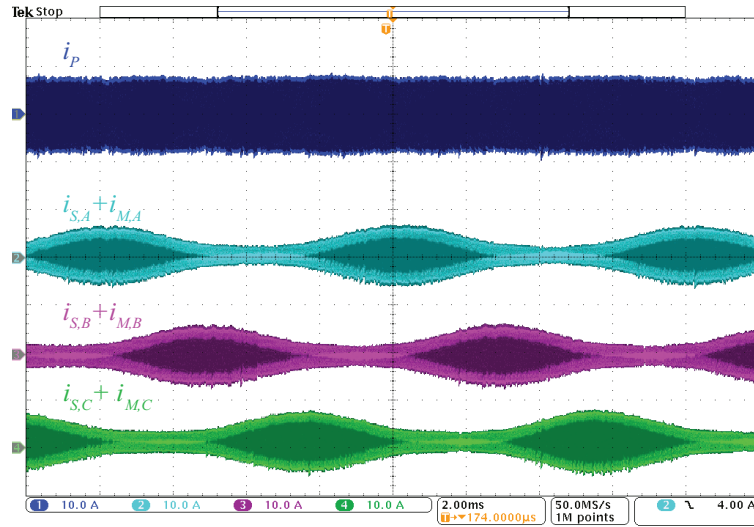
In order to verify the approximations introduced in Section 5.2.1.3, two model based simulations are performed, and compared with the experimental results. An accurate model is developed

Table 5.7: Design parameters

t_{dp}	t_{ds}	L_M
65 ns	548 ns	1.1 mH



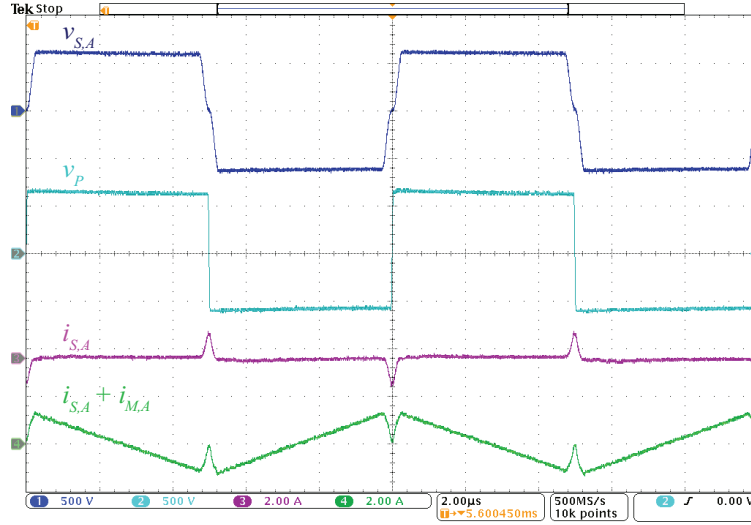
(a) Primary current i_P , and secondary currents through L_s .



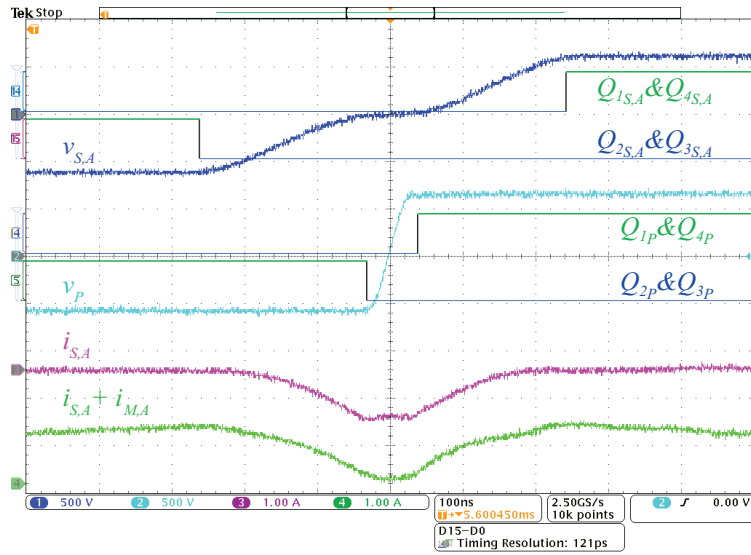
(b) Primary current i_P , and secondary currents through L_s and L_M .

Figure 5.11: Quadruple active bridge primary and secondary currents.

based on the equivalent circuits shown in Fig. 5.5. A simpler model, which is used to derive design equations in Section 5.2.1.1, is based on the equivalent circuits shown in Fig. 5.6. Fig. 5.10 shows a good agreement between the state-plane trajectories obtained from the accurate model, from the approximate model, and from the experimental waveforms.



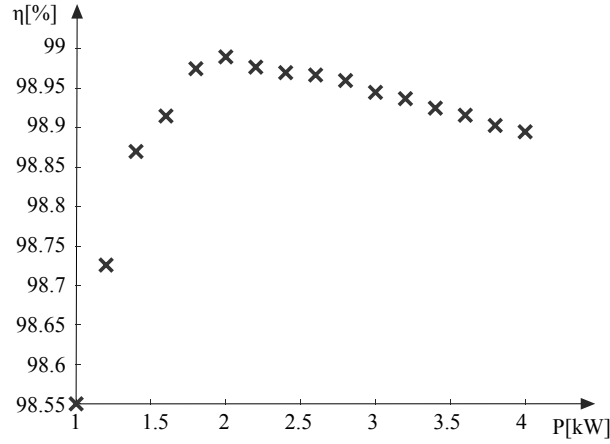
(a) Switching-node voltages $v_{S,A}$, v_P , and currents $i_{S,A}$ and $i_{S,A} + i_{M,A}$.



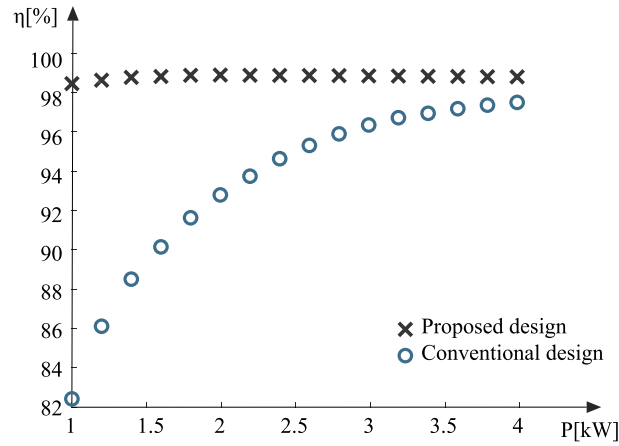
(b) Waveforms during ZVS transition.

Figure 5.12: Quadruple active bridge primary and secondary currents.

Measured efficiency of the prototype converter is shown in Fig. 5.13a as a function of the average output power. Efficiency remains greater than 98.5% from 1 kW to 4 kW, with a peak efficiency of 99.0%. In Fig. 5.13b, measured efficiency is compared with efficiency of the conventionally operated prototype where all the circuit parameters are the same, but the transformer core does



(a) Efficiency of the experimental prototype using the optimized magnetizing inductance and dead times.



(b) Measured efficiency of the conventionally operated prototype (with large magnetizing inductance), compared to the measured efficiency of the experimental prototype with optimized magnetizing inductance and dead times.

Figure 5.13: Efficiency measurements.

not include an air gap and the magnetizing inductance is much larger. The prototype with the optimized L_M and optimized dead times features a much flatter efficiency curve, and substantial efficiency improvements compared to the conventional design, especially at lower power levels. At the rated power (4 kW), measured efficiency of the conventionally operated prototype is 97.6%, while measured efficiency of the optimized prototype increases to 98.9%, which corresponds to an

overall loss reduction by more than 50%.

5.2.3 Summary of the Section

This part of work shows how the transformer magnetizing current can be used to achieve zero voltage switching (ZVS) throughout the line cycle in a transformer-isolated quadruple active bridge (QAB) dc-dc converter feeding three-phase ac output. By placing an airgap into the high frequency transformer's core, a circulating magnetizing current is introduced, which makes ZVS possible during low power transfer intervals. Simple phase shift modulation is employed, without the need for changing modes over the line cycle. A detailed analysis of the switching transient is presented, including effects of the nonlinear device capacitances. Suitable approximations are introduced to obtain closed form, design-oriented expressions for the magnetizing inductance, and the primary-side and secondary-side dead times, so that ZVS is achieved, while minimizing the magnetizing current, without loss of accuracy. The approach is particularly well suited for higher voltage applications, where hard switching losses can be significant. Experimental results on a SiC-based 600 V, 4 kW prototype operating at 100 kHz verify the model, and show that efficiency remains greater than 98.5% over 1-4 kW average output power, with 99.0% peak efficiency and more than 50% loss reduction at rated power compared to conventionally operated prototype. Efficiency improvements are even higher at lower power levels.

5.3 ZVS Sequence Analysis Considering the Parasitic Capacitance of the Series Inductor

5.3.1 Zero voltage switching at zero instantaneous power transfer in one phase

Similarly to Subsection 5.2.1, a zero - power crossing of a phase is considered for design of the magnetizing inductance and a proper combination of the primary and secondary-side dead times, with a difference that parasitic capacitance of the series inductor is taken into consideration.

Theoretical, model-based waveforms during the rise-time transition of the secondary switching node are shown in Fig. 5.14. Definitions of the time instants and the time intervals during the

transition are given in Tables 5.8 and 5.9, while the corresponding equivalent circuit models for the switching sequence consisting of Intervals I, II and III are shown in Fig. 5.15.

At the beginning of time Interval I (Fig. 5.15(a)), the secondary side switches $Q_{2S,A}$ and $Q_{3S,A}$ are turned off. The magnetizing inductance current $i_{M,A}$ starts charging voltage dependent switching-node capacitance $C_S(v)$ of the phase A secondary bridge, and the switching node voltage $v_{S,A}$ starts increasing. As $v_{S,A}$ increases, a negative voltage is applied across the series inductance, and the current $i_{S,A}$ starts decreasing.

The primary-side switches Q_{2P} and Q_{3P} turn off at the beginning of Interval II. The equivalent circuit in Interval II is shown in Fig. 5.15(b). During this interval, phases B and C are charging the switching-node capacitance $C_P(v)$ on the primary side. It is assumed that the QAB is closed-loop controlled to operate as a DCX, so that $v_{S,B}$ and $v_{S,C}$ can be considered constant voltage sources. The rise time of the primary side switching node v_P is faster than $v_{S,A}$, because the sum of the currents $i_{S,B}$ and $i_{S,C}$ is much higher than the peak of the magnetizing current. This implies that $\frac{dv}{dt}$ across the series inductance parasitic capacitance C_{L_S} is approximately constant, therefore the constant current through C_{L_S} charges $v_{S,A}$ linearly.

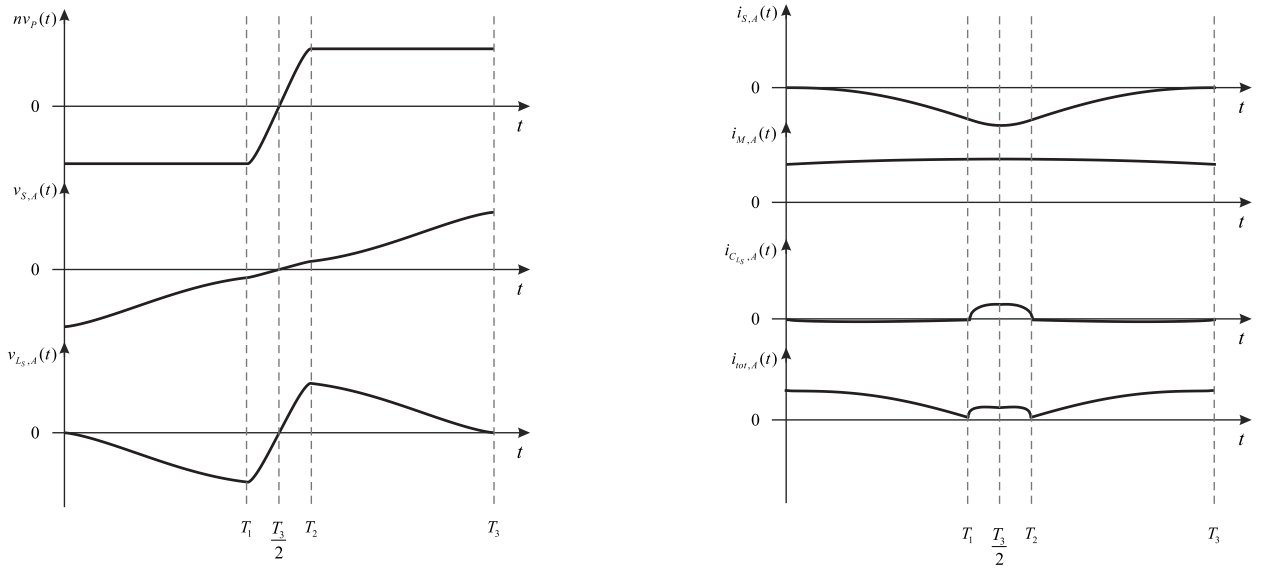


Figure 5.14: Model-based waveforms of the ZVS transition at the zero power transfer instant for Phase A. Referring to Fig. 5.3, $T_3 = t_{ds}$ and $T_2 - T_1 = t_{dp}$.

Table 5.8: Time instants of the switching sequence during ZVS transition

T_1	$0.5(t_{ds} - t_{dp})$
T_2	$0.5(t_{ds} + t_{dp})$
T_3	t_{ds}

Table 5.9: Time intervals of the switching sequence during ZVS transition

Interval I	$0 \leq t < T_1$
Interval II	$T_1 \leq t < T_2$
Interval III	$T_2 \leq t < T_3$

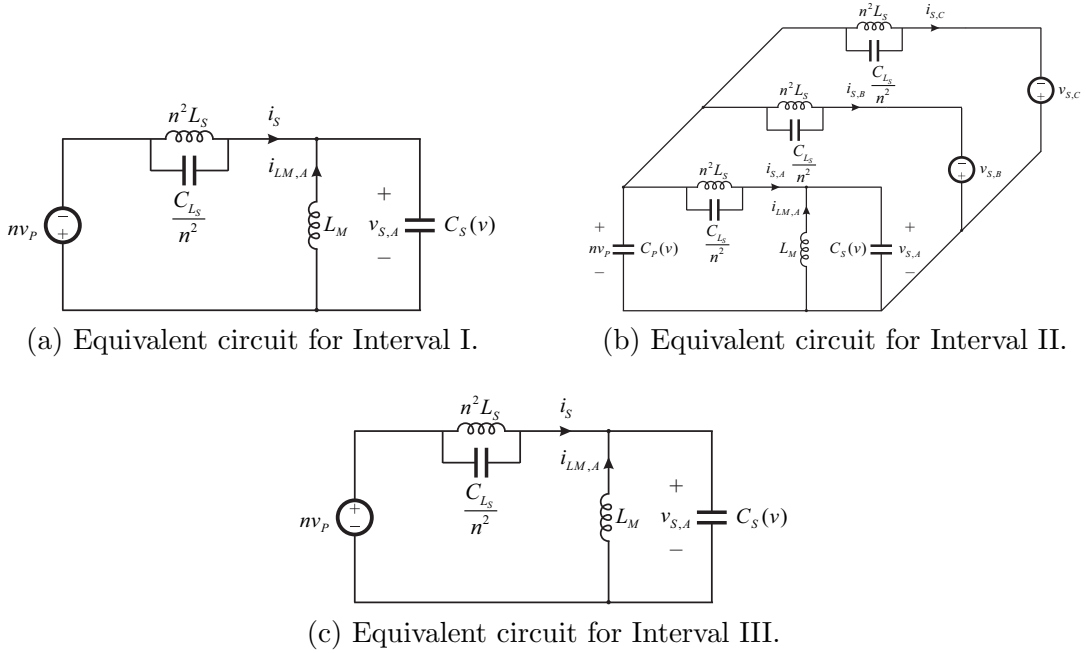


Figure 5.15: Equivalent circuits during ZVS transition at the zero power transfer instant for one of the phases.

At the mid-point of Interval II, nv_P becomes higher than $v_{S,A}$, and the slope of $i_{S,A}$ changes polarity. Interval II ends, completing the ZVS transition of v_P , at the end of the primary-side dead time t_{dp} .

Interval III starts with turning on switches Q_{1P} and Q_{4P} of the primary full bridge. The corresponding equivalent circuit is shown in Fig. 5.15(c). During this interval, current $i_{S,A}$ is increasing until $v_{S,A}$ reaches the end of the ZVS transition. At that instant, $Q_{1S,A}$ and $Q_{4S,A}$ are turned on, which ends Interval III and the secondary phase A dead time t_{ds} .

It should be noted that the total current that charges the switching node capacitance,

$$i_{tot,A} = i_{S,A} + i_{M,A} + i_{C_{LS},A} \quad (5.13)$$

reaches a minimum at the beginning of the Interval II. If this current became negative, it would start discharging the secondary side switching-node capacitance $C_S(v)$, which means that it would not be possible to complete the ZVS switching sequence as described above. Fig. 5.14 shows theoretical waveforms for the case when the minimum of $i_{tot,A}$ is zero. This represents the optimal design, in the sense of achieving ZVS operation while minimizing the peak of the magnetizing inductance current, and therefore minimizing the conduction losses introduced by the circulating current.

5.3.2 Parameter Selection for Minimum Peak Magnetizing Current

As one could note that the switching sequence presented in Section 5.3.1 and 5.2.1 is rather similar with the exception of interval II, where the secondary side switching node is being charged by the other two phases through the parasitic capacitance of the series inductor. Observing the approximate circuits shown in Fig. 5.17, it is straight forward to see that C_S doesn't affect the approximate calculation of the primary side deadtime. Therefore, the primary side deadtime calculation follows directly from Subection 5.2.1.2. The following Subections will focus on the secondary side analysis, e.i. calculation of the magnetizing inductance and the secondary-side dead time.

5.3.2.1 Nonlinear switching node capacitance

In the small-signal sense, capacitance at the half-bridge switching node is a parallel combination of the two device output capacitances, $C_{oss,hb}(v) = (C_{oss}(v) + C_{oss}(V_A - v))$, as shown in Fig. 5.16, where $C_{oss}(v)$ curve can be found from the device datasheet, and V_A is the dc voltage across the half bridge. The total half-bridge switching node capacitance is a combination of the device capacitances, series inductor and transformer winding capacitance, and the parasitic PCB trace capacitance. The half-bridge capacitances of the primary and the secondary side, denoted as

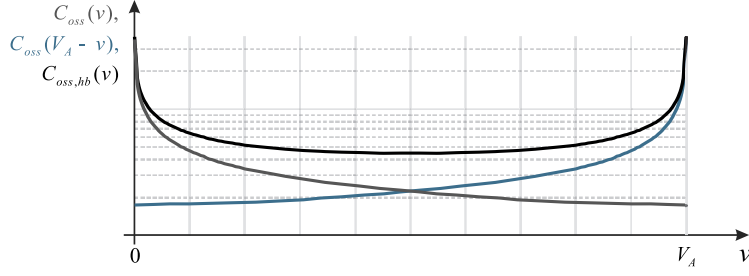


Figure 5.16: Half-bridge switching node device capacitance.

$C_{P,hb}(v)$ and $C_{S,hb}(v)$, respectively, can be found as:

$$C_{P,hb}(v) = C_{oss,hb,P}(v) + 2(3C_{L_s} + C_{PCB,P}), \quad (5.14)$$

$$C_{S,hb}(v) = C_{oss,hb,S}(v) + 2\left(\frac{C_{tr}}{n^2} + C_{PCB,S}\right). \quad (5.15)$$

It should be noted that C_{L_s} has been left out of $C_{S,hb}(v)$, since this capacitance will be treated separately from the rest of the lumped secondary-side capacitances. For the equivalent circuit representation used in Fig. 5.15 and Fig. 5.17, it is convenient to define full-bridge switching-node voltage dependent capacitances as $C_P(v) = C_{P,hb}(v)/2$ for the primary side, and $C_S(v) = C_{S,hb}(v)/2$, for the secondary side.

The energy and charge equivalent primary-side full-bridge switching-node capacitance are found, respectively, as follows [17]:

$$C_{P,E} = \frac{n^2 \int_0^{\frac{V}{n}} v C_{P,hb}(v) dv}{V^2} \quad (5.16)$$

$$C_{P,Q} = \frac{n \int_0^{\frac{V}{n}} C_{P,hb}(v) dv}{2V}. \quad (5.17)$$

The analysis in Section 5.3.2.2 considers only one half of the secondary side ZVS transition. More precisely, the secondary side ZVS analysis is divided in two segments. In the first segment ($0 \leq t < T_1$), the energy equivalent secondary-side full-bridge switching-node capacitance $C_{S,I}$ is obtained by integration up to V'

$$C_{S,I} = \frac{\int_0^{V'} v (C_{S,hb}(v) + 2C_{L_s}) dv}{V'^2}, \quad (5.18)$$

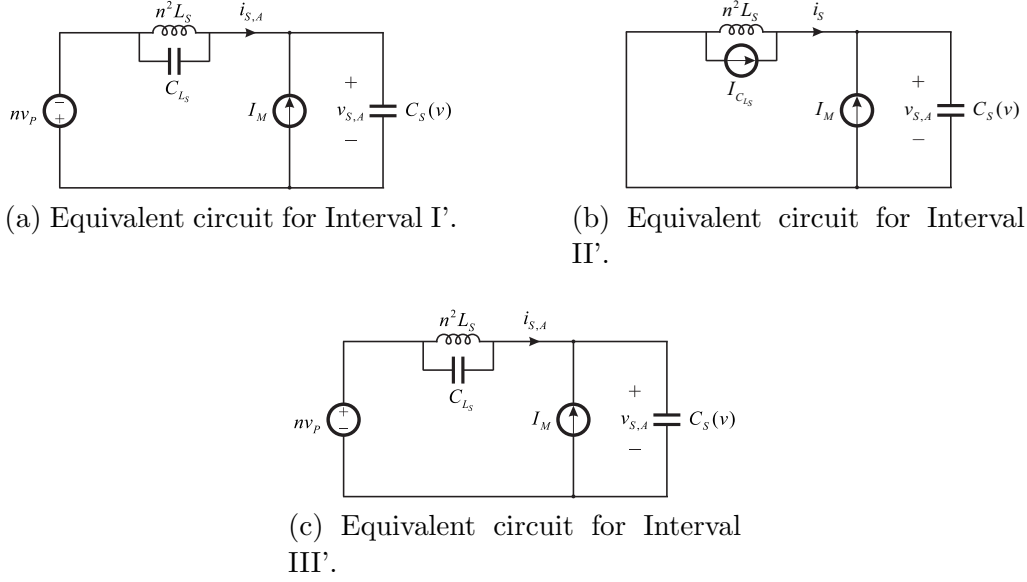


Figure 5.17: Approximate equivalent circuits during ZVS transition.

where V' is equal to one half of the dc link voltage reduced by the half of the $v_{S,A}$ increase during the second segment ($T_1 \leq t < T_1'$). A more detailed derivation of V' is addressed in Section 5.3.2.2.

During the second segment, $v_{S,A}$ is approaching one half of the dc link voltage, resulting in a relatively flat nonlinear capacitance, as illustrated in Fig. 5.16. Therefore, the secondary-side full-bridge switching-node capacitance $C_{S,II}$ during the second segment can be obtained simply as

$$C_{S,II} = C_{S,hb}(0.5V) + 2C_{L_S} . \quad (5.19)$$

5.3.2.2 Magnetizing inductance and secondary-side dead time

The switching sequence, described in Section 5.3.1, involves equivalent circuits shown in Fig. 5.17. An exact solution is complicated for two reasons: nonlinear nature of the switching-node capacitances, and multi-resonant responses, especially in Interval II. An approximate, design-oriented analytical approach is developed in this section to arrive at relatively simple, yet accurate design guidelines for the selection of the magnetizing inductance L_M and the secondary-side dead-time t_{ds} . The following approximations are applied in order to simplify the equivalent circuits in

Fig. 5.15 and arrive at the approximate equivalent circuits in Fig. 5.17:

- Since the primary side switching node voltage exhibits an approximately linear rise, the C_{LS} branch current is approximated with a constant current source $I_{C_{LS}}$ in Interval II (between T'_1 and T'_2), as shown in Fig. 5.18.
- The primary-side switching-node voltage v_P is approximated by a stair-step waveform during Interval II, as shown in Fig. 5.18. The approximation is justified by the fact that Interval II is relatively short compared to the overall ZVS transition time, and details of $nv_P(t)$ transitioning from 0 to V have little impact on the secondary-side ZVS transition waveforms. Furthermore, the approximate stair-step waveform is symmetric around the mid-point of the transition, which also simplifies the analysis.
- The magnetizing inductance current is considered constant and equal to I_M during the ZVS transition. This is justified by the fact that the magnetizing inductance is much larger than the series inductance, so that variations in i_M are relatively small during the ZVS transition.

The approximate equivalent circuits of the ZVS switching sequence are shown in Fig. 5.17. Definitions of the time instants and time intervals corresponding to the approximate switching sequence are given in Tables 5.4 and 5.5. The approximations greatly reduce complexity of the analysis, simplifying the switching sequence states to second-order circuits well suited for state-plane analysis. Since the switching sequence and the waveforms are symmetrical around $T_3/2$, as shown in Fig. 5.14, it is sufficient to perform the analysis over one half of the ZVS transition, from 0 to $T_3/2$.

The secondary side half-transition can be divided into two intervals:

- Interval I' (approximate equivalent circuit is shown in Fig. 5.17a); in order to achieve ZVS with a minimum magnetizing current, i_{tot} should drop to zero at T'_1 , as discussed in Section 5.3.1. Equivalently, $i_{S,A}$ should drop to $-I_M$. At this point, $v_{S,A}$ reaches $-\Delta V_{S,A}$.

- First half of interval II' (approximate equivalent circuit shown in Fig. 5.17b); with the help of $I_{C_{LS}}$, the secondary-side voltage rises by $\Delta V_{S,A}$, and reaches zero in the middle of Interval II'.

For state-plane analysis of the circuit in Figs. 5.17a and 5.17b, the normalized voltage and current can be written as

$$m_{S,A} = \frac{v_{S,A}}{V_{base}}$$

$$j_{S,A} = \begin{cases} \frac{i_{S,A}}{I_{base,I}} & \text{for Interval I,} \\ \frac{i_{S,A}}{I_{base,II}} & \text{for Interval II} \end{cases} \quad (5.20)$$

where

$$V_{base} = V, \quad I_{base,I} = \frac{V_{base}}{R_{0,I}}, \quad I_{base,II} = \frac{V_{base}}{R_{0,II}} \quad (5.21)$$

and

$$R_{0,I} = n\sqrt{\frac{L_S}{C_{S,I}}}, \quad R_{0,II} = n\sqrt{\frac{L_S}{C_{S,II}}}. \quad (5.22)$$

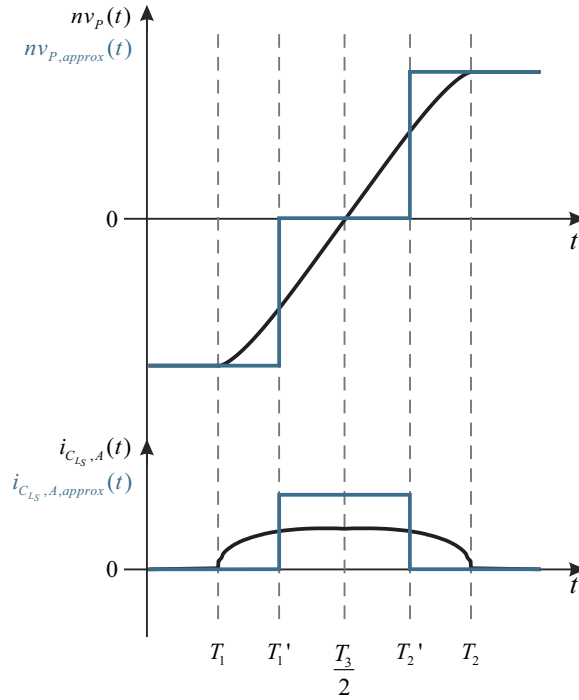


Figure 5.18: Exact and approximate waveforms of the primary-side switching-node voltage $nv_p(t)$ during Interval II.

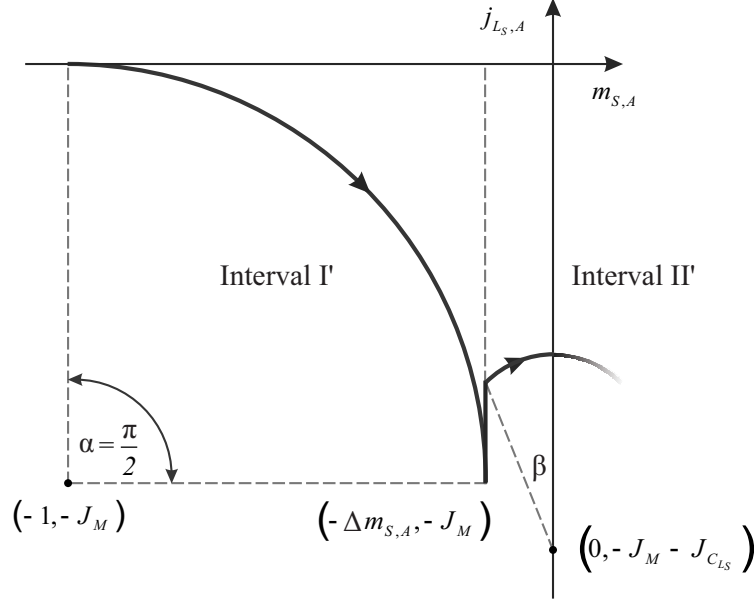


Figure 5.19: State plane trajectory during intervals I' and II'.

The resulting state-plane trajectory is shown in Fig. 5.19. A discontinuity can be observed in $j_{S,A}$ because the two intervals have two different base currents. On the other hand, since R_0 does not affect the voltage normalization, m_S remains continuous.

Since the analysis of Interval I' requires the knowledge of $\Delta V_{S,A}$, Interval II' is considered first.

Interval II'

Given the approximation that the primary side switching-node voltage v_P is increasing linearly, and that the secondary side switching-node voltage $v_{S,A}$ does not change much compared to v_P , current $I_{C_{LS}}$ can be found approximately as:

$$I_{C_{LS}} = \frac{2VC_{LS}}{n^2 t_{dp}}, \quad (5.23)$$

which in normalized form becomes:

$$J_{C_{LS}} = \frac{nI_{C_{LS}}}{V} \sqrt{\frac{L_S}{C_{S,II}}}. \quad (5.24)$$

Angle β is

$$\beta = \frac{t_{dp}}{4n\sqrt{L_S C_{S,II}}}, \quad (5.25)$$

and $\Delta m_{S,A}$ is found as

$$\Delta m_{S,A} = J_{C_{L_S}} \tan(\beta), \quad (5.26)$$

which yields

$$\Delta V_{S,A} = n I_{C_{L_S}} \sqrt{\frac{L_S}{C_{S,II}}} \tan\left(\frac{t_{dp}}{4n\sqrt{L_S C_{S,II}}}\right). \quad (5.27)$$

It is convenient to define V' as

$$V' = \frac{1}{2}(V - \Delta V_{S,A}). \quad (5.28)$$

This V' has been used as the integration limit in (5.18) to determine $C_{S,I}$.

Interval I'

In order for the normalized voltage to reach $-\Delta m_{S,A}$ while the normalized current drops to $-J_M$, the following condition must be met

$$J_M = 1 - \Delta m_{S,A}. \quad (5.29)$$

The required amplitude of the magnetizing current can be found from (5.27) and (5.29):

$$I_M = \left(1 - \frac{\Delta V_{S,A}}{V}\right) \frac{V}{n} \sqrt{\frac{C_{S,I}}{L_S}} \quad (5.30)$$

and the required magnetizing inductance is

$$L_M = \frac{V}{4I_M} \left(\frac{1}{f_{sw}} - t_{ds} - t_{dp} \right) \quad (5.31)$$

where t_{dp} can be found from (5.5). It remains to determine the secondary-side dead time t_{ds} .

Since the energy stored in the magnetizing inductance is just enough to discharge the switching node capacitance, the charge equivalent linear capacitance cannot be used to determine the secondary-side dead time. The rise time of the secondary side switching node can be estimated more accurately by solving the circuit in Fig. 5.17(a),

$$t_{ds} = \frac{t_{dp}}{2} + 2 \int_0^{V'} \frac{C_s(v_x) dv}{\sqrt{I_M^2 - \frac{4}{n^2 L_s} \int_0^v C_s(v_x) v_x dv_x}}, \quad (5.32)$$

where

$$C_s(v_x) = C_{S,hb}(v_x) + 2C_{L_S}. \quad (5.33)$$

This result can be used to properly set the dead time in a practical implementation. With the goal of arriving at a simpler, closed-form solution for the required magnetizing inductance, it should be noted that the impact of t_{ds} in (5.31) is relatively small. An approximate expression for t_{ds} can therefore be found from the state-plane analysis illustrated in Fig. 5.19 by noting that T'_1 interval corresponds to angle $\alpha = \pi/2$,

$$\alpha = \frac{T'_1}{n\sqrt{L_S C_{S,I}}} = \frac{\pi}{2}, \quad (5.34)$$

using the energy-equivalent secondary-side capacitance $C_{S,I}$ evaluated over one half of the dc link voltage. Given that $T'_1 = 0.5(t_{ds} - 0.5t_{dp})$, (5.34) yields an approximate expression for the secondary-side dead time

$$t_{ds,approx} = \frac{t_{dp}}{2} + \pi n \sqrt{L_S C_{S,I}} \quad (5.35)$$

where L_S and t_{dp} can be found from (5.2) and (5.5), respectively.

Finally, an approximate closed-form expression for the required magnetizing inductance L_M follows from (5.31)

$$L_M \approx \frac{V}{4I_M} \left(\frac{1}{f_{sw}} - t_{ds,approx} - t_{dp} \right) \quad (5.36)$$

where, in terms of the circuit specifications and parameter values, t_{dp} can be found from (5.5), I_M from (5.30), and $t_{ds,approx}$ from (5.35).

5.3.3 Sensitivity to parameter variations

The analysis and the design guidelines presented in this section depend on the circuit parameter values, specifically the switching node capacitance and the series inductance. A sensitivity analysis with respect to ΔL is performed for the converter prototype specifications given in Section 5.5. Fig. 5.20 shows how a percent variation ΔL in the series inductance affects relative changes

Table 5.10: Experimental prototype parameters

P	V	n	f_{sw}
10 kW	1 kV	1	200 kHz

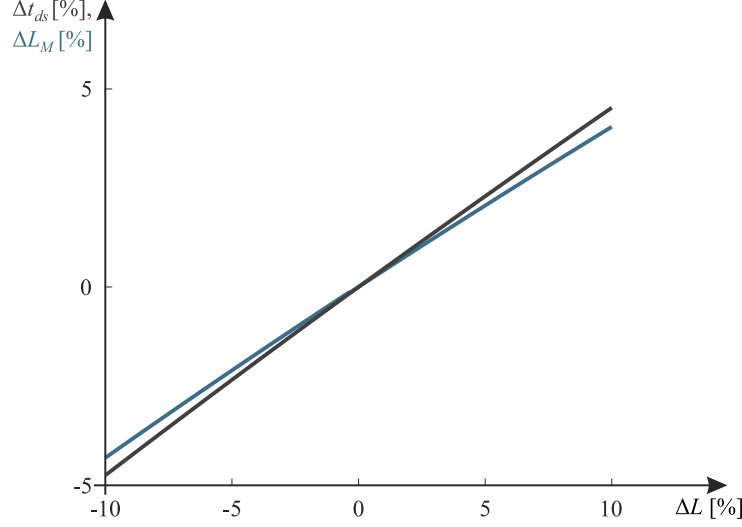


Figure 5.20: Effects of the variation in the series inductance on the changes Δt_{sd} and ΔL_M in the design parameters.

in the resulting design parameters Δt_{sd} and ΔL_M . With respect to both design parameters, a relatively low sensitivity of approximately 0.5 is observed. Furthermore, given the approximation (5.5) used to determine the primary-side deadtime, this design parameter is not affected significantly by the variation in series inductance.

5.4 Design optimization

For a given series inductance L_S , and the corresponding maximum phase shift φ_m , the design approach described in Section 5.3.2 minimizes the magnetizing current required to achieve ZVS at all times. In this section, major loss mechanisms, including semiconductor conduction losses, as well as core and conduction losses in the magnetics, are analyzed as functions of the maximum phase shift, and the optimum values of φ_m and L_S are found to minimize the losses. The case study is a 10kW, 1kV QAB stage, with the specifications summarized in Table 5.10. The MOSFETs are

Table 5.11: Capacitances in the experimental prototype

C_{tr}	C_{L_s}	C_{PCB}	$C_{P,Q}$	$C_{S,I}$	$C_{S,II}$
265 pF	55 pF	35 pF	497 pF	606 pF	526 pF

1700 V SiC (Wolfspeed Cree C2M0045170P). Values of the parasitic capacitances that are important for the minimum peak magnetizing current calculation are shown in Table 5.11. The optimization is carried out at 75% of the full load, since this load has the highest weight in the CEC efficiency calculation [9].

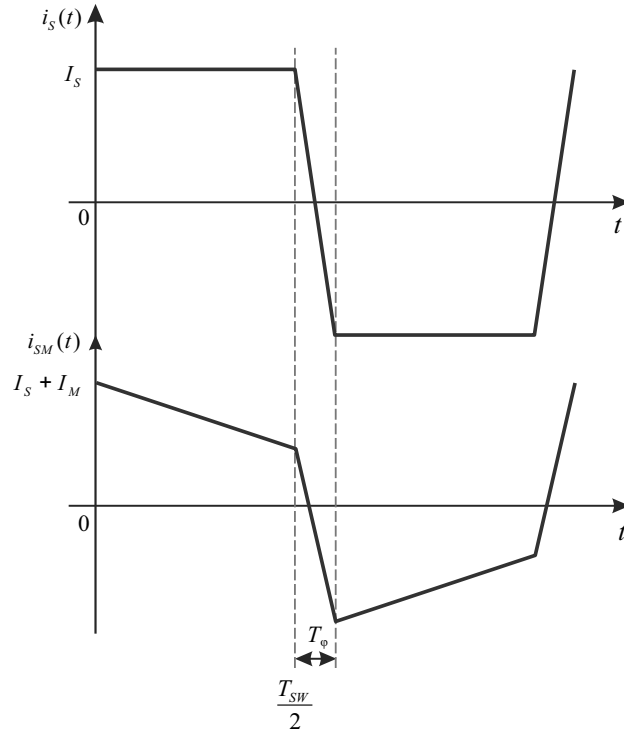


Figure 5.21: Theoretical currents waveforms during a switching period.

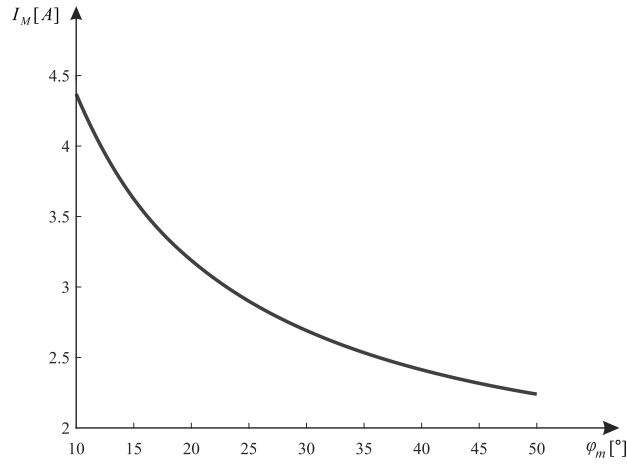


Figure 5.22: Peak magnetizing current dependence on φ_m .

5.4.1 Active-bridge conduction losses

Since the input average current is constant, the primary side RMS current $I_{PR,RMS}$ can be calculated simply by integrating the trapezoidal current waveform with the peak value given by (5.3):

$$I_{PR,RMS} = \left(\frac{P}{V}\right) \frac{\sqrt{\left(1 - \frac{2\varphi_m}{3\pi}\right)}}{\left(1 - \frac{\varphi_m}{\pi}\right)}. \quad (5.37)$$

Secondary-side current waveshapes $i_S(t)$ and $i_{SM}(t) = i_S(t) + i_M(t)$ are shown in Fig. 5.21. It is important to note that the phase shift φ and the amplitude I_S vary over a half line period,

$$I_S(t) = \frac{2P}{3V \left(1 - \frac{\varphi(t)}{\pi}\right)} \quad (5.38)$$

while the peak I_M of the magnetizing current can be found from (5.30). Secondary RMS current $I_{SEC,RMS}$ can be found by first calculating the secondary RMS current over a switching period $i_{SM,RMS}(t)$ based on the waveforms shown in Fig. 5.21 and the expressions for I_S and I_M , and then by integration over the line cycle. The peak of the magnetizing current and the primary and the secondary RMS currents are shown in Fig. 5.22 and Fig. 5.23 as functions of φ_m . It can be noted that I_M decreases as φ_m increases. This is because a higher φ_m implies a large L_S , and a smaller magnetizing current is therefore required to achieve the ZVS sequence described in

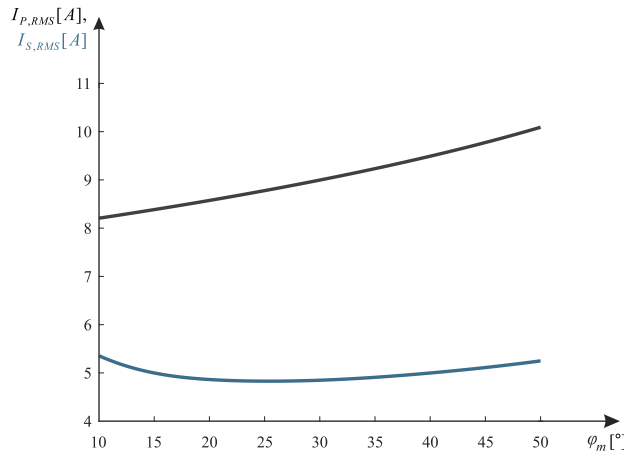


Figure 5.23: RMS primary and secondary currents as functions of φ_m .

Section 5.3.1. Following the trend in DAB converters [18], the primary-side RMS current increases as φ_m increases because of the larger reactive component of the series current. The secondary-side RMS current has both magnetizing and series current components, which is why $I_{SEC,RMS}$ is a convex function of φ_m .

The primary-side active-bridge conduction loss is given by:

$$P_{cond,PR} = 2R_{on,PR} \left(\frac{P}{V} \right)^2 \frac{\left(1 - \frac{2\varphi_m}{3\pi} \right)}{\left(1 - \frac{\varphi_m}{\pi} \right)^2} \quad (5.39)$$

and the secondary-side active-bridge conduction loss can be found by integration over a line cycle:

$$P_{cond,SEC} = 6R_{on,SEC} I_{SEC,RMS}^2 \quad (5.40)$$

5.4.2 Loss in the magnetic components

The high-frequency transformer is a critical component, since the converter module is intended for the system architecture in Fig. 5.1, where the transformer needs to withstand medium voltage (MV) between primary and secondary windings. Planar technology is chosen for magnetics implementation because of the ease of manufacturability and repeatability [69, 68, 84].

The transformer design is based on two side-by-side EILP 102 cores, with 20 turns per winding on 4 PCB layers using 5 Oz copper. The primary and secondary layers are interleaved. The required MV isolation is achieved using polyimide dielectric (instead of standard FR4) between the PCB layers and by keeping sufficient spacing between the copper traces, the vias and the core, as described in more detail in [64]. The MV isolation requirement results in significantly longer and narrower traces in the transformer, which leads to higher dc resistance, and thereby increased winding losses.

Increasing the magnetizing current is achieved by insertion of an air-gap in the transformer core, which does not affect the core loss but affects the transformer winding loss significantly. To minimize proximity effects, the primary and secondary winding layers are interleaved. However, as illustrated by FEA simulation results in Fig. 5.25, with the air-gap, the H -field distribution has

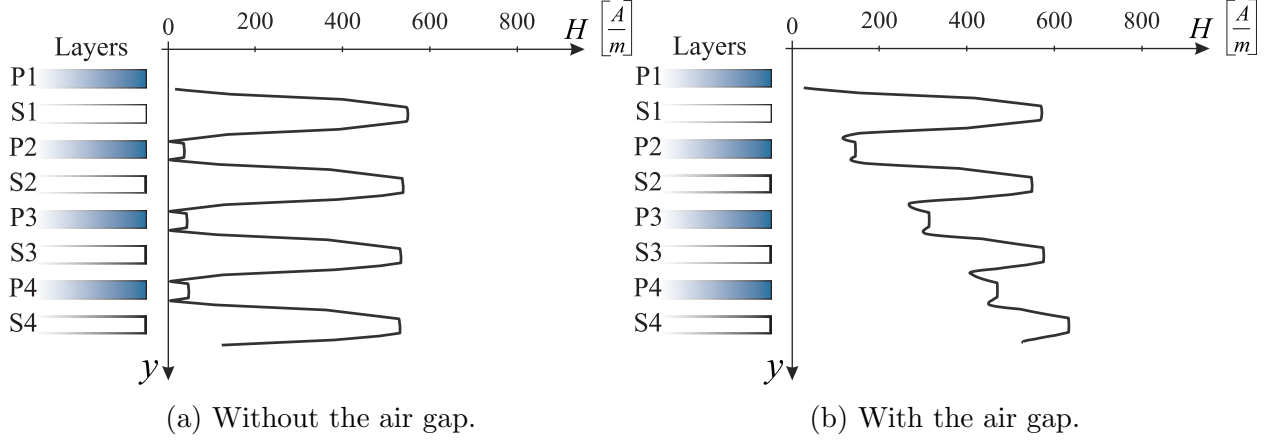


Figure 5.24: H field magnitude in the planar high frequency transformer along y axis at one instant during a line cycle.

significantly larger intensity around the top layers of the transformer windings. Fig. 5.24 shows 2D plots of the $|H(y)|$ dependence, without and with the air-gap. With the air-gap (Fig. 5.24b), the H -field increases progressively through the layers. This is because the currents through the primary and the secondary side of the transformer are not perfectly balanced (see Fig. 5.21), which results in increased proximity losses compared to the case of perfect interleaving between the primary and the secondary layers illustrated in Fig. 5.24a.

Since standard analytical methods [26] do not apply to gapped transformers where the magnetizing current is significant, a more general method is used to accurately predict the loss in the windings. As discussed in [80], for arbitrary relationships between the magnitude and phase of the primary and secondary currents, the transformer winding loss can be found using a resistance matrix:

$$\begin{aligned}
 P_{cu,tfo} = & \frac{1}{2} \sum_{\omega} R_{11}(\omega) I_1(j\omega) I_1^*(j\omega) \\
 & + R_{12}(\omega) (I_1(j\omega) I_2^*(j\omega) + I_2(j\omega) I_1^*(j\omega)) \\
 & + R_{22}(\omega) I_2(j\omega) I_2^*(j\omega),
 \end{aligned} \tag{5.41}$$

where $I_1 = I_{S,A}$ and $I_2 = I_{S,A} + I_{M,A}$ are phasors of the currents through primary and

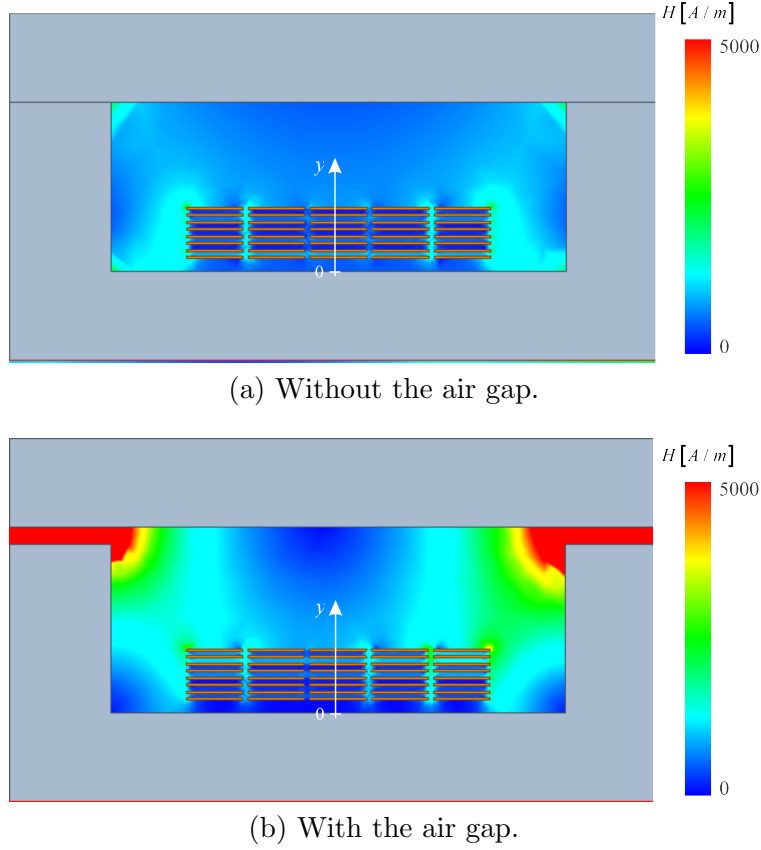


Figure 5.25: 2D FEA simulation showing H field distribution in the planar high frequency transformer at a point of the line cycle.

secondary windings of the transformer, respectively. Since the currents shown in Fig. 5.21 have high harmonic content, the losses are calculated up to the 10^{th} harmonic. For example, at 200 kHz, the resistance matrix of the transformer obtained using 3D finite-element analysis (Ansys Maxwell) simulations is:

$$\begin{bmatrix} R_{11} & R_{12} \\ R_{12} & R_{22} \end{bmatrix} = \begin{bmatrix} 2.6 \, \Omega & -2.1 \, \Omega \\ -2.1 \, \Omega & 2.6 \, \Omega \end{bmatrix}. \quad (5.42)$$

The 3D model of the MV high-frequency transformer built in Ansys Maxwell is shown in Fig. 5.26. The series inductors are using ELP 64 core, with 10 turns of 2 Oz copper in 5 layers. The AC resistance of the inductor at 200 kHz is:

$$R_{ind} = 392 \, \text{m}\Omega. \quad (5.43)$$

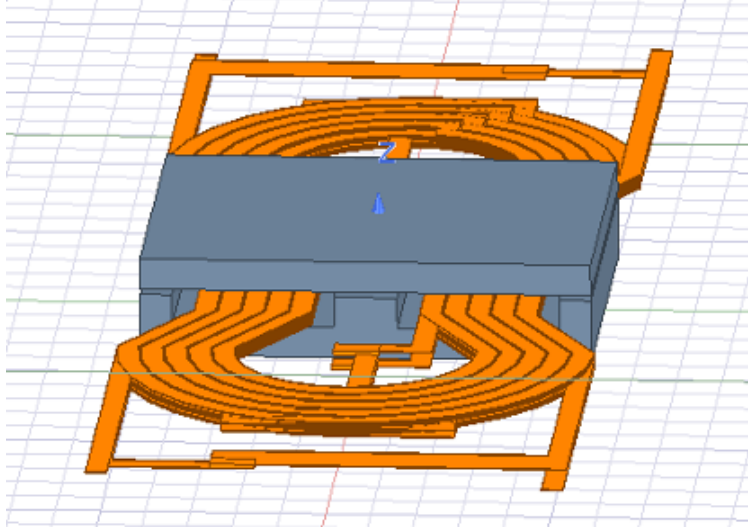


Figure 5.26: 3D model of the MV high frequency transformer used for finite-element analysis in Ansys Maxwell.

In contrast to the transformer winding losses, losses in the series inductors are not affected by the magnetizing current. However, the maximum phase shift affects both the core and the conduction loss in the inductors. A larger maximum phase shift implies more volt-seconds applied and a larger RMS current, therefore increasing both core and conduction loss, as shown in Fig. 5.27b.

5.4.3 Total modeled loss

Contributions to the loss of each component separately, and the total modeled loss are shown in Fig. 5.27 and Fig. 5.28, respectively, as functions of the maximum phase shift φ_m as the design parameter. The modeled losses are expressed as percentages of 7.5 kW, which is the power level considered for design optimization.

For small values of φ_m , the required peak of the magnetizing current increases, thus increasing the loss in the secondary-side bridge and the transformer windings. For large values of φ_m , the reactive component in the series current increases, resulting in increased conduction losses. In choosing the optimal value of φ_m , it is further important to take into account the primary-side ZVS condition given by (5.4). Fig. 5.28 shows how this constraint restricts the range of considered maximum phase shift above a lower limit for φ_m . The maximum phase shift that minimizes the

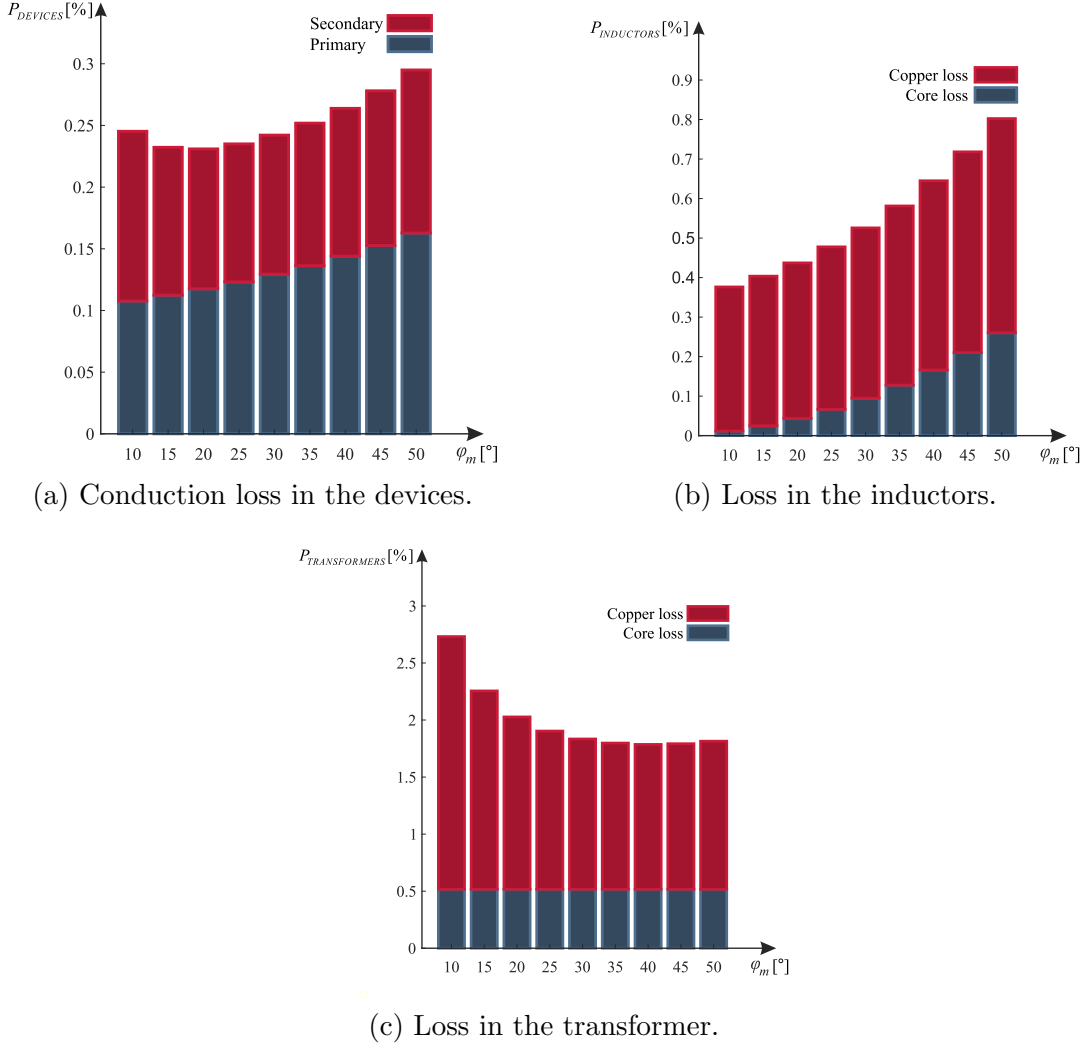


Figure 5.27: Component losses as functions of the maximum phase shift φ_m .

total loss in the converter is $\varphi_m = 30^\circ$.

5.5 Experimental results

The experimental prototype of the dc-to-3-phase ac module is shown in Fig. 5.29. The prototype specifications are summarized in Table 5.10, and the component parameters are provided in Table 5.12. The prototype consists of one primary board, three secondary boards, and the planar magnetics. The primary and each of the secondary boards have a dedicated microcontroller. Each secondary board includes a secondary-side bridge of the QAB, and an H-bridge inverter, as shown

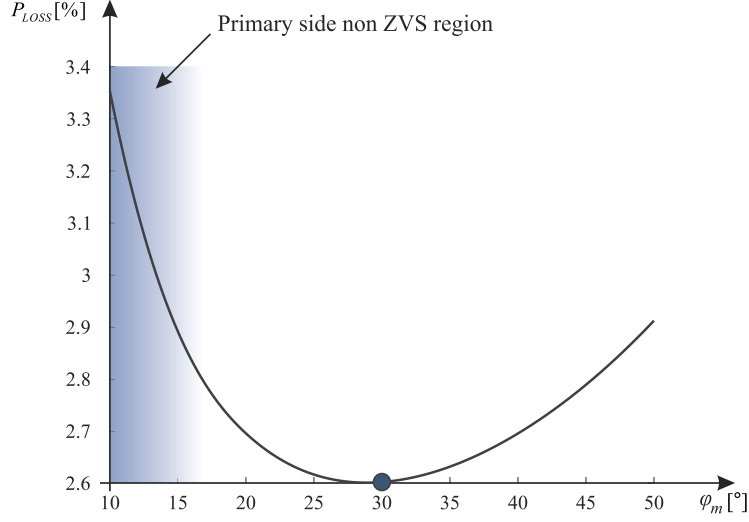


Figure 5.28: Total loss as a function of φ_m .

in Fig. 5.2.

All the communication between the primary and the secondary boards is done through optical cables. The signaling includes: (i) synchronization pulses at $f_s = 200\text{ kHz}$ from the primary to each of the secondary boards to facilitate the phase-shift control of the QAB, and (ii) 60 Hz synchronization pulses used for setting the power reference at the secondaries, which is realized using the Controller Area Network (CAN) protocol.

To validate dc bus voltage regulation and voltage ripple, Fig. 5.30 shows a transient response to a 50-100% load step at the inverter output. The PIR controller, designed as discussed in [74], is capable of firmly regulating the output voltage against load transients. Also, as expected, a twice line frequency ripple is visible in the dc-link voltage due to the large output current disturbance at this frequency. However, the dc-link voltage is maintained within relatively narrow limits. At full load the ripple amplitude is 4% of the dc voltage, while at light load it's less than 1%. This validates the assumption that the dc bus voltage can be considered constant in the analysis.

Table 5.12: Components used in the hardware prototype

Component	Part number	Details
MOSFET	C2M0045170P	SiC, 1.7 kV, $R_{dson} = 45\text{ m}\Omega$
Inductor	EILP 64	$n_{turns} = 10$, $n_{layers} = 5$, $t_{cu} = 2\text{ Oz}$, $l_{gap} = 2.28\text{ mm}$
Transformer	2 x EILP 102	$n_{turns} = 20$, $n_{layers} = 4$, $t_{cu} = 5\text{ Oz}$, $l_{gap} = 1.4\text{ mm}$ $t_{prepreg} = 5\text{ mil (polyimide)}$ $V_{Hipot} = 26\text{ kV}$
DC-link cap	8 x C4AQSBW4800A3JJ	$8\mu\text{F}$ each

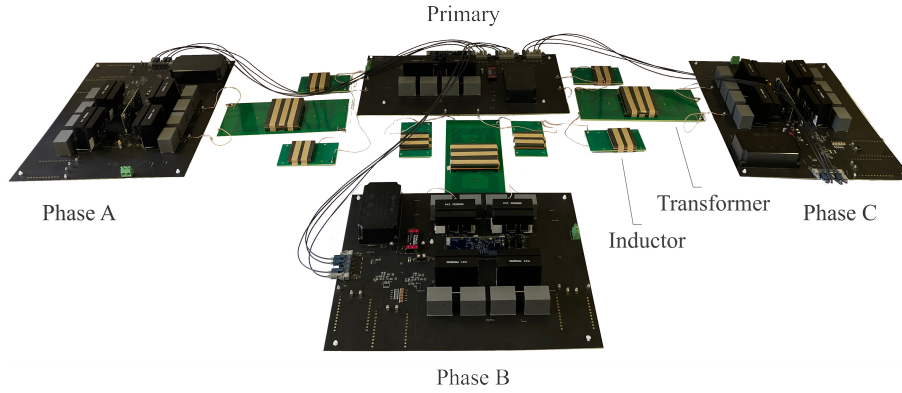


Figure 5.29: 1 kV, 10 kW SiC-based prototype of the isolated DC to three-phase AC module.

5.5.1 Design validation

The primary-side dead time is calculated from (5.5), while the secondary-side dead time and the magnetizing inductance are calculated according to (5.32) and (5.36), respectively, and the results are summarized in Table 5.13. By inserting the air-gap in the transformer, the value of the magnetizing inductance is reduced from 6 mH to $385\mu\text{H}$. The air-gaps inserted in the transformers and the inductors are 1.4 mm and 2.28 mm, respectively. The peak flux density in the transformer core is 60 mT, which is independent of the instantaneous power level, while the peak flux density in the inductor core varies with the instantaneous power in the range from 0 to 45 mT.

The series inductance is split in two, to provide symmetric impedance in the common-mode path and thus reduce common-mode current circulation through the transformer [65, 37].

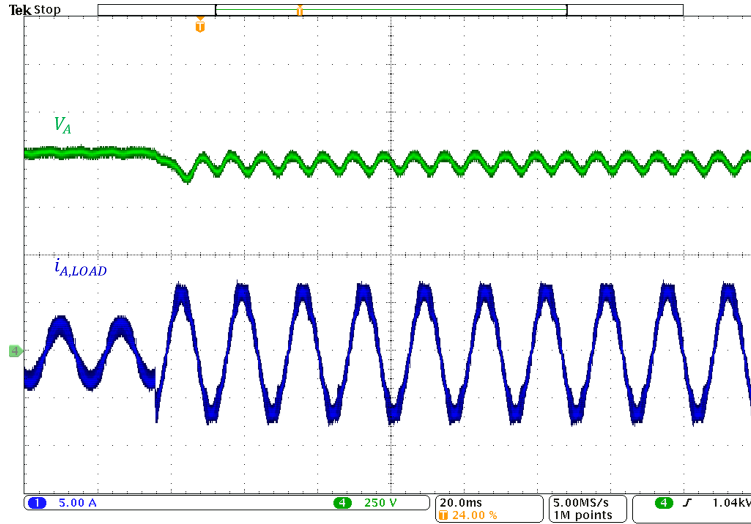
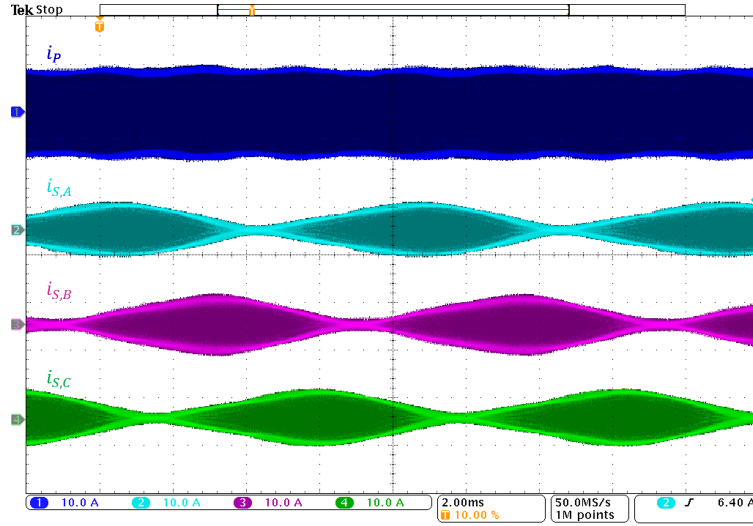


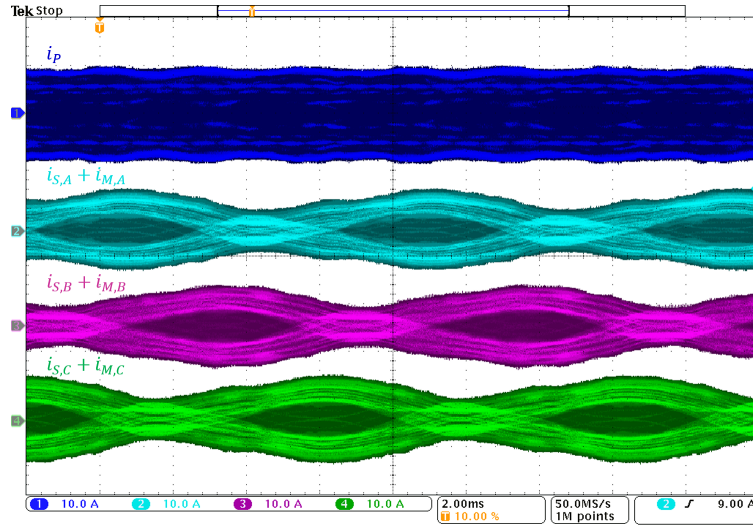
Figure 5.30: Phase A dc-link voltage V_A and the inverter output current $i_{A,LOAD}$, during a step change from 50% to 100% of load.

Fig. 5.31 shows how the three-phase secondary QAB currents are summing up to a constant-envelope current on the primary side. The waveforms are shown for the currents $i_{S,A}$, $i_{S,B}$ and $i_{S,C}$ in Fig. 5.31(a), and the currents including the magnetizing currents in Fig. 5.31(b), which illustrate how the additional circulating currents are relatively small. Fig. 5.32(a) shows ZVS operation at the zero power crossing of phase A, while Fig. 5.32(b) confirms that the measured waveforms closely match the theoretical waveforms shown in Fig. 5.14. It should be noted that the planar implementation of the magnetic components have pronounced parasitics, which result in increased high-frequency parasitic oscillations. For example, Fig. 5.32b shows that there are high-frequency components in $i_{S,A}$ and in $i_{S,A} + i_{M,A}$ due to resonance between the parasitic capacitance of the series inductors and the leakage inductance of the transformer. Aside from high-frequency effects, however, the waveforms in fact demonstrate very good match with the model.

In order to verify the approximations introduced in Section 5.3.2.2, two model-based simulations are performed, and compared with the experimental results. An accurate model is developed based on the equivalent circuits shown in Fig. 5.15. A simpler model, which is used to derive design equations in Section 5.3.2, is based on the equivalent circuits shown in Fig. 5.17. Fig. 5.33 shows a good agreement between the state-plane trajectories obtained from the accurate model, from the



(a) Primary current i_P , and secondary currents through L_S .

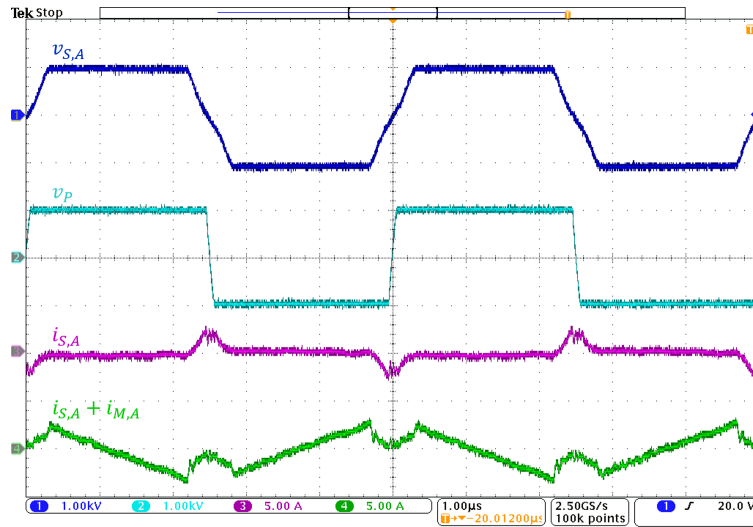


(b) Primary current i_P , and secondary currents through L_S and L_M .

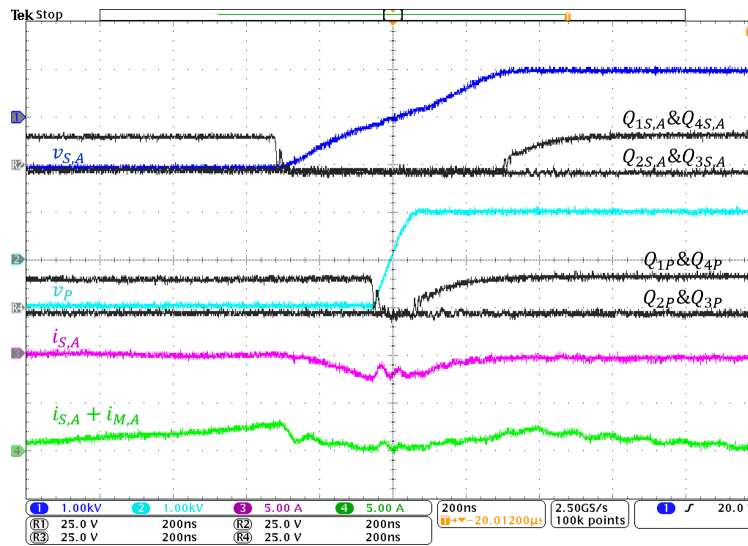
Figure 5.31: Quadruple active bridge primary and secondary currents.

approximate model, and from the experimental waveforms.

The optimization carried out in Section 5.4 is validated experimentally by testing different designs around the optimum φ_m point. Each of the measured data points corresponds to different transformer and inductor air-gaps adjusted around the values obtained by the model-based optimization. As Fig. 5.34 shows, the experimentally measured optimal φ_m matches the model-



(a) Switching-node voltages $v_{S,A}$, v_P , and currents $i_{S,A}$ and $i_{S,A} + i_{M,A}$.



(b) Waveforms during ZVS transition.

Figure 5.32: Waveforms illustrating zero voltage switching at the zero power instant for phase A.

predicted value. Additionally, the measured points around the minimum follow the trend of the model-predicted curve.

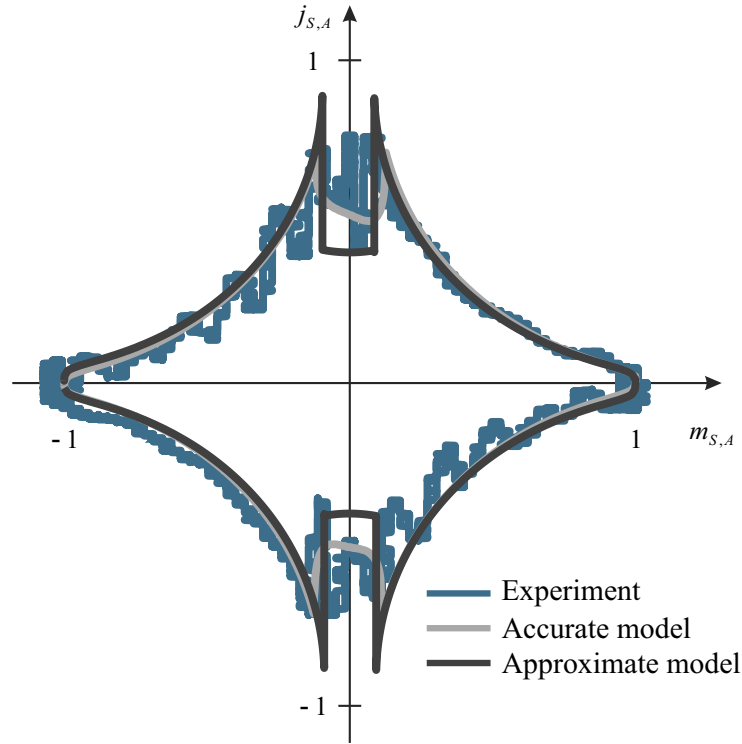


Figure 5.33: State plane trajectory at the time Phase A power is zero. Experimental results are overlapped with solutions based on accurate and approximate models.

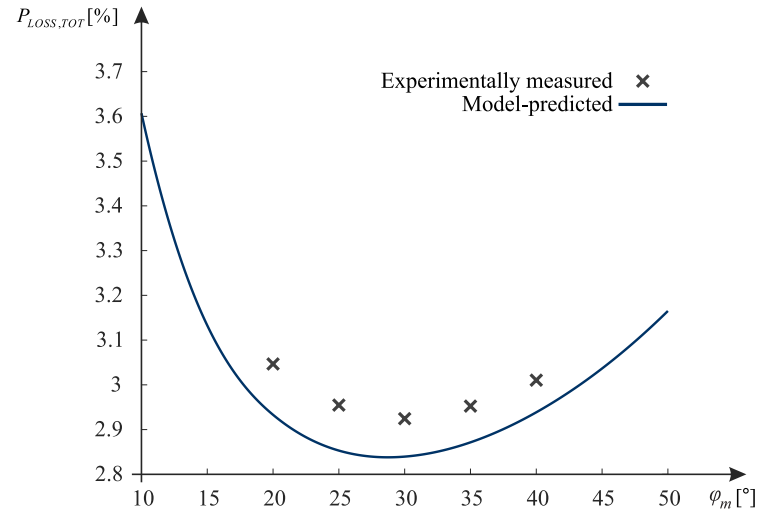


Figure 5.34: Experimentally measured loss for designs around the optimum φ_m together with the model-predicted optimization curve.

Table 5.13: Dead times, magnetizing inductance, and maximum phase shift in the experimental prototype

t_{dp}	t_{ds}	L_M	φ_m
110 ns	740 ns	385 μ H	30°

5.5.2 Efficiency comparison against a conventional design using a large magnetizing inductance

When the same prototype is operated with a transformer without the air-gaps, while keeping all other parameters the same, switching losses on the secondary-side devices are excessively large, which results in much reduced efficiency. Due to thermal limitations, it is not possible to operate the prototype without the transformer air-gaps at full voltage and power. To illustrate the advantage of the proposed design methodology over the conventional design with ungapped transformers, the model-based efficiency curves are compared in Fig. 5.35. One may note that the additional loss incurred due to the circulating currents in the gapped-transformer design is much smaller than the secondary-side switching loss in the conventional ungapped-transformer design. As expected, the benefit of the proposed design is particularly visible at lower average power levels, where the energy

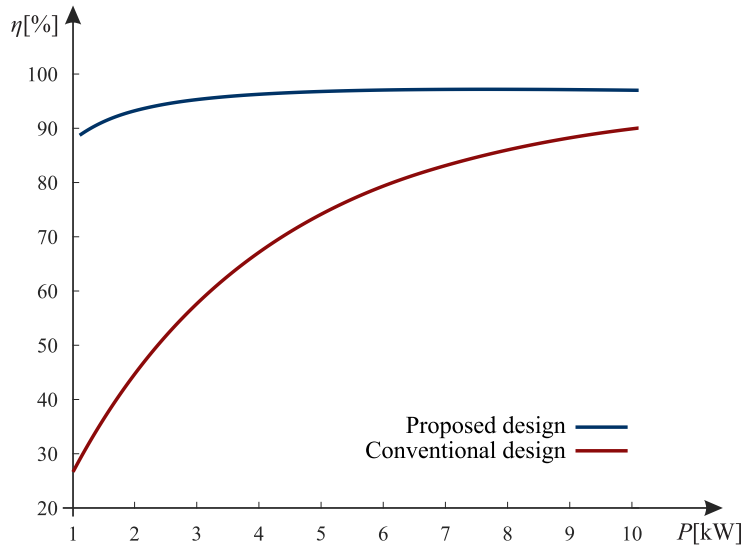


Figure 5.35: Model-predicted efficiency curves for the design with the optimized maximum phase shift, magnetizing inductance, and dead times, and for the conventional design with ungapped transformers.

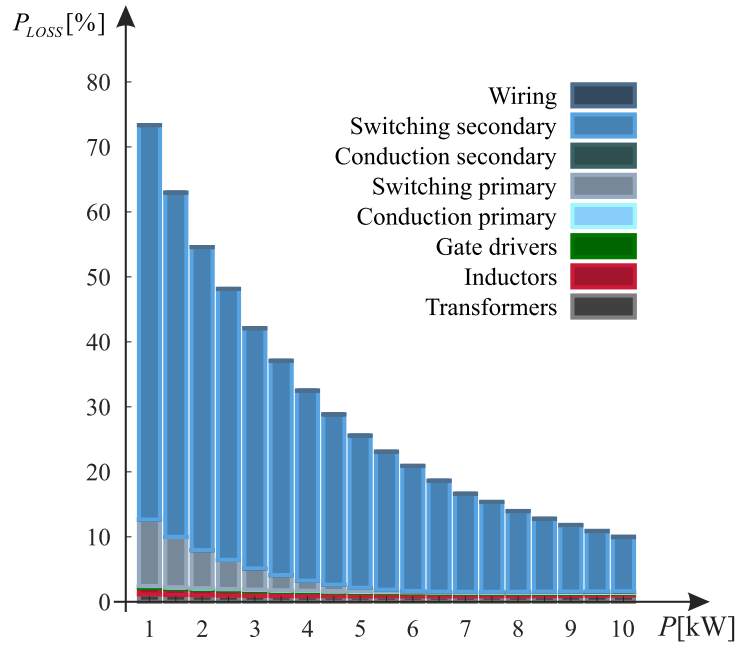


Figure 5.36: Model-predicted loss breakdown of the QAB prototype using conventional design with ungapped transformers.

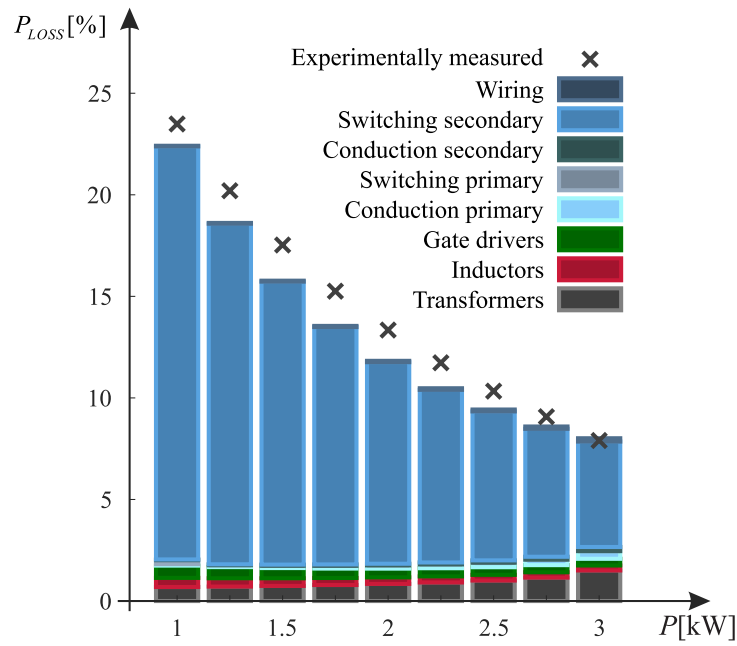


Figure 5.37: Loss of the experimental QAB prototype operating at 500 V dc link voltages using conventional design with ungapped transformers, together with a model-predicted loss breakdown.

provided by the series inductance, in the conventional design, becomes insufficient to achieve ZVS

over a larger portion of the line cycle. However, even at high load there is an efficiency improvement because the benefits of soft switching over the entire line cycle outweigh the conduction-loss penalty introduced by the extra magnetizing current.

Fig. 5.36 shows that, in the conventional design, the majority of the loss comes from hard switching of the SiC devices, especially at lighter loads. The switching loss of the secondary-side devices is excessively high because the switching-node capacitance includes the significant interwinding capacitance of the transformer with MV isolation, in addition to the device and PCB capacitances. Furthermore, the dc bus voltage (1 kV) and the switching frequency (200 kHz) are relatively high.

To validate the predicted loss of the conventional design, an experiment is conducted at a reduced voltage of 500 V, over a wide load range. Fig. 5.37 shows the loss breakdown, which demonstrates a good match with the experimentally measured total loss. The results confirm validity of the loss model and the fact that the switching losses dominate in the conventional design with ungapped transformers.

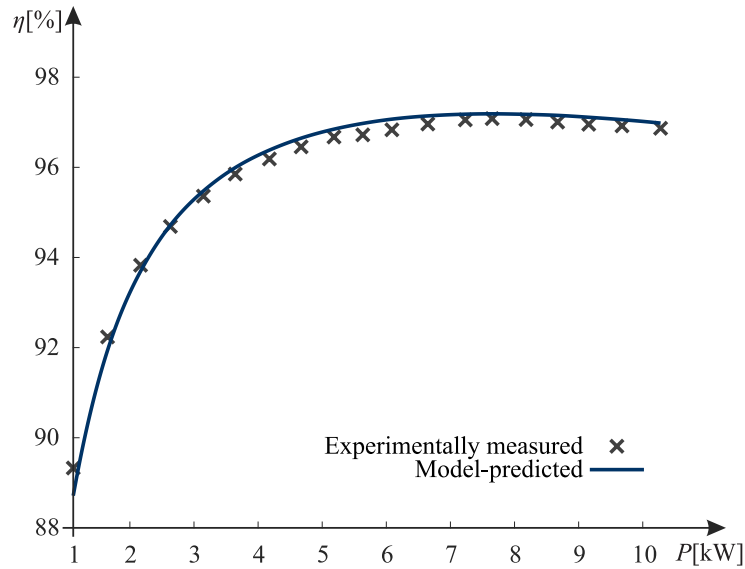


Figure 5.38: Efficiency of the experimental QAB prototype using the optimized maximum phase shift, magnetizing inductance, and dead times, together with a model-predicted efficiency curve.

5.5.3 Efficiency and loss breakdown

Measured efficiency of the prototype converter is shown in Fig. 5.38 as a function of the average output power. The efficiency curve is relatively flat, with a peak efficiency of 97.1% at the output power of 7.5 kW, where the design is optimized. The converter efficiency is measured Yokogawa Precision Power Analyzer WT3000. The power analyzer has built-in analog low-pass filters, which enable highly accurate sampling of the dc and fundamental frequency components [93].

The model-based loss breakdown, together with the measured loss, are shown in Fig. 5.39, over a wide load range. A good match is obtained between the predicted and the measured loss. The largest portion of the loss is taken by the high-frequency transformers, due to the MV isolation requirements and the additional winding loss incurred by the circulating currents, as elaborated in Section 5.4.2.

Fig. 5.40 shows thermal images of the power devices and the transformer in the experimental

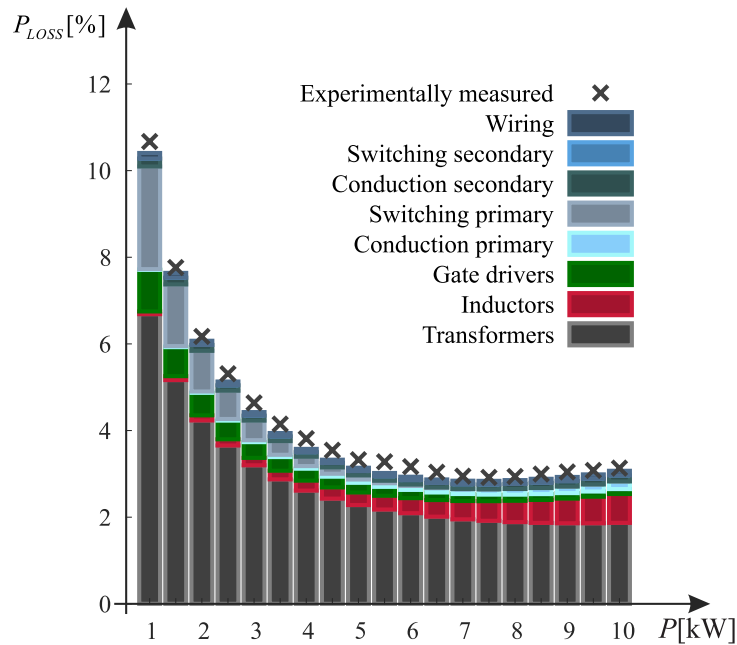
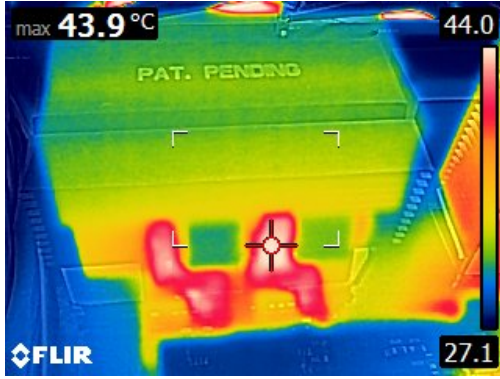
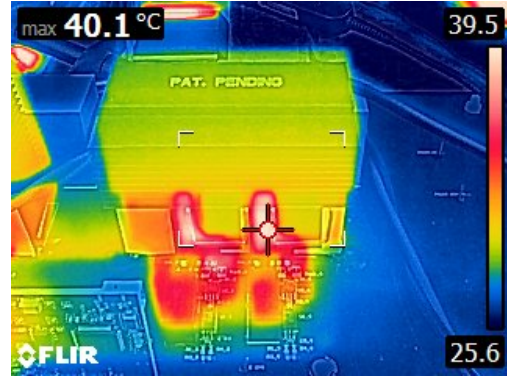


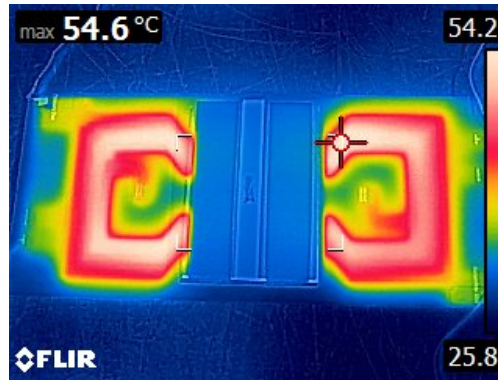
Figure 5.39: Loss of the experimental QAB prototype using the optimized maximum phase shift, magnetizing inductance, and dead times, together with a model-predicted loss breakdown.



(a) Primary-side MOSFETs .



(b) Secondary-side MOSFETs.



(c) Transformer.

Figure 5.40: Thermal images of the devices and one of the transformers in the experimental prototype operating at full power (10 kW) and at room ambient temperature, without any forced-air cooling.

prototype operating at full power and at room ambient temperature, without any forced-air cooling.

5.6 Conclusions

This chapter presents the design of a quadruple active bridge (QAB) converter operating as a fixed-ratio “dc transformer” (DCX) in an isolated DC to three-phase AC module intended for MV modular system architectures. The QAB stage produces three isolated DC link voltages, which serve as inputs for three single-phase dc-to-ac inverter stages. The QAB employs simple phase shift to regulate the DC link voltages. Assuming a balanced three-phase system, the QAB primary-side power is constant, but each secondary side processes time-varying power having a component at

twice the line frequency, which makes it difficult to maintain zero-voltage switching (ZVS) in the secondary-side active bridges during low-power portions of the line cycle. By placing an airgap into the high-frequency transformer cores, the transformer magnetizing current is increased to achieve ZVS throughout the line cycle. A detailed analysis of the switching transient is presented, including effects of the nonlinear device capacitances and series-inductor parasitic capacitances. Suitable approximations are introduced to obtain closed-form, design-oriented expressions for the magnetizing inductance, and the primary-side and secondary-side dead times, so that ZVS can be achieved while minimizing the magnetizing current. Furthermore, loss models are developed to enable the system design optimization using the maximum phase shift as a design parameter. An optimum maximum phase shift, series and magnetizing inductances, and dead-times are found to minimize the total loss in the converter.

The proposed approach and the design optimization strategy show significant loss reduction compared to the conventional design with an ungapped transformer. The approach is particularly well suited for higher-voltage applications, where hard switching losses can be significant. The method would be less beneficial in lower-frequency, lower-voltage or higher-current applications where conduction losses dominate. Experimental results on a SiC-based 1 kV, 10 kW prototype operating at 200 kHz verify the developed models and the optimization approach. The prototype has a relatively flat efficiency curve with the peak efficiency of 97.1% at 7.5 kW.

Chapter 6

Conclusions and Future Work

6.1 Thesis Summary and Conclusions

The miniaturization of power converters has been driven by advances in converter configurations, advances in power semiconductor devices, and an increase in switching frequency. Thermal management and efficiency requirements become the key challenges in the design of high-power-density converters, especially in applications that require a high conversion ratio. “Dc transformers” (DCX) are a class of converters that are known to be highly efficient when operated around a nominal conversion ratio, due to soft switching of semiconductor devices, relatively low conduction losses, and small amounts of energy stored in passive components. This thesis is focused on modularization of DCX converters, which can further improve their performance. The design optimization of modular DCX-based converter architectures is discussed from multiple perspectives: topology, semiconductor devices, modulation strategies, and optimization and integration of magnetic components. The thesis is divided into two major parts.

The first part of the thesis is focused on the design and optimization of GaN-based high step-down stacked active bridge (SAB) converters. Chapter 2 discusses the advantages of splitting the high-voltage side active bridge into multiple modules, by stacking them in series. It is shown that stacking multiple modules in series using lower voltage-rated devices can be beneficial from the conduction loss point of view, considering the fixed total semiconductor area. It is also shown that there is a limit to the benefits of increasing the number of modules stacked in series. Stacking a very large number of modules, and using very low voltage-rated devices, can have detrimental

effects on the loss. Therefore, there is a range of the number of modules with devices that have a correspondingly chosen voltage rating that results in superior performance.

Chapter 3 presents a transformerless high step-down SAB dc-dc converter [59]. The SAB converter is comprised of series-stacked capacitively coupled inverter modules and parallel-connected rectifier modules. The nominal conversion ratio is set by the number of stacked inverter modules, whereas the output current capability scales with the number of paralleled rectifier modules. Effects of timing mismatch and switch node parasitic capacitances on the voltage balancing among the series-stacked modules are analyzed. It is shown that natural voltage balancing is easily achievable in practice. Various implementations of the series inductance are compared in terms of loss, considering a fixed total volume. It is found that the realization with four inductors coupled on the same custom ferrite core results in the minimum loss among the considered candidates. The approach is verified by experimental results on a 400-to-48 V, 3 kW SAB prototype using GaN devices and featuring 400 W/in³ power density. A flat efficiency curve is obtained, with 99% peak efficiency, 97.5% full-load efficiency, and 98% efficiency at 20% load.

Chapter 4 presents a galvanically isolated version of the SAB converter. Galvanic isolation is achieved by inserting small transformers between the inverters and the rectifier bridges. The main novelty of this work is the custom core magnetic structure with planar windings, uniquely designed for the iSAB configuration. The magnetic structure couples all the transformers, and integrates the series inductances on the same core, therefore reducing the footprint of the magnetics. The approach is verified by experimental results on a 400-to-48 V, 3 kW, 400 kHz iSAB prototype using GaN devices and having 96.7% peak efficiency.

Chapter 5 addresses the second part of the thesis, discussing the topic of Modular Silicon Carbide (SiC) Based String Inverters for Medium-voltage Transformerless PV Systems. A series-stackable modular converter architecture is used as an interface between a low-voltage dc (LVDC) to medium-voltage (MV) three-phase ac grid. Each module is based on a quadruple active bridge (QAB) converter that operates as a DC transformer. The QAB stage produces three isolated copies of the input dc voltage, allowing flexible stacking of three single-phase dc-to-ac inverter stages.

The module configuration with QAB stage takes advantage of three-phase ac power cancellation, therefore minimizing energy storage requirements. Each of the module phases processes a pulsating power having a component at twice the line frequency. This presents a challenge in maintaining zero-voltage switching (ZVS) on the secondary sides of the QAB during low-power portions of the line cycle. The design of the QAB stage is covered in this thesis. A detailed analysis of ZVS switching waveforms is presented, including effects of nonlinear device capacitances. It is shown how ZVS can be achieved at all times using a relatively small circulating current provided by the magnetizing inductance of the high-frequency transformer. Analytical expressions are given for the optimal magnetizing inductance values and the dead times of the QAB primary and secondary bridges [60, 61]. The approach is verified by experimental results on a 1 kV, 10 kW SiC-based prototype, demonstrating a relatively flat efficiency curve with a peak efficiency of 97.1% at 75% load.

6.2 Future Work Directions

Voltage scaling of semiconductor devices in a stacked active bridge (SAB) converter, presented in Chapter 2, is investigated empirically, using data provided by the EPC GaN manufacturer. This analysis can be further extended by deeper studies of the physical mechanisms behind increased specific on-resistance (RSP) of the very low voltage-rated devices. Furthermore, a similar analysis can be conducted for SiC devices.

Steady-state analysis of voltage sharing among the modules in the SAB under timing mismatch and other tolerances in the circuit is presented in Chapter 3. Dynamic modeling of the balancing mechanisms would be a useful extension of this work. A more detailed analysis of the effect of the coupling coefficient of the series inductors in the magnetic structure on the voltage balancing between the modules would be a valuable contribution.

Chapter 4 introduces an isolated SAB (iSAB) with an advanced magnetic structure that integrates the four transformers, together with the series inductors on the same custom-made ferrite core. A useful research direction can be a more detailed study of the flux sharing between

the different core posts, which can be beneficial for leakage flux estimation, as well as a more precise core loss prediction.

Chapter 5 discusses hardware design optimization of a Quadruple-Active-Bridge (QAB) stage in a dc to three-phase ac module. Since the QAB stage needs to provide a stiff dc bus voltage for each of the secondary inverters, tight voltage regulation is required. More advanced control techniques can be investigated, in order to achieve a fast transient response to abrupt changes in the load, which can come from the ac grid side.

The modularization concept can be applied to the Direct Power Converter (DPx) shown in Fig. 6.1 [13], which aims at addressing the challenge of efficient high step-down conversion,

The converter consists of only two switches, a transformer, and input and output filter capacitors. During on-time, shown in Fig. 6.2a, both of the devices are on, and the power is directly transferred from the input to the output through the transformer. During the off-time, as shown in Fig. 6.2b, both of the devices are off, and a resonant circuit is formed between the magnetizing inductance of the transformer and the parasitic capacitances of the two devices. At the end of the resonant transition, the magnetizing current is reset to its initial value, and the voltages across the switches are zero, achieving soft-switching. This converter features high efficiency while operating with high duty cycles. Nonetheless, high duty-cycle results in high peak voltage across the primary-side switch, as shown in (6.1),

$$V_{Q1,pk} = \frac{\pi}{2} \frac{V_{IN}}{1 - D}, \quad (6.1)$$

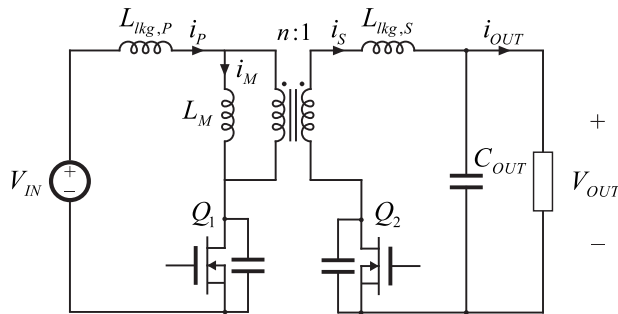


Figure 6.1: Direct Power Converter (DPx).

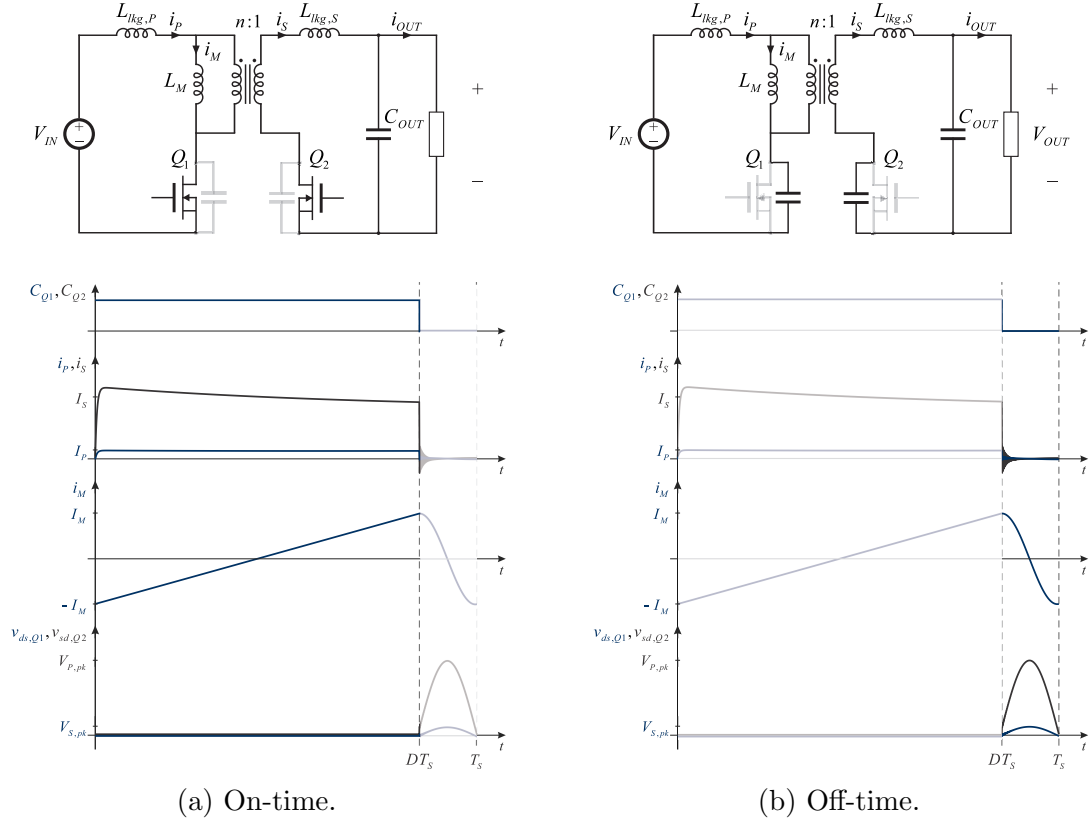


Figure 6.2: Equivalent circuits and operating waveforms of DPx over the switching period.

which results in the requirement for high-voltage-rated semiconductor devices on the primary side.

As discussed in Chapter 2, splitting the high voltage side into multiple modules, as shown in Fig. 6.3, enables the use of devices with lower voltage rating and with better specific on-resistance, thus improving performance. The modularization brings additional advantages, such as the utilization of smaller turns-ratio transformers, which are simpler to design, and increased output current capability of the converter. The voltage stress on the primary side devices could be further reduced by introducing active-clamp circuitry.

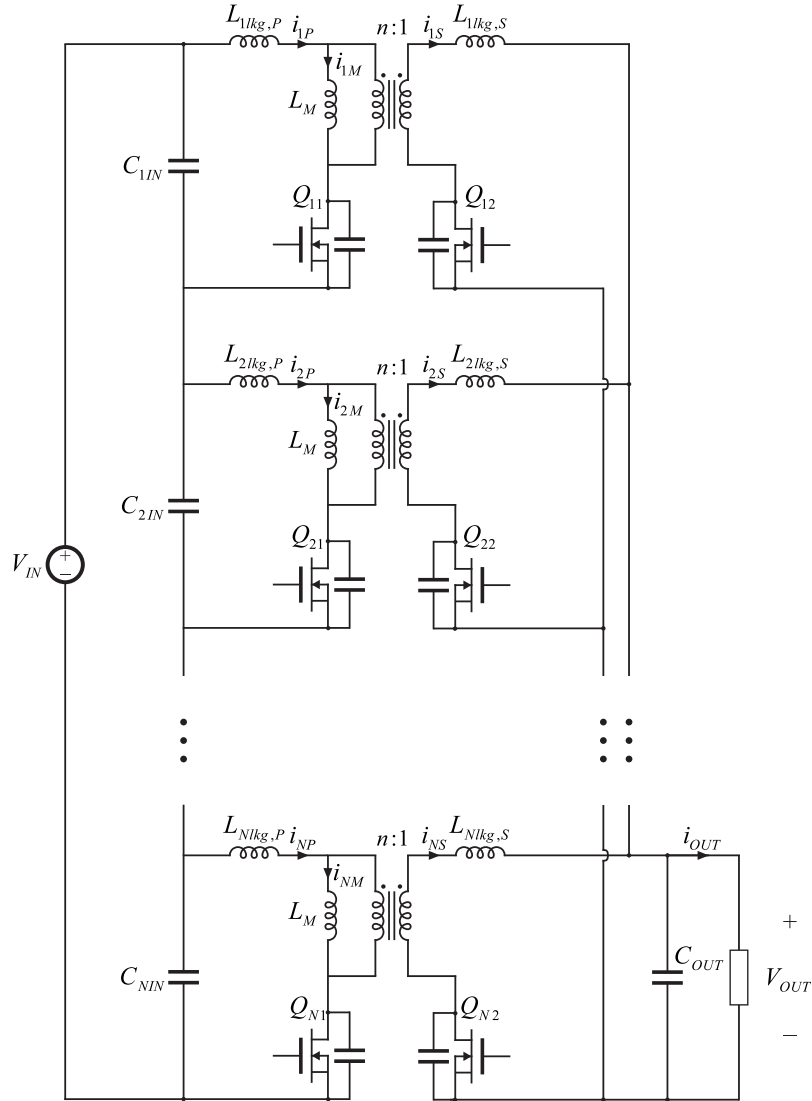


Figure 6.3: Modular, stacked active bridge direct power converter (SABDPx).

Bibliography

- [1] <https://www.hitachienergy.com/us/en/news/perspectives/2021/08/power-electronics-revolutionizing-the-world-s-future-energy-systems>. 2021.
- [2] <https://epc-co.com/epc/products/gan-fets-and-ics>. 2022.
- [3] Rose A. Abramson, Samantha J. Gunter, David M. Otten, Khurram K. Afridi, and David J. Perreault. Design and evaluation of a reconfigurable stacked active bridge dc/dc converter for efficient wide load-range operation. In 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), pages 3391–3401, 2017.
- [4] P. K. Achanta, B. B. Johnson, G.-S. Seo, and D. Maksimovic. A multilevel dc to three-phase ac architecture for photovoltaic power plants. IEEE Transactions on Energy Conversion, 34(1):181–190, March 2019.
- [5] Michael Antivachis, Matthias Kasper, Dominik Bortis, and Johann W. Kolar. Analysis of capacitive power transfer GaN ISOP multi-cell DC/DC converter systems for single-phase telecom power supply modules. In IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, pages 1280–1287, 2016.
- [6] R. Ayyanar, R. Giri, and N. Mohan. Active input-voltage and load-current sharing in input-series and output-parallel connected modular DC-DC converters using dynamic input-voltage reference scheme. IEEE Transactions on Power Electronics, 19(6):1462–1473, 2004.
- [7] Jaeil Baek, Youssef Elasser, Kaladhar Radhakrishnan, Houle Gan, Jonathan P. Douglas, Harish K. Krishnamurthy, Xin Li, Shuai Jiang, Charles R. Sullivan, and Minjie Chen. Vertical stacked LEGO-PoL CPU voltage regulator. IEEE Transactions on Power Electronics, 37(6):6305–6322, 2022.
- [8] Jaeil Baek, Ping Wang, Shuai Jiang, and Minjie Chen. LEGO-PoL: A 93.1% 54v-1.5v 300a merged-two-stage hybrid converter with a linear extendable group operated point-of-load (LEGO-PoL) architecture. In 2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL), pages 1–8, 2019.
- [9] Ward Bower, Chuck Whitaker, William Erdman, Michael Behnke, and Mark Fitzgerald. Performance test protocol for evaluating inverters used in grid-connected photovoltaic systems. 12 2010.

- [10] Luis Camurca, Marius Langwasser, Rongwu Zhu, and Marco Liserre. Future mvdc applications using modular multilevel converter. In 2020 6th IEEE International Energy Conference (ENERGYCon), pages 1024–1029, 2020.
- [11] Hua Chen. Advanced electrified automotive powertrain with composite dc-dc converter. In Ph.D. Thesis, University of Colorado Boulder., 2016.
- [12] Minjie Chen and H. Vincent Poor. High-frequency power electronics at the grid edge: A bottom-up approach toward the smart grid. IEEE Electrification Magazine, 8(3):6–17, 2020.
- [13] José A. Cobos, Alejandro Castro, Óscar García-Lorenz, Juan Cruz, and Álvaro Cobos. Direct power converter -dpx- for high gain and high current applications. In 2022 IEEE Applied Power Electronics Conference and Exposition (APEC), pages 1016–1022, 2022.
- [14] Samantha Coday, Nathan Ellis, Nicole Stokowski, and Robert C.N. Pilawa-Podgurski. Design and implementation of a (flying) flying capacitor multilevel converter. In 2022 IEEE Applied Power Electronics Conference and Exposition (APEC), pages 542–547, 2022.
- [15] L. F. Costa, G. Buticchi, and M. Liserre. Modular Smart Transformer architectures: An overview and proposal of a interphase architecture. In 2017 IEEE 8th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), pages 1–7, 2017.
- [16] Levy F. Costa, Giampaolo Buticchi, and Marco Liserre. Modular smart transformer architectures: An overview and proposal of a interphase architecture. In 2017 IEEE 8th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), pages 1–7, 2017.
- [17] D. Costinett, D. Maksimovic, and R. Zane. Circuit-oriented treatment of nonlinear capacitances in switched-mode power supplies. IEEE Transactions on Power Electronics, 30(2):985–995, Feb 2015.
- [18] D. Costinett, H. Nguyen, R. Zane, and D. Maksimovic. GaN-FET based dual active bridge dc-dc converter. In 2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), pages 1425–1432, 2011.
- [19] D. Costinett, R. Zane, and D. Maksimović. Discrete-time small-signal modeling of a 1 mhz efficiency-optimized dual active bridge converter with varying load. In 2012 IEEE 13th Workshop on Control and Modeling for Power Electronics (COMPEL), pages 1–7, June 2012.
- [20] Daniel Costinett, Dragan Maksimovic, and Regan Zane. Design and control for high efficiency in high step-down dual active bridge converters operating at high switching frequency. IEEE Transactions on Power Electronics, 28(8):3931–3940, 2013.
- [21] Daniel Costinett, Dragan Maksimovic, and Regan Zane. Circuit-oriented treatment of nonlinear capacitances in switched-mode power supplies. IEEE Transactions on Power Electronics, 30(2):985–995, 2015.
- [22] Daniel Costinett, Hien Nguyen, Regan Zane, and Dragan Maksimovic. GaN-FET based dual active bridge DC-DC converter. In 2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), pages 1425–1432, 2011.

- [23] Ratul Das and Hanh-Phuc Le. A regulated 48v-to-1v/100a 90.9%-efficient hybrid converter for pol applications in data centers and telecommunication systems. In 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), pages 1997–2001, 2019.
- [24] R.W.A.A. De Doncker, D.M. Divan, and M.H. Kheraluwala. A three-phase soft-switched high-power-density dc/dc converter for high-power applications. IEEE Transactions on Industry Applications, 27(1):63–73, 1991.
- [25] Moshe Domb. High power density, high efficiency 380v to 52v LLC converter utilizing E-Mode GaN switches. In PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, pages 1–7, 2016.
- [26] P. L. Dowell. Effects of eddy currents in transformer windings. Proceedings of the Institution of Electrical Engineers, 113(8):1387–1394, August 1966.
- [27] Youssef Elasser, Jaeil Baek, Kaladhar Radhakrishnan, Houle Gan, Jonathan Douglas, Harish K. Krishnamurthy, Xin Li, Shuai Jiang, Charles R. Sullivan, and Minjie Chen. Vertical stacked 48V-1V LEGO-PoL CPU voltage regulator with 1A/mm² current density. In 2022 IEEE Applied Power Electronics Conference and Exposition (APEC), pages 1259–1266, 2022.
- [28] Nathan M. Ellis and Robert C.N. Pilawa-Podgurski. A symmetric dual-inductor hybrid dickson converter for direct 48V-to-PoL conversion. In 2022 IEEE Applied Power Electronics Conference and Exposition (APEC), pages 1267–1271, 2022.
- [29] Robert W. Erickson and Dragan Maksimović. Converter Transfer Functions, pages 277–346. Springer International Publishing, Cham, 2020.
- [30] R.W. Erickson and D. Maksimović. Fundamentals of Power Electronics. Springer International Publishing, 2020.
- [31] J. Everts. Closed-form solution for efficient ZVS modulation of DAB converters. IEEE Transactions on Power Electronics, 32(10):7561–7576, Oct 2017.
- [32] J. Everts, F. Krismer, J. Van den Keybus, J. Driesen, and J. W. Kolar. Optimal zvs modulation of single-phase single-stage bidirectional dab ac–dc converters. IEEE Transactions on Power Electronics, 29(8):3954–3970, Aug 2014.
- [33] Chao Fei, Rimon Gadelrab, Qiang Li, and Fred C. Lee. High-frequency three-phase interleaved LLC resonant converter with GaN devices and integrated planar magnetics. IEEE Journal of Emerging and Selected Topics in Power Electronics, 7(2):653–663, 2019.
- [34] Chao Fei, Fred C. Lee, and Qiang Li. High-efficiency high-power-density LLC converter with an integrated planar matrix transformer for high-output current applications. IEEE Transactions on Industrial Electronics, 64(11):9072–9082, 2017.
- [35] Leopoldo G. Franquelo, Jose Rodriguez, Jose I. Leon, Samir Kouro, Ramon Portillo, and Maria A.M. Prats. The age of multilevel converters arrives. IEEE Industrial Electronics Magazine, 2(2):28–39, 2008.
- [36] Rimon Gadelrab, Fred C. Lee, and Qiang Li. Three-phase interleaved LLC resonant converter with integrated planar magnetics for telecom and server application. In 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), pages 512–519, 2020.

- [37] Yucheng Gao, Vivek Sankaranarayanan, Robert W. Erickson, and Dragan Maksimovic. Analysis and attenuation of differential-mode resonances due to winding capacitances in high-power planar transformers. In 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), pages 1411–1417, 2020.
- [38] T. Guillod, D. Rothmund, and J. W. Kolar. Active magnetizing current splitting zvs modulation of a 7kv/400v dc transformer. IEEE Transactions on Power Electronics, pages 1–1, 2019.
- [39] B. Hafez, H. S. Krishnamoorthy, P. Enjeti, U. Borup, and S. Ahmed. Medium voltage AC collection grid for large scale photovoltaic plants based on medium frequency transformers. In 2014 IEEE Energy Conversion Congress and Exposition (ECCE), pages 5304–5311, 2014.
- [40] Y. Hayashi, Y. Matsugaki, and T. Ninomiya. Capacitively isolated multicell Dc-Dc transformer for future Dc distribution system. IEEJ journal of industry applications, 6:268–277, 2017.
- [41] F. Hoffmann, L. Camurca, and M. Liserre. Modular EV Fast Charging Station Architectures based on Multiphase-Medium-Frequency Transformer. In IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society, pages 1327–1332, 2018.
- [42] Qingyun Huang, Qingxuan Ma, Alex Q. Huang, and Michael de Rooij. 400V-to-48V GaN modular LLC resonant converter with planar transformers. In 2021 IEEE Energy Conversion Congress and Exposition (ECCE), pages 2129–2135, 2021.
- [43] J. E. Huber and J. W. Kolar. Solid-State Transformers: On the Origins and Evolution of Key Concepts. IEEE Industrial Electronics Magazine, 10(3):19–28, 2016.
- [44] Jonas E. Huber and Johann W. Kolar. Volume/weight/cost comparison of a 1mva 10 kv/400 v solid-state against a conventional low-frequency distribution transformer. In 2014 IEEE Energy Conversion Congress and Exposition (ECCE), pages 4545–4552, 2014.
- [45] M. R. Islam, A. M. Mahfuz-Ur-Rahman, M. M. Islam, Y. G. Guo, and J. G. Zhu. Modular Medium-Voltage Grid-Connected Converter With Improved Switching Techniques for Solar Photovoltaic Systems. IEEE Transactions on Industrial Electronics, 64(11):8887–8896, 2017.
- [46] R. A. Jensen and C. R. Sullivan. Optimal core dimensional ratios for minimizing winding loss in high-frequency gapped-inductor windings. In 2003 IEEE Appl. Power Electron. Conf. Expo. (APEC), volume 2, pages 1164–1169 vol.2, 2003.
- [47] Shuai Jiang, Stefano Saggini, Chenhao Nan, Xin Li, Chee Chung, and Mobashar Yazdani. Switched tank converters. IEEE Transactions on Power Electronics, 34(6):5048–5062, 2019.
- [48] S.D. Johnson and R.W. Erickson. Steady-state analysis and design of the parallel resonant converter. IEEE Transactions on Power Electronics, 3(1):93–104, 1988.
- [49] M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar. ZVS of power mosfets revisited. IEEE Transactions on Power Electronics, 31(12):8063–8067, Dec 2016.
- [50] J.G. Kassakian and D. Lau. An analysis and experimental verification of parasitic oscillations in paralleled power MOSFET's. IEEE Transactions on Electron Devices, 31(7):959–963, 1984.

- [51] Somnath Khatua, Debaprasad Kastha, and Santanu Kapat. A transformer-less quadruple active half-bridge converter for the two-stage 48 V VRM application. In 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), pages 488–495, 2019.
- [52] M. N. Kheraluwala, R. W. Gascoigne, D. M. Divan, and E. D. Baumann. Performance characterization of a high-power dual active bridge dc-to-dc converter. IEEE Transactions on Industry Applications, 28(6):1294–1301, Nov 1992.
- [53] Samir Kouro, Mariusz Malinowski, K. Gopakumar, Josep Pou, Leopoldo G. Franquelo, Bin Wu, Jose Rodriguez, Marcelo A. Pérez, and Jose I. Leon. Recent advances and industrial applications of multilevel converters. IEEE Transactions on Industrial Electronics, 57(8):2553–2580, 2010.
- [54] C. Kumar, G. Buticchi, and M. Liserre. Operation and control of smart transformer-based electric vehicles charging system. In IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society, pages 4266–4271, 2017.
- [55] Yutian Lei, Wen-Chuen Liu, and Robert Carl Nikolai Pilawa-Podgurski. An analytical method to evaluate and design hybrid switched-capacitor and multilevel converters. IEEE Transactions on Power Electronics, 33(3):2227–2240, 2018.
- [56] Yanchao Li, Xiaofeng Lyu, Dong Cao, Shuai Jiang, and Chenhao Nan. A high efficiency resonant switched-capacitor converter for data center. In 2017 IEEE Energy Conversion Congress and Exposition (ECCE), pages 4460–4466, 2017.
- [57] Yanchao Li, Xiaofeng Lyu, Dong Cao, Shuai Jiang, and Chenhao Nan. A 98.55% efficiency switched-tank converter for data center application. IEEE Transactions on Industry Applications, 54(6):6205–6222, 2018.
- [58] A. Lidow, M. de Rooij, J. Strydom, D. Reusch, and J. Glaser. GaN Transistors for Efficient Power Conversion. Wiley, 2019.
- [59] Branko Majmunović and Dragan Maksimović. 400-48-V stacked active bridge converter. IEEE Transactions on Power Electronics, 37(10):12017–12029, 2022.
- [60] B. Majmunović, S. Mukherjee, R. Mallik, S. Dutta, G. Seo, B. Johnson, and D. Maksimović. Soft Switching Over the Entire Line Cycle for a Quadruple Active Bridge DCX in a DC to Three-Phase AC Module. In 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), pages 3464–3471, 2020.
- [61] Branko Majmunović, Satyaki Mukherjee, Trent Martin, Rahul Mallik, Soham Dutta, Gab-Su Seo, Brian Johnson, and Dragan Maksimović. 1 kv, 10-kw sic-based quadruple active bridge dcx stage in a dc to three-phase ac module for medium-voltage grid integration. IEEE Transactions on Power Electronics, 37(12):14631–14646, 2022.
- [62] B.P. McGrath and D.G. Holmes. Multicarrier pwm strategies for multilevel inverters. IEEE Transactions on Industrial Electronics, 49(4):858–867, 2002.
- [63] B.P. McGrath, D.G. Holmes, and T. Lipo. Optimized space vector switching sequences for multilevel inverters. IEEE Transactions on Power Electronics, 18(6):1293–1301, 2003.

- [64] Satyaki Mukherjee, Ashish Kumar, and Sombuddha Chakraborty. Comparison of DAB and LLC DC–DC converters in high-step-down fixed-conversion-ratio (DCX) applications. IEEE Transactions on Power Electronics, 36(4):4383–4398, 2021.
- [65] R. T. Naayagi. Electromagnetic compatibility issues of dual active bridge dc-dc converter. In 2013 International Conference on Energy Efficient Technologies for Sustainability, pages 699–703, 2013.
- [66] Ahmed Nabih and Qiang Li. Low-profile and high-efficiency 3 kw 400 v-48 v llc converter with a matrix of four transformers and inductors for 48v power architecture for data centers. In 2021 IEEE Energy Conversion Congress and Exposition (ECCE), pages 1813–1819, 2021.
- [67] G. Oggier, G. O. García, and A. R. Oliva. Modulation strategy to operate the dual active bridge dc-dc converter under soft switching in the whole operating range. IEEE Transactions on Power Electronics, 26(4):1228–1236, April 2011.
- [68] Z. Ouyang and M. A. E. Andersen. Overview of planar magnetic technology—fundamental properties. IEEE Transactions on Power Electronics, 29(9):4888–4900, 2014.
- [69] Z. Ouyang, O. C. Thomsen, and M. A. E. Andersen. Optimal design and tradeoff analysis of planar transformer in high-power DC–DC converters. IEEE Transactions on Industrial Electronics, 59(7):2800–2810, 2012.
- [70] David J. Perreault, Jingying Hu, Juan M. Rivas, Yehui Han, Olivia Leitermann, Robert C.N. Pilawa-Podgurski, Anthony Sagneri, and Charles R. Sullivan. Opportunities and challenges in very high frequency power conversion. In 2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition, pages 1–14, 2009.
- [71] H. Qin and J. W. Kimball. Solid-state transformer architecture using AC-AC dual-active-bridge converter. IEEE Transactions on Industrial Electronics, 60(9):3720–3730, Sep. 2013.
- [72] H. Qin and J. W. Kimball. Solid-state transformer architecture using ac-ac dual-active-bridge converter. IEEE Transactions on Industrial Electronics, 60(9):3720–3730, Sep. 2013.
- [73] Hengsi Qin and Jonathan W. Kimball. Generalized average modeling of dual active bridge DC–DC converter. IEEE Transactions on Power Electronics, 27(4):2078–2084, 2012.
- [74] Hengsi Qin and Jonathan W. Kimball. Closed-loop control of dc–dc dual-active-bridge converters driving single-phase inverters. IEEE Transactions on Power Electronics, 29(2):1006–1017, 2014.
- [75] J. Rodriguez, Jih-Sheng Lai, and Fang Zheng Peng. Multilevel inverters: a survey of topologies, controls, and applications. IEEE Transactions on Industrial Electronics, 49(4):724–738, 2002.
- [76] JosÉ Rodriguez, Steffen Bernet, Bin Wu, Jorge O. Pontt, and Samir Kouro. Multilevel voltage-source-converter topologies for industrial medium-voltage drives. IEEE Transactions on Industrial Electronics, 54(6):2930–2945, 2007.
- [77] S. Saeed and J. Garcia. Extended operational range of dual-active-bridge converters by using variable magnetic devices. In 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), pages 1629–1634, March 2019.

- [78] J. A. Santiago-González, D. M. Otten, and D. J. Perreault. Light load efficiency improvements in dual active bridge converters via dead time control. In 2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL), pages 1–7, June 2018.
- [79] R. Severns. Additional losses in high frequency magnetics due to non ideal field distributions. In [Proceedings] APEC '92 Seventh Annual Applied Power Electronics Conference and Exposition, pages 333–338, 1992.
- [80] J.H. Spreen. Electrical terminal representation of conductor loss in transformers. IEEE Transactions on Power Electronics, 5(4):424–429, 1990.
- [81] Charles R. Sullivan, Bradley A. Reese, Aaron L. F. Stein, and Phyo Aung Kyaw. On size and magnetics: Why small efficient power inductors are rare. In 2016 International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM), pages 1–23, 2016.
- [82] Yi Tang and Frede Blaabjerg. Power decoupling techniques for single-phase power electronics systems — an overview. In 2015 IEEE Energy Conversion Congress and Exposition (ECCE), pages 2541–2548, 2015.
- [83] Q. Tian, A. Q. Huang, H. Bai, J. Lu, Hui Teng, M. Mcammond, and A. Brown. A novel light load performance enhanced variable-switching-frequency and hybrid single-dual-phase-shift control for single-stage dual-active-bridge based ac/dc converter. In IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, pages 1227–1232, Oct 2016.
- [84] D. van der Linde, C. A. M. Boon, and J. B. Klaassens. Design of a high-frequency planar power transformer in multilayer technology. IEEE Transactions on Industrial Electronics, 38(2):135–141, 1991.
- [85] Jacobus Daniel van Wyk and Fred C. Lee. On a future for power electronics. IEEE Journal of Emerging and Selected Topics in Power Electronics, 1(2):59–72, 2013.
- [86] M. Vasiladiotis, A. Rufer, and A. Béguin. Modular converter architecture for medium voltage ultra fast ev charging stations: Global system considerations. In 2012 IEEE International Electric Vehicle Conference, pages 1–7, 2012.
- [87] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca. Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters. In 2002 IEEE Workshop on Computers in Power Electronics, 2002. Proceedings., pages 36–41, 2002.
- [88] V. Vorperian and Slobodan Cuk. A complete dc analysis of the series resonant converter. In 1982 IEEE Power Electronics Specialists conference, pages 85–100, 1982.
- [89] Shuo Wang, Hongfei Wu, Fred C. Lee, and Qiang Li. Integrated matrix transformer with optimized PCB winding for high-efficiency high-power-density LLC resonant converter. In 2019 IEEE Energy Conversion Congress and Exposition (ECCE), pages 6621–6627, 2019.
- [90] A.F. Wittulski and R.W. Erickson. Steady-state analysis of the series resonant converter. IEEE Transactions on Aerospace and Electronic Systems, AES-21(6):791–799, 1985.
- [91] Dan Holden Wolaver. Fundamental study of dc to dc conversion systems. 1969.

- [92] Bo Yang, F.C. Lee, A.J. Zhang, and Guisong Huang. LLC resonant converter for front end DC/DC conversion. In APEC. Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.02CH37335), volume 2, pages 1108–1112 vol.2, 2002.
- [93] YOKOGAWA. WT3000 Precision Power Analyzer, 2 2014. 8th Edition.
- [94] Li Zhang and Xinbo Ruan. Control schemes for reducing second harmonic current in two-stage single-phase converter: An overview from dc-bus port-impedance characteristics. IEEE Transactions on Power Electronics, PP:1–1, 01 2019.
- [95] Weimin Zhang, Fred Wang, Daniel J. Costinett, Leon M. Tolbert, and Benjamin J. Blalock. Investigation of gallium nitride devices in high-frequency LLC resonant converters. IEEE Transactions on Power Electronics, 32(1):571–583, 2017.
- [96] S. Zhao, Q. Li, F. C. Lee, and B. Li. High-Frequency Transformer Design for Modular Power Conversion From Medium-Voltage AC to 400 VDC. IEEE Transactions on Power Electronics, 33(9):7545–7557, 2018.
- [97] Jianglin Zhu. Transformerless Stacked Active Bridge DC-DC Converters: Analysis, Synthesis and Design. PhD thesis, University of Colorado Boulder, 2020.
- [98] Jianglin Zhu and Dragan Maksimovic. 48 V-to-1 V transformerless stacked active bridge converters with merged regulation stage. In 2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL), pages 1–6, 2020.
- [99] Jianglin Zhu and Dragan Maksimović. A family of transformerless stacked active bridge converters. In 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), pages 19–24, 2019.
- [100] Jianglin Zhu and Dragan Maksimović. Transformerless stacked active bridge converters: Analysis, properties, and synthesis. IEEE Transactions on Power Electronics, 36(7):7914–7926, 2021.

Appendix A

Derivation of Relations Between Parameters Mismatch and Voltage Imbalance Between The Modules in SAB

The voltage balancing analysis presented in Section III is based on the normalized voltage and current expressions (A.1) and (A.2) obtained from the state-plane diagrams shown in Fig. 3.5, for two modules under imbalanced conditions.

Given a normalized voltage imbalance Δm , the state-plane diagram in Fig. 3.5a for Module 1 can be solved as follows:

$$\begin{aligned}
 J_{x,1} &= \sqrt{J_{pk,1}^2 - 4(1 - \Delta m)} \\
 \alpha_1 &= \arccos \left(1 - \frac{(J_{pk,1} - J_{x,1})^2 + 4(1 - \Delta m)^2}{2(\Delta m^2 + J_{pk,1}^2)} \right) \\
 \beta_1 &= \frac{J_{x,1} + J_{y,1}}{2 - \Delta m} \\
 \zeta_1 &= \frac{J_{pk,1} - J_{y,1}}{-\Delta m} \\
 \frac{\pi}{F} &= \alpha_1 + \beta_1 + \zeta_1 \\
 J_{IN,1} &= \frac{F}{2\pi} \left(\frac{J_{y,1} - J_{x,1}}{2} \beta + \frac{J_{pk,1} + J_{y,1}}{2} \zeta \right)
 \end{aligned} \tag{A.1}$$

Similarly, a set of expressions can be written for the state-plane diagram in Fig. 3.5b for Module 2:

$$\begin{aligned}
J_{x,2} &= \sqrt{J_{pk,2}^2 - 4(1 + \Delta m)} \\
\alpha_2 &= \arccos \left(1 - \frac{(J_{pk,2} - J_{x,2})^2 + 4(1 + \Delta m)^2}{2(\Delta m^2 + J_{pk,2}^2)} \right) \\
\beta_2 &= \frac{J_{x,2} + J_{y,2}}{2 + \Delta m} \\
\zeta_2 &= \frac{J_{pk,2} - J_{y,2}}{\Delta m} \\
\frac{\pi}{F} &= \alpha_2 + \beta_2 + \zeta_2 \\
J_{IN,2} &= \frac{F}{2\pi} \left(\frac{J_{y,2} - J_{x,2}}{2} \beta + \frac{J_{pk,2} + J_{y,2}}{2} \zeta \right)
\end{aligned} \tag{A.2}$$

The steady-state solution under imbalanced conditions is found through an iterative procedure using (A.1) and (A.2). For a given $t_{\Delta\beta}$, Δm is swept from zero to a maximum value. The steady-state solution is obtained for Δm for which the charge-balance of the input capacitors is satisfied, i.e., $J_{IN,1} = J_{IN,2}$. If the condition cannot be met, the circuit cannot reach a steady-state operation for the given timing mismatch $t_{\Delta\beta}$, which implies that the voltages diverge until one of them takes up the entire input voltage.

Appendix B

Loss Modelling in SAB

This appendix presents a brief summary of the loss modelling used in this chapter.

B.1 Inductor loss

B.1.1 Copper loss

Inductor winding loss is calculated as follows:

$$P_{copper} = \sum_{k=1}^{10} I_{k,RMS}^2 R_{k,ac,winding}, \quad (\text{B.1})$$

where $I_{k,RMS}$ is the RMS value of the k^{th} harmonic of the inductor current. Ac resistance at the k^{th} harmonic is found as $R_{k,ac,winding} = R_{dc,winding} F_{k,r}$, where $F_{k,r}$ is calculated according to [26].

B.1.2 Core loss

Losses in the ferrite core are calculated using the iGSE method [87], using the Steinmetz parameters for the core material: K_{fe} , α and β ,

$$P_{core} = \frac{1}{T_{sw}} \int_0^{T_{sw}} k_i \left| \frac{dB}{dt} \right|^\alpha (\Delta B)^{\beta-\alpha} dt, \quad (\text{B.2})$$

where B is the flux density through the center post of the ferrite core. Parameter k_i can be found as [87]:

$$k_i = \frac{K_{fe}}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos \theta|^\alpha 2^{\beta-\alpha} d\theta}. \quad (\text{B.3})$$

B.2 Semiconductor device losses

B.2.1 Conduction loss

Device conduction loss is found as:

$$P_{cond,dev} = k_t R_{ds,on} I_{dev,RMS}^2, \quad (B.4)$$

where $I_{n,RMS}$ is the RMS value of device current. Parameters k_t and $R_{ds,on}$ are a temperature coefficient and the on resistance of the device, respectively.

B.2.2 Turn-on loss

Switching loss due to partial hard turn on of a device is estimated as:

$$P_{turn_on,dev} = C_{Q,\Delta V} (\Delta V)^2 f_{sw}, \quad (B.5)$$

where ΔV is the voltage across the device prior to turn-on transition, and $C_{Q,\Delta V}$ is the charge equivalent capacitance of the device, taking ΔV into account. More details on finding the equivalent charge capacitance can be found in [21].

B.2.3 Turn-off loss

When the turn off currents are high, the drain to source voltage discharges sooner than the entire current shifts from the channel to the parasitic capacitance of the device. This results in a turn-off loss, which can be approximated as:

$$P_{turn_off,dev} = \frac{I_{off}^2 t_{off}^2}{48 C_{Q,V}} f_{sw}, \quad (B.6)$$

where I_{off} is the the device current prior to turn-off transition, t_{off} is the overlap transition time, and $C_{Q,V}$ is the charge equivalent capacitance of the device.

B.3 PCB losses

Conduction losses in the PCB traces are found as:

$$P_{PCB,cond} = \sum_{k=1}^n R_{k,trace} I_{k,RMS}^2, \quad (B.7)$$

where R_{trace} is a DC or AC resistance of the particular trace, depending on the nature of the current, and $I_{k,RMS}$ is the RMS current through the trace. All the trace resistances, including vias, are calculated by importing 3D models from Altium Designer to Ansys Maxwell 3D. The resistances are then found by running eddy-current simulations.