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Reliable CPS Design for Mitigating Semiconductor and Battery Aging in Electric Vehicles

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***Abstract*—Reliability and performance of cyber-physical systems (CPS) in electric vehicles (EVs) are influenced by three design aspects: (i) controller design; (ii) battery usage, i.e., battery rate capacity and aging effects; (iii) processor aging of the in-vehicle embedded platform. In this paper, we present a two-phase design optimization framework involving control algorithm development, battery modeling and processor aging analysis. First, before processor aging, a Pareto front between quality of control (QoC) and battery usage is obtained. Second, as the processor ages, the controller is re-optimized considering the prolonged sampling period to avoid QoC deterioration of safety-critical applications with a compromise on battery usage and comfort-related applications. An outlook following this line of research on reliable CPS design in EVs is discussed, that we believe, will be pursued by researchers in the CPS community.**

***Keywords*-cyber-physical systems; battery aging; quality of control; semiconductor aging;**

I. Introduction

In the past few years, electric vehicles (EVs) have been developed by most major automotive manufacturers in the world as a potential alternative of conventional vehicles with internal combustion engines (ICEs). The main advantages of EVs over ICE vehicles are independence from fossil fuels, zero local emission, high operating energy conversion efficiency, and friendliness to smart transportation. In cyber-physical systems (CPS) of EVs run many important embedded control applications, such as electric motor control, anti-lock braking control, yaw stabilization, adaptive cruise control, and battery management. They are often evaluated by quality of control (QoC). As illustrated in Figure 1, in order to ensure vehicle performance and reliability, besides control algorithms development, the CPS design needs to take into account a number of application-specific issues like battery usage and processor aging.

Battery is the key component of an EV. One major concern obstructing the market penetration of EVs is the range anxiety. An intuitive solution is to provide a battery pack with large *capacity*. However, the capacity comes at a cost, which is another factor hindering the public acceptance of EVs. In addition, the capacity is restricted by the space that can be allocated to the battery pack in EVs. Moreover, the battery weight increases together with the capacity, leading to higher energy consumption. From a certain point, adding battery capacity does not result in a longer driving range anymore. For all these practical reasons, the battery pack in an EV usually has limited capacity. In order to make the best use of the given battery, the rate capacity and aging effects need to be mitigated.

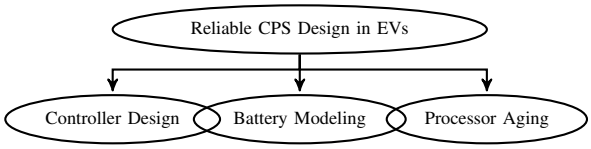

Figure 1. Design aspects for reliable CPS in EVs

All off-the-shelf battery packs are labeled with a nominal capacity. However, due to the rate capacity effect, the full charge capacity (FCC) of a battery pack, which is defined to be the amount of electric charges that can be delivered from the battery after it is fully charged, actually varies with different discharging current profiles. Generally speaking, larger discharging current tends to reduce the FCC. In practice, an approximate relationship between the average discharging current and the FCC can be built. For most common lithium-ion batteries in the market, the capacity could get significantly compromised if the rate capacity effect is not properly considered in the CPS design of EVs.

Battery aging occurs with chemical reduction and oxidation of the electrolyte by the anode and cathode, respectively, and thermal decomposition of the electrolyte. As the battery ages, the nominal FCC fades. Reaching 80% of the nominal capacity is a commonly used end of life (EOL) criterion. There are two aging processes — calender aging and cycle aging, depending on if the battery is used or not. The magnitude of the discharging current is a major factor contributing to capacity fading. Since the battery aging is negligible for low C-rates (e.g., 1C rate means that the fully charged battery will be fully discharged in 1 hour.), the peak discharging current can be used as a metric to minimize for battery aging mitigation.

There has been extensive work to model the battery behavior. In general, researchers have developed three types of battery models to characterize the rate capacity effect — electrochemical models [1], electrical-circuit models [2] and analytical models [3]. An analytical model describes the battery at a higher level of abstraction than the other two types. The major properties of the battery are modeled by a couple of equations, which makes this type of model

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much easier to use. With carefully chosen parameters based on experimental data, reasonable accuracy of about $10\,\%$ error can be achieved. Battery aging, as a more complex phenomenon, is often analyzed with experimental data. In this work, we use extended Peukert's law presented in [3] to characterize battery capacity rate effect and the data in [4] for battery aging.

One method to improve the battery usage while mitigating the rate capacity and aging effects is to design the controller in such a way that both the energy consumption of the control task and the discharging current are small. In this work, we present an optimization framework considering QoC as one design objective and battery usage as the other. We quantify the battery usage by the number of times the control system, powered up by a fully charged battery pack, can reach a steady state after a disturbance occurs. The Pareto front exploring the trade-off between these two design objectives is found.

In the CPS design of EVs, another important issue besides battery usage is processor aging. Electronics plays a major role in CPS of modern vehicles. A processor is the key part ensuring correct functioning and timing behavior of control applications. As the integrated circuit fabrication technology has progressed, processors become more and more susceptible to aging. Although electronic control units (ECUs) in conventional vehicles typically use medium- to low-end processors, next-generation smart vehicles are expected to be equipped with a number of intelligent applications, and thus require high-end embedded processors. There are many paths for digital signal transmission in a processor and each path consists of a number of transistors. The time that a signal takes to travel through a path is called path delay. As a processor ages, the transistor switching time is increased and the path delay gets prolonged. Signals may not be able to go through some of the paths within one clock cycle, which results in timing constraints violation and false calculation.

This issue can be handled by safety margins, supply voltage regulation or clock frequency scaling [5]. Currently, the most widely used method is implementing a frequency or voltage guard band. The processor is operated at a lower frequency or higher voltage to meet worst-case path delays. It is noted that a higher supply voltage makes transistor switching faster. In this way, as the processor ages and gets slower, the system does not have to be changed. However, the guard band leads to a passive design and a waste of resources. In cost-sensitive domains like EVs, there is a strong motivation to make full use of resources and minimize the guard band, while reliable functionality is maintained.

Instead of having a fixed setting that deals with worst-case conditions, some newer approaches suggest changing settings dynamically. By monitoring the critical path with the longest delay, the supply voltage of the processor is adjusted accordingly [6]. These approaches are effective but can be difficult to implement. The supply voltage is usually limited by the maximum allowable input current in the circuit, cooling constraints and other temperature-dependent reliability issues, which are sensitive in the automotive domain.

In this work, we use autonomous frequency scaling to deal with processor aging. On-chip monitors could be used to measure the delay of the critical path. It always has to be guaranteed that the signal transmission can be complete along any path within one clock cycle, in order to ensure correct functionality. Therefore, the processor operating frequency is reduced based on the new critical path delay by a frequency synthesis circuit. From the control point of view, a shorter sampling period can potentially provide a better QoC. With a smaller processor operating frequency, the sampling period increases and QoC gets deteriorated, which is dangerous and thus highly unwanted for safety-critical applications, such as electric motor control in EVs. To deal with the above situation, we propose to re-optimize the controller with the longer sampling period, which results from processor aging. The processor aging effect is mitigated in the way that QoC does not get deteriorated with a compromise on battery usage.

Organization of the paper: Design aspects of CPS in EVs including control algorithms development, battery modeling and processor aging analysis are discussed in Section II. The two-phase design optimization framework is presented in Section III, together with experimental results. An outlook following the line of research on reliable CPS design in EVs is summarized in Section IV.

II. Design Aspects of CPS in Electric Vehicles

As discussed, there are three aspects to take account of, in order to design reliable CPS with high performance in EVs. First, we describe basics of control applications under consideration. Second, battery rate capacity and aging effects are presented. Third, aging of the processor in the embedded computing platform is analyzed.

A. Feedback control applications

In this work, we consider discrete-time linear single-input single-output (SISO) systems. The dynamics is as follows,

$$\begin{aligned} \mathbf{x}[k+1] &= \mathbf{A}_d\mathbf{x}[k] + \mathbf{B}_d u[k], \\ y[k] &= \mathbf{C}_d\mathbf{x}[k], \end{aligned} \tag{1}$$

where sampling instants are $\{t[k]|k \in \mathbb{N}\}$ and the sampling period is $t[k+1]-t[k]=h$. The system state is $\mathbf{x}[k] \in \mathbb{R}^n$, the control input is $u[k]$, and the system output is $y[k]$. System matrices $\mathbf{A}_d$, $\mathbf{B}_d$, and $\mathbf{C}_d$ are of appropriate dimensions.

One common control objective is to make $y[k] \to y_{ref}$ as soon as possible, where y_{ref} is the desirable value for $y[k]$ to achieve. Towards this and other application-specific control objectives, we need to design $u[k]$ utilizing the states $\mathbf{x}[k]$.

This is essentially a state-feedback controller with a general structure as follows,

$$u[k] = \mathbf{K} \times \mathbf{x}[k] + F \times y_{ref}, \tag{2}$$

where $\mathbf{K}$ is the feedback gain vector and F is the static feedforward gain. The system closed-loop dynamics becomes

$$\mathbf{x}[k+1] = (\mathbf{A}_d + \mathbf{B}_d\mathbf{K})\mathbf{x}[k] + \mathbf{B}_d F y_{ref}. \tag{3}$$

The feedback gain vector $\mathbf{K}$ is designed to stabilize the closed-loop system matrix $(\mathbf{A}_d + \mathbf{B}_d\mathbf{K})$. A commonly used technique to compute $\mathbf{K}$ is pole-placement, where $\mathbf{K}$ is designed by placing the eigenvalues (i.e., poles) of $(\mathbf{A}_d + \mathbf{B}_d\mathbf{K})$ at the desired location. Different choices of poles p result in different QoCs. The static feedforward gain F is designed to achieve $y[k] \to y_{ref}$ and computed by

$$F = 1/(\mathbf{C}_d(\mathbf{I} - \mathbf{A}_d - \mathbf{B}_d \times \mathbf{K})^{-1}\mathbf{B}_d), \tag{4}$$

where $\mathbf{I}$ is an n-dimensional identity matrix.

Settling time is a common metric to quantify QoC. It is defined to be the time duration t_s necessary for $y[k]$ to reach and stay in a certain range around y_{ref}. Shorter t_s indicates better QoC. Besides, we consider the constraint on the input signal $u[k]$, e.g., voltage or current limit of the input energy source. The controller needs to be designed such that the maximum value of $u[k]$ does not exceed the limit U_{max}, i.e., $u[k] \leq U_{max}$.

In this work, we consider a DC motor running in the speed mode, which is a key application in EVs. There are two system states — the angular velocity of the motor and the current in the armature circuit. The control input is the voltage applied to the motor and the system output is the motor speed. Clearly, the control input cannot exceed the operating voltage of the battery pack. Another constraint is on the armature current.

B. Battery rate capacity and aging effects

As discussed, a natural objective of CPS design in EVs is to minimize the energy consumption of each control task. However, this is not enough to thoroughly and accurately consider the energy impact from control applications. Due to the battery rate capacity effect, the FCC of a battery pack varies depending on discharging current profiles. This effect needs to be considered in CPS design in EVs, since different controller designs (choices of poles) result in different current profiles. The rate capacity effect is described by extended Peukert's law [3] as shown below,

$$L_t = \frac{a}{\left(\frac{\sum_{k=1}^{n} I_k(t'_{k+1} - t'_k)}{L_t}\right)^d}, \tag{5}$$

which is able to handle non-constant loads. $t'_1 = 0$ is the starting time stamp and $L_t = t'_{n+1}$ is the total duration that the battery can be used and divided into n slots. In this particular work, each slot is equal to one sampling period

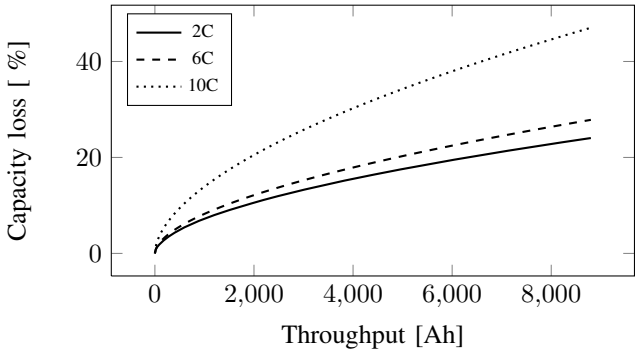

Figure 2. Capacity loss for a 2.2Ah cell cycled at various C-rates with 80% DoD at the temperature of 45°C

of the control system. For the kth time slot, I_k is the average current for the sampling period from t_k to t_{k+1}. Parameters a and d are determined by experimental data. It is noted that this is an approximation of the battery rate capacity effect by considering the average discharging current. As discussed in Section I, more accurate methods can be used as well, and the entire design framework presented in this paper still holds.

Besides the settling time t_s as a design objective to quantify QoC, we propose battery usage as the other objective in the CPS design for EVs, which is characterized by the number of times r the control system can reach a steady state after a disturbance occurs with a fully charged battery pack. In order to maximize r, (i) the energy consumption of each control task has to be small, and (ii) the average discharging current is desirably small to improve the FCC. Assuming that the battery only powers the electric motor control task, based on the control systems description in Section II-A and (5), r can be calculated as

$$r = \frac{a}{\left(\frac{\sum_{k=1}^{n_{sp}} I_k(t_{k+1} - t_k)}{t_s}\right)^d \times t_s}, \tag{6}$$

where t_s is the time taken to complete one control task, i.e., settling time, as discussed in Section II-A. $t_{k+1} - t_k$ is the sampling period of the control system, i.e., h. These time slots are constant since we consider control systems with constant sampling period. n_{sp} is the total number of sampling periods in each task. As presented in Section II-A, when the controller design is decided, from experiments we can get the value of t_s and the supplied current profile, based on which the sum of current $\sum_{k=1}^{n_{sp}} I_k(t_{k+1} - t_k)$ can be derived. In general, with different controller designs, i.e., eigenvalue selections, these two objectives t_s and r take different values. It is thus a constrained bi-objective optimization problem.

Battery aging is another effect with considerable influence on the nominal FCC along with time. The magnitude of the discharging current is a main factor contributing to battery aging, besides depth of discharge (DoD) and temperature.

Measurements illustrating the dependency of capacity fading on the discharge current shows that at low discharge rates, the aging effect is negligible while at high C-rates, a serious impact can be observed [4]. Therefore, battery aging is more related to the peak discharging current of a control task. The problem of high C-rates gets more severe in hybrid EVs as their battery's capacity is typically small [7]. The loss of capacity for different C-rates using the results from [4] is plotted in Figure 2.

C. Processor aging

As discussed in Section I, automotive-use processors are becoming more and more susceptible to aging, which gets QoC degraded. This is dangerous and highly undesirable in safety-critical domains like EVs. The main transistor aging mechanisms are Hot Carrier Injection (HCI) and Negative Bias Temperature Instability (NBTI). They cause degradation in the electrical characteristics of transistors, such as a shift of the threshold voltage. As a result, the switching times of transistors are prolonged.

As mentioned in Section I, one appropriate way to keep functions correct is reducing the processor operating frequency. Before everything else, we need to know the extend of aging. An on-chip aging monitor could be implemented to watch the delay of the critical path. Shrinking transistor dimensions make larger within-die and die-to-die variations. The static timing analysis at the circuit level is not able to precisely determine which path among all is the critical one in modern processors. However, we can identify all critical path candidates, which are a subset of all paths in the processor that can become the critical one during the runtime. To avoid interference on real functions run on the processor, Critical Path Replicas (CPRs), which are replicas of these candidates, are fabricated on the chip. The aging monitor then sends signals to CPRs to get the current critical path delay, based on which it is known whether the operating frequency needs to be reduced and if so, by how much. A frequency generator changes the operating frequency accordingly, if necessary.

When the processor operating frequency is decreased, the execution time of control programs gets longer. The sampling period as described in Section II-A is mainly constrained by the worst-case execution time (WCET) of the control program. Therefore, the sampling period of the control system is increased. It is possible to counteract the aging effect by inserting a safety margin between the WCET and the sampling period. However, this is a waste of resources and not desirable for cost-sensitive domains like EVs. In general, a shorter sampling period means more frequent response from the controller and thus potentially better QoC. When the increased sampling period due to processor aging is fed into the control system presented in Section II-A, we can obtain the results showing how QoC changes.

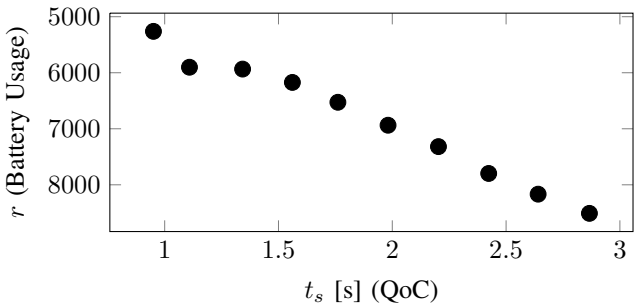

Figure 3. The trade-off between QoC and battery usage before the processor ages

Based on the method presented in [5], we are able to estimate how much processor aging can be expected in EVs. The processor only ages when it is used, i.e., in the non-idle state. Taking an electric bus as an example, the drivers take shifts and the bus is driven approximately 16 hours every day. The processor is always in the non-idle state while the bus is driven. After 5 years of use, the overall operation time of the processor is approximately $\frac{2}{3} \times 5 = 3.33$ years. According to the results presented in [5], the processor is roughly 10% slower.

III. Design Optimization Framework and Experimental Results

We present two optimization phases for CPS design of EVs. In Phase I, before the processor ages, there are two objectives to optimize — t_s to quantify QoC and the battery usage r. This is a constrained bi-objective optimization problem. Constraints include system stability, control input saturation (370V), and the maximum allowed current in the motor (200A) and battery cells (5A). The motor starts from 1200 RPM and aims at 3600 RPM. The sampling period is 0.22s. Both gradient-based and stochastic techniques can be used to solve such an optimization problem. A combination of them is able to achieve better solutions [8]. The trade-off between t_s and r is shown in Figure 3. Ten controller designs are selected to represent a good distribution. It is noted that r only reflects the battery rate capacity effect. The relationship between r and the peak current of the control task in one battery cell, which is used to illustrate the battery aging, is reported in Figure 4. The overall discharging current is evenly distributed among parallel battery cells. It can be seen that for the ten controllers selected to be designed, the battery rate capacity effect is in line with the battery aging effect, i.e., the peak current of the control task in one battery cell I^c_{max} rises as r decreases. Therefore, r is an objective quantifying battery usage taking both effects into account. With the peak currents in Figure 4 and data from [4], we can approximate the battery life[1] of each design point as shown in Figure 5.

[1]A quadratic model is built for the relationship between battery life and the discharging current.

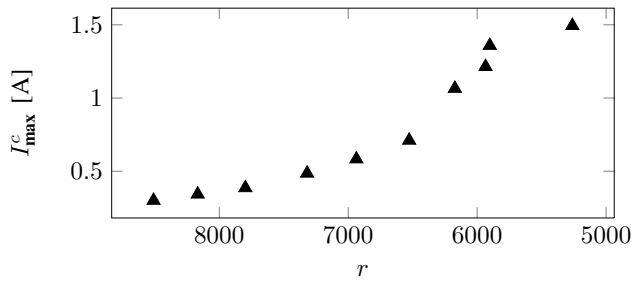

Figure 4. The relationship between battery rate capacity effect and battery aging

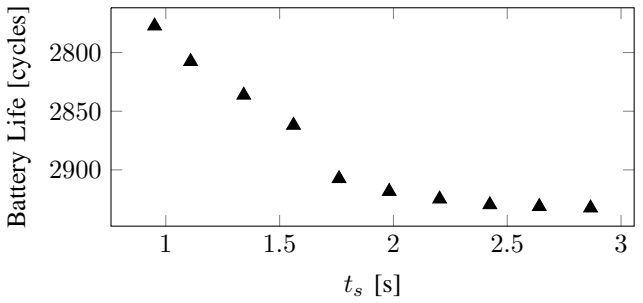

Figure 5. The battery life corresponding to QoC of each design point

In Phase II, after the processor ages by 10%, we evaluate the QoC and battery usage of each controller design as shown in Figure 6. For all cases, QoC gets worse. This is highly undesirable for safety-critical applications, where QoC deterioration must be prevented, Therefore, we propose to re-optimize the controller with the constraint that the QoC has to at least remain unchanged. The battery usage becomes the single objective to maximize. Results are reported in Figure 7. For every design case, QoC does not get deteriorated, with a compromise in the battery usage.

IV. Outlook

In this section, we discuss four topics along the direction of reliable CPS design in EVs that can be pursued by researchers in the CPS community in the future.

A. Incorporation of all initial conditions

One of the shortcomings of the presented results in Section III is that one can only deal with a single initial condition which is not very realistic in practical scenarios. Note that the probability of fixing the initial condition of a system to a specific value is almost zero. Therefore, the results in Section III need to be generalized to the case of an infinite (even uncountable) set of initial conditions. More specifically, it is interesting to know if there exists one controller that is able to respect the input constraint and keeps the QoCs not deteriorated after the processor ages, for all possible initial conditions. Furthermore, a number of controllers can be computed to cover the entire space of initial conditions, in order to achieve better QoC and battery usage.

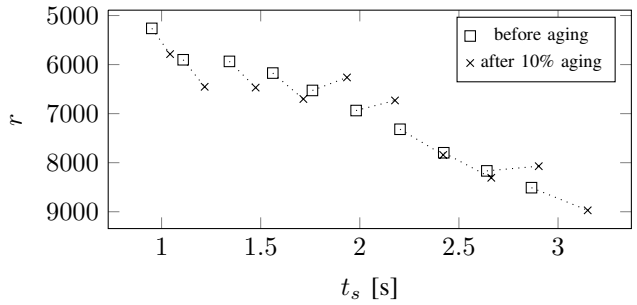

Figure 6. Processor aging effects in both QoC and battery usage. Two points for the same controller design before and after processor aging are connected with a dotted line.

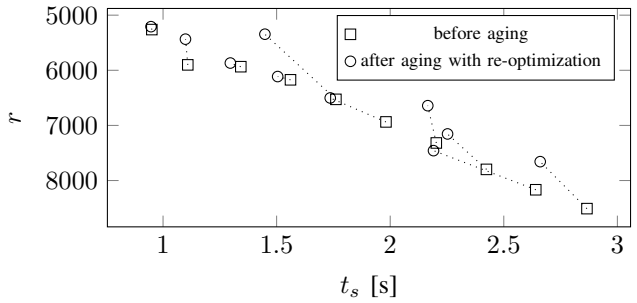

Figure 7. Processor aging is mitigated with controller re-optimization. For all design cases, QoC does not get deteriorated.

One major challenge is to find the feasible set of initial conditions for a given controller. Assuming that the operating envelope of the actuator is $\mathcal{U}$, the corresponding feasible set of system states is $\mathcal{X}$. The uncountable set of initial conditions can be chosen as the largest level set of a Lyapunov function candidate contained in $\mathcal{X}$, which ensures that the actuator operates under the envelope $\mathcal{U}$ as the system evolves. One can maximize the size of the set of initial conditions by choosing the Lyapunov function appropriately. A similar method can be applied to deal with the constraint on QoC. After computing the feasible set of initial conditions for a given controller, an optimization technique can be applied to derive the desired controller.

B. QoC compromise of comfort-related applications

In this work, we consider the speed control of an electric motor, which is a safety-critical application. Therefore, the QoC cannot be deteriorated as the processor ages. It is common that multiple applications run on one ECU. Some of the applications can be comfort-related, such as suspension control. Besides the controller re-optimization method presented in this work that keeps QoCs of safety-critical applications not degraded with a decrease on the battery usage along the processor aging, QoCs of these comfort-related applications could also be compromised to fulfill the same purpose.

Assuming that there are three applications $\mathcal{C}_1$, $\mathcal{C}_2$ and $\mathcal{C}_3$ running on one processor, where $\mathcal{C}_1$ and $\mathcal{C}_2$ are safety-critical, and $\mathcal{C}_3$ is comfort-related. The control loops of

these three applications take l_1, l_2 and l_3 time units, respectively. The sampling order is in the round-robin fashion, i.e., $\mathcal{C}_1, \mathcal{C}_2, \mathcal{C}_3, \mathcal{C}_1, \mathcal{C}_2, \mathcal{C}_3, \cdots$. The sampling period of each application is then $h = l_1 + l_2 + l_3$. After the processor ages, l_1, l_2 and l_3 get prolonged. As discussed before, h becomes longer and QoCs of all applications could get worse. One method to mitigate processor aging in this scenario is that we keep h unchanged. Control loops of safety-critical applications $\mathcal{C}_1$ and $\mathcal{C}_2$ are completed as before, which leaves insufficient time for $\mathcal{C}_3$. This comfort-related application $\mathcal{C}_3$ can be suspended when the sampling period is up and continues in the second sampling period. The QoC of $\mathcal{C}_3$ will get worse, but the QoC and battery usage of $\mathcal{C}_1$ and $\mathcal{C}_2$ remain unchanged. It is worth investigating whether the QoC of comfort-related applications or battery usage should be compromised as the processor ages, and what is the optimal sampling order for the scenario of multiple applications running on one processor.

C. Alternative method of control algorithms design

The results in Section III are obtained by using the pole-placement method to design a controller making the closed-loop system globally asymptotically stable. However, owing to errors arising from the software implementation of the controller, (e.g., quantization errors due to fixed-point arithmetics and sampling errors due to time discretization), the implementation of this control algorithm can only guarantee practical stability, i.e., under the implementation, the trajectories of the controlled system converge to a bounded set around the equilibrium point, and the size of the bounded set is proportional to the error in the implementation.

Alternatively, one can use the recently developed symbolic techniques providing provably correct controllers taking into account the implementation errors and operating envelope of the actuators. One can use those techniques to synthesize controllers enforcing logical specifications on the system rather than only conventional stability. Examples of those specifications include linear temporal logic or automata on infinite strings, and as such they are not amenable to classical approaches for control systems. Limitation of this method is that a considerably larger memory is required. We refer the interested readers to [9] for a brief survey of those existing techniques.

D. Battery aging mitigation

Battery aging is a complex process to analyze. In this work, we use the peak current of a control task to approximately compute the battery life, since most works on battery aging in the battery community only provide experimental results of constant discharging currents. In order to more precisely take battery aging effect into account, battery tests with discharging current profiles under real-world automotive scenarios are required. With these test results, it can be more accurately known which controller design better mitigates the battery aging, which makes the Pareto front exploring the trade-off between QoC and battery usage practically more useful.

Building a hybrid electrical energy storage (EES) system consisting of a supercapacitor and a battery could also mitigate battery aging. As discussed in Section II-B, battery aging is mainly caused by large discharging currents, which can be supplied by the supercapacitor [10], since the life cycles of supercapacitors are considerably larger than those of lithium-ion batteries. There have been works studying EES systems with multiple elements [11], [12] and how to dimension them. However, none of the papers have considered battery aging in the CPS design context, which can be explored in the future work.

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