Atomic Layer Deposition Enabled Interconnect and Packaging Technologies for As-Grown Nanowire Devices

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The final copy of this thesis has been examined by the signatories, and we find that both the content and the form meet acceptable presentation standards of scholarly work in the above mentioned discipline.

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Atomic Layer Deposition Enabled Interconnect and Packaging Technologies for As-Grown Nanowire Devices

Thesis directed by Professor Ronggui Yang and Professor Y. C. Lee

Abstract

Nanowires (NWs) have attracted considerable interests in many applications due to their small size, extremely high surface-to-volume ratio, and superior material properties. They are promising material candidates as fundamental building blocks for future electronic, optoelectronic, energy, sensor, and biomedical applications. The majority of research activities have focused on the synthesis of NWs. With the advent of high-performance NWs, interconnect and packaging of NWs are becoming increasingly important for device applications. Vertical NW array devices, compared with horizontal NW configurations, are of great importance for achieving ultra-high integration density at the device level without the need of additional assembly and rearrangement processes. Currently, however, it is very challenging to interconnect and package as-grown vertical NWs because of their small sizes and extremely high aspect ratios. This thesis work contributes to the design, fabrication, and characterization of atomic layer deposition (ALD)-enabled interconnect and packaging technologies for as-grown vertical NWs. The first goal of this thesis is to develop a generic interconnect technology that can interconnect and encapsulate as-grown vertical NWs. We have developed a novel interconnect solution by encapsulating as-grown NWs with a nanoscale multilayer consisting of ALD-alumina and tungsten (W) layers for dielectric and electrical interconnects. The electrical connection of ALD-enabled interconnect was verified by the photoluminescence (PL) measurement of NWs. By injecting current into W interconnect along NWs, a dynamic PL tuning experiment was

demonstrated, and this experiment verified the connection of W interconnect on NWs. The effect of the matrix layer on PL measurement has been studied and a process has been developed to eliminate such an effect. With local removal of ALD-W at the tips of the NWs, we verified that the PL is measured from the tip of the NWs. By measuring temperature dependence of peak PL wavelength from the tips of the NWs, we are able to predict tip temperature and corresponding thermal performance of as-grown NW devices. With the increase of device integration density and power consumption in electronics and optoelectronics, thermal management is one of the most critical packaging issues. A much higher power density than that in conventional planar devices is expected for as-grown vertical NW devices due to the potentially much high integration density. The second goal of this thesis is thus devoted to developing an effective cooling design and fabrication for as-grown NW devices. Thermal simulation is used to guide the design and fabrication of cooling-enhanced as-grown NW devices. NWs are successfully encapsulated with adjustable-thickness coverage of electroplated copper as effective heat spreading. Thermal simulation predicts a reduction of thermal resistance by 52X for the electroplated copper on as-grown NW devices compared with state-of-the-art polymer encapsulation.

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Chapter 1. Introduction

1.1 Introduction

In the past decade, tremendous progress has been made to synthesize NWs with superior properties [1-3]. NWs are promising material candidates as fundamental building blocks for future electronic [4-13], optoelectronic [14-21], energy [22,23], sensor [24-26], and biomedical [27,28] applications. Synthesized wires are usually constructed as horizontal device configurations by NW assembly, interconnect, and packaging processes [29-33]. A vertically configured NW-based device is of great importance to achieving high integration density at a device level. However, little progress has been made and little attention has been given to the development of interconnect and packaging technologies for as-grown NWs. Compared with horizontally configured devices, it is very challenging to interconnect and package as-grown NW devices due to their small size and large surface-to-volume ratio. This thesis is aimed at the development of novel interconnect and packaging technologies for as-grown NW devices.

This chapter provides necessary background and gives an overview for this thesis. Section 1.2 introduces nanowire-based devices. Section 1.3 classifies nanowire-based device configurations according to present applications. Section 1.4 describes the important background to state-of-the-art interconnect methods for as-grown NW devices. Section 1.5 discusses crucial thermal management issues in packaging as-grown NW devices. Section 1.6 summarizes the research objectives and technical contributions, and outlines the organization of this thesis.

1.2 Nanowire-based Devices

Many NW-enabled devices have demonstrated enhanced device performance in the

laboratory. This section describes some nanowire-based devices, such as anodes for batteries, DNA sensors, field effect transistors (FETs), and light-emitting diodes (LEDs).

Nanowire-based Electrodes for Batteries. Nanowire materials have been used as high-performance electrodes for batteries because of large surface areas provided by the wires [22-23]. The performance is enhanced because a greater surface area enables a better use of the electrode material for charging and discharging.

Nanowire-based biomedical sensors. Silicon NWs have been constructed as detectors of DNA and sensors to recognize the biomedical reagents by measuring the conductance change with/without the binding of DNA on the surface of NW [28]. Due to the small size of the wires, nanowire-based DNA sensors are much more sensitive in detecting the conductance change.

Nanowire-based FETs. NWs have been employed as FETs [4-13]. Silicon nanowire-based FET further extends the device downsizing due to the wrapped-around gate structure that allows a better electrostatic gate control than conventional planar transistors do [10].

Nanowire-based LEDs. c-axis GaN nanowire is the ideal material for LED application due to its unique properties such as having a direct bandgap and being free of dislocations [34,35]. These dislocation-free nanowire-based LEDs may reach the highest possible efficiency due to their potentially excellent internal quantum efficiency and light extraction efficiency [36,37].

1.3 Configurations of Nanowire-based Devices

Configurations of nanowire-based devices can be classified into two main groups: horizontal and vertical. Most present devices are constructed with a horizontal configuration. Fig. 1.1 shows a horizontal nanowire device for LED application [21]. To construct an LED device, p- and n-type GaN NWs were first synthesized on two different growth substrates, respectively.

Both p- and n-type NWs were then taken from the as-grown substrates by ultrasonic agitation and were assembled on a device substrate to configure p-n junction by dielectrophoresis. The p-n junction is at the cross region between the two wires. Metal pads for current inputs/outputs (IOs) were locally deposited on the ends of the NWs using focused-ion-beam (FIB) deposition or electron-beam lithography. Currently, horizontal four-terminal and two-terminal device structures are used in most nanowire applications.

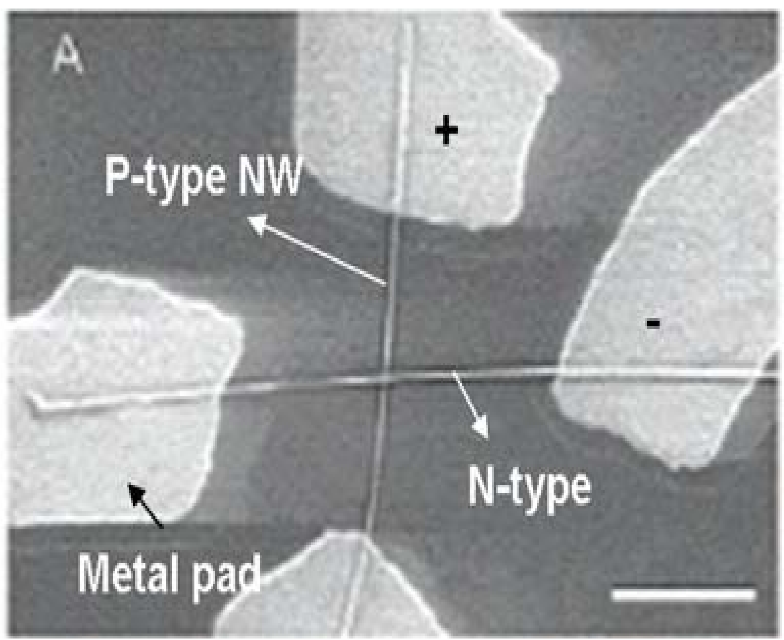


Fig. 1.1: Horizontal configuration of a NW-based LED. Scale bar is 1um [21].

Compared with horizontal devices, vertical or so-called as-grown NW-based devices are constructed on the as-grown NW directly. Fig. 1.2 shows core-shell as-grown NWs for LED devices [38]. N-type core NWs were first grown on a growth substrate, and p-type shells were then synthesized outside the n-type wires. The p-n junction is formed at the interface between the n-type core wire and the p-type shell. Metallization interconnect along the wire then needs to be fabricated for current input and output.

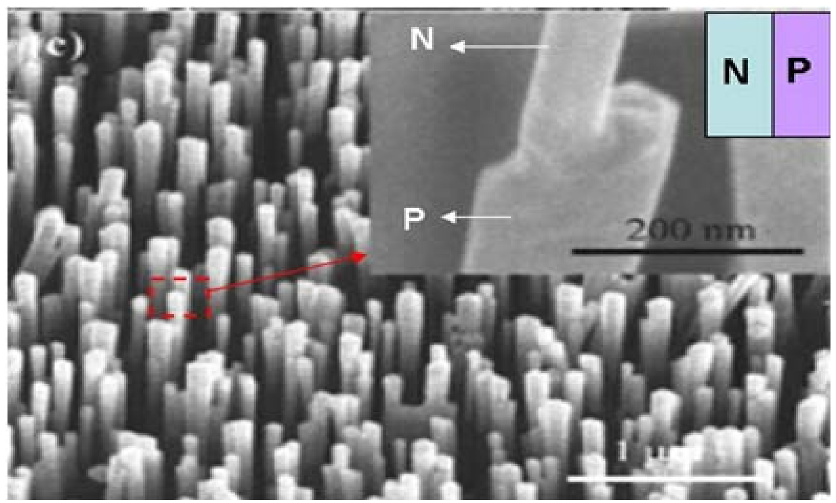


Fig. 1.2: Core-shell as-grown NWs for LED application [38].

For a horizontally configured NW device, the device size is limited by the length of the NW and metal pad size. The NW length is from a few hundreds of nanometer to a few microns. As a result, each device occupies a surface area based on the length of the NW. Although the wire length can be shrunk to a smaller dimension by controlling wire growth time, it significantly increases the difficulty in assembling extremely tiny NWs to form the p-n junction. The size of the metal pad for I/Os also determines the device size. Metal pad sizes need to be carefully designed to match the sizes of current probes for power supply. The current methods for metal interconnect utilize FIB deposition or E-beam lithography process. Nevertheless, it is clear that device size is difficult to be shrunk further, and device integration density is very low.

For a vertically configured NW device, the device size is extremely small due to the nature of as-grown configuration on which the device is built. Thus, the device integration density is extremely high compared with that in as-grown configuration. There is no additional assembly process in the device fabrication. However, to interconnect and package nanoscaled, high-aspect-ratio as-grown NWs in device fabrication is a challenge. Our study focuses on the

development of interconnect and packaging technologies for as-grown NW devices in order to achieve a high device integration density.

1.4 Interconnect of As-Grown Nanowire-based Devices

As-grown nanowire materials are promising fundamental building blocks for future applications and have been extensively studied over the past decade. However, there has been little progress in the development of interconnect and integration methods for electrically connecting as-grown NWs.

Parthangal et al. [39] demonstrated an approach to electrically connect vertically aligned nanowire arrays using conductive nanoparticles. Zinc oxide NWs were grown on gold catalyst layers through a thermal evaporation process. The bottom ends of the NWs that directly contacted with gold layers functioned as the bottom electrodes. To finish the electrical connecting path, the top ends of the NWs were deposited with an Au nanoparticle film as the top electrodes. The electrical path was formed from the bottom Au electrode through NWs to the top Au nanoparticle film. The top ends of the NWs were randomly coated with Au nanoparticles, but it is difficult to access the major surface along the as-grown nanowire for performance enhancement.

Latu-Romain et al. [40] presented a vertical integration method for as-grown NWs. Silicon and ZnO NWs were grown on a conductive layer as the bottom electrodes and were then encapsulated with chemical vapor deposition (CVD) oxides, spin-on-glass (SOG), and polymer (accuflo T-27 from Honeywell) as a robust structure. Filling materials were first spin-coated on NWs, and chemical mechanical polishing (CMP) was used to reduce the thickness of the filling material up to the top of the NWs. Fig. 1.3 shows the as-grown Si NWs (a) and filled polymer

after CMP (b and c). NWs' tips were exposed after the filling materials were etched by wet (d) or dry etching (e). Dry etching is a better choice to achieve anisotropic etching of filling materials. Metallic Ti/Au contacts as the top electrodes were patterned by lift-off technique on the top of the NWs. The electrical path formed from the bottom conductive layer through the NWs to the top electrode (f) is same as in the previous study.

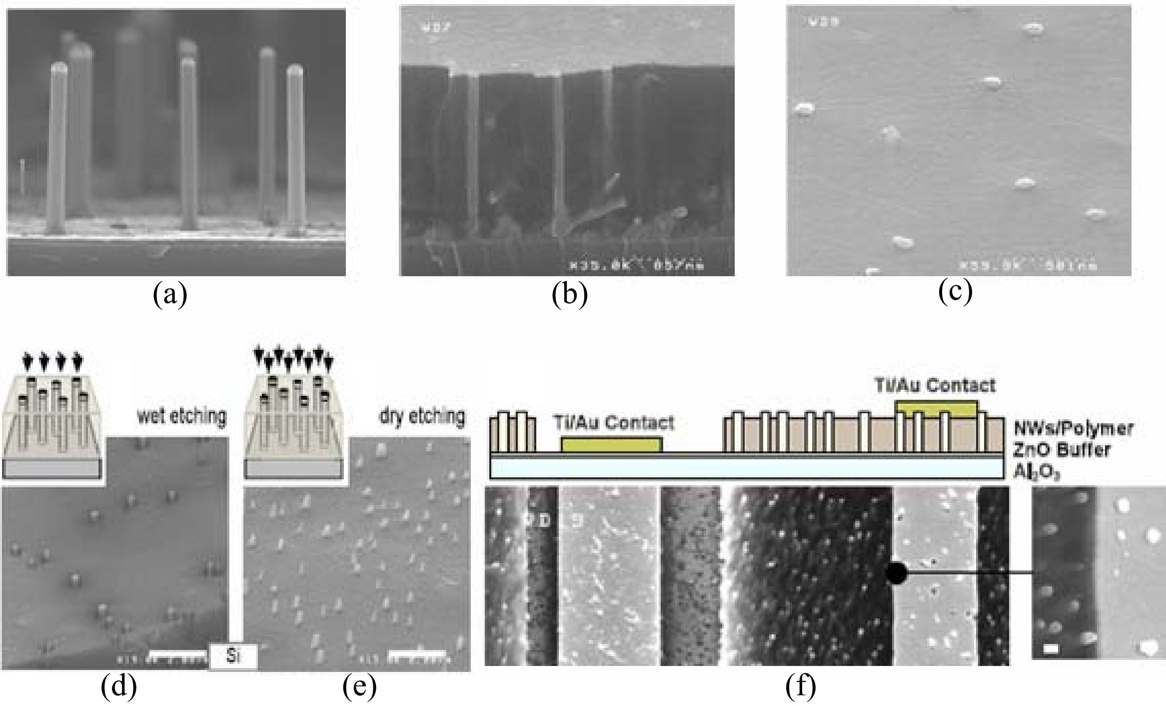


Fig. 1.3: (a) As-grown Si NWs with gold catalyst on top. (b) and (c) Polymer-integrated Si NWs after CMP. (d) Wet and (e) dry etchings of SOG-integrated Si and ZnO NWs after CMP. Scale bar is 2um. (f) Top and bottom metallic contacts on ZnO NWs embedded in ployner [40].

Islam et al. [41] demonstrated an epitaxial bridging technique to interconnect NWs. Two opposing silicon electrodes were first formed using wet etching. NWs were then grown from one silicon electrode and electrically connected to the other with the increase of growth time. Low

contact resistance between the wire and the electrode was achieved because the wire was grown from the catalyst on the electrode. The electrical path was from the silicon electrode through the NWs to the other electrode. In the fabrication of an as-grown NW device, the metallization process is needed for current input and output. Different interconnect processes have been developed for different applications. Lai et al. [16] demonstrated vertical nanowire array-based LEDs. ZnO NWs were grown on p-type GaN, and the p-n junction was formed at the interface between the nanowire and GaN film. The NWs were encapsulated with PMMA. The metal interconnect was deposited on top of the wires and p-GaN film. Likewise, an electrical path was formed from the bottom electrode on p-GaN film through ZnO NWs to the top electrode.

The present work seeks to develop a generic interconnect technology for as-grown NW arrays with a novel nanoscaled conductor/dielectric multilayer fabricated using atomic layer deposition (ALD). The metal interconnect is formed not only from both ends of NWs but also the surface along the NWs, as shown in the Fig. 1.4 (b). The interconnect along the nanowire is important for the utilization of the large surface area provided by the wires for performance enhancement. To use it for different applications, tips of the interconnected wires can either be covered by the metallization or be exposed without it.

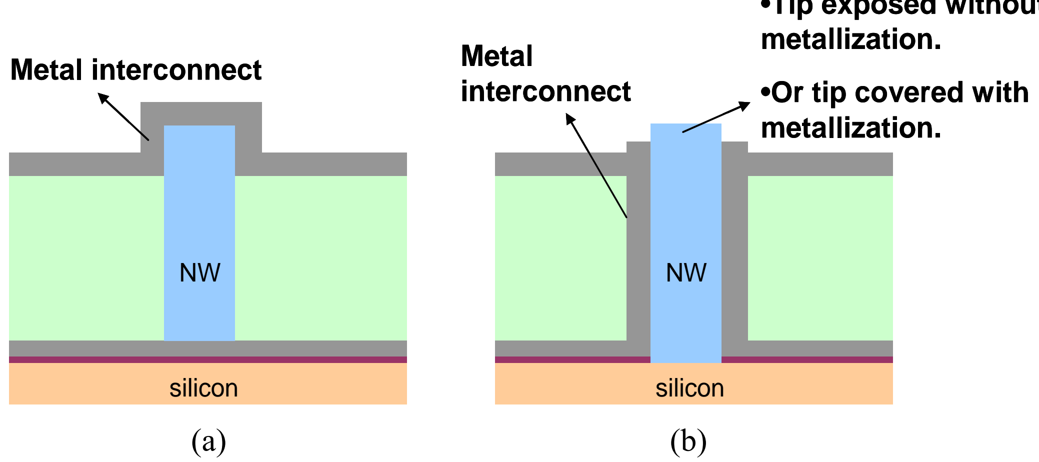


Fig. 1.4: Metal interconnect (a) on both ends and (b) along the surface of an as-grown NW.

1.5 Packaging of As-Grown Nanowire-based Devices

With the increase of device integration density and power consumption in electronics and optoelectronics, thermal management has emerged as one critical packaging issue. With high integration density in as-grown nanowire-based devices, a much higher power density than that in the conventional planar devices is expected. By far, what seems to be lacking is an effective thermal management solution in the packaging of as-grown NWs. For effective cooling, we have found that vertical NWs in fact provide us with a unique opportunity to access each hot device directly. Vertical nanowire array, as shown in Fig. 1-3 (a), offers an extremely high surface-to-volume ratio of each nanowire and a large space between the wires. A high thermal conductivity material can fill the space and provide an effective direct cooling contact to each nanowire.

Finite-element numerical simulation was conducted to study the heat spreading effect of a planar heat source on a substrate (case A) and an as-grown GaN NW heat source on the substrate with/without encapsulations (cases B-F). Detailed simulation conditions and results are listed in Table 1. We assumed constant temperature boundary condition (BC) at the bottom side of the substrate and adiabatic BC elsewhere. To create an equal heat source condition in both planar and NW configurations in the simulation, the heat source area was $4x10^6$ (nm^2) in all simulation cases. The geometry of the substrate, 200um x 200um x 200um (LxWxH), was chosen according to thermal constriction resistance.

Let us consider a planar GaN LED and its p-n junction heat source with an area of 2um × 2um (case A), fabricated at the center of a GaN substrate with a volume of 200um x 200um x 200um (LxWxH). A heat flux source was uniformly applied to the p-n junction region, and we obtained a junction-to-substrate thermal resistance of $0.18x10^4$ (K/W). When a vertical GaN NW (200nm x 200nm x 5um, LxWxH) without any encapsulation (case B) was used as the p-n

junction and heat source of the LED on a silicon substrate had the same volume as the GaN substrate, its thermal resistance, $48x10^4$ (K/W), was 267 times higher than that in the planar device configuration. Such a high resistance in a nanowire device without encapsulation is detrimental to device operation and limits its performance.

Currently, polymers and SOG are used as filling materials to encapsulate NWs. If a polymer such as Benzocyclobutene (BCB) is used to encapsulate the NW (case C), the thermal resistance drops from $48x10^4$ to $22x10^4$ (K/W). To enhance the thermal performance, the best way is to replace the low thermal conductivity encapsulation material with a high thermal conductivity one such as copper. If copper is used (case D), the thermal resistance is significantly reduced to $0.053x10^4$ (K/W). The thermal conductivity of copper used in the simulation was 360 W/mK, which was measured by pump-probe thermoreflectance technique explained in Appendix A. When filling the space with high thermal conductivity materials, the junction temperature and thermal resistance can be reduced by the merit of a large surface-to-volume ratio and effective heat spreading area of vertical NWs. In device applications, however, interconnects are needed. High-quality interconnects are important to provide a reliable electrical connection and dielectric isolation for NW devices, and it is important to study the thermal performance of NWs with interconnects and encapsulations.

The atomic layer deposition (ALD) process [42-43] is employed to deposit high-quality nanoscale electrical/dielectric interconnects. Assuming a total thickness of 40nm of ALD-alumina and W layers (20nm each) on a NW with copper encapsulation (case E), the thermal resistance can be only $0.072x10^4$ (K/W). The thermal performance of Cu-encapsulated NW with ALD interconnects (20nm each in case E) is even two times better than that in the conventional planar configuration (case A). However, top length of the nanowire cannot be encapsulated with

electrically conductive copper in order to interconnect metal layer along the as-grown NW. For example, top 1um length of the NW is encapsulated with BCB for the interconnect process, and the rest is used for the device active region that generates heat. With three ALD interconnects (two 50nm Al_2O_3 and one 40nm tungsten) and full copper encapsulation on the device active region, the thermal resistance can be 0.144×10^4 (K/W), as listed in case F. By filling high thermal conductivity materials directly on a hot source (device active region), the temperature difference between the junction and substrate can be substantially reduced. The overall device performance and efficiency can be enhanced while the device is operating at low-junction temperatures by the direct access to cool the active power dissipation region of vertical NW devices [44].

Table 1: Numerical simulation results to study thermal management issue in packaging as-grown NW configurations.

Simulation case	Cross-sectional Schematic drawing (not to scale)	Thermal resistance ($x10^4$, K/W)		Temperature difference (°C) Power: 1mW
A. Heat source on GaN substrate (K_{GaN}=130 W/mK)	Heat flux source GaN	0.18		1.8
B. GaN NW on silicon substrate ($K_{GaN\ NW}$= $K_{Silicon}$=130 W/mK)	GaN NW heat source Si	48		480
C. BCB-encapsulated NW (K_{BCB}=0.29 W/mK)	BCB Si	22		220
D. Cu-encapsulatd NW without ALD interconnects (K_{Cu}=390 W/mK)	Cu Si	0.053		0.53
E. Cu-encapsulated NW with two interconnects (one Al_2O_3 and one W) (K_{Al2O3}=25, K_W= 174 W/mK)	2 Interconnects Cu Si	10nm each	0.063	0.63
		20nm each	0.072	0.72
F. Copper-encapsulated NW with three interconnects (two 50nm Al_2O_3 and one 40nm W) (top 1um of NW encapsulated with BCB for interconnect)	BCB 3 Interconnects Cu Si	0.144		1.44

1.6 Research Objectives

To employ as-grown NWs in future applications, interconnect and packaging technologies must be developed. Specific research objectives and contributions of this thesis are (Fig. 1.5):

1) A generic process to interconnect and encapsulate as-grown NWs by using ALD technology has been developed. The ALD-tungsten metallization on GaN nanowire (5-10um in length, 80-200nm in diameter) arrays encapsulated with BCB is successfully

interconnected to the top electrode. As-grown GaN NW array is interconnected with the tip covered and exposed, which can be used in different applications such as FETs and LEDs.

2) The connection of ALD-tungsten interconnect along NWs is verified by photoluminescence (PL) measurement. PL wavelengths of the nanowire array can be tuned dynamically by changing the input current supplied to the ALD-tungsten interconnect, which heats the NWs. With the NW interconnected with the tip exposed, temperature dependence of PL peak wavelength measured at the nanowire tips can be used for NW tip temperature characterization.

3) An effective cooling solution for as-grown NW thermal management has been designed and fabricated. Copper electroplating for fabricating a cooling structure has been successfully integrated into the interconnect process. The fabrication results led us to the conclusion that the top 1um of the nanowire is used for the interconnect process and the rest is used for the device active region. With electroplated copper (thermal conductivity ~ 360 W/mK) fabricated on the active region of as-grown NWs as a direct cooling structure, 52x thermal resistance reduction can be achieved compared with start-of-the-art structure using spin-on-glass or polymer (thermal conductivity is around 1 W/mK) encapsulation.

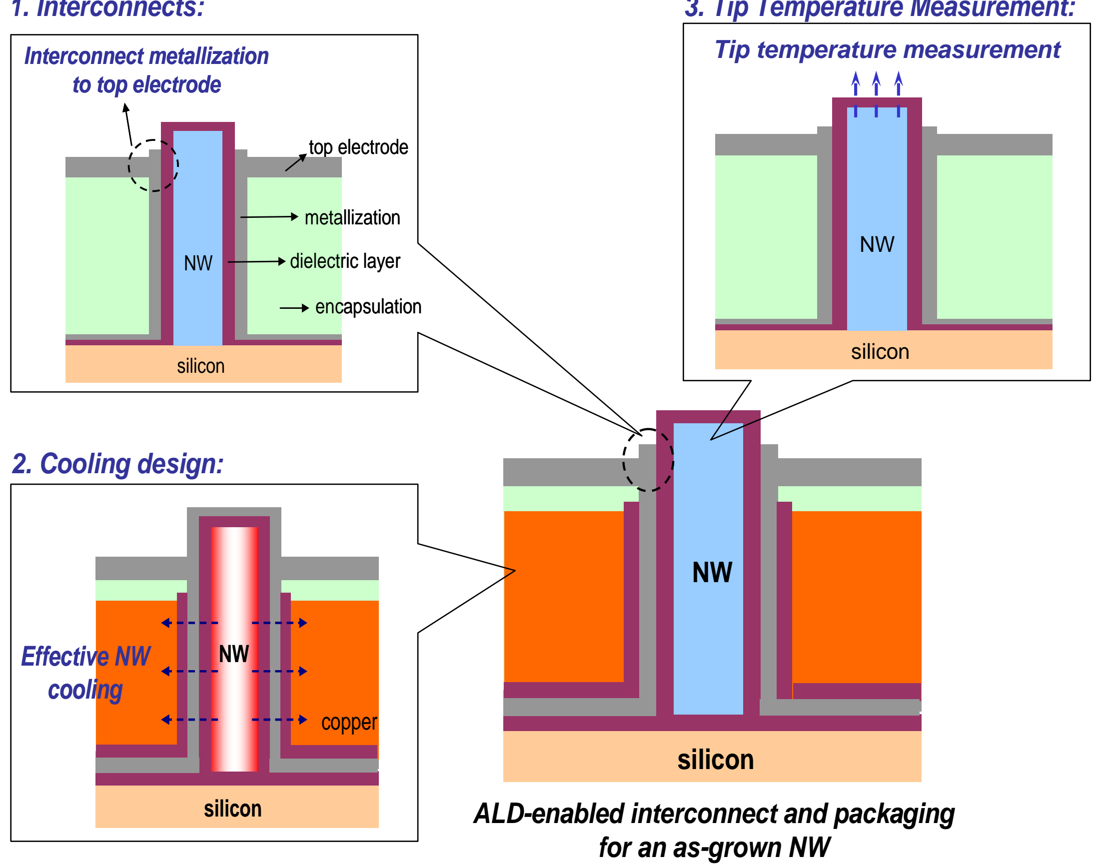


Fig. 1.5: As-grown nanowire (1) interconnected with ALD multilayer, (2) encapsulated with electroplated copper for effective heat spreading, and (3) interconnected with the tip exposed for tip temperature measurement.

1.7 Organization of Dissertation

This dissertation is divided into four chapters. The first chapter gives an overview of NWs, including device applications, device configurations, device interconnect, and packaging. According to the challenges and needs defined in the literature, the research objectives are described in this chapter. In Chapter 2, we report the details of interconnect technology developed in this dissertation in terms of design, fabrication, and characterization. Chapter 3

focuses on the thermal management issue in packaging of as-grown nanowire devices. Thermal design, performance simulation, and device fabrication are presented in detail. Finally, the last chapter summarizes the achievements and contributions of this research and offers recommendations for future study.

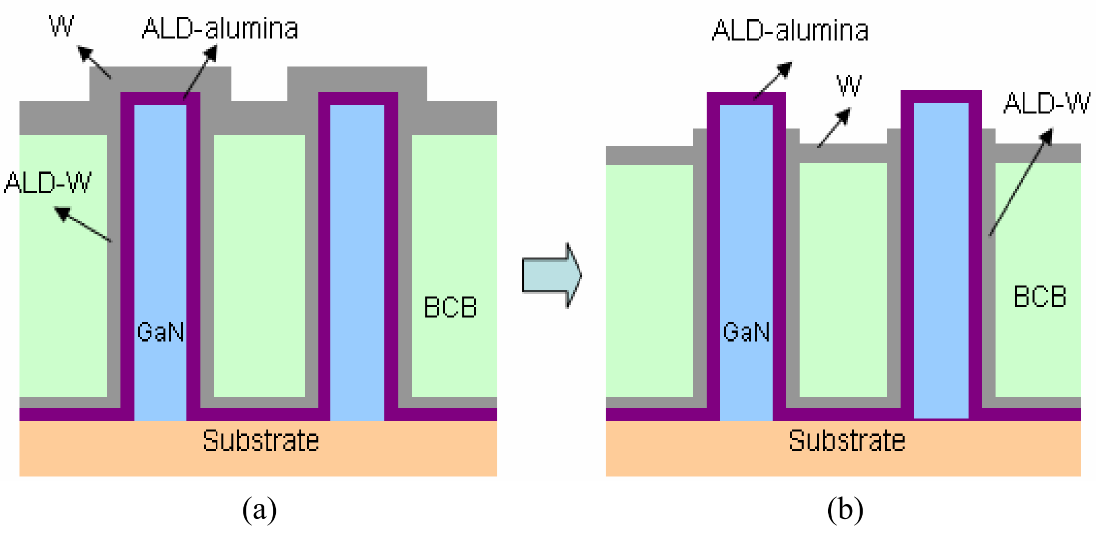
Chapter 2. Interconnect of As-Grown Nanowires

In this chapter, we present a new interconnect technology for as-grown NW arrays with a novel nanoscaled conductor/dielectric multilayer fabricated using ALD. As-grown GaN NW arrays (NW, 5-10um in length, 80-200nm in diameter) are interconnected with the tip covered or exposed for different applications. BCB is used as the filling material to encapsulate the NWs and, most importantly, as the etching mask for local removal of tungsten interconnect on the NWs. PL measurement is conducted to verify the interconnection, and the results demonstrate the dynamic wavelength tuning of GaN NWs by heating the NWs via input current supplied to the ALD-tungsten interconnect. In addition, the GaN matrix effect on the PL measurement has been studied and successfully eliminated.

2.1 Introduction

Low-dimensional nanowire materials are promising fundamental building blocks for future applications, as we have discussed in Chapter 1. Studies have been performed on interconnect and integration of as-grown NWs [16,39-41]. Usually, NWs are parts of interconnects, and electrodes are formed on top and bottom of NWs. For as-grown NW-based LEDs, FETs, sensors, or batteries, device performance could be significantly enhanced through the utilization of the large surface-to-volume ratio of as-grown NWs while coated with high-quality electrical and dielectric interconnects. It is a challenge to interconnect these vertical/as-grown NWs because of their small diameters, extremely high aspect ratios, and random distributions on the substrate. For certain applications, to locally remove and connect interconnects on as-grown NWs is another challenge.

To meet these needs and challenges, our study develops a novel interconnect technology for as-grown NW arrays with not only the utilization of surface of NWs but also the capability of local removal of metallization on the NW. As shown in Fig. 2.1, the surface of the NW is coated with a novel nanoscaled conductor/dielectric multilayer fabricated by the ALD process and is interconnected to a top electrode. NWs can be interconnected with the tip covered with ALD-W metallization as the electrode for such applications as FETs (Fig. 2-1(a)). For such applications as LEDs, the NW can be interconnected with the tip exposed (without W metallization, as shown in Fig. 2.1b).



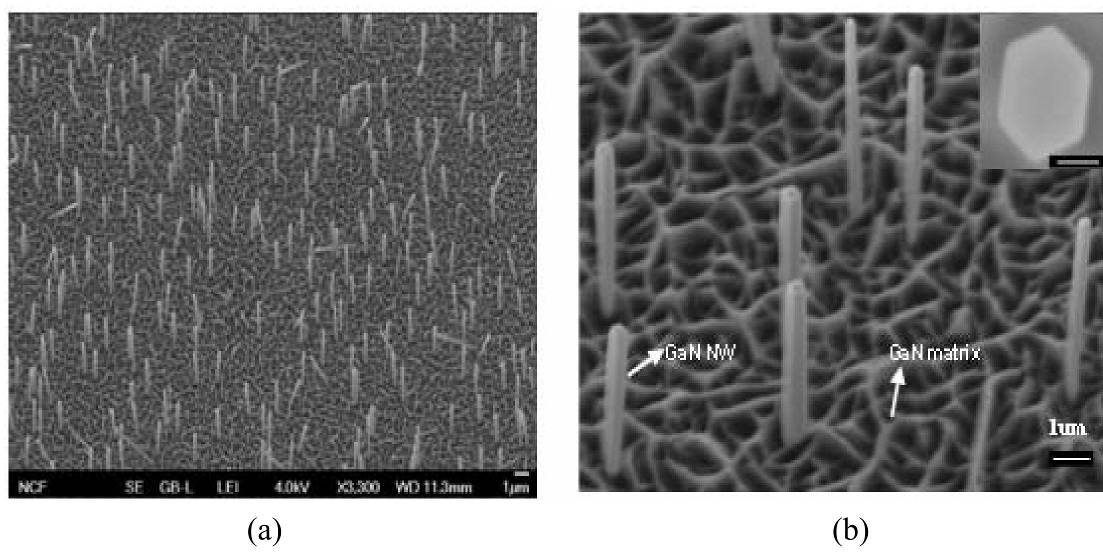
(a) (b)

Fig. 2.1: Schematic drawing of (a) NWs interconnected with tips covered, and (b) NWs interconnected with tips exposed.

2.2 Nanowires Interconnected with Tips Covered

Fig. 2.2 shows the c-axis-oriented GaN NWs as a mechanical platform used for interconnect and packaging in this study. Wires were grown on Si (111) in an entirely catalyst-free fashion using nitrogen-plasma-enhanced molecular beam epitaxy (MBE); the detailed

synthesis technique could be found in references [35,45]. NWs were grown above the GaN matrix on Si substrate (Fig. 2.2b), and these wires were randomly distributed on substrate with a typical diameter of 150nm and length of 8um by field-emission scanning microscopy (FESEM) examination.



(a) (b)

Fig. 2.2: FESEM image of c-axis-oriented GaN NWs. NWs, 5-10μm in length and 80-200nm in diameter, were grown on silicon (111) by nitrogen plasma enhanced MBE [35,45]. The faceted GaN matrix is visible in the image. Inset: top view of single NW (Scale bar: 100nm).

We then employed ALD processes to deposit dielectric and metallic interconnects on GaN NWs. ALD is a low-temperature (for example, 120°C for Al_2O_3 and W film growth) thin film growth technique allowing atomic-scale thickness control. ALD utilizes a binary reaction sequence of self-limiting chemical reactions between gas phase precursor molecules and a solid surface. Films deposited by ALD are extremely smooth, pinhole-free, and conformal to the underlying substrate surface. This conformality enables successful uniform coating of the entire high-aspect-ratio nanowire device. Furthermore, ALD is a low-temperature process enabling

deposition on thermally sensitive materials.

ALD-Al_2O_3 (30nm) and ALD-W (40nm), which serve as a dielectric layer and an electrical connection layer, respectively, were sequentially deposited on the surface of the NWs. The conformality of ALD-Al_2O_3 coating was verified by FESEM, as shown in Fig. 2.3, from side view and top view (inset). Fig. 2.4 shows the FESEM images of tungsten layers (deposited by ALD and sputtering) and placed on top of the ALD-Al_2O_3 layer. Apparently, ALD deposition provides a more conformal tungsten coating (Fig. 2.4a) compared with sputtered W (Fig. 2.4b).

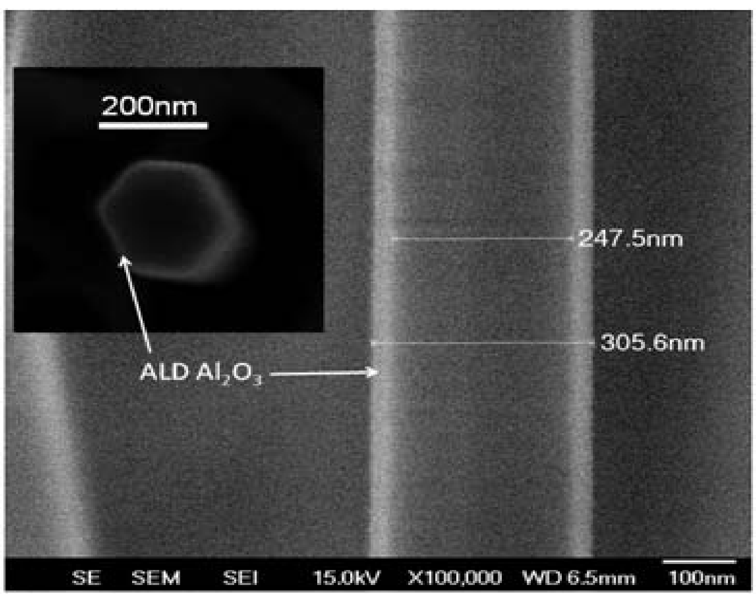
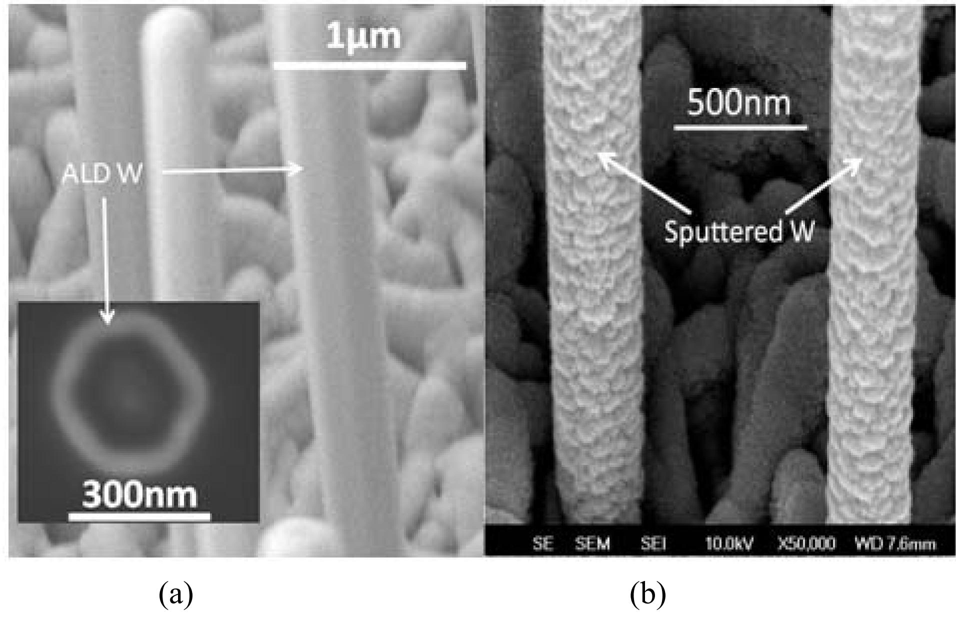


Fig. 2.3: Cross-sectional and top view (inset) SEM images of ALD-Al_2O_3 layer (30nm, shell) on GaN NW (core). Conformal Al_2O_3 (30nm) was deposited on the surface of NWs as a dielectric layer using atomic layer deposition. Scale bar: 100nm.

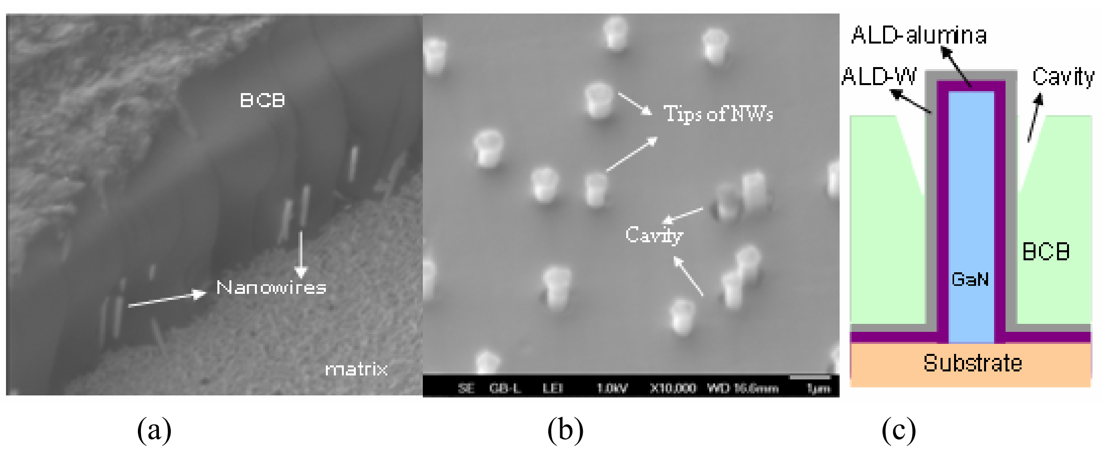


(a) (b)

Fig. 2.4: Tungsten (W) layers deposited on GaN NWs by different coating methods (a) ALD-W (inset: white shell) and (b) Sputtered-W. Compared with sputtered W, ALD-W is much smoother and more conformal to the surface of NWs with a high aspect ratio (5-10um in length and 80-200nm in diameter). ALD-W layer is used as a metal interconnect for as-grown GaN NWs.

A polymer encapsulation process for the interconnected as-grown NW devices has also been developed. This encapsulation process was needed to finalize the interconnect of the devices coated with the ALD conductor/dielectric multilayer and to provide a robust mechanical support. In this study, we selected Benzocyclobutene (BCB) as the filling material to encapsulate as-grown NWs. BCB has been widely adopted in a variety of electronic applications, including silicon and compound semiconductor passivation, interlayer dielectric, flat panel display, IC packaging, integrated passives, MEMS, wafer bonding and 3D integration, and optoelectronic components due to the favorable material properties of BCB such as low dielectric constant (2.65) and low dissipation factor (0.0008) [46-48]. Several droplets of BCB were dripped on the NWs chip, soft-baked at 90˚C for 4 minutes, exposed to UV, and then hard-baked at 250˚C for 1

hour. Fig. 2.5a shows the FESEM image of NWs buried in thick BCB. To expose the tips of the NWs, mechanical polishing was first employed to reduce the thickness of BCB, and then plasma reactive ion etching (RIE) was used for selective BCB etching. Our study uses gas ratio (O_2 : CF_4 = 6 sccm: 4 sccm) in RIE, and this recipe gives us BCB etching rate of 0.5um/min. The effects on BCB etching rate and flatness of RIE etching recipes have been studied in literature [49-52]. Fig. 2.5b shows the exposed NW tips. However, as shown in Fig. 2.5b and 2.5c, the polishing process could result in NW tip damage, as well as in residual voids and cavities between BCB and the NWs. Such cavities may electrically isolate the NW tip from the top conducting surface.

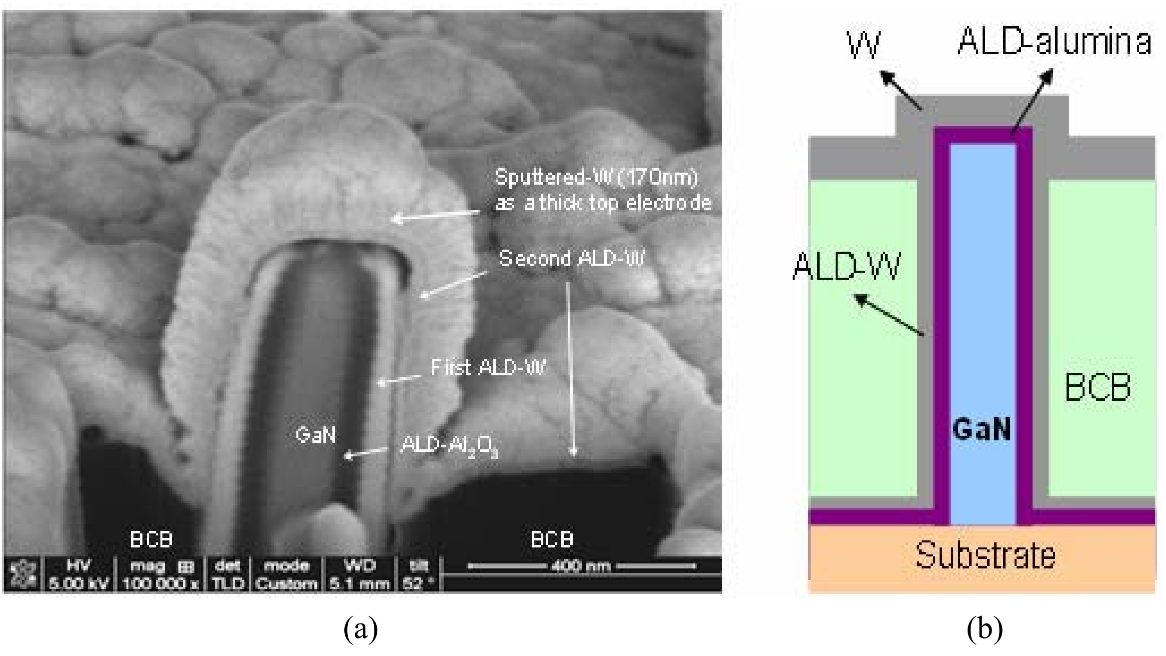


(a) (b) (c)

Fig. 2.5: BCB encapsulation process for as-grown GaN NWs. (a) GaN NWs were buried in thick BCB by dripping. (b) Mechanical polishing was employed to reduce thickness of BCB, and tips of NWs were then exposed after RIE process. (c) Schematic drawing of cavity shown in (b). Scale bar in (b):1um.

To eliminate these cavities, a second ALD-W (30nm) coating was introduced to ensure a conformal conductor coating that would cover every NW tip even down and into the cavities. This ALD conductor coating is followed by a thick top W electrode, which is deposited by sputtering with a thickness of 170nm. As a result, a continuous electrical interconnection from

the top tips of the NWs through the surface of the NWs to the bottom substrate is formed. The top electrode can be patterned to interconnect a specific number of NWs. This ALD-enabled interconnection scheme is of critical importance for the development of as-grown FETs. In other potential applications of nanowire structures, such as supercapacitors, the ALD-alumina dielectric layer may also play an important role. Fig. 2.6 reveals the detail of the layer-by-layer structure using FIB cross-sectional cutting. The conformal ALD-Al_2O_3 / ALD-W layers on the NWs and the second ALD-W layer to fill the voids/cavities described earlier are shown in the figure.



(a) (b)

Fig. 2.6: (a) Cross-sectional view of NW with ALD layers after FIB cutting. Scale bar: 400nm. (b) The corresponding schematic drawing. The second ALD-W was deposited for conformal coverage in the cavities. Sputtered-W with a thickness of 170nm was deposited after the second ALD as a thick top electrode.

2.3 Nanowires Interconnected with Tips Exposed

For as-grown NW-based LEDs or lasers, tip regions of NWs are the passages of light output. Light output could be blocked by the design of a whole surface of metal interconnect on top of encapsulation material and NWs. Apparently, a local interconnect process to connect NW-based devices is essential to many other practical applications. To demonstrate the capability of fabricating specific NW-based device configurations by using ALD-enabled interconnects, we have successfully developed a fabrication process to locally remove the metal layer at the tip region of NWs. With the local interconnect process, ALD-W could provide current injections on NW-based devices while ALD-W at NW tip region is locally removed. These nanowire array devices could then be tested electro-optically, as described in section 2.4.

The goal of the local interconnect process is to remove the W metallization layer from the tips of NWs. Fig. 2.7 shows the detailed schematic process flow and the corresponding experimental results. No photolithography mask is needed in this process. The process starts with as-grown GaN NWs (Fig. 2.7a) coated with ALD-Al_2O_3 and W (Fig. 2.7b). Fig. 2.7b shows a cross-sectional image of ALD-Al_2O_3 and W on a NW. SEM image was taken at the edge of a NW chip cut from a NW wafer. The NW was broken due to the cutting force. Again, Al_2O_3 and W grown by the ALD method are conformal. To improve the wettability of NW surfaces, oxygen plasma treatment of 20 seconds was conducted before BCB spin-coating on the NW sample. Next, tips of NWs were exposed by selective RIE etching (Fig. 2.7c), and ALD-W at the tips was removed by W-etchant. ALD-Al_2O_3 is a good passivation layer and can sustain W-etching process. By controlling the etching time, the length of W removal at the tips can be controlled. We observed local W removal at the tips after further BCB etching by RIE (Fig.

2.7d). The top W interconnect was made by first a thin ALD-W layer (36nm), for making sure that all NWs are covered and interconnected, and then a thick sputtered-W layer (110nm) (Fig. 2.7e). Then, BCB was spun on the sample again. The tips of the NWs were exposed by RIE, and W (ALD-W and sputtered-W) at the tips was removed by W-etchant (Fig. 2.7f). The etching time is critical not only to control the length of W interconnect at the tip to be removed but also not to cut off the top interconnect between the NWs. Finally, BCB was removed by RIE, as shown in Fig. 2.8. The ALD-W on NWs are electrically interconnected, and W at the tips is removed (Fig. 2.8). In the local interconnect process, BCB was spun on the NW sample, not by dripping. Thick BCB is not desirable because a mechanical polishing process is required to reduce the thickness of BCB. Using BCB spin-coating, the thickness of BCB can be controlled by the ramping and spinning speed. Thus, polishing process can be eliminated if BCB is thin. Since we have eliminated the mechanical polishing process, we do not need to worry about the possibility of NW damage. Cavity issue can also be improved by oxygen plasma treatment before BCB spin-coating. The detailed step-by-step fabrication procedure is described in Appendix B.

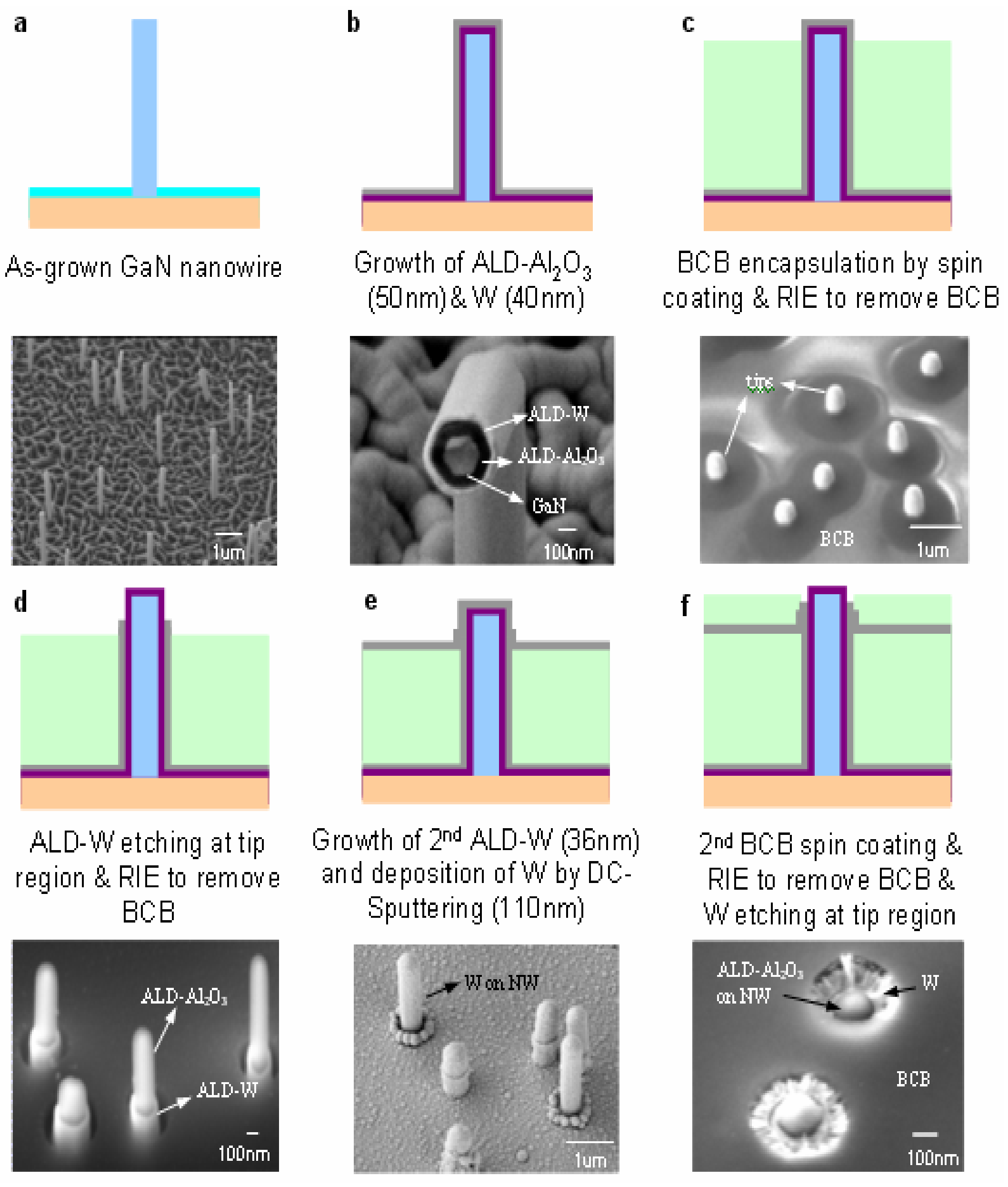


Fig. 2.7: Fabrication process flow and corresponding experimental results of a local interconnect process that results in NWs interconnected with tips exposed (no W-layer on the NW tip).

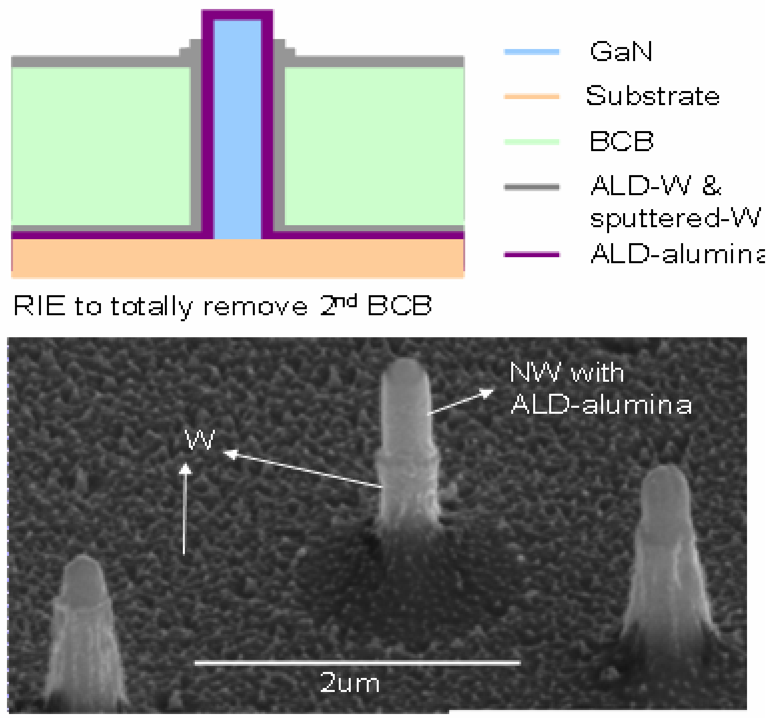


Fig. 2.8: (top) Schematic drawing of the final step of the local interconnect process and (bottom) SEM image of GaN NWs with tips exposed (no W at the tip region) after the local interconnect process.

2.4 Interconnection of Metallization Interconnect

Photoluminescence (PL) system is a non-contact optical tool to characterize the bandgap of semiconductor materials [53-55]. In our study, temperature dependence of PL peak wavelength is employed to verify the connection of metallization interconnect along as-grown NWs. As described by the well-known Varshni expression in Fig. 2.9, the bandgap of semiconductors and its corresponding photoluminescence wavelength changes with temperature [56]. Around room temperature, it exhibits a linear relation. By applying the current into

metallization interconnect that heats the wires, we can observe the PL-to-temperature change and are able to confirm the metallization connection.

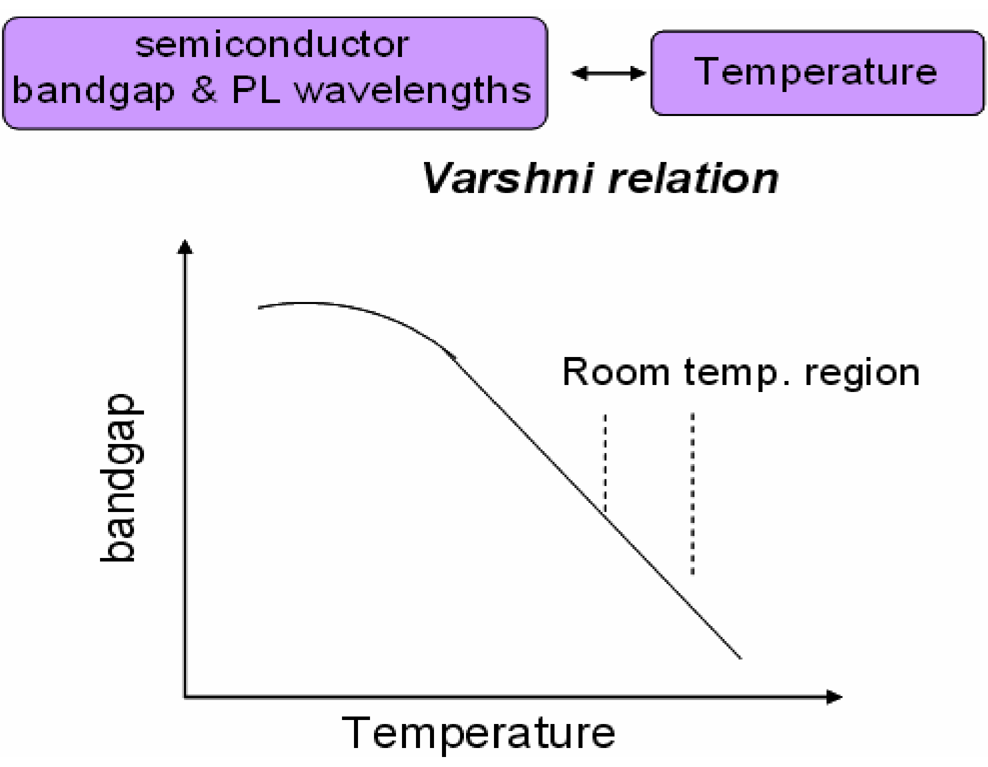


Fig. 2.9: Temperature dependence of GaN bandgap and corresponding PL wavelength.

2.4.1 Temperature Dependence of Photoluminescence Wavelength

In an experiment, we apply current injection into the W metallization interconnect along the NWs and observe the corresponding PL change. The ALD-W interconnect is heated due to joule heating when the current is passed through. As a result, the NWs are heated. When the temperature of a semiconductor increases, the lattice expands and then leads to a change of energy bandgap. PL experiment is used to measure this change and verify the W metallization interconnect along the NWs. The schematic drawing of the experimental setup for steady-state PL measurement is shown in Fig. 2.10. A NW sample (Fig. 2.8) was placed on a thermoelectric

(TE) device and excited with a continuous-wave (CW) HeCd laser operating at 325nm (3.815eV). The TE device, functioning as a heater, can quickly and uniformly heat the NW sample to a specified temperature. Surface temperatures of the TE device were recorded by a K-type thermocouple (TC). We changed the input power of the TE device and recorded PL signals at different surface temperatures of the TE device to obtain the temperature dependence of PL wavelength. Compared with change by TEC heating, the PL change induced by joule heating can be measured only if connection of metallization is connected.

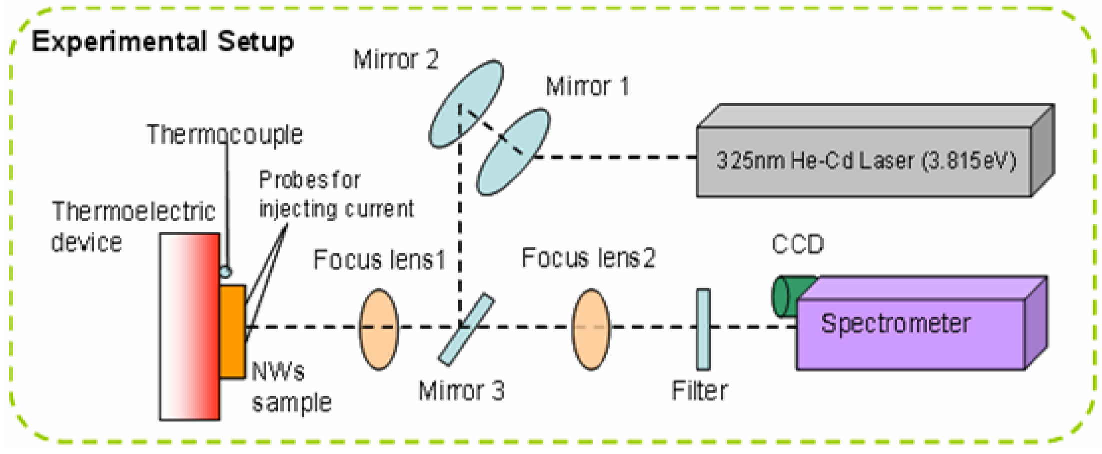


Fig. 2.10: Steady-state PL system used for measuring temperature-dependent PL wavelength

2.4.2 Current Injection through Metallization

To control the current flow in ALD-W on NWs, two metal pads were made by FIB machining as shown in Fig. 2.11. As illustrated in Fig. 2.11 (a), metal pads 1 and 2 were separated by a FIB machined trench but electrically connected through the ALD-W interconnect on the NWs and the NW base region. The electrical path for the current to flow through, as shown in Fig. 2.11 (b), is from the positive electrode (Pad 1) through the ALD-W along the NWs to the W on the base region and back to the negative electrode (Pad 2).

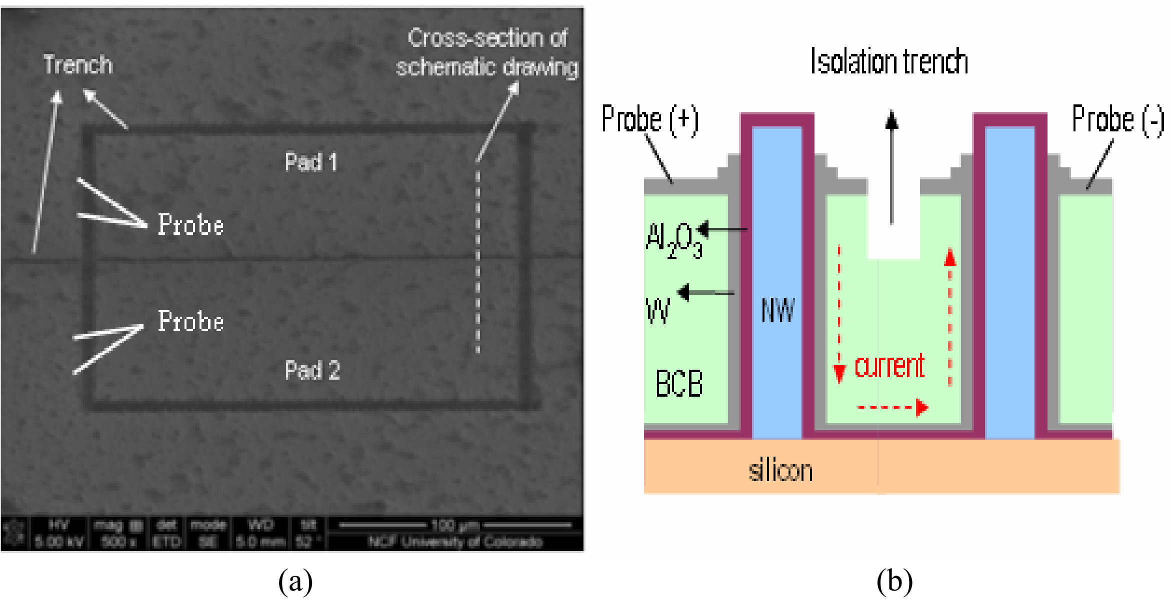


Fig. 2.11: (a) SEM image of trenches fabricated by FIB and (b) schematic drawing of cross-sectional view. Trenches were fabricated by FIB cutting to isolate pad 1 and pad 2. The dimension of each pad is 200um (width) x 100um (length). The depth of the trenches is 3um.

Fig. 2.12 shows the PL measurement results with/without injecting current into the ALD-W interconnect. We first use TEC to heat the NWs and tune the PL wavelength (solid line in blue). This shift can also be achieved by heating the same NW sample via current injection into the ALD-W interconnect as shown in the figure (dash line in red). Red-shifted PL spectrum is observed with power input of 1637mW into the ALD-W interconnect. Bandgap of GaN NW is changed due to the temperature increase by power input into the ALD-W interconnect, thus changing the the PL peak wavelength. The connection of the ALD-W interconnect is verified by PL measurement with injecting current. We also note that there is a slight change of the PL slope for different heating mechanisms (TEC heating or current injection), which could be due to the non-uniformity of the temperature distribution along the NWs.

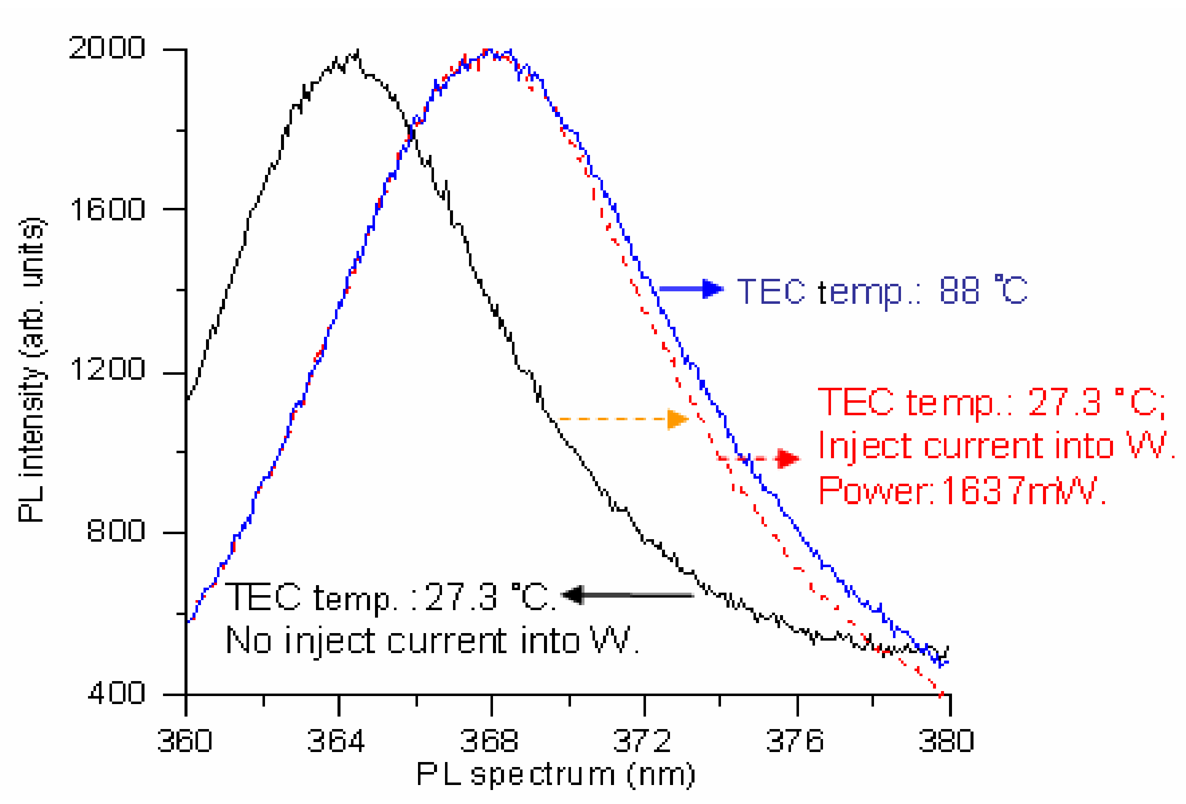


Fig. 2.12: Experimental results of PL tuning by using TEC to heat NWs (solid line in blue) and by injecting current into W interconnect to heat the NWs (dash line in red).

The connection of the W interconnect on the NWs was confirmed by current injection into the W interconnect to tune the PL wavelength. The difference in the PL slope could be due to the non-uniformity of the temperature distribution along the NWs under different heating mechanisms (TEC heating or current injection).

2.5 Tip NW Photoluminescence Measurement

The W metallization interconnect at the tips of NWs was locally removed by the developed interconnection process. However, as-grown GaN NWs were grown above the GaN

matrix on silicon wafer, as shown in Fig. 2.13. Same as GaN NWs, the GaN matrix is also an object that illuminates if irradiated by the laser. It is important to investigate the GaN matrix effect on the PL measurement and eventually verify the location of the PL measured.

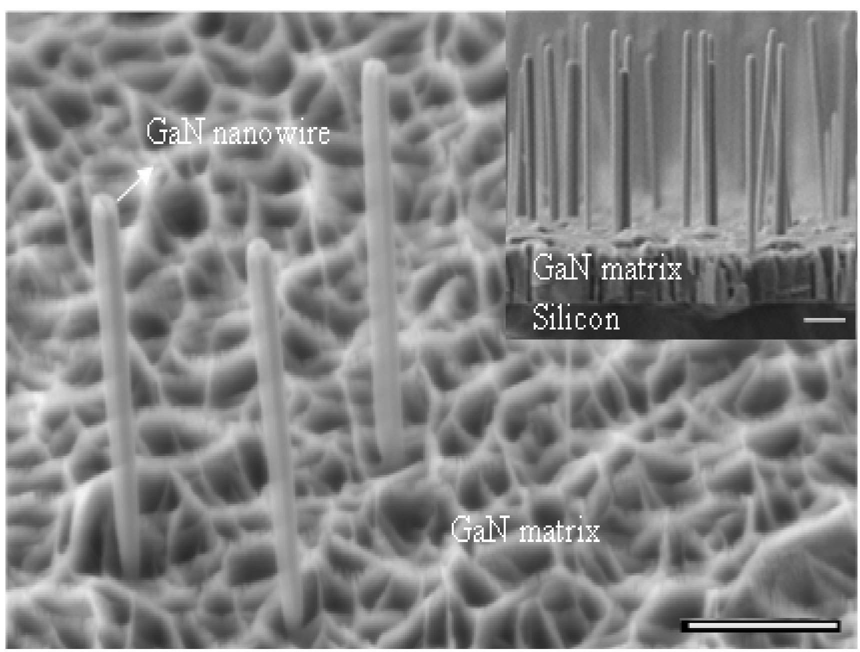


Fig. 2.13: c-axis-oriented GaN nanowire array grown by catalyst-free MBE on silicon (111), inset: cross-sectional view of NW array. Scale bar: 1um for both.

2.5.1 The Effect of Substrates and Matrixes

To investigate the GaN matric effect, we have measured the temperature dependence of the PL peak wavelength from different NW samples: (1) ALD alumina-coated GaN NWs on alumina-coated matrix, and (2) ALD alumina-coated GaN matrix (no NWs). The GaN matrix-only sample was prepared by soaking the NW sample in a container with isopropanol. The GaN NWs were then removed from the as-grown substrates by agitation in an ultrasonic bath. The thickness of ALD-alumina for both samples is 50nm grown at 120 ºC. Both NW samples were

placed on a TE device and excited with a CW HeCd laser operating at 325nm (3.815eV) in the setup of Fig. 2.10. Same as the procedure described in 2.4.1, we changed the input power of the TE device and recorded PL signals at different surface temperatures of the TE device to obtain the temperature dependence of PL peak wavelength from both samples. A quadratic fit using data close to the raw peak was chosen to determine the peak PL wavelengths. This method gives less uncertainty and better temperature-to-wavelength sensitivity than simply using the peak PL wavelength or using mean values. Temperature-to-wavelength sensitivity using different methods to determine the PL peak wavelength is discussed in Appendix C. At one TEC temperature condition, we record six measurements. The HeCd laser spot diameter is around 13um, and the average number of NWs shined by the laser is 10 by FESEM examination.

Fig. 2.14 shows the temperature dependence of PL peak wavelength measured from both samples. PL measurements on both samples follow a linear relation as expected since the temperature dependence of the semiconductor energy bandgap is linear. The temperature dependence of PL peak wavelength measured from GaN matrix-only sample with ALD-alumina (star in blue) had the same relation as those of ALD-alumina coated NWs and the matrix sample (square in orange). Comparing the results of both samples, we found out that the majority of luminescence was from matrix area, not from NWs, when NW samples were shined by the laser. The surface area of silicon wafer, as observed in Fig. 2.13, is mostly occupied by the faceted GaN matrix layer, not by GaN NWs growing out of the matrix layer.

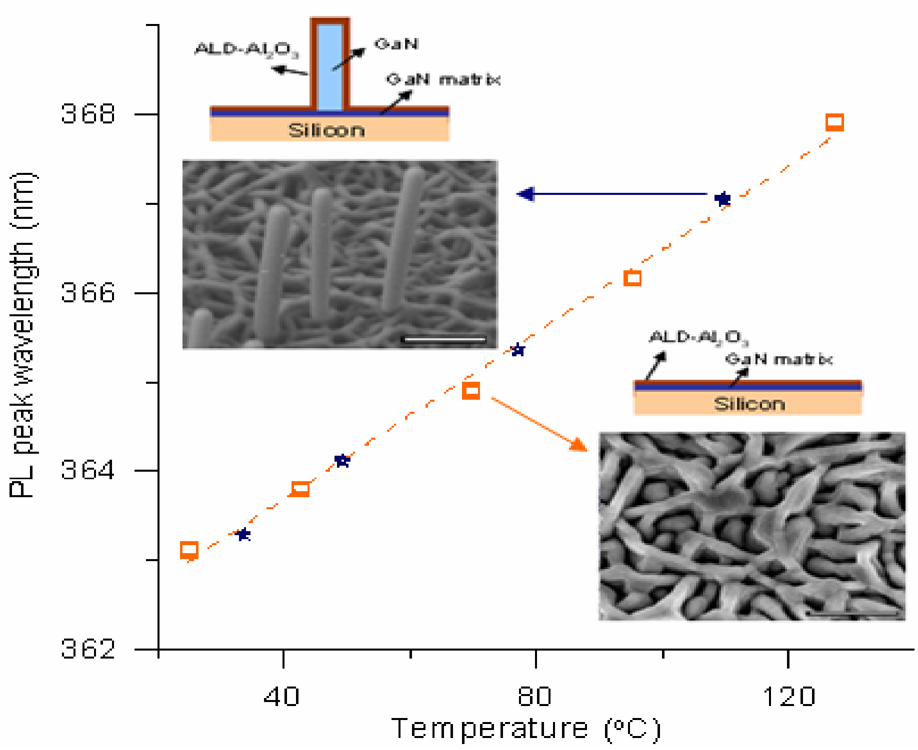
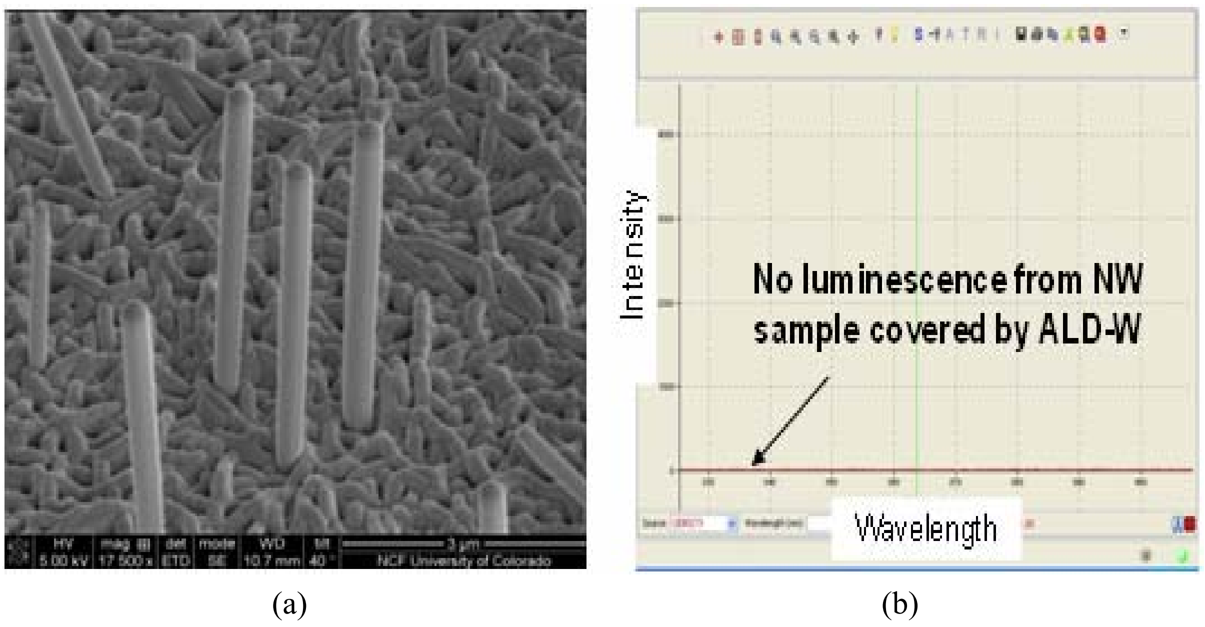


Fig. 2.14: PL measurements on alumina-coated GaN NWs on alumina-coated matrix (square in orange), and alumina-coated GaN matrix (star in blue). The thickness of ALD-alumina is 50nm, and the growth temperature is 120 ºC.

2.5.2 Fabrication Processes for NW-only PL Measurements

To successfully measure the PL signal from as-grown GaN NWs, we have to eliminate luminescence from the GaN matrix excited by the HeCd laser. However, distinguishing measurement signals originated from the growth substrate or matrix layer in as-grown NWs is a challenge because of the nanoscaled dimension and as-grown configuration. The NW sample (NWs on matrix with a 50nm ALD-alumina) was further deposited with a 40nm-thick ALD-W as shown in Fig. 2.15 (a). With full coverage of ALD-W on GaN NWs and GaN matrix layer, no PL light was generated from the PL measurement as the HeCd laser was reflected and blocked

(Fig. 2.15(b)). Apparently, metal layers can totally block the HeCd laser to prevent luminescence from underlying the GaN structures.



(a) (b)

Fig. 2.15: (a) NWs coated with 40nm-thick ALD-tungsten. (b) No luminescence observed from the PL measurement on W-coated as-grown NWs.

To measure the PL signals from NW-only, as-grown NWs had to be exposed from ALD-W layer. With developed selective removal of ALD-tungsten surrounding the tips of NWs, we were able to measure the PL from the NWs only. The detailed schematic drawings and corresponding experimental results of selective removal of ALD-tungsten at tips are illustrated as shown in Fig. 2.16. First, ALD-alumina (50nm) and ALD-tungsten (40nm) were sequentially deposited on as-grown NW sample (Fig. 2.16a). Next, the NWs were fully encapsulated with BCB using spin-coating (Fig. 2.16b). Before the spin-coating process, oxygen plasma treatment of 20 seconds was used to improve the wettability of the NW surface. The tips of the NWs were exposed by selective BCB etching using oxygen RIE (Fig. 2.16c). When the tips were exposed,

the ALD-tungsten at the tip region was removed by W wet etching process. The etching process etched the ALD-tungsten at the tip region only, and the exposed length at the tips could be controlled by etching time. The ALD-alumina still remained on the NWs (Fig. 2.16d). Finally, BCB was partially (Fig. 2.16e) removed and largely (Fig. 2.16f) removed by RIE.

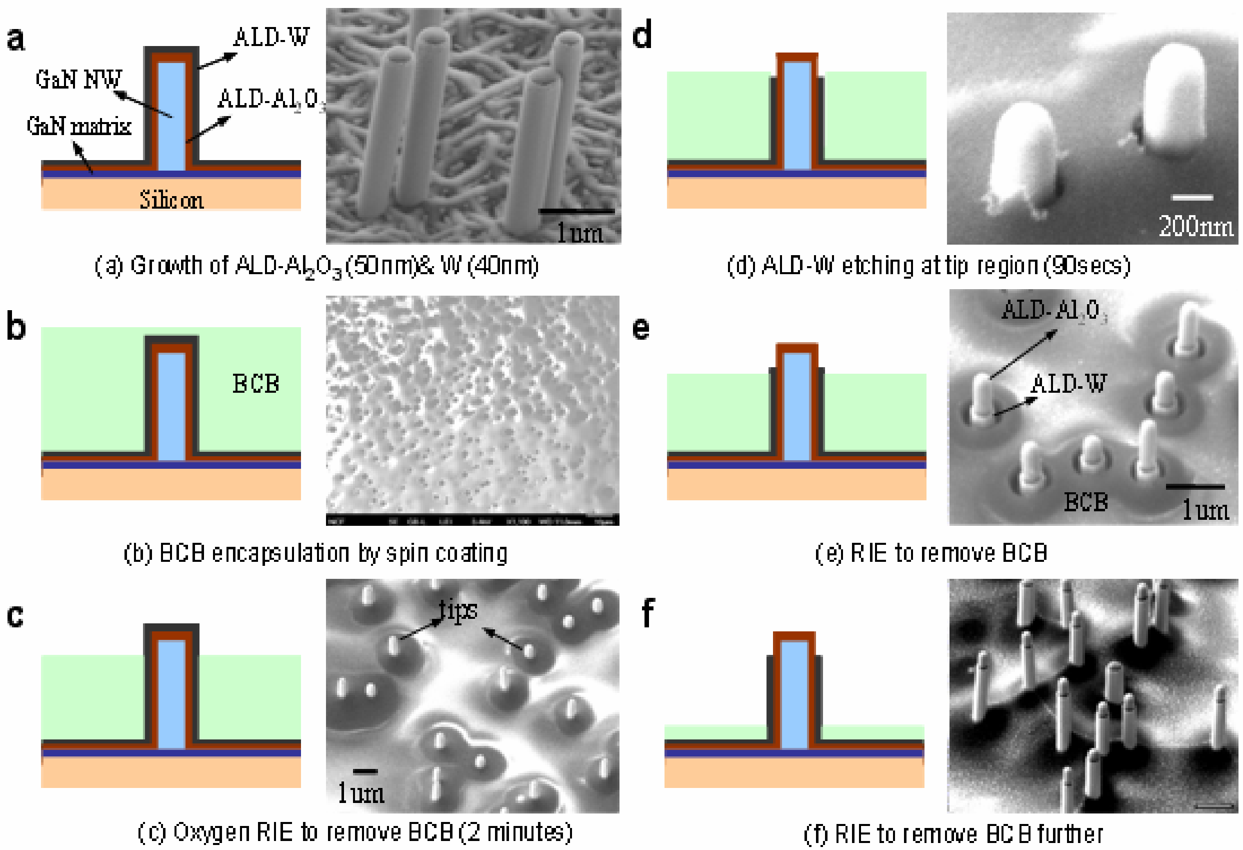


Fig. 2.16: The schematic drawings and corresponding experimental results of the selective removal of tungsten at the tips.

2.5.3 Tip NW Photoluminescence Measurement

Fig. 2.17 shows the PL measurement results on ALD-W coated NWs without W at the tips. We observed a blue shift in the PL peak spectrum between the PL measurement on GaN

NWs and on the GaN matrix. The intensity at the peak PL wavelength of GaN NWs (peak intensity is 2253 at 23 ºC) was about 15 times smaller than that of the matrix material (the peak intensity is 32324 at 23 ºC). This measurement confirms our previous observation that the majority of luminescence is from the matrix area, not from the NWs, when the NWs and matrix were both shined by the HeCd laser at the same time. The higher PL intensity is measured when the larger surface area of the material is shined by the laser. The slopes of temperature dependences of PL peak wavelength in the two cases are different. The mechanism for the PL shift between the NWs and matrix layer may be caused by the difference of defect structure between the GaN NWs and GaN matrix layer. Compared with GaN NWs, the GaN matrix layer growing at the base of the wires was found to have a high density of basal plane stacking faults [57]. Based on the study on matrix effect and elimination, we confirm that the PL measured on the NW sample interconnected with the tip exposed in Fig. 2.8 is from the tips of the NWs since only the tip regions are without the W layer. The temperature dependence of the PL peak wavelength measured at the tip of NWs can be applied to characterize the tip temperature of as-grown NWs. Using temperature dependence of PL peak wavelength as a calibration curve, we can retract the tip temperature of the NW from corresponding wavelengths. Compared with [58], the tip NW PL measurement without the matrix and substrate effect demonstrates a feasible method to characterize temperature or thermal properties of as-grown NWs directly. Appendix D demonstrates an application of temperature dependence of NW-only PL peak wavelength for NW temperature characterization.

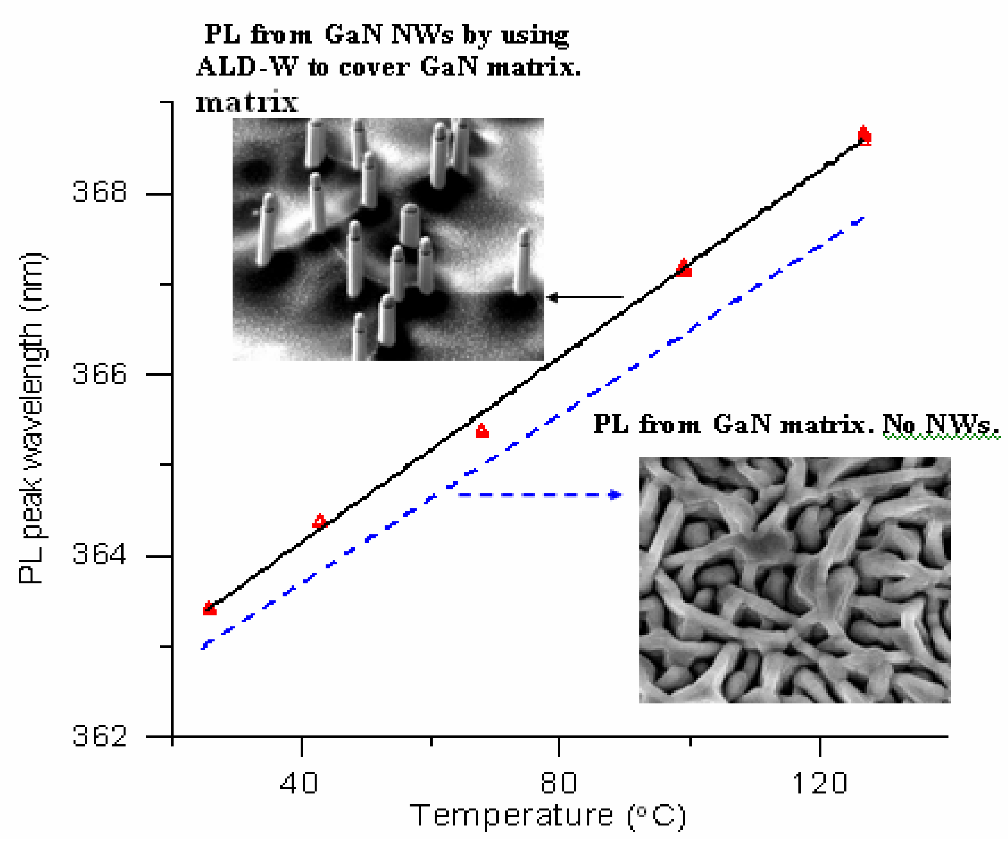


Fig. 2.17: PL measurements on GaN NWs with ALD-W to block the matrix layer (fitted line in black) and GaN matrix layer (fitted dash line in blue).

2.6 Tuning GaN Nanowire Bandgaps by Heating

Wavelength controllability is important for applications of laser and LEDs. Previous studies focused on tuning the NW bandgap by changing material compositions [59,60]. Changing the material properties from the material itself is one way; applying an external pressure, temperature, or electrical field could result in a dynamic tuning of the bandgaps. In our study, we demonstrate the dynamic tuning of GaN nanowire bandgaps by heating the NWs through the ALD-W interconnect. With current injection to the ALD-W interconnect, the connection quality of the ALD-W interconnect along NWs can also be verified by this bandgap-

tuning demonstration. The ALD-W interconnect is locally heated due to joule heating when the current passes through. As a result, the NWs are heated. As the temperature of the semiconductor increases, the lattice expands and then leads to a change of energy bandgap. We used the PL system to characterize the dynamic tuning of the GaN nanowire bandgap. Since W on the tips of NWs was removed by local interconnect process, PL light can be generated and measured from the tips. The PL signals are from the tips of the NWs. Spatially resolved PL measurement has been conducted to verify the tip PL measurement and is described in Appendix E. The PL signals are tuned by changing the power input supplied to ALD-W on NWs. To control the direction of current flow in ALD-W along the surface of NWs, two metal pads were made by FIB machining as shown in Fig. 2.18. Metal pads 1 and 2 are separated by FIB machined trenches but electrically connected through the ALD-W interconnect on NWs and the NW base region.

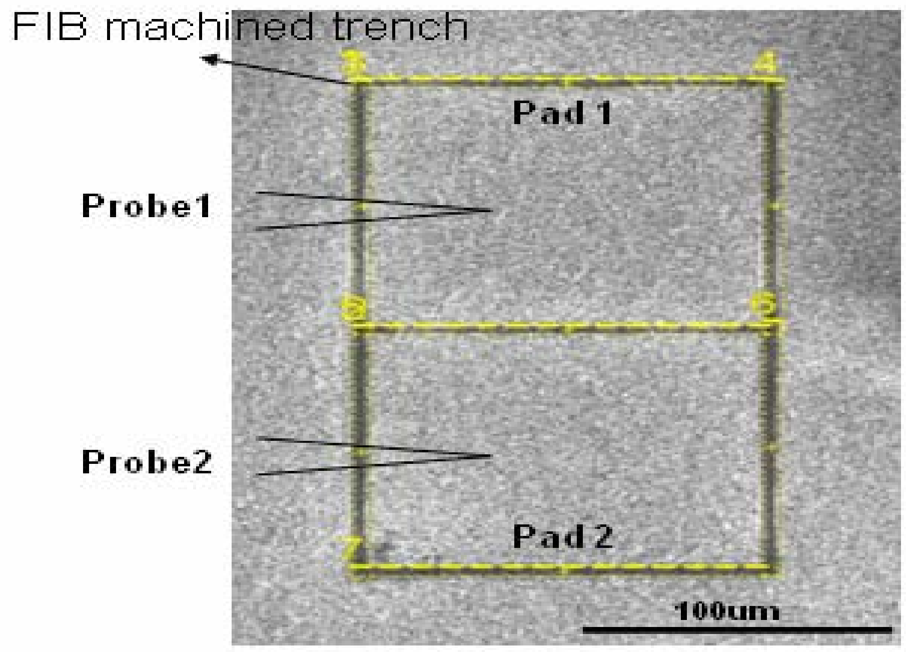


Fig. 2.18: SEM image of NW sample with FIB machined trenches for bandgap-tuning experiment.

PL tuning results are shown in Fig. 2.19. In the experiment, temperature dependence of the PL peak wavelength was first measured. We changed the input power of the TEC and recorded PL signals at different TEC temperatures. There was no power input into the ALD-W interconnect via electrical probes. It should be noted that the PL peak wavelength was determined by using the quadratic fit to the neighboring data of the raw peak. At one TEC temperature condition, we recorded six measurements and made one error bar with one standard deviation. Afterward, we started to inject current into the ALD-W interconnect on NWs via probes and tune the PL peak wavelengths. In Fig. 2.19, two target wavelengths, 368nm and 366.04nm, were chosen when surface temperatures of the TEC were 88 °C and 55.5 °C, respectively. At lower temperature conditions of the TEC (27.3 °C and 38.8 °C), we started to heat the NWs by injecting the current into the ALD-W interconnect on the NWs. By changing the input current supplied to the ALD-W interconnect, the PL peak wavelengths were tuned to our targets. The only flowing path for the injected current was first from pad 1 through the ALD-W interconnect on the NWs to the base region and then back from the base region to pad 2 through the ALD-W interconnect on the NWs. Tunable GaN NWs by heating demonstrates a feasible method to fast tune the bandgap of GaN NWs. This heating effect is also important to NW-based devices with interconnect along the NWs.

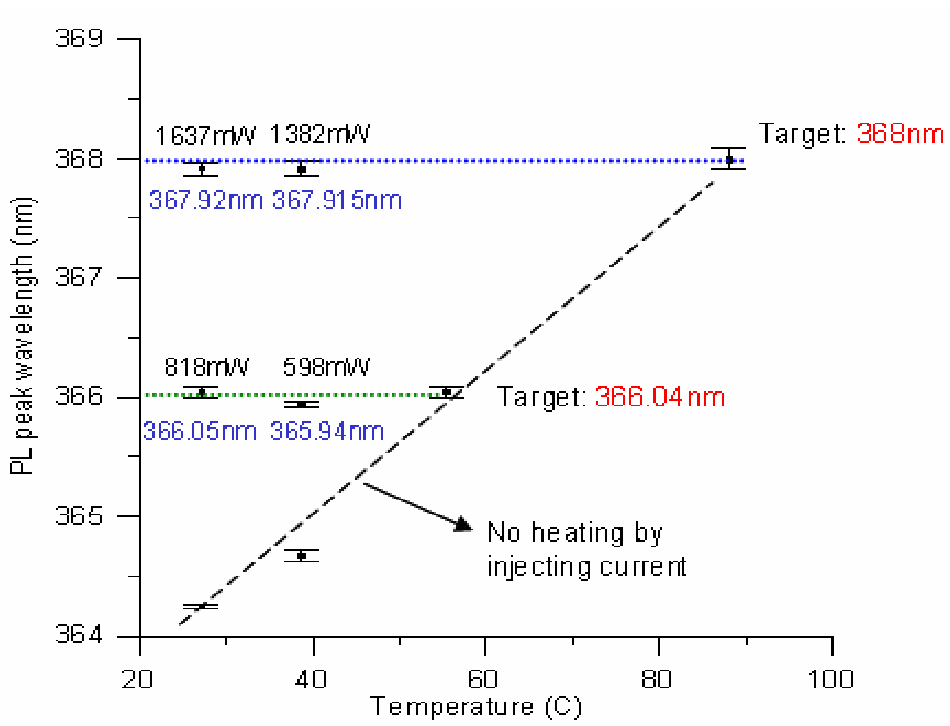


Fig. 2.19: Experimental results of tunable PL wavelength by heating. The PL peak wavelength of a NW array can be dynamically tuned to target wavelengths by changing the input power supplied to the ALD-tungsten interconnect. The PL peak wavelength is determined by using the quadratic fit to the neighboring data of the raw peak.

2.7 Summary and Conclusions

We have demonstrated an ALD-enabled interconnect technology for as-grown nanowire arrays. The nanoscaled conductor/dielectric multilayer is essential to the interconnect technology. FESEM images and cross-sectional image by FIB confirm the conformal ALD-Al_2O_3 and W layer along the GaN NWs with a high aspect ratio. We have also developed a fabrication process to locally remove and connect the W interconnect on NWs. By injecting current into the W interconnect along the NWs in a dynamic PL tuning experiment, we have also

verified the connection of the interconnect on NWs. The effect of the GaN matrix layer has been studied and further eliminated by covering all GaN matrixes with thin atomic-layer-deposited tungsten (ALD-W). The ALD-W at the tips of the NWs was removed by using a maskless ALD-W etching process for tip PL measurements. The interconnect technology can be used in various NW-enabled nanoelectronic and nanophotonic applications.

Chapter 3. Thermal Management of As-Grown Nanowires

Thermal management has become a technical bottleneck in electronic and optoelectronic devices as the need for higher device integration density and power consumption has increased [61-63]. Active devices, such as LEDs or ICs, were fabricated on a substrate by semiconductor manufacturing, and usually thermal engineers were not allowed to design cooling solutions in it. Once the heat has spread from heat dissipation regions to the substrate, a variety of cooling solutions were carefully chosen to conduct the heat from the substrate to the environment and to the next cooling stage. Applying direct cooling to a hot spot or heat source is known to be the most effective cooling solution; however, in current planar device configurations, it is a challenge to apply any cooling solution on hot devices directly.

As discussed in Chapter 1, the use of as-grown NWs gives us an opportunity to cool hot devices directly by filling high thermal conductivity materials between the gaps. The state-of-the-art encapsulation process uses low-thermal-conductivity polymers or silicon dioxide to fill the gaps between the wires, as shown in Table 1. To enhance the thermal performance, the best way is to replace low-thermal-conductivity filling materials with high-thermal-conductivity ones such as copper. This chapter presents an effective thermal design for as-grown NWs and a fabrication process for this design.

3.1 Cooling Design

The interconnect process developed in Chapter 2 uses BCB as the etching mask. Top nanowire length is required for the metallization interconnect process from W along the NW to the top electrode because BCB has to be spun on the NW as the etching mask. With BCB cover over copper surface on the NW, the W metallization layer is able to be connected to the top

electrode and locally removed. Based on the NW device configuration described above, the top nanowire length has to be reserved for BCB for interconnect; the remaining length of the nanowire can thus be used for the active device region (heat source) that generates heat, as shown in Fig. 3.1. With this configuration, there are several challenges in thermal design and fabrication of any proposed cooling solution: (1) Copper has to be deposited as close to the NWs as possible to obtain a short heat conduction path. (2) High copper coverage is needed to fully encapsulate the NW active device for effective cooling. (3) Dielectric and metallic interconnects should be as thin as possible for low interface thermal resistance. (4) Any fabrication process of a copper structure should be compatible with the interconnect process developed in Chapter 2.

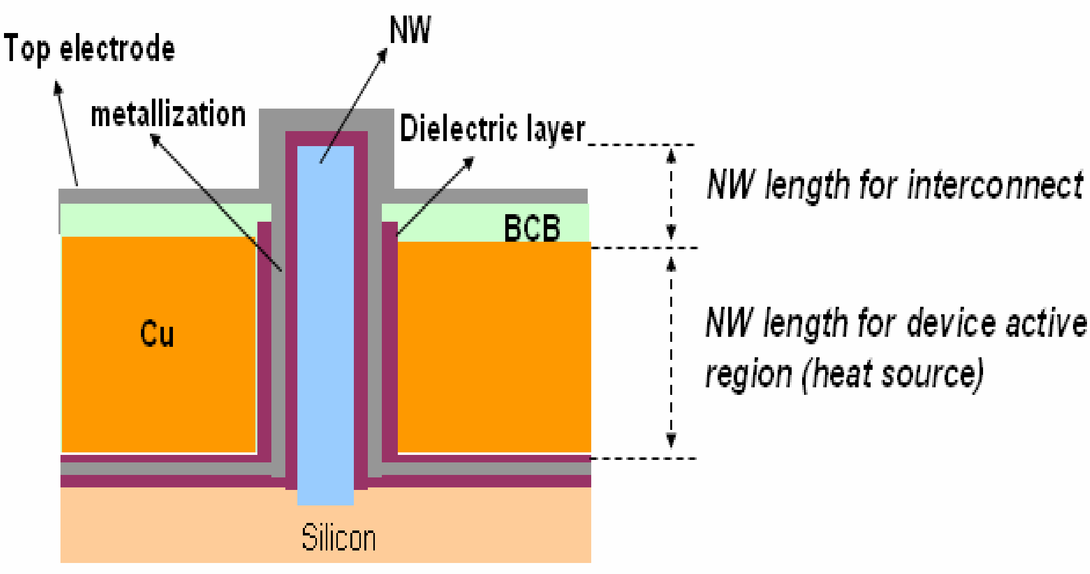


Fig. 3.1: Schematic drawing of as-grown NW interconnect design with the NW tip covered by metallization and encapsulated with copper for effective cooling. For the interconnect purpose, the top length of the NW is coated with BCB as etching mask. The rest of the NW is used for the active device region that generates heat. The active region is encapsulated with copper for effective cooling.

3.2 Cooling Performance

Thermal simulation is used to guide the design and fabrication of a cooling structure for as-grown NWs. The finite-element numerical simulation is conducted to evaluate the thermal performance of an as-grown nanowire encapsulated with different copper-encapsulation widths and lengths, as shown in Fig. 3.2. Thermal resistance is defined as the temperature difference of maximum temperature in the NW (tip NW) to silicon substrate temperature divided by power consumption in the NW. The length of the nanowire in the simulation is 5um, and the whole NW functions as a heat source (in the active device region). We varied the length of copper from 3um to 5um and the width from 50nm to 1000nm to compare the cooling performance. From Fig. 3.2, it is clear that thermal resistance drops substantially with the increase of either copper width or length. Lower thermal resistance can be achieved when a larger surface area of the NW active region is encapsulated with copper for heat spreading. The thermal resistance is reduced to a minimum when the entire active region of the NW is encapsulated with copper (5um active region length of NW by 5um copper).

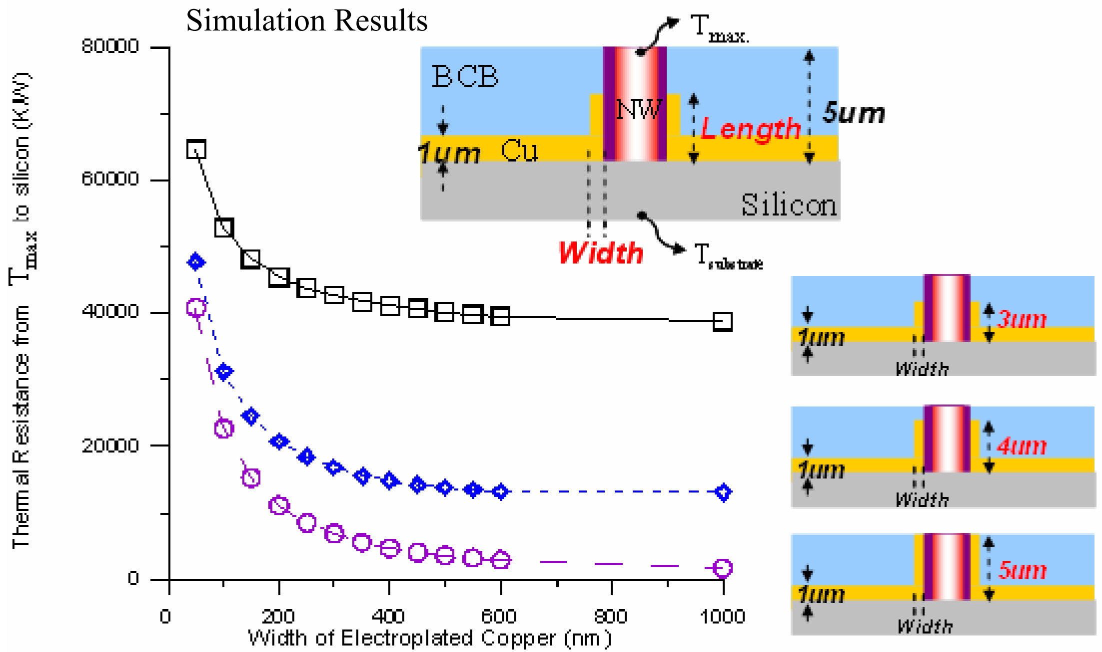


Fig. 3.2: Simulation results of an as-grown NW with different copper coverage levels. The NW length is 5um. The length of copper is varied from 3um to 5um. The width is varied from 50nm to 1000nm. Thermal resistance is defined as temperature difference (tip temperature of the NW to silicon substrate) divided by power.

As-grown NW devices need BCB as an etching mask to interconnect the metallic layer on the NW to the top electrode. To compare the cooling performance with state-of-the-art encapsulation process, such as one using BCB polymer, we assumed that 1um of the NW length is used for the interconnect process, not for the device active region. The rest of the wire is then used for the device active region that generates heat. The thermal resistance can be reduced by 52x if we can replace BCB with copper on the NW active region (Fig. 3.3).

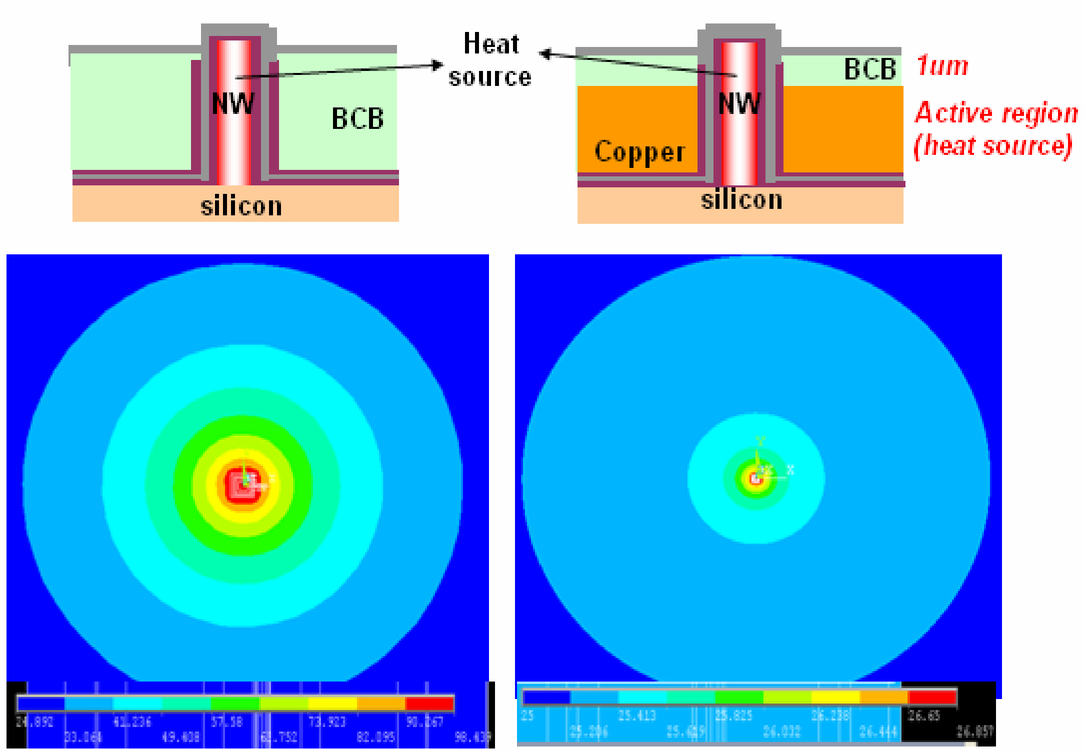


Fig. 3.3: Simulation results of thermal performance of BCB- and copper-encapsulated NWs. The total length of the NW in 5um. 4um of the NW is simulated as a heat source, and 1um of the wire

is used for the interconnect. Thermal resistance of copper-encapsulated NW is 52x smaller than that of the NW with BCB encapsulation.

3.3 Fabrication of Cooling-Enhanced As-Grown Nanowire Devices

Effective cooling design for as-grown NWs is very important in practical applications. Without effective cooling, an as-grown NW device will no longer function reliably over time. However, it is very challenging to apply any conventional cooling solutions to effectively conduct or spread heat from the NW heat source directly because of the nanoscale dimension and extremely high aspect ratio of as-grown NW devices. To overcome the technological bottleneck, the best solution is to design and integrate a cooling mechanism into the device fabrication at the early stage. Likewise, the design and fabrication of an effective cooling structure should be considered and integrated in the device fabrication. For the fabrication of as-grown NW devices, the metallization interconnect is one of the most important processing steps. As a result, the fabrication of the cooling structure should be compatible with the metallization process of as-grown NW devices.

3.3.1 Copper-Encapsulated Nanowires

Conventional semiconductor fabrication processes, such as sputtering, evaporation, or electroplating, can be utilized to fill copper or other metal materials between the NWs. We have evaluated the feasibility of the sputtering process to fill copper between the NWs. Fig. 3.4 shows the FESEM image of NWs covered with copper by DC-sputtering for 1 hour. However, a few fabrication issues arise from using the sputtering process: (1) The first fabrication issue is this process is time-consuming. The deposition rate of sputtering is too low (200 A/minute) to fully

encapsulate as-grown NWs with the average length of 5um. For a length of 5um, it will take at least about 5 hours. (2) It is very difficult to deposit materials uniformly on high-aspect-ratio as-grown NWs by using sputtering or evaporation processes. NWs could not be encapsulated uniformly by sputtered-copper because aspect ratio of NWs (>50 L/D) is extremely high. The thickness deposited at the tip region of a NW is thicker than the thickness in the middle and bottom regions (inset of Fig. 3.4). Copper atoms were bombarded from the sputtered target and most likely coalesced at the tip of the NW because the tip is the location with the smallest mean free path. (3) Air in the voids will significantly lower the thermal performance of a copper structure on as-grown NWs. Voids were formed after copper-sputtering for 1 hour, as shown in the inset of top view in Fig. 3.4.

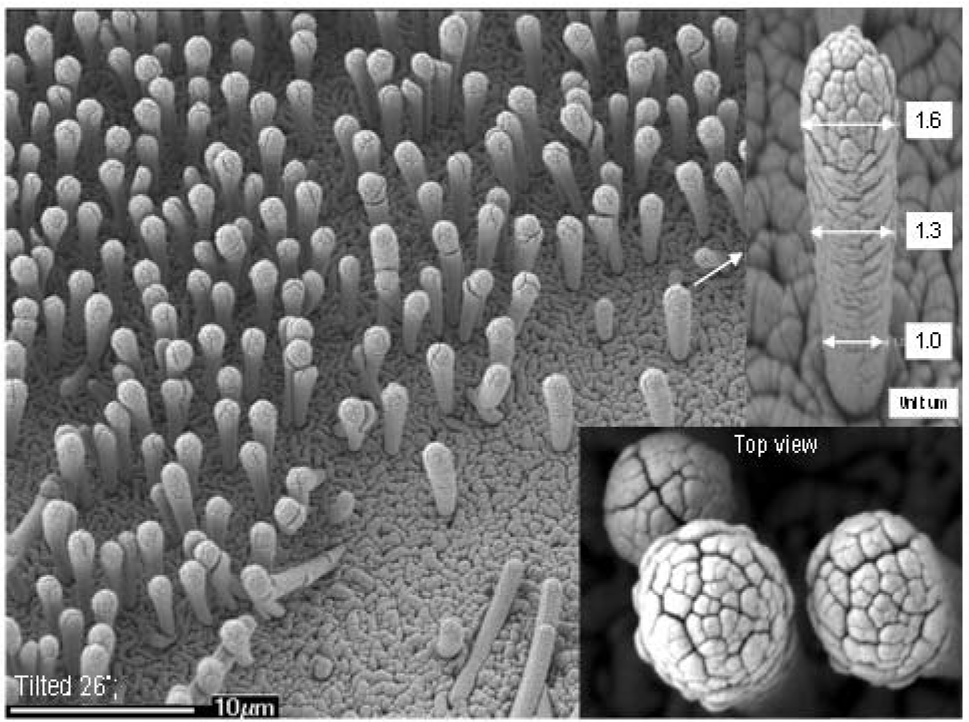


Fig. 3.4: FESEM image of NWs covered with Ti and copper. Ti (~50nm) was deposited by thermal evaporation, and copper (1.2um) was deposited by DC-sputtering. Total sputtering time is 1 hour, and deposition rate is around 200A/minute.

To overcome the fabrication issues in sputtering or evaporation processes, a copper electroplating process is employed to fill the gaps. Copper electroplating is a fast and economic solution for depositing copper material on high-aspect-ratio structures [64-65]. Copper electroplating has been employed in filling gaps between carbon nanofibers for the application of high-performance thermal interface material (TIM) [66]. Nanofibers were fully encapsulated with electroplated copper as a high thermal conductivity filling material for improving the performance of TIM. Copper provides effective lateral heat spreading and improves mechanical reliability. Copper-filled nanofibers demonstrate efficient interfacial thermal conduction. However, for nanowire-based optoelectronic and electronic devices, metallization interconnect along the surface of NWs is required in device fabrication. The copper filling process has to be compatible with the metallization interconnect process.

Our study has developed a maskless interconnection process for as-grown NWs with an effective cooling design by applying electroplated copper directly on NWs as a heat spreading material. This process is compatible with the developed metallization interconnect process described in the previous chapter. Fig. 3.5 shows the detailed fabrication process. It starts with as-grown NWs coated with three ALD layers as interconnects. Both inner and outer ALD-alumina layers are 50nm as dielectric isolations. The middle one is a 40nm tungsten layer serving as a metallization interconnect. Thin films deposited by ALD are extremely conformal, as shown in Fig. 3.5a. Titanium (30nm) and copper (250nm) were sequentially deposited on the NWs as the adhesion layer and the seed layer for the copper electroplating process (Fig. 3.5b). It should be noted that the seed layers were deposited using thermal evaporation. In evaporation apparatus, a NW sample is first fixed at a sample holder, and the holder is tilted at an angle of 5 degrees to the evaporation target. The holder is rotated during the entire evaporation process. Copper

electroplating is then used to increase the thickness of copper for heat spreading (Fig. 3.5c). The coverage of electroplated copper on NWs is controlled by the plating time. By adjusting the plating time, the NWs can be encapsulated with copper at different coverage levels.

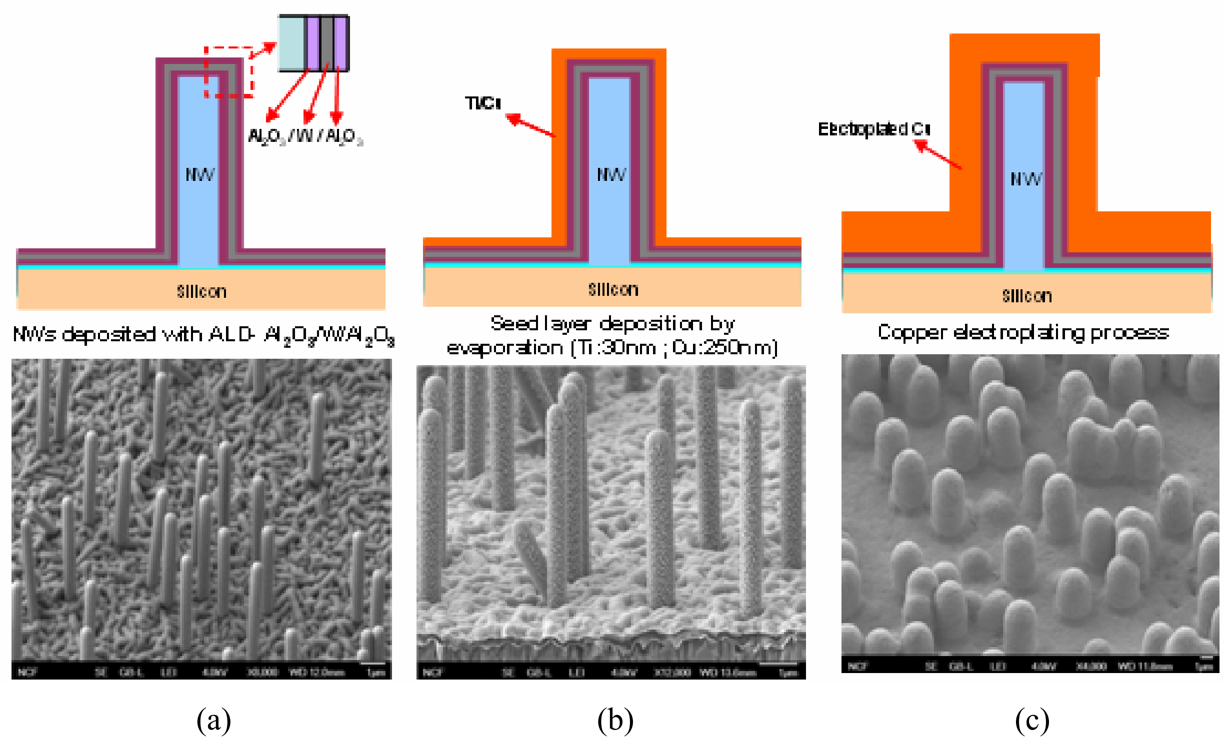


Fig. 3.5: Schematic drawings and corresponding FESEM images of experimental results of the copper encapsulation process. (a) As-grown NWs coated with three interconnects by ALDs. (b) Seed layer deposition for the copper electroplating process by evaporation. (c) The copper electroplating process for 2.5 minutes to increase the copper thickness.

For metallization interconnect, the middle tungsten layer has to be connected to a top electrode for current input/output. BCB was used as the etching mask for the metallization process. Before BCB spin-coating on the NW sample, oxygen plasma treatment of 30 seconds was conducted to improve the wettability of the NW surfaces. BCB was then spun on the NW sample (Fig. 3.6a). The spinning speed is an important parameter to determine the encapsulation

thickness of BCB on NWs. We first used 500 rpm for 5 seconds to spread BCB over the whole sample and then used a high spinning speed of 3500 rpm for 30 seconds to reduce the encapsulation thickness. A high spinning speed is used to achieve a lower encapsulation thickness of BCB on NWs. The lower encapsulation thickness is desirable for the following BCB etching process to decrease processing time. Tips of the NWs with electroplated copper were exposed by using selective BCB etching by RIE, as shown in Fig. 3.6b. Next, the copper surrounding the tip region of the NWs was etched by copper etchant, CE100 from Transene Inc. The etching process is a critical step to determine the coverage thickness of copper on NWs for heat spreading. The processing issue in copper etching is discussed in more detail in the next section. We fast dipped the NW sample into etchant for 5 seconds (Fig. 3.6c). The top portion of copper on the NWs was etched away, and the etched thickness was defined by the etching time. Fig. 3.6c clearly shows that outer ALD-alumina is a good passivation layer and could sustain the etching of copper etchant (CE-100).

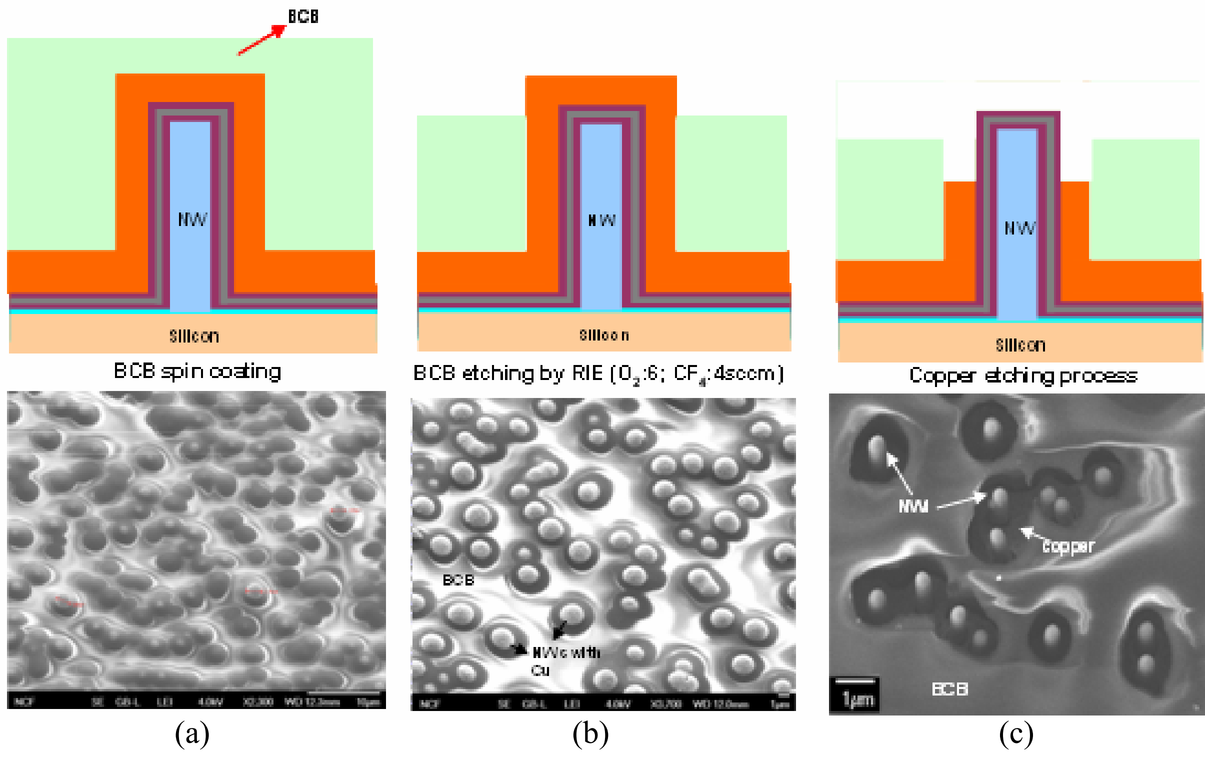


Fig. 3.6: Schematic drawings and corresponding FESEM images of experimental results of the copper encapsulation process. (a) BCB coating on copper-encapsulated NWs. (b) Tips of the NW with electroplated copper exposed by using selective BCB etching by RIE. (c) The copper etching process for 5 seconds to etch copper surrounded the tip region.

BCB was totally removed by RIE (Fig. 3.7a). Next, oxygen plasma treatment, BCB spin-coating, and BCB etching by RIE were sequentially performed to cover the electroplated copper on NWs with BCB and to expose tips of the NWs with ALD-Al_2O_3 /W/Al_2O_3 (Fig. 3.7b). Outer ALD-Al_2O_3 at the tip region was then etched away by 2% HF for 60 seconds (Fig. 3.7c). The gaps between BCB and ALD-W were formed after Al_2O_3 removal (inset of Fig. 3.7c). To observe the gaps, the NWs were broken by using a strong water jet. It clearly showed that outer ALD-Al_2O_3 was totally etched by 2% HF (only ALD-W and inner ALD-Al_2O_3 on NWs). BCB

was spun to fill the gaps, and the tips were exposed by RIE etching again. The thick top W electrode was sputtered on the sample to finalize the entire process. Fig. 3.8 shows the finished sample and the corresponding cross-sectional image by FIB machining (Fig. 3.8b). The NW is successfully surrounded by electroplated copper through conformal nanoscale electrical/dielectric interconnects by ALD. ALD-W is successfully connected to the top electrode for I/Os.

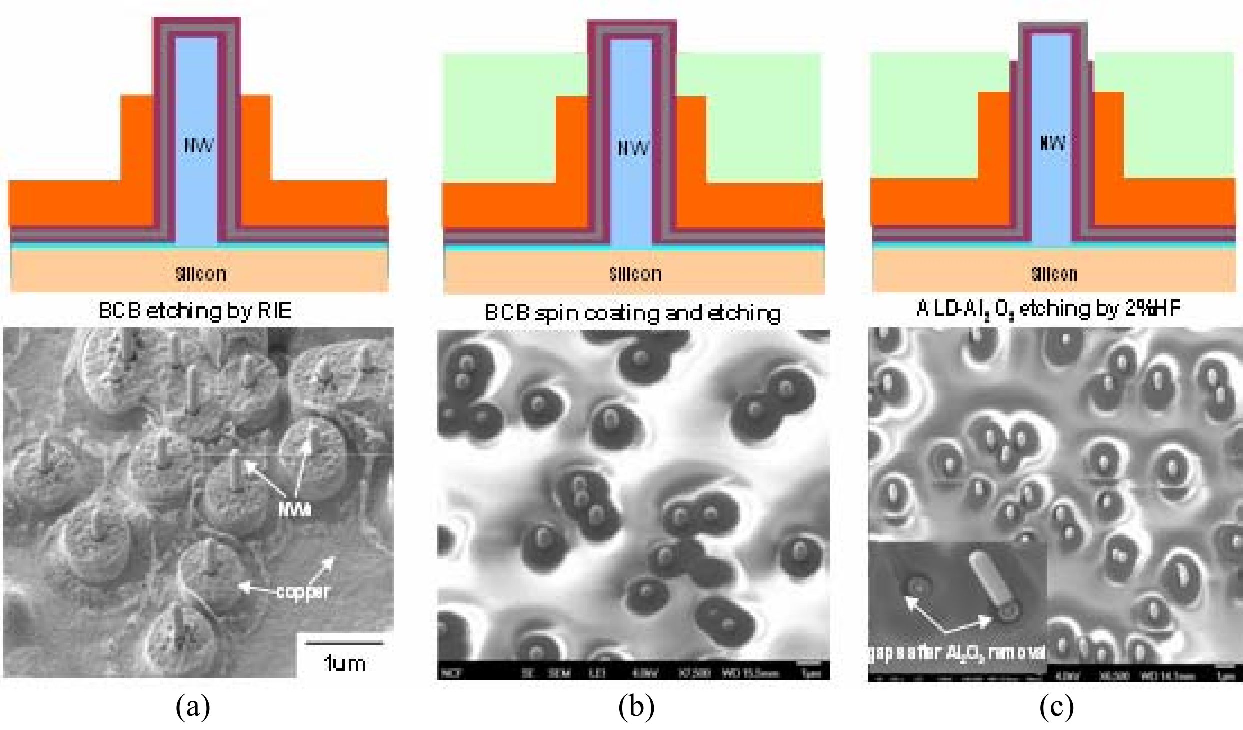


Fig. 3.7: Schematic drawings and corresponding FESEM images of experimental results of the copper encapsulation process. (a) BCB removal by RIE and NWs surrounded by electroplated copper. (b) Tips of the NWs exposed after BCB coating and selective etching. (c) Removal of outer ALD-Al_2O_3 by 2% HF.

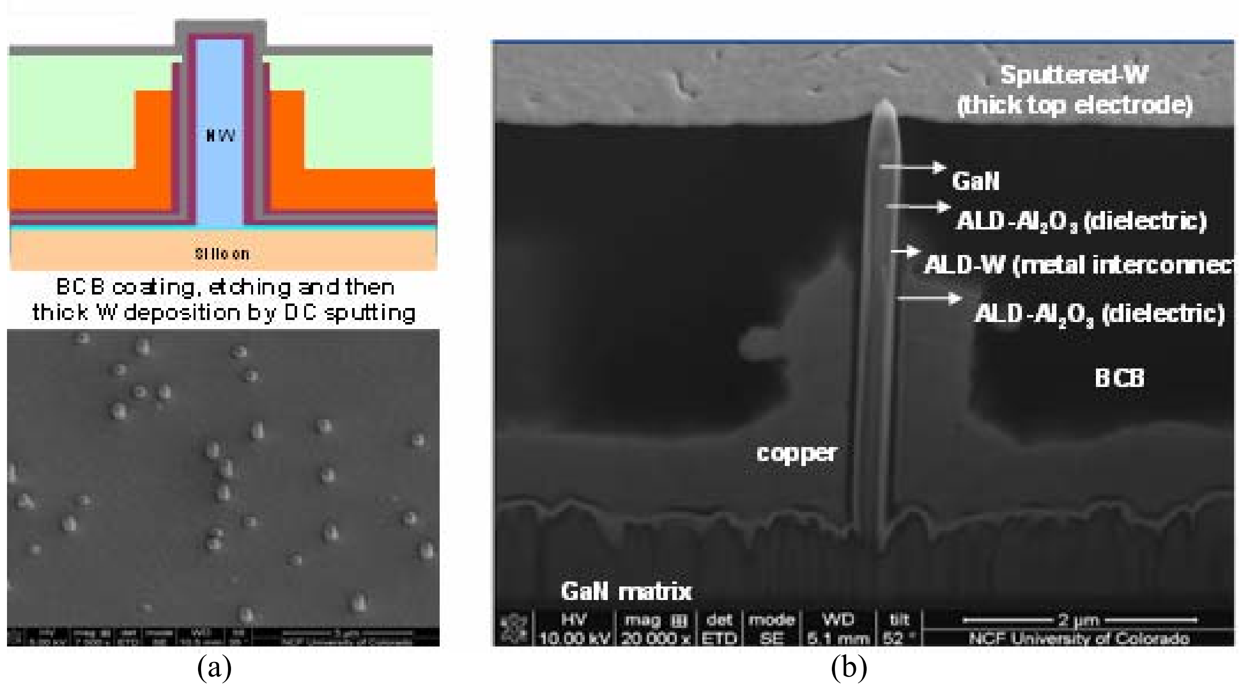


Fig. 3.8: Schematic drawings and corresponding FESEM images of experimental results of the copper encapsulation process. (a) Interconnected NWs covered by top W electrode. (b) Cross-sectional view of the copper-encapsulated NW with ALD layers after FIB cutting.

3.3.2 Adjustable Copper-Encapsulated Thickness for NW Cooling

Etching of electroplated copper is one critical step to determine the copper coverage area on as-grown NWs. It is very important to control uniform etching thickness to interconnect W metallization along the NW to the top W electrode successfully. Fig. 3.9 illustrates the etching issue if the etching thickness of copper is not uniform. Before the copper etching process, thse NWs are encapsulated with copper and BCB (Fig. 3.9a). Low etching-rate copper etchant (for example, Transene Copper Etchant 49-1 with the etching rate of 20nm/second) results in a non-uniform thickness exposure of the NWs because copper is etched isotropically. Fig. 3.9b shows the NWs with different thickness levels of copper after non-uniform copper etching. Afterward,

BCB is spun on the sample as the etching mask for removing ALD-alumina at the tips of the NWs. With non-uniform copper thickness, it is very difficult to cover all copper with BCB for etching ALD-Al_2O_3 at the tip region (fig. 3.9b). By etching outer ALD-Al_2O_3 for interconnecting W along the NW, some copper is exposed because it is not covered with BCB. The copper exposure results in electrical shortage after the deposition of the top thick W electrode.

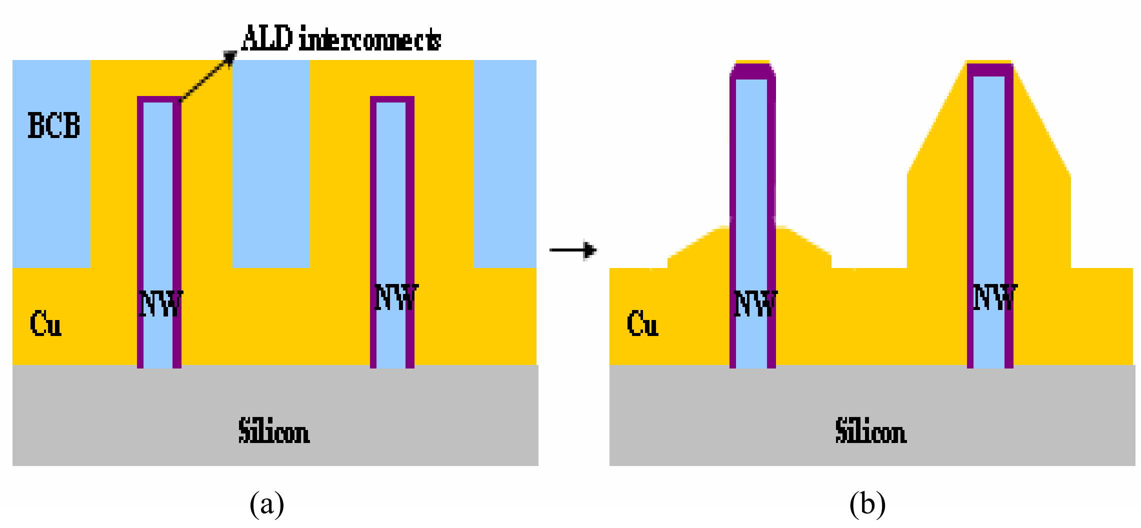


Fig. 3.9: Schematic drawings of non-uniform thickness of copper etching. (a) NWs with copper and BCB before the copper etching process. (b) Different copper coverage thickness levels on NWs after the etching process.

Fig. 3.10 shows the FESEM image of different thickness levels of copper on NWs after non-uniform copper etching. Copper etchant, 49:1 from Transene Inc., was used to etch copper for 40 minutes. Some NWs are exposed without copper; however, some NWs are still encapsulated with copper, and the tips of the NWs are not exposed. This will cause the failure of the following interconnect process and will lower the yield of copper-encapsulated NW interconnects.

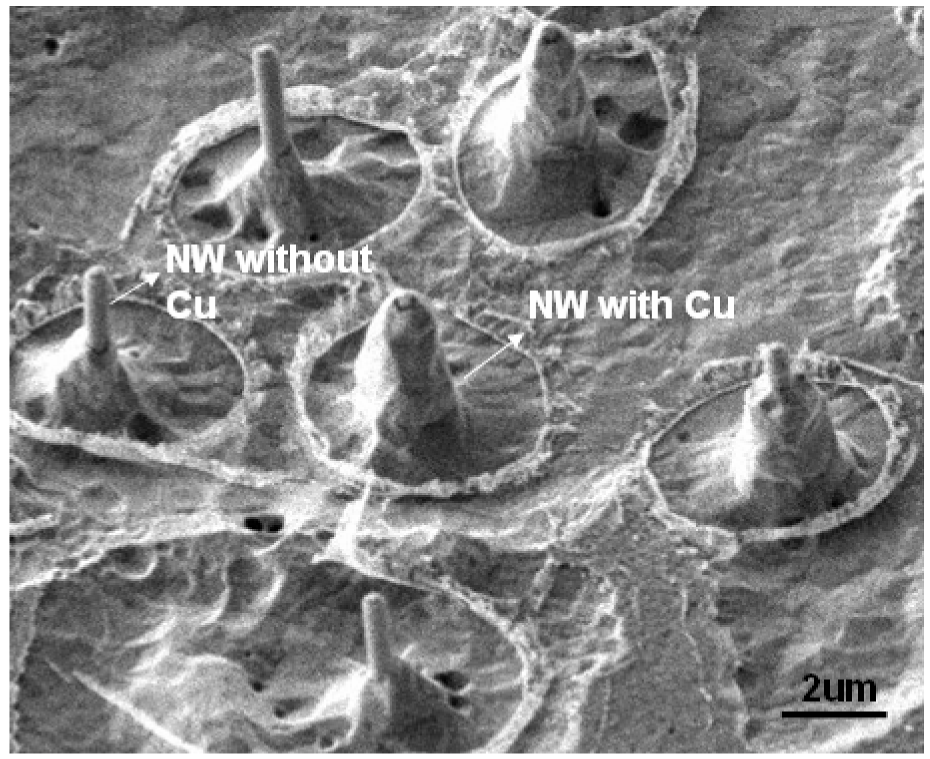


Fig. 3.10: FESEM image of different copper thickness levels on NWs after non-uniform copper etching process. Some NWs are exposed without copper, but some are still covered with copper.

Fabrication issues in non-uniform copper etching were overcome by using high etching-rate etchant (CE100 from Transene Inc.), and we were able to control uniform copper etching thickness. Fig. 3.11 demonstrates different copper coverage areas on NWs by tuning copper plating and etching times. The plating current was controlled at 0.01A in all processes. Fig. 3.11a shows that the NW was partially encapsulated with copper by plating for 150 seconds and then etching for 7 seconds by CE100. By decreasing the etching time from 7 to 5 seconds (Fig. 3.11a to Fig. 3.11b), copper coverage on the NW was increased. As we further increased the plating time and decreased the etching time (from Fig. 3.11a to 3.11d), the NW was encapsulated with a high copper coverage. By plating for 240 seconds and etching for 1 second, we accomplished the

best copper coverage on the NW (Fig. 3.11d) and achieved 52x thermal resistance reduction compared with a full BCB encapsulation on the NW.

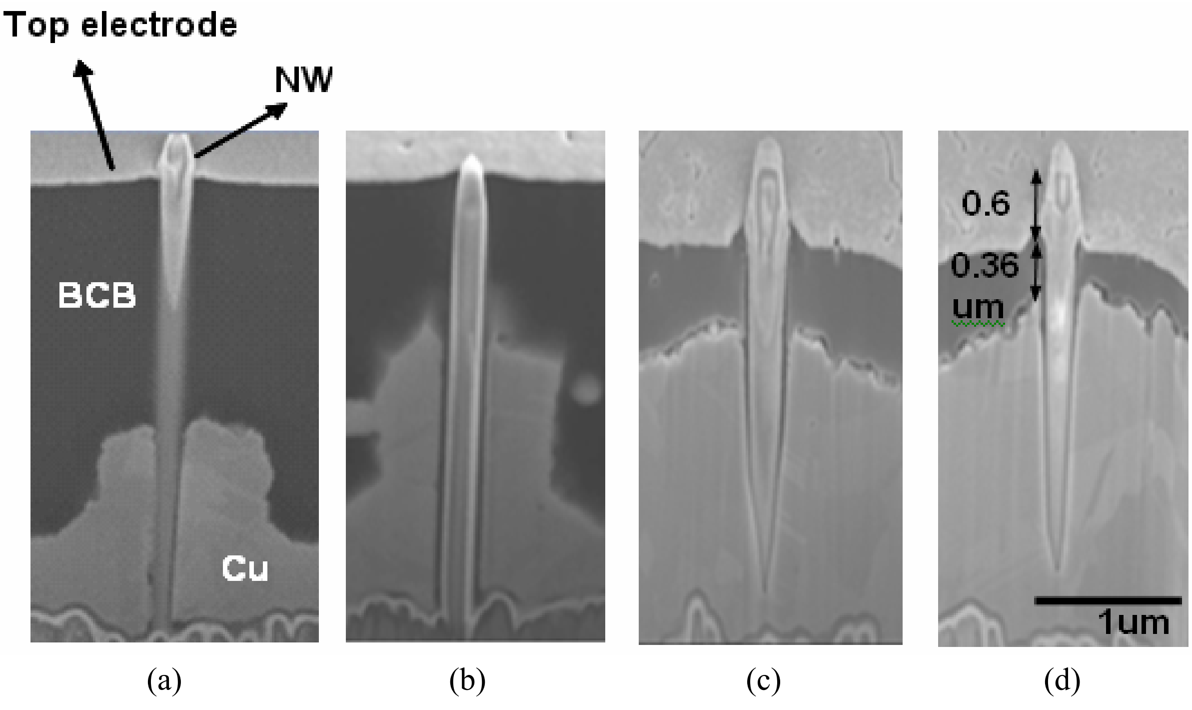


Fig. 3.11: Cross-sectional micrographs of a NW encapsulated with different copper coverage areas by adjusting copper plating and etching times. (a) Plating for 150 and etching for 7 seconds. (b) Plating for 150 and etching for 5 seconds. (c) Plating for 210 and etching for 2 seconds. (d) Plating for 240 and etching for 1 second.

As indicated in Fig. 3.11, the top 1um of the NW could not be covered with electroplated copper. This 1um length of the NW is required for the interconnect process of metallization from W along the NW to the top electrode because BCB has to be spun on the NW as the etching mask. With BCB covering on the NW, the outer ALD-Al_2O_3 at the tip region can be locally etched, and the middle W layer is able to be connected to the top electrode. When the full NW length is used for the device active region that generates heat (Fig. 3.12a), W along the NW

cannot be interconnected to the top electrode if full copper coverage is on the NW. According to the fabrication process, we conclude that the top 1um of the NW should be used for interconnect, and the rest is used for the device active region in as-grown NW applications (Fig. 3.12b). Interconnection of W on NWs has been verified by four-probe measurements, as described in Appendix F.

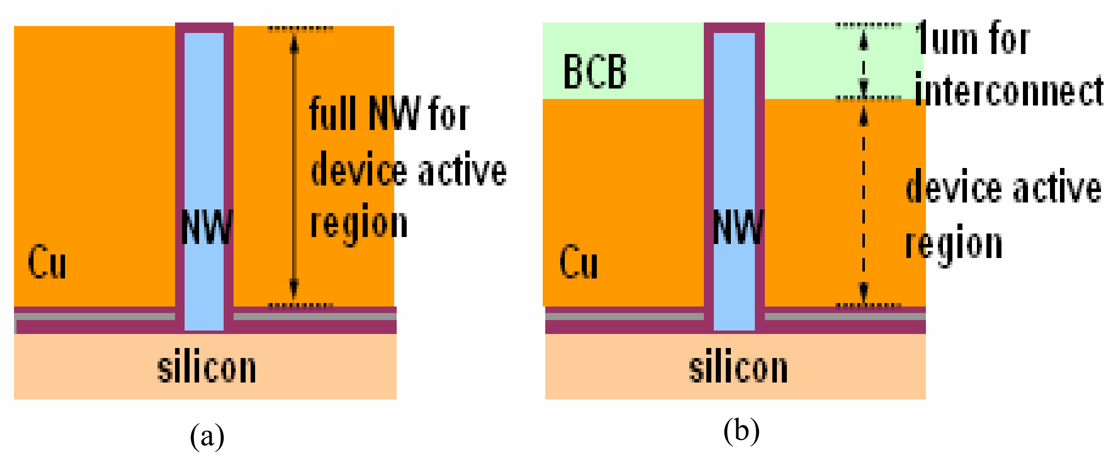


Fig. 3.12: (a) Full length of the NW used for the device active region. With this configuration, the metallic layer on the NW cannot be interconnected to the top electrode. (b) Top 1um of the NW is used for interconnect, and the rest is for the device active region.

The interface between copper and dielectric/metallic interconnects plays a vital role in overall thermal performance. Fig. 3.13 reveals the top view of layer-by-layer structure of the copper-encapsulated NW sample. The sample was polished by a grinding machine to remove the top W electrode for interface observation. Fig. 3.13a shows that each NW is surrounded with cooling-enhanced electroplated copper (area in gray). The area in white is BCB, which is spun between the NWs as the etching mask. From Fig. 3.13b, GaN NWs are first contacted with precise thickness of multilayer interconnects by ALD (Al_2O_3/W/Al_2O_3) and then encapsulated

with copper. The thickness of multilayer interconnects by ALD determines the overall thermal performance of the copper-encapsulated NW device. With exact thickness control by the ALD process and close copper encapsulation, we are able to guarantee the thermal performance of the NW device with specific thickness of the interconnects. Lower thermal resistance can be achieved with the reductions in the interconnect thickness.

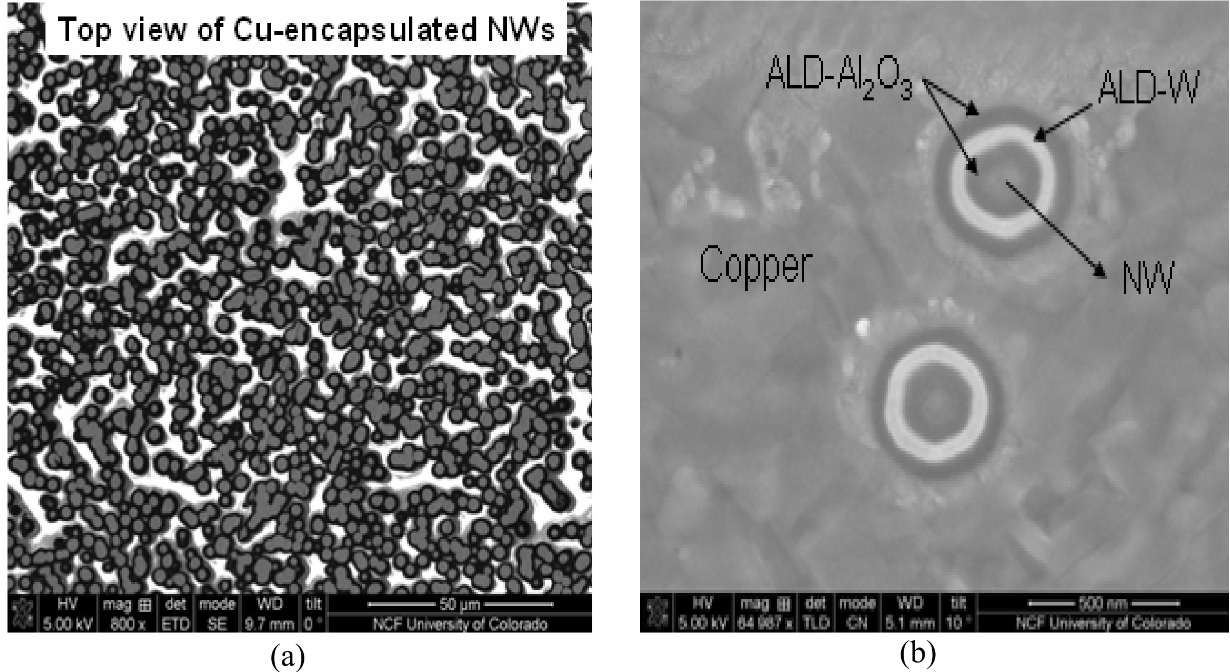


Fig. 3.13: (a) Top view of copper-encapsulated NWs. The area in gray represents NWs encapsulated with copper, and the area in white is BCB. (b) Top view of layer-by-layer structure between copper and NW. NWs are closely surrounded by copper through conformal ALD-W and ALD-Al_2O_3.

The coverage uniformity of copper-encapsulated NWs over the entire sample is shown in Fig. 3.14. The entire NW sample size is around 1cm by 1cm. Magnification in FESEM is at 29x (lowest magnification), and SEM image was taken at the right-lower region of the sample. Fig.

3.14 shows the SEM image taken at the edge of the sample. It shows that the region with copper-encapsulated NWs successfully interconnected with the tip covered is at the center region of the sample. A 50% yield rate of NWs on the sample can be successfully encapsulated and interconnected by the process by FESEM examination. If the NW sample is larger, the edge bead effect can be reduced, and the yield can be further increased. Fig. 3.15 to Fig. 3.18 show the FESEM images taken at each location.

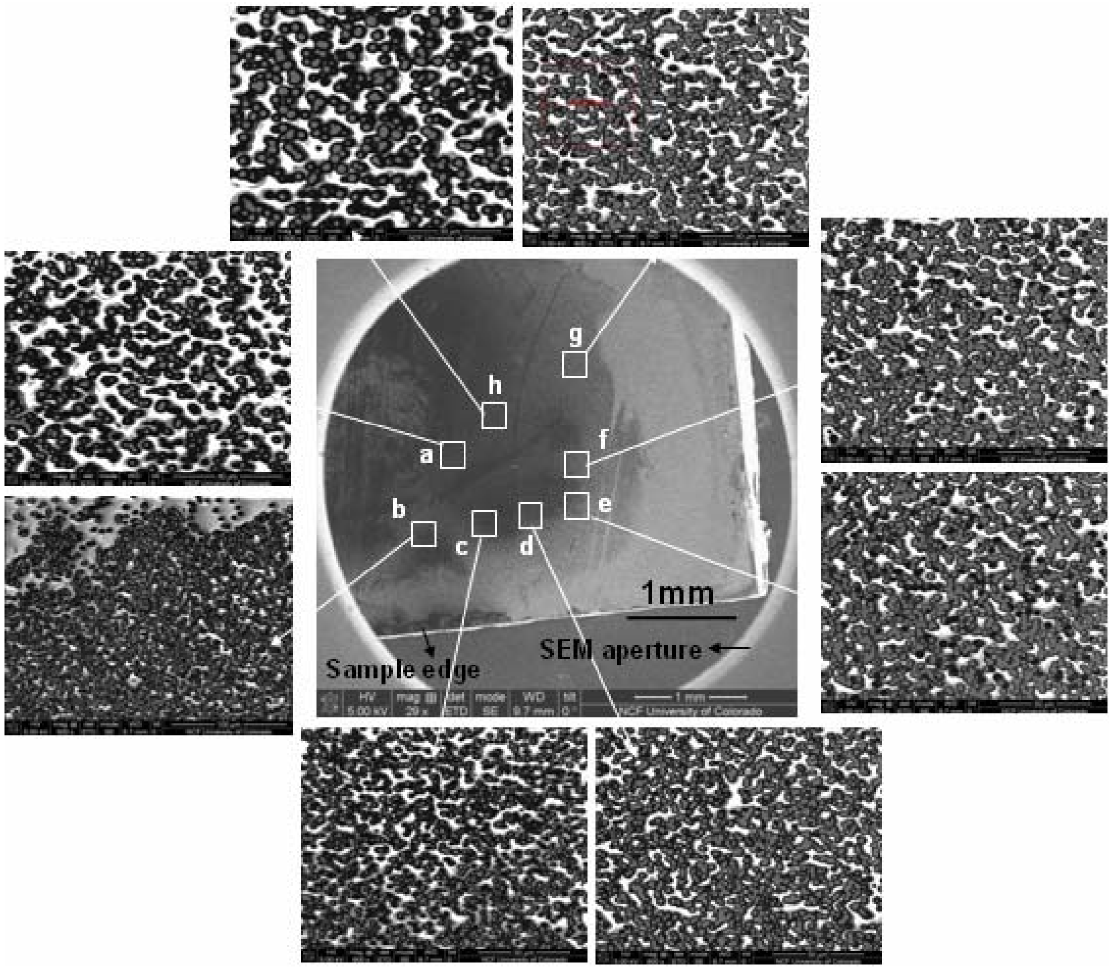
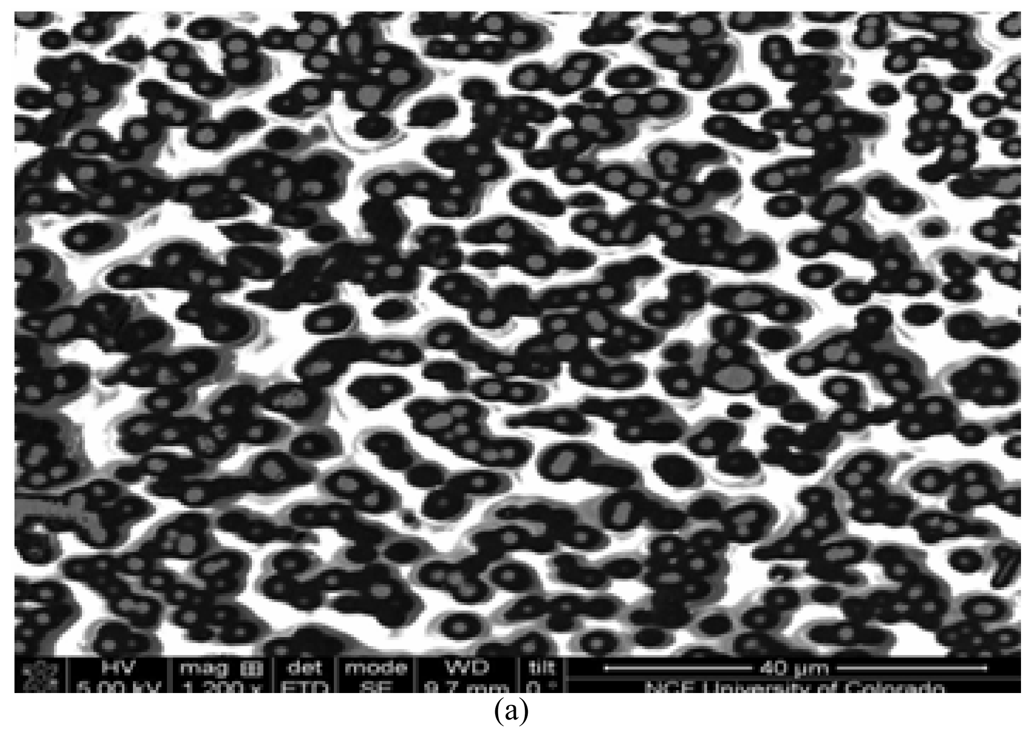
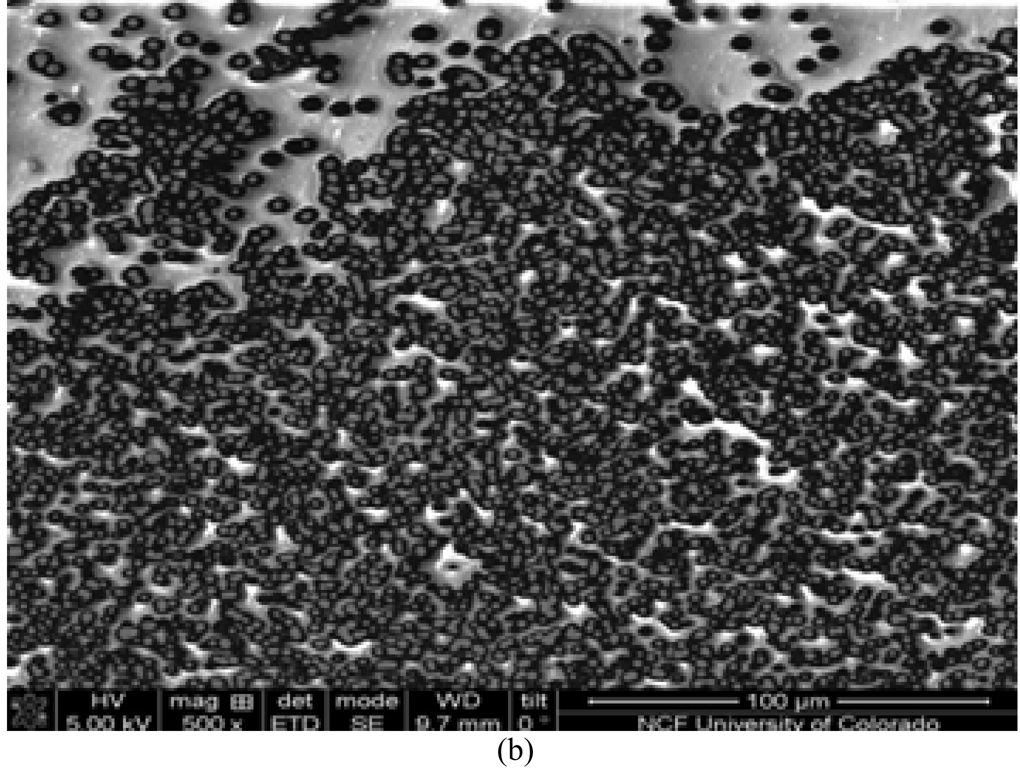


Fig. 3.14: Top view of FESEM images of copper-encapsulated NWs taken at right-lower region of the sample with 1 cm^2.

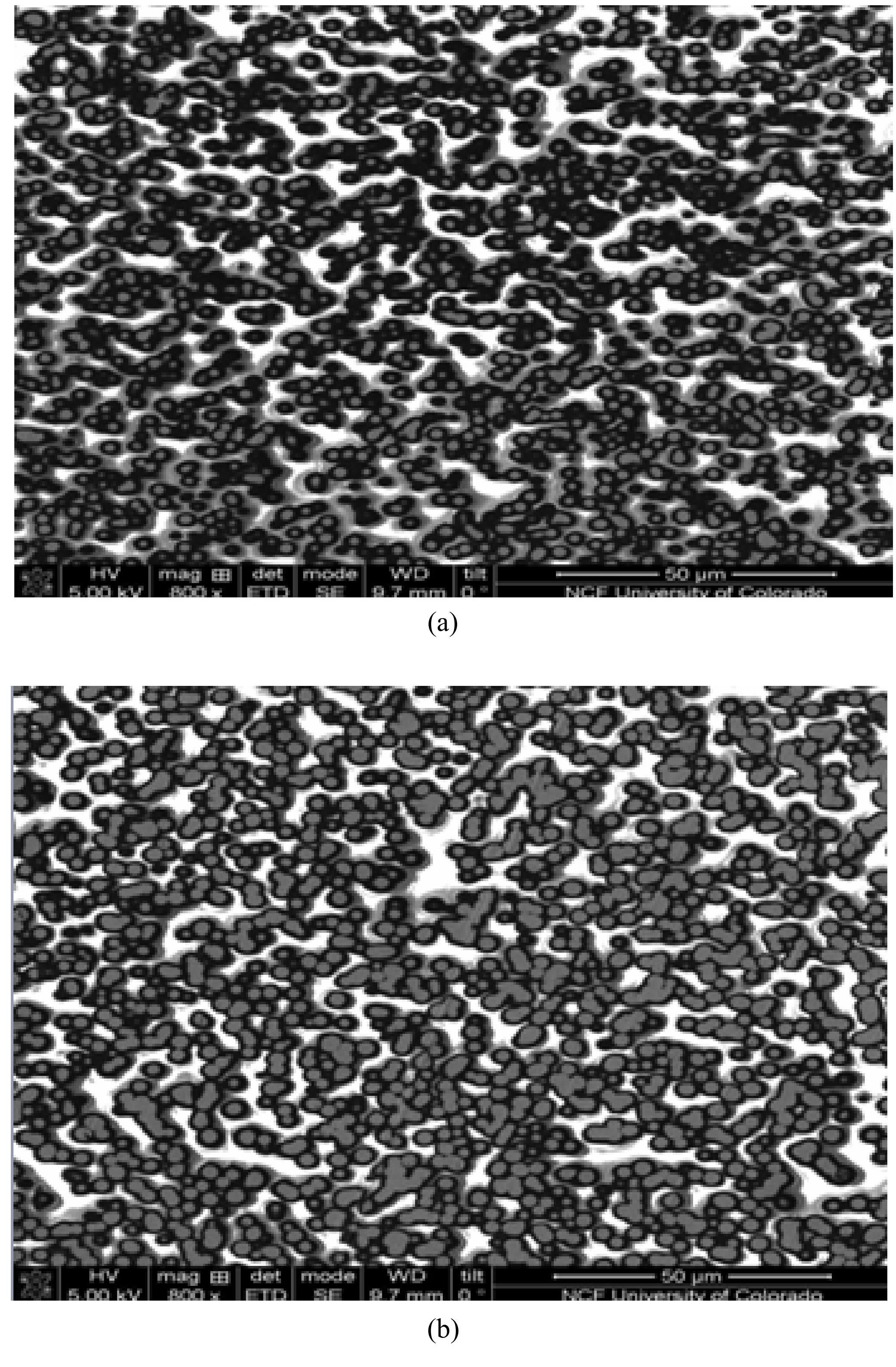


(a)



(b)

Fig. 3.15: (a) FESEM image taken at location a. (b) FESEM image at location b.



(a)

(b)

Fig. 3.16: (a) FESEM image taken at location c. (b) FESEM image at location d.

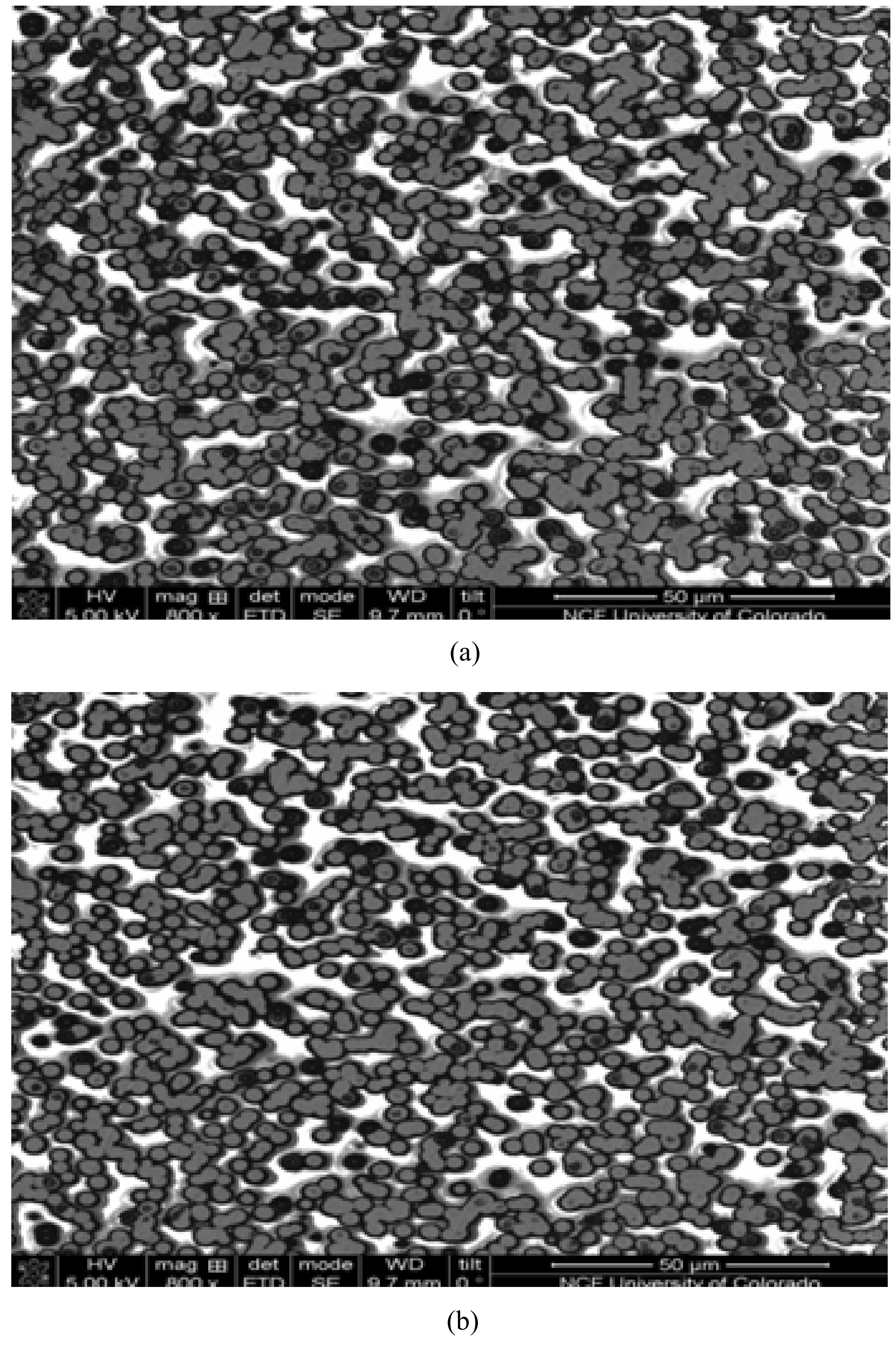
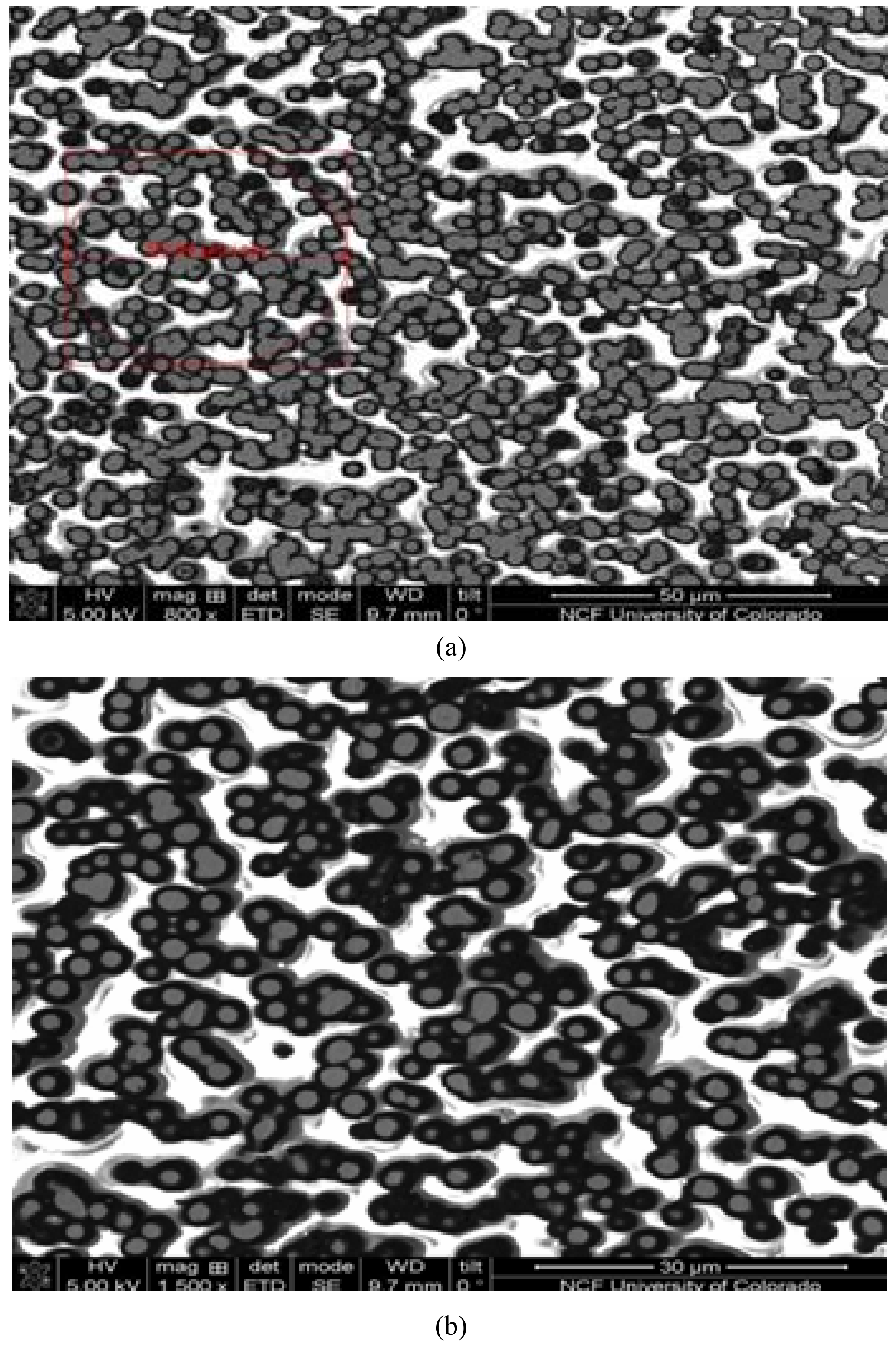


Fig. 3.17: (a) FESEM image taken at location e. (b) FESEM image at location f.



(a)

(b)

Fig. 3.18: (a) FESEM image taken at location g. (b) FESEM image at location h.

3.4 Summary and Conclusions

We have successfully developed an effective cooling design and fabrication for as-grown NW thermal management. NWs are encapsulated with electroplated copper and interconnected with the tip covered. By tuning the copper plating and etching times, we have accomplished adjustable copper coverage area on the NWs and achieved 52x thermal resistance reduction compared with full BCB encapsulation used in state-of-the-art applications. Based on the fabrication process, we conclude that the top 1um of the NW length has to be reserved for the interconnect process, and the rest is for the device active region. Layer-by-layer structure in FESEM image shows that NWs are closely encapsulated with electroplated copper through nanoscaled ALD-enabled interconnects, resulting in low thermal resistance. A 50% yield rate of successful NW encapsulation and interconnection is estimated by FESEM examination.

Chapter 4. Summary and Recommendations

4.1 Summary and Conclusions

The research on as-grown NW devices has seen rapid progress with the applications in nanoelectronics, optoelectronics, sensors, and actuators. This research contributes to the following aspects of interconnect and packaging technologies for as-grown NW devices.

1) Although NW devices have been demonstrated in the laboratory setting, the interconnect technology for as-grown NWs has had less progress in the past. We have developed a generic interconnect technology for as-grown NWs. Since no photo-mask can be used for high-aspect-ratio as-grown NWs, BCB is used as the etching mask to replace the photo-mask. Surface area of NWs is successfully connected to the top electrode, and NWs can be interconnected either with the tips covered or exposed for the use in different applications. Interconnection has been verified by a current injection experiment, and this experiment demonstrated a dynamic tuning method of the GaN bandgap by current injection through interconnect that heats the NWs. We have also studied the matrix effect on PL measurement and eliminated this effect by covering the matrix with ALD-W. ALD-W at the tips of NWs is locally removed, and PL measurements confirm that the PL signals measured are at tips of the NWs. By measuring the temperature dependence of the PL peak wavelength, the tip temperature and corresponding thermal performance of as-grown NW devices can be characterized.

2) Thermal management is one critical packaging issue, and it has never been addressed in as-grown NW research communities. We have successfully developed an effective cooling design and fabrication for as-grown NW devices. Thermal simulation is used to guide the thermal design and fabrication. Simulation results show that thermal resistance drops substantially with the increase of copper coverage on NWs. A copper encapsulation process has been developed

and successfully integrated into the interconnect process. NWs are closely encapsulated with copper through multilayer ALD-enabled interconnects. A 52x thermal resistance reduction has been accomplished by using the copper encapsulation process, compared with the results of a full BCB encapsulation used in present devices. To encapsulate NWs with copper and interconnect them to the top electrode simultaneously, our fabrication processes suggest that the top 1um length of the NW should be used for the interconnect and the rest for the device active region. This process also demonstrates a 50% yield rate on the NW sample of 1cm by 1cm by FESEM examination.

4.2 Recommendations for Future Studies

With the recent progress in nanowire materials' synthesis and fabrication, interconnect and packaging technologies will play a significant role in device fabrication and application. The following works in characterization, strain study, and device fabrication are desirable as the needs and extensions for future studies.

4.2.1 Thermal Characterization of Copper- and BCB-encapsulated Nanowires

In this study, we evaluated the thermal performance of copper- and BCB-encapsulated NWs by thermal simulation. It is important to validate the simulation results by experiment. However, the first challenge in this task is how to measure the temperature of NWs and the corresponding thermal performance due to NWs' extremely small dimensions and random distribution on a substrate. Conventional temperature measurement techniques, such as thermocouples and IR camera, cannot be employed for nanoscale dimensions. In conventional LEDs and FETs, junction temperature can be indirectly measured by temperature dependence of

(1) forward bias voltage and (2) PL peak wavelength [67-68]. For temperature measurement of NWs, by far, there is no existing method to measure temperatures for as-grown NW samples.

Temperature-dependent PL peak wavelength measured at the tips of NWs can be used to predict the tip temperatures of the NWs. By using temperature dependence of the peak wavelength, we are able to retract the temperatures from wavelengths. To compare the thermal performance of BCB- and copper-encapsulated NWs, we can remove most of the wires by FIB and fabricate one-wire devices encapsulated with BCB and copper. At the same power input into the metal interconnect, we are able to compare the heat spreading performance of copper- and BCB-encapsulated NWs.

4.2.2 Fabrication of As-Grown Core-Shell Nanowire Light-Emitting Diodes with Effective Cooling

Our study demonstrates interconnect and packaging technologies for as-grown nanowire devices. The completion of interconnect and packaging of as-grown NWs would be the first step toward the development of as-grown NW-based micro/nano systems and devices, which will improve the performance and reduce the manufacturing cost of future as-grown NW-based applications. In this section, we propose a process for fabricating as-grown core-shell nanowire-based LEDs with a cooling-enhanced structure. Fig. 4.1 shows the process flow in detail, and we list each of the processes as follows.

a. Grow core-shell GaN nanowires on a silicon substrate by MBE.

b. Deposit the dielectric layer (alumina) by ALD.

c. Apply the BCB process as the etching mask using the following processing steps: use oxygen plasma treatment on the NW sample, spin-coat BCB on the sample, and etch BCB by RIE to

expose ALD-alumina at the tips of the NWs. Then, etch ALD-alumina by 2% HF and remove BCB by RIE (CF_4:O_2= 4:6).

d. Deposit W (metal interconnect) and alumina (dielectric insulator) by ALD, respectively.

e. Deposit titanium and copper as the electroplating seed layer by thermal evaporation.

f. Electroplate thick copper as the heat spreading material.

g. Apply the BCB process as the etching mask using the following processing steps: use oxygen plasma treatment on the NW sample, spin-coat BCB on the sample, and etch BCB by RIE to expose the electroplated copper at the tips of NWs.

h. Etch electroplated copper at the NW tip region and remove BCB totally.

i. Apply the BCB process as the etching mask using the following processing steps: use oxygen plasma treatment on the NW sample, spin-coat BCB on the sample, and etch BCB by RIE to expose ALD-alumina on the tips of NWs.

j. Etch ALD-alumina by 2% HF. Then, reduce BCB thickness by RIE.

k. Interconnect metal along the nanowire to a top thick electrode (tungsten) by the evaporation or sputtering process.

l. Apply the BCB process as the etching mask using the following processing steps: use oxygen plasma treatment on the NW sample, spin-coat BCB on the sample, and etch BCB by RIE to expose tungsten on the tips of NWs. Etch tungsten by tungsten etchant. Remove BCB by RIE to finish the device fabrication process.

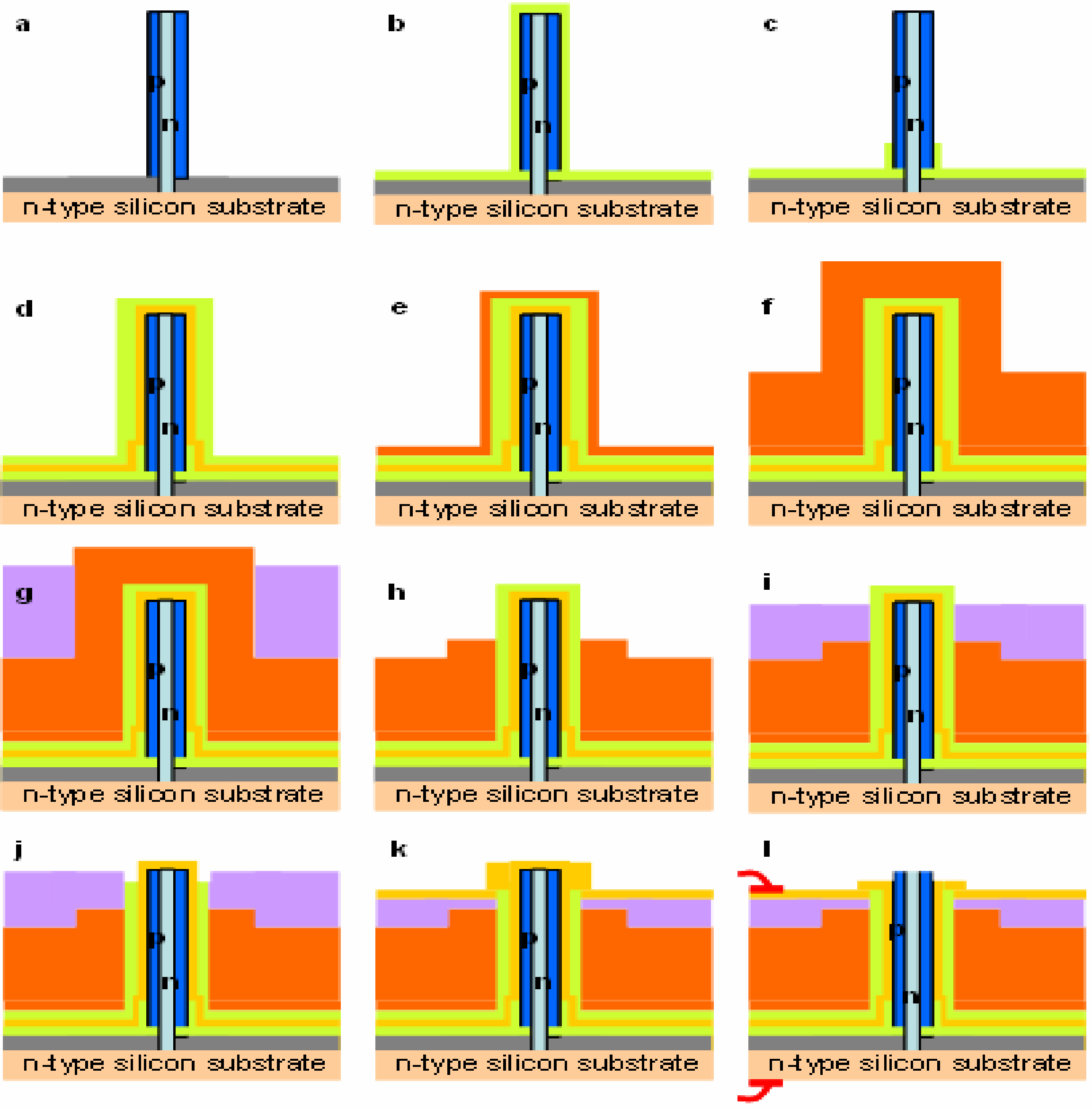


Fig. 4.1: Proposed fabrication process for as-grown core-shell GaN nanowire-based LED with a cooling-enhanced design.

4.2.3 Study of Strain Effect on Nanowires with Different Coatings

The strain effect on NW is an important study, especially when NWs have undergone different temperature processes, such as the growth of ALD-alumina on NWs. This section introduces the preliminary results observed in this dissertation. Two NW samples were prepared

for studying the strain effect on GaN nanowire. One NW sample was coated with 50-nm atomic-layer-deposition alumina; the other was without ALD-alumina. In Fig. 4.2, our preliminary results show blue-shifted PL spectra of the NW sample coated with ALD-alumina. It should be noted that PL signals measured from both samples are mainly from the matrix due to the matrix effect, as discussed in section 2.5.1. Due to the difference of coefficient of thermal expansion (CTE) between the GaN matrix and ALD-alumina, compressive strain [54] is introduced to the bare GaN matrix after we grow ALD-alumina with a thickness of 50nm at 120 °C and then cool the sample down to room temperature. Strain-free condition should be restored if both samples are heated to the ALD growth temperature, 120 ºC. However, due to the complex structure of the GaN matrix, it is difficult to measure the strain restoration.

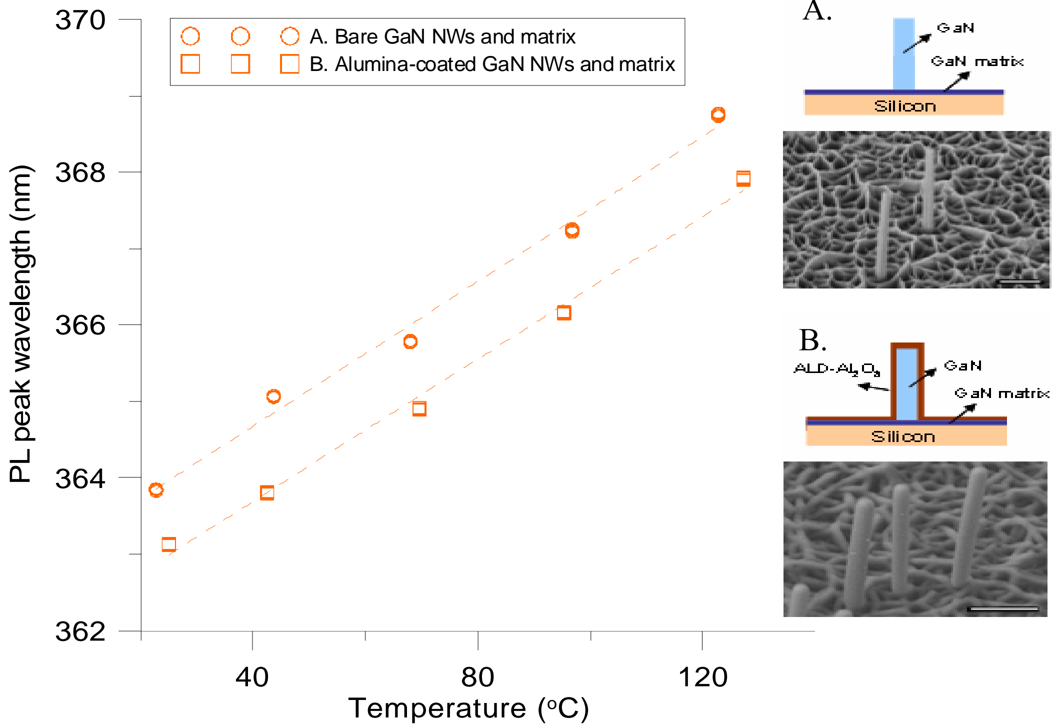


Fig. 4.2: PL measurements to study bandgap shift due to the strain effect. Sample A without ALD-alumina coating. Sample B with ALD-alumina coating. Blue-shifted PL spectra of NW sample A coated with ALD-alumina.

To eliminate the matrix effect, sample A was first grown with 50-nm alumina. Both samples were grown with 40-nm W. W at the tips of both samples was removed for NW-only PL measurement. Alumina on sample A was further removed by 2% HF to restore the strain-free condition at the tips of the NWs (Fig. 4.3a).

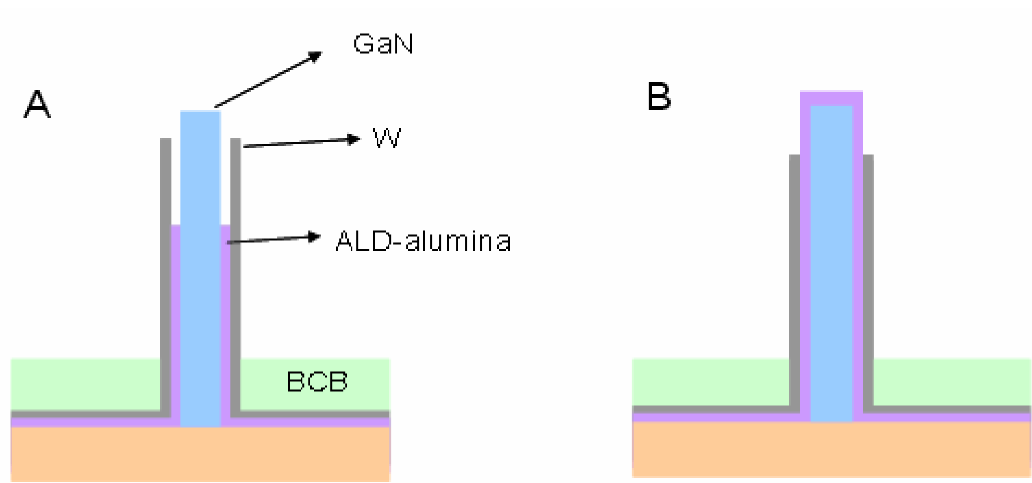


Fig. 4.3: (a) In sample A, ALD-alumina at the tips of the NWs was removed by 2% HF to restore strain-free condition. (b) In sample B, ALD-alumina remains on the tips of the NWs for comparison.

Temperature-dependent PL measurements were performed to investigate the strain effect on as-grown NWs with and without ALD-alumina coating. The trends of both samples with the ALD-W covering matrix are different from those without W coating. When both samples were heated by TEC from room temperature to 120 ^{o}C, the bandgap shift reduced with the increase of temperature. This experiment demonstrates the strain release by the removal of ALD-alumina. However, further experiments are needed to study the strain effect in comparison with bandgap shift calculation [69-70].

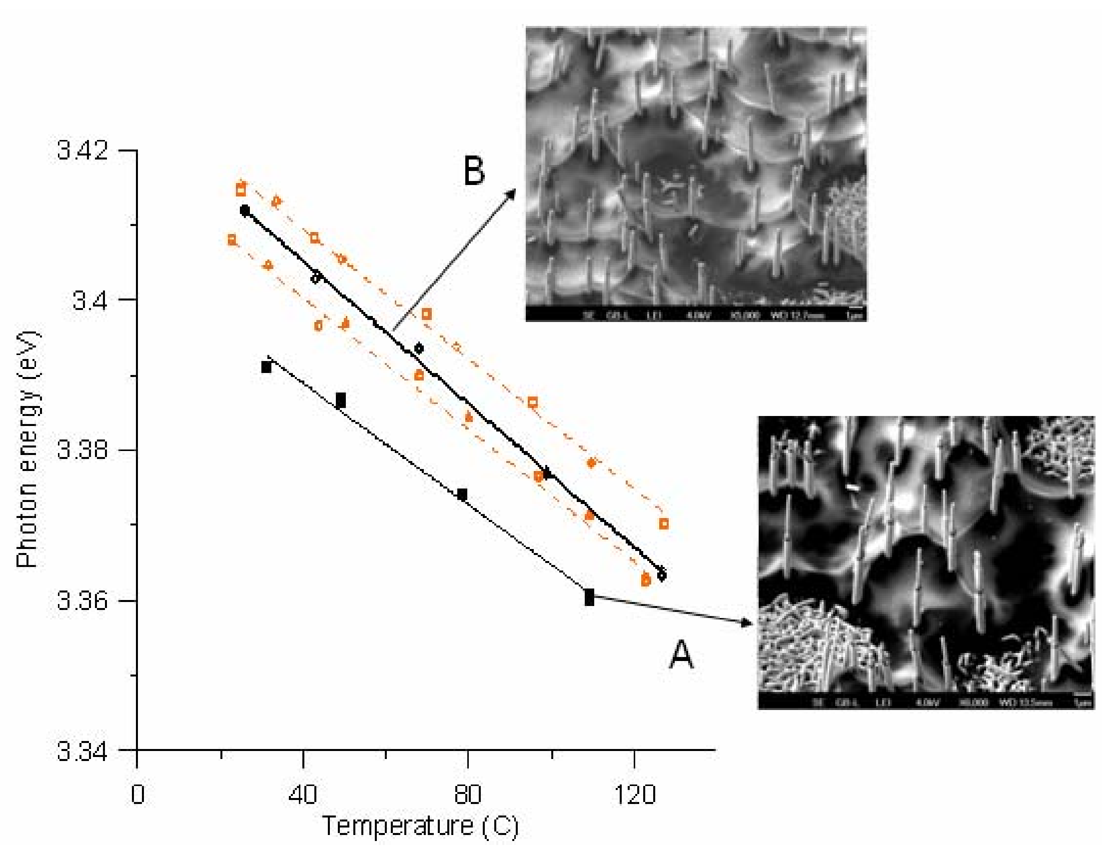


Fig. 4.4: PL measurements on samples A and B for the study of the strain effect.

4.2.4 Nanogap Fabrication Using ALD Layers as Sacrificial Layers

Thin film grown by ALD technology is known for exact thickness control by the growth cycle and for excellent step coverage on a sample even with a high aspect ratio. Controlling the thickness of ALD-deposited sacrificial layer, we are able to fabricate a nanogap with precise control of the gap thickness. The uniform gap thickness is important to devices using electrostatic force for detection and actuation such as NEMS switches or tunneling devices [71-73]. Fig. 4.5 shows the FESEM images of (a) 40-nm and (b) 50-nm nanogaps by using ALD-W and ALD-alumina as sacrificial layers, respectively.

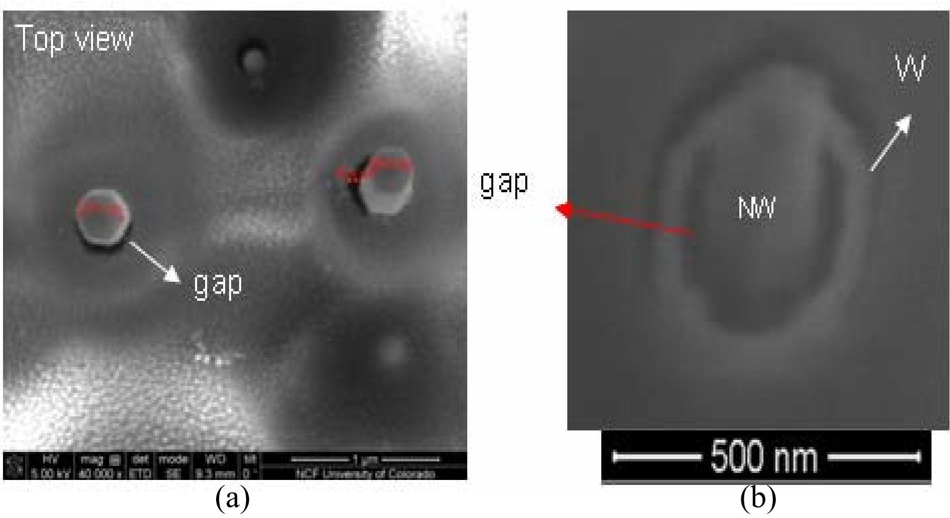


Fig. 4.5: FESEM images of nanogap fabrication using (a) 40-nm ALD-W and (b) 50-nm ALD-Al_2O_3 as sacrificial layers.

Nanogap fabrication can be employed for tuning NW bandgap by electrical field. The bandgap of a NW can be dynamically tuned as the strain on the wire increases by electrical field. Fig. 4.6 shows the schematic drawing of device configuration. Future works should focus on the design and fabrication of electrodes that surround NWs by FIB. Asymmetric electrode shape can provide an asymmetric electrostatic force on NW for bending. The calculation and study of the bending force induced by the electrical field are of importance in device performance. Once the bending of NW occurs, PL system can be used to measure the bandgap change of the wire under bending.

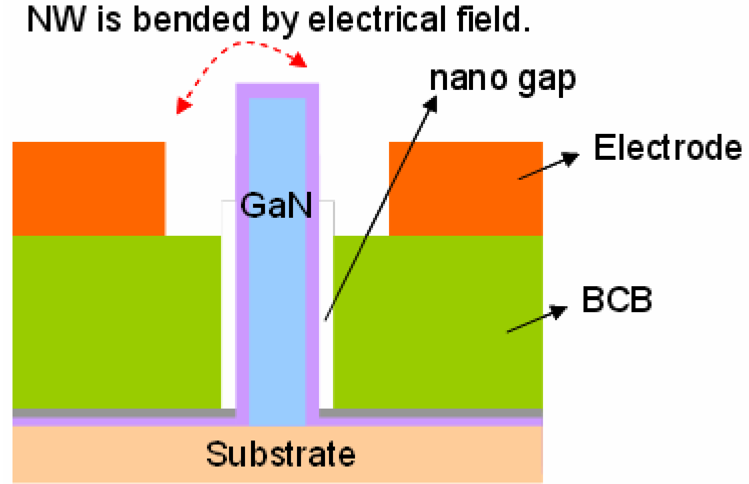


Fig. 4.6: Schematic drawing of the GaN NW bandgap tuning by using electrical field to bend NWs.

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Appendix A

Effective Thermal Conductivity Measurement of Cooling-Enhanced Nanowires

In this study, the thermoreflectance measurement using pump-probe technique is conducted to measure the effective thermal conductivity of copper- and BCB-encapsulated NW samples. In this technique, the sample is first shined by a "pump" pulse of light over a short period of time. The surface of the sample absorbs the energy, and the energy decays over time. The "probe" pulse or a continuous beam then impinges on the same location of the sample and measures the difference of temperature-dependent optical properties, such as reflectivity. By measuring the reflectivity change on the sample surface, we can predict the sample's thermal diffusivity and corresponding thermal conductivity (Fig. A.1). The detailed measurement principle and experimental setups can be found elsewhere in literature. Here, we only introduce the sample preparation and measurement results.

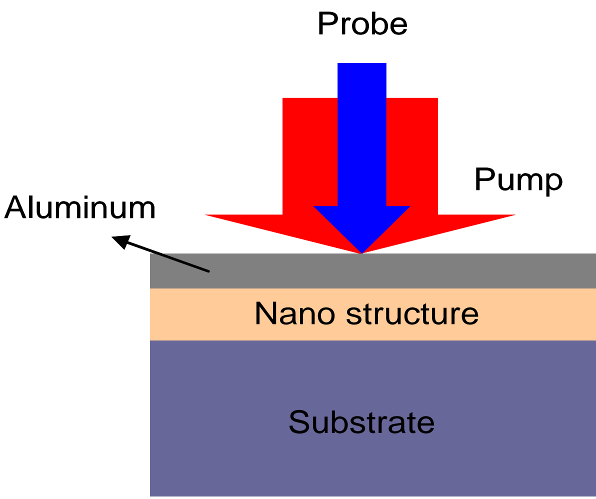


Fig. A.1: Schematic drawing of thermoreflectance measurement using the pump-probe technique.

Three NW samples have been prepared for the thermoreflectance measurement. The schematic drawings and corresponding FESEM images are shown in Fig. A.2. Fig. A.2 shows

the NW sample (sample A) fully encapsulated with BCB (Fig. A.2a). Sample A is treated by the oxygen plasma process and coated with BCB. To reduce the BCB thickness and increase the surface flatness, the sample is polished using a grinding machine with the use of additional diamond suspension particles (250nm from Struers). Fig. A.2b (sample B) shows the NW sample encapsulated partially with copper and BCB. As in the process described in section 3.4.1, we control the plating time and corresponding copper coverage on NWs. BCB is then coated to fill the gaps between copper-encapsulated NWs. The sample is finally polished by a grinding machine as described above. Fig. A.2c (sample C) shows the NWs fully encapsulated with copper. The plating time in sample C is twice that in sample B preparation (2.5 minutes). After the NWs are fully encapsulated with copper, the sample undergoes the polishing process to reduce thickness and increase flatness, as we did for sample A and B.

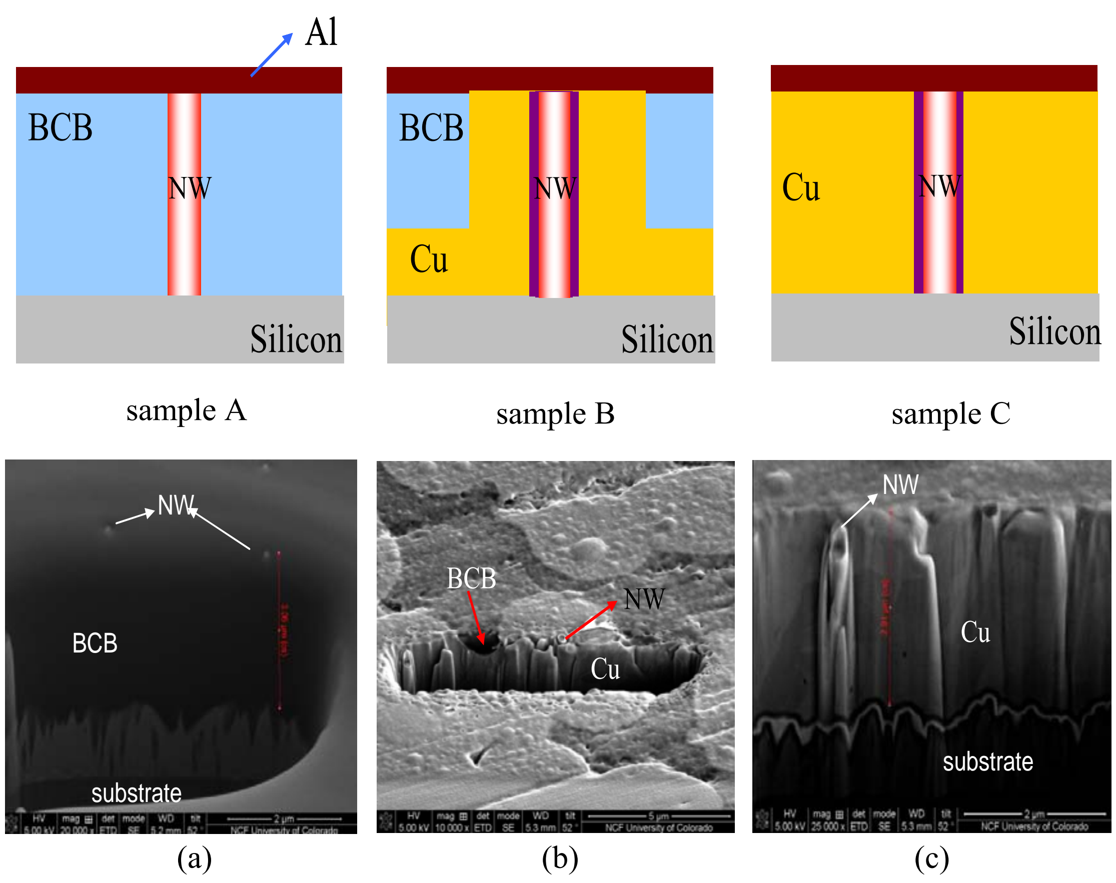


Fig. A.2: Schematic drawings and corresponding FESEM images of (a) fully BCB- encapsulated, (b) BCB- and copper-encapsulated, (c) fully copper-encapsulated NWs.

Effective thermal conductivity is estimated by the thermal resistance analysis. For each NW, the 1-D thermal resistance under parallel configuration can be written using Eq. A.1 as,

$$1/R_{total}=1/R_{NW}+1/R_{copper}+1/R_{BCB}+1/R_{interconnects} \quad (A.1)$$

where R_{NW}, as shown in Fig. A.3 is the thermal resistance of the NW, which is defined as the NW length divided by the product of thermal conductivity and cross-sectional area of the NW. Other thermal resistances are defined as discussed above.

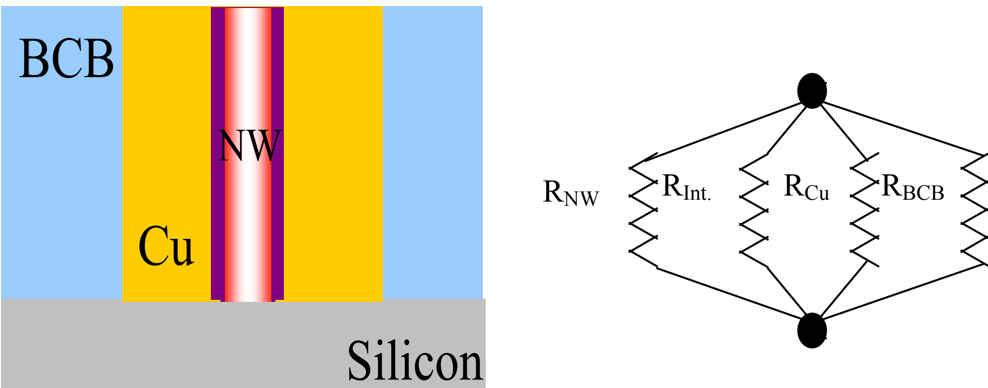


Fig. A.3: Schematic drawing of the thermal resistance analysis for a NW encapsulated with copper and BCB.

Since the length in all materials is the same, we can cancel it from the Eq. A.1 as

$$A_{total}\,K_{eff} = A_{NW}K_{NW} + A_{Cu}K_{Cu} + A_{BCB}K_{BCB} + A_{Interconnects}K_{Interconnects} \quad (A.2)$$

The laser spot is around 50um, and about 10 NWs are shined by the laser. The total NW area is extremely small relative to the total area. We thus neglect the items of the NW and interconnects in Eq. A.2 and use area ratio to replace area of copper and BCB, that is:

$$K_{eff} = \beta_{Cu} K_{Cu} + (1-\beta_{Cu}) K_{BCB} \qquad (A.3)$$

where β_{Cu} is the area ratio of copper, and $(1-\beta_{Cu})$ is the area ratio of BCB. With the material properties ($K_{BCB} = 0.29$ W/mK and $K_{Cu} = 400$ W/mK) used in equation Eq. A.3, we can obtain the effective thermal conductivity of NWs with different encapsulation conditions. Fig. A.4 shows the calculation and experiment results of the effective thermal conductivity of NWs with different encapsulations. The effective conductivity of full copper encapsulation ($K_{Cu} = 360$ W/mK) is used for CFD modeling in Chapters 1 and 3.

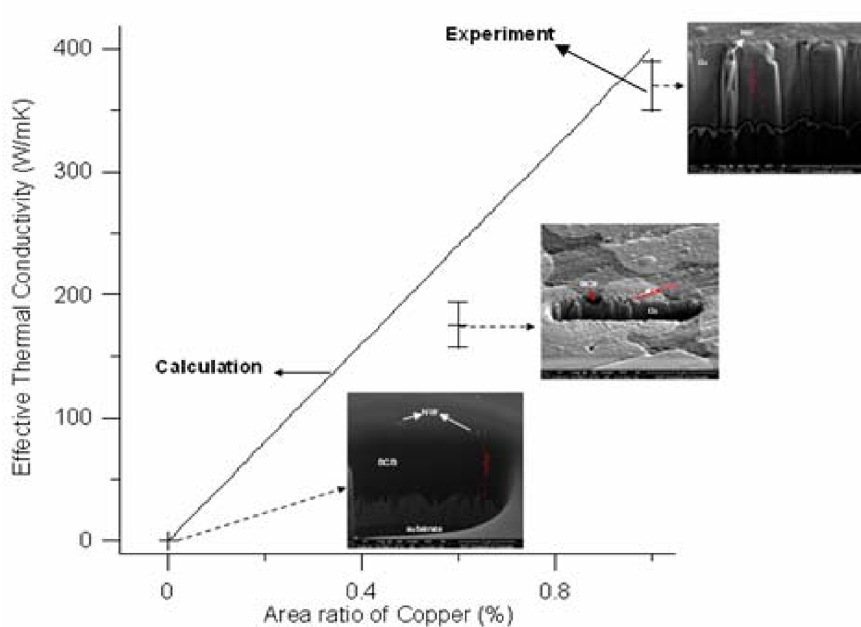


Fig. A.4: Effective thermal conductivity of NWs with different encapsulation conditions. Error bars are experimental results, and calculation results are represented as the line.

Appendix B

Recipe of NW Interconnected with the Tip Exposed

Experiment procedures and recipe for interconnect with NW tips exposed.

1. Attach a nanowire sample (around 1cm x 1cm) coated with ALD layers (50nm Al_2O_3 and 40nm W) on a holder chip by using carbon tape (used in SEM sample attachment) as shown in the following image.

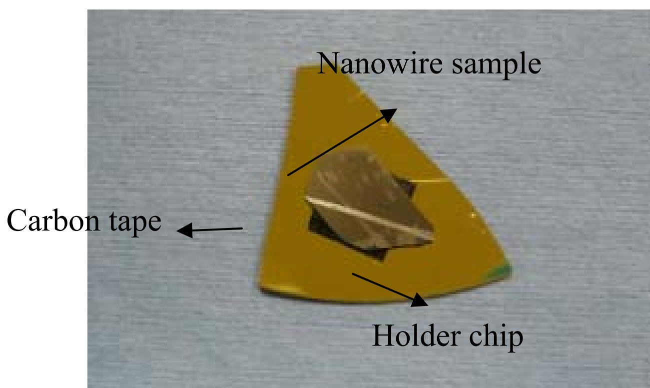


Fig. B.1: Photo of a NW sample attached on a holder chip

2. BCB preparation: BCB (the one packaged with a plastic bag in the freezer in Fab lab) is diluted with T1000 (in the yellow room in MEMS lab). Use a plastic tube to get BCB and another tube to get T1000, and then mix them in a clean glass bottle. The ratio is 1 to 1. Put diluted BCB in the refrigerator if not using it and cool it down for 1 hour if taking out from the refrigerator.

3. Oxygen plasma treatment: Take the sample into the chamber of the plasma machine. Pump the chamber down to 0.5 mtorr. Open the valve of the oxygen tank and set the flow rate at 2 sccm.

When the pressure is stable, turn on the RF power and set the RF power at 75 watt and the processing time at 60 seconds.

4. Spin-coater setup: A two-step coating is used in the experiment. The first step is 500 rpm (ramping: 300 rpm) for 5 seconds and the second step is 3000 rpm (ramping: 500 rpm). The objective of first coating is to spread BCB on the sample uniformly. The second coating controls the thickness of BCB on the sample.

5. BCB spin-coating: Put the sample on the holder of spin-coater. Drip 2-3 drops of BCB on the sample. Start spinning, and when the spinning rate reaches 3000 rpm (from the first step to the second step and reaches the spinning rate of the second rate), stop spinning. NWs are functioned as a structure to hold the BCB on the sample. Thickness of BCB on the NW sample is controlled by the spinning rate. When trying lower spinning rate, we can get thicker thickness of BCB.

6. Soft-bake: 70 °C for 3 minutes. The purpose of soft-bake is to dry the solvent in BCB or other negative polymers. The temperature and time are determined by the percentage of solvent baked. A useful way to determine the temperature and time is to measure and compare the weight of the sample before and after soft-bake process. By this step, we can calculate how much solvent has been baked out, and thus adjust the processing temperature and time. This step is very useful not only for BCB, but also for all negative photoresistors.

7. UV exposure: 20 seconds.

8. Hard-bake: 100 °C for 10 minutes. Use an optical microscope to inspect the sample surface after coating (this can give a brief idea and fast inspection of the coating condition under different spinning rates).

9. FESEM inspection: To reduce the problem of BCB polymer charging, two good SEM recipes go as follows. 1). Stage height: 17mm. WD: 13mm. Gentle beam mode (GB-L). LEI mode. 3.4~4 kV. 2). Stage height: 17mm. WD: 14mm. SE, SEM mode, LEI mode. 5 kV.

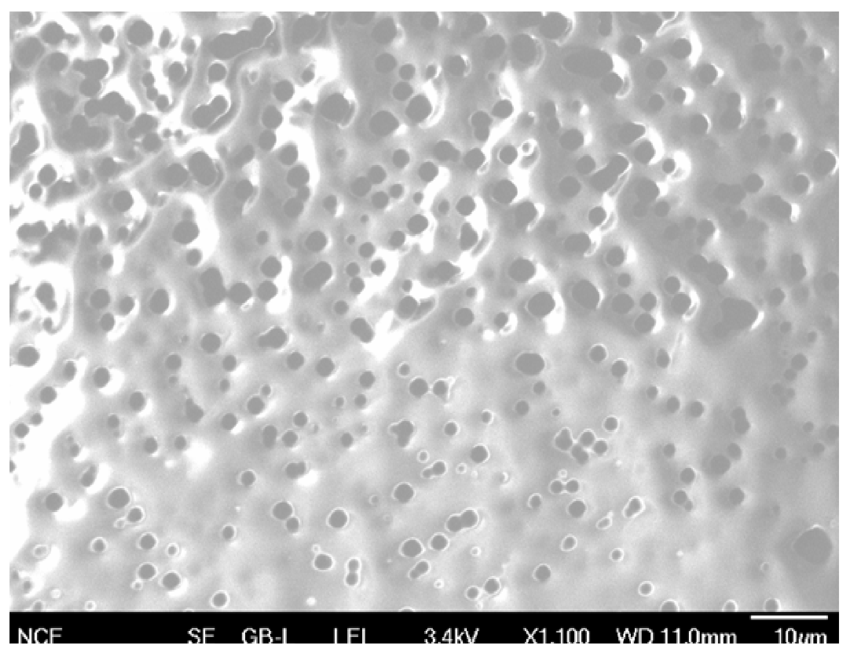


Fig. B.2: SEM of the NW sample after BCB spin-coating

10. RIE to reduce thickness of BCB: RIE recipe (O_2 : CF_4 = 6 sccm: 4 sccm). RF power is around 340 watt. RF voltage is 16 volt. Etching time is 2 minutes and 10 seconds.

11. FESEM inspection: Check the etching condition using FESEM and locate the tips' exposed region. If the tips are not exposed, perform procedures 10 and 11 until the tips are exposed. The major exposed area should be at the center of the sample. BCB thickness at the sample edge is always thicker than that at the center.

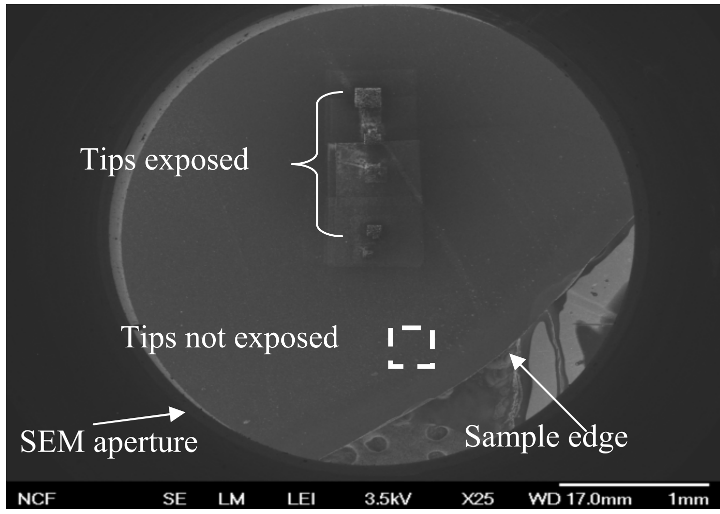
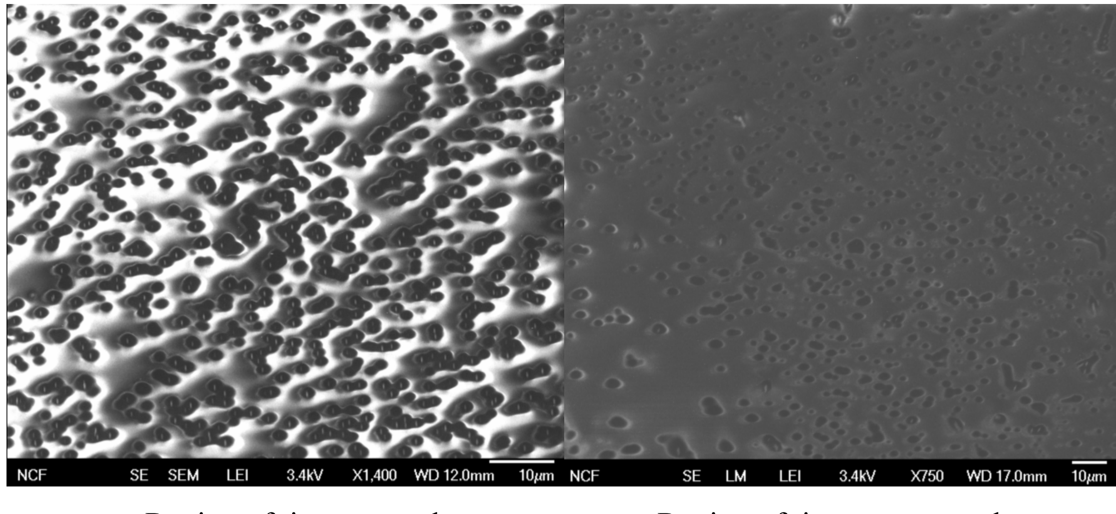


Fig. B.3: SEM picture of the NW sample after RIE process to expose the tips



Region of tips exposed Region of tips not exposed

12. ALD-W etching: Use copper etchant 49:1 (under the electroplating plating tank) to etch ALD-W for 1 minute and 30 seconds. Immerse the sample into DI water and then bake the sample at 70 °C for 2 minutes to dry the sample.

13. FESEM inspection: Inspect the etching condition of ALD-W using FESEM. Use FESEM to make sure that the ALD-W is etched away by the etchant.

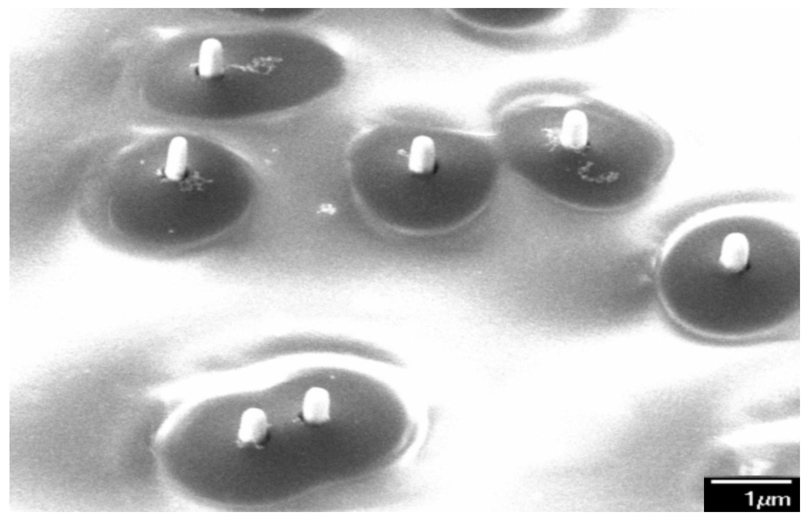


Fig. B.4: SEM picture of the NWs after the ALD-W etching process

14. Take a photo to remember the loading orientation of the NW sample in FESEM as shown in following picture. This helps us take the same orientation of the NW sample.

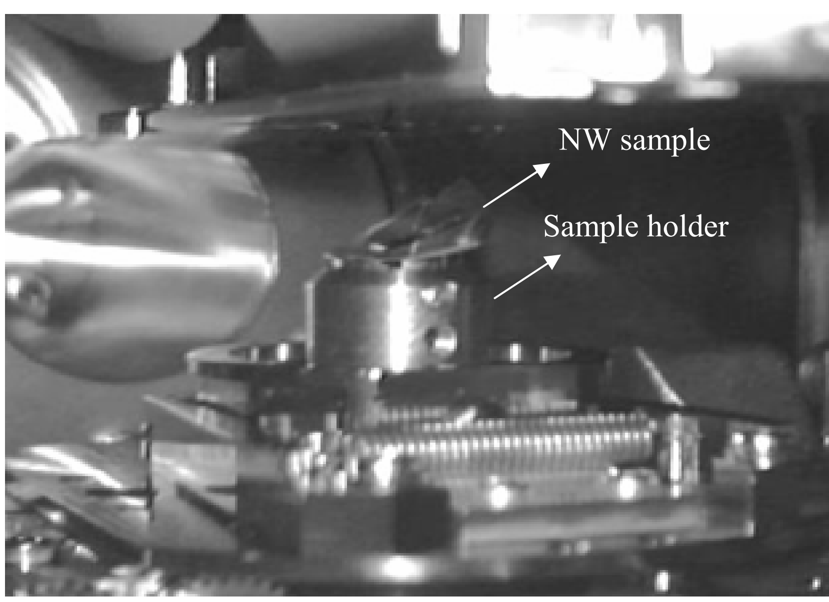


Fig. B.5: Picture of sample loading configuration in FESEM

15. Two methods can be used to check the etching process of ALD-W at tips: The first one is to etch the BCB thickness to expose the tip more, as shown in the following image; the second method can use EDX in FESEM to measure the material composition at the tip of the NW.

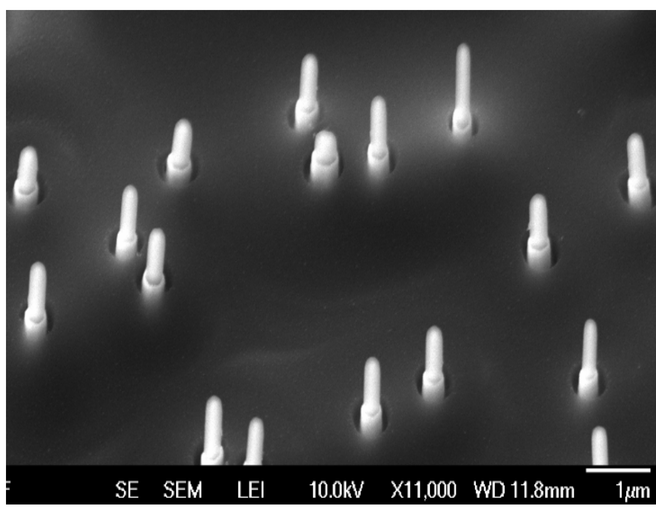


Fig. B.6: SEM picture of the NWs after the ALD-W etching process

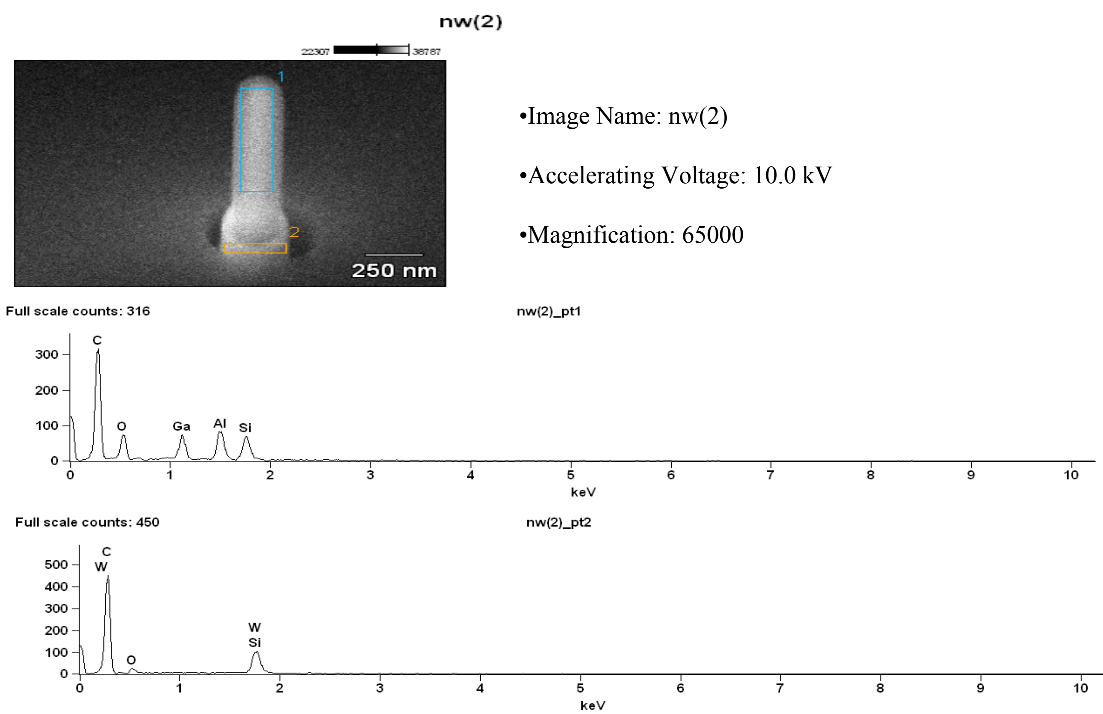


Fig. B.7: EDX analysis at the tip region of the NWs after the ALD-W etching process

16. Thick W deposition by a thin ALD-W with 31nm and then a thick sputtered-W as the top electrode. Sputtering recipe: Use DC-sputter in CNL for W sputtering for 10 minutes. Sputtering power is 120 watt. Pressure in chamber when sputtering: 5mTorr. Thickness monitor parameter: use 800 as material variable.

17. FESEM inspection: Inspect the NW sample after W sputtering as shown in the following SEM image.

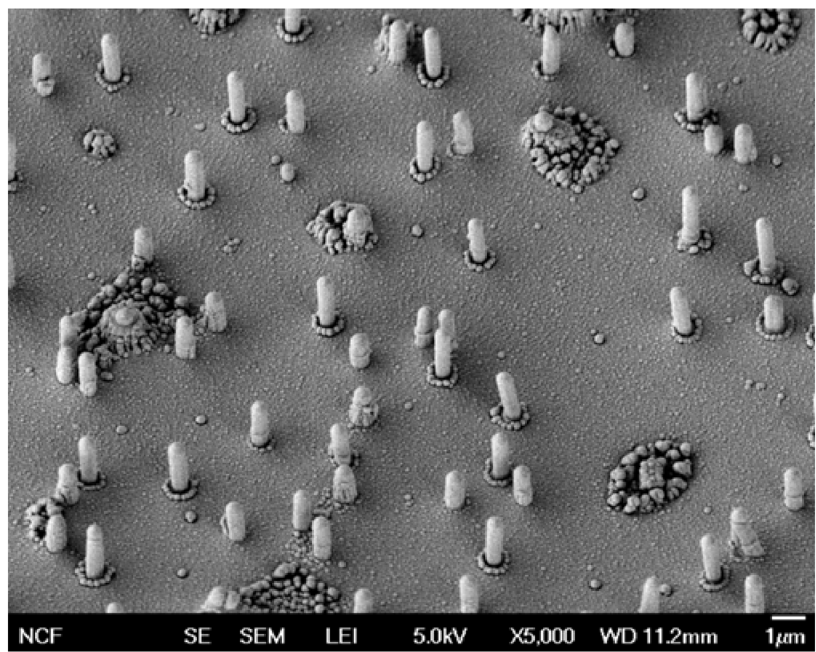


Fig. B.8: SEM image of the NWs after the ALD-W and sputtered-W deposition processes

18. Oxygen plasma treatment: Take the sample into the chamber of the plasma machine. Pump the chamber down to 0.5 mtorr. Open the valve of the oxygen tank and set the flow rate at 2 sccm. When the pressure is stable, turn on the RF power and set the RF power at 60 watt and the processing time at 40 seconds.

19. Second BCB spin-coating: Put the sample on the holder of the spin-coater. Drip 1-2 drops of BCB on the sample. Start spinning, and when the spinning rate reaches 3000 rpm (from the first step to the second step and reaches the spinning rate of the second step), stop spinning.

20. Soft-bake: 70 °C for 3 minutes.

21. UV exposure: 20 seconds.

22. Hard-bake: 100 °C for 10 minutes. Using the optical microscope to inspect the sample surface after coating (with BCB, the color is changed).

23. FESEM inspection: Use FESEM to inspect the second BCB coating on the NW sample as shown in the following SEM image. When BCB charging occurs, it means that the sample is coated with BCB.

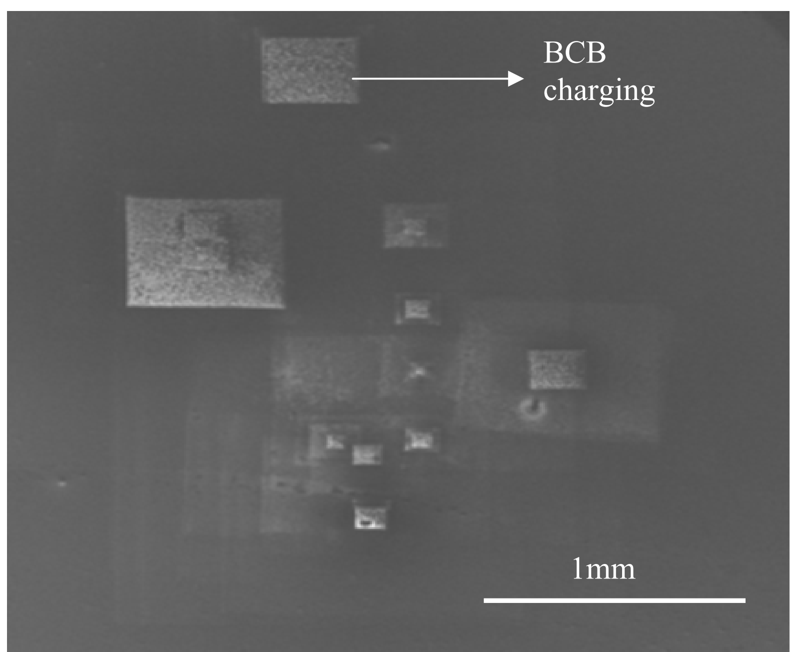


Fig. B.9: SEM image of the NW sample spin-coated with BCB

24. First RIE to reduce the thickness of the second BCB: RIE recipe (O_2 : CF_4 = 6 sccm: 4 sccm). RF power is around 348 watt. RF voltage is 18 volt. Etching time is 2 minutes and 5 seconds.

25. FESEM inspection: Use FESEM to inspect etching of the second BCB on the NW sample, as shown in the following SEM image. From the SEM image, we can check the exposed condition of the NW tips. If most of the tips are not exposed, perform RIE until the tips are exposed.

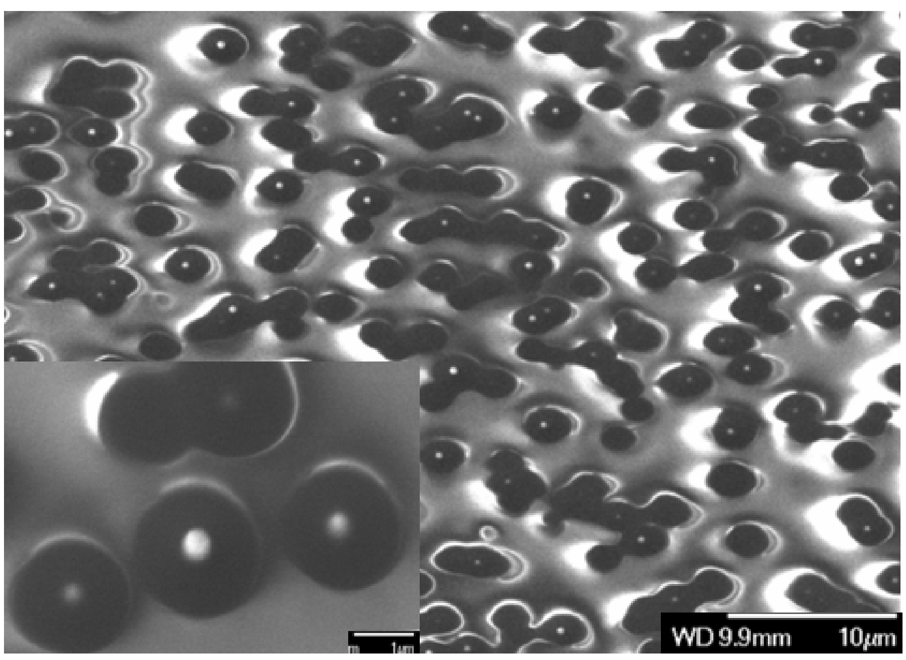


Fig. B.10: SEM image of the NW sample after the first RIE etching

26. Second RIE to reduce the thickness of the second BCB: RIE recipe (O_2 : CF_4 = 6 sccm: 4 sccm). RF power is around 343 watt. RF voltage is 16 volt. Etching time is 2 minutes.

27. FESEM inspection: Use FESEM to inspect etching of the second BCB on the NW sample, as shown in following SEM image. From the SEM image, we can check the exposed condition of the NW tips. If most of the tips are not exposed, perform RIE until the tips are exposed. From the SEM image below, the tips of the NWs are exposed more, but there are still some tips of the NWs covered by BCB (not exposed).

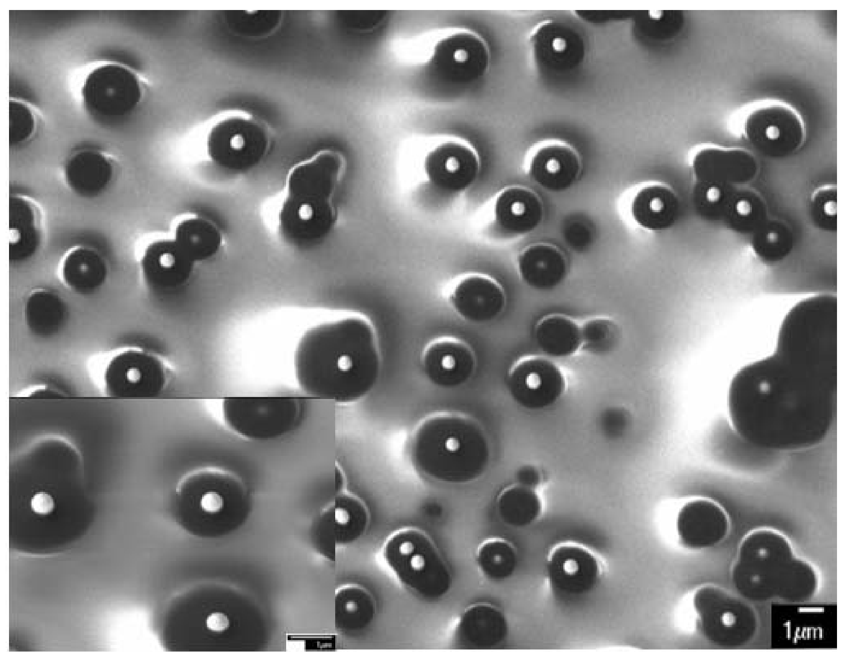


Fig. B.11: SEM image of the NW sample after the second RIE etching

28. Third RIE to reduce the thickness of the second BCB: RIE recipe (O_2 : CF_4 = 6 sccm: 4 sccm). RF power is around 348 watt. RF voltage is 18 volt. Etching time is 30 seconds.

29. FESEM inspection: Use FESEM to inspect etching of the second BCB on the NW sample, as shown in following SEM image. From the SEM image, we can check the exposed condition of the NW tips. Most tips of the NWs are exposed from the SEM image below.

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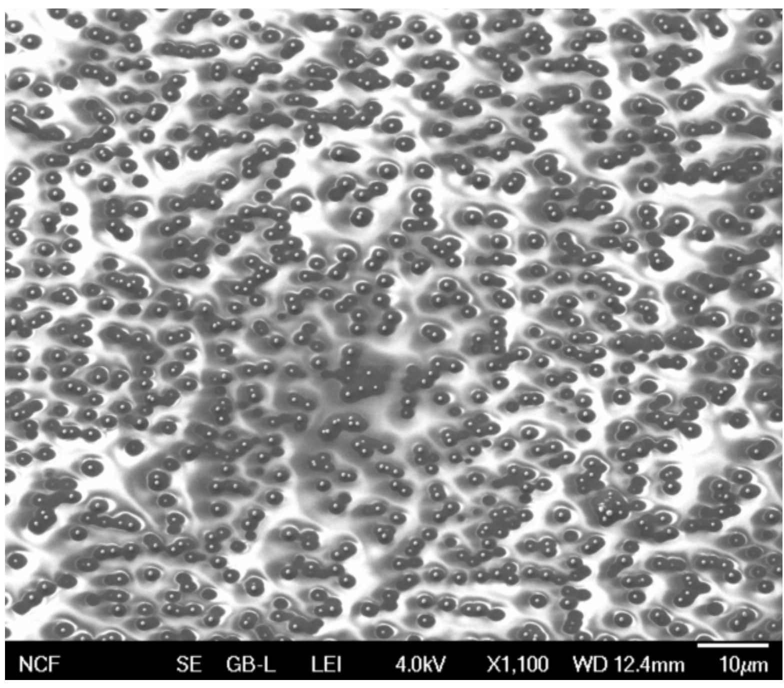


Fig. B.12: SEM image of the NW sample after the third RIE etching

30. First W etching: Use a copper etchant to etch W at the tips of the NWs. The first W-etching time is 1 minute. Then bake the sample at 70 °C for 2 minutes.

31. FESEM inspection: Use FESEM to inspect W etching result, as shown in following SEM image. From the SEM image, we can check the etching condition of W at the NW tips. Most W at the tips of the NWs are etched from the SEM image below. Since the lengths of each NW are different, there are still a few NWs whose tips are not exposed.

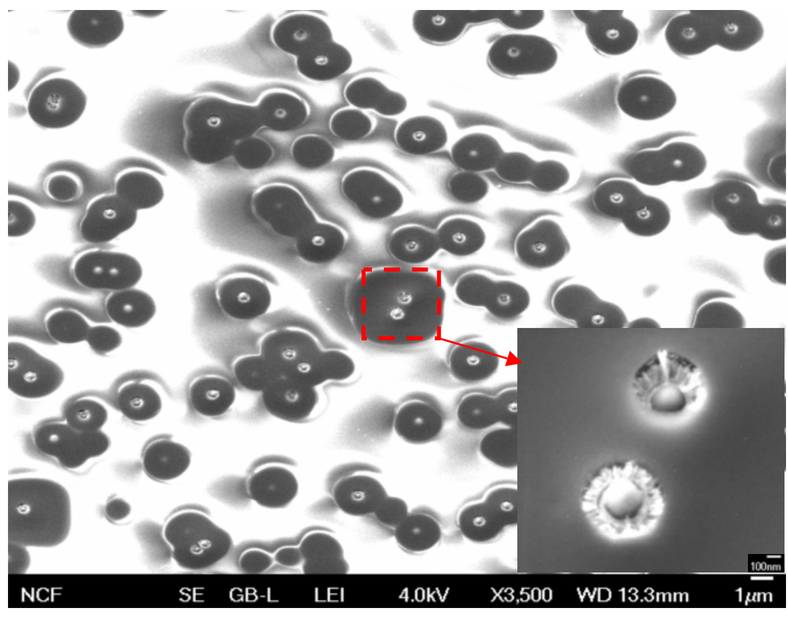


Fig. B.13: SEM image of the NW sample after the first W etching

32. Second W etching: Use a copper etchant to etch W at the tips of the NWs. The second W-etching time is 35 seconds. Then bake the sample at 70 °C for 2 minutes.

33. FESEM inspection: Use FESEM to inspect W etching result, as shown in following SEM image. From the SEM image, we can check the etching condition of W at the NW tips.

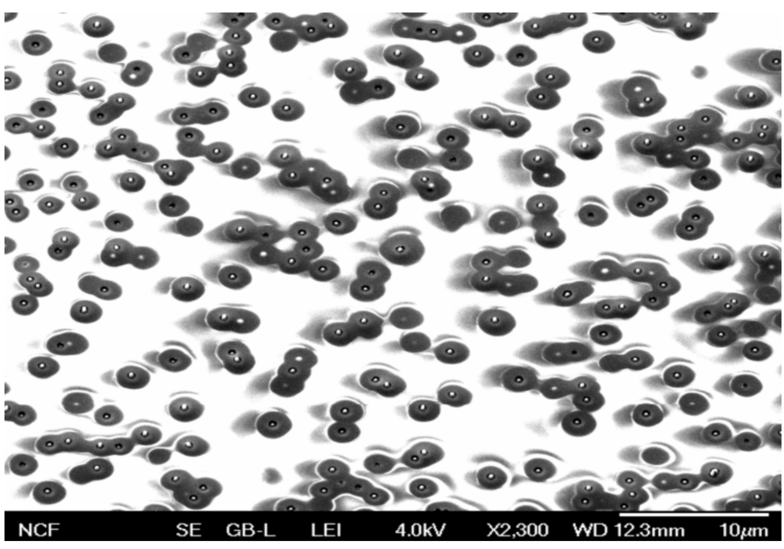


Fig. B.14: SEM image of NW sample after second W etching

33. First RIE to remove BCB: RIE recipe (O_2 : CF_4 = 6 sccm: 4 sccm). RF power is around 348 watt. RF voltage is 17 volt. Etching time is 4 minutes.

34. FESEM inspection: Use FESEM to inspect BCB removal, as shown in following SEM image. From the SEM image, we can check the etching condition of BCB.

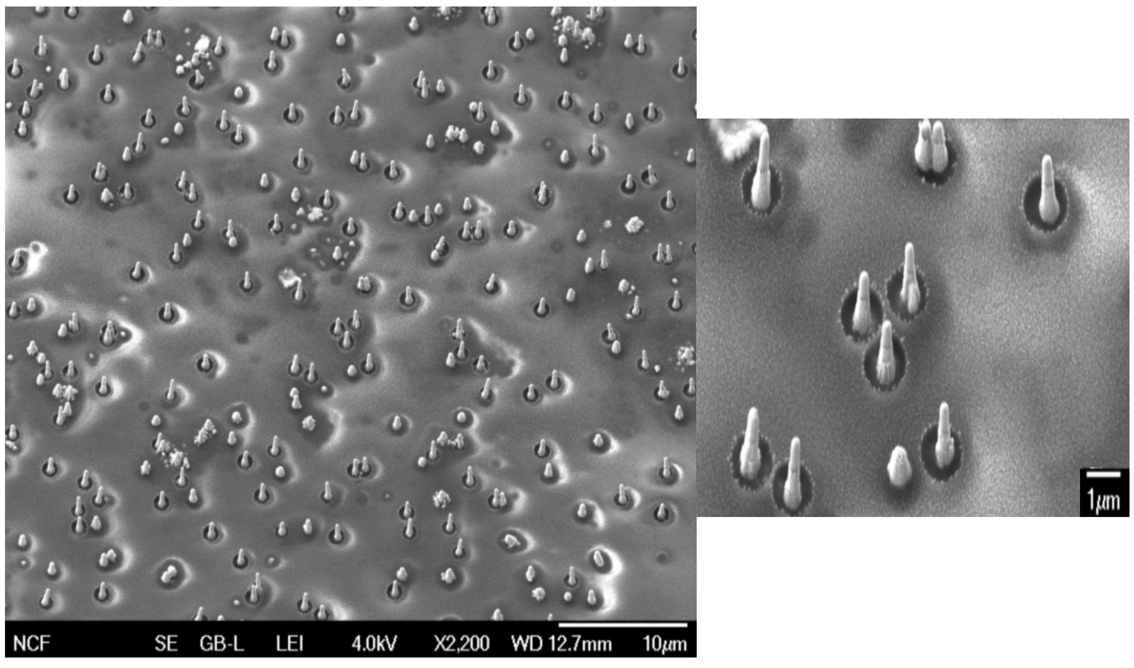


Fig. B.15: SEM image of the NW sample after the first BCB etching

33. Final RIE to remove BCB: RIE recipe (O_2 : CF_4 = 6 sccm: 4 sccm). RF power is around 348 watt. RF voltage is 17 volt. Etching time is 4 minutes.

34. FESEM inspection: Use FESEM to inspect BCB removal, as shown in following SEM image. From the SEM image, we can check the etching condition of BCB. Control of etching time is very important to prevent the top W from RIE etching.

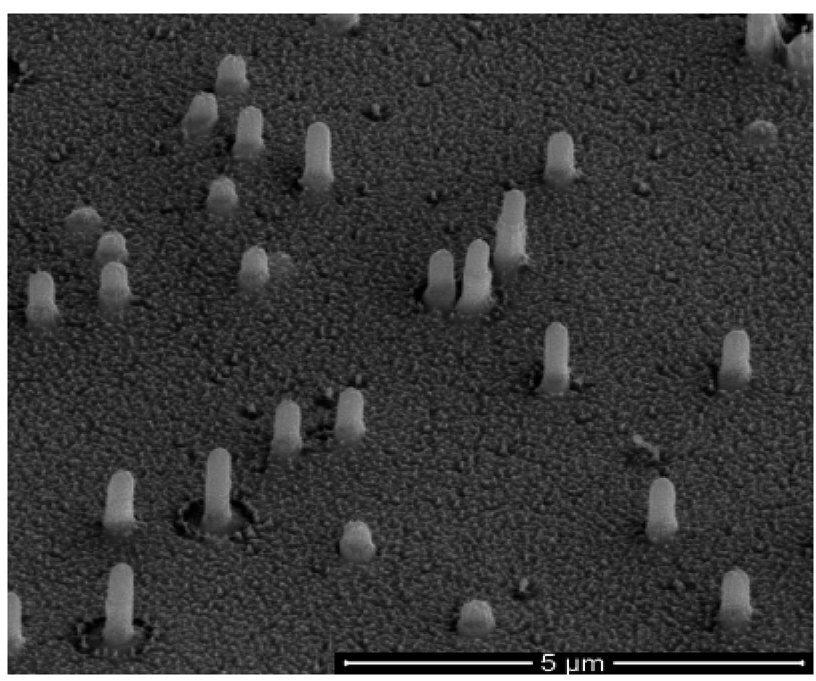


Fig. B.16: SEM image of the NW sample after the final BCB etching

Appendix C

Method to Determine Peak PL Wavelength

In this study, we used PL peak wavelength to represent the bandgap of GaN nanowire at corresponding temperature. Peak wavelength has the highest luminescence emission and is the best location for representing the bandgap of as-grown GaN nanowire. Fig. C.1 shows the raw PL data measured from a bare as-grown NW sample at 23 ºC. The range of wavelength measurement is from 325.32nm to 408.44nm, and 1044 pixels in processed spectrum are recorded in one measurement. It shows that the peak location is difficult to be determined because of the wavelength fluctuation at the peak region. The method to determine peak PL wavelength is important to temperature-to-wavelength sensitivity in temperature dependence of the peak PL wavelength. In this study, we have compared three methods – direct pickup of wavelength with maximum intensity, weighted mean, and quadratic fit – to determine PL peak wavelengths in terms of temperature-to-wavelength sensitivity.

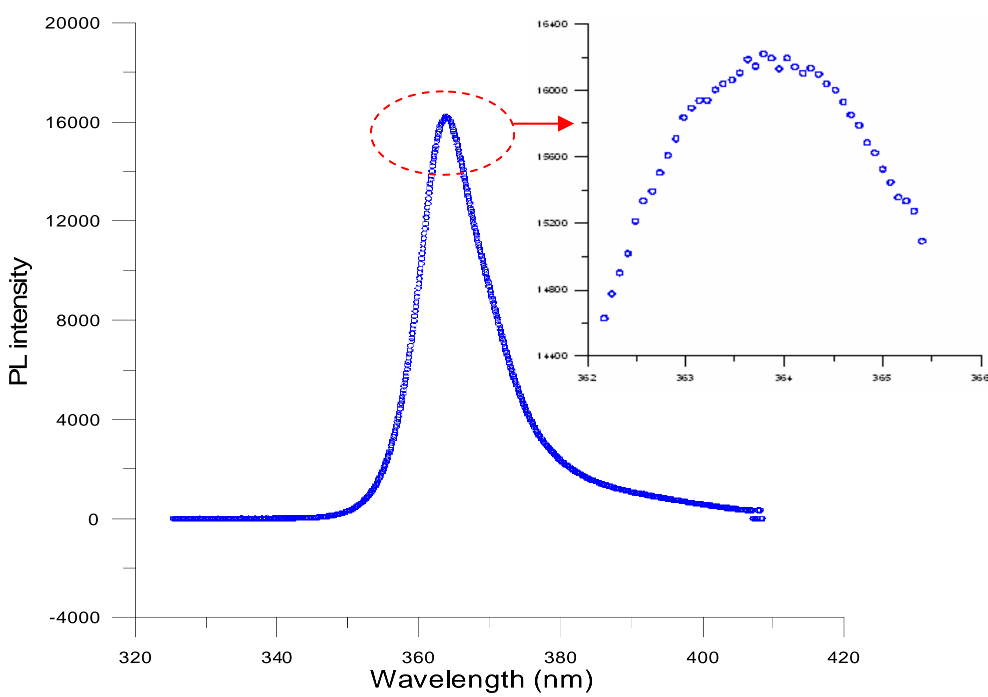


Fig. C.1: Raw PL data of GaN NWs measured at 23 ºC. Inset: magnified view of PL data at peak location.

Fig. C.2 shows the comparison of temperature dependence of PL peak wavelengths determined by these three methods. At one temperature condition, we recorded six data for making one error bar. The peak wavelength determined by a weighted mean has less uncertainty (error bar); however, the temperature-to-wavelength sensitivity is smaller than that in the other methods. Direct pickup of the peak wavelength with the maximum luminescent intensity demonstrates good temperature-to-wavelength sensitivity, but the uncertainty is larger than others. A quadratic fit using data close to the raw peak is finally chosen in this study to determine the peak PL wavelengths because this method gives less uncertainty and better temperature-to-wavelength resolution.

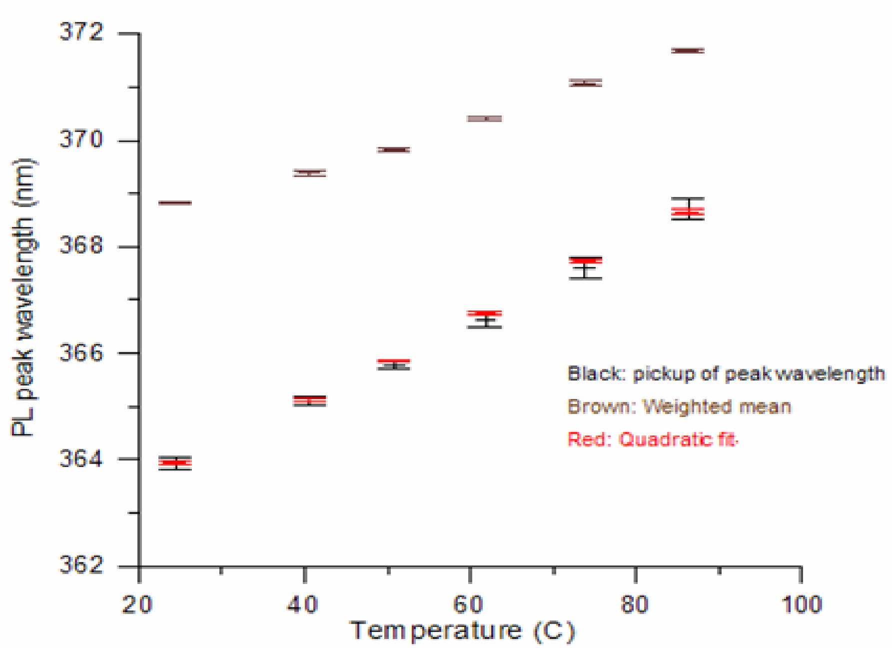


Fig. C.2: Comparison of temperature dependence of the PL peak wavelength determined by direct pickup of peak wavelength (black), weighted mean (brown), and quadratic fit (red).

Matlab code for peak PL wavelength chosen by using different methods

```
clear;

clc;


indx=[];

maxwave=[];

weightcenter=[];

weightcenter61=[];

mean60=[];

qudrfit=[];

fitgoodness=[];

indx2=[];

date=[];

temperature=[];


for i=1:6

name=['dataset' num2str(i) '.txt']


data=load(name);


% ========================================

% data_temp=load(name);

% data=data_temp(2:length(data_temp),:);

% date=[date; data_temp(1,1)];

% temperature=[temperature; data_temp(1,2)];

% ========================================
```

```
 indx=find(data(:,2)==max(data(:,2)));
indx2=[indx2; indx]
maxwave=[maxwave; data(find(data(:,2)==max(data(:,2))),1)];  %max wavelength (nm)
weightcenter=[weightcenter; sum(data(:,1).*data(:,2))/sum(data(:,2))]
weightcenter61=[weightcenter61; sum(data(indx-20:indx+20,1).*data(indx-20:indx+20,2))/sum(data(indx-
20:indx+20,2))];
mean60=[mean60; mean(data(indx-20:indx+20,1))];
datax=data(indx-20:indx+20,1);
datay=data(indx-20:indx+20,2);
[fresult,gof]=qudratic_fit2(datax,datay);
qudrfit=[qudrfit; fresult.b]
fitgoodness=[fitgoodness; gof.adjrsquare]


end
csvwrite('test2.csv',[date indx2 maxwave weightcenter weightcenter61 mean60 qudrfit fitgoodness])
```

Appendix D

Application of Tip Photoluminescence Measurement for Tip Temperature Measurement

In Chapter 2, we studied and eliminated the matrix effect by covering the ALD-W on it. The elimination of the matrix gives us an opportunity to measure NW-only PL signals. This section presents an application of temperature dependence of NW-only PL peak wavelength. The dependence was employed to predict real-time NW temperatures. To eliminate luminescence from the GaN matrix layer, we prepared an ALD-W-coated GaN NW sample encapsulated with electroplated copper. Electroplated copper, functioning as the effective cooling material for as-grown NWs, was used to encapsulate NWs and cover the matrix for temperature measurement. Our processing steps are illustrated as follows. We started with GaN NWs, as seen in Fig. D.1. Each wire had to be electrically isolated but thermally conducted to copper. An extremely thin ALD-alumina (50nm) covered each wire with a pinhole-free dielectric layer. This layer was then covered by ALD-tungsten (40nm) for a good copper contact (Fig. 5a). The adhesion (Ti:30nm) and electroplating seed layers (Cu:250nm), were deposited on the NWs by the evaporation process, as shown in Fig. 5b. At the end, the GaN NWs were fully encapsulated with copper after the electroplating process (Fig. 5c). The tips of the NWs were exposed for the interconnect or other functional integration after the copper etching process (Fig. 5d). The GaN matrixes were fully covered by ALD-W and copper after the fabrication process.

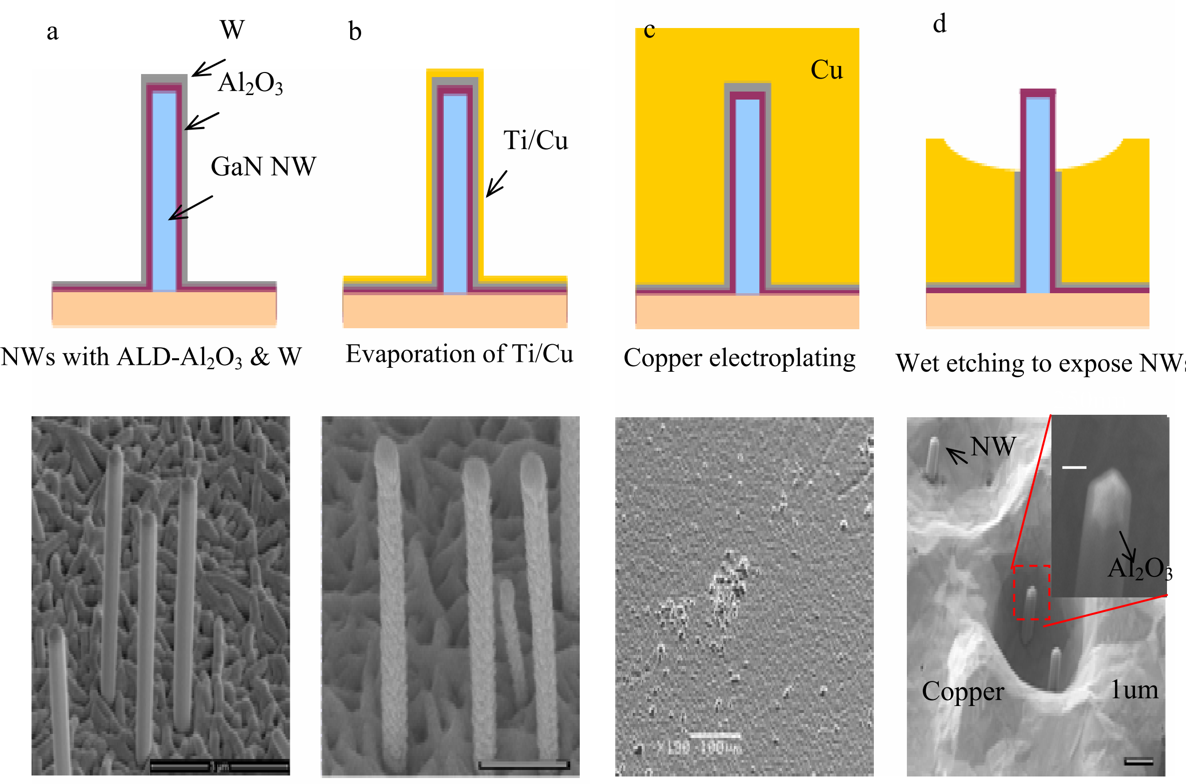


Fig. D.1: Schematic drawings and corresponding experimental results of the copper encapsulation process

The copper-encapsulated NW sample was placed on the TE device in the experimental setup of Fig. 2.10. To obtain the temperature dependence of the PL peak wavelength, we heated the NW sample by changing the input power of the TE device and recorded corresponding PL signals at different surface temperatures of the TE device. Figure 6a shows the temperature dependence of the PL peak wavelength and data were fitted by a linear equation with the least squares method. The parameters α=0.083 and β=360.6 gives the best fit in the fitted equation, $\lambda = \alpha \mathrm{T} + \beta$, where λ is the PL peak wavelength and T is the temperature of the NW in centigrade. The fitted linear equation was used as a calibration equation for the NW temperature

measurement. The temperature of the NWs can be determined by measuring its PL peak wavelengths. Figure 6b shows the real-time PL measurements of copper-encapsulated NWs. We recorded PL peak spectra with time intervals of 10 and 6 seconds when the TE device was operated from 0V to 7.5 and 9V, respectively. With temperature dependence of the PL peak wavelength, the temperature and corresponding thermal performance of as-grown NW devices can be characterized in real time.

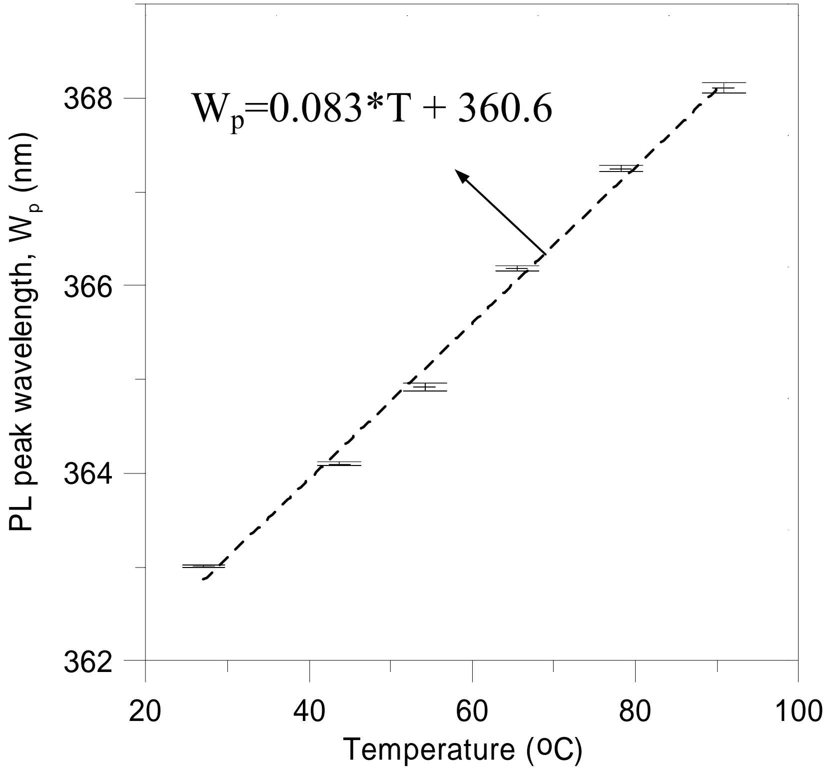


Fig. D.2: Temperature dependence of PL peak wavelength. At one TEC temperature condition, we record six measurements and make one error bar with one standard deviation.

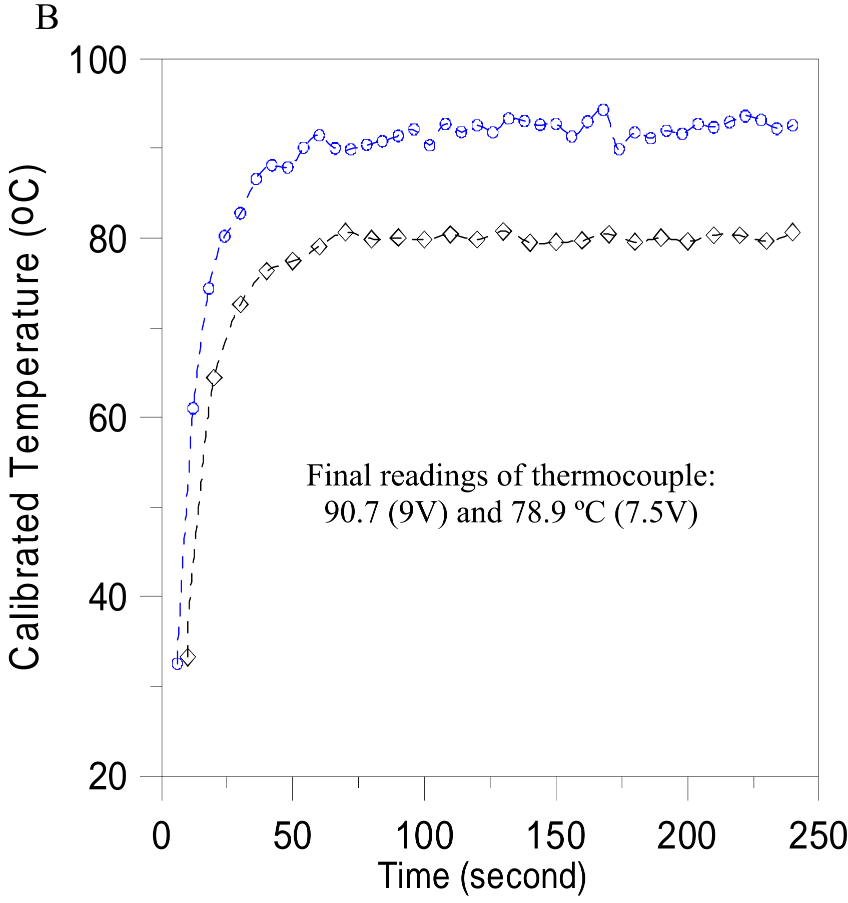


Fig. D.3: Real-time PL measurement at TEC input voltage from 0V to 7.5V (diamond in black) and 9V (square in blue), respectively. Final readings of thermocouple: 90.7 ºC (0~9V) and 78.9 ºC (0~7.5V).

Appendix E

Spatially Resolved PL Measurement

Spatially resolved PL measurement is conducted to confirm the measured PL from the tips of NWs. One NW is dispersed on fused silica. CW HeCd excitation light is focused on a 1-um spot at the center of a 12-um-long NW. PL light is collected without additional spatial restriction and through a pinhole placed in the image plane at one wire end. The light collected from the wire end is red-shifted relative to the spatially unfiltered PL, as shown in Fig. E.1. This shift is accompanied by no significant line narrowing. We attribute this red shift to band-edge reabsorption. PL collected from the NW end traverses more material as it is waveguided down the length of the wire.

With the local ALD-W etching process, PL light can be measured. No additional blue shift is observed. If the measured PL originates from anywhere but the tip region, red-shifted PL spectra due to band-edge reabsorption would be expected. This is not the case, and this PL result on the as-grown NW sample is, therefore, consistent with the single-wire spatially resolved PL measurement.

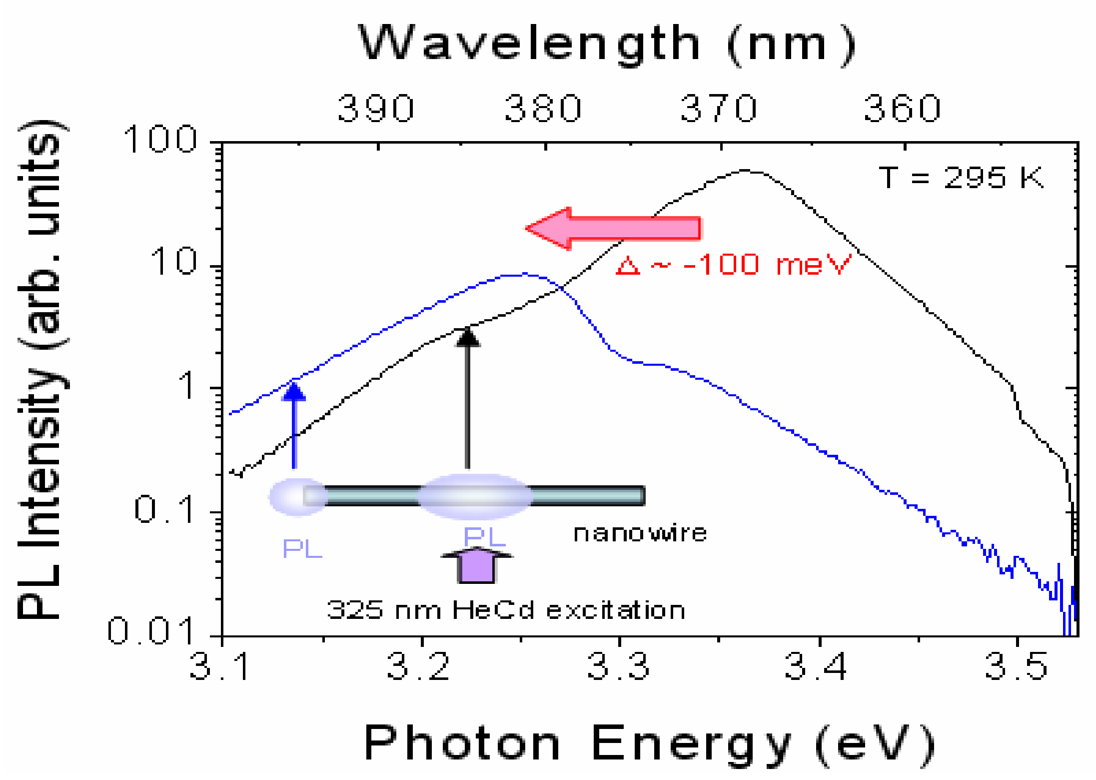
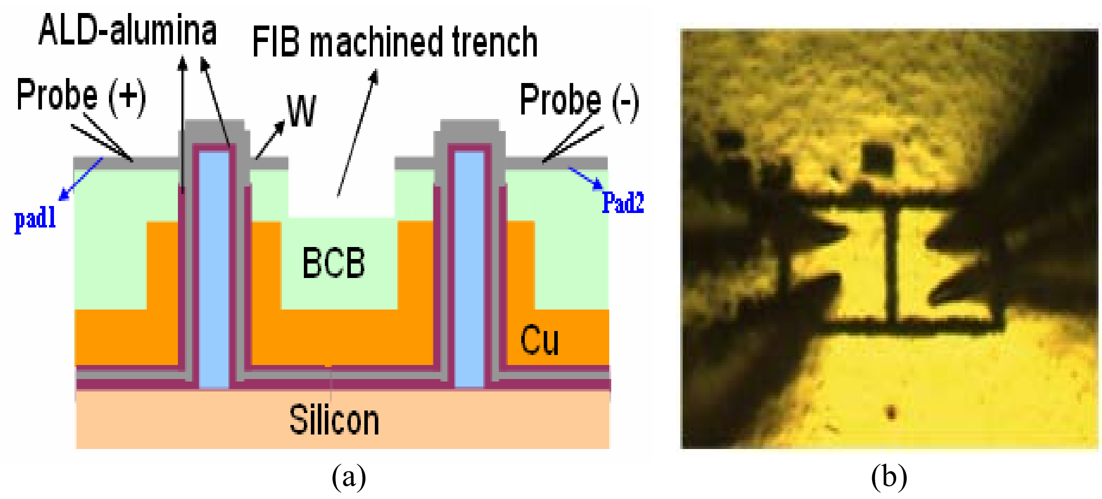


Fig. E.1: Spatially resolved PL measurement on one nanowire dispersed on fused silica.

Appendix F

Interconnection of Metallization along Cooling-Enhanced As-Grown NWs

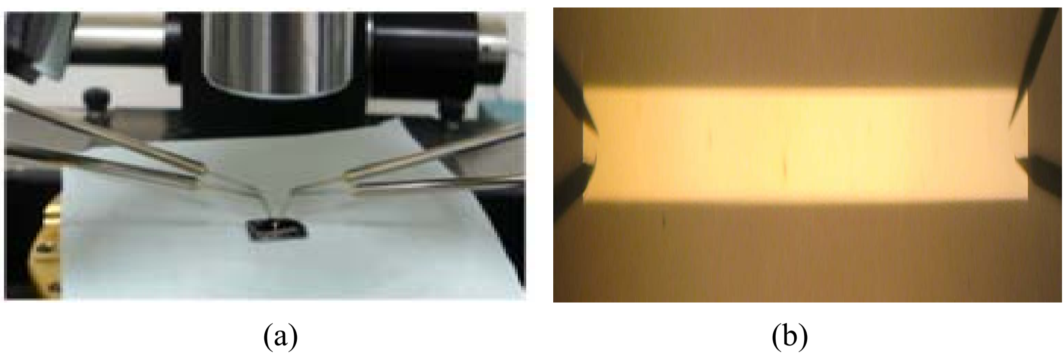
In spite of the excellent capability of ALD technology in conformal coverage and precise thickness control, the extreme aspect ratio of NWs could decrease the electrical conduction of the ALD-W layer. Interconnection of copper-encapsulated NWs interconnected with the tip covered has been verified by four-probe resistance measurement. By measuring electrical resistance of the ALD-W layer, one can know if the ALD-W is able to interconnect the NWs and how good the conductivity of the ALD-W layer is. Two metal pads were fabricated by FIB machining, as shown in Fig. F.1. As illustrated in Figure F.1a, metal pad 1 and pad 2 are separated by FIB machined trench but electrically connected through the ALD-W interconnect on the NWs and base matrix layer.



(a) (b)

Fig. F.1: (a) Schematic drawing and (b) photo of the experimental setup of the four-point resistance measurement. Metal pads were fabricated by FIB machining.

Resistivity of the ALD-W layer deposited on a flat glass substrate was measured (Figure F.2) and used as the reference value for the comparison with the NW sample. The experimental images are shown in Fig. F.2.



(a) (b)

Fig. F.2: (a) Probes on the sample with the ALD-W layer for the four-probe measurement. (b) Magnified photo of the four-probe resistivity measurement of the ALD-W layer on glass as a reference sample.

Samples B, C, and D in Fig. 3.11 were measured in the experiment. The number of the GaN NWs inside the pad area were counted and used for the resistivity calculation. At each pad, parallel electrical resistance was calculated in terms of the number of NWs. Two pads were then calculated as serial resistance. It should be noted that the resistance of the base matrix layer was ignored for simplicity of the calculation. Thus, there was a difference in resistivity between the NW samples and the reference (ALD-W on glass) by the factor of two. The difference may be attributed to (1) complicated geometry of ALD-W on the base matrix layer or (2) oxidation of the ALD-W layer during the BCB curing procedure. Table F.1 summarizes these measurements. It is clear that ALD-W on a NW is successfully interconnected to the top electrode, and the interconnection is good.

Table F.1: Resistivity of ALD-W on copper-encapsulated NWs and of ALD-W on glass by four-probe measurement.

Sample (neglect matrix and top electrode resistance)		Resistance (ohm)	Resistivity (ohm cm)
ALD-W metallization along NWs (Cu-encapsulated sample)	(B) Pad size: 30x30 (um^2); NW number: 62, 60	20.57	4.17E-04
	(C) Pad size: 40x40 (um^2); NW number: 147, 159	8.08	4.03E-04
	(D) Pad size: 40x40 (um^2); NW number: 141, 114	13.3	5.48E-04
ALD-W on glass			2.60E-04