Microfabricated Broadband Components For Microwave Front Ends

by

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Cullens, E. D. (Ph.D., Electrical Engineering)

Microfabricated Broadband Components For Microwave Front Ends

Thesis directed by Prof. Zoya Popović

Broadband components for microwave and millimeter-wave RF front ends enable increased flexibility and functionality, such as using one front end for multiple electronic warfare frequency bands or using frequency scanning to electronically steer the main beam of a radar array. This thesis explores the usefulness of a sequential copper deposition, microfabrication process known as the PolyStrata^{TM} process for broadband passive elements in two frequency ranges: 4-18 GHz and 130-180 GHz.

The 4-18 GHz band research focuses on taking advantage of the low loss, low dispersion, high isolation, and relatively high power handling capability of the PolyStrata^{TM} process by enabling passive parts of a MMIC to be moved off chip, thus saving expensive semiconductor wafer area. Specifically assembly structures referred to as sockets, inductors, and bias tees are designed, fabricated, and tested as a means of hybridly integrating MMICs, SMDs, and Polystrata^{TM} lines. Measured data is in agreement with full-wave simulations and shows that PolyStrata^{TM} integration introduces minimal parasitics and is therefore an attractive packaging technology.

The 130-180 GHz band research focuses on taking advantage of the accuracy and tight tolerances of the PolyStrata^{TM} process to make frequency-scanning, traveling-wave, slotted waveguide arrays at G-band using a WR-05 compatible PolyStrata^{TM} waveguide. The array achieves scanning greater than 1°/GHz, and more than 20° steering with less than 15% fractional bandwidth. The a 20-element slot array has a beamwidth of 6.3° near the center of the band (150 GHz). The array is 2 cm in length, has a mass of approximately 0.063 mg, can be connected to standard waveguide, and is scalable to a 2-D array.

Dedication

To my parents and grandparents, for their love, support, and examples to which I aspire.

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Chapter 1

Introduction

The topic of this thesis is broadband microfabricated microwave circuits in the 4-18 GHz frequency range and millimeter-wave scanning antennas at G-band (130-180 GHz). The lower frequency components have applications in electronic warfare and for RF front ends where multiple applications can be served by the same hardware. Figure 1.1 shows a microfabricated broadband power amplifier in which the passive part of the circuit is implemented in micro-coaxial lines which have the following advantageous properties over standard technology:

(1) low loss (measured 0.1dB/cm up to 40 GHz [1, 2]),

(2) low dispersion (TEM mode dominant up to 400 GHz for 250-μm diameter 50-ohm lines [3, 4]),

(3) wide range of characteristic impedances (8-120 ohms [5]),

(4) very high isolation (-60 dB for lines sharing a common shield wall [2, 6]), and

(5) relatively high power handling capability (53 W at 2.5 GHz [5] and more recently 100 W CW at S-band [7]).

For broadband transmitters, power combining networks need to have low loss and low dispersion, as well as the ability to be integrated with active devices while maintaining low parasitics. In addition, a MMIC generally has less than 5% of its area dedicated to active components, as shown in Figure 1.2 [8]. Therefore, the integration of passive components realized in the PolyStrata^{TM}

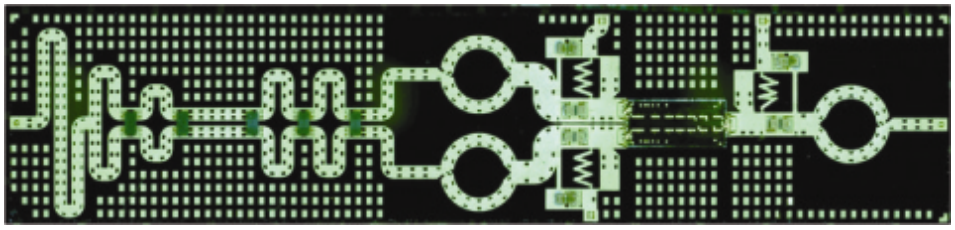


Figure 1.1: Photograph of a 6mm GaN power die composed of two 3mm strings. The input signal is divided in PolyStrata^{TM}, then fed to each string on the die separately. The combined output then leaves the die and goes back to the PolyStrata^{TM} environment.

process with active devices from wafers that can cost in excess of $30,000 represents a substantial step forward in circuit design, both in how effectively the wafer's area is used and in how well the composite circuit performs, since rectangular coaxial lines in the PolyStrata^{TM} process have lower loss, lower dispersion, and higher isolation enabling higher packing densities than either microstrip or CPW.

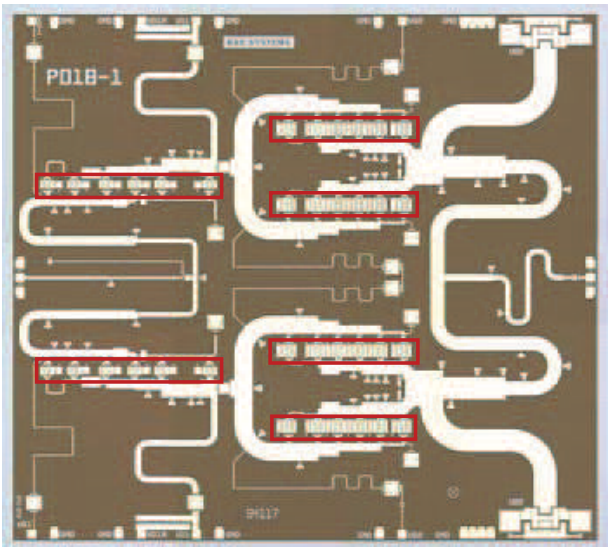


Figure 1.2: A wide-band power MMIC whose transistors are highlighted in red. Only 2% of the chip's area (8 mm x 8 mm) is occupied by the active devices.

To meet the technical goal of migrating passive components off of MMICs operating from 4-18 GHz, the research presented in this thesis addresses design of assembly structures for active

and passive component integration, monolithic high current handling inductors for biasing, and off-chip broadband bias lines enabling reduction of overall chip size.

Reduction in overall size for RF front ends can also be done by moving higher in the frequency spectrum. In the 130-180 GHz band, the size and weight (mass) of microfabricated waveguide components is very small and ideally suited for spaceborne applications. The application motivating the G-band work in this thesis is a landing radar for planetary missions [9, 10], as shown in the conceptual drawing of Figure 1.3.

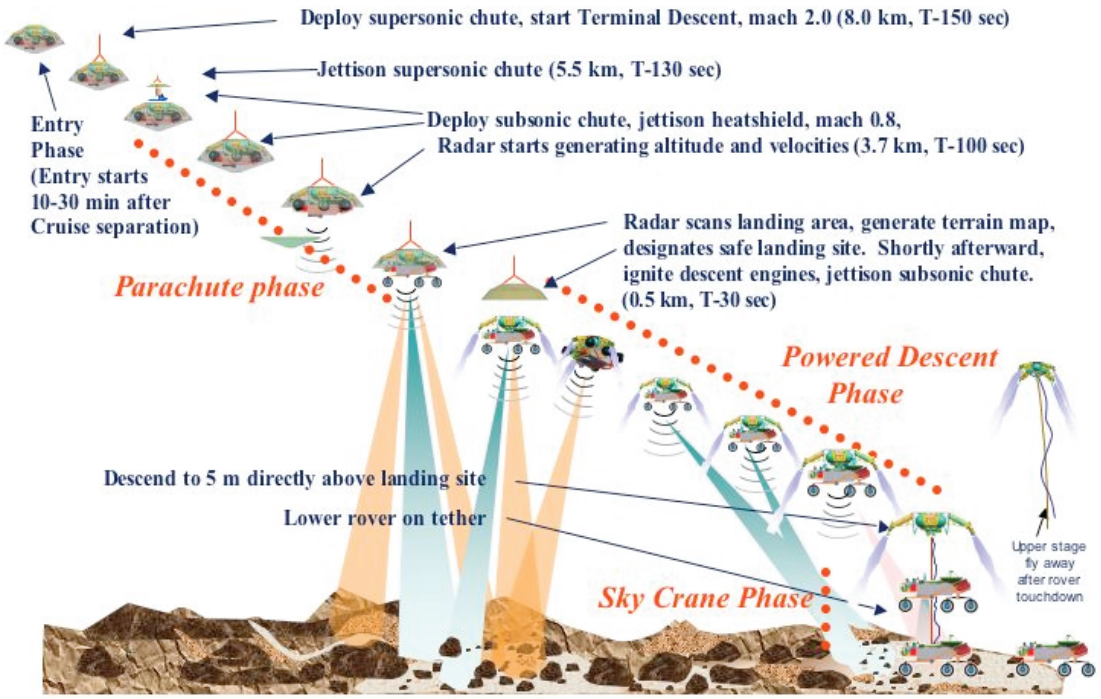


Figure 1.3: Conceptual drawing of how future planetary explorers may be delivered via a deployment system known as the "Sky Crane" [10].

Though such a radar would have limited application on Earth due to atmospheric absorbtion as shown in Figure 1.4, many planets (Mars in particular) do not have a significant atmosphere, and thus the band is not heavily attenuated. At millimeter-wave frequencies, coax would become

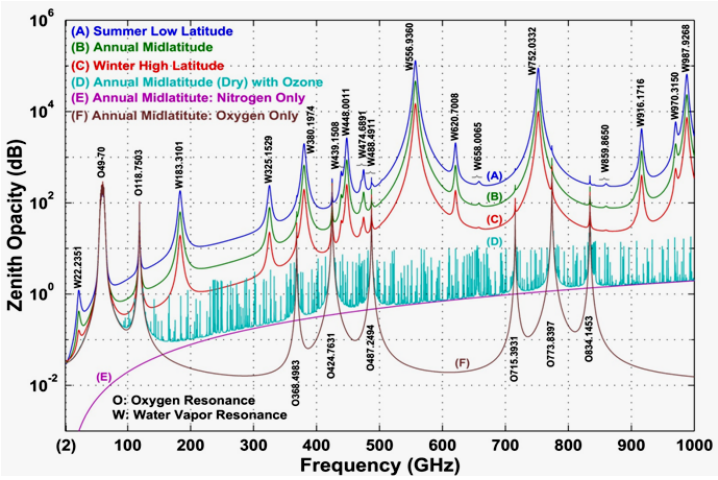


Figure 1.4: Zenith opacity, which relates to atmospheric attenuation as reported by Klein and Gasiewski [11].

too lossy, but waveguide can be fabricated in the same high accuracy process used for the coaxial lines of Figure 1.1. A few examples of G-band microfabricated waveguide components are shown in Figure 1.5. Since there are few active solid-state devices that operate in this frequency range, a standard phased array antenna with phase shifters is currently not possible due to lack of phase shifters with acceptable loss. Therefore, the approach taken in this work for beam steering is traveling-wave, frequency scanned, slotted waveguide arrays.

1.1 PolyStrata^{TM} Microfabrication Technology

The PolyStrata^{TM} process involves sequential deposition of copper layers and photoresist on an optically-flat surface, typically a silicon wafer. In the case of rectangular coaxial lines, the inner conductor is supported by dielectric straps, while waveguide has no straps. Once all the strata are deposited, the photoresist is dissolved ("released") through periodic gaps in the copper ("release holes") leaving an air-filled coaxial line or a hollow waveguide. This process is illustrated in Figure 1.6.

A complicated process such as this has several requirements and guidelines. First of all, copper layer thicknesses range from 10 μm to 100 μm, with gap-to-height and width-to-height aspect

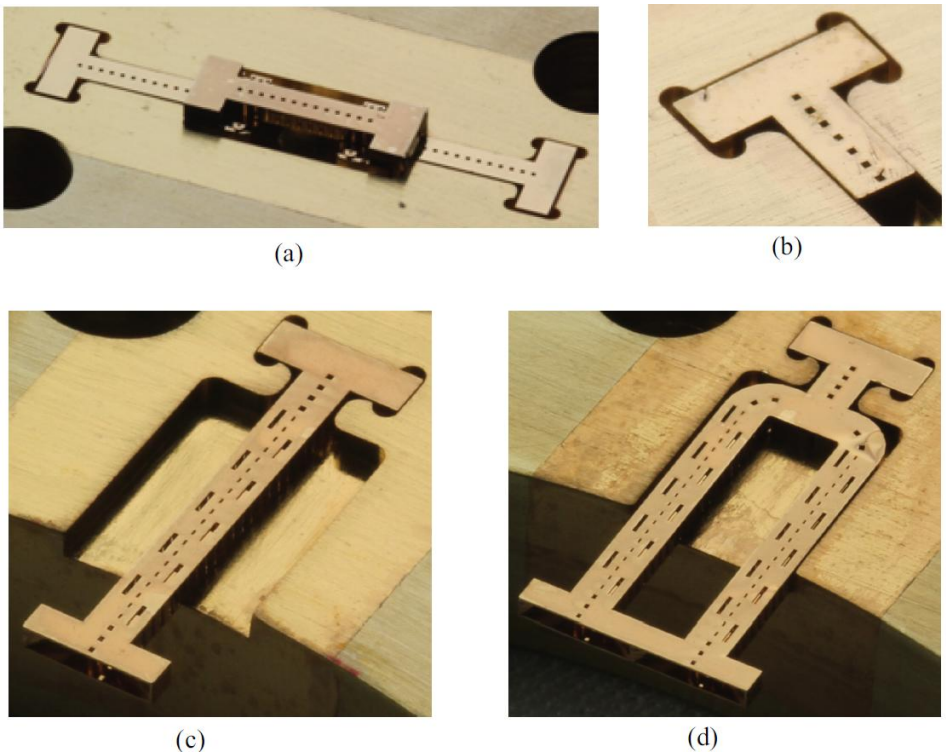


Figure 1.5: Assorted G-band waveguide components that can be microfabricated in the PolyStrata^{TM} process. All components are affixed to brass to allow mating to standard WR-05 flanges. The length of the array in (c) is 1.43 cm.

ratio limits of 1:1.2 and 1:1.5, respectively (the guideline is a 1:1 ratio for both gap-to-height and width-to-height aspect ratios). Furthermore, any single section of copper should have a footprint of at least 15000 μm^2, or in the case of a vertical column, a minimum diameter of 150 μm. In rectangular coax, the release holes and dielectric straps have a standard periodicity of 700 μm, where dielectric straps have a length of 100 μm and release holes have dimensions 200 μm x 200 μm. In waveguide, top release holes are 200 μm x 200 μm, side release holes are 200 μm x 675 μm, both with a periodicity of 500 μm. The last requirement is that prior to electroplating the copper, a metallization must first exist. For many strata, there will be copper in a lower stratum which allows the electroplating to occur. However, for all copper on strata 1 and often for copper on subsequent strata, gold "seed" layers must first be grown to allow the copper to be electroplated. Each gold seed layer adds complexity to the manufacturing process, and thus potentially reduces the yield

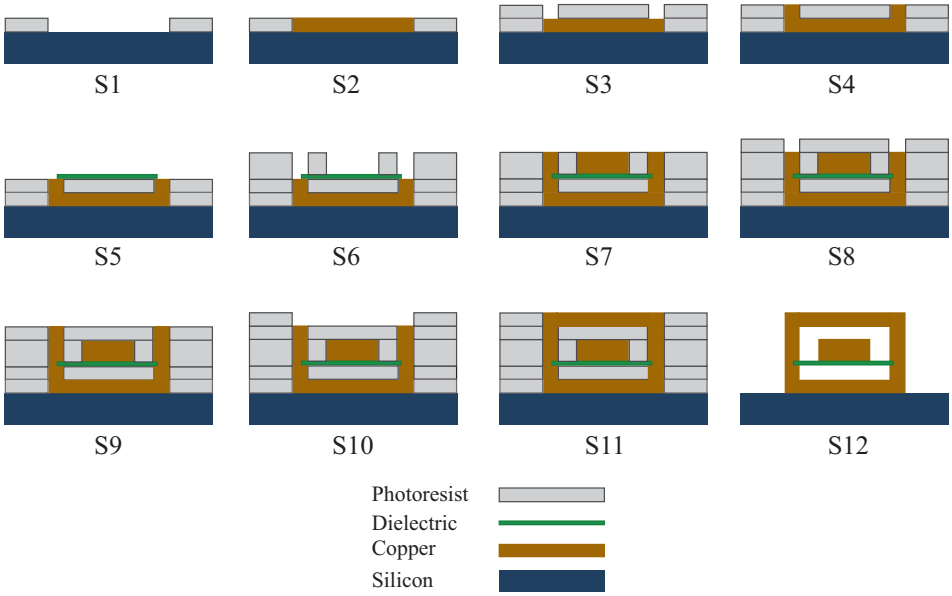


Figure 1.6: Graphical explanation of the PolyStrata^{TM} process for a 5-layer micro-coaxial line. In the first step photoresist is applied and patterned on the silicon wafer with a mask. Next, a uniform copper layer is electroplated on the wafer and then planarized. The same steps are repeated to grow the structure. In order to support the inner conductor, dielectric straps are embedded into the sidewalls through photopatterning. Steps 1 - 5 are repeated to complete the structure. With this method up to 15 independent layers can be made. The last step is releasing the photoresist to complete the fabrication of an air-filled micro-coaxial line [12].

that a fabrication run will have. As such, the location of gold seed layers are to be minimized, and are often chosen by the foundry. This has the effect of limiting geometry choices which may impact design, e.g. the conical inductor discussed in Chapter 3 may not be possible and certain characteristic impedances, discussed below in Section 1.2, may not be available either.

These requirements play roles throughout the designs in this thesis. In Chapter 2, aspect ratio and minimum footprint requirements limit structural support geometry affecting where the supports can be placed and to what extent the parasitics (generally capacitance) introduced by their presence can be minimized. In Chapter 3, the minimum diameter of vertical columns and aspect ratio requirements govern how thin the inductor windings may be and thus affect inductance. In Chapter 5, release holes size and periodicity must be accounted for in order to ensure that the waveguide is functioning as intended.

Despite the requirements on design, the flexibility offered by the PolyStrata^{TM} process enables unconventional thinking by the designer. The outer conductor and inner conductor may be shaped at will, which enables circuit element design (in Chapter 3) and antenna design (in Chapter 5) which is simply not possible in most any other technology.

1.2 PolyStrata^{TM} Rectangular Coax

Due to its exceptional performance and TEM behavior, rectangular coax has been the standard transmission line in the PolyStrata^{TM} process. Two different build choices are standard for coaxial lines: a 5-strata build and an 11-strata build, shown in Figure 1.7. For a given 5-strata configuration, the width of the inner conductor (W_i) and the width of the inside wall of the outer conductor (W_a) can be varied to change the characteristic impedance of the line. An 11-strata build may have more flexibility in characteristic impedance choice as the strata comprising the inner conductor can be varied depending on the location of gold seed layers.

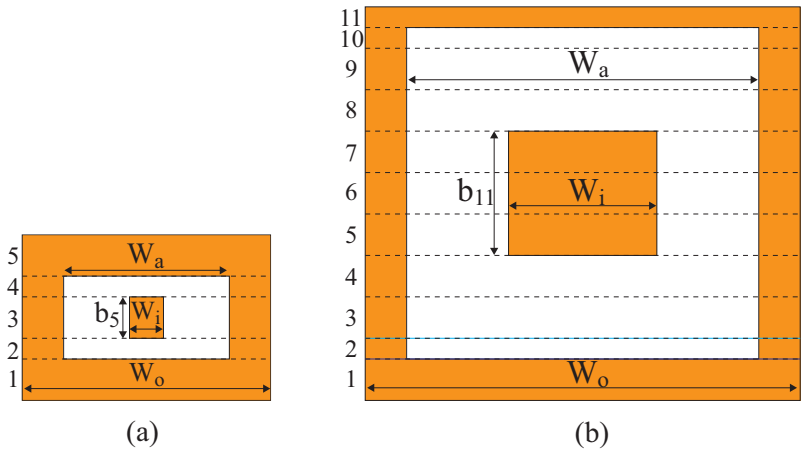


Figure 1.7: Cross section of (a) a 5-strata micro-coaxial line, and (b) an 11-strata micro-coaxial line. In order to obtain a characteristic impedance of 50 Ω in the 5-strata design (where strata 2 and 4 are 50 μm and strata 1, 3, and 5 are 100 μm) W_i should be 82 μm and W_a should be 400 μm. To obtain a characteristic impedance of 50 Ω in the 11-strata design (where strata 2, 10, and 11 are 50 μm and all other strata are 100 μm) W_i should be 358 μm and W_a should be 850 μm.

Figure 1.8 shows a section of 50Ω micro-coaxial line along with its physical dimensions. As described above, the inner conductor is supported by dielectric support straps placed periodically

along the length of the line. Release holes are present in the outer conductor to allow the photoresist to be released from the structure in the last step of fabrication.

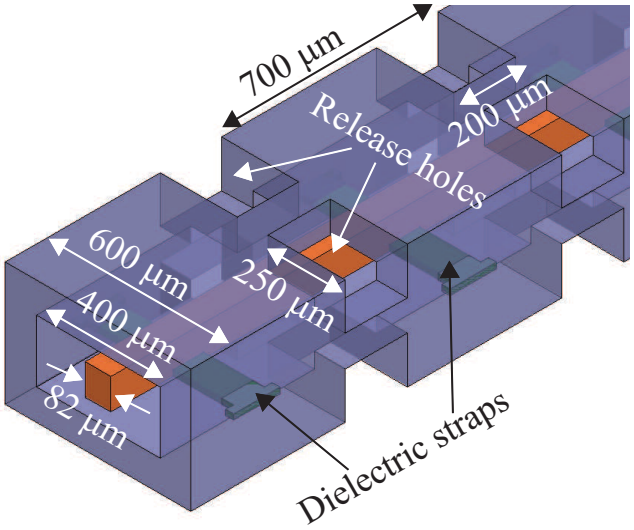


Figure 1.8: Physical geometry of a 50Ω rectangular micro-coaxial line. Periodic dielectric support straps support the inner conductor. The outer conductor contains release holes that allow the photoresist to be evacuated in the final step of fabrication. The characteristic impedance of the line is determined by the relative dimensions between the inner conductor and outer conductor.

1.3 PolyStrata^{TM} Waveguide

When designing waveguide in the PolyStrata^{TM} process, the release holes must be placed in a manner that does not disturb the wall currents, as illustrated by Figure 1.9. These currents, J_s, are found using the equation $\vec{J} = \hat{n} \times \vec{H}$, where $\hat{n}$ is the unit normal to the wall. Using this boundary condition, for a waveguide whose width is given as x, height by y, and length by z, the current in the top wall ($y = b$) is given by [13]

$$\vec{J_s} = \frac{-E_0}{\omega\mu} e^{-\jmath k_g z} \left[k_g \sin(k_c x)\hat{\mathbf{z}} + \jmath k_c \cos(k_c x)\hat{\mathbf{x}} \right]. \tag{1.1}$$

The sidewall currents are given by the equation

$$J_y = -\jmath \frac{E_0 k_c}{\omega\mu} e^{-\jmath k_g z}. \tag{1.2}$$

and are directed in the y direction only. From these equations, it can be determined that a vertical slot in the sidewall and a narrow longitudinal slot down the center of the top wall will not radiate as they are to the surface current vectors. The resultant waveguide geometry is shown in Figure 1.10. The waveguide cross section is sized to mate to WR-05, and release holes are sized and spaced according to manufacturing guidelines.

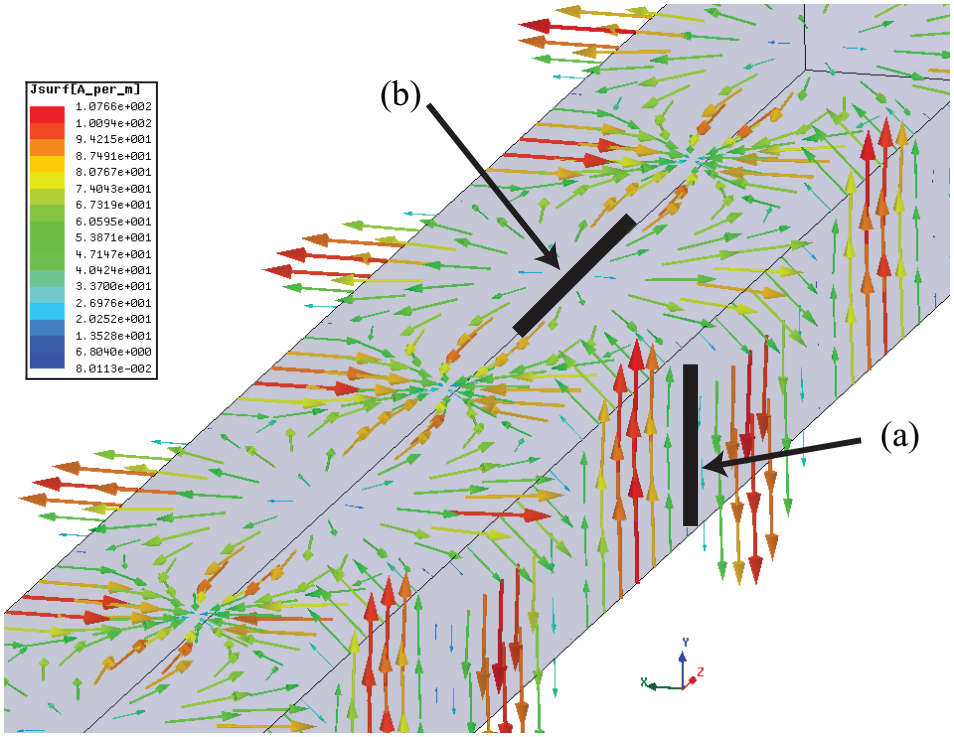


Figure 1.9: Illustration of current vectors in a TE_10 dominant mode rectangular waveguide and how non-radiating slots can be placed parallel to those vectors in the waveguide walls to avoid radiation. Along the sidewalls, the current vectors are only in the y-direction, so slot (a) is placed vertically. Along the top of the waveguide, the current vectors have no x-direction only at the centerline of the waveguide, so slot (b) can be made longitudinal along the centerline.

1.4 Previously Demonstrated PolyStrata^{TM} Components

A wide range of passive components have been demonstrated from 2 to 38 GHz using PolyStrata^{TM}. These include

– hybrid directional couplers at 30-42 GHz with 0.3 dB insertion loss with a 2° phase imbal-

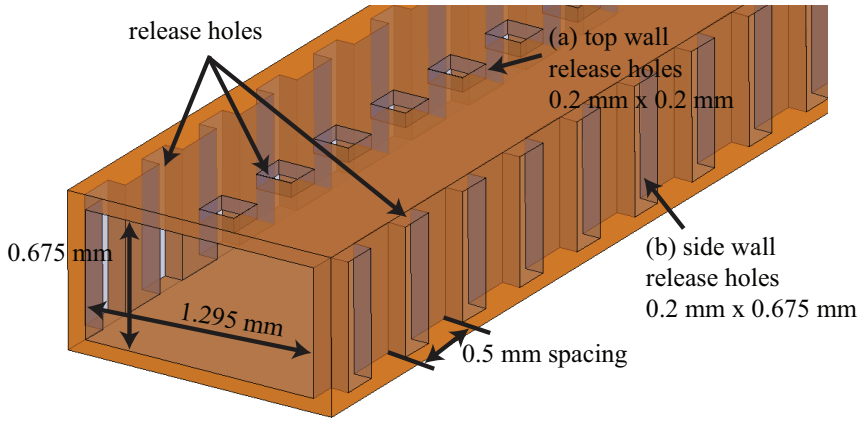


Figure 1.10: WR-05 compatible waveguide geometry realized in the PolyStrata^{TM} process.

ance [1, 14],

– coupled lines [1],

– microresonators with measured Q factors up to 829 at 26 GHz [2, 15, 16, 17],

– Wilkinson power dividers [18, 19],

– transformers [20, 21, 22], and

– antennas of various types, including patches [23, 24, 25, 26], log-periodic antennas [21, 22, 27], and spiral antennas [28].

The PolyStrata^{TM} process is a low-temperature process, so thus far it is not possible to fabricate quality resistors or capacitors, so there is a need for hybrid integration with minimal parasitics so that the broadband nature of PolyStrata^{TM} microcoax can be exploited. Furthermore, to the best of the author's knowledge, no components above W-band have been demonstrated to date [21, 28, 29, 30]

Other rectangular coaxial cable micromachining technologies utilize a center conductor that is supported by posts that short the center conductor to ground [31, 32, 33]. This immediately limits the bandwidth of any structure designed and also disqualifies the lines from handling a DC bias

voltage. Although not suitable for coaxial lines, the gold-coated, SU-8 photoresist micromachining process has demonstrated WR-03 waveguide components [34] and may be of future high frequency interest.

1.5 Thesis Outline

The first chapters of this thesis give details on several 4-18 GHz broadband micro-coaxial components:

- Chapter 2 presents the design, simulations and measurements of assembly structures in the micro-coaxial environment for surface mount R, L and C in standard packages, as well as an example of how an active device can be hybridly integrated with PolyStrata^{TM} lines
- Chapter 3 discusses monolithic inductors that are a high current alternative to surface mount devices (SMDs)
- Chapter 4 shows how the sockets from Chapter 2 and inductors from Chapter 3 can be integrated into broadband bias tee networks

Appendix A presents work done on a broadband MMIC traveling wave amplifier in the 4-18 GHz range designed in the TQS TQPED GaAs pHEMT process for possible integration with PolyStrata^{TM} lines in a 50-ohm environment.

The second part of the thesis focuses on G-band waveguide PolyStrata^{TM} frequency scanned arrays:

- Chapter 5 presents details on the design and packaging of a traveling-wave, frequency scanning, broad wall, uniform slot, slotted-waveguide array,
- Chapter 6 presents measured radiation patterns, gain, return loss and scanning of 10- and 20-element arrays.

Finally, Chapter 7 summarizes the contributions of this thesis and discusses some directions for future work, including W-band micro-coaxial frequency scanned arrays.

Chapter 2

Micro-coaxial Sockets for Passive and Active Surface-mount Devices

2.1 Introduction

This chapter addresses assembly structures referred to as "sockets", illustrated in Figure 2.1, which can be made in the PolyStrata^{TM} process to accommodate surface-mount devices (SMDs), discrete active devices, chips, or integrated circuits. Since the PolyStrata^{TM} process is a low-temperature process, thus far it has not been possible to monolithically integrate resistors, capacitors, or active devices. However, hybrid assembly into carefully designed micro-coaxial structures allows choice of best available SMDs or actives, while presenting minimal parasitic impedances.

In this chapter, socket design and performance both for passive devices and active devices are discussed. The PolyStrata^{TM} process is well suited for hybrid integration due to the ability to shape precisely both the inner and outer conductors, as well as allowing surface-mount technology (SMT) parts to be placed in series or shunt configurations. One half of of series socket geometry is shown in Figure 2.1(a) and a series 0303 resistor in a series socket is shown in Figure 2.1(b). The integration of dielectric straps with the process allows many different configurations providing for mechanical stability of any mounted devices.

2.2 General Design Tips

The first step of socket design is to select a component geometry. From that geometry, the surrounding PolyStrata^{TM} coaxial line can be altered in order to accommodate the package of interest. Examples of packages include standard 0603 (60 mils by 30 mils), 0402 (40 mils by 20 mils),

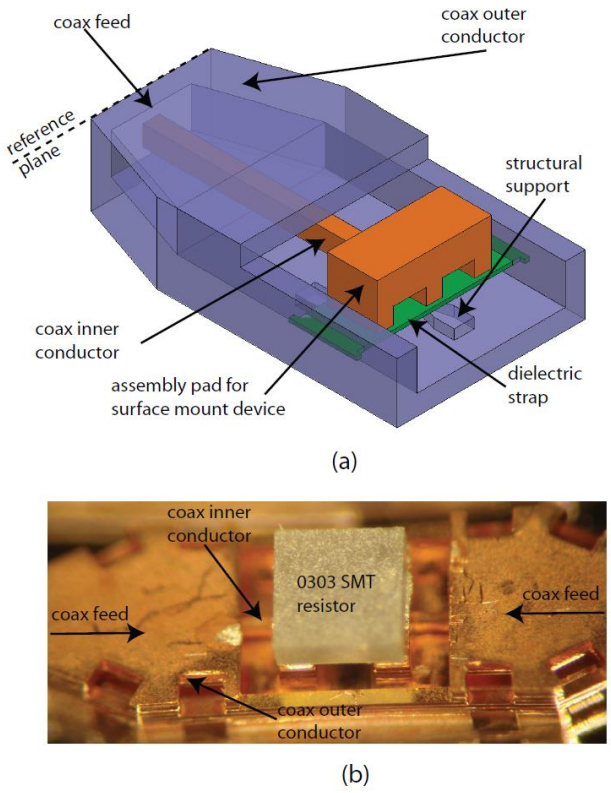


Figure 2.1: (a) 3-D geometry of one-half of a surface-mount component assembly structure (socket) in the copper-based, coaxial PolyStrata^{TM} environment. (b) Photo of an 0303 sized die component mounted in a series socket between two 50Ω microcoaxial lines. The inner conductor is 82 by 100 μm^2. The outer conductor's inside dimensions are 400 by 200 μm^2.

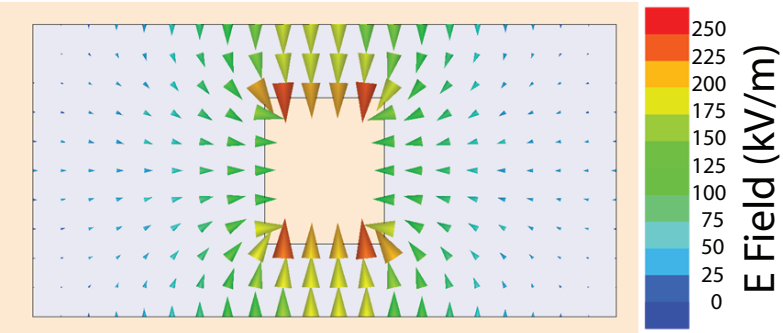


Figure 2.2: Simulated field distribution in a 50Ω line. The arrows show the total E-field vector.

0303 (30 mils by 30 mils), et cetera. Details to consider include, but are not limited to, mechanical stability, line impedance geometry, parasitics, component placement tolerance, and solder or epoxy placement tolerance. Land patterns detail how component placement and soldering is standardized for automated processes, but these patterns are larger than what is needed for manual component placement. A good rule of thumb for manual placement is to have pads for surface mount devices at least 50-100 μm larger than the device and to maintain at least 20 μm gap to avoid bridging solder or epoxy shorting the device.

The best place to begin design is by analyzing the field distribution present in the coaxial line. Two valuable insights can be gained from field simulations. First of all, knowing the field distribution will assist in how modeling is to be accomplished. For example, if a boundary or excitation is to be used that applies in a circuit model analysis but not in a physical sense, then that boundary should not be used in an area of large field distribution. Secondly, knowing the field distribution aids in obtaining socket designs that reduce parasitics. In Figure 2.2, one can see that the field is weaker around the sides of the line. Applying this knowledge to reducing parasitics leads one to the insight that altering the sides of the socket will not have as much effect as altering the top or bottom of the socket due to the relatively low field strength along the vertical side walls.

Once the field distribution is known, consideration may be given to structural support and component stability within the socket. Ideally, one would like the surface-mount component to be in line with the center conductor as shown in Figure 2.3, but due to component and solder or epoxy

placement requirements, that is not always possible. Since the PolyStrata^{TM} lines are generally small compared to components, consideration must be given to the fact that the component may be considerably wider than the center conductor and thus need lateral stabilization, an example of which is labeled "structural support" in Figure 2.1(a). These structural supports are possible because of the straps, since they can provide electrical isolation between the inner conductor and the structural support (ground potential).

2.3 Sockets for Passive SMT Components

The coaxial lines are closed structures, so a finite-element method (FEM) is a natural choice for analyzing them, and Ansoft HFSS^{TM} was used for the results presented here. The surface-mount passive sockets are relatively complicated 3-D structures (Figure 2.1), so FEM analysis is appropriate, but should be used with care due to the open nature of the geometry. In the simulations, radiation boundary conditions are assigned both above and on the sides surrounding the device while below the socket there is a silicon substrate with a ground plane underneath (as the devices were fabricated on silicon for planarization and are measured on a metal probe station).

The SMT component mounted in PolyStrata^{TM} has microcoaxial input and output wave ports as shown in Figure 2.1(a). For meaningful S-parameter data, the socket needs to be populated appropriately in the numerical model. An SMT component is pictured in Figure 2.1(b), but its electromagnetic properties are unknown, since the manufacturer provides only circuit parameters and outside dimensions. Figure 2.4 shows to scale an 0402 component along with several simulation options. Due to the relative size of the component, the fields in the socket are strongly affected by the exact dimensions and materials, so the boundary conditions imposed by different simulation set-ups can have very different results. Thus, for a shunt socket a terminating resistance (i.e. $50\,\Omega$) was simulated in the following various geometries:

- sheet wave port (Figure 2.4(a),(b))
- sheet lumped port (Figure 2.4(a),(b))

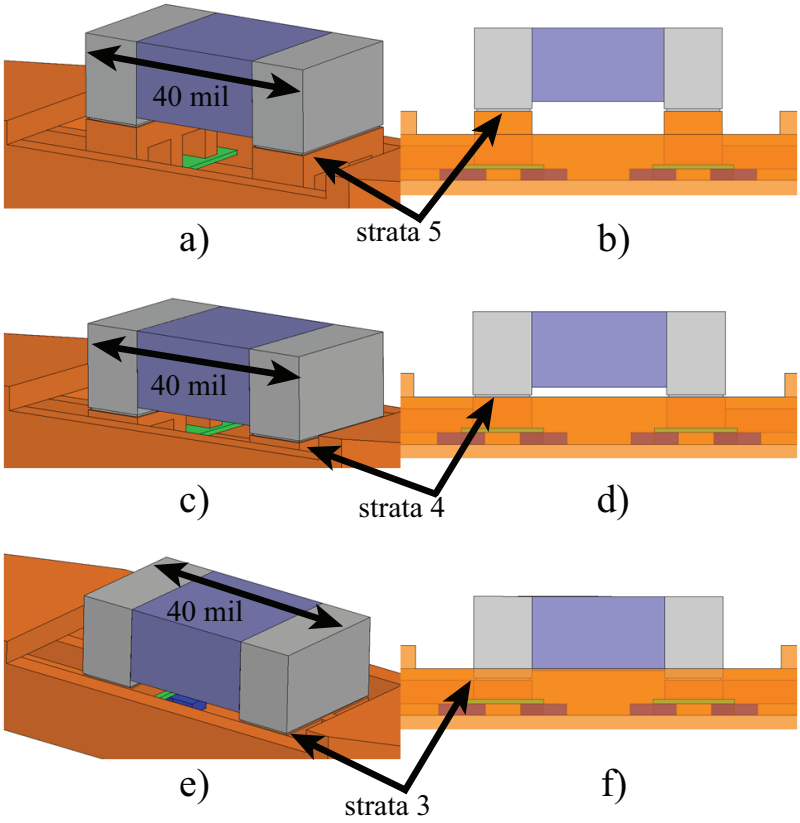


Figure 2.3: Visualization of components mounted at different heights within the socket.

- sheet impedance (Figure 2.4(a),(b))
- sheet resistance (Figure 2.4(a),(b))
- 0402 outline with sheet impedance of various widths (Figure 2.4(c))
- 0402 volumetric model (Figure 2.4(d))

Once the return loss of the terminated one port device was better than 10 dB from 4-18 GHz for all geometries, the socket was mirrored in order to make a series socket (similar to Figure 2.11b). This series socket then was checked by placing a short and an open between the two surface-mount pads. The return loss for the short showed better than 15 dB over the band, while the transmission for the open showed lower than -40 dB, thus indicating that the fields were highly contained in the geometry and radiation was minimal as confirmed by examining the radiation pattern and efficiency.

In order to compare simulation to experimental data and assess what method gives best agreement, PolyStrata^{TM}-based TRL calibrations standards were designed. The frequency range is calibrated with two different line lengths which cover 2-7 GHz and 7-22 GHz. The calibration standards include transitions from CPW probes to the microcoax, referred to as launches, and described in detail in [35]. The calibration places the reference plane at the edge of the socket in Figure 2.1(a). Shunt and series sockets were then manufactured in a 5-strata process and the following SMT components were mounted using silver epoxy (Epoxy Technology H20E):

- series 50 Ω 0303 resistor
- shunt 50 Ω 0402 resistor
- series 3 pF and 82 pF capacitor (Dielectric Labs)
- shunt 3 pF and 82 pF capacitor (Dielectric Labs)
- shunt 75 Ω 0402 resistor

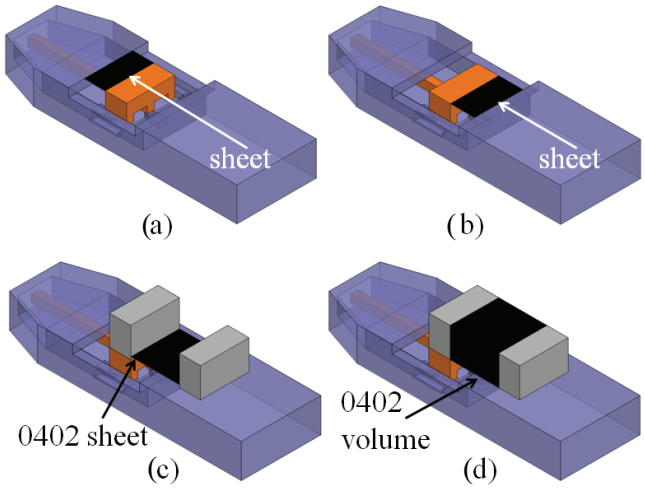


Figure 2.4: Four different geometries for hybridly integrated SMT sockets. In (a)-(c), the resistor or capacitor are modeled with a sheet impedance. (d) has the advantage of being 3-D and thus more representative of the actual component, however, since physical descriptions are not available an appropriate model is difficult to determine.

– series 1.2 nH inductor

– series 0 Ω 0402 resistor

This work discusses measurement and analysis for the first three cases as examples which illustrate most completely and concisely the results.

A 50 Ω resistor was chosen as a good test case, with an expected insertion loss

$$IL = 10 \log \frac{|S_{21}|^2}{1 - |S_{11}|^2} = 3 \,\text{dB} \tag{2.1}$$

and return loss 9.54,dB. As seen in Figure 2.5, the 0303 resistor in series behaves almost exactly as a theoretical 47 Ω resistor (within the tolerance of the actual resistor), which has a return loss of 9.90 dB and an insertion loss of 2.88 dB. As mentioned before, the 7 GHz crossover point calibration between the low and high frequency line standards is evident, and the data shows that the calibration for high frequency was a bit better than it was for low frequency.

In order to determine the parasitics that are present in the design, the component values of a physics-based, equivalent-circuit model of a shunt-configured, surface-mount resistor are fit using measured results. The final circuit model is shown in Figure 2.6, and the performance is shown in Figure 2.7.

With confidence in the simulation methods, a model was needed for a capacitor. Given the broad bandwidth of the design, a Dielectric Labs "Ultra Broadband" capacitor (Millicap®) was selected. Since this component had no published s2p file, the device was placed in a series socket and measured. Once measured, simulations were done to do a best fit to the actual performance of the device. Various models were tested including volumetric and sheet models, but in the end the model that worked best was a sheet impedance with PEC shields above and below it to minimize the effect of the boundary conditions that the sheet impedance imposes.

2.4 Sockets for Active Devices

The PolyStrata^{TM} process also allows integration with active devices. Depending on the type of integration, e.g. flip-chip or wire-bond, different "active sockets" are designed in order to

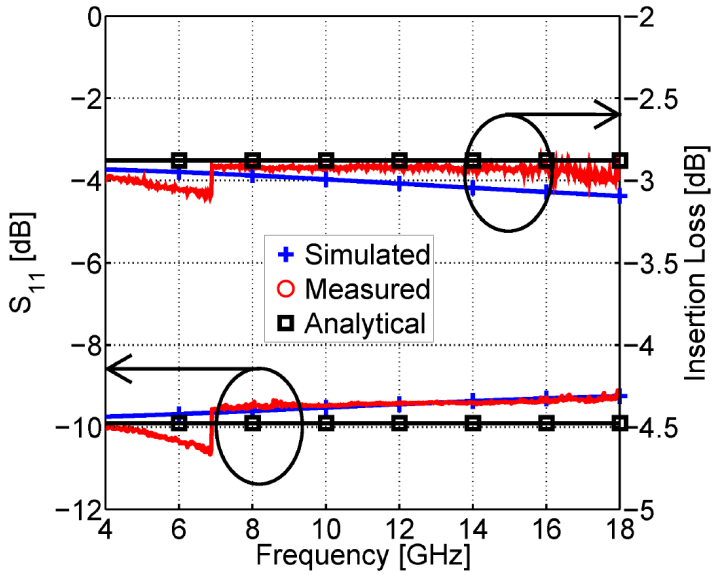


Figure 2.5: Simulated, measured, and ideal performance of a series, 50 Ω resistor in a 50 Ω line. The insertion loss is approximately 3 dB, and the return loss is approximately 10 dB for all three cases.

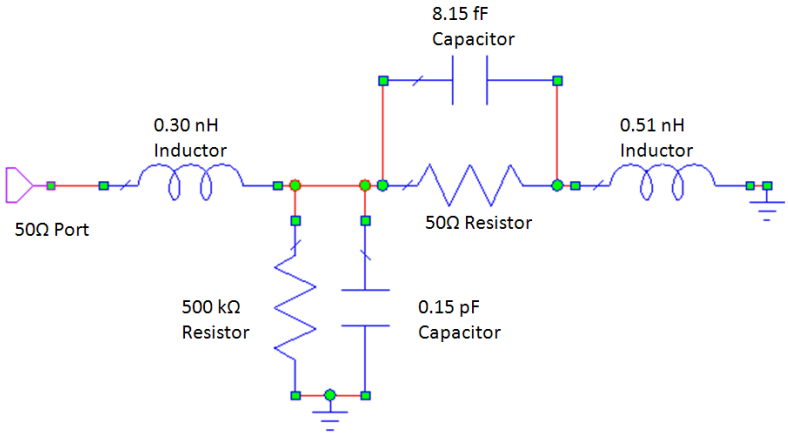


Figure 2.6: Equivalent circuit model for a 50 Ω resistor in a shunt socket.

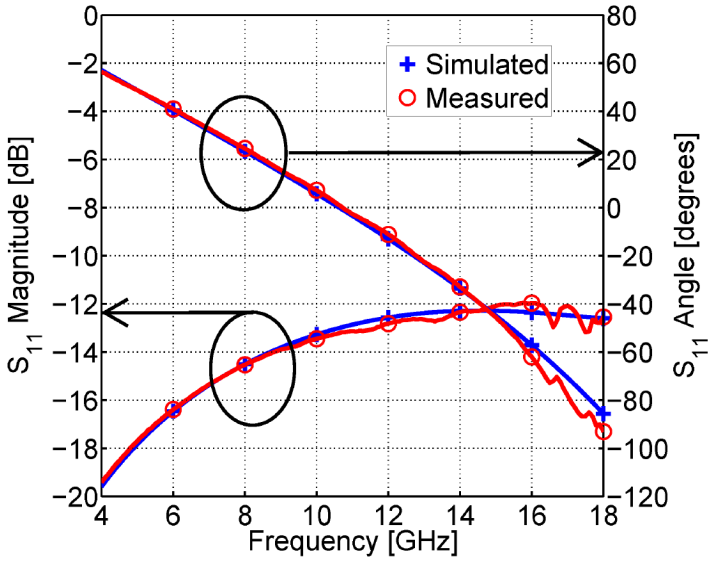


Figure 2.7: Comparison between measurement and circuit simulation for an 0402 50 Ω resistor assembled in shunt in a 50Ω, micro-coaxial line.

compensate for parasitics. For the 50 Ω characteristic impedance, the active socket design was to mate the coaxial lines to a flip-chip assembly of a distributed amplifier gain block comprised of a 600 μm gate periphery GaN HEMT MMIC on a 100 μm thick SiC substrate [36]. The design shown in Figure 2.8 includes a pair of two-wire bias lines for the gate and drain biases, and 50 Ω input and output ports. The return loss is better than 40 dB and $|S_{21}|$ is better than -0.05 over the entire design band 4-18 GHz. The comparison of the measured small-signal performance of the chip both on wafer and in the PolyStrata^{TM} process (Table 2.4) confirms that there is no degradation in performance when the active device is hybridly integrated into the monolithic microcoaxial environment over the region of the band for which the 1-10 GHz active device overlaps. The chip was designed and measured by Robert Actis at BAE, Nashua, NH.

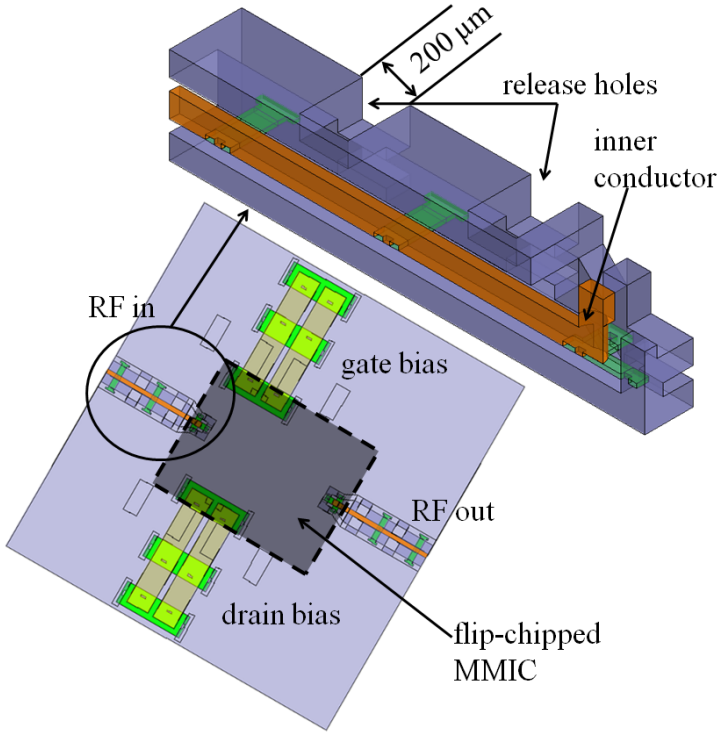


Figure 2.8: A top-down view of a complete assembly structure for a flip-chip integrated active device input and output matched to 50 Ω. The RF input line is expanded and cut-away to show the geometry of the line and active socket.

Table 2.1: MMIC performance as measured both on wafer and mounted in a PolyStrata^{TM} active socket

	4 GHz	6 GHz	8 GHz	10 GHz
$\|S_{11}\|$ on wafer	-18.48 dB	-30.05 dB	-12.69 dB	-9.59 dB
$\|S_{11}\|$ in PolyStrata	-17.27 dB	-29.51 dB	-12.07 dB	-8.86 dB
Magnitude Difference	0.018	0.002	0.017	0.029
$\|S_{21}\|$ on wafer	10.27 dB	9.2 dB	10.88 dB	7.07 dB
$\|S_{21}\|$ in PolyStrata	10.55 dB	9.58 dB	11.13 dB	7.27 dB
Magnitude Difference	0.093	0.129	0.102	0.053

2.5 Sockets in Non-50 Ω Environments

When expanding this technology into non-50 Ω environments, several difficulties arise. First, parasitics become even more important. Take for example a bond wire of length 0.25 mm connecting two pieces of transmission line. The bond wire will have an inductance of about 0.25 nH, which at 18 GHz introduces about 28 Ω of parasitic reactance. Comparing return loss in a 50 Ω environment to that in a 12.5 Ω environment, the lower impedance suffers about 10 dB return loss over the entire band. A comparison of $|S_{11}|$ and $|S_{21}|$ for the two different characteristic impedances is shown in Figure 2.9.

With this challenge in mind, an active socket design in 12.5 Ω was done. Two approaches became clear due to different restrictions on manufacturability. The first is to choose a different geometry that works around fabrication constraints of aspect ratio by bonding the active device not to the top strata (strata 11) of the PolyStrata^{TM} structure, but to strata 10, just below the top. This geometry and its associated results are shown in Figure 2.10. This shows that the transmission, $20 \log |S_{21}|$, is better than -0.1 dB across the band of 4-18 GHz, while the return loss is better than 15 dB over the same band.

The second geometry was chosen for better bondwire manufacturing compatibility, maintaining the transition on the top layer of PolyStrata^{TM}. Here, the fabrication aspect ratio is the limiting factor, and the performance is as shown in Figure 2.10. Although the performance is not as good as the previous geometry, the transmission, $20 \log |S_{21}|$, is better than -0.8 dB across the

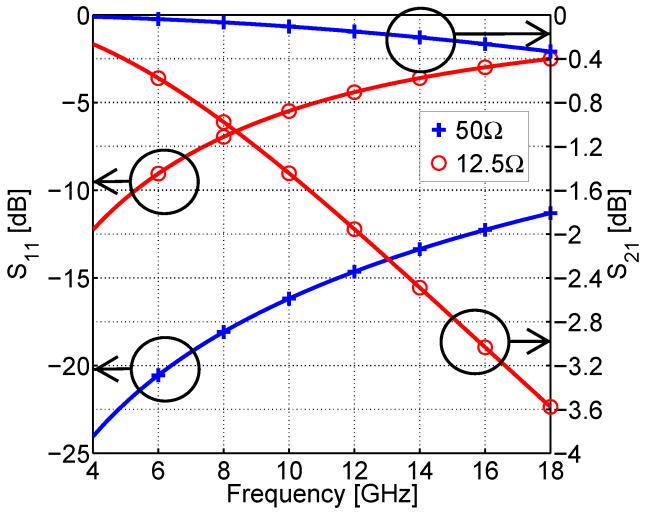


Figure 2.9: Effect of a 0.25 mm long bondwire (0.25 nH inductance) in series between two transmission lines on $|S_{11}|$ and $|S_{21}|$ in a 50 Ω (blue) and 12.5 Ω (red) system. This illustrates the care that must be taken when using a low impedance environment in design.

band of 4-18 GHz, while $20 \log |S_{11}|$ is better than 5 dB over the same band.

2.6 Conclusions and Contributions

In summary, this chapter presents methods for hybrid assembly of standard surface-mount components into the PolyStrata^{TM} microcoaxial environment. It is shown that the electrical characteristics such as return loss and insertion loss can be kept at acceptable levels even in low-impedance environments. In a 50 Ω coaxial environment, the added insertion loss is between 0.05-0.12dB in the frequency range 4-18 GHz. The hybrid integration allows choosing high-quality transmission lines such as microcoax and high-performance surface mount lumped elements (e.g. capacitors and resistors) as well as MMICs and integrating them for best overall electrical performance. This work is the basis for the results reported in [8, 5, 37].

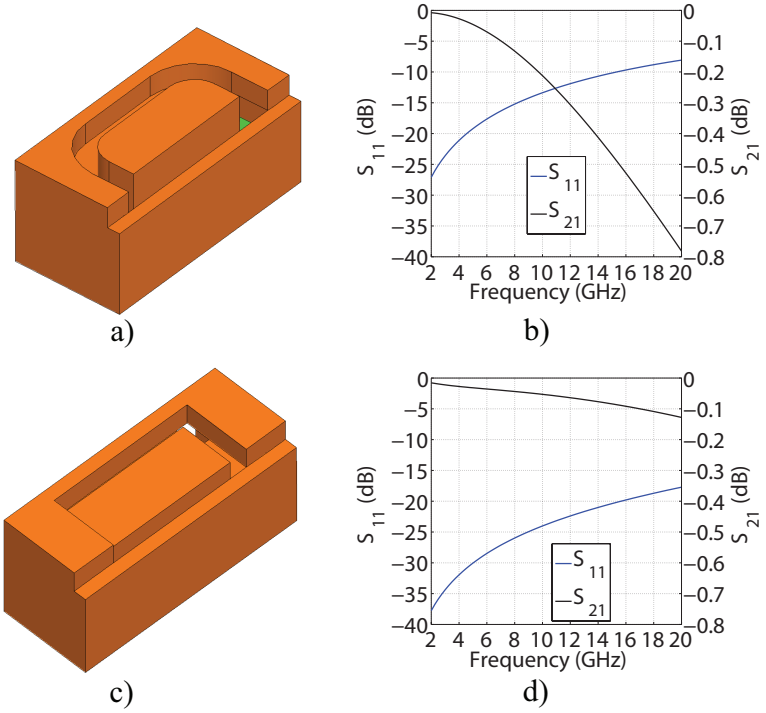


Figure 2.10: (a) Geometry for conventional wire bonding to the top of the structure. The minimum gap is based on lithography requirements. (b) Alternate geometry for bonding to a lower layer. Choosing (b) over (a) reduces return loss from 20 dB to 30 dB, and reduces $|S_{21}|$ from 0.05 dB to 0.02 dB.

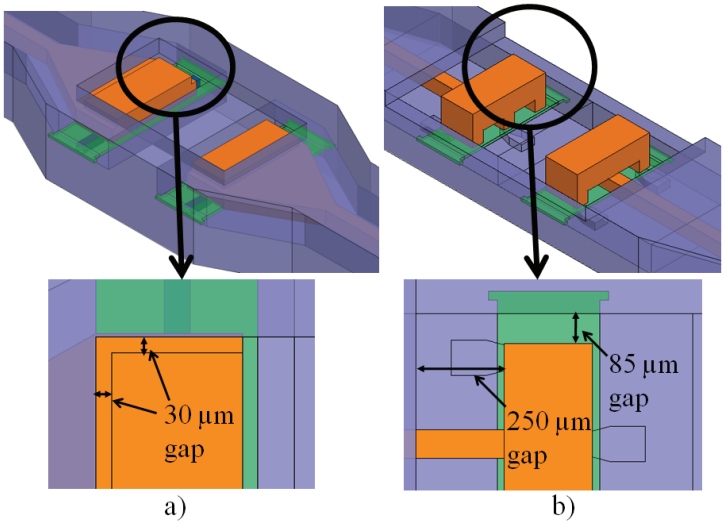


Figure 2.11: An illustration of the marked difference between the geometry of a 12.5 Ω socket (a) and a 50 Ω socket (b). While the gap size for (a) is small enough that it can affect ease of manufacturability, it is required to minimize field disturbances and thus reflections when transitioning to a surface-mount device.

Chapter 3

Inductors

3.1 Introduction

At microwave frequencies, inductors with inductance values above a few nH are difficult to realize due to capacitance between windings. A first-order equivalent circuit of a realistic inductor is shown in Figure 3.1(a). Above the self-resonant frequency, $f_r = \frac{1}{2\pi\sqrt{LC}}$, the inductor reactance is capacitive. The losses (R_s) contribute to a decrease in quality factor, Q. PolyStrata^{TM} inductors offer reduced capacitance (air is the only dielectric material in contact with the windings), increased current handling, and are 3-dimensional. The same first-order equivalent circuit can be used to model both categories of inductor: spiral and solenoid.

Spiral inductors are available as surface mount devices [42, 43] as shown in Figure 3.1(b), but are primarily used in integrated circuits like Figure 3.1(c) due to their compatibility with IC processes due to their 2-dimensional nature. However, since they are fabricated on a substrate, they have a considerable capacitance between windings owing to the dielectric constant of the substance on which they are fabricated. They also require large footprints to achieve useful inductance values. Some IC processes do not allow the inductors to be round, so the inductors are often square. As the RF current flows, it experiences a phenomenon called current crowding at the bends due to the skin and related effects. In addition to quasi-static conductor and dielectric substrate losses, current crowding contributes to additional conductor losses. The inductors are fabricated using the metal layers of the IC process. This places a limit on the cross section of the metal traces, corresponding to a limit in the current handing these inductors can safely handle. A commercially

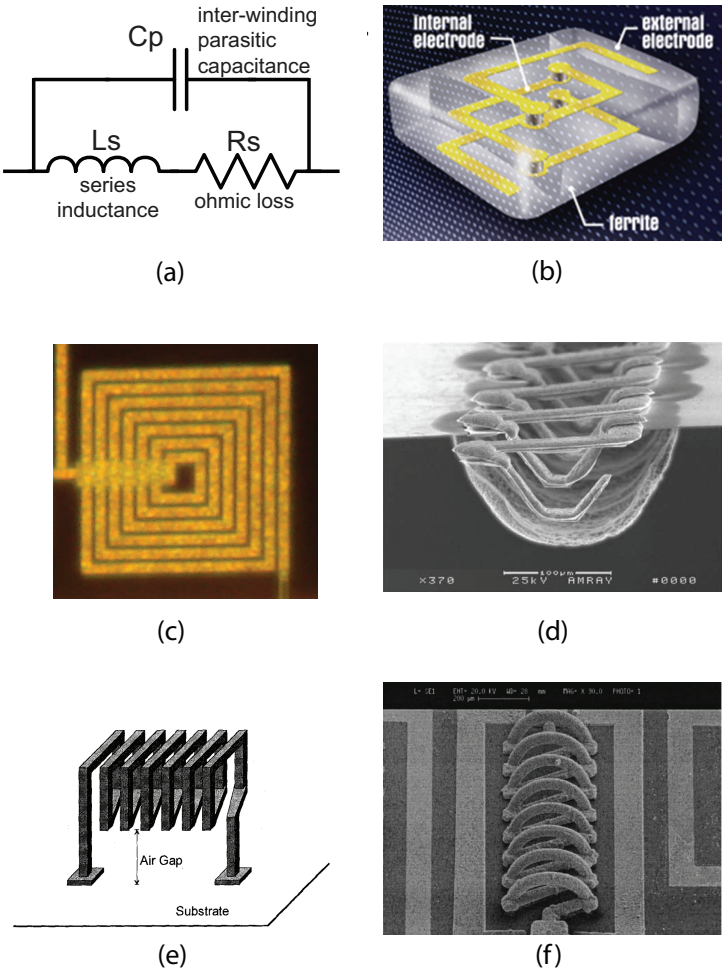


Figure 3.1: (a) Illustration of a basic circuit model for any inductor. (b) Commercially available spiral inductor in a surface-mount package [38] (c) Spiral inductor integrated in GaAs (d) Micro-fabricated, integrated, solenoid inductor made using etching techniques [39] (e) Micro-fabricated solenoid inductor that attaches to bonding pads on top of an IC [40] (f) 3-dimensional inductor fabricated to be compatible with an IC [41]

available GaAs process, for example [44], has thicknesses for Metal 1, 2, and 3 of 2 μm, 2 μm, and 5 μm, respectively. Thus for an inductor using Metal 1 and Metal 2, the minimum thickness of metal will be 2 μm, which handles considerably less current than a line of 100 μm thick copper.

Solenoid inductors include the classical wire-wound, ferrite-core inductor. At RF, they are realized in three basic ways: wire-wound chip (SMD) inductors, trench inductors, and micromachined inductors. Wire-wound inductors are the most common variation and find usage anywhere

that an SMD can be used. Since they are comprised of wires instead of thin metal strips, they can handle appreciably more current. Trench inductors, illustrated in Figure 3.1(d) are a means of fabricating solenoid inductors on a chip that is compatible with the etching processes required to make the trench. Like spiral inductors, they use very thin copper traces and are on a substrate which decreases their current handling and increasing the inter-winding capacitance. Micromachined inductors are the third class. They are often envisioned as a bridge between wire-wound chip and spiral inductors. Most often they are connected to pads on the chip, as shown in Figure 3.1(e), though other fabrication techniques exist where structural support is given via the chip itself, Figure 3.1(f).

Inductors micro-fabricated in the PolyStrata^{TM} process can be either solenoid (3D) or spiral (2D) as shown in Figure 3.2. Furthermore, due to the structural support of dielectric straps, the spiral need not be placed on the substrate for structural support, but rather can be suspended in air. PolyStrata^{TM} inductors are discussed in more detail in Section 3.3.

3.2 Inductance and Q Factor

Inductors are characterized by their inductance, value of Q, resonant frequency, current handling, and size. Inductance and Q found in datasheets are measured at a given frequency well below resonance (e.g. 600 MHz, 900 MHz). In most of the existing literature, the inductance (L) and the quality factor Q are found using

$$L = -\frac{1}{\omega \cdot \Im(Y_{11})} \tag{3.1}$$

$$Q = \frac{\Im(Y_{11})}{\Re(Y_{11})}, \tag{3.2}$$

where Y_{11} is the input admittance of the inductor when measured in series as a 2-port measurement. These equations, however, can result in misleading values. Figure 3.3 shows that the inductance evaluated from Equation 3.1 for an experimental component is a strong function of frequency, which does not correspond to standard inductor the definitions

$$V = \jmath\omega LI \tag{3.3}$$

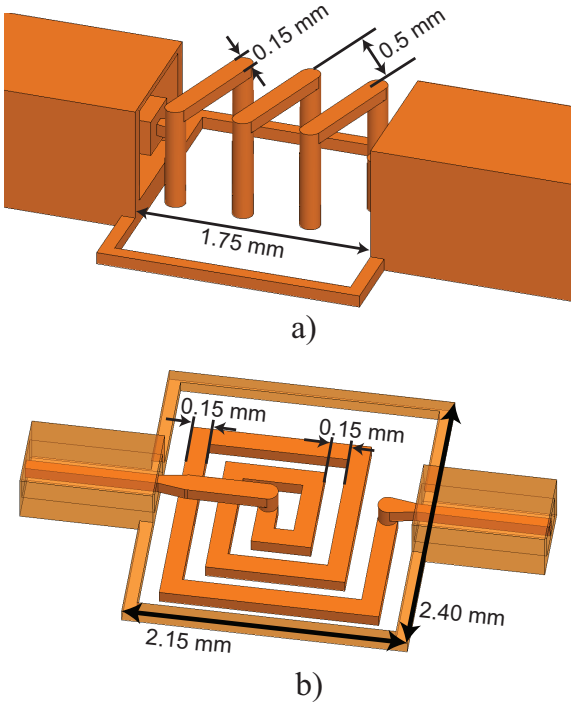


Figure 3.2: (a) Solenoid inductor in the PolyStrata^{TM} process. This inductor is discussed in more detail below. (b) A spiral inductor in the PolyStrata^{TM} process. This inductor on low-resistivity silicon was simulated to have an inductance of 0.5 nH, a Q of 3, and a resonant frequency of 69.3 GHz.

and

$$V = L\frac{\partial i}{\partial t}. \tag{3.4}$$

The equation makes sense considering the reactance of a simple parallel inductor and capacitor,

$$X = \frac{1}{-\frac{\jmath}{\omega L} + \jmath\omega C}, \tag{3.5}$$

at low frequency when the equation simplifies to $\jmath\omega L$, but at resonance and above, Equation 3.1 is no longer valid. By definition, the Q is used to describe the behavior (i.e. the energy stored in the reactance per cycle divided by the amount of energy dissipated by the resistance per cycle) at resonance. However, Equation 3.2 yields a value of 0 at resonance, since the capacitive and inductive reactance cancel.

A better approach then is presented by Kuhn [45] and is adapted here. The underlying

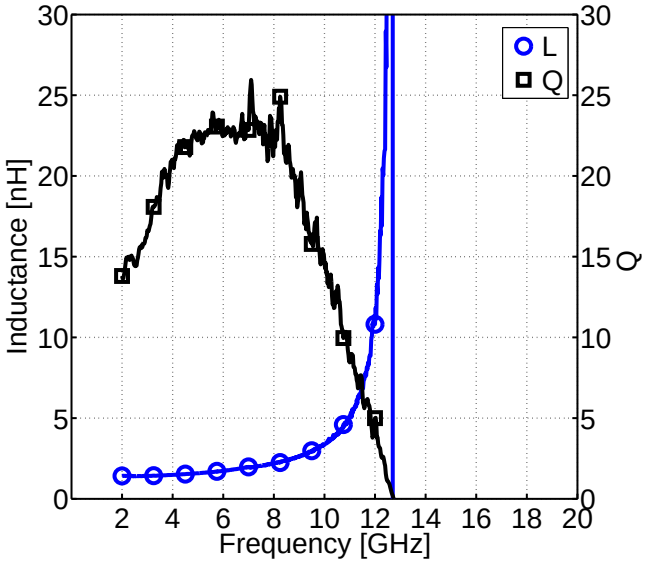


Figure 3.3: Extracted inductance and Q found using standard literature equations from measurements of a 3-turn PolyStrata^{TM} inductor.

concept is that although the lumped-element equivalent model can vary significantly, the overall behavior of an inductor to a first order approximation consists of three elements, an inductance in series with a resistance, with a capacitor parallel to that combination, Figure 3.1(a). In this case, inductance can be expressed as a frequency independent value. Furthermore, with the resistance known, a more standard definition of Q can be used:

$$Q = \left.\frac{\omega L}{R}\right|_{resonance}. \tag{3.6}$$

The procedure to calculate these values is as follows:

(1) Convert S-parameter data into admittance data.

(2) Use Equation 3.1 to find apparent inductance, L_{app}.

(3) Find L_s from the low frequency value of L_{app}.

(4) Find f_{res} as the frequency where L_{app} transitions from positive to negative.

(5) Compute C_p from L_s and f_{res}.

(6) Find the impedance $Z_{RL}(\omega)$ by subtracting C_p from admittance data and then converting admittance data to impedance.

(7) Express $Z_{RL}(\omega)$ as the series combination of R_s and L_s.

(8) Evaluate Q as $Q = \omega L/R_s$.

Contrasting this approach with the standard equations used to describe inductors, the inductor of 3.3 has an inductance of 1.42 nH, and a Q at resonance of 35.6. The calculated impedance of the inductor closely matches the measured reactance, as illustrated in Figure 3.4, and the Q has a non-zero, and thus meaningful, value at resonance.

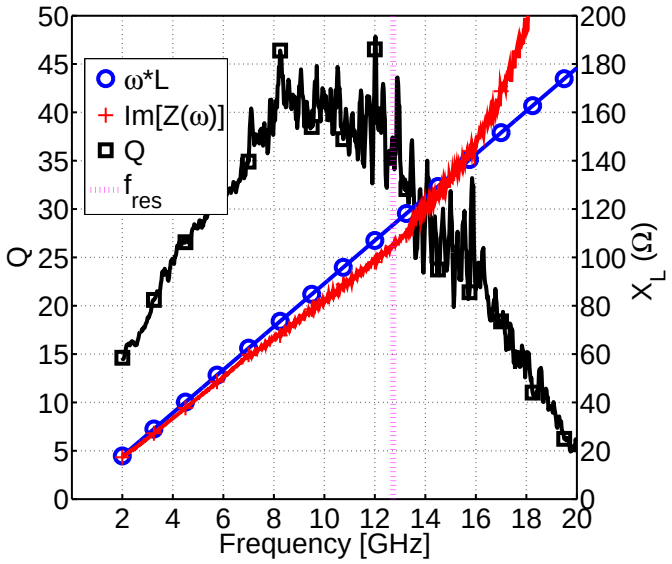


Figure 3.4: Measured Q (expressed as ωL / R_s), reactance and equivalent reactance of extracted inductance for the same 3-turn PolyStrata^{TM} inductor as Figure 3.3. In this case, Q is not 0 at resonance (vertical line) and inductive reactance is a function of frequency while inductance is not.

3.3 Air-Core Solenoid Inductors in the PolyStrata^{TM} Process

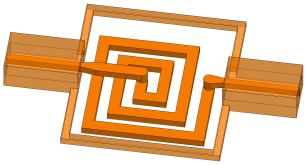
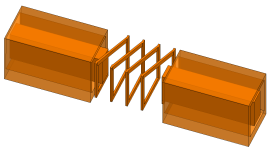
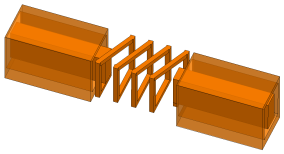
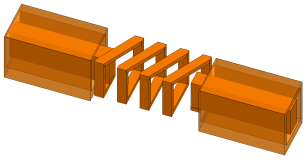
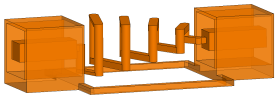
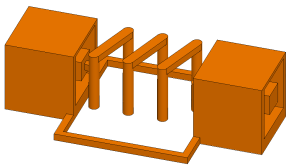
The PolyStrata^{TM} process enables both solenoid inductors, Figure 3.2(a), and spiral inductors, Figure 3.2(b). However, since the bottom strata is generally thick, and due to the effect of the substrate on parasitic capacitance, solenoid inductors are preferred. While the spiral could

be moved to a higher strata and supported with dielectric straps, or the entire structure could be released from the substrate and an alternate means of support proved, the height of the strata in general will be a limitation on the inductance due to the large cross-section due to the height of the strata. This means that primary limitation of the spiral inductor will be size (due to aspect ratio requirements which are discussed in Section 3.6), as increasing the number of turns increases both the length and width of the footprint, as opposed to just the solenoid which increases only the length.

The focus of this work then became 3-dimensional solenoid inductors, and attention was turned to geometry specifics. Several different geometries can be fabricated in the PolyStrata^{TM} process, as shown in Table 3.1. With coils parallel to attempt to maximize flux linkage, the coils can be made thin to increase inductance (Table 3.1, Style-2) or thick to increase current handling (Style-4). The flexibility of the PolyStrata^{TM} process enables an exotic geometry called a conical inductor, illustrated in Table 3.1 as Style-5. This inductor theoretically acts as a broad-band RF choke made of several different inductors of different values in series. The narrow end of the inductor corresponds to small inductor values (with a higher resonant frequency) while the larger coils correspond to larger values of inductance. This could also be extended to a biconical inductor, where the goal would be that parasitic capacitance between coil windings could be reduced by having the windings at different diameters, increasing the resonant frequency at the expense of inductance due to a drop in cross sectional area, or simply altering coil winding cross sections, as shown by Style-6.

It has been found that the lowest parasitics for PolyStrata^{TM} air-core inductors occur when the vertical columns are round and the columns are offset, Style-7 in Table 3.1. Another advantage to this inductor geometry is that the inductor is compatible with a PolyStrata^{TM} run of any number of layers, so it is the most general. Conical inductors, which can conform to the offset, round vertical column constraints, are worthy of further exploration, but have drawbacks including increased gold seed layer required (discussed further in Section 3.6) and more complicated means of minimization of parasitics.

Table 3.1: Simulation results for various inductor types in an 11-strata process.

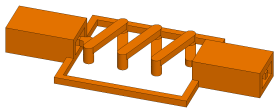
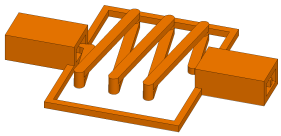
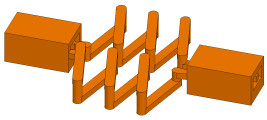
	Style	**L (nH)**	**f_{res}**	**Q**	**Comments**
	(1) spiral inductor on silicon substrate	0.5	69.3	3	significant size contrast with low inductance value
	(2) square post, Z-turn, thin windings	4.5	10.5	96	base design
	(3) square post, Z-turn, medium windings	3.8	10.75	130	increased winding capacitance maintains f_{res} as inductance drops
	(4) square post, Z-turn, thick windings	3.3	10.75	170	increased windings continues to lower resistance and improve current handling
	(5) round post, conical inductor	4.3	9.7	31	conical inductor test
	(6) round post, nonuniform height windings	3.6	10.7	35	variation of preferred design to increase f_{res}
	(7) round post, zig-zag turn, medium windings	4.5	10.0	38	preferred design in PolyStrata^{TM}

The coils are constrained in height by the specifics of the strata details of the run, which was limited to 5 for all further design, but the area can be increased by making the turns very wide as illustrated in Table 3.2 Style-2. The excess width, however, causes an increase in capacitance as

well which results in an excessive decrease in resonant frequency.

Though a 5-strata design is more limited than an 11-strata design, an exotic inductor once again was postulated and simulated as shown by Table 3.2, Style-3. This design is an adaptation of a transmission line equivalent circuit model. The common model is that of Figure 3.5(a) where a single inductance and capacitance is shown along the signal section of the transmission line. A more accurate model, however, is that of Figure 3.5(b), where inductance is found both in series with the signal and the ground. Since the PolyStrata^{TM} process does not have a pre-defined way of grounding (e.g. a ground plane in microstrip), the ground can be shaped and modified as desired. Conceptually, then, the PolyStrata^{TM} process allows the ground to be configured as another solenoid inductor, Figure 3.6, increasing the overall inductance of the element.

Table 3.2: Inductor comparison table for inductor designs in a 5-strata process.

	Style	**L (nH)**	**F$_{res}$**	**Q**	**Comments**
	(1) 3-turn nominal design	1.4	19.6	19.6	good balance between size, resonant frequency, and inductance
	(2) 3-turn extra wide	2.1	11.8	17	lowered Q and marked decrease in resonant frequency due to increased parasitics
	(3) 3-turn double inductor	4.5	10.5	2.6	idea based on transmission line theory

For reliability, the conventional design shown in Table 3.2, Style-2 was chosen as the primary geometry, and the number of turns could then be addressed, as Figure 3.7 shows. The number of turns was varied from zero (strip inductor) to 10 turns, and a determination of inductance, Q, and resonant frequency was made. Figure 3.8 shows that as expected, as the number of turns goes up, the inductance increases and the resonant frequency decreases. Figure 3.9 shows that for inductors of two turns and above, the quality factor does not vary significantly. From these results,

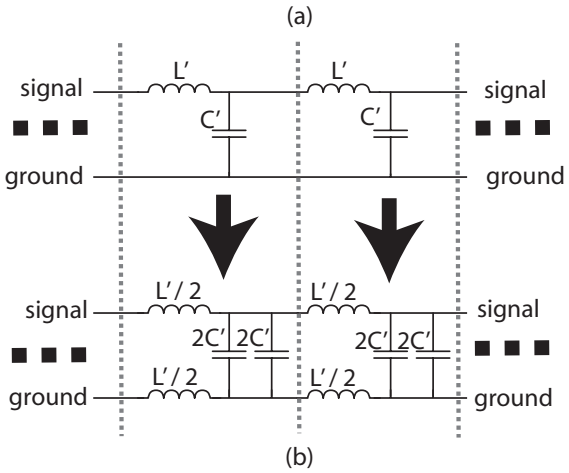


Figure 3.5: (a) Lumped element equivalent circuit for a lossless transmission line. (b) Alternate lossless transmission line circuit illustrating how ground path can have effects on line characteristics and performance.

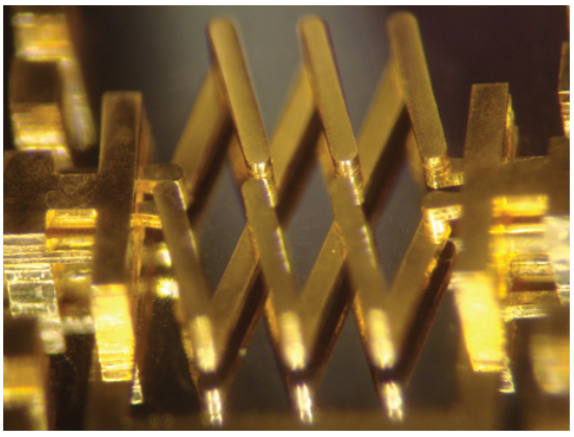


Figure 3.6: Illustration of a potential new type of inductor. This inductor is derived from the transmission line model of Figure 3.5(b) where inductance is presented not only in series with the signal line, but also in series with the ground line, theoretically doubling the value.

the 3-turn inductor was chosen as the base geometry, as its inductance and resonant frequency are comparable to a commercially available inductor for comparison. Once the number of turns was fixed, the design could be finalized by determining the best turn to turn spacing, overall length, and turn width to achieve a reasonable Q, and more importantly a resonant frequency between 4 and 18 GHz that would allow the inductor to be characterized around its resonant frequency

within the bands that the wafer calibration would support. Additionally, since the purpose of the inductor is as an RF choke, a parallel resonant circuit inline with a transmission line accomplishes this functionality well.

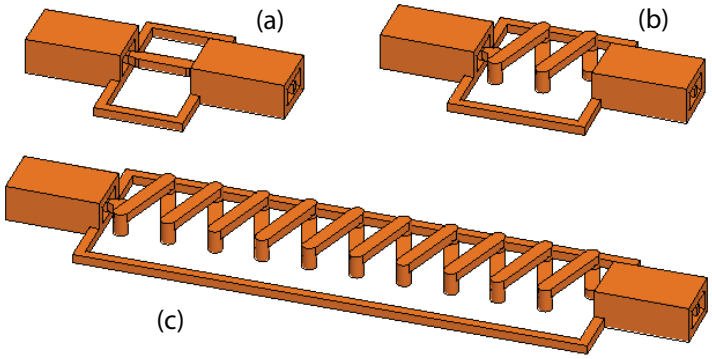


Figure 3.7: Three geometries simulated while varying an inductor's number of turns to determine the best geometry for fabrication: (a) 0-turn inductor, (b) 2-turn inductor, (c) 10-turn inductor.

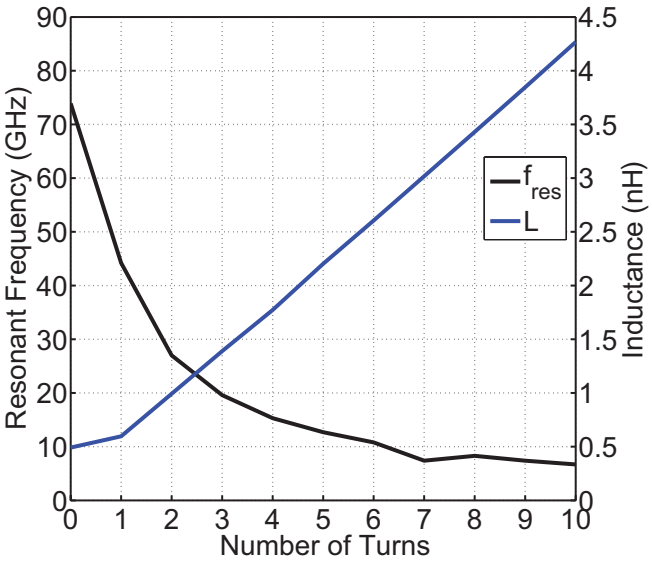


Figure 3.8: This figure is a graph of resonant frequency and inductance results for the HFSS inductor turns study. Given a calibration frequency range of 4 - 18 GHz, the 3-turn inductor was selected for its compact size, resonant frequency near the frequency range, and characteristics similar to a commercially available SMT inductor for comparison.

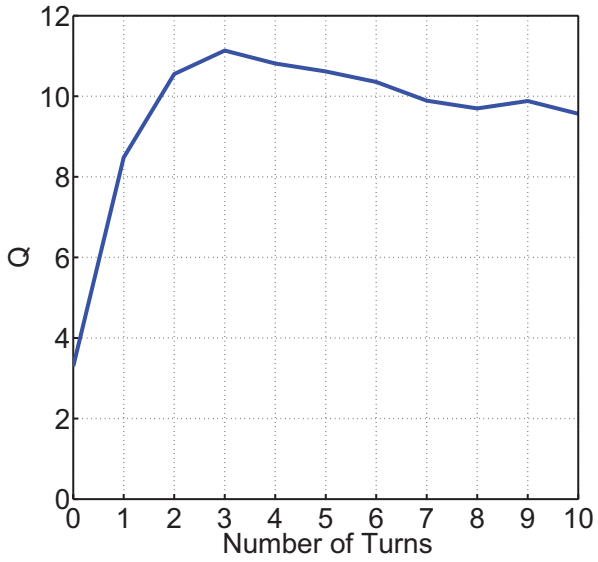


Figure 3.9: Resonant frequency Q factor results of the HFSS simulations of inductors varying from 0 to 10-turns in the PolyStrata^{TM} process.

3.4 Fabricated Inductor Results

Though a 3-turn inductor would serve as the primary geometry, three different inductors were fabricated, a 3-turn inductor, a 1-turn inductor, and a 0-turn or strip inductor, as shown in Figure 3.10. Similar to the 3-turn inductor, the 1-turn inductor was adjusted to obtain a resonant frequency between 4 and 18 GHz. The 0-turn inductor was fabricated in order to compare with analytical solutions for a strip inductor [46].

The inductance of the 3-turn and the 1-turn inductor were both slightly less than the 1.7 nH of inductance found by simulation, but as shown in Figure 3.11(a) the inductances are repeatable around 1.4 nH, an error of about 10%. The 0-turn inductors are also below their simulated inductance of 1.2 nH, reinforcing this trend of difference. The resonant frequencies, shown in Figure 3.11(b), follow simulation quite well. The 0-turn inductor is not shown, as its resonant frequency is above the highest measurable point (22 GHz). The 1-turn inductors the simulated resonant frequency is 13.55 GHz, and the average measured resonant frequency is 13.69 GHz for an error of 1%. Similarly, simulated resonant frequency for the 3-turn inductor is 12.38 GHz and the average mea-

sured resonant frequency is 12.39 GHz for an error of about 0.08%. Since the measured inductance is lower, this would indicate that the equivalent parasitic capacitance in measurement is slightly larger than that in simulation.

The Q values for the inductors are substantially different, however. Simulation showed Q's around 10, where Figure 3.12 shows measured Q values between 30 and 45. This is interesting considering the difference between inductances, but since that the losses in the inductors are very small and found in the denominator of Equation 3.6, a small difference in simulated and measured loss can cause large differences in quality factor. Table 3.3 provides a statistical summary of the measured and simulated performance.

Table 3.3: Summary of simulated and measured performance for 0-, 1-, and 3-turn inductors.

Parameter	Number of Turns	Simulated Value	Measurement Average	Standard Deviation
Inductance	0-turn	1.16 nH	0.98 nH	0.061
	1-turn	1.65 nH	1.36 nH	0.051
	3-turn	1.70 nH	1.43 nH	0.047
Resonant Frequency	0-turn	30.0 GHz	$>$ 22 GHz	n/a
	1-turn	13.6 GHz	13.69 GHz	0.051
	3-turn	12.4 GHz	12.39 GHz	0.036
Q	0-turn	6.33	n/a	n/a
	1-turn	9.60	34.60	3.82
	3-turn	12.9	34.02	5.28

3.5 Current Handling

One of the major shortcoming of all RF inductors is the current handling capability, also called ampacity. In order to maintain low parasitics and high resonant frequencies, ampacity is almost always sacrificed. The inductors fabricated in the PolyStrata^{TM} process have inductance, Q factor, and resonant frequencies comparable to commercially available SMT inductors; however, where a 1.2 nH SMT inductor has a current limit of 2.1 A [47] the current limit of PolyStrata^{TM} inductors is much, much higher.

Neglecting the interconnect and circuit external to the inductor, the inductor can be treated as a wire when calculating ampacity. Though many rules of thumb exist (e.g. 4 A/mm^2 for insulted

wire and $6\,A/mm^2$ for wire in air, or diameter (in inches) $4869.48 \cdot d^2$ for magnet wire [48]), most commonly a table is used to determine how much current a wire can handle, often for a given temperature rating, as is the case with the National Electrical Code (NEC) Table 310.16 [49].

For bondwires and other wires whose diameters are not found in the NEC table, some manufacturers use military specifications to derive ampacity [50]. Section 3.5.5.3 of MIL-M-38510 [51] prescribes that for wires not in thermal contact with a substrate (i.e. inductors), the current should be limited by the equation

$$I = Kd^{3/2}, \tag{3.7}$$

where I is the maximum allowed current, K is a material and length dependent constant, and d is the diameter (or equivalent diameter) of the wire. When taking into account a square cross section, Figure 3.13 can be created to predict behavior. The design goal of the inductor was to handle 2.5 A of current. The inductors tested were 5-strata inductors, whose windings were 100 μm by 100 μm or 150 μm diameter columns. From Figure 3.13, one would expect that these inductors will handle almost 12 A of current, however, the lines are only 82um by 100um (cross section equivalent to 90 μm), so they should handle 5.2 A of current. Testing revealed that these inductors in fact did handle in excess of 5.0 A, a safety margin of 2 over the design goal of 2.5 A and more than double a commercially available SMT inductor (2.1 A [47]).

3.6 Limitations of the PolyStrata^{TM} Process

The PolyStrata^{TM} process has a few limitations. First of all, since the copper must be grown, a seed layer must exist below all copper. While not a limitation, per se, as the number of gold seed layers increases, the complexity of the manufacturing increases, and the yield of the build decreases. While this does not mean that a build cannot be accomplished, it is possible for delamination to occur, and in turn entire sections of the inductors then wash away during the photoresist evacuation phase of manufacture. Another limitation is aspect ratio, both for gap and for copper. Aspect ratio is essentially a minimum width requirement. For example, if a strata has a height of 50 μm, and

the aspect ratio requirement is 0.9 for copper, the minimum width of copper must be at least $50\,\mu\text{m} \cdot 0.9 = 45\,\mu\text{m}$. This requirement means that when making an air-coil inductor, the top and bottom of the inductor will be limited to a minimum cross section, which may interfere with design constraints. The primary limitation of the process so far as inductors are concerned is the minimum area requirement. This requirement means that although the aspect ratio requirement may be met, a structure may not be acceptable because there is not enough of a copper footprint. An example which encompasses all of these limitations is the conical inductor, shown in Figure 3.14. In this case, because the air-core inductor has windings on many strata, many gold seed layers would be required. Each horizontal section of the inductor is limited in minimum cross section not only by the height of the strata, but also the aspect ratio which governs the minimum width of the section. Finally, each of the sides of the air-coil inductor need not only be at least 100 x 100 μm to satisfy aspect ratio, they need to be larger than that to satisfy a minimum area requirement (e.g. 150 μm diameter instead of 100 μm diameter). While the first limitation increases the simplicity of the design, it is not a requirement, only a best practice limitation. The latter two limitations although limiting the inductance achievable effectively ensure that any given PolyStrata^{TM} inductor will have high DC current handling due to a relatively large cross section.

3.7 Conclusions and Contributions

The primary contribution of this chapter is the design and demonstration of coil inductors made in a 3-D air process, allowing low parasitic capacitance and a variety of inductor geometries. The inductors handle record current levels of 5 A for their inductance, quality factor, and size. Furthermore, these inductors add an extra aspect to the PolyStrata^{TM} design toolbox, enabling lumped matching elements and bias tees. This work is the basis of results reported in [37].

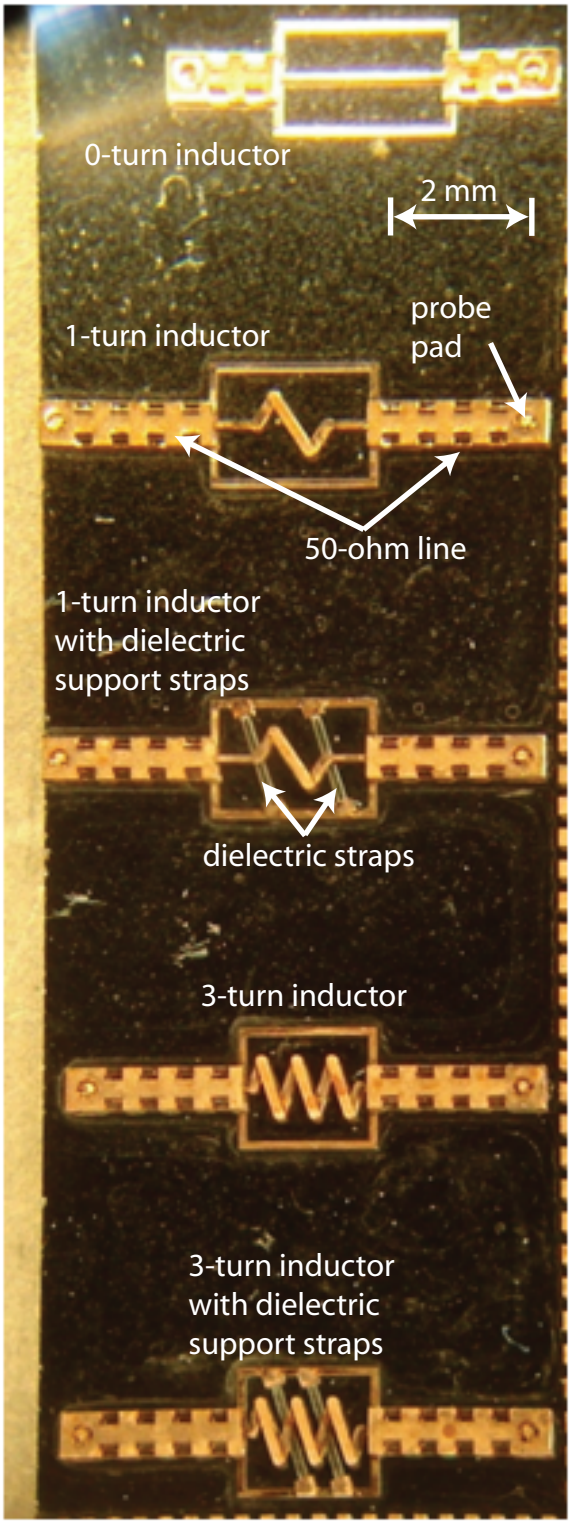


Figure 3.10: Photograph of fabricated inductors on a silicon wafer. Dielectric straps were added to determine if their role as potential structural support for considerably longer inductors (e.g. 10 turns) would be feasible. The 1-turn inductor geometry was adjusted to allow characterization of resonant frequency within the 4 - 18 GHz frequency range.

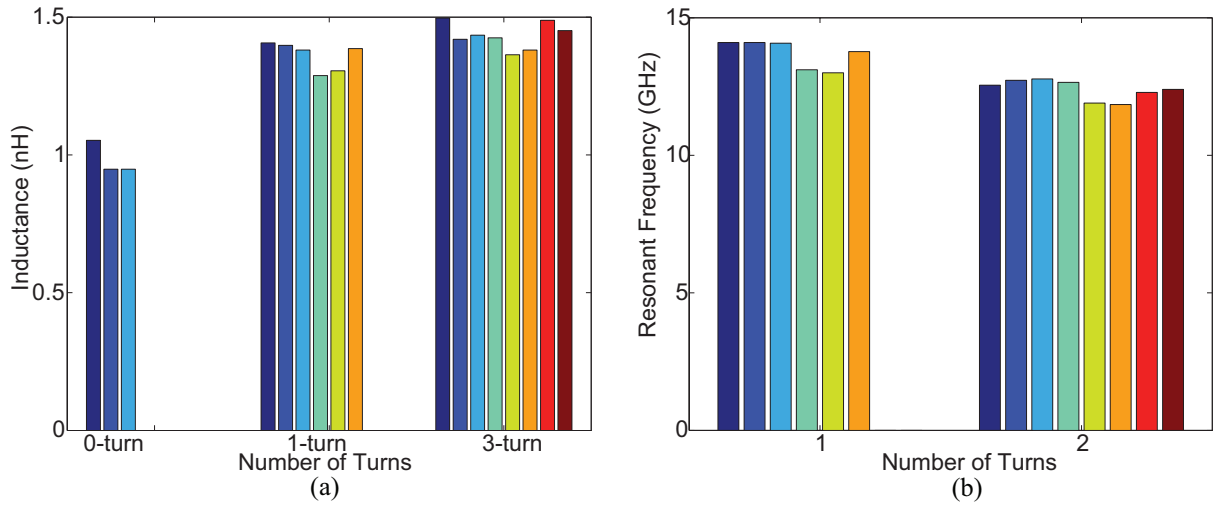


Figure 3.11: A bar graph displaying the variance in (a) inductance for three different cases of PolyStrata^{TM} inductors and (b) resonant frequency for two different cases of inductors (the 0-turn resonant frequency was higher than the measurable range). The inductance values are about 10% lower than predicted by simulation, while the measured resonant frequencies are well within 1% of simulation.

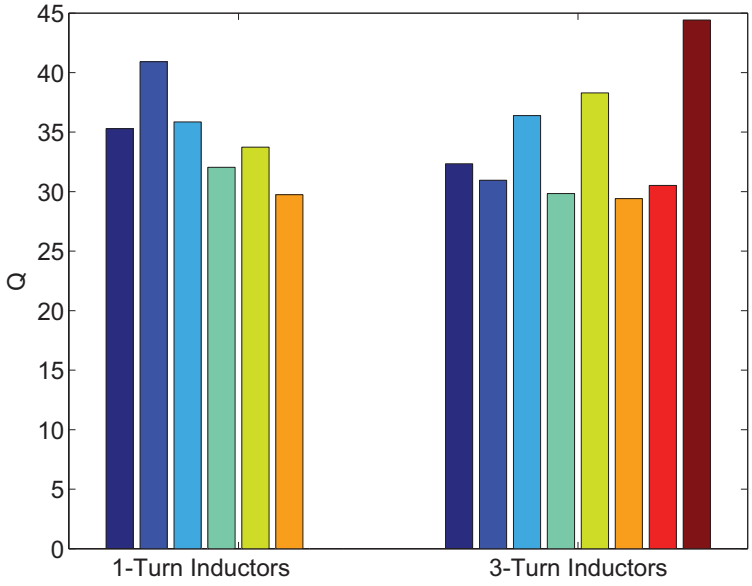


Figure 3.12: A bar graph displaying the variance in resonant Q for measured 1-turn and 3-turn inductors. The 0-turn inductor variation is not included as the resonant frequency was above the maximum measured frequency, so Q at resonance could not be measured.

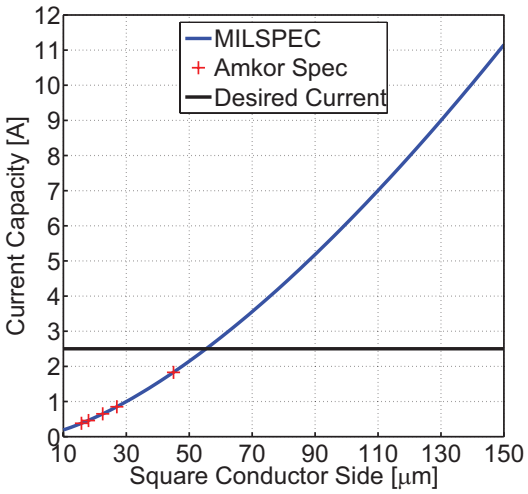


Figure 3.13: Current capacity (ampacity) as defined by Equation 3.7. The Amkor specifications are for copper bondwires of various diameter that Amkor offers. The design goal for the current handing of the inductor is 2.5 A, but for the inductor as fabricated, 10 A should be the failure point. However, since the lines have a smaller cross section than the inductor, the predicted failure is at 5.2 A, which corresponds well with the observed failure which occurred above 5.0 A. Comparable commercially available SMT inductors are specified as handling 2.1 A.

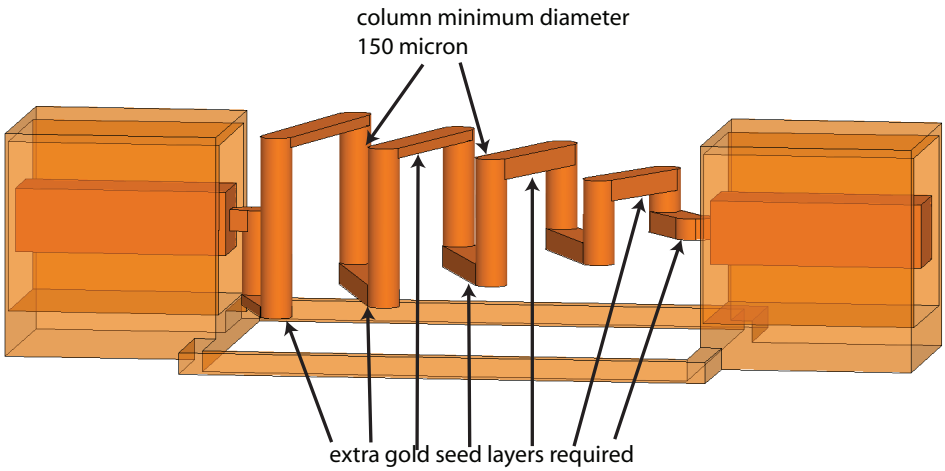


Figure 3.14: Conical inductor design highlighting the need for a significantly larger number of gold seed layers as well as where the minimum diameter / minimum footprint requirement is a limitation.

Chapter 4

Bias Tees

4.1 Introduction

This chapter presents miniature broadband bias tee networks designed in a micro-coaxial environment. Bias networks are a necessary part of every active microwave circuit. These three port devices are generally characterized in terms of input and output RF match, isolation between RF and DC ports, insertion loss, bandwidth, DC current handling, RF power handling, and size. For example, commercially available connectorized bias tees cover the range from a few hundred MHz to 50 GHz [52]. Broadband bias tees typically are limited to 500mA current handling and 2 W RF power, while narrow-band (e.g. 0.8-1 GHz) components handle up to 5 A of DC current [53]. Surface mount bias tees, which have a footprint of about 32 by 28 mm^2, are also available [54] and handle about 0.5 A and operate up to 4.2 GHz.

The goal of this work is to demonstrate miniature bias tees with high DC current and RF power handling capabilities that are compatible with the micro-coaxial, wafer-scale environment called the PolyStrata^{TM} process explained in Chapter 1. These bias tees will be designed using the sockets described in Chapter 2 and inductors both monolithic, as described in Chapter 3, as well as off the shelf chip inductors in PolyStrata^{TM} sockets.

This chapter presents broadband microcoaxial bias tees with a footprint around 8mm^2 as shown in Figure 4.1 where surface mount capacitors are assembled into the micro-coaxial environment. Various components required for the bias tee are described, followed by results of several bias tee designs for 4-18 GHz operation.

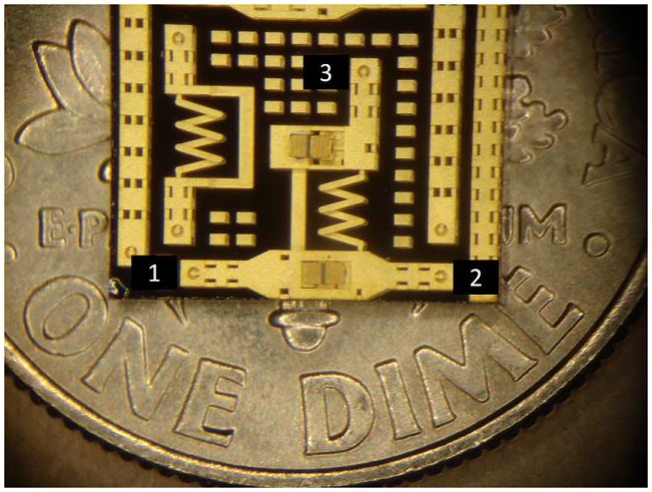


Figure 4.1: A gold-plated bias tee fabricated in the PolyStrata^{TM} copper process on an optically flat substrate. The RF ports are labeled 1 and 2, while 3 is the DC port. All ports are compatible with standard 150 μm and 250 μm pitch CPW probes for testing. This bias tee includes two 0402 capacitors which are hybridly assembled into the microcoaxial environment while the inductor is fabricated monolithically in the PolyStrata^{TM} process. The size of the bias tee is around 8 mm^2

4.2 Bias Tee Design and Characterization

Bias tees are commonly designed for 50Ω input and output impedances at the RF ports, which is convenient for all active devices pre-matched to 50Ω . MMICs usually have integrated biasing networks which take up a significant portion of the expensive real-estate [8], and in addition require off-chip capacitors for stability. The bias tees presented in this work are designed for MMICs which do not use valuable semiconductor area on passive bias elements, and which can also be designed with lower impedance input and output ports. Thus, it would be useful to have bias tee circuit designs for various characteristic impedances. For example, a 12.5-Ω bias tee is designed on both sides of a socket which houses a low impedance 4-16 GHz power amplifier MMIC with no on-chip bias networks. The 12.5Ω ports are then matched to 50Ω RF input/output through a ultra-broadband microcoaxial impedance matching network. This 4:1 impedance transformer has a 11:1 bandwidth (2-22 GHz) with a small and flat group delay, and is described in [55].

This chapter discusses both 12.5 Ω and 50 Ω bias tee networks. To characterize the assembled surface mount devices in the sockets, as well as the bias tees, PolyStrata^{TM}-based TRL calibrations

standards were designed to cover 2-7 GHz and 7-22 GHz. The calibration standards included transitions from CPW probes to the microcoax, referred to as launches, described in detail in [35]. The reference plane was defined at the edge of the socket in Figure 4.2(a). Measurements of non-50Ω impedance devices are de-embedded from 50Ω calibrated measurements.

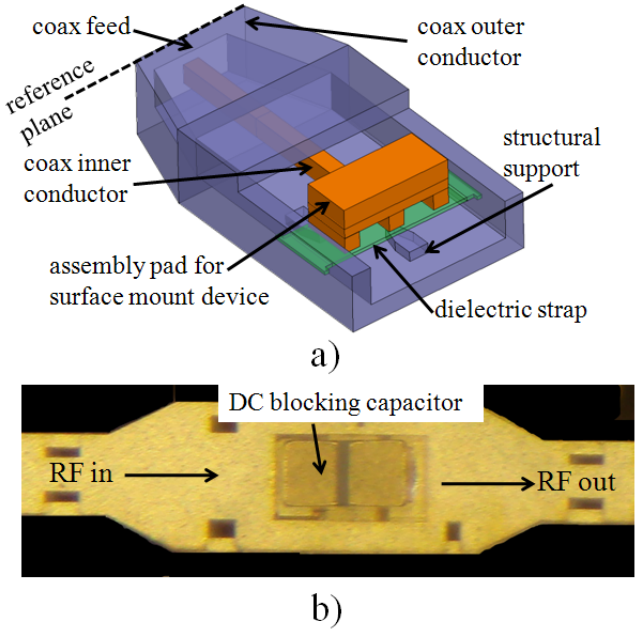


Figure 4.2: (a) 3-D geometry of one-half of a surface mount component assembly structure (socket) in the copper-based microcoaxial environment referred to as PolyStrata^{TM}. (b) Photograph of a 0402 packaged blocking capacitor mounted in a series socket between two microcoaxial lines.

4.2.1 Bias Tees in a 12.5 Ω Environment

Photographs of two 12.5Ω bias tees are shown in Figure 4.3: one with a surface mount commercially-available 2.2 nH inductor with a resonant frequency of 15 GHz, and the other with a monolithically integrated 3-turn inductor with simulated inductance of 3.1 nH and a resonant frequency around 12 GHz. Each bias Tee has an 0402 series blocking capacitors (3 pF) and an 0402 shunt capacitors (3 pF) at the DC port. The bias tee circuits can also be tuned for specific parameters, such as offsetting parasitic inductance that occurs when wire bonding to a chip. Such tuning can be done with the addition of a shorted stub (Figure 4.3(b)) or introducing other parasitics by

altering the geometry of the transmission line. Figure 4.4 shows measured and simulated performance for the two bias tees. The simulations were performed with Ansofts HFSS finite element code and include all details of the geometry. The surface mount components are modeled as impedance sheets with appropriate value of surface reactance, and with dimensions given by the package. The insertion loss and match for a bias tee with a surface mount inductor are shown in Figure 4.4(a), and the performance for a bias tee with a PolyStrata^{TM} monolithic 3-turn solenoid choke is shown in Figure 4.4(b). Both designs show a better than 0.7 dB insertion loss from 4 to 16 GHz with a better than 12 dB match. The bias tees were used with no degradation in a 20 W power amplifier with over 2 A of DC current. All the 12.5 Ω measurements were fitted with a geometric taper from the 12.5-Ω geometry to the 50-Ω geometry to allow for the measurements taken in Figure 4.4. Since this taper was not able to be separately measured nor calibrated out, an HFSS model was used to obtain scattering parameters which were then used to de-embed the tapers. Figure 4.5 shows that the tapers do not significantly impact the transmission through the four bias tees, and when the tapers have been removed from measurement, return loss improves by as much as 5 dB. A 3-port TRL was not available, so isolation measurements were not taken, though simulation shows that the DC line is isolated 20 dB or better for all impedances presented.

4.2.2 Bias Tees in a 50 Ω Environment

The 50 Ω bias-tees designs differ from the 12.5 Ω bias tees not only in the impedance of the RF transmission line geometry, but also the inductor. Since the DC line is now of the same impedance as the signal line, there is more loading of the RF path by the DC line, leading to reduced isolation. In order to attempt to increase the isolation, the monolithic inductor was made a larger value. When measured on a 2-port network analyzer with the isolated port open, a reflection now occurs around 7 GHz, as seen in Figure 4.6. In order to understand this resonance, measurements were performed with a power meter and source to monitor the reflection, isolation and transmission, and the results are shown in Figure 4.7. These measurements show that when the isolated port is terminated, the resonance does not exist.

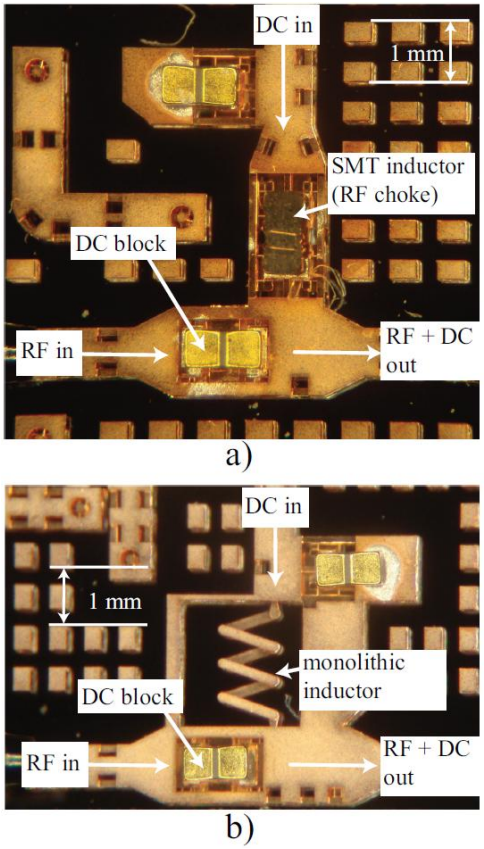


Figure 4.3: (a) Photograph of a bias tee implemented in microcoaxial 12.5Ω impedance lines with a surface-mount blocking capacitor and RF shorting capacitor, and surface-mount Coilcraft choke. (b) Photograph of bias tee with a monolithically integrated PolyStrata^{TM} 3-turn solenoid inductor choke.

4.3 Conclusions and Contributions

The primary contribution of this chapter is the heterogeneous integration of the PolyStrata^{TM} process with a proprietary amplifier in the GaN process as well as commercially available surface mount passive devices. This integration was done in the form of miniature high current high-power bias-tee networks in both 12.5 Ω and 50 Ω microcoaxial impedance environments, and shows the viability of moving passive components off of MMICs allowing more efficient use of chip area potentially reducing cost.

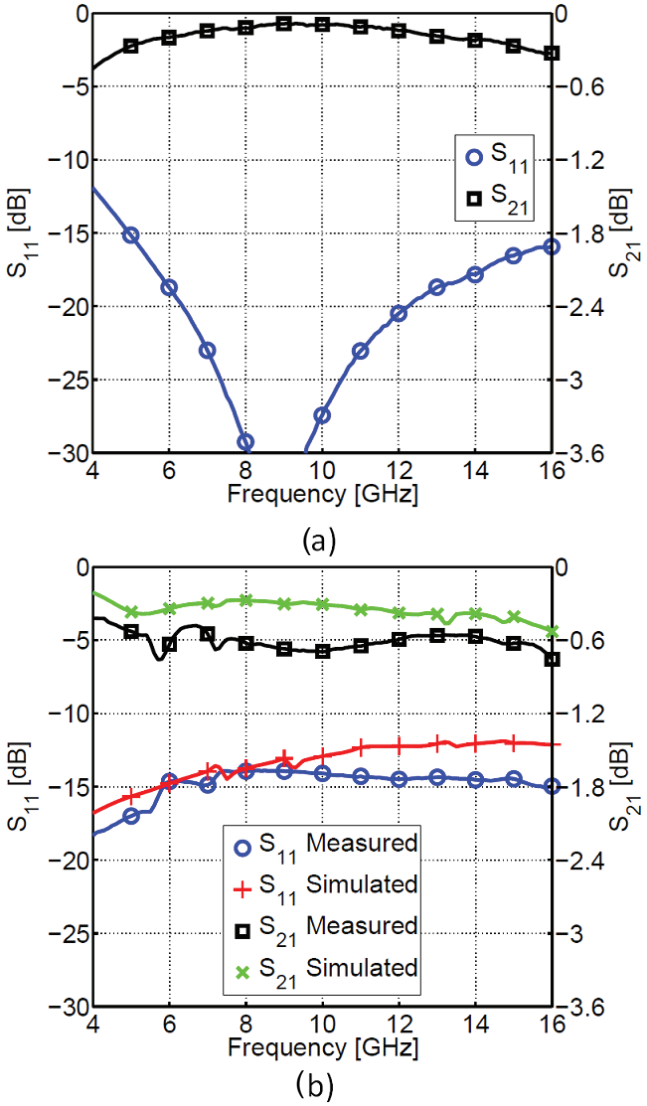


Figure 4.4: Measured insertion loss and match for (a) the bias tee from Figure 4.3(a) which uses a surface-mount choke and (b) measured and simulated loss and match for the bias tee with a monolithically integrated inductor from Figure 4.3(b).

The bias tees discussed in this chapter compare favorably with other bias tees in various technologies as shown by Table 4.1. The most striking contributions of the bias tees are the greatly enhanced current and RF power handling capability demonstrated, while maintaining a compact size, low insertion loss and return loss, and a large 3 dB bandwidth. Furthermore, the PolyStrata^{TM} bias tees are versatile in that they can be released from the native substrate and mounted on any

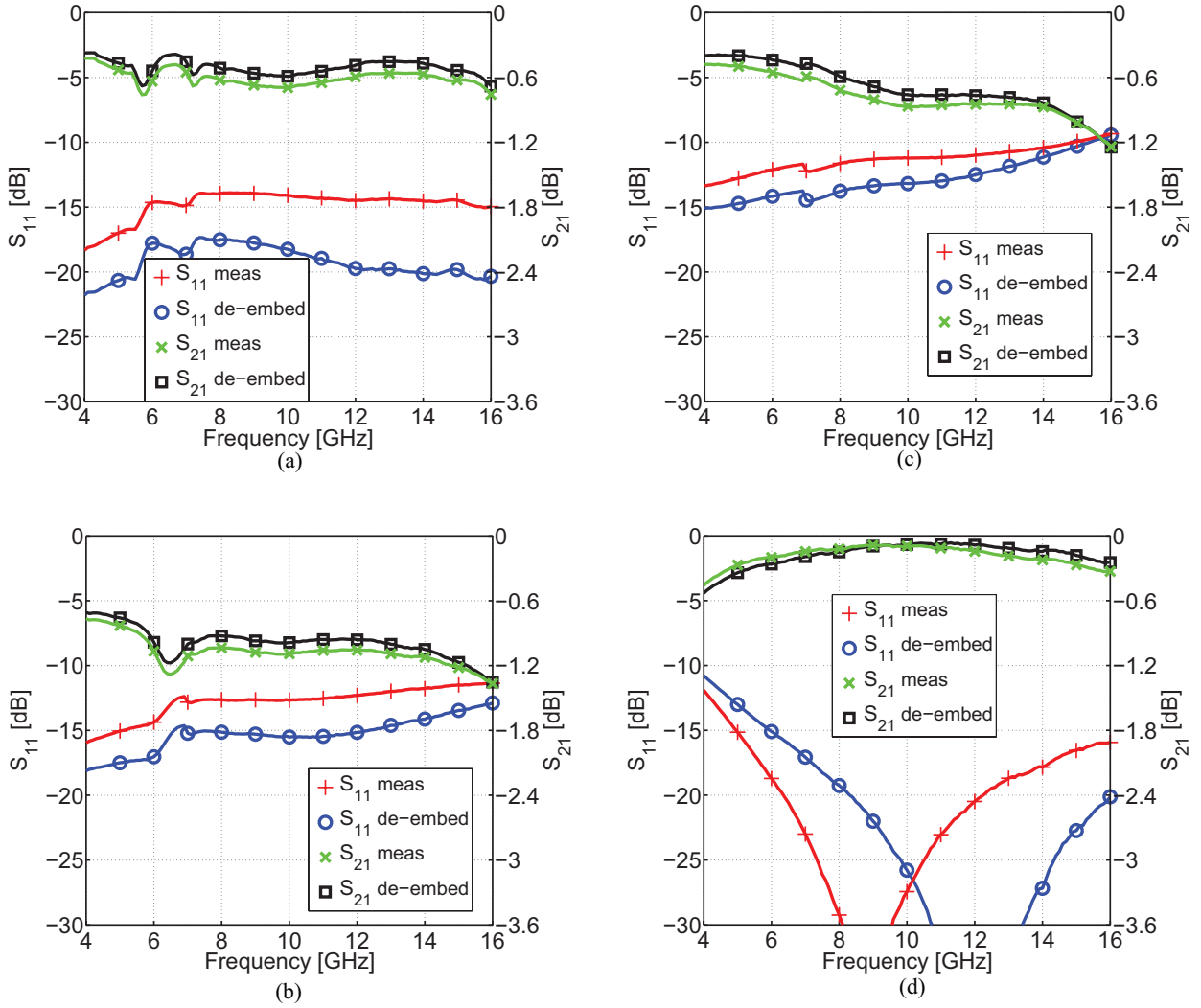


Figure 4.5: Comparison of bias tee performance both as measured and after geometric tapers were de-embedded from measurement data for (a) vertical transition bias tee (b)stub-matched bias tee (c) transmission line matched bias tee (d) SMT inductor bias tee.

hybrid circuit, as has been demonstrated with other components. In addition, the connections to CPW probes (launches) used in this work for measurements can be replaced by suitable transitions to a variety of media. The results of this chapter are reported in [5, 37].

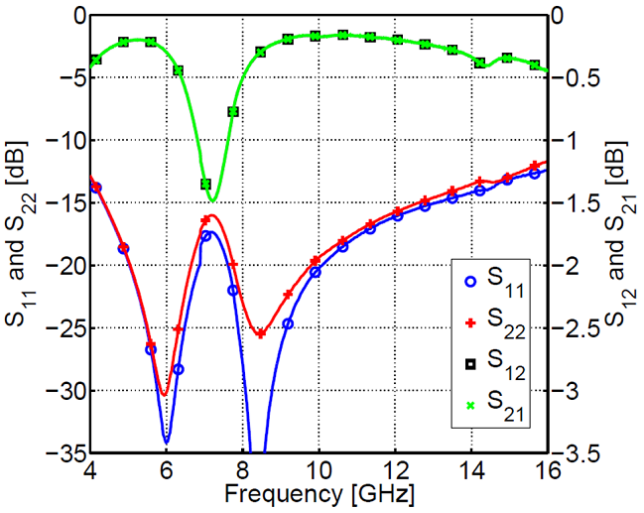


Figure 4.6: Measured insertion loss and match for a 50 Ω bias tee.

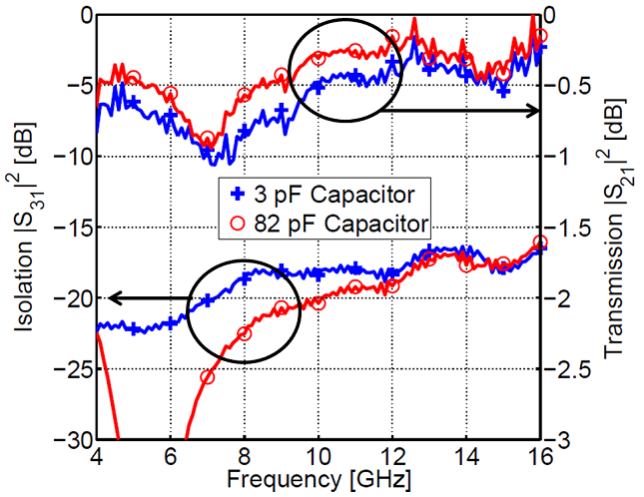


Figure 4.7: Measured isolation and transmission for the same 50Ω bias tee as Figure 4.6. The top two curves correspond to the measured transmitted power, and the bottom two to the power measured in the isolated port, normalized to the incident power. Measurements are performed for two values of SMD capacitors.

Table 4.1: Comparison of three bias tees in different technologies.

	Bias Tee Type		
	MEMS [56]	**Picosecond 5545 [56]**	**PolyStrata**
DC Current	50 mA	500 mA	> 5 A
RF Power	Not Available	2 W avg. max	20 W
Area	4 mm^2	645 mm^2	8.3 mm^2
BW (-3 dB)	20 GHz	20 GHz	18 GHz
Capacitance	8.2 pF	30 nF	3 pF
Inductance	18 nH	340 μH	1.2 nH
Insertion Loss	< 1.5 dB f < 24 GHz	< 1.5 dB f < 12 GHz	< 1.5 dB f < 18 GHz
Return Loss	> 10 dB f < 24 GHz	> 12 dB f < 14 GHz	> 10 dB f < 18 GHz

Chapter 5

G-band Frequency Scanned Slotted Waveguide Array Design

5.1 Introduction

This chapter addresses design, simulation, and fabrication of a G-band, frequency-scanned, slotted-waveguide array in the PolyStrata^{TM} process. Beam steering is usually accomplished with phase shifters distributed in the feed network of an antenna array [57, 58]. At millimeter-wave frequencies above V-band, however, phase shifters either do not exist or are lossy and expensive [59, 60]. Another way to accomplish beam steering is by frequency scanned arrays [61, 58]. In this approach, an array of antennas is fed serially with a dispersive feed line, and a frequency variation along the feed corresponds to phase changes between elements, which results in beam scanning. Usually, a large bandwidth is needed to accomplish a wide scan angle.

Frequency-scanned arrays have been used for radar since the 1950s [62], and have been implemented from S to Ka bands in waveguide [63, 64]. Usually, dominant-mode rectangular waveguide is used for the feed, and slot antennas are machined in the broad [65, 66, 67] or narrow [68, 69, 70] walls of the waveguide. Waveguide is dispersive, so shorter feed sections can be used for substantial phase shifts. However, microstrip quasi-TEM feeds have also been implemented, e.g. in an L-band, vertically-polarized phased array of 18 elements with 100° steering [71]. A microstrip array with 13 elements was demonstrated in the 5.8 GHz ISM band using a microstrip feed for folded dipole antennas. Since the ISM band is narrow, lossy bandpass filters were inserted between elements to increase dispersion and allow scanning of 100° within a 2.5% bandwidth [72].

This work presents a frequency scanned antenna array for planetary landing radar [9, 10].

Since it is desirable to have a very small and lightweight antenna which is intended to operate in an atmosphere with low attenuation, the band chosen for this work is 130-180 GHz. In this frequency range, phase shifters do not exist and frequency scanning is an attractive solution. The standard dominant mode rectangular waveguide in this band is WR-05 (1.295 by 0.648 mm in cross-section). A micro-fabrication process referred to as the PolyStrata^{TM} process [73] is adopted in this work for fabricating the waveguide feed, antennas, and adaptors to standard flanged waveguide. This process has been used in the past for fabricating micro-coaxial lines and components with low loss, high yield, light weight, and dense packing, [3, 29, 22, 18]. To the best of our knowledge, the components demonstrated here present the first micro-fabricated, dominant-mode, rectangular waveguide in this new technology.

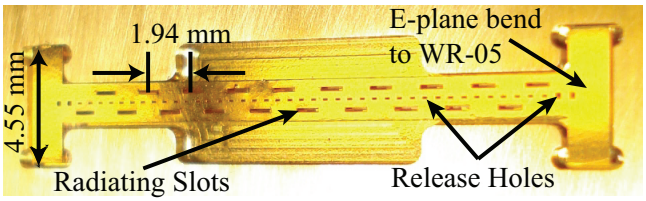


Figure 5.1: Photograph of a 20-element micro-fabricated slotted-waveguide traveling-wave array. The array is fabricated in copper, gold plated, and mounted on a brass fixture. The feed and termination are connected to standard WR-05 through a custom designed E-plane bend. The overall array length between the E-plane bends is 2.06 cm.

5.2 Slot Design

Slotted waveguide arrays can be realized in several different ways. First, the slots can be either in the broad wall of the waveguide or in the narrow wall (also called edge slot array). The waveguide itself can vary in type, with rectangular waveguide and ridge waveguide being the most common types for this application. The slots can be $\lambda_g/4$ (resonant) at the desired frequency of operation or they can be slightly larger or smaller (traveling-wave). Finally, the array can be fed from the end, center, or along the array. Often times the feed will be a sinuous feed [74, 61] in conjunction with synthesized antenna patterns (e.g. Taylor distribution) to create a 3D structure

that scans pencil beams by feeding the array with discrete frequencies (most commonly in X-band).

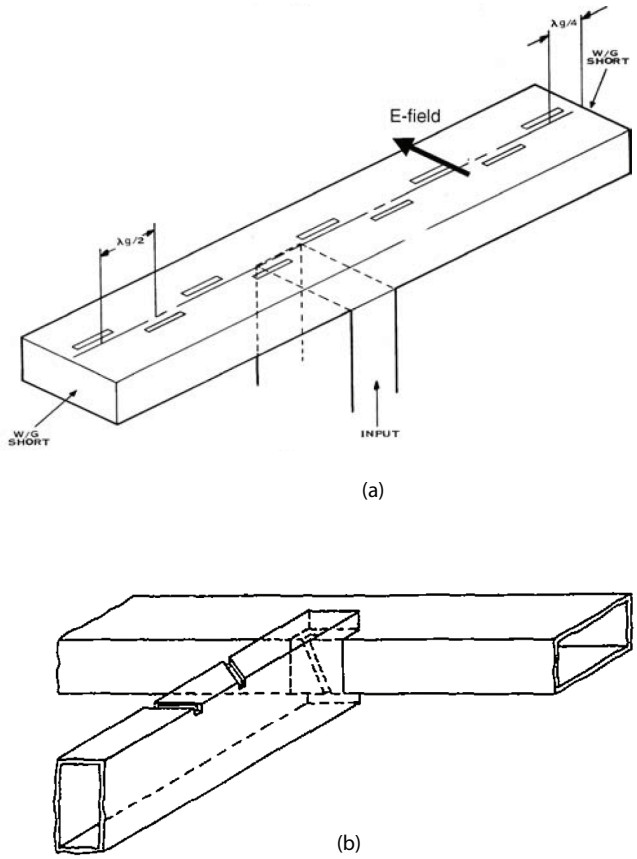


Figure 5.2: Illustration of different characteristics of a slotted waveguide array. Array (a) [61] is a broad-wall, resonant, center fed, slotted waveguide. The waveguide shorts at the end of the array create a standing wave, which is characteristic of a resonant array, along with all the spacings corresponding to multiples of $\lambda_g/4$. Array (b) [61] is a narrow-wall (or edge-slot), end fed, slotted array. If the slots are not spaced $\lambda_g/4$ apart, it is a traveling-wave array; however, if they are spaced $\lambda_g/4$ apart, it will be a resonant array.

The design goals of the work presented here were for a linear, broadband array that performs continuous scanning for space borne applications that have severe volume and mass constraints. The bandwidth disqualified the narrow-band resonant slot array. Fabrication requirements constrain the design to broad-wall slots, and though ridge waveguide is possible in the PolyStrata^{TM} process, an end-feed, rectangular waveguide was selected. Thus, the architecture chosen is a end-fed, broad-wall, traveling-wave, slotted, rectangular waveguide array.

Consideration was given to arranging the slots to conform to a Tchebychev [75] or a Taylor distribution [66], but since the dispersion of the waveguide alters the phase of the power arriving at each slot, the distributions effectively become frequency-dependant. Although either the Taylor or the Tchebychev at a single frequency will have lower sidelobes and a narrower beamwidth, the uniform slot distribution ensures broadband radiation patterns. Figure 5.1 shows a uniformly distributed slot array, with slot to slot spacing of 0.97 mm, slot length of 0.88 mm, and width of 0.15 mm.

Table 5.1: Summary of waveguide parameters.

Waveguide	h (mm)	w (mm)	$\lambda_{TE10}^{130\,GHz}$	$\lambda_{TE10}^{180\,GHz}$
PolyStrata	0.675	1.295	2.31	1.67
WR-05	0.648	same	same	same

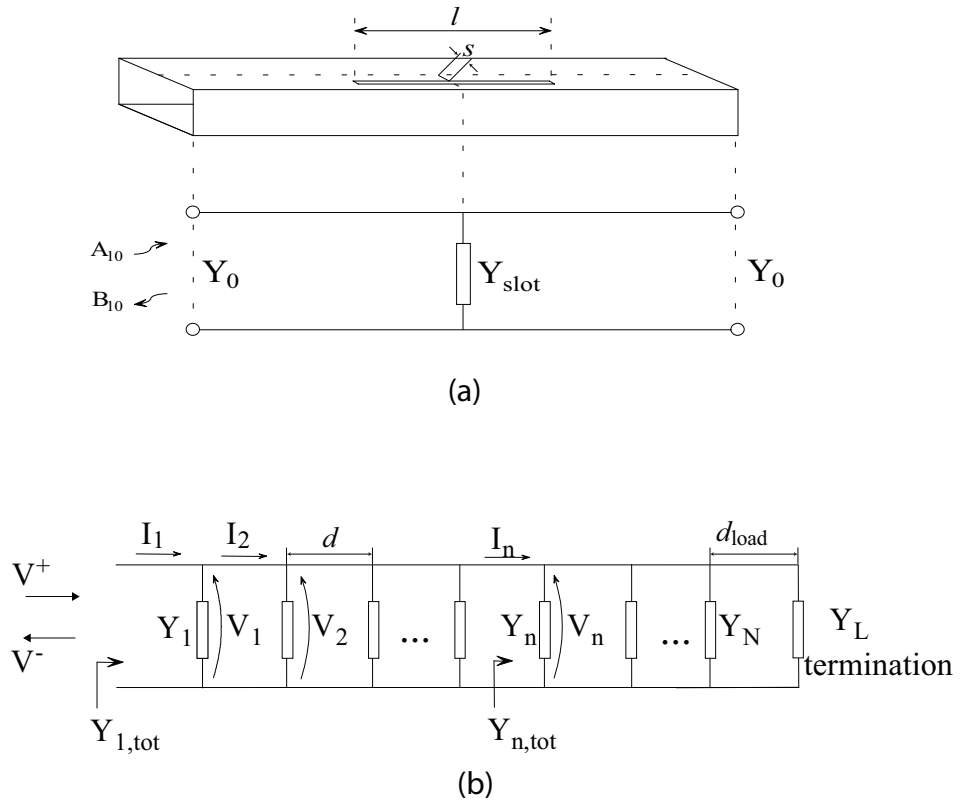


Figure 5.3: Equivalent circuit of a single slot (a) and an array of slots (b). The admittance of a single slot depends on its length (l), offset from the center of the waveguide (s), and frequency (f).

The antenna array initial design follows the procedure outlined by Elliott [67, 76] and Volakis [77] that have been implemented by various authors [78, 79]. The array can be modeled as a series of shunt complex admittances, whose normalized conductance can be found by [80]

$$g = \frac{2.09a\lambda_g}{b\lambda_0}\cos^2\left(\frac{\lambda_0\pi}{2\lambda_g}\right)\sin^2\left(\frac{x\pi}{a}\right), \tag{5.1}$$

where a and b are the waveguide's respective width and height, x is the slot displacement from the middle of the waveguide, λ_g is the guided wavelength, and λ_0 is the free space wavelength. The normalized admittance (y)of these slots can also be found from

$$y = \frac{Y(s,l,f)}{Y_0} = \frac{-2S_{11}}{1+S_{11}}, \tag{5.2}$$

where S_{11} is determined for the single slot from incident and reflected voltages, A_{10} and B_{10} as shown in Figure 5.3(a). For a uniform array, once this admittance is calculated, transmission line theory can then be applied to calculate the total admittance of the array as

$$y_n^{tot} = y_N + \frac{y_{n+1}^{tot}\cos\phi + \jmath\sin\phi}{\cos\phi + \jmath y_{n+1}^{tot}\sin\phi}, n = N-1, ..., 1 \tag{5.3}$$

where $y_N^{tot} = y_N + y_L$ and $\phi = \beta_{10}d$. From these admittances, the mode voltages can be calculated from [81]

$$V_n = V_{n-1}\frac{Y_{n-1,tot} - Y_{n-1}}{Y_{n,tot}\left(\cosh\left[(\alpha+\jmath\beta)\,d\right] + \sinh\left[(\alpha+\jmath\beta)\,d\right]\right)}, n = 2, ..., N \tag{5.4}$$

and the voltage of the first slot, V_1, is given by the relationship

$$S_{11} = \frac{1-Y_{1,tot}}{1+Y_{1,tot}} \Longrightarrow V_1 = V^+\left(1+S_{11}\right) = \frac{2V^+}{1+Y_{1,tot}}. \tag{5.5}$$

Elliott [82] shows that by assuming an array of N narrow slots (where $n = 1$ to N) and a slot length, the slot voltages V_n^s can be found from the mode voltages V_n above. These slots are mutually coupled, so an $N \times M$ matrix of coupling coefficients, g_{mn} describes the array. Thus, the radiation pattern can be obtained from the slot voltages, which can be found using an iterative algorithm given by Gatti and Dionigi [81].

Although parts of the above procedure were used to calculate initial slot dimensions, a full-wave simulator was used to analyze fields and scattering parameters. A common design practice is

to ensure that approximately 10% of the power incident at the feed port of the array is delivered to the termination, implying a maximum radiation efficiency of 90%. In the case presented here, this common practice was not adhered to in order to increase gain by dissipating less power as noted in [70]). The resulting non-uniform illumination of the end slots manifests itself as reduced gain flatness and a nonmonotonic frequency steering function (how the beam moves as frequency changes) . To verify the tradeoff between maximum radiation efficiency and gain flatness / steering function, a 10-slot and a 20-slot array were designed, the former with more power dissipated in the termination with a more linear steering function expected.

5.3 Array and Feed Fabrication and Packaging

The PolyStrata^{TM} waveguide, due to its versatility and small feature size, is ideal for use with waveguide above W-band. In this design, the waveguide has the same width as WR-05, resulting in the same dominant-mode cutoff frequency, guided wavelength, and dispersion characteristics. The difference between the PolyStrata^{TM} waveguide and standard WR-05 rectangular waveguide is the height, as summarized in Table 5.1. The equal widths (w) allow straightforward transitions to fixtures required to feed and characterize these structures. For example, the traveling-wave feed requires a termination, and a commercially available, low-VSWR, WR-05 load can be connected easily by adding a 90-degree PolyStrata^{TM} bend as discussed below.

The PolyStrata^{TM} process height requirements prevent direct connections to WR-05, so an E-plane bend was designed to feed the array at a 90° angle, as shown in Figure 5.5. The reflection coefficient of the bend ($|S_{11}|$) is below -30 dB. The PolyStrata^{TM} waveguide to WR-05 E-plane bend and its S-parameters are shown in Figure 5.4.

5.4 Connection to Standard Waveguide

To connect to a standard WR-05 flange [83], a brass fixture with WR-05-sized waveguide through-vias is designed Figure 5.6(a) and machined using EDM (electro-discharge machining). The PolyStrata^{TM} array is attached to the fixture using gold-to-gold thermosonic bonding [84].

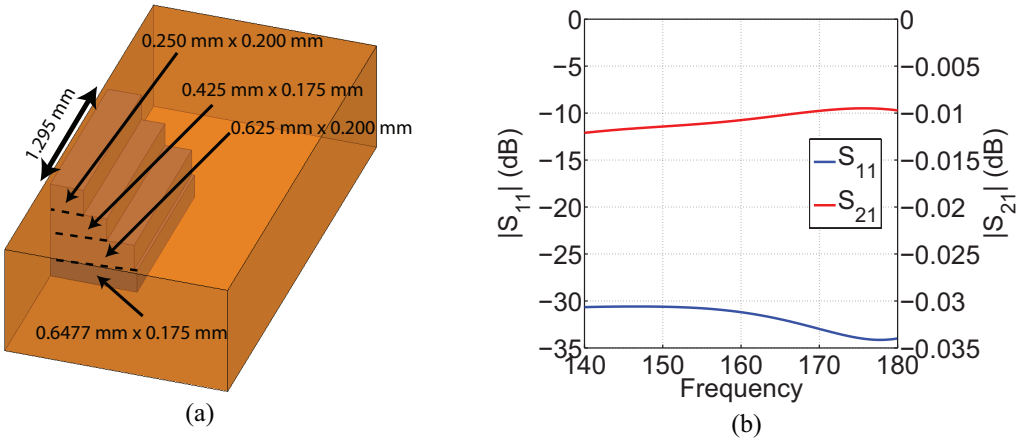


Figure 5.4: The geometry of the E-plane bend (a) uses a stair-step approach that follows the gold seed layers for height. This E-plane bend also accomplishes the transition from PolyStrata^{TM} waveguide (1.295 mm by 0.675 mm) to WR-05 (1.295 mm by 0.6477 mm) all while maintaining $|S_{11}|$ below -30 dB (b).

The brass fixture then connects to a grid matching aluminum mount (for weight reduction) which then connects to the antenna rotation stage as shown in Figure 5.6(b).

Since EDM yields waveguide with rounded corners, the brass waveguide was dimensioned to be 1.359 mm (53.5 mil) wide by 0.660 mm (26 mil) high to account for the corners' radius of curvature of 0.178 mm (7 mil). These dimensions were chosen based on full-wave simulation of the transition from WR-05 to the rounded brass flange to the size of the E-plane bend. Taking into account both machining tolerance and placement tolerances, the scattering parameters for this brass through-via waveguide is shown in Figure 5.7.

5.5 Simulation

A 10-element array was initially designed so that each slot would be resonant midband and have a normalized midband conductance of approximately 0.08. Upon simulation of the entire array, the VSWR, shown in blue in Figure 5.8(b), was found to be above 2:1 both at bottom and top of the frequency band. The design was then parameterized so that the length of the slot, the width of the slot, the slot-to-slot spacing, and the offset of the slot from the centerline of the

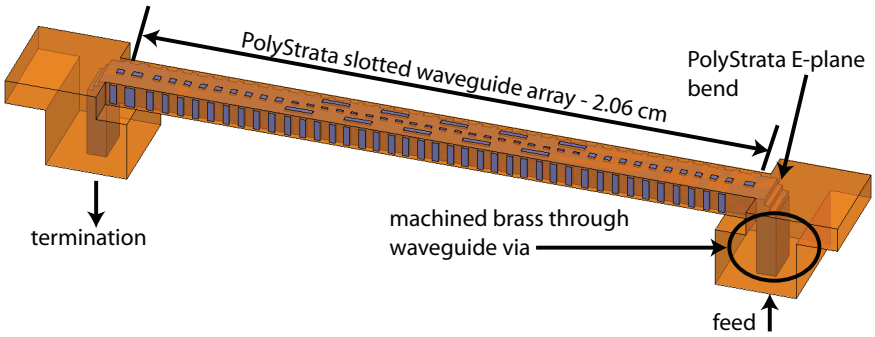


Figure 5.5: 10-element slot waveguide array with E-pane beds and waveguide through-via connections shown. The holes on the vertical walls and the smaller holes on the horizontal top wall are release holes necessary for the fabrication and they do not impact the electromagnetic performance in the frequency range of interest. The 20-element array from Figure 5.1 has the same geometry.

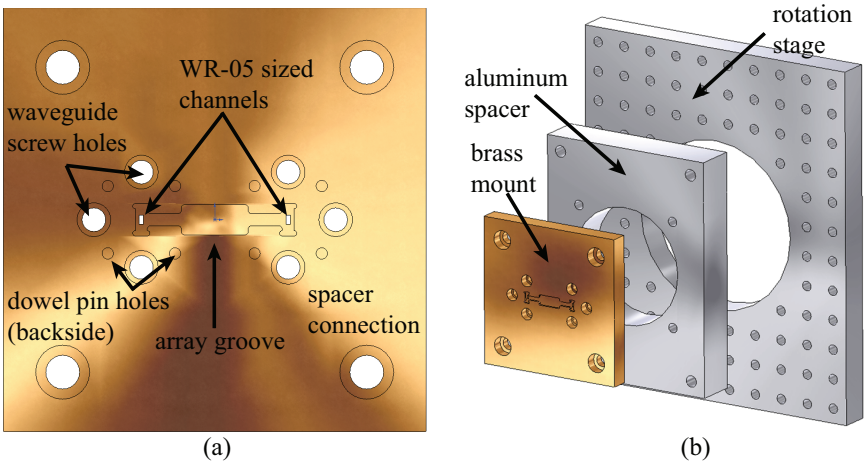


Figure 5.6: Sketch of (a) the brass mating flange and (b) the assembly structure for radiation pattern measurements. The micro-fabricated waveguide array is mounted in the grove so that the E-plane bends connect directly to the waveguide through-vias.

waveguide could be independently varied. The array performance could then be improved to a final 10-element design, shown in red in Figure 5.8(a)-(d). This 10-element design could then be doubled in length to form a 20-element design, shown in black in Figure 5.8(a)-(d).

Along with lowering the VSWR, a goal of increasing the maximum radiation efficiency was established. Maximum radiation efficiency is essentially a measure of how much power is being radiated for a given input power absent loss. The radiated power, P_{rad}, depends on the power

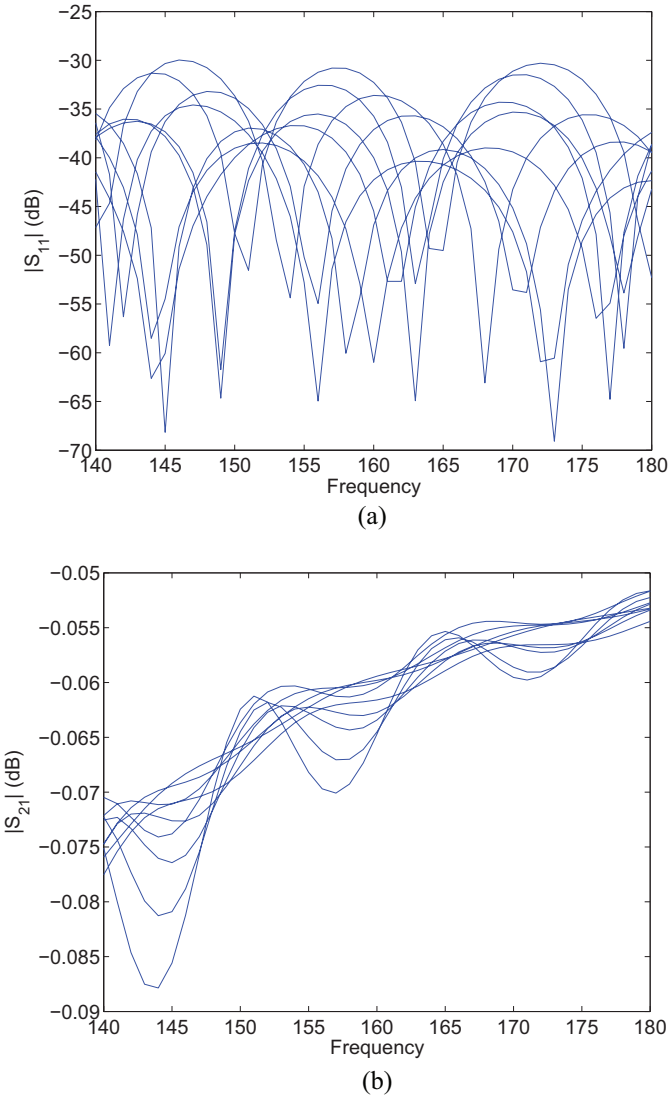


Figure 5.7: Scattering parameters, (a) $|S_{11}|$ and (b) $|S_{21}|$, for the brass discontinuity between WR-05 and the E-plane bend. The results show that for available manufacturing tolerances (maximum 10 μm for both X and Y) and placement tolerances (maximum of 50 μm for both X and Y), the brass waveguide thru-via with rounded corners does not cause $|S_{11}|$ to get much worse than -30 dB nor $|S_{21}|$ to go below -0.09 dB

dissipated in the feed, P_{loss}, and the incident power, P_{inc}, as:

$$P_{rad} = P_{inc}(1 - |S_{11}|^2 - |S_{21}|^2) - P_{loss}. \tag{5.6}$$

Therefore, normalizing everything to P_{inc} and setting $P_{loss} = 0$, a measure of the maximum radiation efficiency can be defined. Since the waveguide arrays are 2-port devices, VSWR does not

completely describe the array as it only takes into account $|S_{11}|$, whose simulation is shown in Figure 5.8(a). Equation 5.6 is a means to gauge the performance of both $|S_{11}|$ and $|S_{21}|$ as well as visualizing how well the array should radiate over frequency. Figure 5.8(d) makes clear that the initial array had a significant drop in simulated radiated power at 170 GHz, which was moved out of band for the final designs.

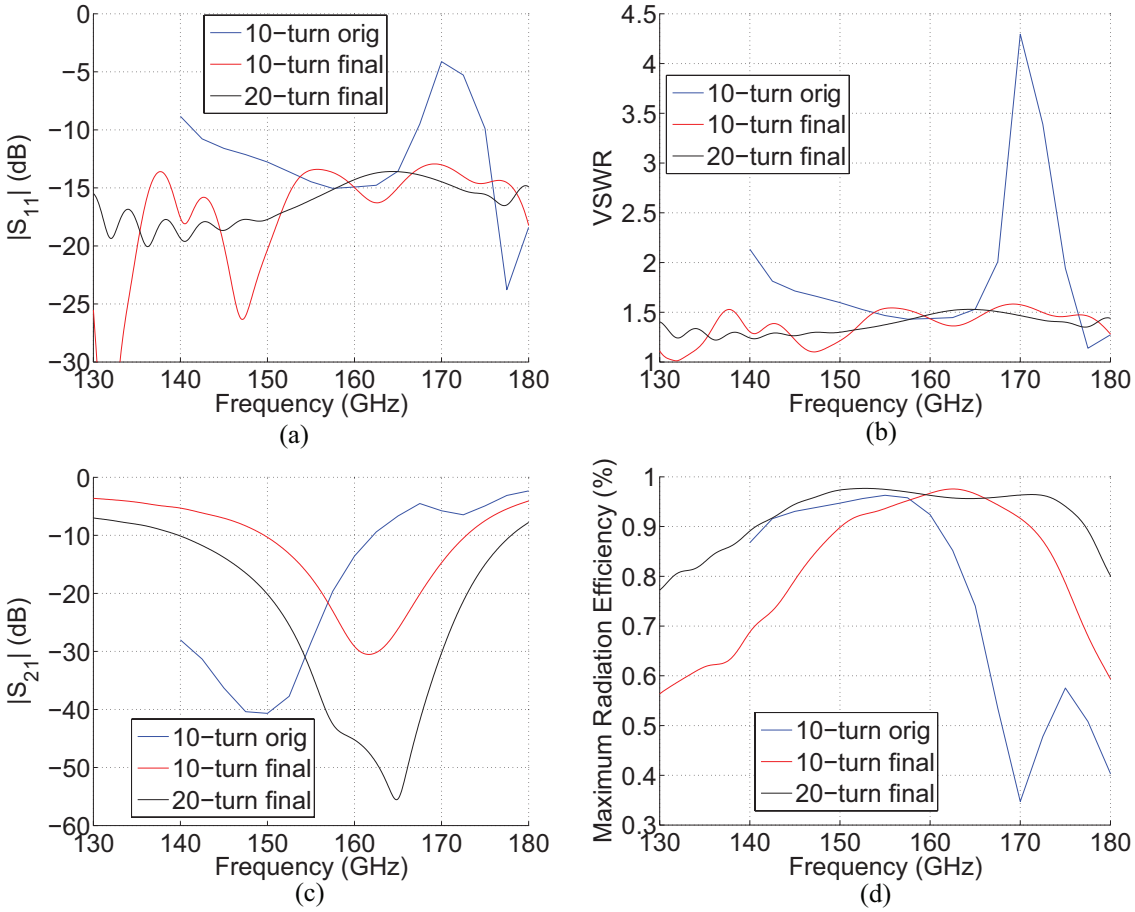


Figure 5.8: Scattering parameters, VSWR, and maximum radiation efficiency for 10-element array from design equations (original), 10-element array after optimizing for $|S_{11}|$ and maximum radiation efficiency (final), and 20-element array (final).

The scanning for the different antenna arrays is shown in Figure 5.9. This figure illustrates that by increasing the maximum radiation efficiency for the 10-element array, the gain can be increased over the majority of the scanning range. Figure 5.9(c) shows that the gain for the 20-

element array is actually more than 3 dB greater than the 10-element array for most frequencies. Though doubling the number of slots normally would result in doubling the gain, the extra increase comes from the increase in radiation efficiency seen when comparing the 10- and 20-element arrays.

5.6 Conclusions and Contributions

The work presented in this chapter resulted in the fabrication of 10- and 20-element, G-band, frequency-scanning, traveling-wave, slotted waveguide arrays in the PolyStrata^{TM} process with interconnects to standard WR-05, to make use of commercially available diode detectors, feed networks, and low-VSWR terminations. This design required E-plane bends shown in Figure 5.10 which lead to waveguide through-vias in a machined brass plate that allows the PolyStrata^{TM} components to mate with standard WR-05 waveguide components.

Though commercially available, low-VSWR terminations were used for the linear arrays, the size of a WR-05 flange is prohibitively large for placing multiple arrays close to one another. Since the size of a flange is 20 mm in diameter and the free-space wavelength at 130 GHz is 2.3 mm, should this design be extended to a 2-dimensional array, each 1D sub-array will not have its own WR-05 termination. A solution to this may be an E-plane horn integrated into the PolyStrata^{TM} process. Such a solution is shown in Figure 5.11. The horn terminations alone, shown in Figure 5.12(a), have a good match ($|S_{11}|$) from 145-180 GHz, but when combined with the array as in Figure 5.12(b) the match is better than -14 dB (VSWR better than 1.50) over the entire range, which satisfies the criteria of a broadband termination for the broadband array, as shown in Figure 5.12(c).

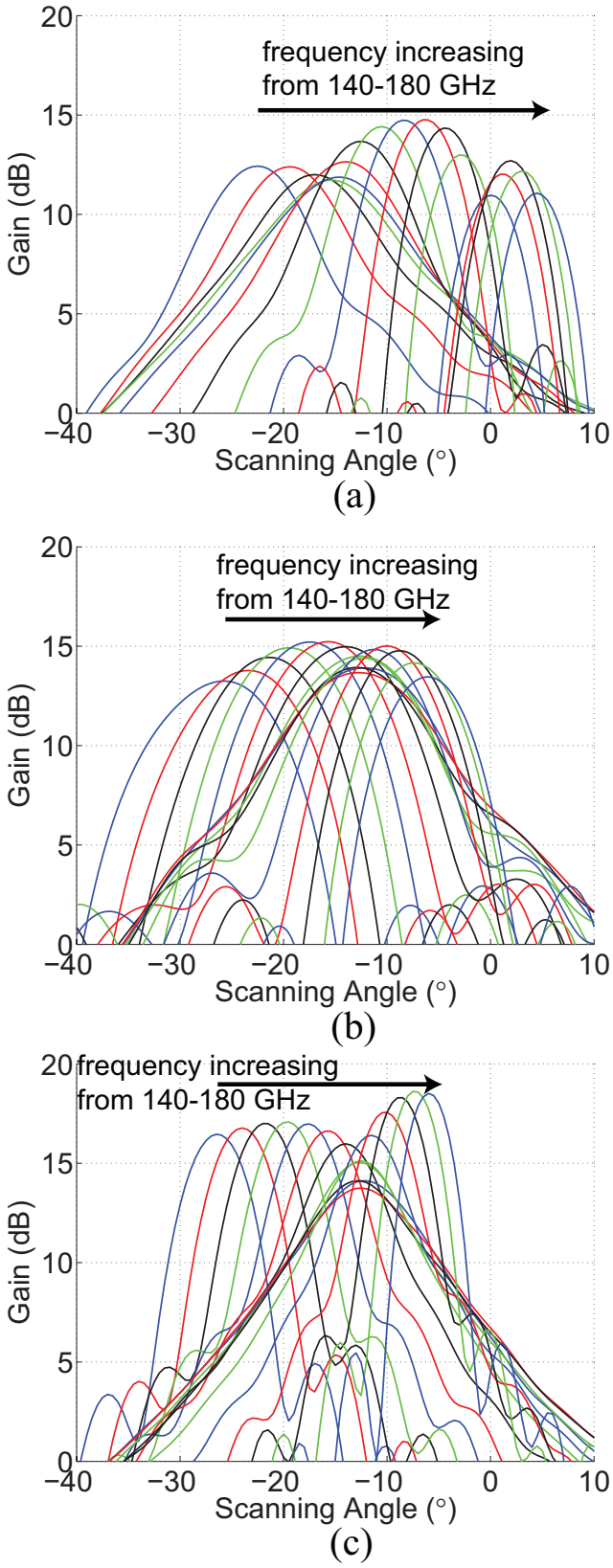


Figure 5.9: Simulated frequency scanning for (a) a 10-element slotted waveguide array after following design equations in literature. After adjusting parameters to increase match, gain, and radiation efficiency, the 10-element array had simulated frequency scanning shown in (b). Two 10-element arrays were then cascaded to produce a 20-element array whose predicted frequency scanning produced narrower lobes and higher gains as expected (c).

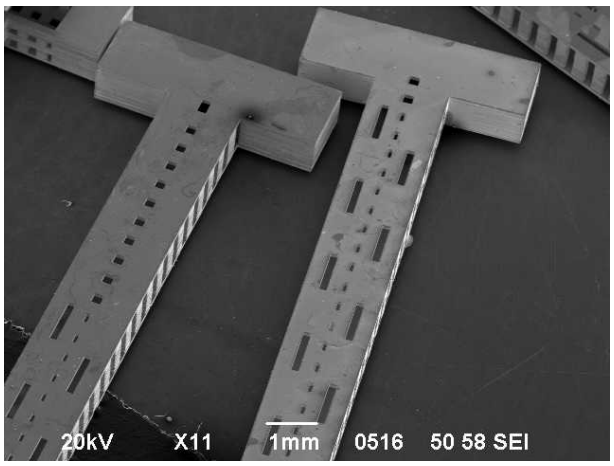


Figure 5.10: SEM photograph of the end of both a 10-element (left) and a 20-element (right) array. The "T" shape allows greater control over the mating process between the PolyStrata^{TM} array and standard WR-05, and within the "T" shape is a custom designed E-plane bend.

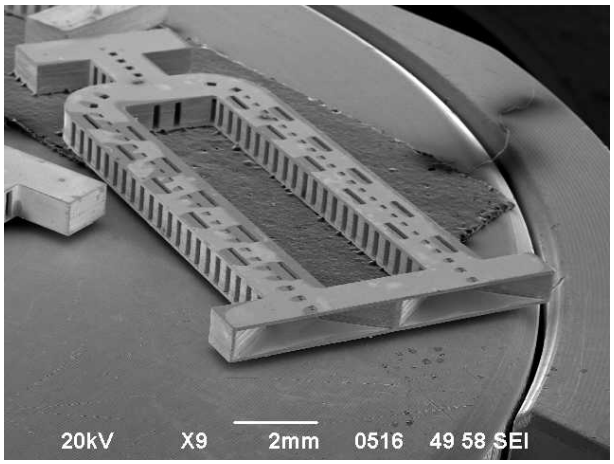


Figure 5.11: SEM photograph of two 10-element arrays corporately fed and terminated in E-plane horns. The horn offers a broadband match for the waveguide over the frequency range of interest. The horn represents a 5:1 reduction in the size of the termination (a WR-05 flange is 20 mm wide, the horn shown is 4 mm wide).

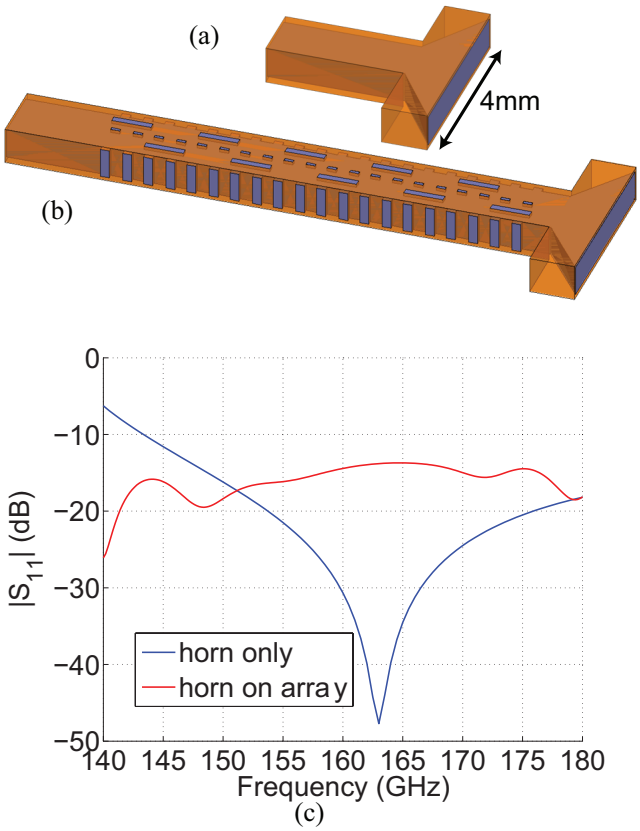


Figure 5.12: An HFSS rendering of (a) an E-plane horn in the PolyStrata^{TM} process as well as (b) how that horn and release holes integrate with a 10-element array. Performance for the horn alone and the complete assembly is shown in (c).

Chapter 6

G-band Frequency Scanned Slotted Waveguide Array Measurements

6.1 Introduction

This chapter addresses the measurements of the arrays discussed in Chapter 5 and a comparison of measured and simulated results. Using a millimeter-wave quasi-optical measurement setup at NIST-Boulder (courtesy of Dr. Erich Grossman), the radiation patterns of the antenna arrays were measured in two bands due to equipment constraints: 150-180 GHz and 130-150 GHz. The configuration of the antenna pattern measurement setup is shown in Figure 6.1 [85]. The millimeter-wave source output is radiated by a scalar feed horn, which couples well into a Gaussian beam. The beam, reflected from a mirror, is collimated by a pair of lenses, reflected from a polarizing mirror, and incident on the antenna array under test. For frequencies in the higher band (150-180 GHz), an Agilent high power swept signal generator with a millimeter-wave module multiplier [86] followed by a VDI diode doubler was used. For frequencies in the lower band, 130-150 GHz, a tunable Gunn-diode oscillator was used, with details of the transmitting portion of the setup shown in Figure 6.2. The array was mounted on a computer-controlled azimuth-elevation stage.

6.1.1 Main Beam Steering

The design goal for the array steering is 15° over a 15% fractional bandwidth. In order to increase the steering, the stronger dispersion close to waveguide cutoff can be utilized. By extending the frequency range of the antenna to below the 140-GHz G-band lower frequency, but above the

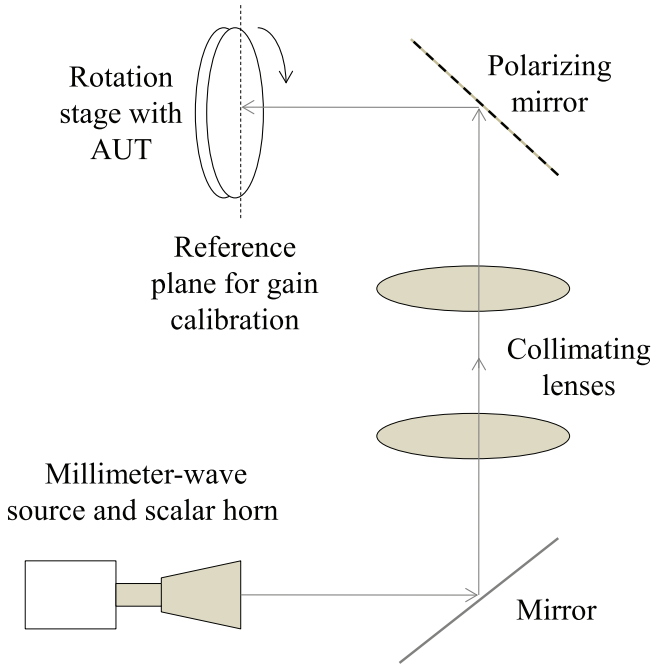


Figure 6.1: Block diagram of the quasi-optical measurement setup for array radiation pattern measurements.

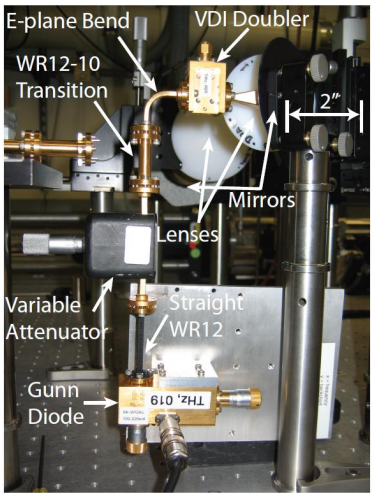


Figure 6.2: Details of the source side of the measurement setup for array measurements from 130-150 GHz.

WR-05 cutoff frequency of 118 GHz, the dispersion was increased, resulting in an increased steering range. Measured normalized radiation patterns from 130 to 180 GHz in Figure 6.3 show that the beam steers from -38° to -5.5°, which is 32.5° over a 32.25% fractional bandwidth, or 0.616°/GHz. In the lower part of this frequency range, however, for 130-150 GHz, the beam steering occurs from -38° to -17.25°, which is 20.75° over a 14.3% bandwidth, or 1.04°/GHz across a 20 GHz range, meeting the design goals. An advantage of the PolyStrata^{TM} process is the flexibility in choosing waveguide feed and slot array dimensions separately to obtain less attenuation in the feed, while increasing the dispersion.

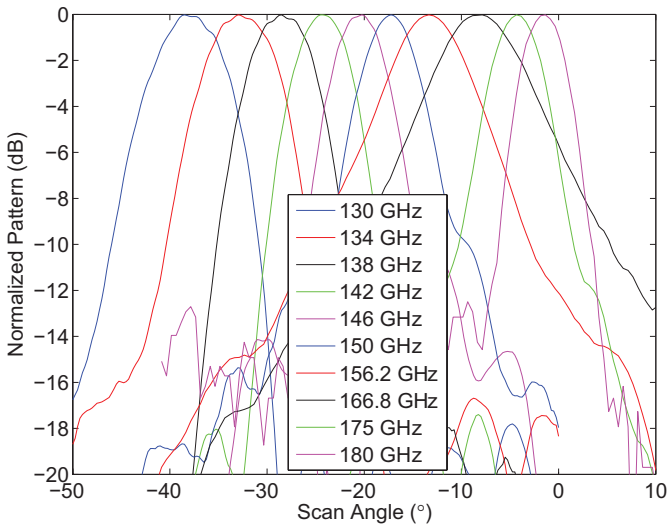


Figure 6.3: Measured normalized radiation patterns of a 20-element slotted waveguide array as the input frequency varies from 130 to 180 GHz. The total scanning is 32.5° over a 32.25% fractional bandwidth.

6.1.2 Gain Calibration

The gain of the array under test was calculated from detected power measurements calibrated with respect to a standard gain horn. A Millitech detector was first used with the horn antenna of

known gain G_H to determine the incident power density, S^H:

$$S^H = \frac{4\pi P_R^H}{G_H \lambda^2} = \frac{4\pi V_d^H}{\alpha D_f G_H \lambda^2} \tag{6.1}$$

where P_R^H is the millimeter-wave power received by the horn, which is related to the voltage detected by the diode detector as $V_d = \alpha D_f \cdot P_R$, and $\alpha < 1$ represents various mismatches that cause additional loss, e.g. waveguide misalignment. The power density will be the same when the array under test is placed at the same plane, so the array gain is given by:

$$G_A = \frac{4\pi V_d^A}{\alpha D_f S_H \lambda^2} = G_H \frac{V_d^A}{V_d^H}, \tag{6.2}$$

where V_d^H is the diode detector voltage measured with the standard gain horn at the reference plane and V_d^A is the diode detector voltage measured with the array at the reference plane. The known horn antenna gain was verified against the data sheets [87] by HFSS simulations, as shown in Figure 6.4. D_f varies over the frequency range, so this calibration was repeated at each frequency.

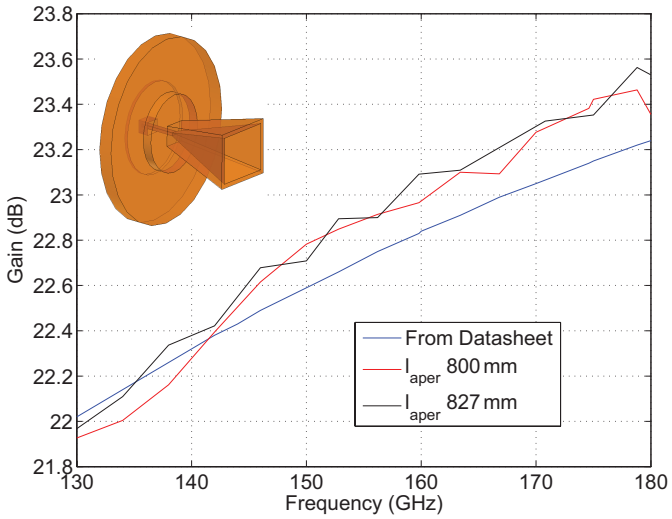


Figure 6.4: Comparison of Custom Microwave HO5R datasheet gain characteristics and HFSS simulated gain characteristics.

6.1.3 Comparison of Measurements and Simulations

The agreement between the measured and the simulated patterns at 130 and 171 GHz is shown in Figure 6.5 for two frequencies that are > 40 GHz apart. As expected, at the higher frequency, the beam is narrower and the sidelobes lower. The 3-dB beamwidths and scanning angles are predicted within few degrees limited by the setup alignment. An example of a two-dimensional measured radiation pattern is given for 142 GHz in Figure 6.6, which as expected has one main lobe, elongated in elevation, that performs scanning in azimuth. The 3-dB beamwidth of this lobe is 6.5°, which matches simulation.

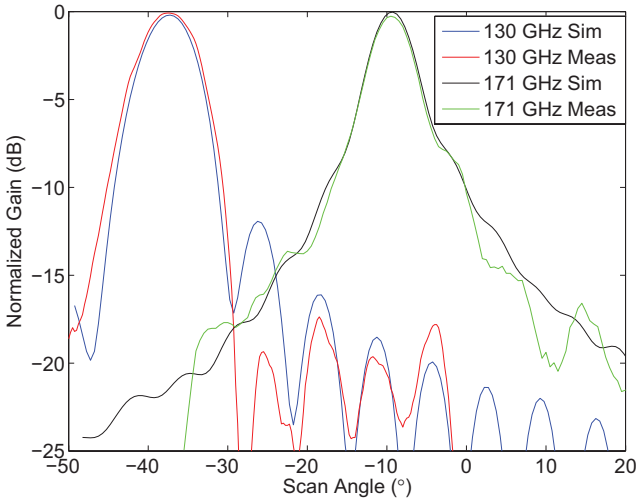


Figure 6.5: Comparison of measured and simulated normalized radiation patterns for a 20-element slot array at 130 and 171 GHz. For these plots, the measured patterns were shifted by a few degrees in order to compare the beam shapes. The angle offset and measurement data spread is given in Figure 6.7.

Due to misalignments and repeatability of the experimental setup at the 1.6 to 2.3-mm free-space wavelengths used for the measurements, there is a quantifiable spread in the measured gain and scanning angle results obtained for multiple measurements over several day periods. These are shown in Figure 6.7(a) and 6.7(b) for the 10-element and 20-element arrays, respectively. The trends of the measured gain and scanning angle frequency dependence follow simulations and the measured scanning angle is within 2° of the simulated angle over most of the range.

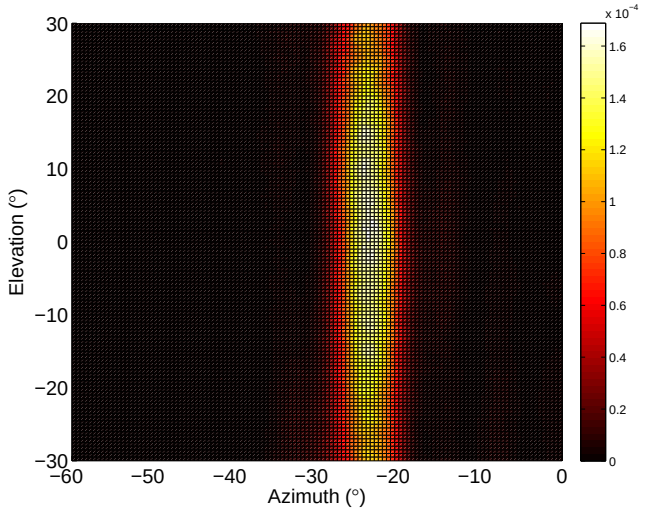


Figure 6.6: Measured two-dimensional radiation pattern of the 20-element array at 142 GHz. The 3-dB beamwidth is 6.5°, as predicted by simulations. The linear scale is in absolute volts as measured by the diode detector.

6.1.4 Scattering Parameter Measurements

The 2-port scattering parameters were measured on a Rohde and Schwarz ZVA-50 network analyzer with ZVA-Z220 G-band millimeter-wave up-converters covering 140 to 220 GHz, which was calibrated using a WR-05 waveguide, 2-port, UOSM (unknown thru / offset short / short / match) calibration. Port 1 is the feed port, while Port 2 is the terminated port of the traveling-wave arrays. Figure 6.8 shows the measured VSWR at Port 1 from 140 to 190 GHz compared to the simulation for the 20-element array showing an excellent input match that extends beyond the 180-GHz upper scanning frequency. The 10-element array exhibited similar characterization with VSWR$<$ 1.75 up to 186 GHz. Since PolyStrata^{TM} waveguide calibration standards were not available for measurement, the standing wave is most likely due to the mount, which includes the waveguide through vias and E-plane bends.

Figure 6.9 shows measured and simulated return loss ($|S_{11}|$) and transmission coefficient ($|S_{21}|$) for the two arrays. From these measurements, an upper limit of the radiation efficiency for each array is be established

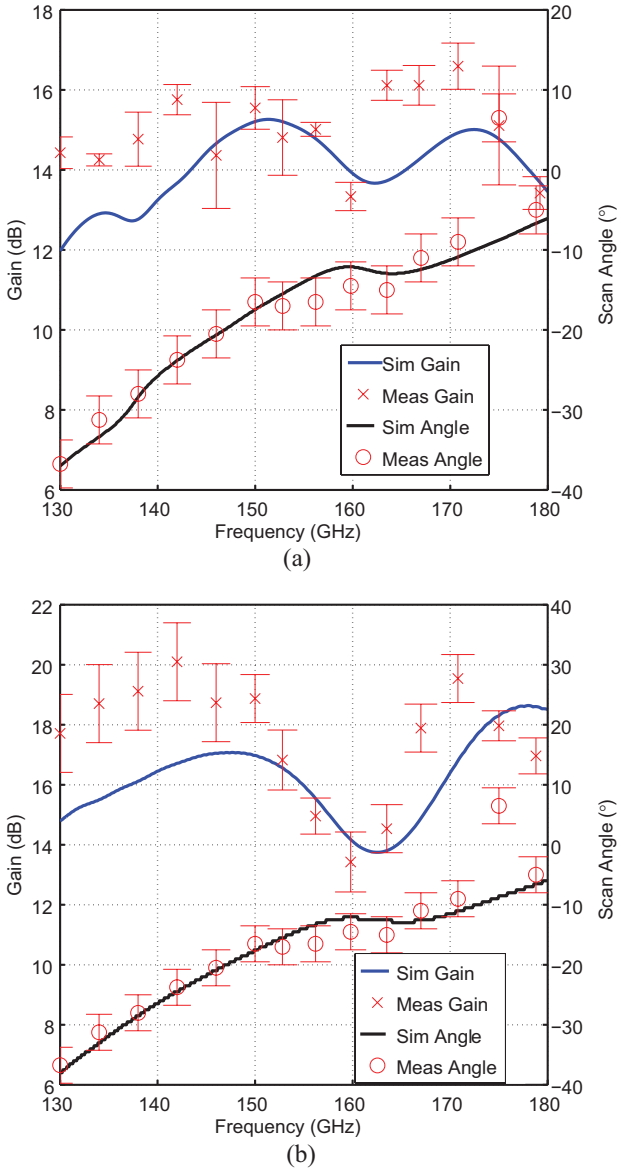


Figure 6.7: Comparison of measured and simulated gain and scanning angle of the (a) 10-element array and (b) 20-element array. The bars indicate spread in multiple measurements due to misalignment and repeatability.

From the low insertion loss and good match illustrated in Figure 6.9, a high radiation efficiency limit is achieved, as shown in Figure 6.10. This figure best illustrates the design tradeoff of absorbing less than 10% of P_{inc} in the load for increased gain at a cost of reduced gain flatness and nonmonotonic beam steering, as discussed in Chapter 5.2. Figure 6.9 clearly shows that $|S_{21}|$

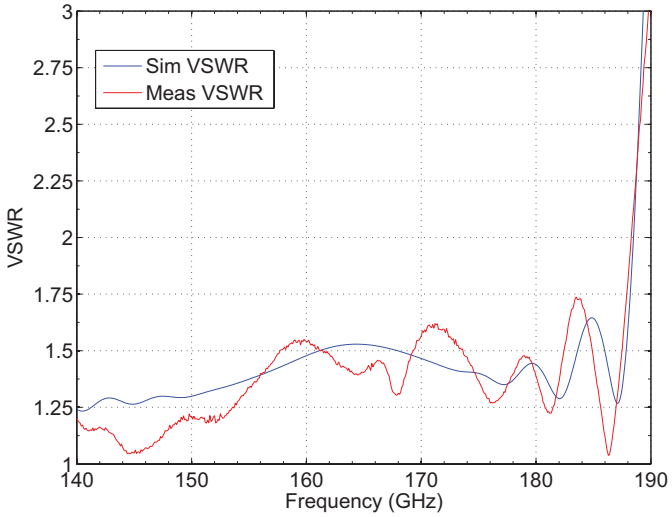


Figure 6.8: Measured and simulated VSWR at Port 1 of the 20-element array using a Rohde and Schwarz ZVA-50 vector network analyzer and an UOSM calibration. The 10-element array also has VSWR < 1.75 up to 186 GHz.

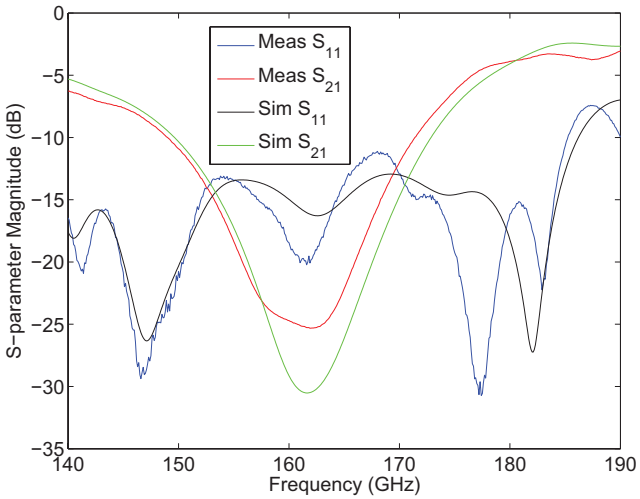
for the 20-element array below 180 GHz is 5-300 dB lower than $|S_{21}|$ for the 10-element array. The result is that below 180 GHz, the 20-element array maximum radiation efficiency is above 85% while the 10-element maximum efficiency drops to below 60%.

While the upper limit of the radiation efficiency can be calculated, the actual radiation efficiency depends on the loss in the feed, which though difficult to separately measure can be estimated based on dominant mode loss in rectangular waveguide. The loss for the fundamental mode is given by, e.g., Marcuvitz [88] as

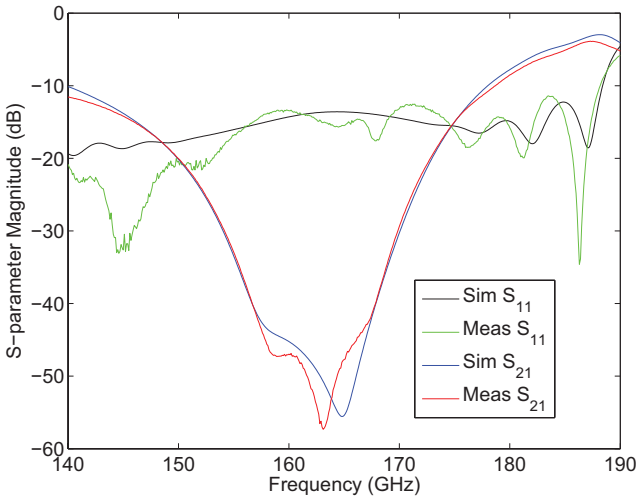
$$\alpha_c^{TE_{10}} = \frac{R_s}{b\eta\sqrt{1-\left(\frac{f_c}{f}\right)^2}}\left[1+\frac{2b}{a}\left(\frac{f_c}{f}\right)^2\right] \tag{6.3}$$

where R_s is the surface resistance, $\eta = 377\,\Omega$, and f_c is the cutoff frequency. Therefore at 150 GHz, the attenuation is 0.091 dB/cm, which for both the 10-element and 20 element arrays results in about 0.2 dB of loss in the waveguide feeds.

Since fabrication introduces both lateral and transverse surface roughness components, a



(a)



(b)

Figure 6.9: Measured and simulated $|S_{11}|$ and $|S_{21}|$ of the (a) 10-element and (b) 20-element traveling-wave arrays.

modified formula for the loss is given in references [4, 89] as

$$\alpha_c' = \alpha_c \left[1 + \frac{2}{\pi} \arctan\left(1.4 \left(\frac{\Delta}{\delta_s} \right)^2 \right) \right], \tag{6.4}$$

where Δ is the RMS surface roughness of the conductor and δ_s is the skin depth of the conductor. This formula is derived from the Wheeler incremental inductance rule as described in [90] and does not specify the type of roughness, so it is only used as a guideline here.

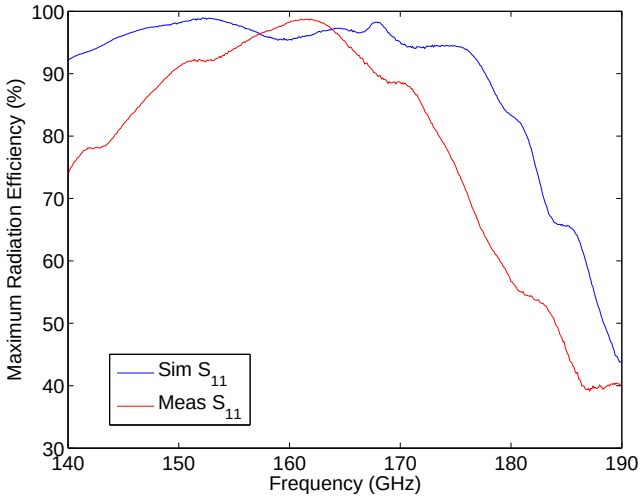


Figure 6.10: Radiation efficiency limit for the 10- and 20-element arrays based on return loss and insertion loss. The maximum percentage of $\frac{P_{rad}}{P_{inc}}$ is calculated based on Equation 5.6 assuming $P_{loss} = 0$.

The PolyStrata^{TM} process results in very smooth horizontal surface since CMP (chemical-mechanical planarization) is used between layer depositions. The vertical surface roughness is larger, and on the order of 0.13 μm as measured by optical interferometry.

Table 6.1: Microfabricated waveguide loss at G-band.

Loss type and Roughness RMS			Frequency 150 GHz
Attenuation [dB/cm]	$\Delta = 0$		0.0902
	$\Delta = 0.13\,\mu$m	Vert walls	0.110
		All walls	0.1443

A summary of predicted loss in the micro-fabricated waveguide is shown in Table 6.1 . These losses are simulated with HFSS when the RMS surface roughness was applied to (1) vertical walls and (2) all of the walls of the waveguide [55]. These simulation results show that waveguide has low loss at G-band. However, the RMS surface roughness has a large effect on the loss of the waveguide at these frequencies. In the worst case, the 0.2 dB waveguide feed loss increases to 0.47 dB, so for 1 W incident power to the 10-element array, Equation 5.6 results in 0.81 W power radiated, down from 0.87 W power radiated without roughness losses. For the 20-element array, the increased loss

reduces radiated power from 0.94 W to 0.88 W.

6.2 Conclusions and Contributions

In summary, this work presents measured and simulated results for one-dimensional slotted waveguide frequency scanning arrays. A 10-element and a 20-element array are characterized from 130 to 180 GHz and exhibit a VSWR < 1.75 and beam scanning of about 1°/GHz with gains of 15.5 dB and 18.9 dB at the band center, respectively. The arrays are fabricated using the PolyStrata^{TM} sequential copper deposition process and are subsequently gold plated and bonded to a fixture that allows mating to standard WR-05 waveguide flanges. The demonstrated approach scales to higher frequencies and to two-dimensional array architectures. In addition, it is possible to use a waveguide feed with higher dispersion to increase scanning angle for a given frequency tuning bandwidth. The results of this work are reported in [91].

Chapter 7

Conclusions

7.1 Thesis Summary

In summary, this thesis presents contributions to broadband microfabricated microwave circuits in the 4-18 GHz and 130-180 GHz bands for various applications, ranging from solid-state 20 W broadband transmitters to low-mass (0.063 mg) phased arrays for planetary landing radar. In specific, the following topics have been described in detail.

(1) Assembly structures for integration of microfabricated coaxial lines and components with standard surface-mount lumped elements. These structures, referred to as "passive sockets" were designed using full-wave electromagnetic simulations and were tested with 0402 and 0303 packaged resistors and capacitors. In the frequency range of interest (4-18 GHz), the sockets exhibit low return loss due to the ability to compensate for the parasitics. Sockets were also designed for active devices and demonstrated on the example of a GaN MMIC small-signal amplifier from 1 to 10 GHz.

(2) In addition to hybrid integration of surface mount commercial inductors, a 3-D monolithic inductor was presented and incorporated into a bias-tee network for GaN power amplifier biasing. The inductor geometry can be optimized due to the 3-D fabrication nature, and the parasitics due to the substrate in printed inductors eliminated since the PolyStrata^{TM} inductor is a coil in air.

(3) G-band arrays of slot antennas were designed and characterized from 130 to 180 GHz for

10- and 20-element traveling- wave arrays with beam steering accomplished by frequency tuning. Interconnects to standard size waveguide were designed and fabricated, along with fixtures for packaging the G-band arrays with standard waveguide terminations and connections to equipment. A quasi-optical setup at NIST was used to measure the radiation patterns as a function of input frequency, and 1° per GHz scanning was observed, consistent with simulations. The arrays also exhibit a good return loss ($<$ 10dB) in the frequency band of interest.

Several possibilities for improvement and further expansions are recommended below.

7.2 Recommendations for Future Work

7.2.1 Hybrid integration

The first recommendation for future work provides guidance on how PolyStrata^{TM} lines and devices can be hybridly integrated with greater performance. This work would be useful because interconnects can have significant parasitics at microwave frequencies, and as such, the inductance presented by bond wires used to connect the MMIC to the PolyStrata^{TM} bias tees can be a huge problem. For example, a 0.5 nH series bondwire inductance represents a $\jmath 30$ series impedance, which in a 50Ω line would result in a mismatch of 10 dB. While effort was put forth in some of the bias tee designs to mitigate the effects of bond wire inductance, a much more elegant solution exists.

To better explain the problem, Figure 7.1 shows two 50 Ω coax lines connected via bondwire. The graph in Figure 7.2 makes it clear that as the bondwire length increases, the increase in parasitic inductance and capacitance shifts the resonant frequency down, reducing the -12.5 dB match from approximately a 20 GHz frequency limit to less than 4 GHz.

The better solution is a direct transition to microstrip, as shown in Figure 7.3. This is available in many processes, including alumina and other common microwave substrates. In this approach, a transition fabricated on another substrate is designed to interface with a low-VSWR

to a micro-coaxial line through a via. Figure 7.4 shows an example of simulated S-parameters for such a transition.

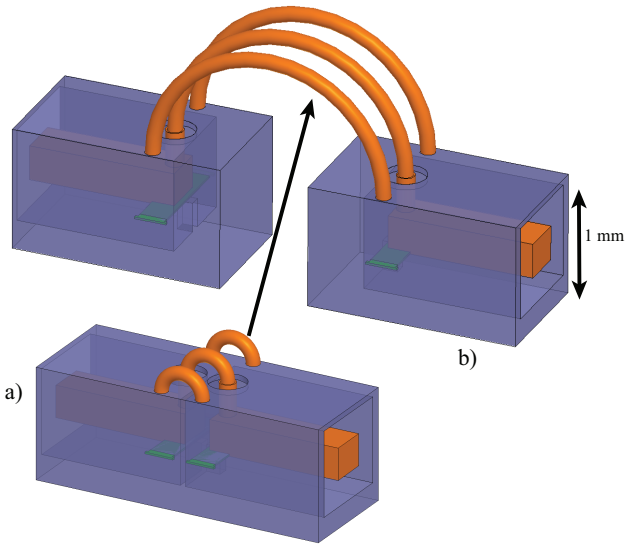


Figure 7.1: Two cases of how bondwire can be used to connect components. As the bondwire length is increased from (a) to (b), the associated parasitic inductance will increase as well.

The second recommendation for future work is the expansion of the work presented in this thesis to an 11-strata process, as all of the hybrid integration was accomplished in a 5-strata process. This gives a larger list of parameters that can be varied, as well as enhancing the power handling capabilities of the structures [5] to make the hybrid integration sockets more versatile.

The third recommendation is integrated heat sinking. Since one advantage of the microcoax lines is a high power handling capability (100 W CW at S-band [7]), and because this thesis has shown how active devices can be hybridly integrated with this technology, heat sinking is a next logical step in this evolution. Active devices can be flip-chip bonded into this process, which allows the backplane of the chip to be available for dissipating heat; however, when devices are hybridly integrated as described above (or wire-bonded), the material characteristics of this technology offer promising ideas.

Many heat sinks are made of brass, which is an alloy of copper, the primary component of

the PolyStrata^{TM} process. An equation used in heat transfer is:

$$\Delta T = \frac{\frac{\Delta Q}{\Delta t} x}{kA} \tag{7.1}$$

where ΔT is the temperature differential (in K), $\frac{\Delta Q}{\Delta t}$ is the rate of heat flow through the material (in W), x is the thickness of the material (in m), k is the thermal conductivity of the material (in $\frac{W}{mK}$), and A is the cross section of the material. Consider a square, 2 cm by 2 cm heat source that is connected to a 500 μm heat sink consisting of diamond ($k = 900$, $x = 487.5\mu$m) via a thermal epoxy connecting medium ($k = 0.2$, $x = 12.5\mu$m per [92]). If 100 W of power is going through this volume, then Equation 7.1 yields that the temperature across the diamond will be 0.542 K and the temperature across the thermal epoxy will be 62.5 K for a net temperature differential of about 63K. If the heat source were gold-gold thermosonic bonded ($k = 318$, $x = 1\mu$m) to 499 μm of copper ($k = 401$) used as part of the PolyStrata^{TM} structure, the corresponding temperature differentials would be 1.244 K across the copper and 0.003 K across the gold for a net temperature differential of about 1 K.

Though this analysis is extremely basic in nature and the full capabilities of thermosonic bonding is not completely known to the author, this example shows that this is an area of interest to further explore the capabilities of the PolyStrata^{TM} process.

7.2.2 Monolithic inductors

Three main areas of research remain with regards to monolithic inductors in the PolyStrata^{TM} process. First, since all the measured inductors presented in this thesis were accomplished in 5 strata, an 11-strata process should be incorporated. Moving to 11 strata allows some of the more exotic geometries discussed in Chapter 3. Second, the dual-wound inductor shown in Figure and discussed briefly in Section 3.3 should be explored in greater detail, including deriving a more detailed lumped element equivalent model to better determine how well it compares to regular inductors. Finally, a library of inductors for the different types of inductors commonly available (solenoid, dual wound, spiral, conical, etc) with various turns and winding sizes should be made or

each of these different types should at least be researched so that each has its own detailed lumped element model so that designers can select which geometries and how many turns they would like for a given design.

7.2.3 Power combining with PolyStrata^{TM} combiners

The low loss of the microcoax, along with its high power handing capability and heat sinking options satisfy two of the greatest needs of power combiners. The 3-D abilities of the technology, accompanied with the large range of characteristic impedances available allow for power combiners of almost any type to be explored. Along with the sockets that this thesis has demonstrated, Wilkinson dividers [18] and transformers [20] have already been realized in this technology. Overall, the PolyStrata^{TM} process has several advantages in the discipline of power combining, especially for higher frequency applications due to its low loss and low parasitics due to the tight tolerance and geometric control available due to the photolithographic nature of the process.

7.2.4 Slot antenna array development

Antennas at G-band represent a large size reduction for an array. Since this thesis has demonstrated linear arrays at this frequency range, a logical progression would be to realize a 2-D array that supplies 2-D steering. Since the array at G-band is very small and has such a low mass, additional feed network design could be used to accomplish 2-D frequency steering. Alternative methods include using more amplifiers which would increase the power delivered to the array possibly increasing the effective range of a radar system.

Slot arrays can also be fed by micro-coaxial lines, as shown in Figure 7.6 [93]. Due to loss considerations [55] these arrays are not suitable for G-band operation, but are attractive options for lower frequency ranges where PolyStrata^{TM} arrays cannot be manufactured in waveguide due to height constraints, for example WR-10 waveguide is associated with W-band and has dimensions 2.54 mm by 1.27 mm exceeding the maximum height of a PolyStrata^{TM} waveguide (currently 0.9 mm). Such an array could be measured in the same way as described in Chapter 6 and provide

the tight tolerances necessary for such high frequency antennas [66].

7.3 Thesis Contributions

This thesis has presented a number of contributions to microwave front ends designed and fabricated in the PolyStrata^{TM} technology. In Chapter 2, methods for hybrid assembly of standard surface-mount components into the PolyStrata^{TM} microcoaxial environment were designed and tested. In a 50 Ω coaxial environment, the added insertion loss is between 0.05-0.12dB in the frequency range 4-18 GHz, and although any parasitic effects are magnified in a lower impedance environment, return loss and insertion loss can still be kept at acceptable levels. This chapter is the basis for the results reported in [8, 5, 37].

Chapter 3 discussed the design of different types of inductors and demonstrated the properties of coil inductors made in a 3-D air process. Since the inductors were not on a substrate nor had a polymer structural support in the center, they were allowed low parasitic capacitance and a variety of inductor geometries. The inductors handle record current levels of 5 A for their inductance, quality factor, and size. Furthermore, these inductors add an extra aspect to the PolyStrata^{TM} design toolbox, enabling lumped matching elements and bias tees, which were discussed in Chapter 4, which detailed the heterogeneous integration of the PolyStrata^{TM} process with a proprietary amplifier in the GaN process as well as commercially available surface mount passive devices. The bias tees were manufactured in 12.5 Ω and 50 Ω microcoaxial impedance environments, and show the viability of moving passive components off of MMICs allowing more efficient use of chip area potentially reducing cost. The results Chapter 4 are reported in [5, 37].

Chapter 5 resulted in the fabrication of 10- and 20-element, G-band, frequency-scanning, traveling-wave, slotted waveguide arrays in the PolyStrata^{TM} process with interconnects to standard WR-05, to make use of commercially available diode detectors, feed networks, and low-VSWR terminations. This design required E-plane bends which lead to waveguide through-vias in a machined brass plate that allows the PolyStrata^{TM} components to mate with standard WR-05 waveguide components. These bends also allow arrays to be considered that have radiating structures

above and feed structures on a lower layer. Because of the size of WR-05 flanges can be prohibitive in terminating these arrays, an E-plane horn was also designed with a VSWR better than 1.50 from 140-220 GHz ($|S_{11}|$ < -14 dB), which satisfies the criteria of a broadband termination for the broadband array.

Chapter 6 presented the measured and simulated results for the arrays of Chapter 5. These arrays are characterized from 130 to 180 GHz and exhibit a VSWR < 1.75 and beam scanning of about 1°/GHz with gains of 15.5 dB and 18.9 dB at the band center, respectively. The arrays are fabricated using the PolyStrata^{TM} sequential copper deposition process and are subsequently gold plated and bonded to a fixture that allows mating to standard WR-05 waveguide flanges. The demonstrated approach scales to higher frequencies and to two-dimensional array architectures. Finally, the technology used to make these arrays allows a waveguide feed with higher dispersion to increase scanning angle for a given frequency tuning bandwidth. The results of this work are reported in [91].

The results demonstrated in this thesis pave the way to new types of high-quality, hybridly integrated microwave and millimeter-wave components.

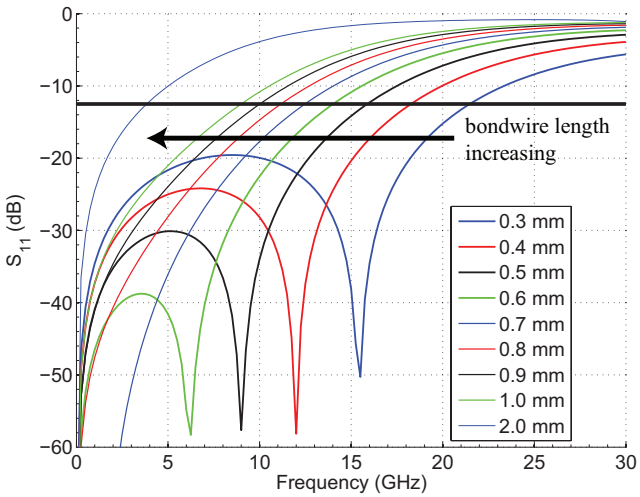


Figure 7.2: As the length of a bondwire interconnect increases, its parasitic inductance increases as well. When connecting two 12.5Ω coax lines, this inductance causes significant return loss degradation. For a 12.5 dB match, doubling the length of the bondwire from 0.5 mm to 1.0 mm to 2.0 mm causes the frequency limit to decrease from 15.8 GHz to 9 GHz to 3.8 GHz.

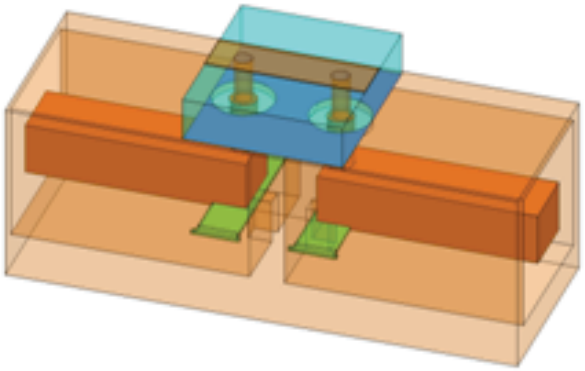


Figure 7.3: For technologies whose processing allow vias (such as alumina) a transition from micro-coax can be incorporated that does not have the parasitic inductance that bondwire presents. The substrate used is 10 mil thick Alumina ($\epsilon_r = 9.9$ and $\tan\delta = 0.006$) and the microstrip connection is 50Ω.

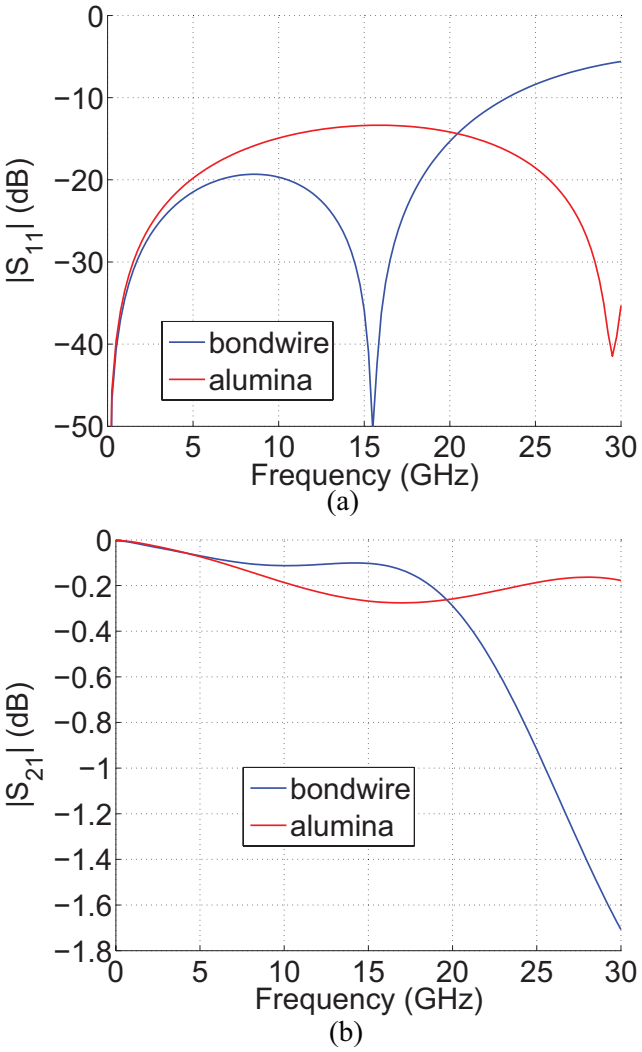


Figure 7.4: A comparison of$|S_{11}|$ (a) and$|S_{11}|$ (b) for the shortest bondwire case of Figures 7.1 and 7.2 compared to the transition of Figure 7.3 showing the broader -10 dB bandwidth of the alumina transition.

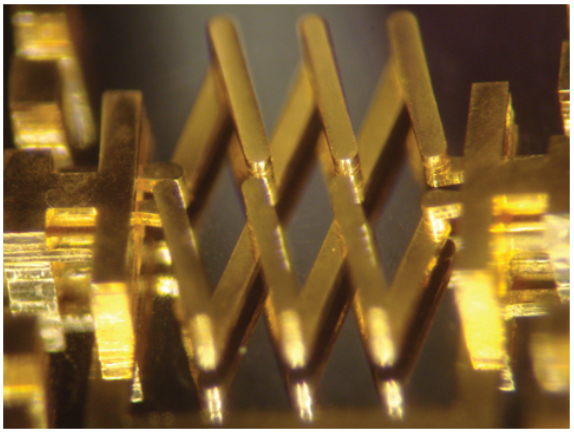
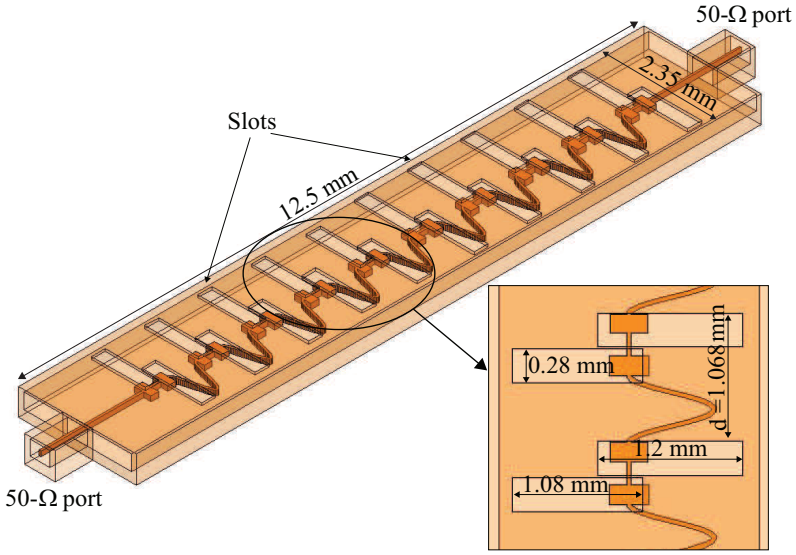
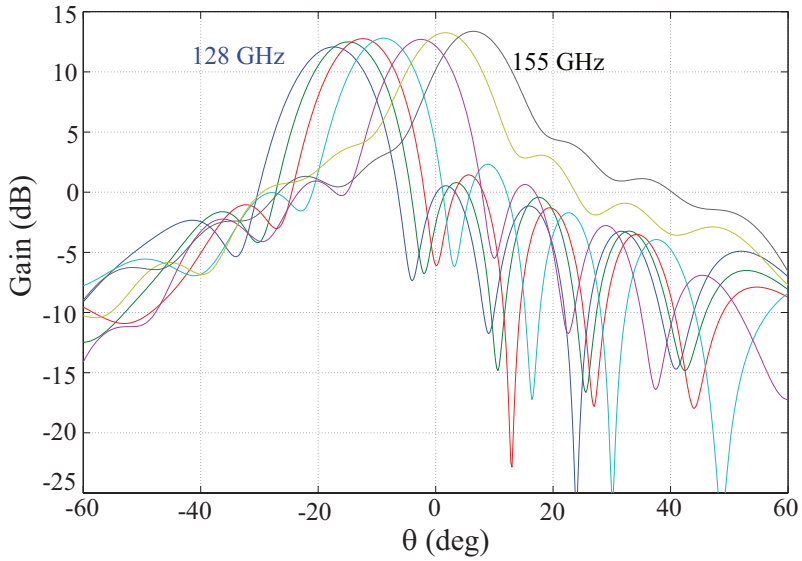


Figure 7.5: Illustration of a potential new type of inductor. This inductor presents inductance not only in series with the signal line, but also in series with the ground line, theoretically doubling the value.



(a)



(b)

Figure 7.6: (a) Double slotted microcoaxial array implementation at W-band. Simulation of this array shows scanning of about 1 °/GHz (b) with a gain of over 10 dB.

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Appendix A

GaAs Distributed Amplifier

A.1 Background

Distributed amplifiers (also known as Traveling Wave Amplifiers (TWA) or Traveling Wave Tube Amplifiers (TWTA or TWT) if implemented in vacuum tubes) are a very novel approach to amplifiers that date back to at least 1947 [94, 95, 96]. They are prized for their broadband characteristics [97] or extended resonance [98, 99] and moderate to high gain.

The way that a distributed amplifier achieves gain over such a large bandwidth is by replacing the shunt conductance, g, in the transmission line lumped model with a transistor supplying a negative resistance (gain) instead. For the purpose of this paper, a cell is considered one section of lumped transmission line that includes one transistor. Multiple cells can be cascaded together, biased off a single gate supply and drain supply, with a single input and a single output. This configuration is referred to in this paper as a stage. Any variety of these cells and stages can be used in combination, each with its own advantages and disadvantages. The theory of operations for a distributed amplifier is covered in Section A.3, TWA Design, while the idea of cell and stage combinations is discussed in Section A.4, Cell Impact On Design.

For this amplifier, the design goal was to cover X-band through Ku-band amplifier (4-18 GHz) with a gain of more than 10 dB over the entire band. Once these criteria were satisfied, noise, gain flatness, power handling, and compression were examined, though not specifically accounted for during the design process. The specific performance of this amplifier is discussed in Section A.6.

A.2 Biasing

Biasing is critical to any amplifier. Because this amplifier is ultra-broadband (127% fractional bandwidth), biasing presents a challenge. Since this amplifier is to be realized in a GaAs MMIC process, lumped components are well characterized and parasitics can be well controlled, so lumped element bias tees were chosen. Target performance for S_{11}, S_{22}, S_{31}, and S_{32} was -20 dB while S_{21} was to be made as close to 0 dB as possible. These goals were met quickly, but due to layout constraints the target performance had to be relaxed slightly. The input bias tee, whose results are shown in Figure A.1, met the target performance quite well. The output bias tee shown in Figure A.2, however, just missed the target. The output bias tee has S_{11} and S_{22} going above -20 dB around 17 GHz. Nonetheless, this is a very low level and shouldn't affect the amplifier much. Figure A.3 shows that both bias tees have good isolation in both directions, especially the input bias tee whose isolation in both directions is below 20 dB from 2-20 GHz. Thus the bias tees were shown to be sufficient over the entire bandwidth.

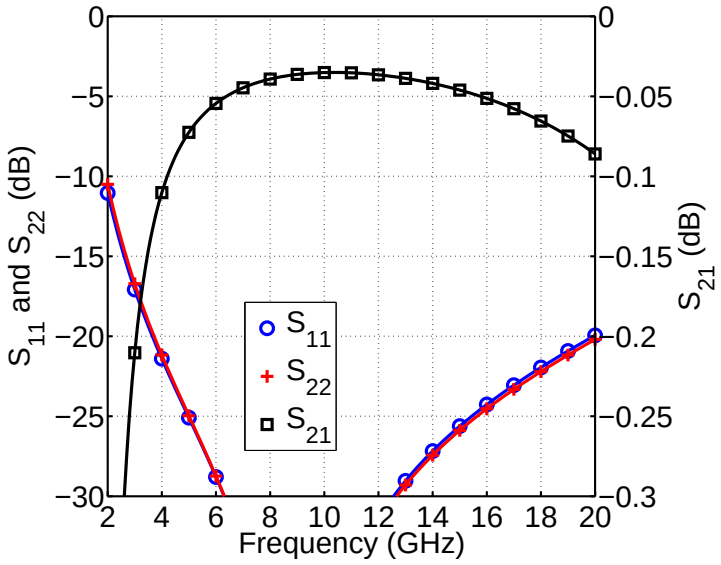

Figure A.1: $|S_{11}|$, $|S_{22}|$, and $|S_{21}|$ for input bias tee (found on cell 1) illustrating return losses ($|S_{11}|$ and $|S_{22}|$) less than -20 dB over band 4-18 GHz and $|S_{21}|$ very close to 0 dB

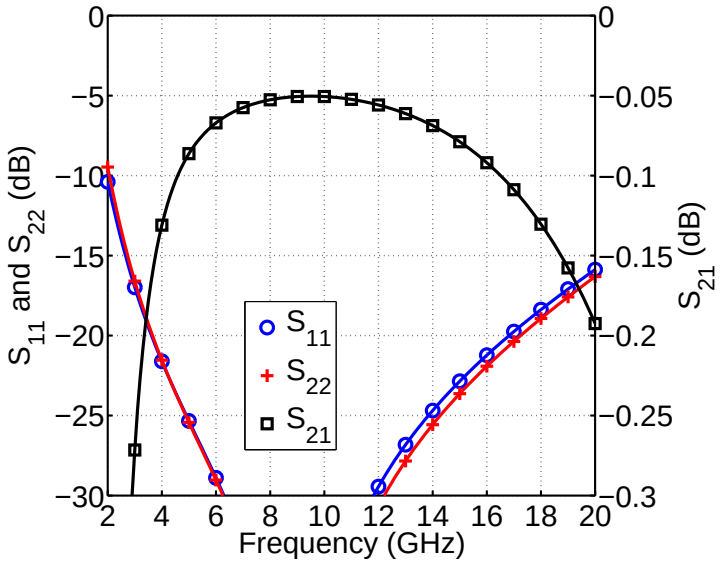

Figure A.2: $|S_{11}|$, $|S_{22}|$, and $|S_{21}|$ for output bias tee (found on cell 4) illustrating return losses (S_{11} and S_{22}) less than -20 dB over marjority of band 4-$\sim$17 GHz and S_{21} very close to 0 dB

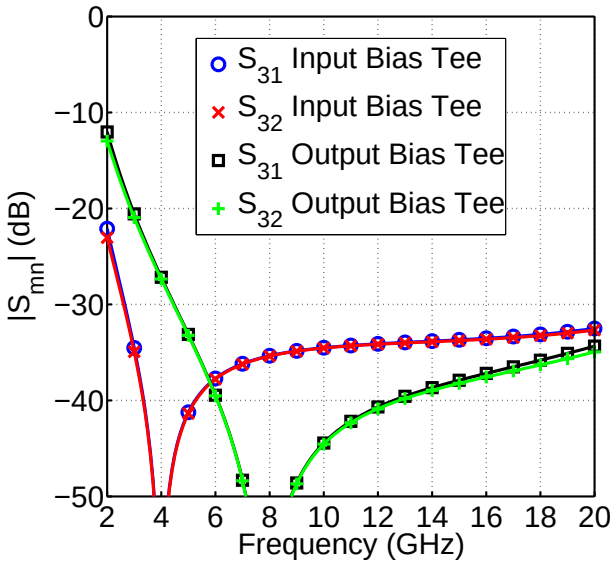

Figure A.3: DC isolation ($|S_{31}|$ and $|S_{32}|$) for input (cell 1) and output (cell 4) bias tees showing that very little RF leakage into or out of the system should occur

A.3 TWA Design

The novelty of a traveling wave amplifier is that if made small enough, the transistor is a lumped element in the transmission line model, which is inherently broadband. If this transistor is

placed in shunt where the shunt conductance normally is only as a negative resistance, now each incremental section of transmission line will cause the signal to grow rather than attenuate. Thus the bandwidth is limited only by the transmission line. This will mean that clever engineering is required such that the transistor can be integrated seamlessly into a lumped transmission line model.

In this design, two transmission lines are considered: one for the input signal to the transistors and one for the transistors' output. To simplify design, the transmission lines were both chosen to be 50Ω. This means that no matching is required to get input signal in or output signal out and both transmission lines, since they have the same lumped component values, will have the same velocity of propagation ensuring that the devices act in phase. Thus the values need to be found for the different lumped elements of the transmission line model. The primary design limitation is the capacitance. Recalling the low-order FET model, one can easily envision that the input signal line will have C_{gs} of the transistor as its capacitance while the output signal line will use C_{ds} for its capacitance. However, since these two values are not equal, an additional capacitor (C_{ext}) must be added in parallel with C_{ds} such that Equation A.1 is satisfied.

$$C_{gs} = C_{ds} + C_{ext} \tag{A.1}$$

To calculate the inductance required, it is well known that the characteristic impedance of the line is found using the Equation A.2. However, since the capacitance can vary depending on the transistor geometry, the problem is still not constrained. The final piece is that the transmission line model has a shape similar to a low pass filter, whose equation is given by Equation A.3. Choosing an upper frequency for the corner or 3 dB frequency of this filter gives a maximum capacitance value and the inductor value follows. As a note, a variety of means exist to design this inductor, one of the more common being Stanford Spiralcalc [100].

$$Z_0 = \sqrt{\frac{L}{C}} \tag{A.2}$$

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{A.3}$$

A.4 Cell Impact On Design

As mentioned above, a cell is a single lumped element section of transmission line which contains a single transistor. A stage is all of the cells which are connected to the same DC voltage. As Pozar [101] points out, the gain of a distributed amplifier which increases based on the number of cells has the fundamental principle of going to zero as the number of cells goes to infinity because of the exponential decay of the signal along the input line causing later amplifiers to have no signal to amplify. For this design, a stage of 1-8 cells was first analyzed. The performance of a stage of 2 cells is shown in Figure A.4. One can see that the stage has gain, but it is only slightly greater than unity. Figure A.5 shows how the gain varies with the number of cells. Given these gain patterns and the unspecified but generally desired characteristic of gain flatness, a 4 cell stage amplifier seems best. However, there exists the potential that a single stage of 8 cells performs better than 2 stages of 4 cells. In fact, the 2 stages of 4 cells performs better as shown in Figure A.6. Taking this discovery a step further, the question of performance difference between a single stage of 4 cells or 2 stages of 2 cells. This question is answered by Figure A.7, which shows that a single stage of 4 cells performs better than a cascade of 2 stages of 2 cells.

Based on Figures A.5-A.7, a stage of 4 cells was chosen. The assembled stage has S-parameters shown in Figure A.8. This stage has gain from 4.59 - 7.25 dB (gain flatness of 2.66 dB) as seen from S_{21} and a standing wave whose frequency (~ 6.2 GHz corresponds to the length of the stage, indicating that there is a mismatch at the ports. However, since the design is for 50Ω, it is advantageous to leave the design as is so that multiple stages can be cascaded.

A.5 Complete Design

The die area afforded for this project was 2.5mm by 2.5mm. This meant that a 4-cell stage could be used, but had be optimized for space to allow for fitting width. This also meant that up

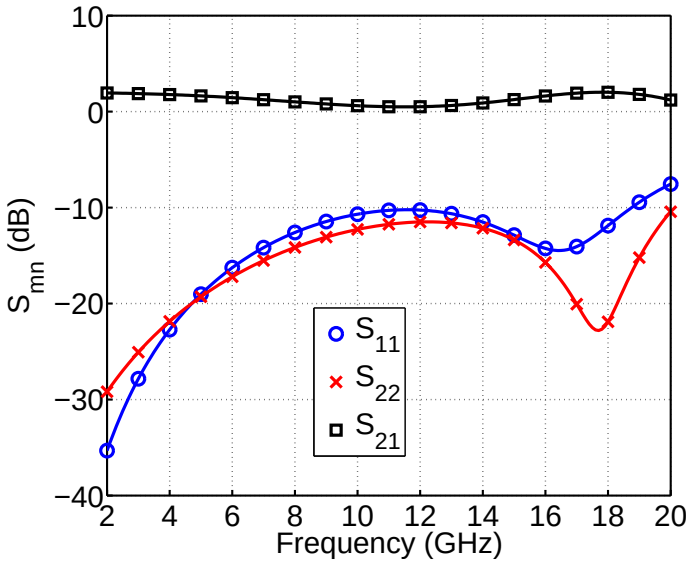

Figure A.4: $|S_{11}|$, $|S_{22}|$, and $|S_{21}|$ for a distributed amplifier consisting of 2 cells showing notably that this amplifier has gain, but not much

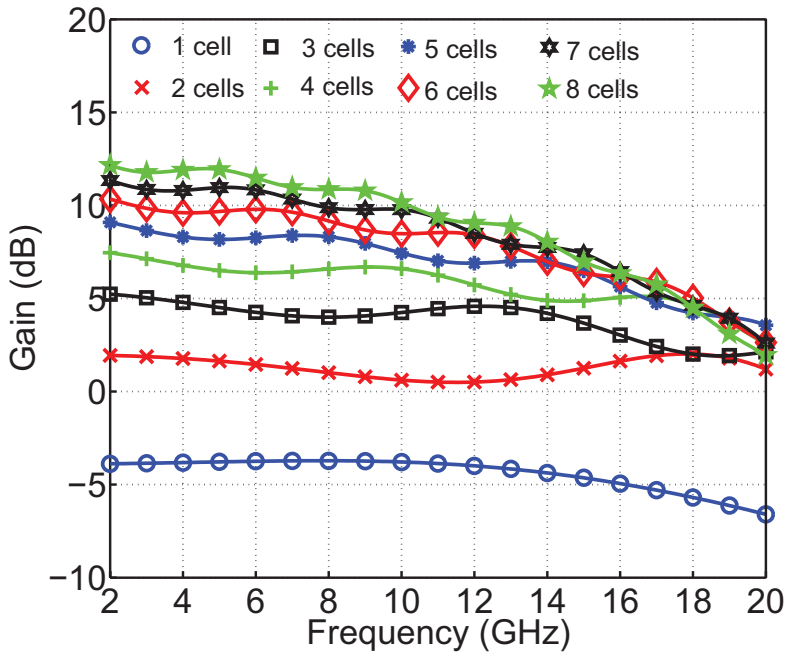

Figure A.5: Gain ($|S_{21}|$) comparisons for distributed amplifiers of varying size (number of cells). Significant improvement is shown going from 1 to 4 cells, but after that the increases in gain are less substantial and decrease gain flatness over band of 4-18 GHz.

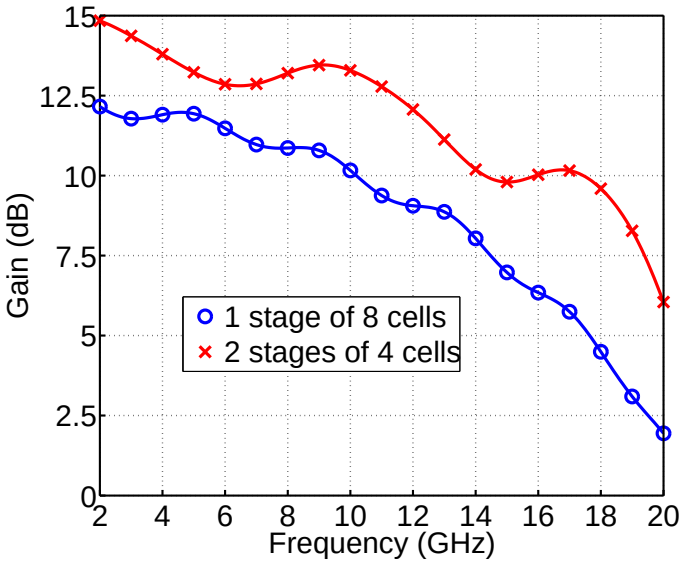

Figure A.6: Direct comparison of two different ways to configure 8 cells, 1 stage of 8 as compared to 2 stages of 4. The 2-stage design clearly has more gain at all frequencies from 2-20 GHz.

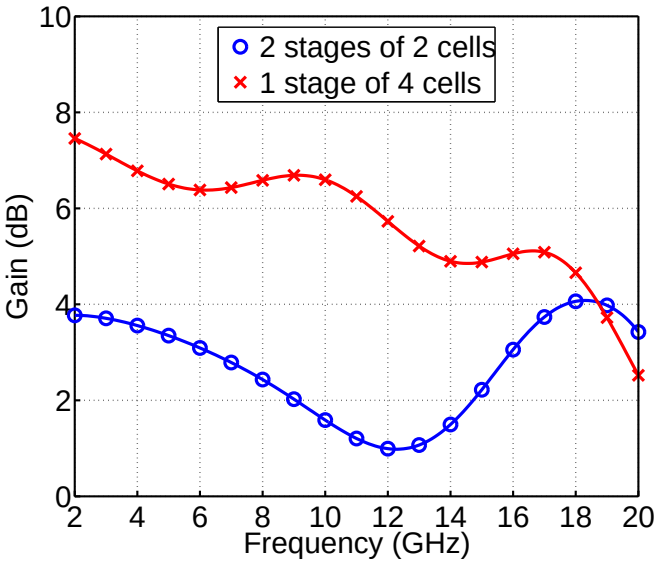

Figure A.7: Direct comparison of two different ways to configure 4 cells, 1 stage of 4 as compared to 2 stages of 2. Unlike the two configurations of 8, the 1-stage configuration has higher gain over design bandwidth of 4-18 GHz.

to three stages could be used. Three stages was chosen due to its superior gain (shown in Figure A.9) as well as its superior space utilization (shown in Figure A.10).

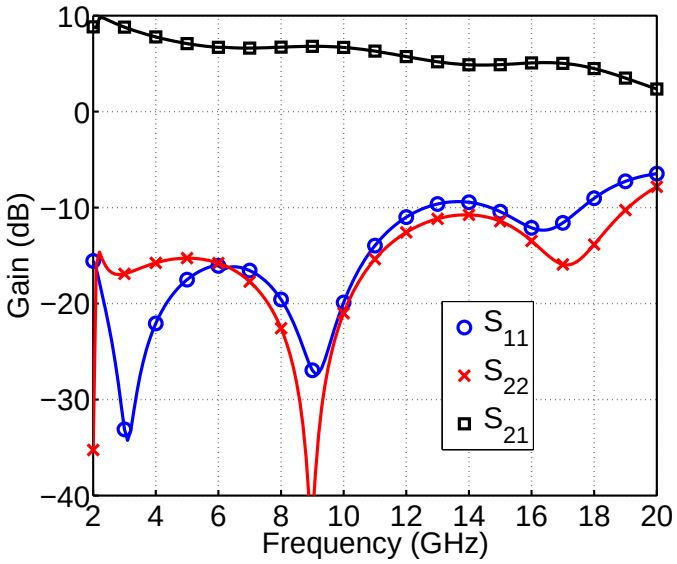

Figure A.8: S-parameters for final stage topology indicating that the stage has fair gain (4.59-9.78 dB) and a standing wave of ~ 6.2 GHz, which corresponds to the stage length

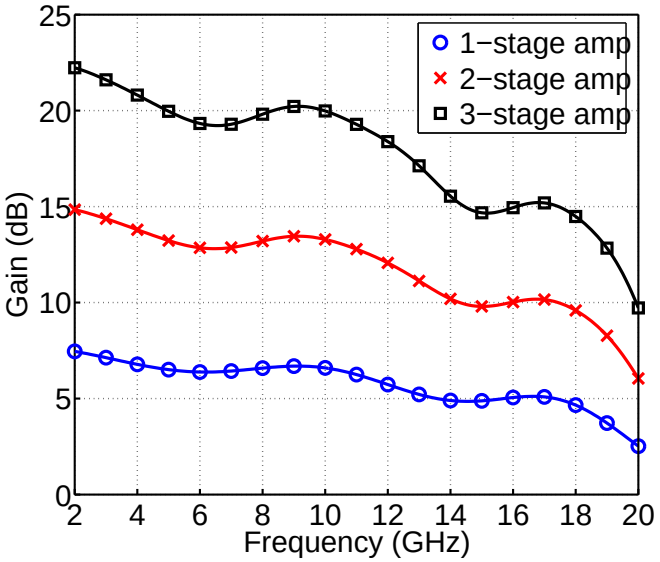

Figure A.9: Graph showing how the number of stages contributes to the overall gain of the amplifier

The clear advantage to the increase in stages is the improvements in gain made in each subsequent addition; however, it is also readily clear that the gain flatness worsens with each gain improvement. This is obviously due in part to the fact that comparing frequencies where

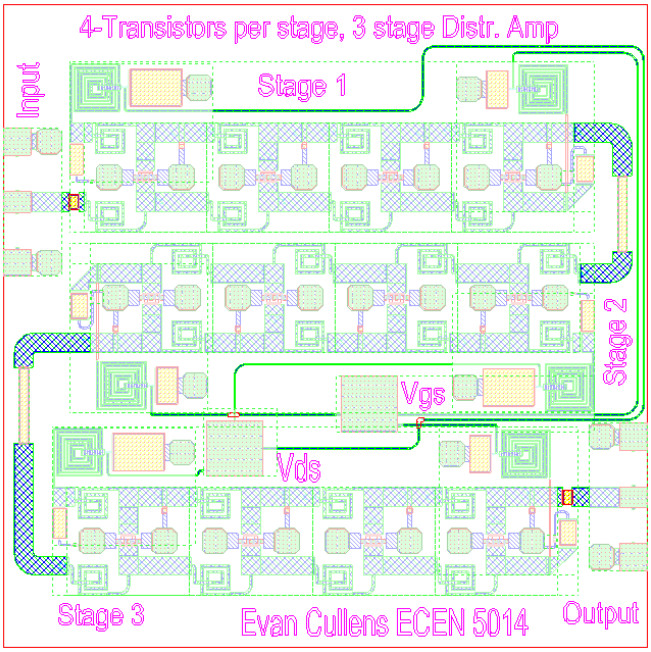

Figure A.10: Amplifier as laid out with 3 stages, 4 cells per stage, which has good real estate usage on the 2.5 mm x 2.5 mm allotted area

gain is larger or smaller, smaller times smaller is much smaller than the larger gains cascaded. However, it is also most likely in part to the cell's impedance not being exactly 50Ω as seen by the standing waves in Figure A.11 and to a much lesser degree the blocking capacitors between stages could be affecting the total circuit's performance. Nonetheless, the circuit performs well. It is of interest to note that although S_{22} has not changed in shape much going from 1-stage to 3-stages, its magnitude has gone up considerably, while S_{11} has acquired possibly another standing wave, seemingly indicating that after amplification the signal is reflecting back through S_{12} adding the second standing wave.

A.6 Completed Design Ratings And Other Performance

Now that the amplifier has been designed, it is worthwhile to examine a few other specifications and then make a list of design ratings. The first specification that is interesting to look at is stability. Several different methods exist to investigate stability, including stability circles [102], the

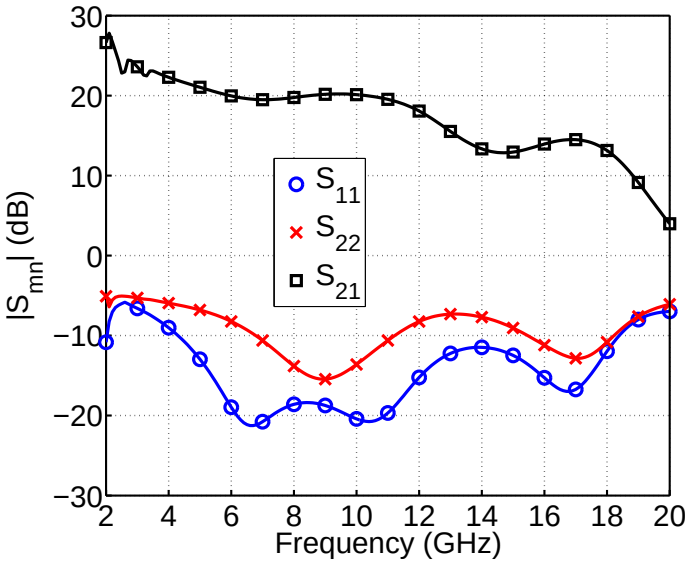

Figure A.11: S-parameters for the completed amplifier including bias tees, input and output lines, and blocking capacitors between stages

K – Δ test [103], and K and B_1 factor analysis [104]. On the designed amplifier, the last method was used to determine stability. The criteria for unconditional stability is that both

$$K > 1 \tag{A.4}$$

and

$$B_1 > 0. \tag{A.5}$$

This analysis was performed on the designed circuit and the circuit was found to be unconditionally stable, as evidenced by Figure A.12. In the figure, K ranges from $\sim$ 200 to over 1000 (truncated by simulator), and B_1 ranges from ~ 0.8 to ~ 1.0 over the frequency range.

The next item of interest, although not specified is noise figure for the amplifier. Since noise is predominantly due to resistances, of which there are quite a few in this amplifier, a large noise figure was expected. However, noise analysis of the circuit showed that the noise figure for the device, seen in Figure A.13 is not horrible dipping below 3 dB midband and always less than 6 dB

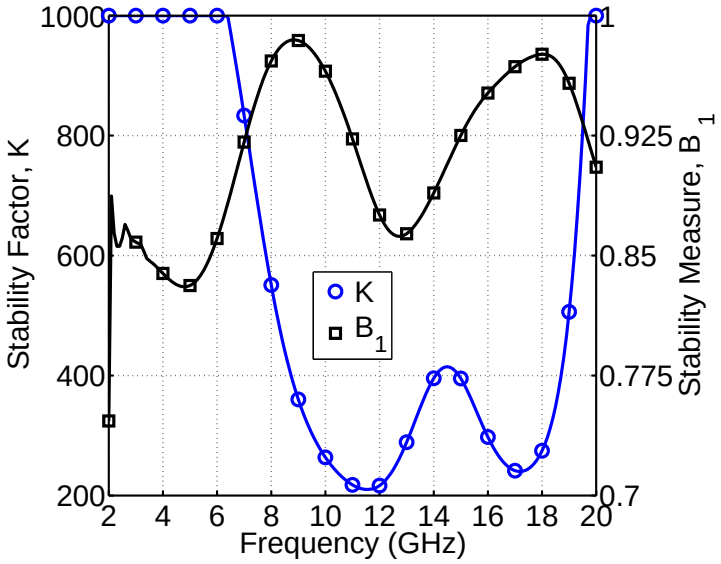

Figure A.12: Graph of K and B_1 stability factors for the complete amplifier showing that the amplifier is unconditionally stable at all frequencies (i.e. $K > 1$ and $B_1 > 0$ at all frequencies)

over the frequency range. Given the standing waves seen earlier, it is plausible that this noise figure could be engineered to be even lower, though it seems unlikely that this would ever make a good low-noise amplifier due to the fundamental necessity for resistors and their affect on noise previously mentioned.

The next item of interest is the linearity in the gain of the amp, or its 1 dB compression point. Since the gain of the amplifier is not perfectly flat, the amplifier should experience different compression points for different frequencies. Four frequencies were considered based on the gain plot of Figure A.11: 4 GHz, 8.5 GHz, 14.4 GHz, and 18 GHz. The output power as a function of input power is shown in Figure A.14. It is easily seen that all of these frequencies are relatively linear between -20 and -15 dBm input power, and all frequencies fall off before 2 dBm of input power. Table A.1 presents the input and output powers at the 1 dB compression point for the four different frequencies. These compression points show a strong dependence on frequency, although the exact nature of that dependence is not quite clear. The highest output power comes at the frequency with the highest gain, and the lowest output power comes at the frequency with the lowest gain; however, the second lowest gain corresponds to the second highest output power. Furthermore, the

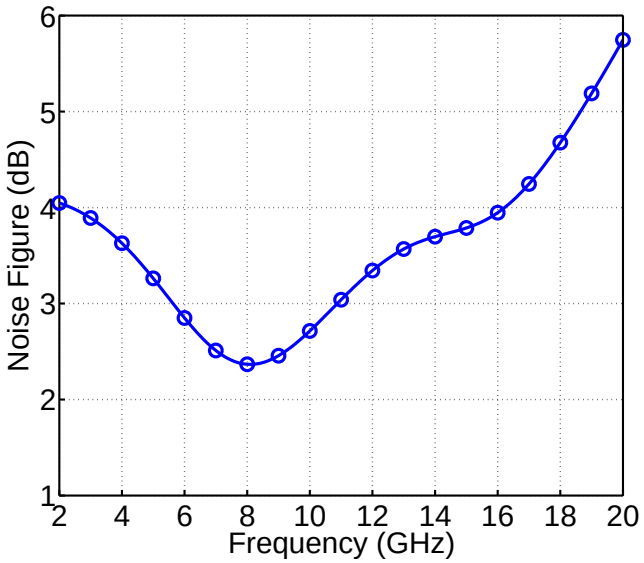

Figure A.13: Noise figure for the completed amplifier showing that midband and complete band noise figure ($< 3\,dB$ and $< 6\,dB$ respectively) are not bad, but as designed not sufficiently good for use as a low noise amplifier

highest output power at compression and the lowest output power at compression both correspond to roughly the same input power. All in all, except for the confusing behavior at 14.4 GHz (which was chosen specifically because there is some strange behavior causing a local minima in gain) the amplifier seems to work well, having a 1 dB compression point near 9 dBm output power.

Table A.1: Comparison of 1 dB compression point powers for different frequencies

Frequency	P_{in} at compression	P_{out} at compression
4.0 GHz	-6.0 dBm	12.54 dBm
8.5 GHz	-8.6 dBm	8.95 dBm
14.4 GHz	-6.6 dBm	4.90 dBm
18.0 GHz	0.0 dBm	11.88 dBm

The last thing examined about this amplifier is how much power it should be able to handle. Novice engineers often neglect to examine things such as current handling capabilities for bias lines or power that a resistor is expected to dissipate, so for completeness they are discussed here. The

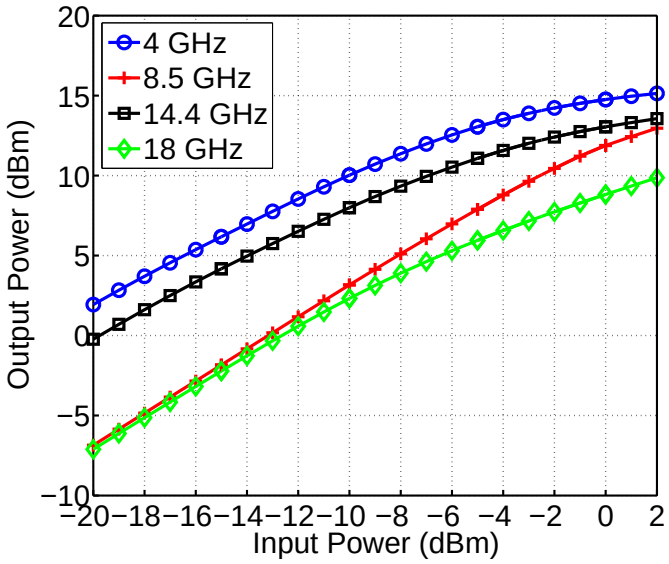

Figure A.14: Graph showing how gain rolls off for the amplifier at four different frequencies, 4.0 GHz, 8.5 GHz, 14.4 GHz, and 18.0 GHz

bias lines for this amplifier are designed to handle up to 18 mA of DC current, while the bias current for a single section of line is expected to be 14-16 mA for a 5 V_{DC} bias (the gate bias current is negligible). The resistors are sized to handle 6 mA of current a piece, which considering resistive losses (I^2R) comes to 1.8 mW or 2.55 dBm. Although some sources state that one-half of the RF power goes into the 50 Ω termination of the output transmission line [97], Figure A.15 shows that for a given stage, for an input of -1 dBm on the input port (Port 1), the power present on the terminated drain port (Port 3) is a strong function of frequency. Furthermore, a standing wave seems to appear corresponding again to the length of the stage. This then is more in line with sources that say that there is "also a backward traveling wave component on the drain line, but the individual contributions to this wave will not be in phase" [105] so one should not expect half the RF power to be dissipated in the drain termination. Since the calculated maximum dissipated power is 2.55 dBm and Figure A.15 shows 2.32 dBm of power dissipated for -1 dBm input power, this can be assumed to be maximum power, so the power out of this stage (Port 2) is the maximum power out for the amplifier, 6.23 dBm. When viewed in context with the gain of two stages cascaded and the 1 dB compression point data gathered above, the conclusion is that -6.0 dBm is the limit

for input power to the amplifier as a hole in order to maintain both linear gain and the amplifier's safety based on power (disregarding any safety margins).

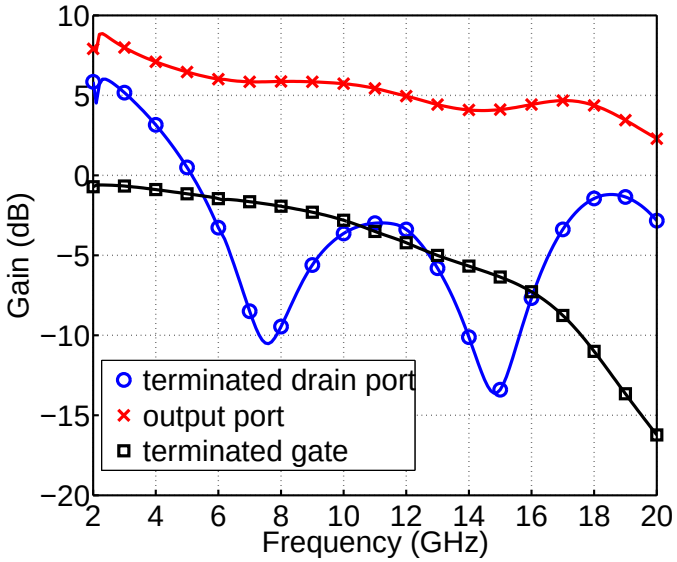

Figure A.15: Graph of how much gain is present from the input port to all other ports within a single stage of the distributed amplifier.

Thus the overall behavior of the amplifier can be summarized as follows:

- Design Frequency Range: 4-18 GHz
- Gain - 17.7 dB ± 4.57 dB
- P1dB - ∼5 dBm or better output power
- Maximum Input Power - -6.0 dBm
- Midband Noise Figure - $<$ 3 dB
- DC Power Consumption - $\leq$ 250 mW at $V_D = 5V$

A.7 Summary

A distributed amplifier with bandwidth from 4-18 GHz was designed. This design was implemented in several stages including selection of number of transistors per stage, number of stages,

bias tee design, and matching design. The final design consists of 4 transistors per stage whose size allows for 50Ω transmission lines both for the input (gate) and the output (drain). The four transistors per stage allowed for a reasonable amount of gain flatness, while the three stages allowed for relatively high gain (∼20 dB). The noise level was better than 3 dB at it's best and better than 6 dB for the entire band.

One incredibly interesting behavior was noted during this design process. This behavior was the incredibly odd gain of a single cell (single transistor aligned in distributed amplifier configuration). This behavior is shown in Figure A.16. Since the transistor is an active device, a single cell is expected to have gain. However, Figure A.16 shows that the single cell actually causes between 3 and 7 dB of attenuation. Previously it was shown that if the number of cells is at least 2, there is gain greater than unity which increases with each subsequent cell (to a limit as discussed in [101]), so this single cell behavior truly is a conundrum. Should this single cell behavior be better understood and engineered, it is feasible that the amplifier overall could have dramatically improved performance. At this point, the diminutive size of the transistor in order to obtain the capacitance desired (4 gates of width 14um for an active area of 64 square um, which is well below the 6 gates of width 50 um or 300 square um default for a device) is the leading candidate for the cause of this phenomena, but further investigation is warranted.

Several lessons were learned throughout this design process. The first is that despite designing each transistor cell for 50Ω, a standing wave was seen in almost all the results. This implies that although each stage is matched well to each other, the actual value deviates from 50Ω. This phenomena needs to be understood should a second design iteration be warranted, especially if the technique of stepped impedance cells or stages is to be implemented. This leads into the second observation that although a unilateral transistor model was assumed, perhaps a bilateral model is necessary to both achieve better performance and achieve better matching. The final lesson learned was that the gain of a distributed amplifier is relatively flat over a broad bandwidth, so one should take care in ensuring that matches to terminations and other factors be carefully monitored throughout the process to ensure that the gain doesn't encounter problems prior to the intrinsic

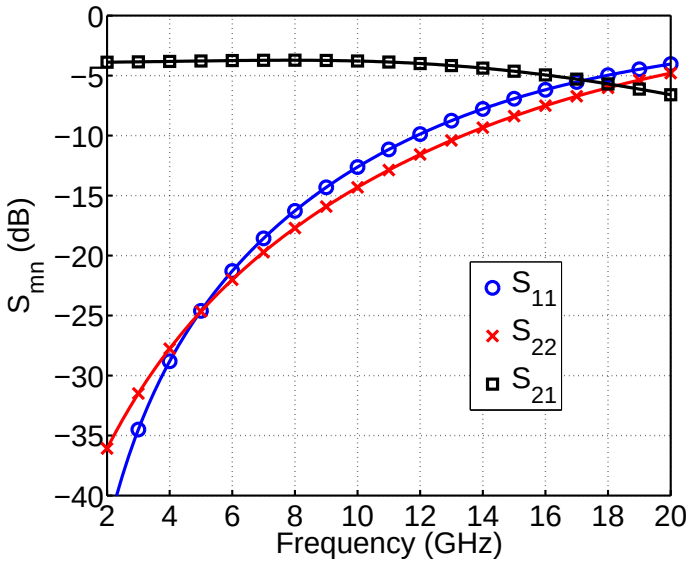

Figure A.16: S-parameters for a single cell showing the odd behavior of $|S_{21}|$ being between -3 and -7 dBm where some value larger than 0 dBm is expected since the cell has a transistor configured to be an amplifier within it

roll-off of the configuration [106]. Nonetheless, this architecture showed itself to be robust and versatile, with a relatively low noise figure and a good gain over a broad bandwidth. Improvements should be sought in maximum output power and compression if possible.