Modular and Reusable Power System Design for the BRRISON Balloon Telescope

by

Nicholas A. Truesdale

B.S. Aerospace Engineering, University of Colorado, 2012

A thesis submitted to the

Faculty of the Graduate School of the

University of Colorado in partial fulfillment

of the requirements for the degree of

Master of Science in Aerospace Engineering

Department of Aerospace Engineering Sciences

2013

This thesis entitled:
Modular and Reusable Power System Design for the BRRISON Balloon Telescope
written by Nicholas A. Truesdale
has been approved for the Department of Aerospace Engineering Sciences

_____

Scott Palo

_____

Eliot F. Young

Date _____

The final copy of this thesis has been examined by the signatories, and we find that both the content and the form meet acceptable presentation standards of scholarly work in the above mentioned discipline.

Truesdale, Nicholas A. (M.S. Aerospace Engineering)

Modular and Reusable Power System Design for the BRRISON Balloon Telescope

Thesis directed by Prof. Scott Palo

High altitude balloons are emerging as low-cost alternatives to orbital satellites in the field of telescopic observation. The near-space environment of balloons allows optics to perform near their diffraction limit. In practice, this implies that a telescope similar to the Hubble Space Telescope could be flown for a cost of tens of millions as opposed to billions.

While highly feasible, the design of a balloon telescope to rival Hubble is limited by funding. Until a prototype is proven and more support for balloon science is gained, projects remain limited in both hardware costs and man hours. Thus, to effectively create and support balloon payloads, engineering designs must be efficient, modular, and if possible reusable. This thesis focuses specifically on a modular power system design for the BRRISON comet-observing balloon telescope. Time- and cost-saving techniques are developed that can be used for future missions.

In this thesis, a modular design process is achieved through the development of individual circuit elements that span a wide range of capabilities. Circuits for power conversion, switching and sensing are designed to be combined in any configuration. These include DC-DC regulators, MOSFET drivers for switching, isolated switches, current sensors and voltage sensing ADCs. Emphasis is also placed on commercially available hardware. Pre-fabricated DC-DC converters and an Arduino microcontroller simplify the design process and offer proven, cost-effective performance.

The design of the BRRISON power system is developed from these low-level circuits. A board for main power distribution supports the majority of flight electronics, and is extensible to additional hardware in future applications. An ATX computer power supply is developed, allowing the use of a commercial ATX motherboard as the flight computer. The addition of new capabilities is explored in the form of a heater control board. Finally, the power system as a whole is described, and its overall performance analyzed. The success of the BRRISON power system during testing and flight proves its utility, both for BRRISON and for future balloon telescopes.

Dedication

For Hannah, who reminds me that childishness is essential in remaining innovative and, above all else, sane.

Acknowledgements

My DayStar teammates – Kevin Dinkel, Zachary Dischner and Jedediah Diller – have provided me with electronics and software worth powering for two years. Dr. Eliot Young has allowed us to realize his dreams, and Dr. Scott Palo has guided us along the way.

Contents

Chapter

Tables

Table

Figures

Figure

Chapter 1

Introduction

NASA flies high altitude balloons capable of lifting up to 3000 kg to an altitude of 30 to 35 km [20]. These payloads are often telescopes or other sensors that experience too much interference from the atmosphere to be used effectively on the ground. In flight, optics are above 99.5% of the Earth's atmosphere [36]. This mitigates the problem of turbulence affecting image quality, and also allows sensors to see the full spectrum without absorption by atmospheric gases. These benefits are also offered by orbital satellites; however, many science missions do not require a full space environment, and stand to save millions of dollars by using high altitude balloons instead.

The list of differences between balloons and satellites does not stop at cost, though the disparity between Hubble Space Telescope's roughy $2.5 billion and a balloon telescope's $10 million is substantial. The balloon environment is much more forgiving than space – there is less radiation and the launch vehicle accelerations are comparatively benign – and this enables much simpler payloads that can use commercial electrical components instead of radiation-hardened ones. Balloons also offer accessibility; a payload is flown and recovered in days or weeks, whereas satellites are almost never serviceable. Thus, balloon payloads can be designed more quickly and can be reused after flight. Satellites are ideal for expensive, specialized, one-time use missions. Balloons facilitate inexpensive, modular and reusable science missions that can fly more often.

A current example of the flexibility of high altitude balloons is the BRRISON balloon mission. BRRISON (Balloon Rapid Response to ISON) is a mission to image the comet ISON in the near-ultraviolet and infrared spectra. ISON has chemical emissions in both wavelength ranges – CO_2

at 4.3 microns and OH at 310 nm, for example – that are impossible to see on Earth due to absorption in the atmosphere. A high altitude balloon proved ideal because of the mission timespan; development began in December, 2012 and the payload flew on September 28, 2013. Such a short mission is impossible on orbital satellites because the design process is far too complex. The reusability of balloon payloads allowed an entire telescope and gondola to be repurposed, and the new design work was minimized to optics benches and electronics.

The telescope on BRRISON has a 0.8 meter aperture and a speed of f/17. The beam from the telescope is directed onto two optical benches, one for infrared imaging (IR) and one for near-ultraviolet and visible imaging (UV-VIS). The IR bench was built by Johns Hopkins University Applied Physics Lab (JHUAPL or just APL) in Laurel, Maryland. The UV-VIS bench was developed by Southwest Research Institute (SwRI) in Boulder, Colorado. This thesis will focus on the SwRI portion of the project, specifically the design of the UV-VIS electronics and power system.

The UV-VIS optical bench has two primary science objectives. The first is to image the comet ISON in several near-UV bandwidths to search for OH and other chemicals. The second is a proof-of-concept for a fast steering mirror (FSM) to remove jitter from images and provide pointing as accurate as 0.01 arcseconds. The first proves the usefulness of balloons for science, while the second is a precursor to diffraction limited imaging by larger telescopes. To achieve these goals, the UV-VIS payload uses two scientific cameras, the FSM itself, and mechanisms to adjust mirror and filter positions. There is also a flight computer dedicated to operating these mechanisms and providing command uplink and data downlink on flight. The cameras, mirrors and computer are all COTS components, and showcase the ability of balloons to support commercial electronics. However, COTS power supplies are not as abundant, especially for the computer. Thus, the largest electrical design effort of the project was the design of the UV-VIS power system.

The Electrical Power System (EPS) for the bench was designed to be modular, extensible and reusable. Balloons are perfectly suited to quick turn-around missions, but this is wasted if every new project is begun from scratch. The EPS in particular is critical to **all** balloon systems, and is the first place time and money can be saved by focusing on reusability. Furthermore, almost

all power systems contain the same fundamentals. Even if specialized power supplies are needed for new instruments, a core system still provides the basis for such extensions.

This thesis focuses on power system design at two levels. First, individual circuits will be discussed. These are the building blocks of any system; having a library of tested parts, footprints and circuit designs reduces PCB design time by an order of magnitude. The circuits discussed are broken into four categories: power conversion, switching and control, sensing, and logic. All four are integral subsets of a complete EPS. For each category, part selection and circuit design is detailed as a reference for the reader. Specific design problems are discussed to mitigate problems in future designs. The second level of the system design is piecing together these circuits to form a complete EPS. The power system for the UV-VIS bench will be discussed, again with the motivation of modularity and extensibility. Assembly and testing results for the EPS are used to validate the performance of the circuits covered in preceding chapters.

The first subset of the EPS is power conversion. Providing specific voltages to electronics is primary purpose of the system. Several types of converters are necessary to provide common voltage rails that are also efficient and can supply large amounts of power. Isolated DC-DC converters come first, converting the raw battery voltage supplied to the system into usable, high-power voltage rails. Subsequently, buck converters are used to derive smaller logic voltages from the main rails. In cases where noise and ripple requirements are strict, linear regulators are used to clean the outputs of switching converters. Finally, some of the circuits require filters to prevent noise from permeating the system. Chapter 3 covers all of these circuits, and is mostly concerned with the selection of converters and the peripheral resistors and capacitors needed to make them operate correctly.

Because power without control is rarely useful, the second key component of the EPS is switching. In consumer electronics, switch design is often simple because there is a human operator. Such physical switches are obviously ill-suited for balloons, though, and power relays are large and unwieldy, making them poor choices for a compact, modular system. Thus, the EPS uses MOSFETs for power control. Though smaller and much more convenient for PCB design, MOSFETs can be difficult to properly control. Chapter 4 focuses on the fundamentals of MOSFETs as switches, and

develops four different circuits that can switch positive, negative, and mixed-voltage rails. Solid state relays (SSRs) are also discussed as useful logic converters in isolated systems.

While the previous two chapters are concerned with power control itself, Chapters 5 and 6 discuss the analog sensing and digital logic necessary for the EPS to interface with the rest of a balloon payload and provide health and status data. Chapter 5 focuses on sensing. Within the power system, this extends to current sensors, op-amp circuits used to measure voltage, and ADCs used to sense the outputs of both and convert them to useful data. This data is then sent to an onboard microcontroller, which is detailed in Chapter 6. In addition to taking data, the logic portion of the EPS is responsible for communicating with a host computer and accepting commands to switch power lines. The UV-VIS EPS uses an Arduino microcontroller board for this purpose; the chapter discusses how the Arduino is integrated into the system.

Having established the various circuits that comprise the UV-VIS EPS, Chapter 7 covers the design of the system itself. The EPS is made up of five boards: one COTS power conversion board, the Arduino microcontroller and three custom PCBs that power the optical bench electronics, the flight computer and the thermal control system respectively. The custom boards are called the Main Power Board, the Computer Power Board and the Heater Control Board. Each is built up using the converters, switches and sensors discussed in previous chapters. This chapter goes through the system requirements, the design and layout of the three custom PCBs, and the assembly of each PCB into the stack. The performance of the stack is then analyzed. Due to the compressed time frame of the project, very little data was gathered before the stack was integrated and sealed away. However, the basic functionality of the various circuits validates component selection, footprints and PCB layout practices. In some cases, circuits did not function as well as they were designed to. This will be used to motivate potential design changes for future revisions of the system.

Chapter 8 concludes the thesis, providing insight into the successes and failures in the current UV-VIS EPS design and offering advice for future applications. The reader should now have the building blocks for a successful power system, as well as a case study for how to assemble these into a modular, extensible and reusable power stack.

Chapter 2

Background

Discussion of the BRRISON power system requires an understanding of high altitude balloons, the BRRISON mission, and the UV-VIS component of the gondola design. This section will give background for high altitude ballooning, focusing on the scientific advantages and technologies. It will then focus on the BRRISON design, narrowing from the system as a whole to the UV-VIS bench to the UV-VIS electronics design. The UV-VIS electronics and the science they provide are the motivation for the power system.

2.1 High Altitude Balloons

High altitude balloons are vehicles capable of carrying scientific payloads to 120,000 feet or higher. At this altitude, the negative effects of the atmosphere are mitigated, allowing payloads to perform science that would be impossible on the ground. Recent advances in balloon technologies have made it possible to test advanced optics and pointing systems [21]. These, in turn, could enable scientific observatories that rival the Hubble Space Telescope in terms of image quality. This section discusses the history of modern ballooning and recent technological advances, detailing the current capabilities of high altitude balloons.

2.1.1 History of Scientific Ballooning

High altitude balloons have been used to reach the stratosphere since the 1930s [15]. While original flights were used to send men to near-space, focus shifted to scientific missions in 1961

with the establishment of the National Scientific Balloon Facility (NSBF) in Boulder, Colorado [20]. The facility moved to Palestine, Texas in 1962, where it currently remains [2]. The NSBF was transferred from the NSF to NASA in 1982, and was renamed the Columbia Scientific Balloon Facility (CSBF) in 2006 to honor the Space Shuttle Columbia. Since its inception, the facility has launched over 1,700 balloons [20].

Today, CSBF flies conventional balloon missions – those lasting approximately 24 hours – from Palestine, Texas and Fort Sumner, New Mexico. Longer duration missions on the order of 20 to 40 days are flown from Sweden and Antarctica. With special superpressure balloons, Antarctic missions have reached 55 days with a goal of 100 days [11].

One of the primary goals in scientific ballooning is to loft a telescope that can acquire diffraction limited images to compete with Hubble. This would require long duration flights, weight capacity to support a 2 meter telescope, and highly accurate pointing systems. The first two are supported by CSBF's current balloon facilities; the third is becoming a reality as more payloads prove the concept of arcsecond and sub-arcsecond pointing systems.

The Balloon-borne Large-Aperture Submillimeter Telescope (BLAST) is one of the earlier missions to prove fine pointing of a telescope on a balloon. BLAST has flown four times since 2003 [5]. After one conventional flight, BLAST was flown once in Sweden and twice in Antarctica. BLAST is notable for lofting a 2 meter telescope during these long duration flights, proving that Hubble-sized optics can operate on a balloon. However, BLAST only achieved 5 arcsecond RMS pointing; while sufficient for far-IR observations, visible optics need much finer control.

Recently, the Wallops Arcsecond Pointer (WASP) has proven that it can point a telescope at the sub-arcsecond level [9]. WASP has flown three times from Ft. Sumner, NM, and has established a baseline design for fine steering. The proposed High Altitude Lensing Observatory (HALO) mission, which would fly in 2014, will use WASP along with a fast steering mirror (FSM) to attempt Hubble-like pointing [9].

In parallel with WASP and HALO, the Stratospheric Tetrahertz Observatory (STO) and BRRISON are also proving that an FSM can be implemented on a balloon. STO, with over a

decade of heritage from the Antarctic flights of Flare Genesis and Solar Bolometric Imager before it, is in turn the precursor for BRRISON. STO flew in 2010 and 2012, and achieved similar pointing accuracy as WASP [6]. One of BRRISON's primary goals is to test an FSM within the STO pointing system, proving precision as low as 5-10 milliarcseconds, the same order of magnitude as Hubble.

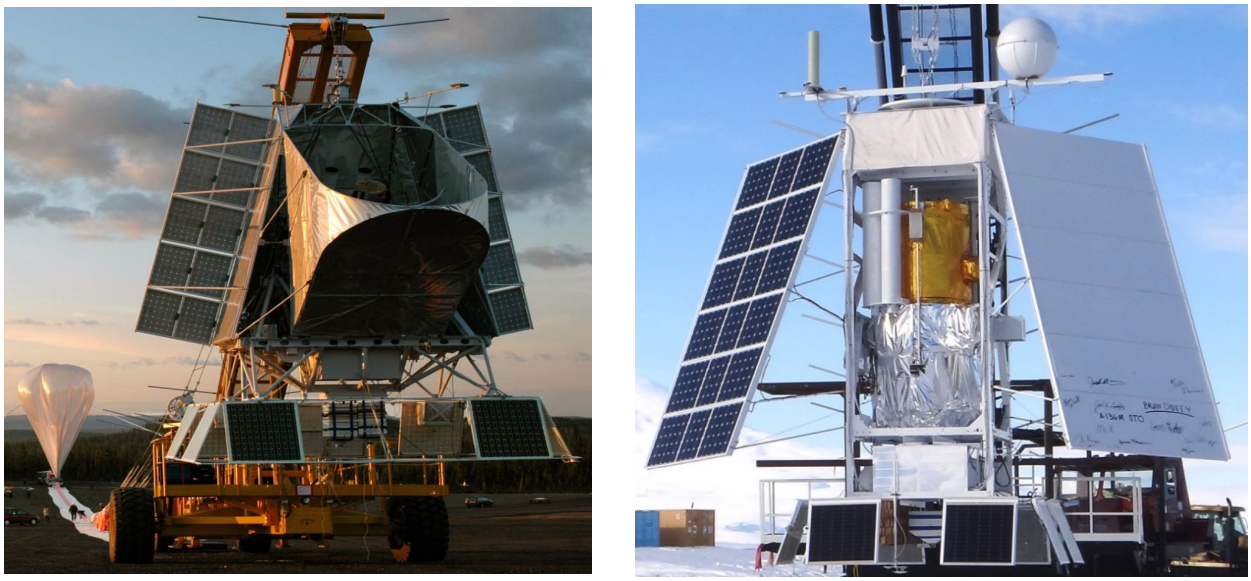

Figure 2.1: The BLAST mission (left) [16] and the STO mission (right) [17] are examples of balloon-borne telescopes that have proven many of the core technologies necessary to achieve near-Hubble performance.

2.1.2 Gondola Capabilities

Balloons are unique in the amount of resources they offer payloads compared to orbital satellites. NASA's newest balloons support payload masses of up to 8,000 lbs, or 3,600 kg, as shown in Figure 2.2. While this is about one third or one quarter of the mass that rockets can send to LEO, the required hardware for balloon payloads is much lower. Short-term flights do not require solar panels, and are controlled with simple line-of-sight communications systems. The structural requirements are also relaxed, because gondolas do not have to survive high loads during launch. Most important, though, is launch cost. Rockets cost roughly $5,000 to $10,000 per kg;

balloons, on the other hand, cost a mere $10 to $100 per kg [18]. The simplicity of balloons reduces design time as well, which further reduces program cost.

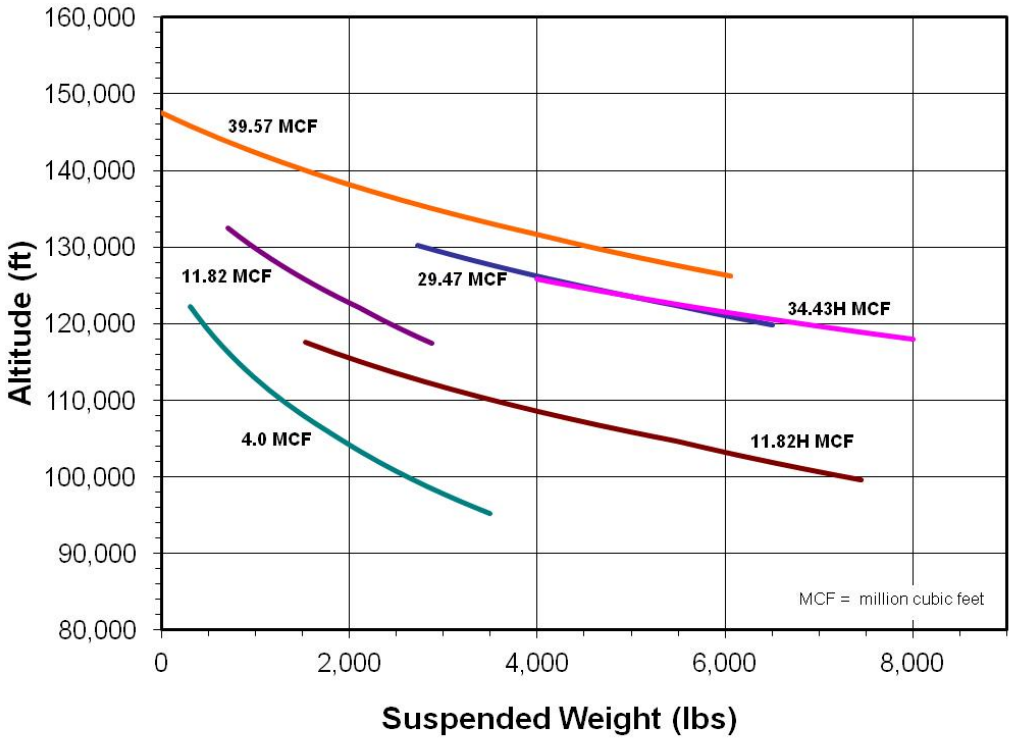

Figure 2.2: CSBF balloons typically offer an altitude of about 120,000 feet, with a payload mass of up to 8000 lbs. New balloons hold as much as 40 million cubic feet of helium, allowing larger payloads to fly higher [20].

High altitude balloons are notable for the lack of design constraints in almost all subsystems. Structurally, gondolas can take almost any shape that is dynamically stable; this leads to very long or tall gondolas for telescopes. Because there is no need to miniaturize telescope optics, conventional mirrors and lenses can be used. Power systems also benefit from gondola size and mass; it is easy to fly large lithium-sulfur battery packs that offer many kilowatts of power. Finally, electronics are simplified by the lack of radiation in the stratosphere, and the possibility of replacement between flights. This allows for inexpensive COTS computers, cameras, and other instruments that could never fly on a satellite.

2.1.3 Flight Types and Locales

Balloon flights fall into three categories: conventional, long duration and ultra-long duration. The first two categories utilize zero-pressure balloons, which have vents to keep the helium inside in equilibrium. These balloons are far simpler to design, but have limited life as helium is lost during day/night cycles. The masses and altitudes in Figure 2.2 are valid for zero-pressure balloons.

Conventional flights are limited by airspace and communications. CSBF flies missions from Palestine, TX and Fort Sumner, NM that last as long as 24 hours. Long duration balloon (LDB) missions are flown in Sweden and Antarctica. Here, the winds cause balloons to circle around the north or south pole, enabling flights that are typically 2 to 3 weeks [20]. The longest flight was made by the Super-TIGER payload, which managed three revolutions about Antarctica over 55 days [10].

Ultra-long duration balloon (ULDB) missions, aim to loft payloads for up to 100 days [14]. This is achieved using super-pressure balloons in stead of zero-pressure ones. The super-pressure balloons are sealed, meaning they can fly indefinitely without venting helium. CSBF has successfully tested a ULDB in Antarctica; future flights will allow payloads to gather significantly more science data than a conventional or even LDB flight. Figure 2.3 shows all three types of balloons in various stages of testing.

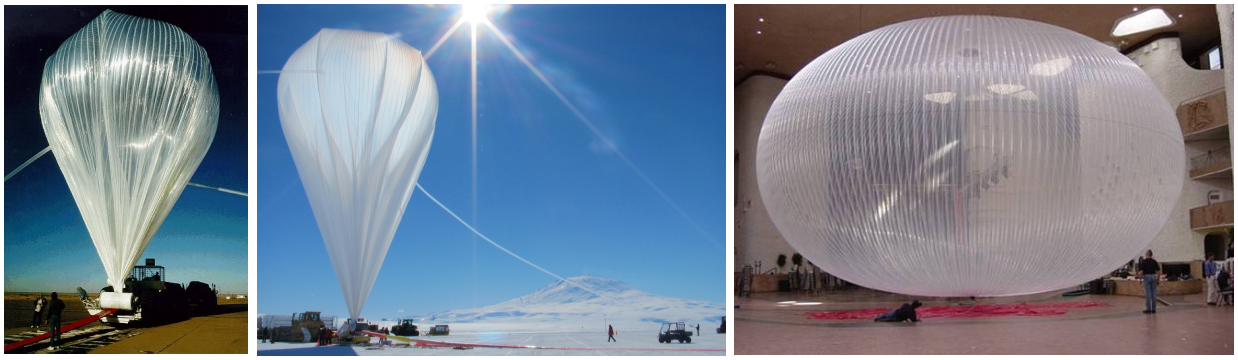

Figure 2.3: From left to right: a conventional balloon launches from Ft. Sumner [20]; an LDB flight commences in Antarctica [10]; a ULDB is tested in a hangar [14].

2.1.4 Environment and Science Capabilities

On the ground, scientific instruments looking toward space are obstructed by the majority of Earth's atmosphere, even when placed atop mountains as the Mauna Kea observatory is. This has several detrimental effects. First, turbulence in the air greatly distorts any image, causing small objects like stars to be blurred out or appear speckled. Second, the atmosphere itself absorbs light due to chemicals like water and carbon dioxide. Especially when so much science is concerned with life-supporting chemicals, this prevents a large percentage of missions from being conducted. Figure 2.4 shows how dramatic atmospheric effects can be even atop Mauna Kea or on the Stratospheric Observatory for Infrared Astronomy (SOFIA) airplane-borne telescope.

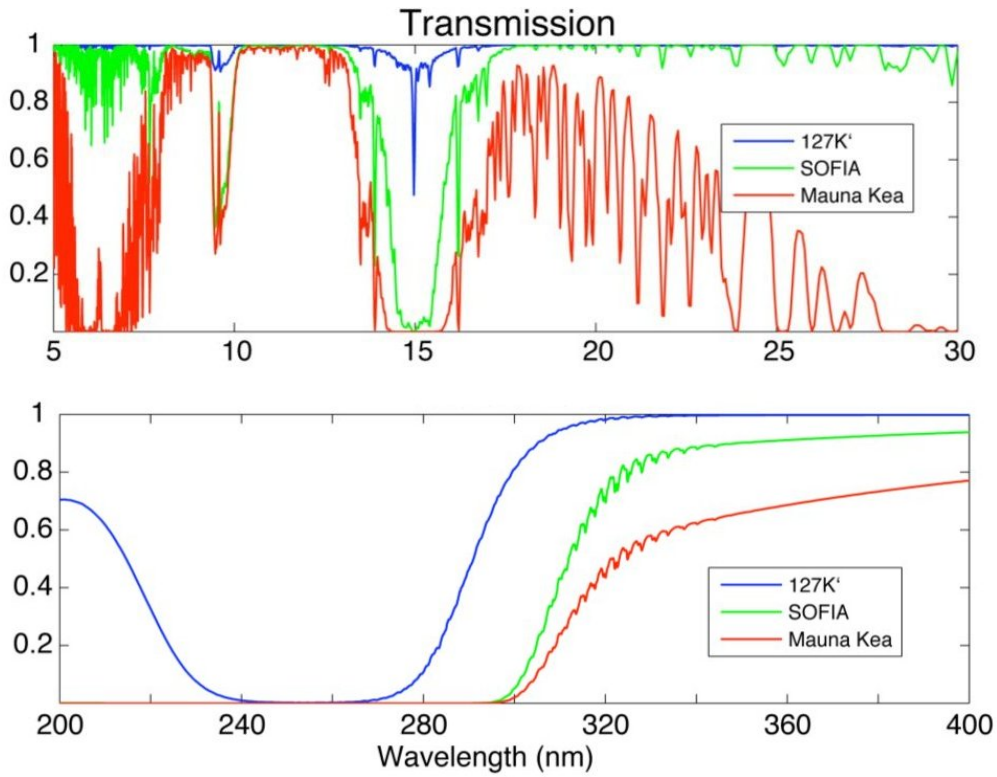

Figure 2.4: Transmission in the mid-IR (top, microns) and near-UV (bottom) is highly altitude dependent. In each band, scientific observations that are impossible on the ground are enabled by high altitude balloons [7].

Telescopes and other instruments on balloons float above 99.5% of the Earth's atmosphere [36]. This mitigates both of the atmospheric seeing problems stated above. There is no turbulence at altitudes of 120,000 feet. As for atmospheric absorption, Figure 2.4 shows transmissivity for near-UV and mid-IR wavelength ranges. Even compared with SOFIA, an airborne telescope, it is clear that high altitude balloons offer far superior seeing than any alternative on or near the ground.

An added benefit of the high altitude environment is that, during daytime, the sky is much darker compared to the ground. Figure 2.5 shows the brightness of the sky versus several parameters. Visibility is especially good in the near-IR spectrum. This enables payloads with IR or not very sensitive visible spectrum instruments to operate diurnally. Furthermore, star trackers and other attitude sensors can keep a gondola pointed during both day and night.

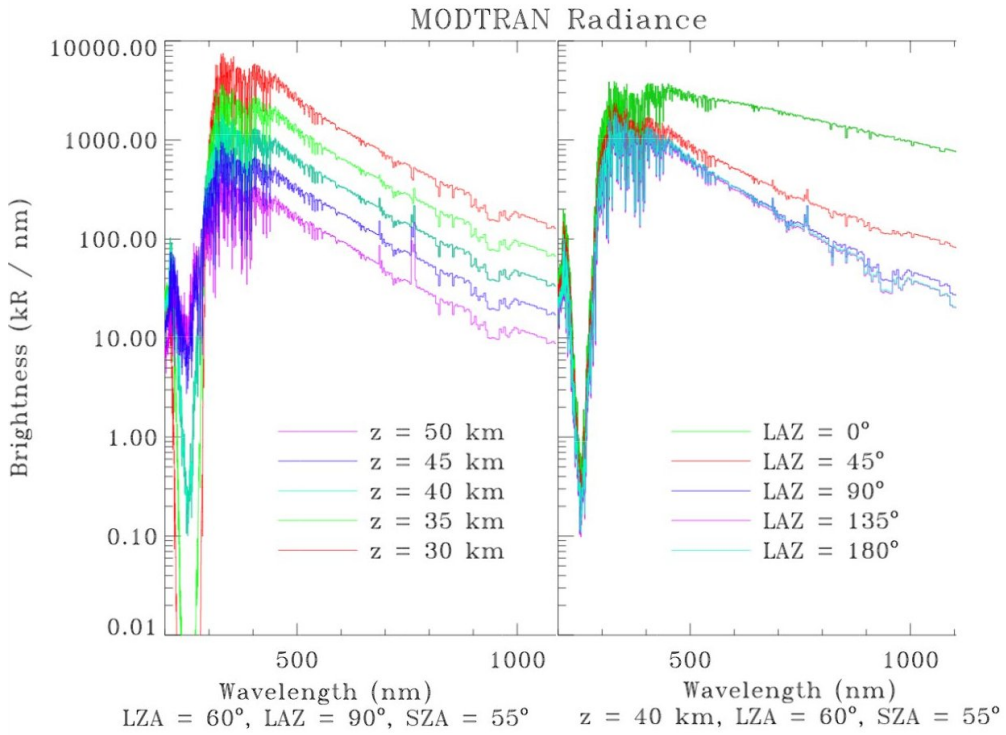

Figure 2.5: A MODTRAN model for sky brightness predicts a λ^4 decay of scattered brightness in the stratosphere [34].

2.1.5 Pointing Knowledge and Control

Another important aspect of optical performance is how accurately a telescope can be pointed. Telescopes are limited in resolution by diffraction. This is a linear function of aperture size and wavelength, given by Equation 2.1. D is the diffraction limit in arcseconds, λ is wavelength in meters and d is aperture diameter in meters.

$$D = \frac{1.22\lambda}{d} \times \frac{206265 \text{ arcseconds}}{\text{radian}} \tag{2.1}$$

Using Hubble as an example, with a 2.4 meter mirror at 500nm, the diffraction limit is 0.0524 arcseconds. The limit is smaller for UV observations and larger for IR. Hubble achieves diffraction-limited seeing over this entire range by pointing with 2-5 milliarcseconds precision for a single observation [12]. To compete with Hubble, balloon pointing systems need to achieve similar precision.

Pointing on a balloon consists of two to three nested stages. First, the gondola is decoupled from the balloon's motion by a flywheel and, sometimes, a vertical wheel as well for elevation control. This stabilizes the gondola on the order of 1-5 degrees. A second system decouples the gondola from the telescope. Azimuth and elevation are controlled by large motors, and roll control may be added as well. This telescope pointing system can achieve accuracies below 1 arcsecond, as shown by plots from STO in Figure 2.6. Similar results from WASP show accuracies as low as 0.22 arcseconds RMS [9].

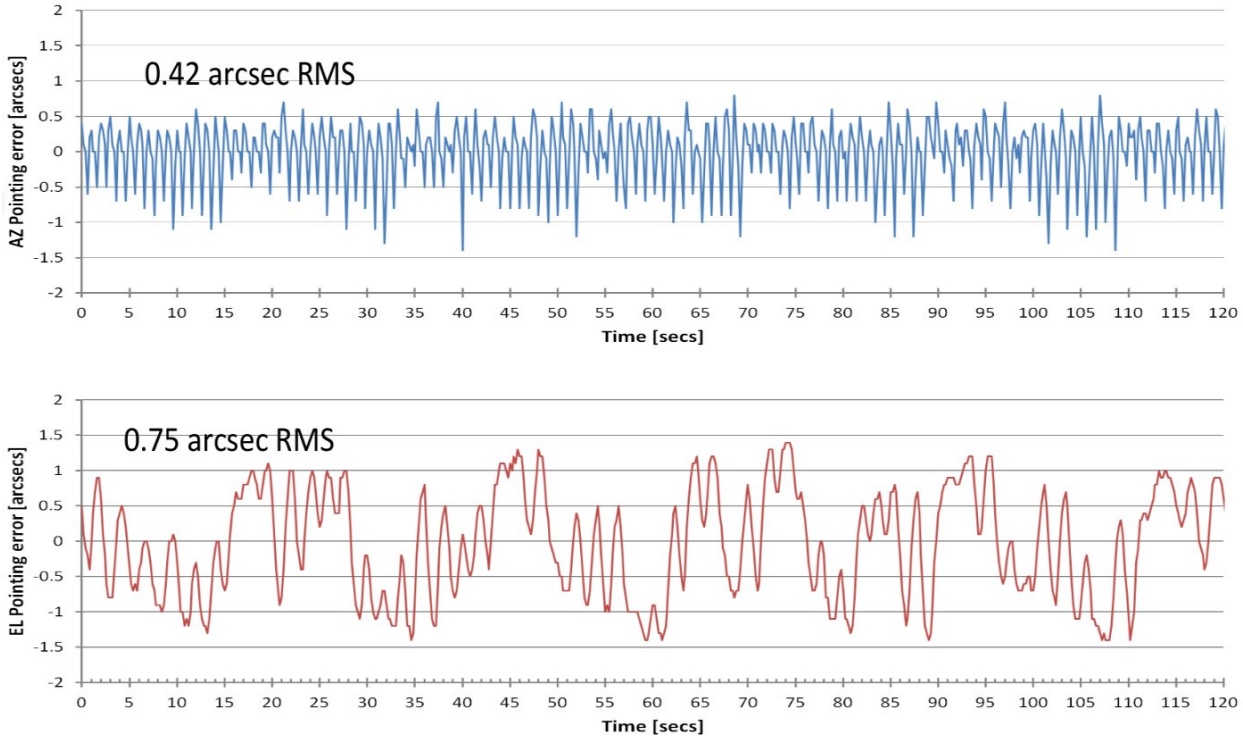

Figure 2.6: STO's telescope pointing system achieves sub-arcsecond precision in both azimuth and elevation [17].

A third stage can be added in the form of a fast steering mirror (FSM). This is a rapidly moving, tip-tilt correction mirror that rejects jitter all the way down to the 10 milliarcsecond range. Simulations from HALO achieve 60 milliarcseconds [9], though the BRRISON FSM is intended to offer 5-10 mas precision, which is nearly as precise as the Hubble Space Telescope.

2.2 The BRRISON Mission

BRRISON is a high altitude balloon mission that flew on September 29, 2013. It consisted of a large balloon gondola housing a 0.8 meter telescope, with separate infrared and ultraviolet/visible optics benches. The target of the mission was the comet ISON; the acronym BRR stands for Balloon Rapid Response, as BRRISON was built in under a year specifically to image the comet.

2.2.1 The Comet ISON

In September, 2012, two Russian astronomers discovered a comet using a telescope that belongs to the International Scientific Optical Network (ISON) [4]. This comet was given the official moniker C/2012 S1, but has since been known as simply ISON. Shortly after its discovery, many other astronomers were able to locate the comet, and the Minor Planet Center projected its orbit to come within 3 solar radii of the Sun. This highly eccentric – almost parabolic – orbit is shown in Figure 2.7. The near pass with the Sun makes ISON a **sungrazing comet**, and its proximity to the Earth means ISON will be visible to the naked eye near its perihelion in November and December, 2013.

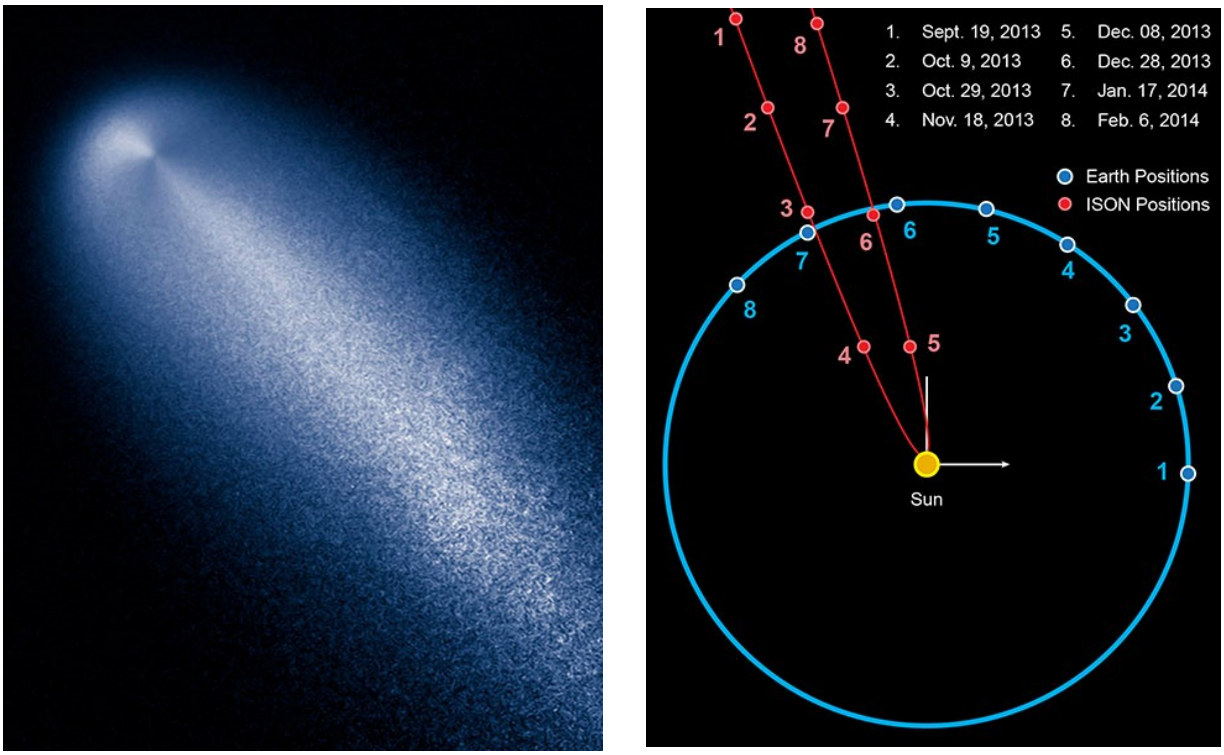

Figure 2.7: At left, the comet ISON is imaged by the Hubble Space Telescope [4]. At right, the orbit of ISON relative to Earth is shown [18]. The closest approach to Earth occurs on December 27, 2013.

While ISON has gained popularity due to its potential as a bright night-sky object, its

scientific relevance is based on its origin. From the comet's orbit, it is clear that ISON is a new body from the Oort Cloud [18]. This means the comet has never experienced large solar or gravitational loads, and its constituent chemicals are largely untouched. Scientists hope to examine OH, CO_2 and water in order to characterize and determine the region in which the ISON formed [3]. This requires observations in the near-UV spectrum for OH, and the near- to mid-IR spectrum for CO_2 and water, which in turn requires a balloon-borne telescope.

2.2.2 BRRISON Mission Origins

Before ISON was discovered, planetary scientists were already working on concepts for a balloon-based observatory. NASA's 2009 decadal survey for planetary science outlined 194 "important questions" that should be answered in the next 10 years. As stated by Tibor Kremic from NASA Glenn, "A balloon platform offers a multi-target/crosscutting capability to address a wide range of decadal science objectives" [16]. Specifically, over 20% of decadal survey questions could be answered by a balloon-borne telescope. In January, 2012, a series of meetings began to analyze the feasibility of an observatory for planetary science, and to develop preliminary designs. Figure 2.8 shows drawings of the proposed telescope gondola.

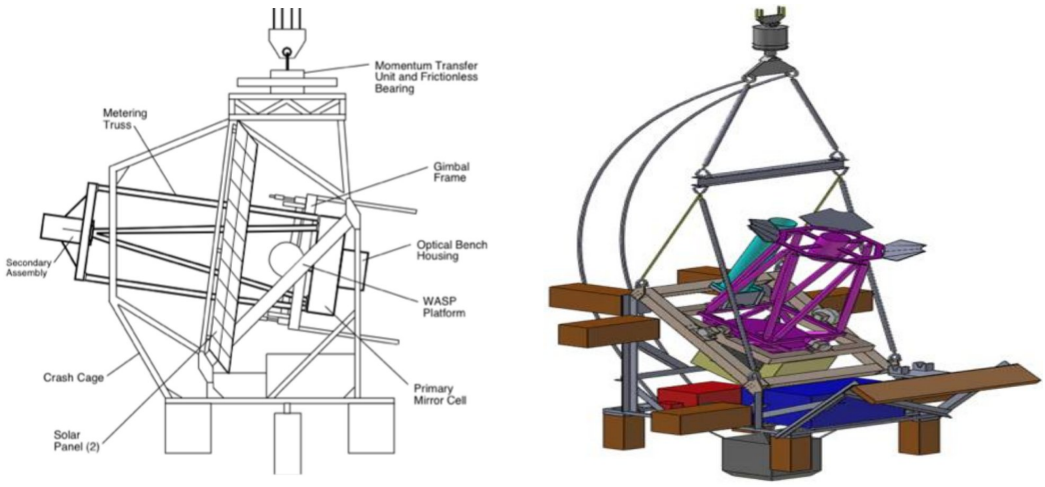

Figure 2.8: A drawing at left [34] and a CAD model at right [8] are both concepts for a planetary science telescope mounted on a balloon gondola.

The discovery of comet ISON prompted much excitement throughout the planetary science community. However, some of the most important questions about new Oort Cloud bodies, such as chemical content and ratios, could not be answered by ground observations because of atmospheric absorption. And, due to the comet's compressed timeline, no orbital payload could be developed fast enough for the necessary IR and UV imaging. A quickly-built balloon payload was the only way to gather this data, so NASA decided to fund a project based on the preliminary planetary science meetings. This payload would become BRRISON.

2.2.3 BRRISON System Overview

Work on the BRRISON gondola was begun in January, 2013. The gondola was fully integrated by August, 2013, as shown in Figure 2.9.

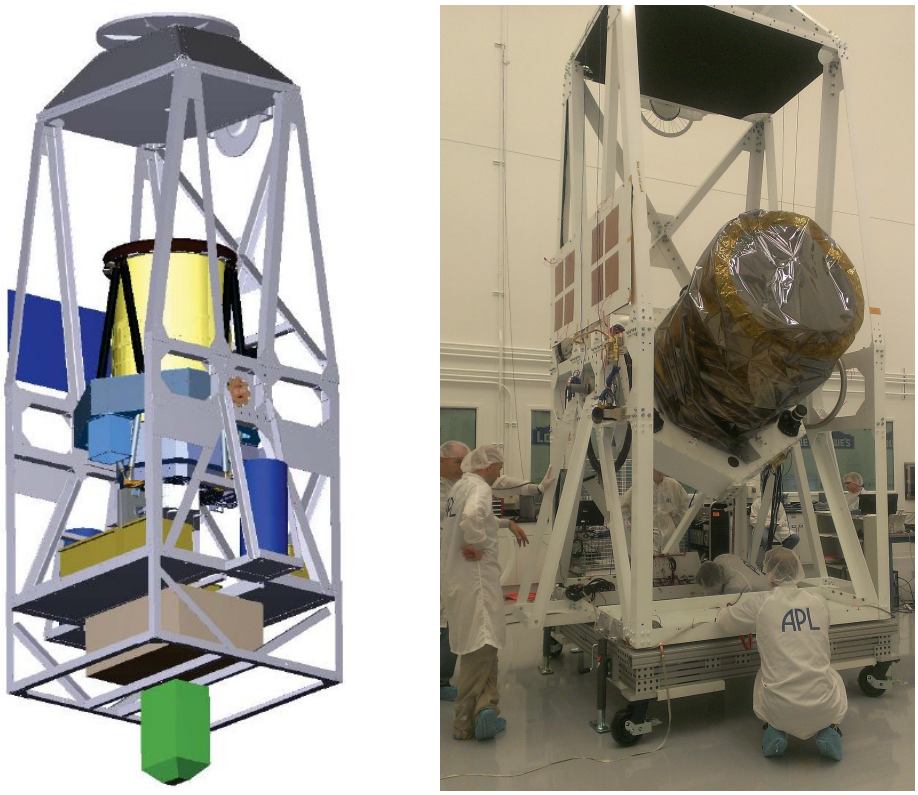

Figure 2.9: The BRRISON gondola, assembled at Johns Hopkins APL in Laurel, MD, houses an 0.8 meter telescope with two optical benches mounted to the back.

Johns Hopkins University APL headed the BRRISON project, and designed the gondola, telescope and IR optics bench. Southwest Research Institute (SwRI) designed and built the UV optics bench. All of the hardware components were integrated at APL throughout the summer of 2013. The gondola was shipped to Fort Sumner in September, checked out, and flown on September 29, 2013.

The BRRISON telescope was actually repurposed from the Stratospheric Tetrahertz Observatory (STO), in order to save time and cost. It is a Cassegrain telescope, with a 0.8 meter diameter primary mirror [6]. The secondary mirror is controlled by a linear stage, allowing the telescope to be refocused during flight to compensate for thermal expansion. Light passes through a hole in the primary mirror, coming to a focus at the first optical bench mounted behind the telescope.

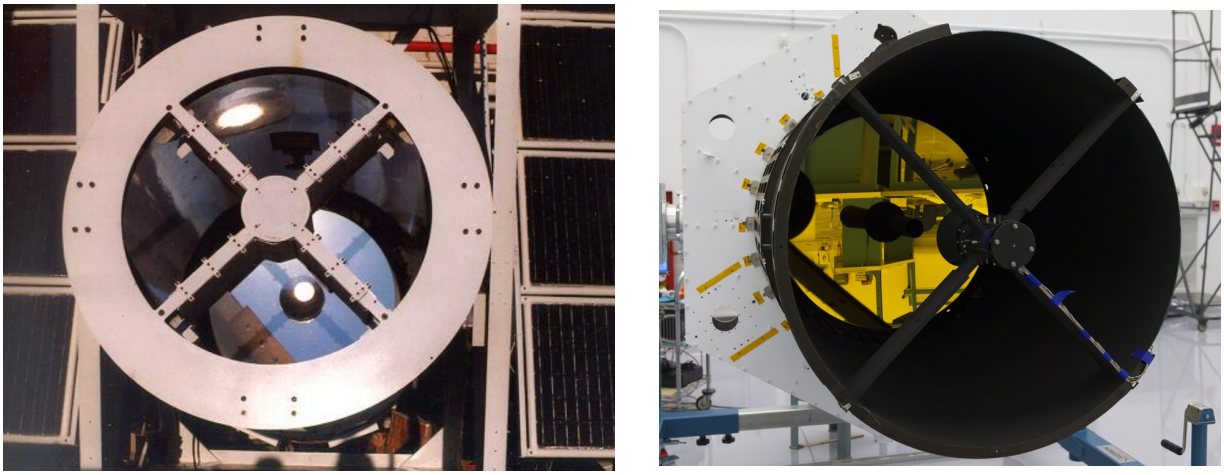

Figure 2.10: STO's telescope, seen integrated with the original payload at left [6], was cleaned, resurfaced and remounted for BRRISON (right) [3].

2.2.4 IR Optical Bench

The first optical bench to receive light is the UV and visible bench (UV-VIS), which is discussed further in Section 2.3. The beam can be reflected onto the bench using a fold mirror, or can pass through to the IR bench. Designed by APL, the IR bench holds a Teledyne H2RG 1-5 micron scientific camera. Designated the BRRISON IR camera (BIRC), this sensor is tasked with

observing near- and mid-IR bands in search of Carbon Dioxide and water spectra. Figure 2.11 shows the optical layout and the camera/filter wheel assembly.

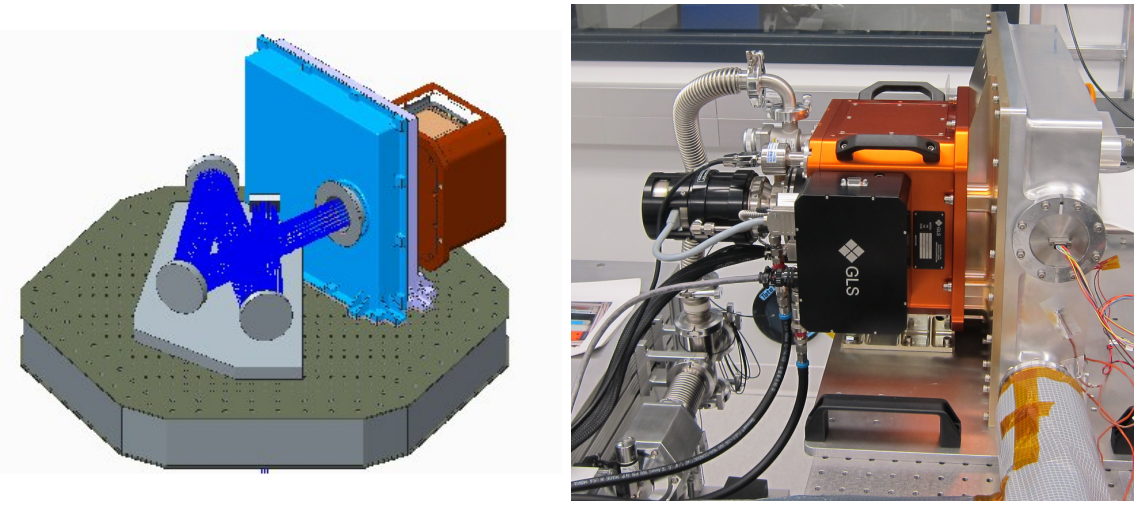

Figure 2.11: The light beam from the telescope is directed through a filter wheel and into the Teledyne IR camera enclosure. The camera itself, at right, must be cooled to cryogenic temperatures to decrease thermal noise [3].

2.3 SwRI and the UV-VIS Optical Bench

The ultraviolet and visible spectrum (UV-VIS) bench for BRRISON provides valuable near-UV science, but also holds the FSM-based super-fine steering system. One of the top level goals of the project is to test this mirror, proving it can point to better than 10 milliarcseconds. If this can be shown, future flights of the BRRISON gondola could rival the performance of Hubble, especially if the existing telescope is upgraded to a 2 meter instrument.

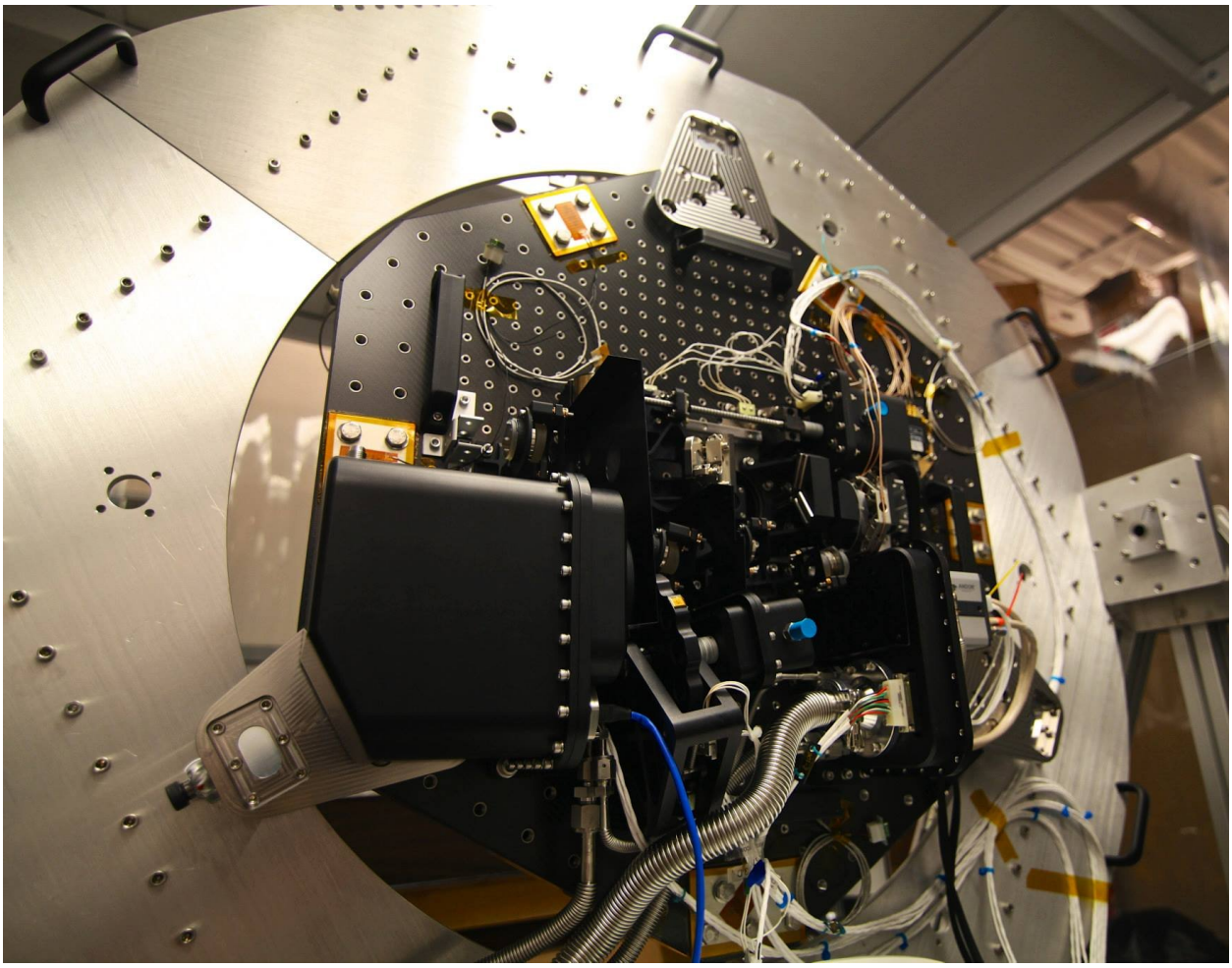

Figure 2.12: The UV-VIS optics bench redirects light from the BRRISON telescope onto a science camera and a guide camera. The light beam is controlled by an FSM, which reduces jitter to less than 0.01 arcseconds.

2.3.1 Optical Bench Design

The UV-VIS super-fine steering system consists of three main components: the FSM, a guide camera and a science camera. The guide camera is used to close the control loop with the FSM, providing feedback on the motion of objects in the frame. The FSM is actuated to cancel out this motion, providing a consistent scene for the science camera to image. Both cameras come after the FSM in the optical path; the guide camera takes images at better than 100Hz, while the science camera may take exposures from 10ms to 30s. For the BRRISON test flight, the science camera is

used to measure the RMS error of the FSM control law.

Getting the telescope beam to focus correctly on two sensors requires several passive optics. Once light is on the bench and has been deflected by the FSM, an off-axis parabolic mirror columnizes the light and directs it onto a dichroic mirror. The dichroic has the property of passing light above 600nm, while reflecting light below 600nm. Thus, all red and IR light is passed to the guide camera, while blue and near-UV light is passed to the science camera. Both beams are refocused with another off-axis parabola before being imaged onto their respective sensors.

There are two other optical mechanisms on the UV-VIS bench: an insertable fold mirror and a filter wheel. The fold mirror is used to redirect light from the telescope onto the bench. If it is retracted, light instead passes to the IR bench. The filter wheel comes right before the science camera. Much like the wheel on the IR bench, this one contains several bandpass filters, meant for viewing specific emission spectra from ISON. There is also a clear filter for general viewing, and six open mounting locations for future missions.

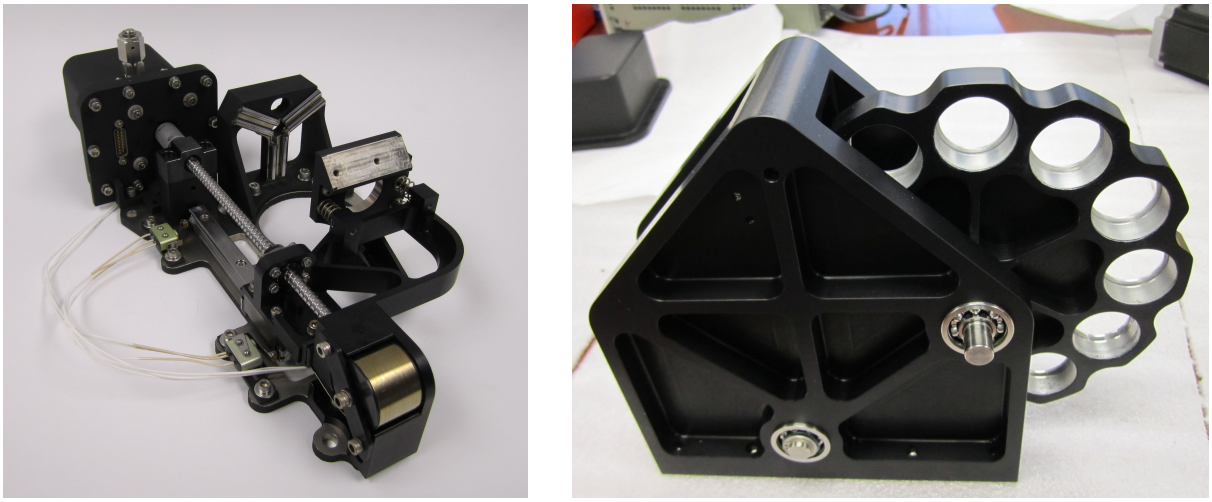

Figure 2.13: The fold mirror (left) and filter wheel (right) mechanisms were designed by High Precision Devices in Boulder, CO.

2.3.2 Bench Electronics

The electrical design of the UV-VIS optics bench focuses on the two cameras and the three optical mechanisms, as well as a thermal control system. These five components are all controlled by the UV-VIS flight computer, which resides in its own pressure vessel away from the bench.

The science camera is shown in Figure 2.14, both alone and mounted on the bench. It is a ProEM+ CCD camera from Princeton Instruments. This camera utilizes a 1024×1024 pixel CCD sensor that is housed in a vacuum chamber. This allows the sensor to be cooled to below $-55°$ C, enabling dark current less than $0.002e^-$ and read noise below $10e^-$. The ProEM is interfaced via gigabit ethernet, allowing it to plug into a computer directly for commanding and image gathering.

Figure 2.14: The science camera is a ProEM scientific CCD from Princeton Instruments. On the UV-VIS bench, it is mounted within a pressure vessel with a power port, an ethernet passthrough for data transfer and a UV-enhanced window.

The guide camera, which is used to control the FSM, is a Zyla scientific CMOS from Andor. The Zyla has a 2160×2560 pixel sensor, which is vacuum sealed and cooled like the ProEM. Unlike the ProEM, the Zyla uses a CMOS sensor rather than a CCD. This allows for much faster readout speeds, which is required to drive the FSM. The Zyla communicates with a computer using two CameraLink cables and an external framegrabber. With this configuration, the Zyla is capable of

transferring full frames at up to 100 frames per second. The camera also supports sub-framing; the UV-VIS control loop can run at up to 600Hz using 80 × 80 pixel frames.

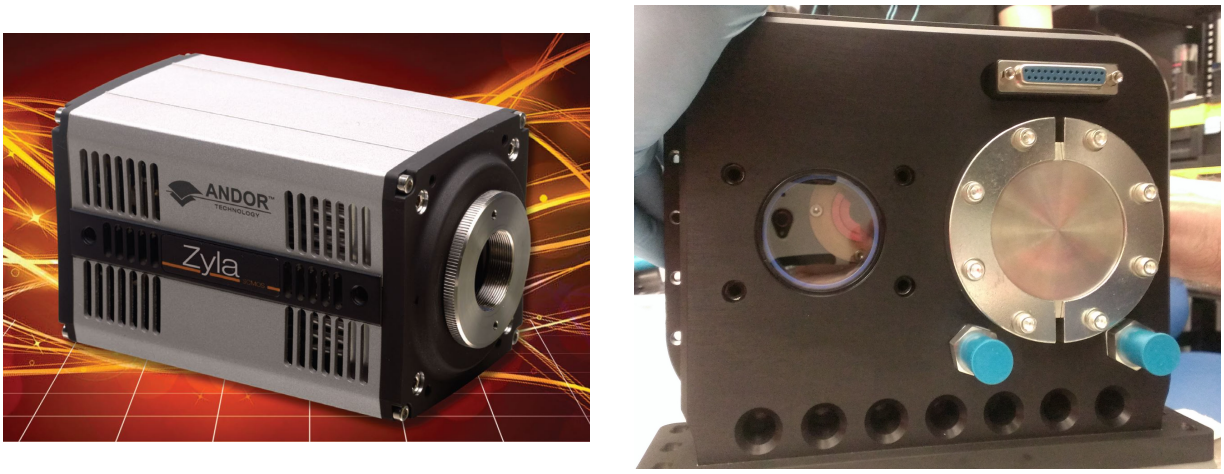

Figure 2.15: The guide camera is a Zyla sCMOS from Andor. It is mounted in a similar pressure vessel as the ProEM, which has ports for power and Camera Link cables.

The FSM is designed by Left Hand Systems. It is an elliptical mirror, 60mm tall and 80.7mm wide, that can be steered over a 10 milliradian range. The angular resolution of the mirror is better than 20 nanoradians when using a clean power supply. This degree of control, combined with the focal length of the telescope, allows the FSM to control the focused beam with about 2-3 milliarcseconds of precision. Left Hand Systems provides control circuitry for the FSM as well. This PCB, called the SC-02, operates on a bipolar voltage source, and takes analog inputs from 0V to 10V that correspond to mirror motion in the tip and tilt directions.

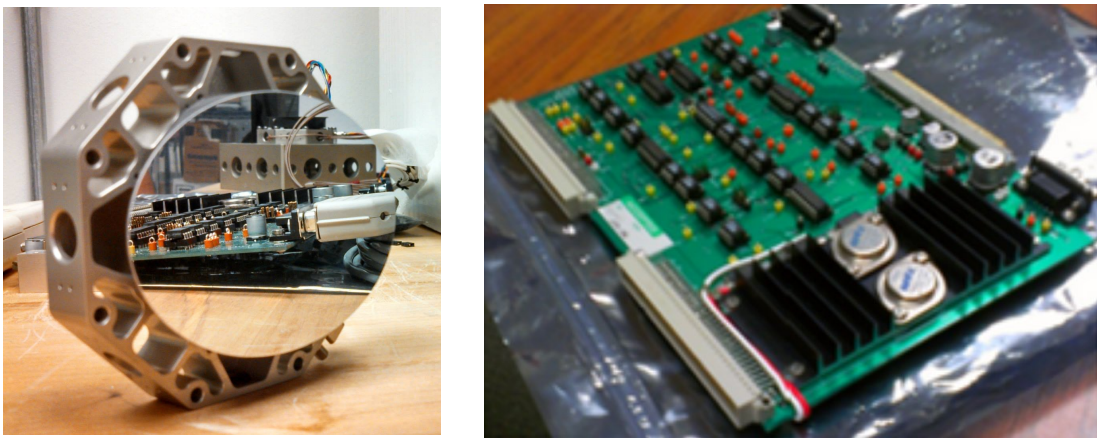

Figure 2.16: The fine steering mirror, left, from Left Hand Systems can correct for motion on the order of 0.005 arcseconds at up to 600Hz. It is operated via a separate control board, right.

The fold mirror and filter wheel are each driven by stepper motors. The filter wheel is spun directly, while the fold mirror is inserted using a worm gear. In both cases, the stepper motor is mounted in a pressure vessel attached to the mechanism chassis. This motor requires a controller, which is shown in Figure 2.17. The two controllers are located in the electronics pressure vessel off of the optics bench.

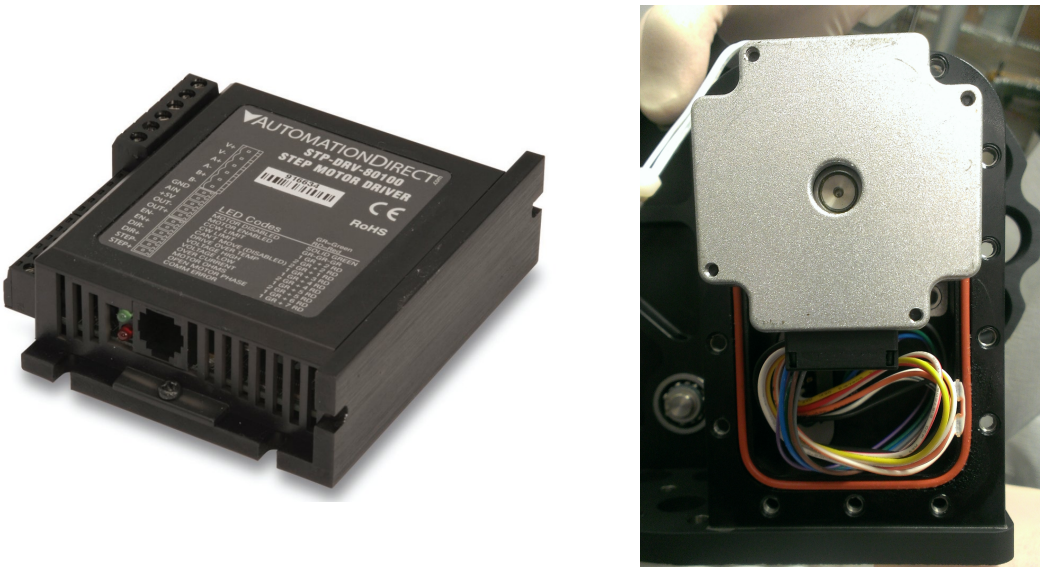

Figure 2.17: Both optical mechanisms are controlled by stepper motors, which require driver electronics (left). The stepper motors themselves are housed in individual pressure vessels (right).

The temperature of the optics bench and its electronics is controlled using an Omron EJ1 commercial heater controller, located in the pressure vessel. This controller reads thermistors on the bench and uses PID control to keep the temperature constant at 20°C. It outputs switching signals for the heaters that are handled by the power system. Figure 2.18 shows the controller and the location of heaters on the optical bench.

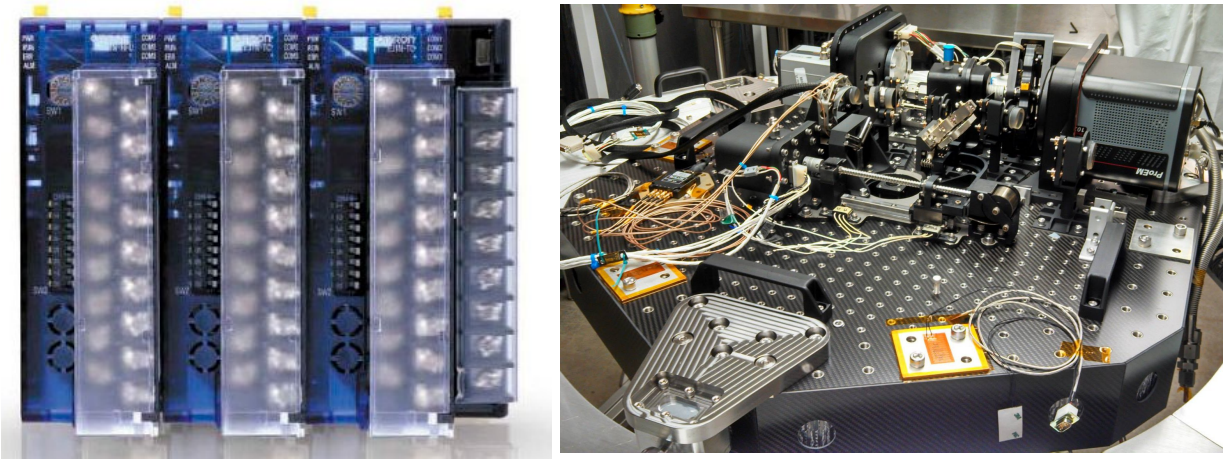

Figure 2.18: The heater controller (left) monitors the heater/thermistor pairs ringing the optical bench (right) in order to keep the bench at 20°C.

2.3.3 Electrical Control System

The UV-VIS optical bench holds five instruments and a thermal control system. These all must be controlled by the flight computer, which is contained in a pressure vessel mounted to one of the rings supporting the optics bench on the gondola. The computer is the foundation of the Electrical Control System (ECS), which also contains the motor and heater controllers shown in the previous section and the power system. As a whole, the ECS controls the UV-VIS optics bench, and also acts as an interface to other computers on BRRISON and the ground support station.

The ECS pressure vessel, shown in Figure 2.19, was designed by HPD. It is a solid aluminum box, with a removable lid that is secured using an O-ring and 50 bolts around the perimeter. Suspended from the lid, an aluminum backplane holds all of the interior electronics.

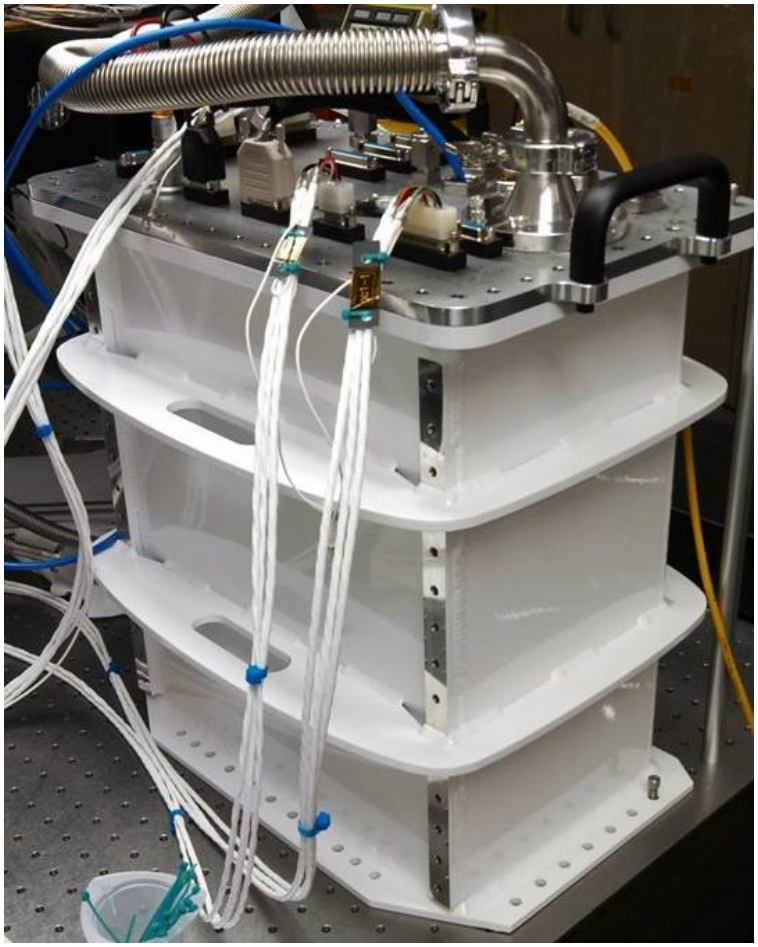

Figure 2.19: The ECS resides in a pressure vessel separate from the optics bench. This box has passthroughs that connect to the cameras, mechanisms and heaters. It also has ethernet and USB ports for programming and ground support communication.

The outer face of the lid holds 21 vacuum-rated passthrough connectors. Power and data cables between the box and the optical bench are predominantly D-Subminiature 9-pin, 15-pin and 25-pin connectors. The exceptions are the ethernet and Camera Link cables for the cameras. The ProEM ethernet cable is unbroken and hermetically sealed, allowing it to travel from the computer directly to the camera. Due to similar concerns about interrupting the sensitive Camera Link cables, a pressure-holding pipe connects the box to the Zyla's pressure vessel, and contains two unbroken Camera Link cables.

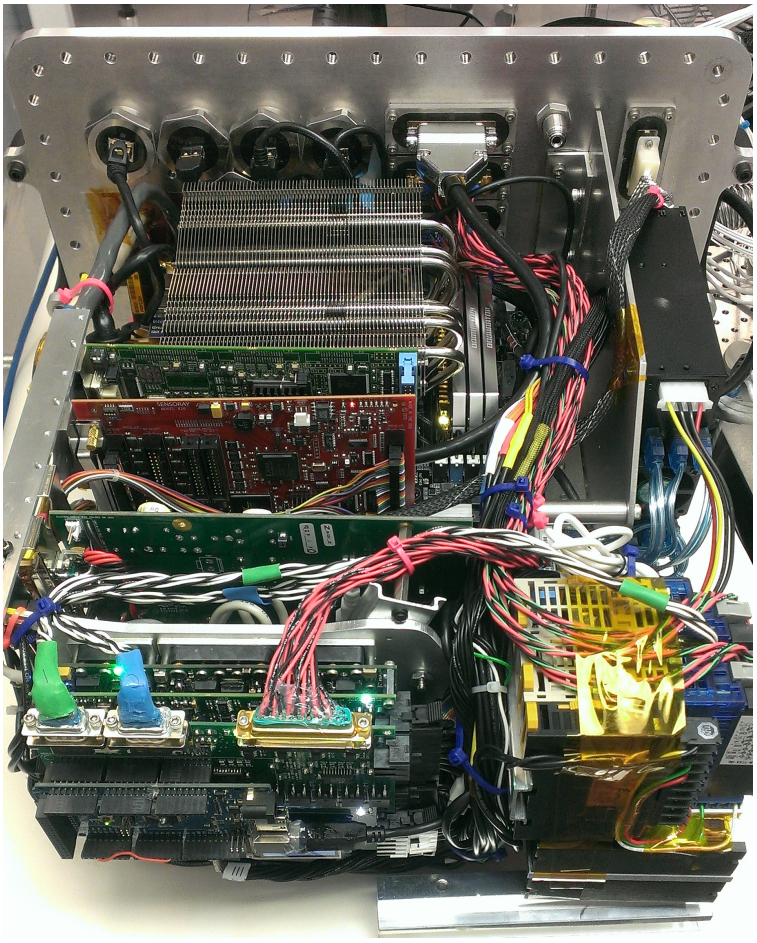

Figure 2.20: The interior of the ECS pressure vessel has a metal backplane, to which the flight computer, its peripherals, the motor and heater controllers, and the power system all mount.

The interior of the ECS box is shown in Figure 2.20. With dimensions 14" by 8" by 16.75", the interior is a tightly packed mix of boards, controllers and wires. The flight computer takes up much of the center of the box, including three PCIe cards, a fan/heatsink, and an enclosure for six SSDs. The power system is mounted in line with the PCIe cards, and the heater and motor controllers are mounted next to it. On the opposite side of the backplane, not visible in Figure 2.20, a VME-550 power card from Aegis and the SC-02 controller for the FSM are mounted. When inserted into the box, the clearance is so small that cabling on all four sides touches the walls, and the power system comes within several millimeters of the bottom.

2.4 UV-VIS Electrical Power System Overview

Where the flight computer is the brain of the system, the Electrical Power System (EPS) is the heart. The EPS distributes power to all of the components within the ECS pressure vessel. Some of these – the two motor controllers and the SC-02 FSM controller – in turn rout power to the optics bench. The cameras and heaters, on the other hand, receive power directly from the EPS.

The UV-VIS EPS receives raw battery power from the gondola-wide power distribution system. The input is nominally 30V, with a range of 20V to 32V based on the batteries' state of charge. It is fused at 20A, meaning the maximum power draw for the UV-VIS payload overall is approximately 600W.

The EPS has three top-level requirements: it must convert voltages to the levels required throughout the system; it must control power to turn on and off different loads; and it must sense and record housekeeping data and respond to errors as they arise. Much of this is achieved using low-level circuitry designed for each specific task. The control and data requirements, however, also drive the need for high-level, configurable logic. Chapters 3 through 5 will discuss the specific circuit designs contained in the UV-VIS EPS, and Chapter 6 will discuss the logic that controls the EPS as a whole.

To meet the top-level requirements in a modular way, the EPS is made up of three custom PCBs: the Main Power Board, the Computer Power Board, and the Heater Control Board. The Main Power Board provides power to everything but the computer, which is powered by the dedicated Computer Power Board. The heaters, which run off of switched battery power, are controlled by the Heater Control Board. Chapter 7 details the overall EPS system design, including the individual boards and the stack as a whole.

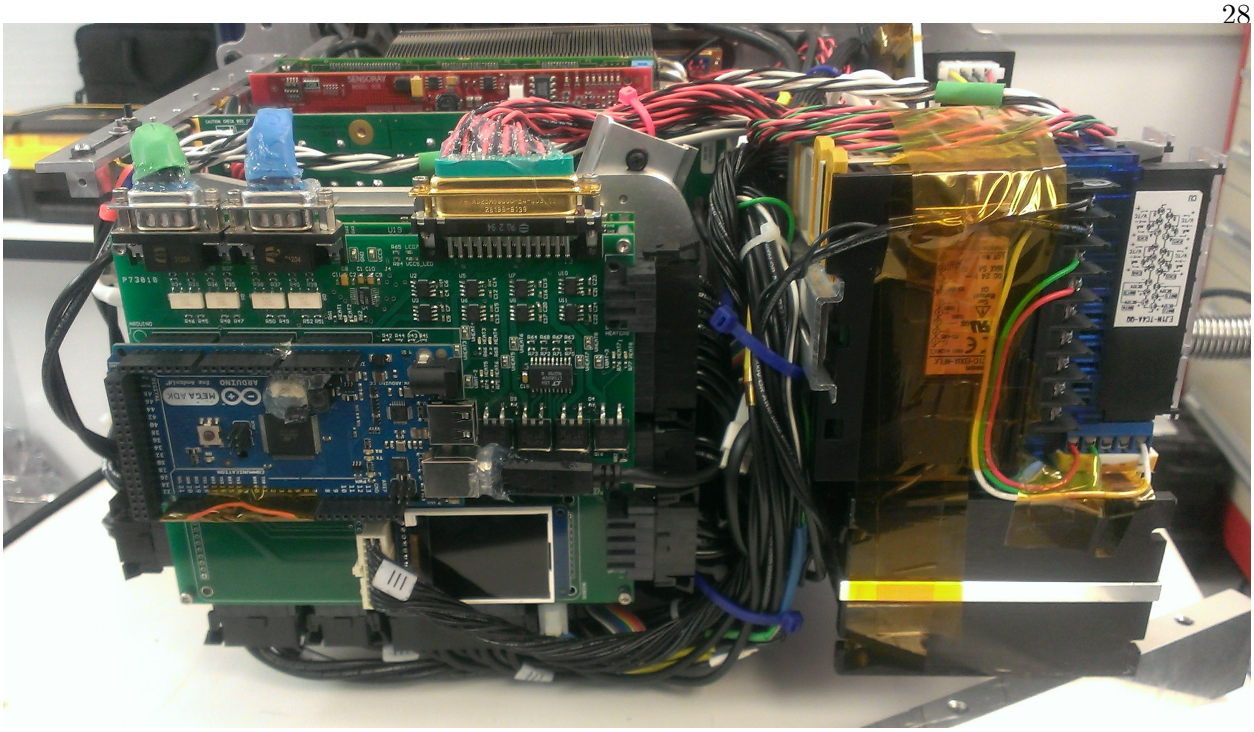

Figure 2.21: The EPS, mounted on the bottom of the ECS pressure vessel backplane, is responsible for converting, controlling, and sensing power for the entire UV-VIS payload.

Chapter 3

Power Conversion

Power conversion and regulation is the most important function of the EPS. Combining several voltage conversion circuits is what allows a disparate collection of electronics – cameras, motors, a computer, etc. – to run from a single battery supply. This section will detail the voltage converters used in the UV-VIS EPS stack.

3.1 Types of Voltage Converters

There are numerous types of voltage converters. Balloon power systems begin with a raw DC voltage, and all but the most specialized instruments also run off of DC power. Thus, all of the converters used in the UV-VIS EPS design are DC-DC converters. This subset of power regulation can be further broken down into linear and switching regulators.

3.1.1 Switching Regulators

The first converters to arise in the design process are usually switching converters. This is due to two major advantages: switching converters have a wide range of input and output voltages, and are also well-suited for high-power applications. Thus, they are typically used to regulate input power and establish main voltages within the system.

Switching regulators consist of a magnetic component (such as an inductor) and a transistor, which is usually a power MOSFET. The duty cycle of the MOSFET controls the power stored in the inductor, and various topologies are used to either increase (boost) or decrease (buck) the input

voltage. Amongst the various switching topologies, a key variable is isolation. Isolated converters use a transformer in place of a standard inductor, allowing the input and output voltages to be fully decoupled. While more complex to design, this isolation is often necessary, especially for system-wide input regulation. The UV-VIS EPS utilizes a mix of isolated step-down converters and more typical buck converters.

DC-DC switching converters are fairly efficient, usually conserving 85% to 95% of the input power. Because of this, large amounts of power can be handled without risking the destruction of the converter. However, this benefit comes at the cost of increased noise. The switching within the regulator circuitry causes transients that can permeate either the input or output voltage rails; ripple can sometimes be as high as 100-200mVpp. Many additional components are required to reduce this ripple; combined with the switch and inductor, this makes designing a switching regulator much more complex than a linear one, especially for high power applications.

3.1.2 Linear Regulators

While not often used for high-power conversion or large voltage drops, linear regulators have their own advantages: low noise and ease of design. Unlike switching converters, which require active and magnetic components, linear regulators are passive, simply dividing the input and dispersing excess power as heat. The output voltage is necessarily smaller than the input; the minimum voltage drop is called the **dropout voltage**, and is an important design parameter because it limits efficiency and also bounds the possible input for a desired output voltage.

Because a linear regulator simply bleeds off extra energy in the conversion process, it becomes highly inefficient as the ratio $V_{\text{in}}/V_{\text{out}}$ grows. Not only is this a problem for power consumption, but the dissipated heat poses a risk as well. Thus, linear regulators are usually only used for low power applications, or when the dropout voltage is as small as possible.

Perhaps the biggest advantage of linear regulators is how little noise they allow on the output voltage rail. Because there are no active or switching components, linear regulators have a **power supply rejection ratio** or PSRR on the order of 60 dB. This translates to a 1000× smaller ripple

on the output than exists on the input. For this reason, linear regulators can be placed at the end of a chain of converters to produce a very clean output voltage. This strategy is used in several parts of the UV-VIS EPS design.

3.2 Main Power Conversion

High power, stand-alone electronics typically require higher DC voltages than board level components. Common voltages are 12V and 24V, though 15V, 18V and 28V appear in many designs as well. Negative voltages are also necessary for some components. In order to be adaptable to various applications, a balloon power supply needs to provide several voltage rails with enough power and current capacity to accommodate the majority of electrical instruments. The rails must be configurable so different voltages can be provided, and they must also be well-regulated to meet the ripple requirements of typical electronics.

The UV-VIS EPS design uses a set of four isolated DC-DC converters to provide two main bus voltages, as well as a positive-negative pair for bipolar applications. The advantage of these converters is twofold: the isolation allows power grounds to remain separate between rails, preventing noise from one rail from permeating the entire system; and isolated converters offer high power output, from 50W all the way up to 350W. This is plenty of power for the majority of applications.

In addition to the converters themselves, each main voltage rail has a noise filter attached to the output. For the two positive main bus voltages, active filtering modules are used to reduce noise from 100-200mVpp to roughly 10mVpp. For the bipolar supply, linear regulators are used.

3.2.1 DC-DC Type I: Positive Bus Voltage

The two main voltage rails – 12V and 24V on the UV-VIS EPS, but configurable for other applications – are supplied using a DC-DC converter brick from Vicor. The brick is a Mini, and is designed with a 9-36V input voltage range (24V nominal). The isolated output allows for an even larger output range; some models step down to 3.3V or 5V, while others boost the input to 36V or 48V. The wide variety of options – all in an identical package – makes the converter very flexible.

Figure 3.1 shows how the Mini is implemented in the UV-VIS EPS design. The converter itself, designated U1, runs with few external components. The four capacitors C1 through C4 serve to filter out small transient currents that the switching power supply generates, shunting them to chassis ground. R3 and R4 serve as lossy elements that can dissipate excess energy. The PC pin on the input side is nominally 4V, and is used to drive an LED when the converter is on.

The other large brick, U2, is a MicroRAM noise attenuator module that Vicor provides to reduce output ripple. Placed in series with the output of the Mini, the MicroRAM can bring the ripple from 200mVpp to less than 10mVpp. To accommodate this, the SENSE pins on the Mini are connected to the attenuator's output; this ensures the output of the entire circuit does not stray from its factory trimmed value.

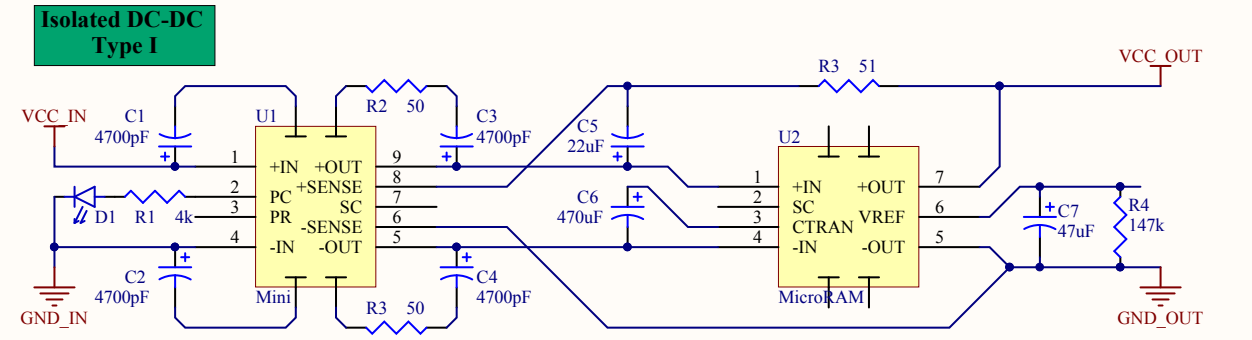

Figure 3.1: The Mini DC-DC converter from Vicor outputs an isolated DC voltage. The MicroRAM module attenuates the noise of the output to as little as 3mVpp ripple.

While some of the external components in Figure 3.1 are included by recommendation of the datasheet, several must be selected by the designer to yield optimum performance. Parts requiring an additional design effort include the decoupling capacitors C1 through C4, the transient response capacitor CTRAN, and the headroom resistor RHR and capacitor CHR.

The decoupling capacitors, C1 through C4, connect the input and output voltages of the Mini brick to chassis ground. The primary goal of the capacitors is to mitigate switching noise by giving transient currents a path to the chassis. Targeting high frequency noise, each of C1 through C4

has a recommended value of 4.7nF or 10nF. The robustness of the capacitors is important, because they pose a safety risk if shorted to the chassis. If possible, each should be a Y capacitor, meaning it is rated for safe bypassing to chassis ground in consumer electronics.

On the MicroRAM module, the CTRAN capacitor controls the output's response to transient load current. Figure 3.2 shows that with no capacitance, there are frequencies for which the transient response is actually amplified by the module, rather than mitigated. In contrast, with a capacitance of 470 µF, the module improves the transient response for all frequencies. The UV-VIS EPS design uses ten 47 µF tantalum capacitors to achieve this bulk capacitance with a 35V voltage rating.

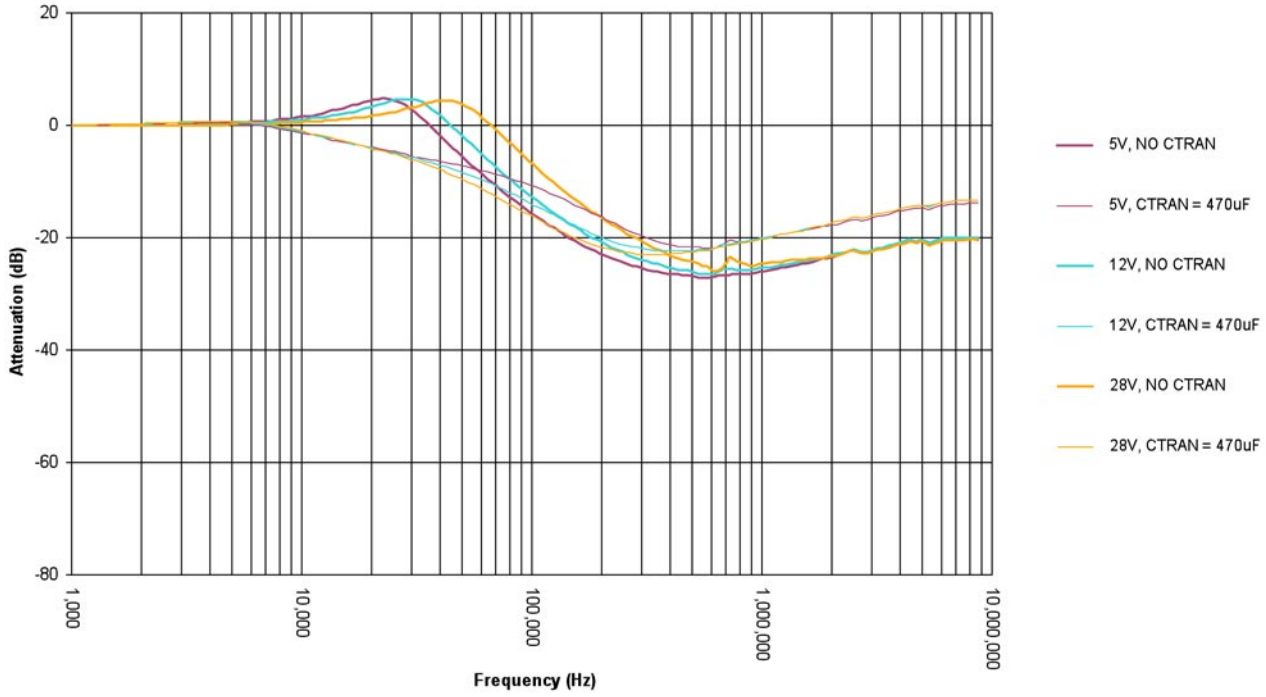

Figure 3.2: The CTRAN capacitor, connected between the CTRAN and VIN- pins on the MicroRAM module, is necessary to remove noise amplification between 10kHz and 80kHz. A large amount of bulk capacitance is required, so many smaller capacitors may be used in parallel.

The difference between the Mini output voltage and the MicroRAM output voltage is called

the **headroom** voltage. While larger headroom necessarily wastes more power, it improves the transient response of the attenuation module. Figure 3.3 shows how the frequency-based response shrinks as headroom increases. The resistor RHR sets the headroom, and differs based on output voltage.

$$R_{HR} = \frac{V_{OUT}}{V_{HR}} \times 2.3\text{k}\Omega \tag{3.1}$$

The UV-VIS EPS sets the headroom at 375mV, which translates to a resistance of 147kΩ for 24V and 73.2kΩ for 12V.

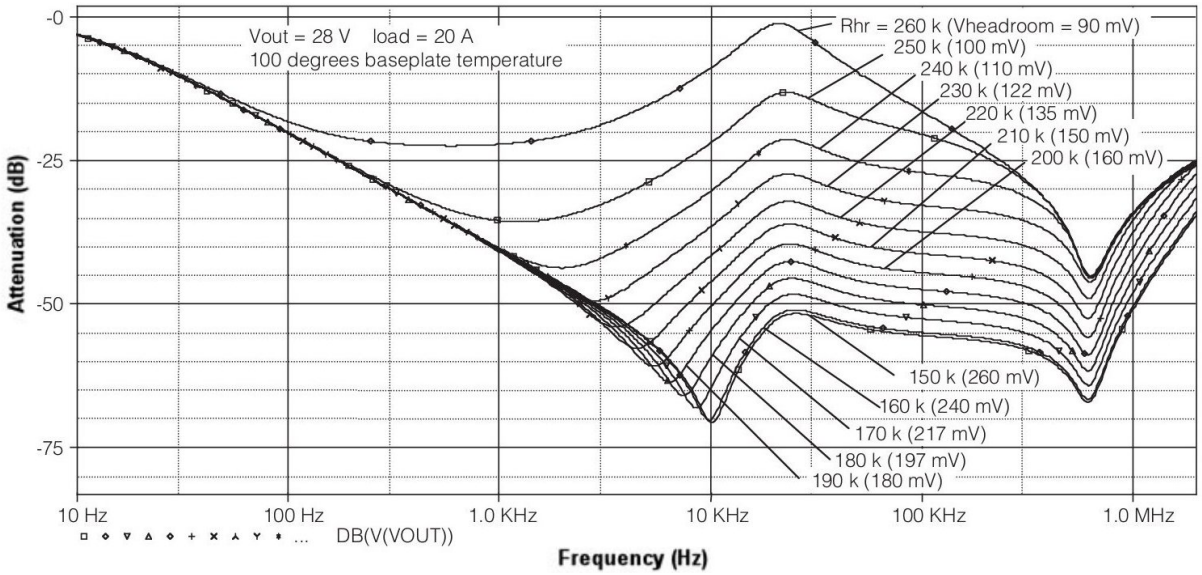

Figure 3.3: The resistor RHR sets the headroom voltage. A higher headroom wastes more power, but can dramatically reduce the noise on the output.

The last component is the headroom capacitor, designated CHR in Vicor documents and C7 in Figure 3.1. This capacitor improves low frequency response by an order of magnitude up to 1kHz, as shown in Figure 3.4. It also improves the response between 10kHz and 100kHz. The value is nominally 100 µF, but can be dropped to 47 µF when capacitor size is constrained. Note that the voltage on the VREF pin is on the order of the output voltage; capacitors **must** have sufficient voltage ratings, or they will be destroyed immediately upon testing.

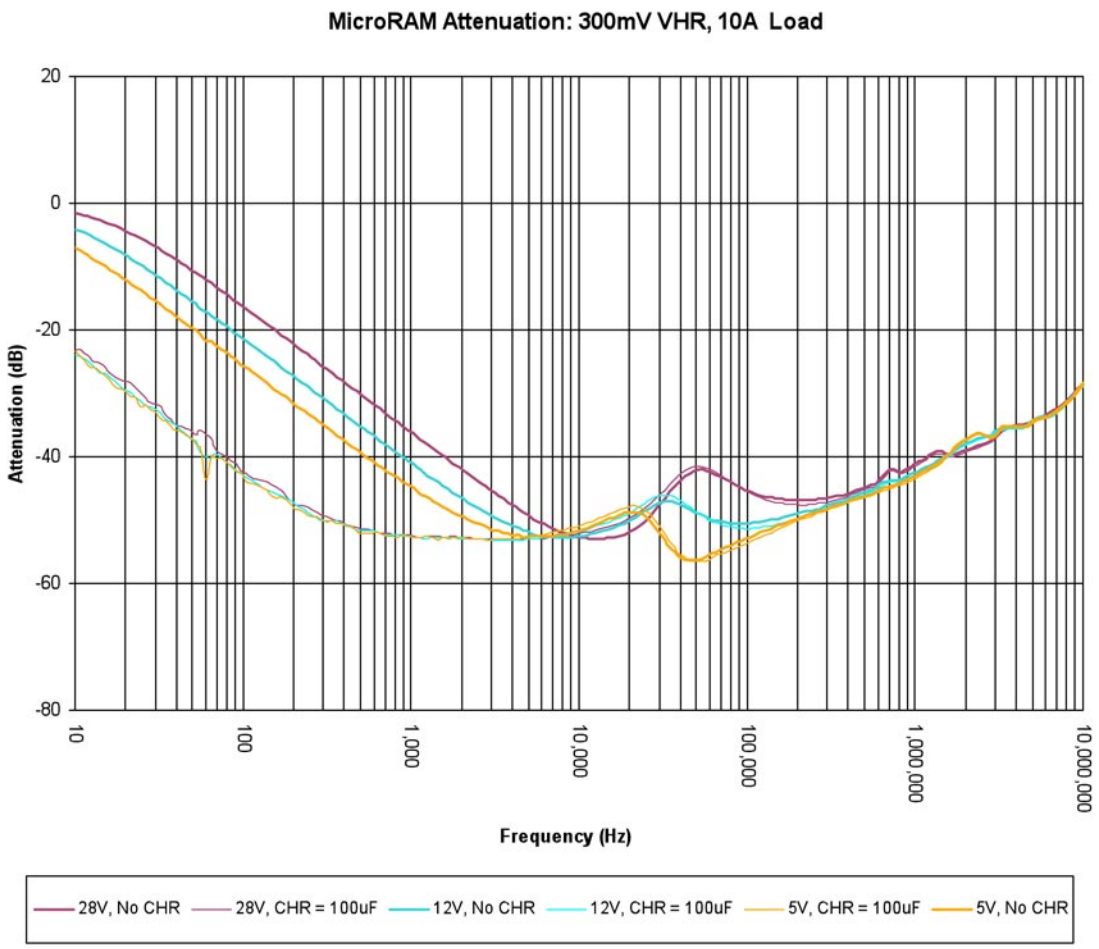

Figure 3.4: The CHR capacitor, connected between the VREF and VOUT- pins on the MicroRAM module, is especially important if low frequency noise is present in the system.

3.2.2 DC-DC Type II: Bipolar Bus Voltage

In addition to the high-power positive voltage rails, the UV-VIS EPS provides a bipolar pair of voltages for applications requiring a negative voltage. While most negative voltages are accompanied by their positive counterpart – hence the bipolar rail design – the voltages are fully configurable. The EPS design nominally produces ±15V, but can be changed to yield a third main rail and an independent negative rail.

As in the previous circuit, the bipolar voltages are generated using isolated DC-DC converters from Vicor. These are Micro converters, similar in design to the Mini's but smaller and with lower

output power. Because the converters are isolated, one can be connected in reverse at the output, as shown in Figure 3.5. In this way, two identical converters referenced to a common ground generate a bipolar pair. As in the previous section, U1 and U2 designate the converters, which are accompanied by decoupling capacitors C1 through C8, resistors R3 through R6, and LEDs on the PC pins. The output voltages are trimmed up by R7 and R8.

Because the two rails source less power than the main rails, and also to save space, the output ripple is mitigated using linear regulators instead of the microRAM modules. U3 is an LT1764A positive regulator and U4 is a LT1185 negative regulator, both from Linear Technologies. Each requires input and output capacitors, designated by C9 through C15. The resistors R10 through R13 set the output voltages. Finally, J1 through J6 are solderable jumpers, allowing the linear regulator stages to be bypassed.

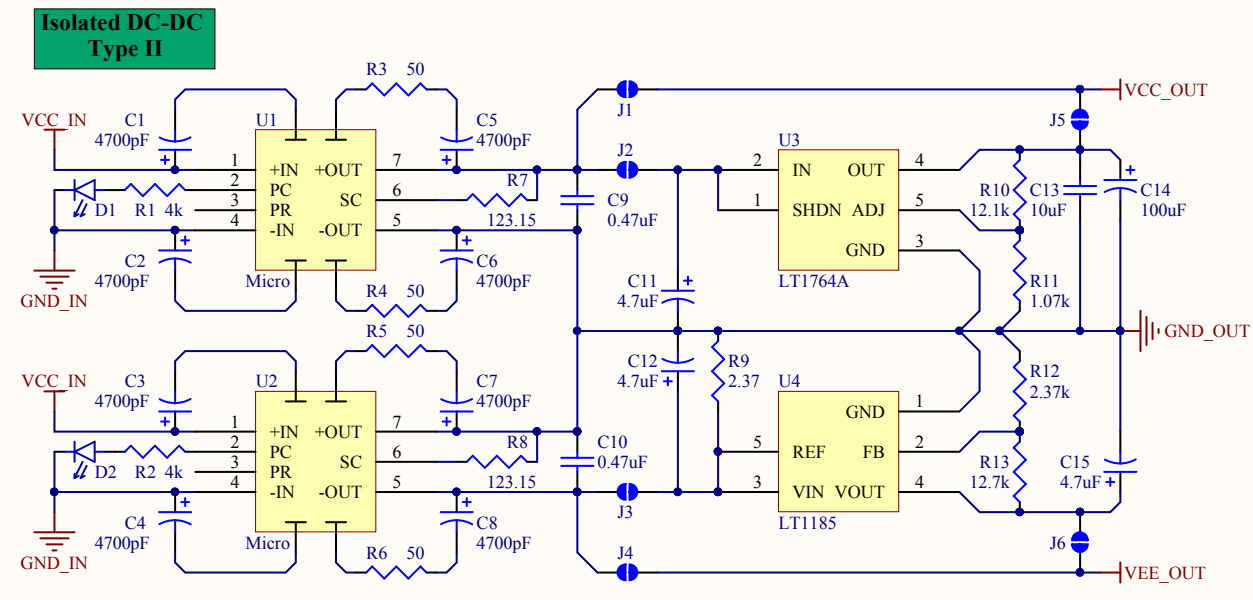

Figure 3.5: For the bipolar voltage rails, identical DC-DC converters are used together with one connected in reverse. The outputs are cleaned using positive and negative linear regulators.

Since the Micro DC-DC converters are so similar to the Mini converters used for the main rails, much of the design work for this circuit is based on the linear regulators. First, the voltage

must be set appropriately. For the LT1764A [25], the resistor divider values are defined by:

$$R10 = R11\left(\frac{V_{OUT}}{1.21\text{V}} - 1\right) \tag{3.2}$$

For the LT1185 [24], the resistors are defined by:

$$R13 = R12\left(\frac{V_{OUT}}{2.37\text{V}} - 1\right) \tag{3.3}$$

The values in Figure 3.5 generate ±15V. The linear regulators have dropout voltages of up to 500mV for the LT1764A and up to 1V for the LT1185. To accommodate these, the Micro brick outputs are trimmed up using the following relation, where V_{NOM} is the factory trimmed output voltage and $V_{OUT} = V_{NOM} + 1$.

$$R7 = R8 = \frac{(V_{OUT} - 1.23)V_{NOM}}{V_{OUT} - V_{NOM}} \times 1\text{k}\Omega \tag{3.4}$$

Another major consideration is the selection of input and output capacitors. Since both the LT1764A and LT1185 are linear regulators, component selection is fairly straightforward. Neither regulator has strict input capacitor requirements, so a bulk capacitor between 1 µF and 10 µF can be used just for bypassing. The UV-VIS EPS uses a 4.7 µF tantalum capacitor for all of the inputs. Aluminum electrolytic capacitors, which can fail at near-vacuum pressure, are strictly avoided as a safety precaution.

The output capacitors are more important, because they affect the regulator's stability. For the LT1764A, lower voltages require an equivalent series resistance (ESR) on the order of 1Ω, though for 3.3V and 5V outputs the bulk capacitance is the driving requirement. The LT1185 specifies a range of about 0.1Ω to 1Ω. For both, at least one tantalum output capacitor is recommended. The LT1185 circuit uses the same 4.7 µF capacitor as the input for simplicity. The LT1764A benefits from a much larger bulk capacitance, so a 100 µF tantalum capacitor is combined with a 10 µF ceramic one (this specific configuration is recommended by the datasheet).

3.2.3 Filtering

While the outputs of the four DC-DC converters in the UV-VIS EPS are isolated, the inputs are all connected to the same DC voltage. This can cause parasitic noise from one converter to degrade the input of others. Noise is caused by switching within the converters, and may back-propogate in the form of differential or common-mode interference. This is mitigated by placing an inductive/capacitive filter before each DC-DC converter.

The filter, shown in Figure 3.6, consists of a common mode inductor or **choke** and several capacitors. The inductor passes any differential noise, but opposes common-mode noise that is generated by the converters. Effectively, it forces the supply and return currents to be equal. The four capacitors to chassis ground also help to pass stray current, with resistors in series acting as lossy elements to dissipate the associated power. The fifth capacitor, C5, helps mitigate differential noise. For applications with more physical space, inductors can be added to the positive input to further attenuate the differential mode.

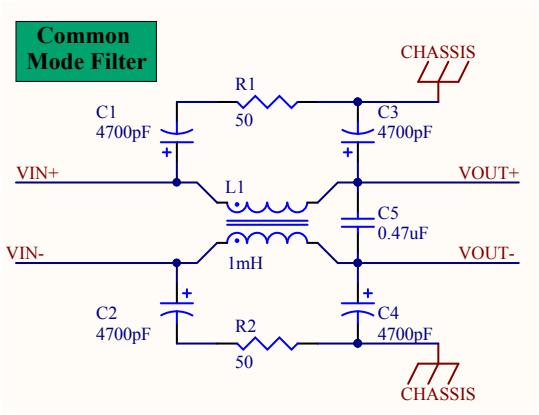

Figure 3.6: A common-mode inductors and capacitors to chassis ground help remove common-mode noise from the DC-DC converter inputs. A capacitor bypassing the two inputs mititgates some differential noise.

3.3 Computer Power Conversion

The previous DC-DC converter designs are intended for components running off of a single voltage rail. However, a key component in the UV-VIS system that requires several voltages is the computer. While some specialized computers exist that accept a single DC input, most COTS motherboards follow the ATX standard, which requires 12V, 5V, 3.3V and -12V. Rather than design a complex set of regulators for computer power, COTS power cards are available that can produce all the necessary voltages in one package.

The power card used by the UV-VIS EPS is a VME-550 from Aegis [22], shown in Figure 3.7. This card supplies four configurable voltages, with options including 12V, 5V, 3.3V and -12V. Two of the four lines are rated to 112W, while the other two are rated to 224W. In the UV-VIS system, the 12V and 5V lines are the highest power; computers draw significant current on the 3.3V line, but the power itself is still fairly low.

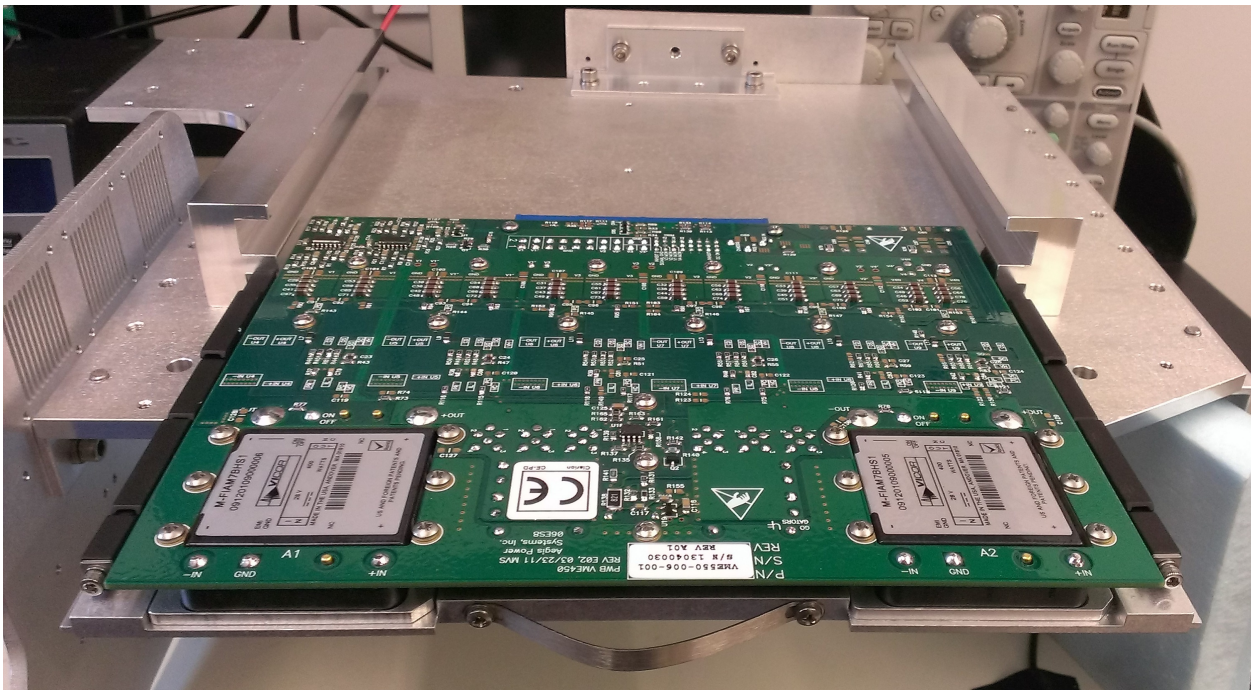

Figure 3.7: The VME-550 from Aegis produces the 12V, 5V, 3.3V and -12V voltage rails used to power the UV-VIS flight computer.

Other than providing exactly the right voltages with significant available power, the VME-550's biggest advantage is low ripple. Each line has a maximum of 50mVpp, which meets the requirements for computer power lines. In practice, the ripple is often closer to 10mVpp, making the voltage rails suitable for most other applications as well. Other benefits of the VME-550 include the wide input range – 18V to 36V – and a high efficiency of 87%. Heat is dissipated via the card's backplane; Figure 3.7 shows the card being mounted to an aluminum heat sink, which is effective for keeping the card within its operational temperature range.

3.4 Buck Converters

While the high power voltage rails use large, isolated DC-DC converters to regulate power, there are many low-power analog and digital components within the UV-VIS EPS that do not require such complex designs. In general, any system is bound to use either 5V or 3.3V (often both), and these voltages can be derived from a larger high-power rail using non-isolated conversion like buck converters or linear regulators.

The conversion scheme shown in Figure 3.8 is centered on a buck converter, with an optional low dropout linear regulator (LDO) to mitigate noise on the output. The buck converter IC is an LMZ22005, part of the Simple Switcher series by Texas Instruments. Unlike most buck ICs, which contain control electronics but require external inductors and sometimes switches, the LMZ22005 contains everything but the input capacitors (C1 through C3), output capacitors (C5 through C7), a soft start capacitor (C4) and a voltage divider (R1 and R2) to set the output voltage. The optional LDO circuit only adds two more output capacitors (C8 and C9) and another voltage-set divider (R3 and R4).

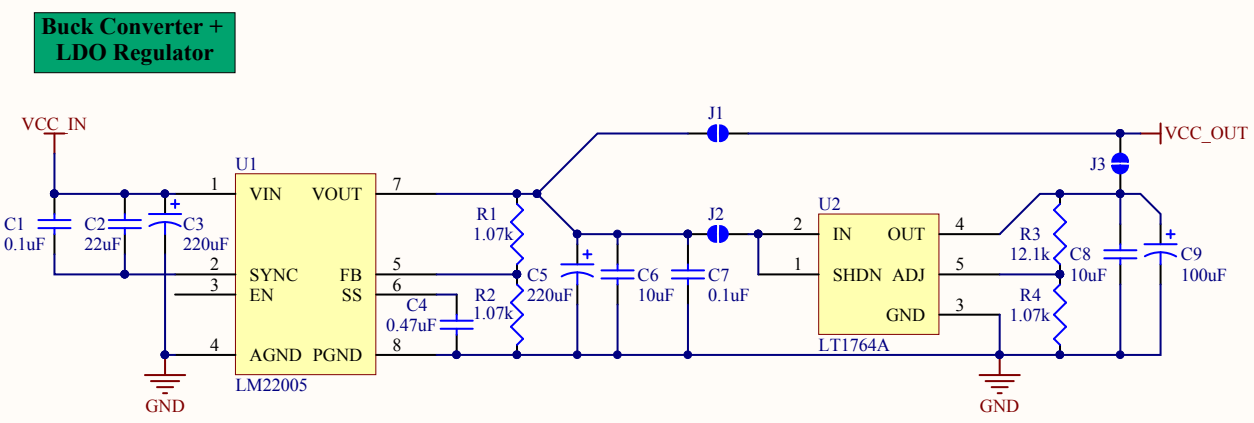

Figure 3.8: A buck converter module drops a higher voltage such as 12V down to 3.3V or 5V. The output can be filtered using a linear regulator.

The first design element in this circuit is the pair of resistor dividers, which set the output voltage. When the LDO is not being used, the output of the buck converter can be set directly to 5V or 3.3V. However when it is in use, the buck must output above the dropout voltage. The resistor values in Table 3.1 result in a 6V and 4.3V output when the LDO is in use. Note that the general voltage set equations are $R_2 = R1\,(1.25V_{out} - 1)$ for the buck converter, and $R_2 = R1\,(0.826V_{out} - 1)$ for the LDO.

Table 3.1: Resistor Values for Buck/LDO Circuit

Configuration	**R1**	**R2**	**R3**	**R4**
5V with LDO	6.81kΩ	1.07kΩ	3.32kΩ	1.07kΩ
5V w/out LDO	5.62kΩ	1.07kΩ	–	–
3.3V with LDO	4.64kΩ	1.07kΩ	1.82kΩ	1.07kΩ
3.3V w/out LDO	3.32kΩ	1.07kΩ	–	–

The LMZ22005 has an input range of 6-20V and an output range of 0.8-6V. The typical application is conversion from 12V to 5V or 3.3V. The robust surface mount package, which has a large grounding pad and heat sink as shown in Figure 3.9, enables up to 5A output current. The

grounding pad, combined with an efficiency of about 90%, keeps the package from overheating. These characteristics make the LMZ22005 ideal for powering many small components on a 5V or 3.3V bus; its 5A output means it can handle numerous loads, and having so much overhead keeps a system easily extensible. The simple design also makes the converter easy to drop into new or existing designs without adding too many components.

An important consideration in converter design is the noise and ripple present on the output. Especially when powering sensitive analog circuits, noise can have a large impact. Figure 3.9 shows a sample plot of the ripple for a 12V to 3.3V design. Even at high frequencies, where switching regulators usually produce the most noise, the LMZ22005 does not reach 10mVpp. This is superior to most buck converters, another reason this chip is so useful as a bus converter. The low ripple also means the LDO in Figure 3.8 is probably not necessary, unless the circuit is repurposed to power more sensitive circuits in future applications.

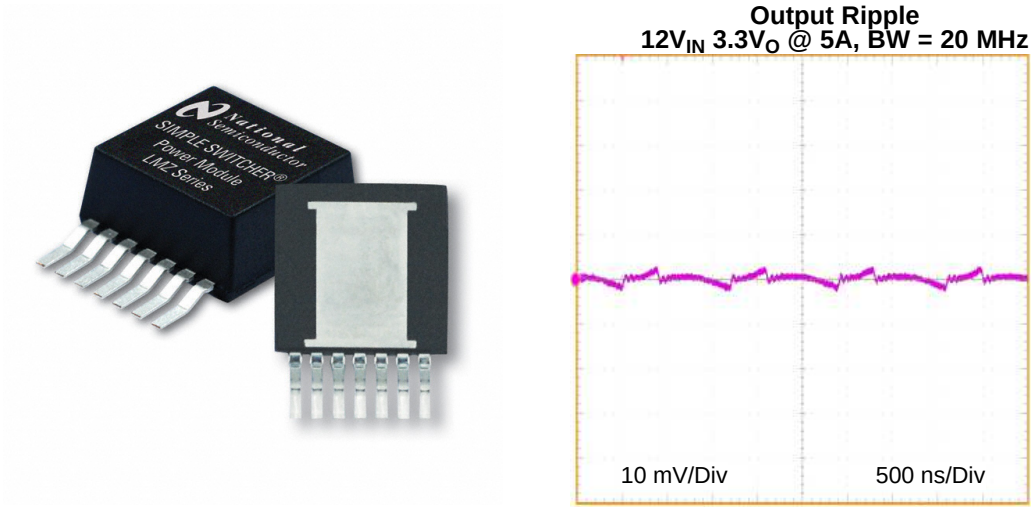

Figure 3.9: The LMZ22005, pictured at left, is capable of outputting ripple on the order of 10mV, even at full current capacity.

When designing voltage regulator circuits, the choice of input and output capacitors can be quite time consuming. One of the goals in defining circuits for general use is to mitigate this process. The capacitors for the LT1764A were discussed in Section 3.2. For the LMZ22005, a large

amount of bulk capacitance is required on the input to mitigate incoming ripple. A 22 µF ceramic capacitor is recommended for bypassing, and a higher ESR tantalum capacitor is used to damp out any resonant noise. This second capacitance can be implemented using several 47 µF capacitors in parallel; these are the largest tantalum capacitors that are rated for 16V without becoming too large for the EPS. The output requires more than 200 µF bulk capacitance. Because the voltage rating can be 6V or 10V, it is possible to implement a 220 µF tantalum capacitor rather than several smaller ones. The 10 µF and 0.1 µF ceramic capacitors double as input capacitors to the LT1764A and high-frequency bypass.

Chapter 4

Power Switching

Next to the conversion of power, being able to switch lines on and off is the most important function of a power system. In human-controlled applications, switching is simple; in digital applications, however, the most difficult design task is in converting a logic signal into an actual switching event. This chapter will cover the control circuitry that governs switches in the UV-VIS EPS. Focus is given to MOSFETs, which are solid state devices that require a complex design as compared to relays, but offer clean, small-profile power switching.

4.1 MOSFET Theory

Switching mechanisms can be divided into electro-mechanical and solid state devices. Ignoring human interface switches, the most common electro-mechanical devices are relays. While relays are simpler to design than many solid state switches, they are large and require magnetics and moving parts. In compact applications, where space is at a premium and magnetic noise can affect neighboring components, relays are not desirable. In contrast, transistors and other solid state devices can handle large amounts of power in small surface mount packages, and do not cause any interference. In the UV-VIS EPS, transistors are used exclusively for switching power lines.

Amongst transistors, there are many topologies that span a wide range of operating conditions. For high power or high current applications, MOSFETs are a common choice. MOSFETs are three-terminal devices with a **gate**, **source** and **drain** pin. Based on the gate voltage relative to the source and drain pins, the MOSFET may be in one of three states: off, resistive and on.

The intermediate resistive state is not useful in power control, so the goal of the switching circuit design is to place the MOSFET in the on or off state.

Like all transistors, MOSFETs come in two types: NPN or N-type, and PNP or P-type. The type of doping dictates the direction of current flow – drain-to-source for N-type FETs, and source-to-drain for P-type. It also determines the necessary gate voltage to turn the MOSFET on. For N-type FETs, a positive gate-to-source voltage is required. P-type MOSFETs, in which current flows the opposite direction, need a negative gate-to-source voltage to turn on. In practice, these characteristics make N-type and P-type FETs suitable for low-side and high-side switching, respectably. However, as Figure 4.1 shows, the other two permutations are possible as well.

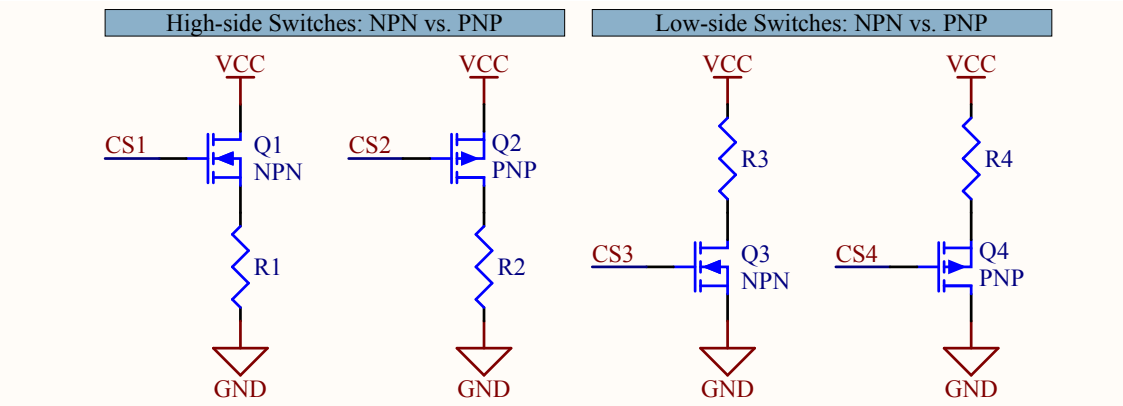

Figure 4.1: There are four switching configurations possible with MOSFETs. Both NPN and PNP FETs can act as high-side switches, where the load is connected directly to ground. Similarly, both can switch on the load side, where the load is connected to the source.

All four switching configurations in Figure 4.1 are valid, but which is the most preferable? The most important consideration is safety; in a centralized system distributing power to many loads, low-side switching means that there are live voltages on every positive connection, even when the loads are off. This is hazardous, as shorts to chassis ground become much more likely. High-side switching is preferred, because when a load is off its only connection is to ground. The other consideration is on-resistance. P-type MOSFETs are many times more resistive than N-types,

making them less efficient. Thus, the best design is an N-type high-side topology.

Using an N-type MOSFET as a high-side switch has several complications. First, the gate-to-source voltage must be positive, meaning the gate voltage must be several volts higher than VCC of the rail being switched. This is further complicated by the fact that, while turning on, the source voltage **is not constant**. Instead, it rises from 0V to VCC as the FET turns on. To prevent the gate-to-source voltage (VGS) from being **too** high during this time, a Zener diode is placed from the source to the gate to clamp VGS.

In the UV-VIS EPS, an AUIRFS4310 N-type MOSFET from International Rectifier is used. This FET can withstand voltages up to 100V, a maximum current of 75A, and a maximum VGS of 20V. The threshold voltage is 4V, and the on resistance only 5.6mΩ. The MOSFET is accompanied by a MMBZ5241BS Zener diode from Diodes Inc., which has an 11V Zener voltage. This prevents VGS from coming near the 20V limit.

4.2 MOSFET Control

Having settled on the high-side, N-type switch topology, control circuitry is necessary to produce suitably high gate voltages to switch 12V and 24V loads. The following four circuits all use N-type MOSFET drivers to do so. Each circuit allows a microcontroller with 3.3V or 5V logic to control much higher voltages.

4.2.1 MOSFET Type-I: Single Channel, Positive Switching

The first type of MOSFET control circuit, shown in Figure 4.2, is used to switch a single positive voltage rail, denoted by VCC. The rail first passes through a shunt resistor R1, then passes through an N-type MOSFET Q1. The output voltage is denoted VCC1, indicating it has the same voltage as VCC but is now a distinct, separately controlled rail. The control signal itself is designated CS1, and is typically either 3.3V or 5V logic. Finally, a Zener diode D1 offers protection for the MOSFET, and a tantalum capacitor C1 protects against noise on the voltage rail.

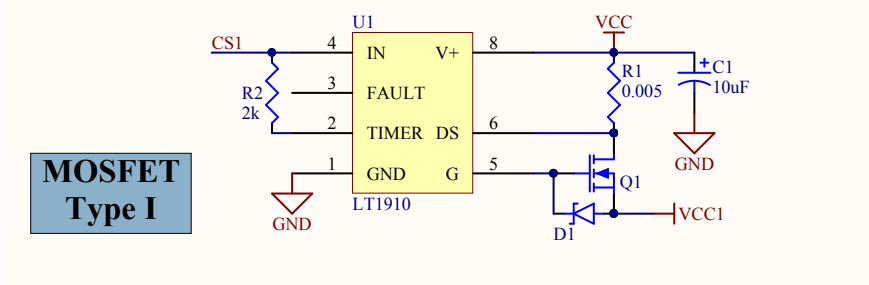

Figure 4.2: The LT1910 is used to control a single voltage rail up to 60V. The control logic is 3.3V and 5V compatible.

The control IC is an LT1910 from Linear Technology. This is an N-type MOSFET driver, intended for high side switching applications. It contains a charge pump that boosts the input signal by several volts; the relationship between the resulting gate voltage and the voltage being switched is shown in Figure 4.3. This plot indicates that the LT1910 is suitable for switching any voltage above 8V.

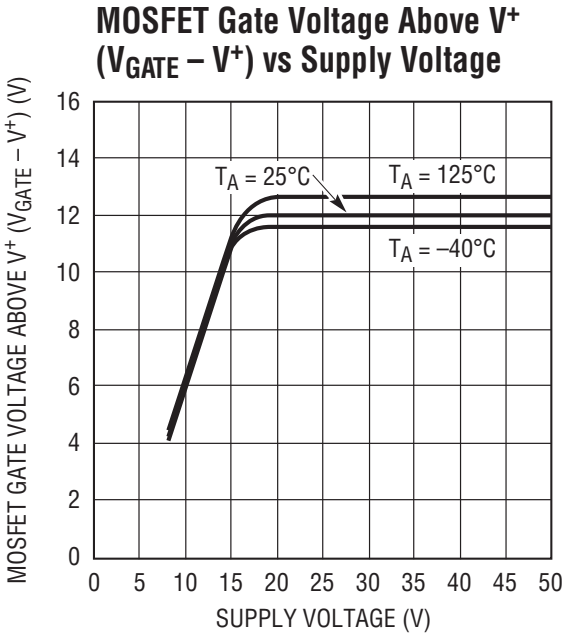

Figure 4.3: The LT1910 contains a charge pump that raises the gate voltage high enough above the supply voltage to turn an N-type MOSFET on.

The LT1910 also has built in overcurrent protection. The shunt resistor R1 is used to sense the current flowing through the MOSFET. Using a Kelvin sense connection, the IC detects the voltage both before and after the resistor, then compares the difference to a 50mV reference. If the difference surpasses this reference voltage, the MOSFET is quickly turned off. Using this relation, a current limit can be chosen by setting the value of R1.

$$R = \frac{0.050}{I_{\text{limit}}} \tag{4.1}$$

For example, choosing a 5A current limit results in a 10mΩ resistor. Note that, because the resistance is so small, trace resistance **must** be considered in the physical layout. If the traces are very thin or very long (or both), the effective resistance will increase, dropping the current limit. This can result in unintended shutoff at low currents. If current limiting is unneeded, R1 can be omitted and the DS pin tied to supply.

The Type-I circuit is a critical building block in the control system design. It offers a very simple digital interface, has built in protection, and is only limited in the current it can control by the MOSFET selection. The circuit is also very flexible; it works for most voltage rails in the system without a need to change any component values. This makes it an ideal pre-designed circuit block that is reliable both in the UV-VIS design as well as future designs.

4.2.2 MOSFET Type-II: Single Channel, Negative Switching

Because it powers an ATX computer, the UV-VIS EPS is required to switch a -12V rail. Designing a negative voltage switch requires additional considerations, because the switch is now on the low side instead of the high side. While the same driving circuitry can be used, the control signal must be referenced to the negative voltage instead of ground.

The Type II MOSFET circuit, shown in Figure 4.4, uses the LT1910 much like the Type I circuit. The chip sees GND as its positive supply, and the negative VEE as its return. The MOSFET, Q1, is placed with its source connected to VEE because of the direction of current flow. Notable differences include the lack of a shunt resistor, and the addition of an isolated logic circuit.

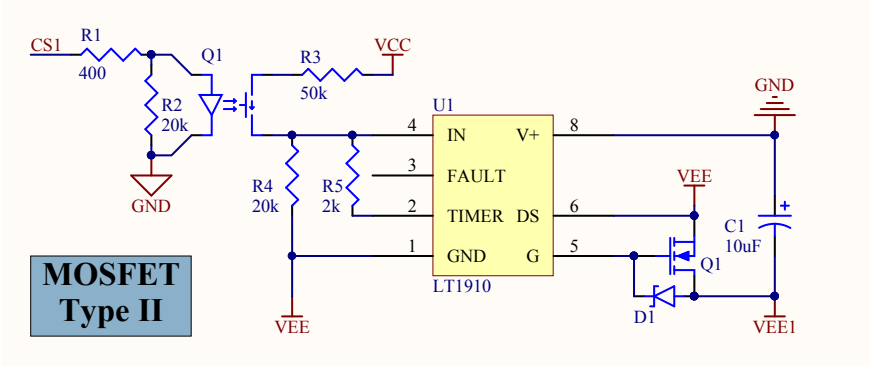

Figure 4.4: A negative voltage rail can be controlled by powering the LT1910 from ground to VEE. The switching logic now must be referenced to VEE for the switch to operate.

The shunt resistor is omitted because the LT1910 is built to sense current relative to its positive supply voltage. When this voltage is not the same as the one being switched, the sense circuit will not function properly. It **is** possible to place a resistor between the load and GND. However, the load cannot share GND with other voltage rails, which is the case for the ATX motherboard. Because of this, and the very low current on the -12V line, the current limiting functionality can be dropped.

The other major difference between the Type I and II circuits is in the logic input. For the negative switch, the LT1910 sees the input relative to VEE. This causes logic low (ideally 0V relative to GND) to appear as a positive voltage. A secondary concern is that the input voltage may surpass the maximum voltage rating. For sufficiently small values of VEE, both issues can be mitigated with a simple voltage divider. However, as VEE grows large, it becomes impossible to distinguish logic high and low signals. This is due to variability in the logic thresholds defined by the chip, as shown in Figure 4.5.

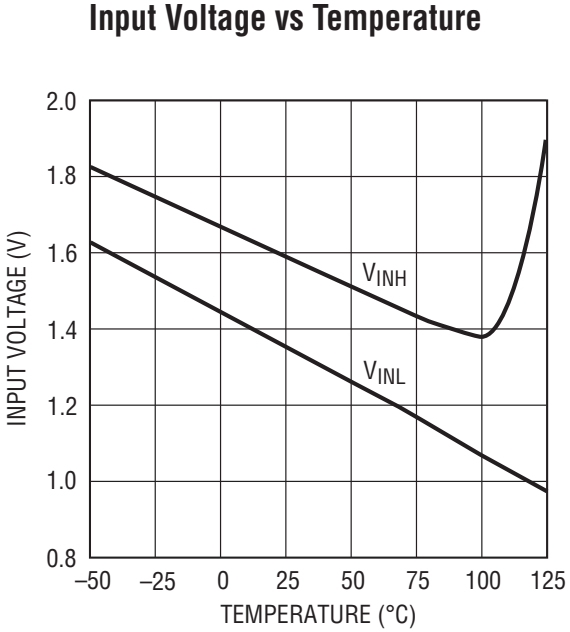

Figure 4.5: The LT1910 can nominally accept inputs between 2V and 15V. The exact on/off threshold voltages are temperature dependent; the designer must ensure that both logic high and low signals remain out of the V_{INL} to V_{INH} range to avoid undefined behavior.

Take for example the case $V_{\text{EE}} = -12\text{V}$ and $V_{\text{CS1}} = 5\text{V}$. The effective logic signals are now 17V and 12V. A voltage divider can be constructed between the two using $R_1 = 90\text{k}\Omega$ and $R_2 = 10\text{k}\Omega$, reducing the signals to 1.7V and 1.2V. At 25°C, these signals effectively control the switch. However, as the temperature rises or falls, one of the signals drops into an undetermined state. There are no values of R_1 and R_2 that yield a suitably safe control scheme; thus, a new logic scheme must be used.

Figure 4.4 shows a solid state relay (SSR) Q2 being used to shift the logic levels seen by the LT1910. This type of circuit is described fully in Section 4.3. Here, it is sufficient to note that, when CS1 is high, the voltage divider between VCC and VEE yields a 4.85V signal. When CS1 is low, the connection with GND is severed, and R4 pulls the input to 0V relative to VEE.

Creating a negative voltage switch is not necessary in many power systems. However, when one is needed, it is preferable to use the same hardware as the positive switches use. The Type II

circuit keeps the LT1910 and the HEXFET power MOSFET used before. The only new component is an SSR, which is another building-block circuit described in this thesis. Overall, a potentially difficult design is mitigated by the Type II circuit.

4.2.3 MOSFET Type-III: Three Channel, Low Voltage

Previous MOSFET circuits have proven useful for voltage rails 8V and above. However, 5V and 3.3V are very common in power system design, and must have their own means of being switched. Fortunately, lower voltages are actually easier for MOSFETs to switch, because the gate-to-source voltage can be lower. Figure 4.6 shows the Type III circuit, which relies on the LTC1163 from Linear to switch three MOSFETs. Each switch has a dedicated logic line; CS1 controls Q1, CS2 controls Q2 and CS3 controls Q3. Other than the FETs themselves, this circuit requires no external components.

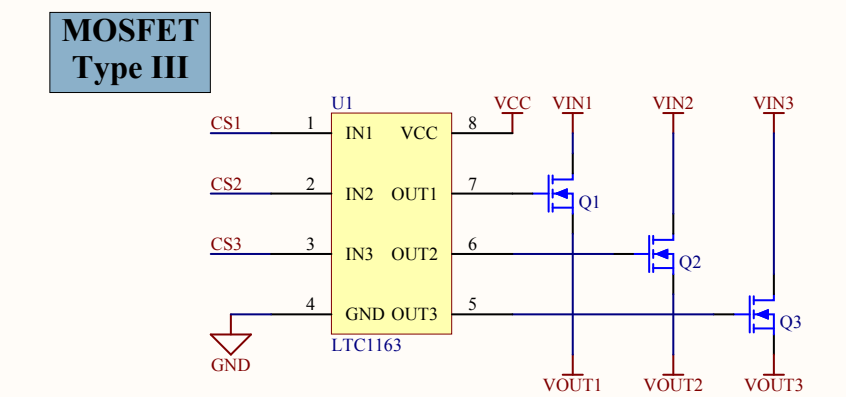

Figure 4.6: The LT1163 is a simple three-channel MOSFET driver for 5V or less. Because the inputs are separate, different voltages can be switched on each channel.

The LTC1163 is similar to the LT1910, in that it uses charge pumps to boost the supply voltage to turn on an N-type MOSFET. Unlike the LT1910, it runs off of standard 3.3V or 5V logic levels. In this application the supply is 5V, meaning the gate drive for each switch is roughly 14V (given by Figure 4.7). This makes the gate-to-source voltage 9V for 5V rails, and 10.7V for 3.3V rails. Thus, any combination of the two voltage rails can be switched using $V_{CC} = V_{CS} = 5V$.

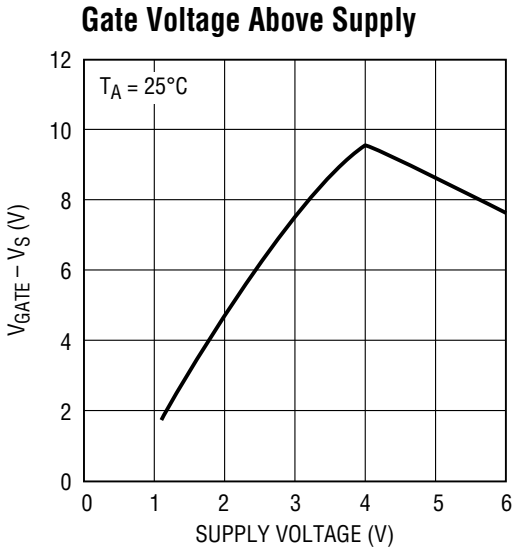

Figure 4.7: The LT1C1163 uses a charge pump to boost the input signal by roughly 8-9V for typical applications. This voltage, applied to the gate of an N-type MOSFET, fully saturates it.

It should be noted that there are no Zener clamp diodes as there were for higher voltages switches. This is because the gate-to-source voltage never exceeds the limit of the MOSFET, which is 20V. If MOSFETs with a lower V_{GS} are used, Zener diodes may be necessary to prevent damage.

The Type III circuit is only used in the UV-VIS EPS to switch computer power rails. However, the LTC1163 can be used for much more extensive mixed 3.3V/5V applications. The very simple design, which needs few external components, makes the circuit very easy to drop into a new or existing design.

4.2.4 MOSFET Type-IV: Four Channel

The final MOSFET circuit is simply an extension of the Type I circuit. It uses an LT1161, which is the quad version of the LT1910. Figure 4.8 shows how the LT1161 is used to derive four switched voltage rails, VCC1 through VCC4, from a single supply voltage VCC. As seen before, shunt resistors R1 through R4 measure the current on each rail, and diodes D1 through D4 protect the MOSFETs from overvoltage during turn on.

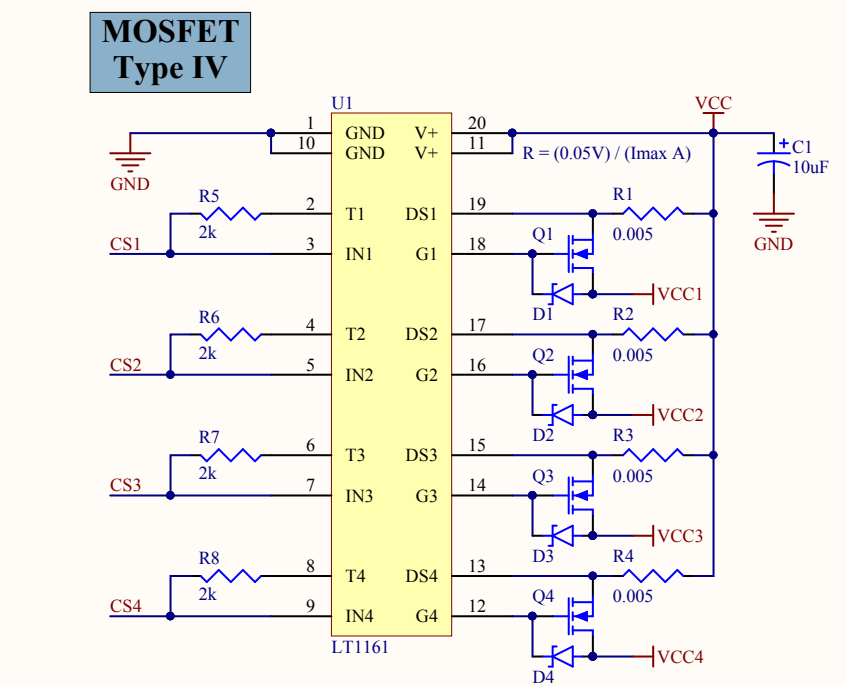

Figure 4.8: The LT1161, a quad version of the LT1910, is used to derive four independently switched rails from a single source.

The Type IV circuit is very useful in systems that widely use a single voltage. Rather than duplicate the Type I circuit several times, a single IC can be used to switch up to four rails. This reduces the number of parts required, and facilitates board layout as well.

4.3 Isolated Switching

While ICs like the LT1910 and LTC1163 used in the MOSFET circuits can interface directly with logic signals from a microcontroller, it is not always so easy to convert such signals to actual switching events. In some cases, this is because the rail being switched has a different "ground" than the logic signals. In others, the logic levels may be incompatible with the circuit and require shifting. Finally, it is also desirable sometimes to isolate digital and power grounds completely.

In all of these cases, a solid state relay (SSR) can be used to transfer the logic signals into the switching circuit, while providing total isolation between the two. Typical SSR's are opto-isolators, which combines an LED and a light-sensitive transistor gate (or gates). When a logic signal turns

on the LED, the gate turns on as well, allowing current to pass. When the LED is off, the gate is high-impedance. As shown in Figure 4.9, this behavior is used to convert a logic signal – CS1 relative to GND1 – into a new signal CS2 relative to GND2. The voltage divider created by R3 and R4 can be tuned to output the desired voltage between VCC and GND2.

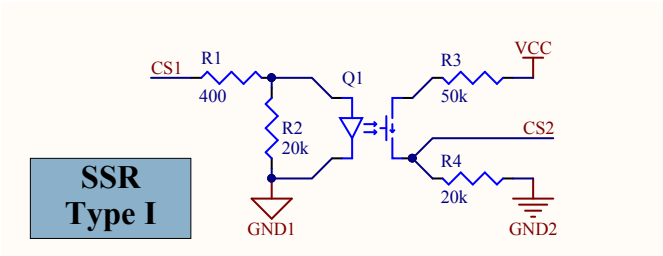

Figure 4.9: A solid state relay is a simple way to change the reference "ground" of a control signal in mixed-ground systems.

There are several resistors in the SSR circuit. R1 is a current limiting resistor, necessary to keep the LED in the SSR from burning out. For a typical 5V application, a 400Ω resistor limits current to 12.5 mA. The value can be tuned to match the input voltage and the current limit of the selected SSR. R2 is a pulldown resistor; it ensures the SSR stays off when no signal is applied. R3 and R4 form a voltage divider that selects the value of CS2. R4 doubles as a pulldown resistor, and should not be omitted. If the desired logic high value is VCC, then R3 can be left out.

The SSR used in the UV-VIS EPS is a G3VM-352J from Omron. It is an eight-pin package that contains two completely isolated SSR circuits. These can, however, run off of a single logical input in order to synchronize two outputs. This behavior is shown in Figure 4.10, which uses the same circuit elements as the previous design. In this case, the two outputs CS2 can control two circuits in tandem; this is the control scheme used for the ±15V rails in the UV-VIS EPS, discussed in Section 3.2.

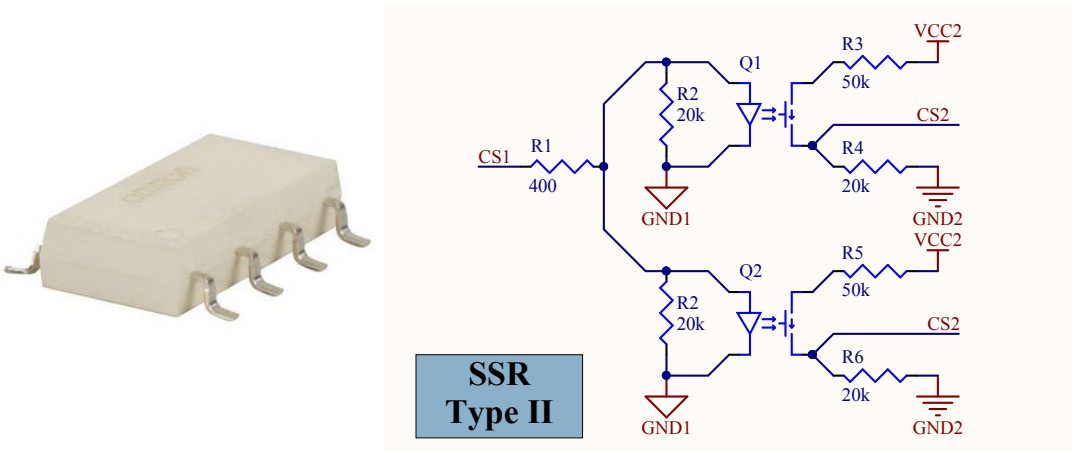

Figure 4.10: The Omron G3VM-352J dual SSR can be used to convert a single logic signal to two isolated, synchronized signals.

The use of opto-isolated SSRs for isolated switching supplements the power MOSFET designs in the previous sections. While the MOSFET circuits provide the mechanism for driving various loads in the UV-VIS system, the SSRs allow digital logic commands to reach these circuits freely, regardless of grounding. The ability to drop this circuit into a design allows the system grounding scheme to focus on power and noise concerns, instead of interfaces between circuits.

Chapter 5

Sensing

A simple EPS can get by with just the regulation and control blocks. However, it is desirable to have housekeeping data for the system, in order to determine either during or after flight whether the system is running nominally. This data can also be used by onboard logic to mitigate errors as they occur. The most common housekeeping data are voltage and current measurements of main power lines. [29].

5.1 Current Sensors

Current, unlike voltage, is difficult to measure. The most basic form of current sensing consists of placing a very small resistor in series, then measuring the voltage drop over it. Such a resistor is called a **current shunt**, and appears in the MOSFET circuits in Section 4.2. The current is found from Ohm's law, $I = V/R$. While this is a useful method in simple circuits, it is not very robust, requires breaking the circuit, and also requires that voltage be measured at two different points. More sophisticated current sensors use the induced magnetic field of the current as a measurement source.

The ACS712 from Allegro is a very common chip that uses the Hall effect to sense current. The Hall effect is the presence of a voltage difference on two sides of a semiconductor when is is subject to a magnetic field perpendicular the flow of current. Thus, the ACS712 is a **transducer**, converting current to voltage without the need for a current shunt.

The basic ACS712 design circuit is shown in Figure 5.1, along with an image of the IC itself.

The first four pins of the IC simply allow the voltage rail to pass through the sensor; VIN and VOUT have the exact same voltage, and positive current is measured as flowing from VIN to VOUT. The sensor is intended to run off of $V_{CC} = 5$V. The supply should be decoupled by C2, which is typically a ceramic 0.1 µF capacitor intended to remove high-frequency noise. C1 is a filter capacitor whose value can be adjusted to improve either noise or response time.

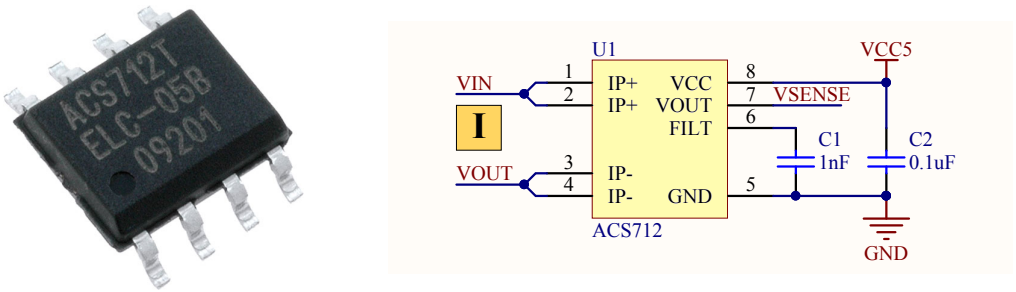

Figure 5.1: The Allegro ACS712 current sensor is a small, 8-pin IC that converts a current measurement to an analog voltage.

The output VOUT is directly proportional to current flow. Three models of the ACS712, optimized for ±5A, ±20A and ±30A ranges, have sensitivities of 185, 100 and 66 mV/A, respectively. The UV-VIS EPS uses the ±5V variant, which yields the highest sensitivity. The output is also dependent upon the value of C1. As Figure 5.2 shows, the filter capacitor drives response time and noise. The UV-VIS EPS mistakenly used a 1nF capacitor, which is ideal for fast data rates. In a slower system that is more concerned with accuracy, however, 100nF $\leq C_F \leq$ 1 µF is an optimal range. Future designs should consider using this range for C1.

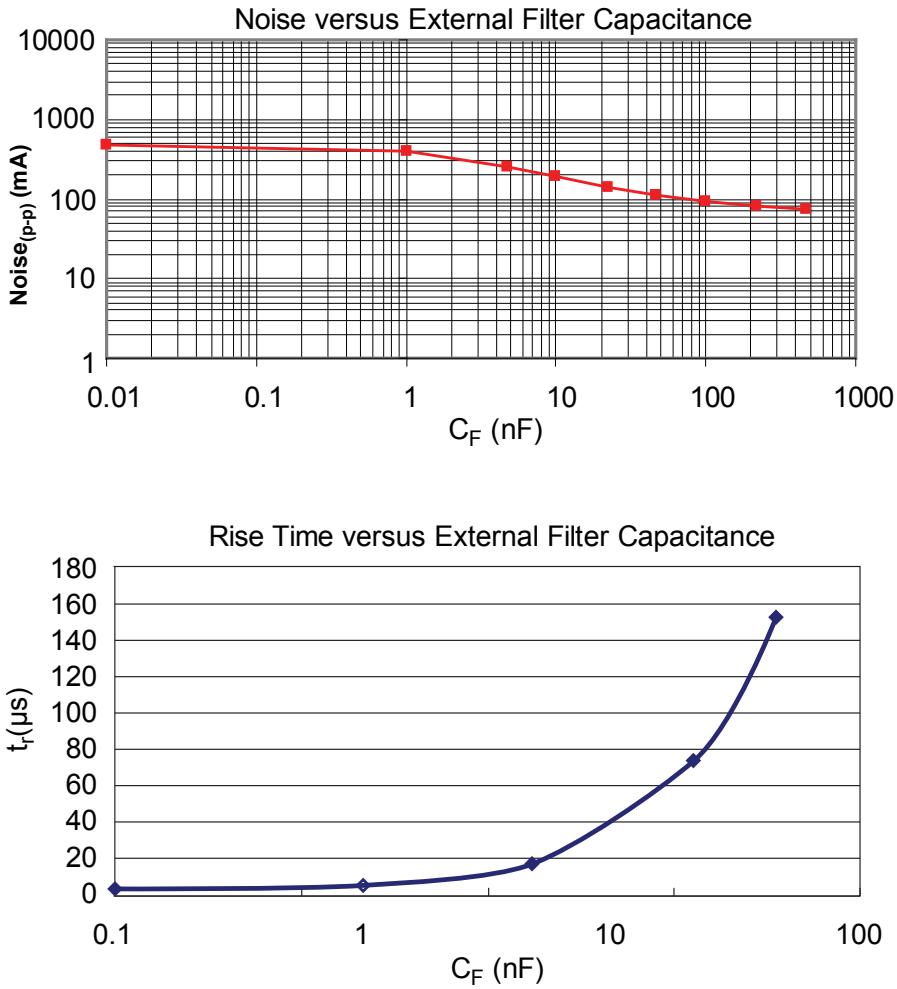

Figure 5.2: The value of C1, denoted C_F, drives both the noise and transient response of the ACS712. Increased capacitance yields lower noise but higher rise time, while decreasing the capacitance yields fast transient response at the cost of higher noise.

5.2 Signal Conditioning: Op-Amps

Many sensors have internal circuitry that conditions their output so it is easily sensed by an analog-to-digital converter (ADC). However, when sensing voltages directly, this circuitry must often be designed separately. This is achieved using operational amplifiers (hereafter op-amps). While op-amp circuits can become very complex to account for a myriad of minor signal imperfections, this section will cover very basic op-amp design. Further reading is recommended in the

Texas Instruments Application Note SLOA098 [13].

The motivation for conditioning voltages comes from ADC internal design. ADCs require that input signals have a low impedance, or else accuracy and response time can be degraded by long capacitor charging times. This is discussed more fully in Section 5.3. When voltages are read directly from a voltage rail, the impedance is not guaranteed to be low. Indeed, many loads are high-impedance, or carry additional capacitance that can alter ADC performance. Thus, a circuit is required between the ADC and its inputs to ensure they meet the ADC's input requirements.

The most simple conditioning circuit is called a **voltage follower**, also known as a unity gain buffer. This circuit, shown connected to a voltage divider in Figure 5.3, simply takes a voltage at the noninverting input and provides the same voltage on the output. The output, labeled VSENSE in this application, has been isolated from the input, and now has the impedance of the op-amp instead of the original circuit.

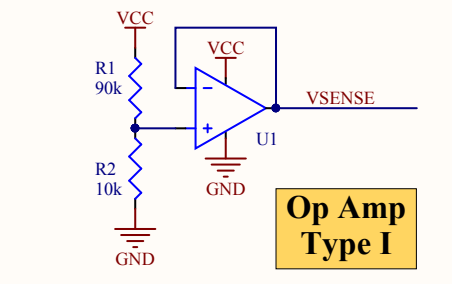

Figure 5.3: A simple voltage follower and divider circuit is used to buffer a voltage rail and scale it to the input range of an ADC.

Figure 5.3 is called a Type I circuit, as it is used to prepare a single voltage for measurement. The voltage divider created by R1 and R2 is necessary for almost all voltages, as the ADCs have a maximum input of 4.096V. In this example, VCC is divided by 10, which is suitable for higher voltage rails like 12V and 24V. A 5V rail might only be divided by a factor of 2, meaning R1 would be changed to 10kΩ.

The op-amps used in the UV-VIS EPS are either LT1884's or LT1885's from Linear Technol-

ogy. These are dual and quad op-amps, respectively, intended for precision sensing applications. They are also rail-to-rail op-amps, which means the output voltage can swing nearly as high as the positive power supply VCC and nearly as low as the negative supply VEE. The reduction in range is about 100mV on either end, though this is highly temperature and power dependent. Note that in Figure 5.3, the negative supply is GND as opposed to -VCC. Op-amps normally use a bipolar input because many circuits have negative gain and thus negative outputs. However, since the Type I circuit only measures positive voltages with no gain, it can be run in **single supply** mode. This is a boon for circuit design, because now the op-amp can use the circuit it is measuring for power supply instead of requiring dedicated voltages. It also removes the need for a negative supply, which is often unavailable in custom power systems.

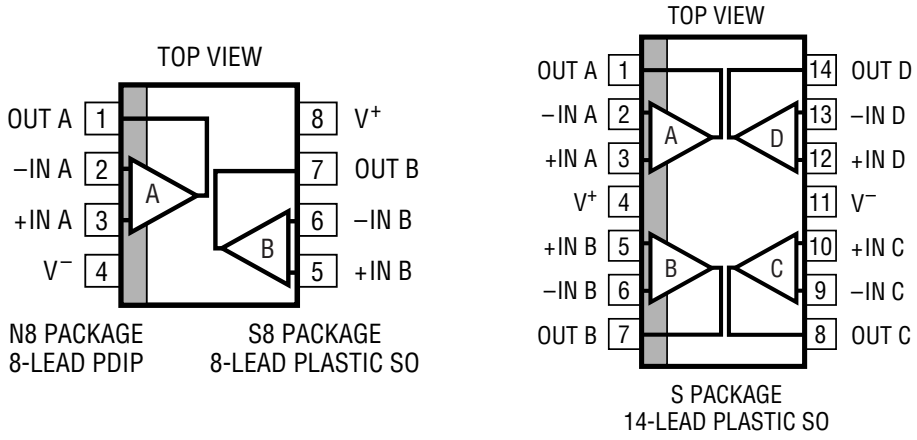

Figure 5.4: The LT1884 and LT1885 chips contain either two or four op-amps. Both packages are useful for reducing the number of components in a design, either when one circuit needs several op-amps, or when several circuits can be clustered in one location.

Some considerations must be made when using VCC and GND from the rail being measured to power the op-amp. First, the op-amp cannot output voltages within 100mV of VCC, so a voltage divider is strictly necessary for accurate measurements. Second, the noisiness of the supply can affect the output. This is typically not a problem – the LT1884 has a noise rejection of over 100dB for frequencies less than 100Hz – but very fast data rates may necessitate a cleaner supply.

The Type I op-amp circuit is suitable for measuring single voltages relative to GND, so long as GND is used by the ADC. However, a voltage rail's GND may be isolated from the ADC, meaning there is no reference point with which to make a measurement. In this case, the ADC can be run in differential mode. This requires two voltages, one scaled relative to VCC and one to GND. Figure 5.5 illustrates how, using two voltage followers and a three-stage divider, these voltages can be output with the proper impedance.

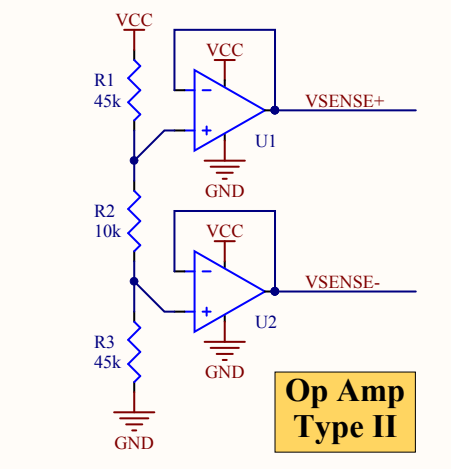

Figure 5.5: A dual voltage follower/divider can be used to condition an isolated voltage for sensing. In this case, both the signal and its reference are divided and buffered.

The Type II circuit is effectively two Type I circuits combined. VSENSE+ and VSENSE- are both derived from a voltage divider, and the range has been reduced by a factor of 10 once more. Note that the outputs are centered around VCC/2; this is to avoid getting too close to the op-amp's voltage rails. Just like VCC cannot be measured, neither can GND. Otherwise, a two resistor divider would suffice.

The final op-amp circuit used in the UV-VIS EPS is intended for sensing isolated **and** bipolar voltage rails, such as ±15V. Because there is a negative voltage VEE, the op-amps must be run in bipolar supply mode. This allows GND to be sensed directly, and VCC and VEE are measured using two Type I circuits, as shown in Figure 5.6. The use of three op-amps makes the LT1885

ideal; the bipolar rails are thus conditioned using only one chip and four resistors.

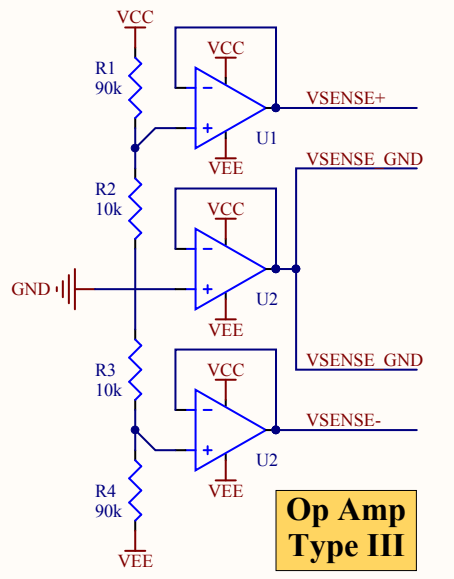

Figure 5.6: A triple voltage follower/divider conditions isolated pairs of voltages.

The Type I, II and III op-amp circuits are simple examples of signal conditioning approaches. Each is used in the UV-VIS EPS, and the simple divider-buffer approach is sufficient for many applications. More sophisticated approaches might use non-unity gain, or negative gain for sensing negative voltages. There are also many ways to improve the possible measurement speed, but these are not necessary for simple housekeeping data and can be researched separately.

5.3 Voltage Sensors: ADCs

With circuits designed for both current and voltage measurements, the final step is to convert the analog signals to digital information that can be stored or sent to a computer. This is achieved using analog-to-digital converters, or ADCs. ADCs are chips that, as the name implies, read in an analog signal and digitize it. Conceptually, this is achieved by using a comparator to match the input against a voltage reference. In practice, though, modern ADCs use a complex series of comparisons, noise filters and other methods to produce very accurate digital representations.

The ADC used by the UV-VIS EPS is the LTC1867 from Linear. This is a 16-bit ADC that

utilizes a multiplexer to provide 8 input channels. These channels can be read, in any combination, at up to 200,000 samples per second (or 200ksps). This speed is more than sufficient for basic housekeeping data, as the set of channels can be read at over 20kHz. The LTC1867 has a trimmed internal reference of 2.5V, and an output range of 4.096V. When operated in unipolar mode, the full output is utilized, and the precision of the ADC is LSB = 62.5μV.

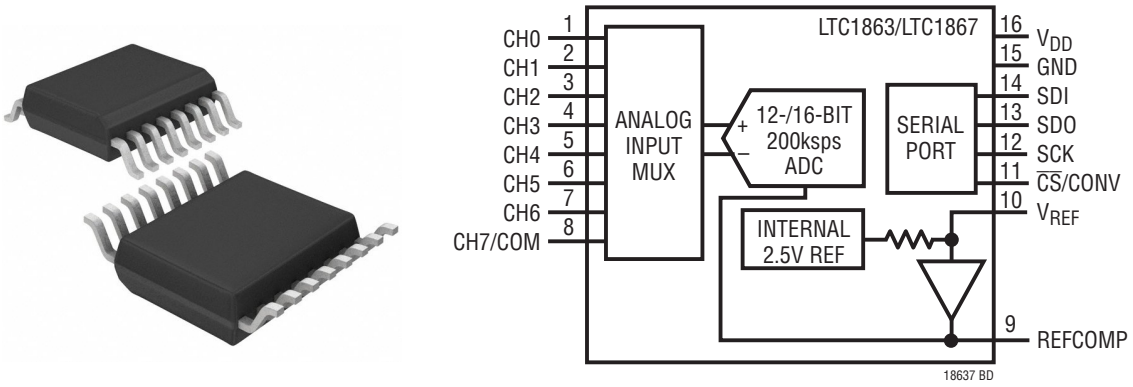

Figure 5.7: The LTC1867 (and its 12-bit counterpart) are 16-pin, 16-bit ADCs with 8 input channels and an SPI digital interface.

The LTC1867 has a simple digital interface based on the SPI bus architecture. This means it accepts commands on the SDI (slave data in) pin, and sends data on the SDO (slave data out) pin. These are the same as the MOSI and MISO (master out/in slave in/out) pins on the SPI bus. There is also a clock pin SCK and a chip select pin CS. The CS pin allows several ADCs to coexist on the same bus; each one gets its own CS, and they all share MOSI, MISO and SCK.

As shown in Figure 5.8, the chip select initializes a conversion when high. Communication is then begun when CS is brought low. A 7-bit command can be sent while data is read; in practice, the master sends two bytes, the first of which contains the command in the first 7 MSB. This command specifies which channel is to be read next and whether to use single or differential mode. Data is read in by the master, and can be converted to a voltage by multiplying the 16-bit value by the ADC precision, 62.5μV/LSB.

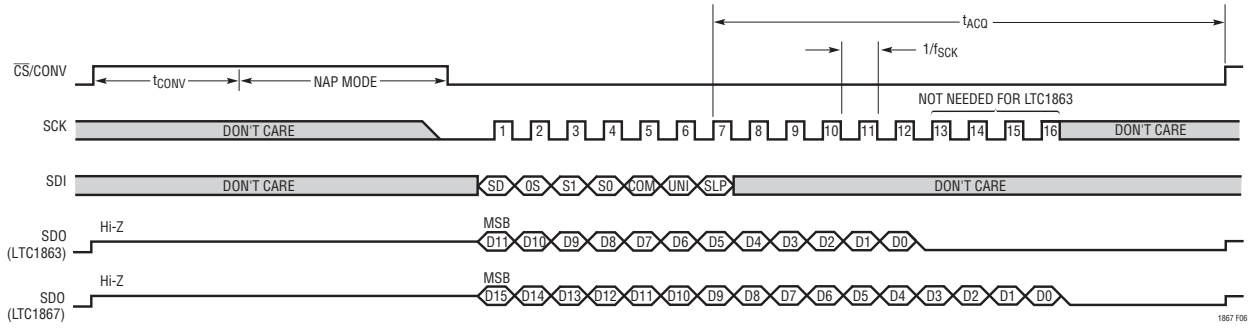

Figure 5.8: LTC1867 digital interface.

5.3.1 ADC Type I: Differential Voltage Sensor

The LTC1867 is used in much the same way regardless of its inputs. The digital interface remains constant (except for the changing CS pin), and it always boasts the same complement of decoupling capacitors C1 through C6, as shown in Figure 5.9. These three pairs of capacitors decouple the supply voltage, the reference voltage and the comparator respectively. The blending of tantalum and ceramic capacitors is recommended by the datasheet. While there is a low power version of the LTC1867 that can run on 3.3V, the normal chip uses $V_{CC} = 5V$.

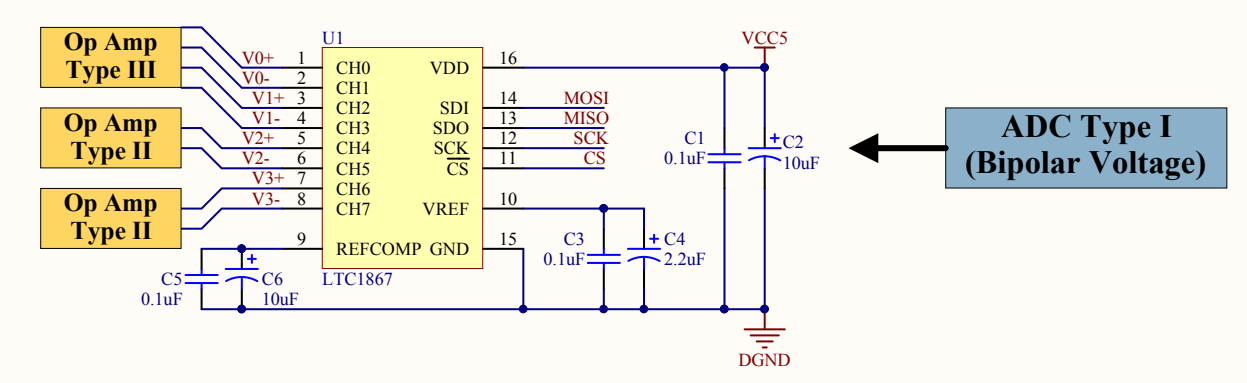

Figure 5.9: The LTC1867 can be configured in differential mode to read voltages relative to their references.

Figure 5.9 shows how the ADC can be used to measure differential inputs. In this mode, the eight channels are coupled, allowing four differential pairs to be measured. The Type II and

III op-amp circuits, described in Section 5.2, are used as inputs for any arbitrary isolated voltages. In the UV-VIS EPS, the Type III circuit measures ±15V, while two Type II circuits measure the battery voltage and the 24V rail. Note that the order is purely arbitrary; any combination of the op-amp circuits can be used to fill the eight channels.

5.3.2 ADC Type II: Current Sensor

A more common application of the LTC1867 is reading eight single-ended inputs referenced to a common ground. Since the ACS712 current sensors, described in Section 5.1, run off of the same VCC and GND as the ADC, their outputs can be read easily. Figure 5.10 shows the Type II configuration, in which eight current sensor circuits are read by a single ADC. Once again, the LTC1867 uses six external capacitors, and sends the current data to a microcontroller via the SPI bus.

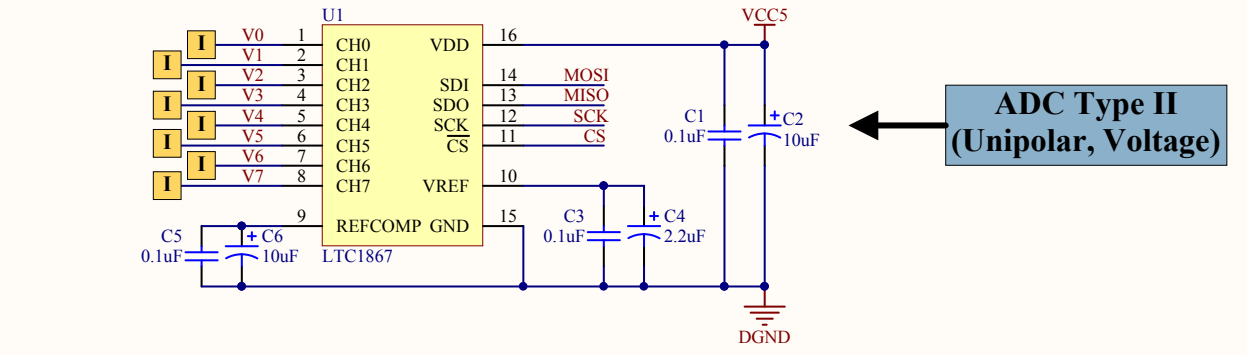

Figure 5.10: Configured in single-ended mode, the LTC1867 is used to read eight current sensors.

5.3.3 ADC Type III: Single-Ended Voltage Sensor

The Type III circuit is effectively identical to the Type II circuit, except that eight single-ended voltages are generated by Type I op-amps instead of current sensors. Other than this, there is no functional difference between the circuits in Figure 5.11 and Figure 5.10. The differentiation is made so that block diagrams of the UV-VIS EPS can state explicitly what each ADC is being used to sense.

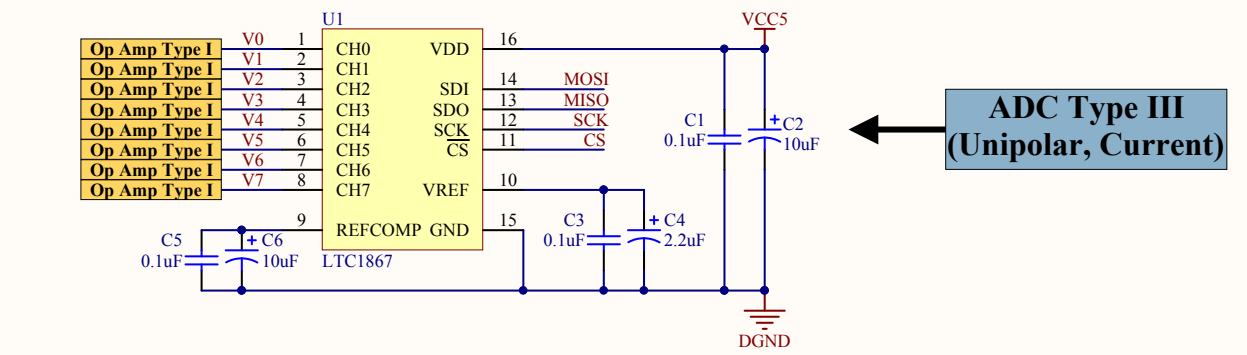

Figure 5.11: The LTC1867 reads eight single-ended voltages that have been generated by op-amp buffers.

5.3.4 ADC Type IV: Mixed Voltage and Current Sensor

A fourth circuit is defined purely for use in block diagrams that describe the UV-VIS EPS. This circuit is a combination of the Type II and III ADC circuits. It splits the eight channels between some number of current sensors and Type I op-amp inputs. This configuration is used multiple times in the UV-VIS EPS when the number of currents and voltages being sensed is not a multiple of eight. The gain in real estate is offset somewhat by a need to parse the different channels in software. This, however, is worth trouble, as it reduces the number of components by seven per consolidated circuit.

Chapter 6

Power Control Logic

The previous three chapters have focused on the fundamental hardware that comprises a power system: power converters, switches and sensors. These are sufficient to form a basic power system in a lab setting. For a flight system, however, there are several logical requirements that drive the need for a digital controller. A flight EPS must be capable of running autonomously, must be commandable, and must provide health and status data. These three functions require communication between the EPS and a human or flight computer. To meet these needs, a flight power system must have at least one embedded microprocessor.

This chapter will focus on both circuit and firmware design for the UV-VIS EPS logic subsystem. A small microcontroller controls the startup and shutdown of the flight computer, and serves as an introductory example of microcontroller design. The brain of the entire EPS is an Arduino microcontroller board, which is much more complex. This chapter is necessarily more specialized than the previous three, though most of the concepts are applicable to future projects as well.

6.1 Microcontroller Overview

As electrical systems have grown smaller and more complex, the need for miniaturized computing has grown as well. In some cases, the principles of digital logic are employed via FPGAs. While powerful and very fast, FPGAs require specialized expertise and are difficult to reprogram once deployed. Microcontrollers and microprocessors, on the other hand, share many principles with modern computers. They are easily programmed and are intended to interface with common

electrical hardware. Microcontrollers, specifically, have general input/output pins (GPIOs) that are user-configurable, as well as integrated memory, timers and low-level communications buses. For this reason, a microcontroller is the most effective way to control a electrical system.

Among the many microcontrollers available today, PIC and AVR are each very common. Both brands are rugged and see use in aerospace projects, but they are even more widely known due to hobbyist electronics. The AVR in particular has been popularized by companies such as Sparkfun and Arduino, both of which offer open source designs and tutorials. This wealth of support makes the AVR easier to design from scratch than the PIC. The added benefit of a GCC compiler allows for a standard C toolchain, making AVR well suited to engineering projects.

6.2 AVR Design

Microcontroller design has two distinct parts. The first is getting the microcontroller itself to run properly; this includes establishing communication with a host computer to flash code onto the chip. The second part is interfacing the microcontroller with the system and any peripheral circuits. Even a small chip like the AVR ATMega168 has 32 pins, most of which are general input/output (GPIO) pins that can be used for any application. A common AVR circuit will have numerous peripherals.

Figure 6.1 shows an ATmega168 microcontroller as used in the UV-VIS EPS. The entire chip runs on 5V, including the AVCC and AREF pins. Capacitors C1 and C2 decouple the power supply; this is more to prevent the AVR from contaminating the supply than vice versa. A 2×3, 0.1" header, denoted AVRISP, is the programming interface. Other than power and ground, four other pins are required to flash code onto the chip. Three of these are the MISO, MOSI and SCK pins that make up the SPI bus. The fourth is the RESET pin, which controls whether the AVR is on or not. The RESET is pulled up to 5V via a 10kΩresistor to ensure the AVR stays on unless the line is asserted low. In user-operated circuits, a push button is often placed between RESET and GND, allowing the user to reset the chip. In remote circuits, the microcontroller either always runs, or another device can be given control over the RESET line.

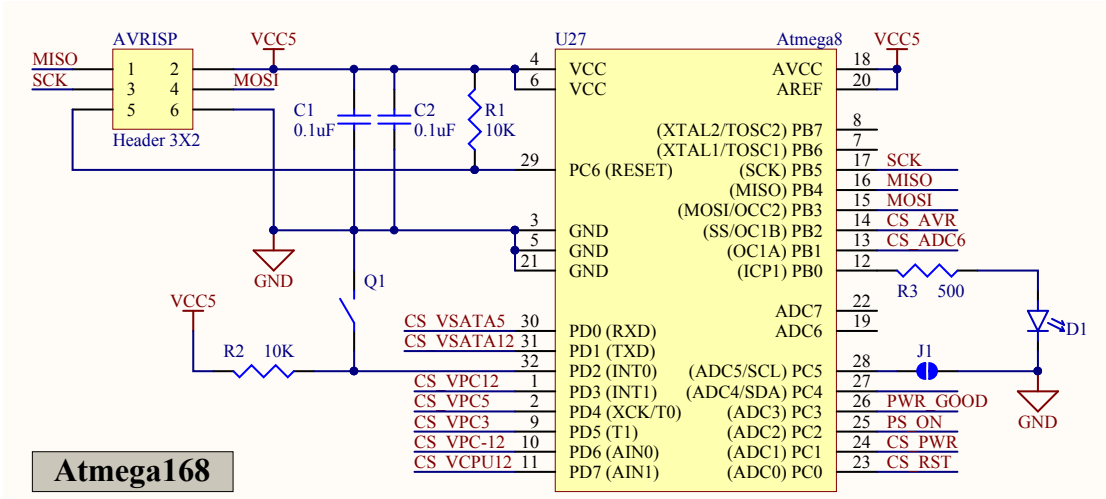

Figure 6.1: Custom designs for microcontrollers involve circuits for power, reset, programming and user interface. Most of the AVR GPIOs are used to interface with switches and sensors.

The AVR interfaces to the system via its GPIOs. These are mostly connected directly to components like MOSFET drivers and ADCs. In Figure 6.1, each of the pins labeled CS on Port D controls a computer power MOSFET. Port B holds the SPI bus, with an ADC chip select and a pin that allows the AVR to be controlled via the bus. The four named pins on Port C are the power and reset switches for the computer, as well as the ATX PSON and PWR GOOD signals.

The remaining GPIOs support various controls for the AVR. Pin PD2 connects via a push button Q1 to GND. Like the RESET pin, it is pulled up to VCC. Depressing the button will change the input from high to low, which can be used to generate an interrupt in the chip's firmware. Pin PC5 can be connected to GND via a jumper. This is intended to be a hardware enable; the AVR can be configured to only run when GND is present on the pin. Finally, pin PB0 drives an LED, and is used in software as a signal for various processes. In a simple test mode, the LED can be lit when Q1 is depressed to indicate that code has been flashed properly.

6.3 Arduino

As mentioned in the previous section, getting a microcontroller running on its own is a large part of the design process. Rather than starting from scratch, commercial boards are available

that provide an already-working microcontroller, effectively mitigating the first half of the design effort. One such solution is an Arduino circuit board. An Arduino houses an AVR microcontroller, breaking out each of the pins and providing communications and power interfaces. The UV-VIS EPS uses an Arduino Mega 2560, which houses one of the largest available 16-bit AVRs, an ATMega2560. The board, shown in Figure 6.2, has enough GPIOs and computational power to run the entire power system.

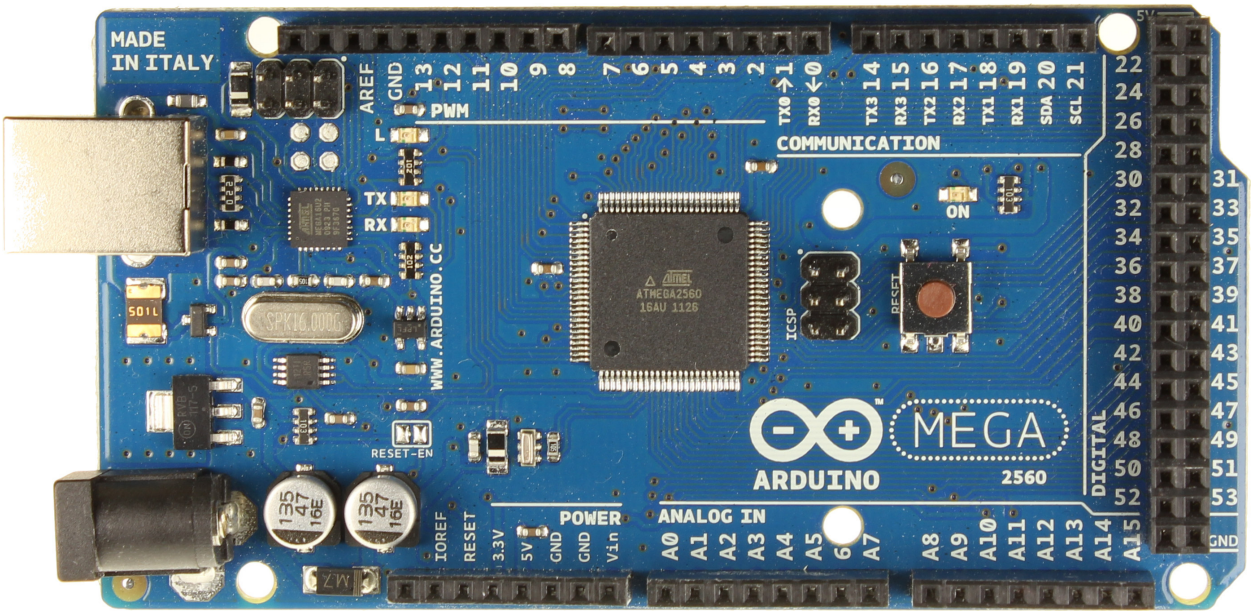

Figure 6.2: The Arduino microcontroller board makes each pin on the ATMega2560 available, and also provides a USB interface and a means of uploading new code.

The Arduino satisfies the first step of the EPS logic design by providing a working microcontroller. There are three remaining steps: the electrical interface, mechanical interface, and firmware. The electrical interface consists of matching the power and GPIO pins of the microcontroller to the switching and sensing circuits on the other boards. The mechanical aspect defines how the Arduino fits together with other boards in the system. Finally, the firmware written to the ATMega2560 onboard is what controls every aspect of the EPS.

6.3.1 Electrical Interface

The electrical schematic of the Arduino is shown below in Figure 6.3. Each grouping of pins roughly reflects the vertical headers provided by the Arduino, which are divided into analog, digital and interface pins. The board runs off of 12V, and produces its own 5V and 3.3V rails. Only two of the ground pins are connected to the rest of the EPS, to prevent ground loops. Two unused pins are also used to transmit 5V and 3.3V from the buck converters discussed in Section 3.4; this provides a choice of 5V and 3.3V rails.

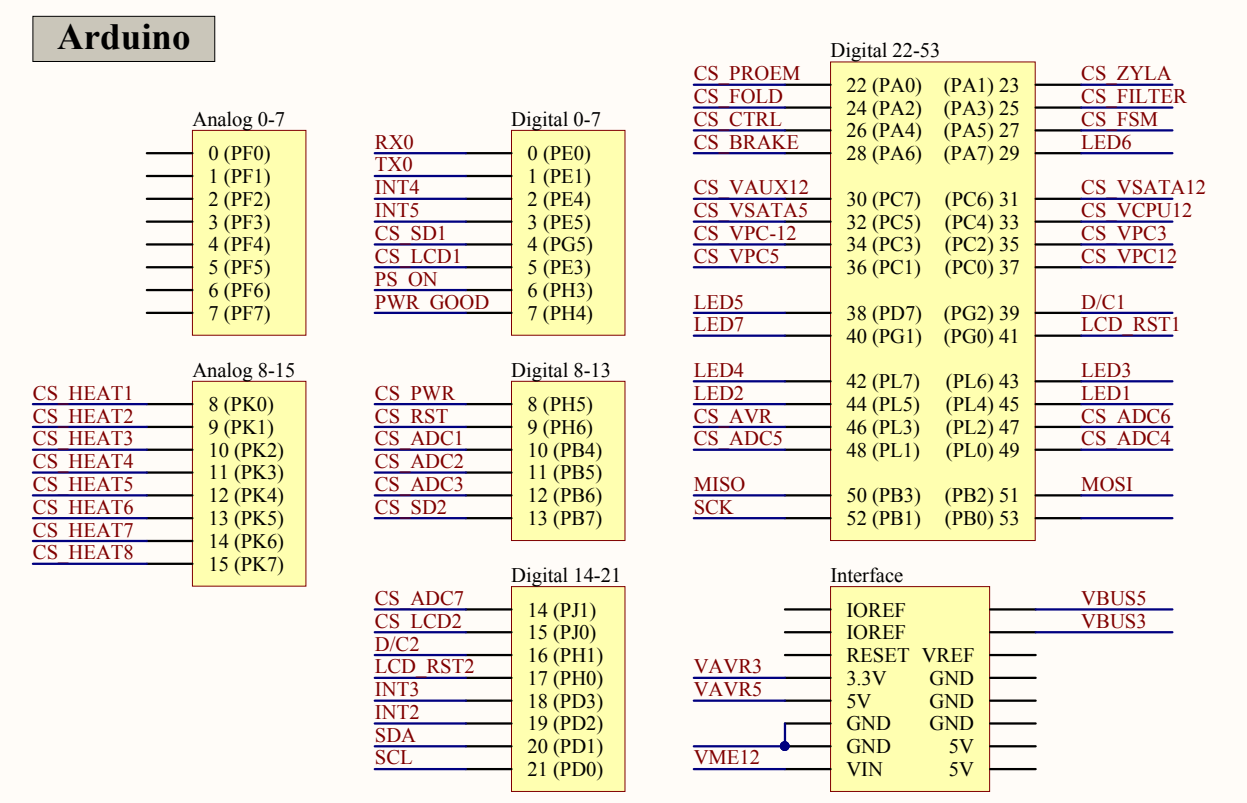

Figure 6.3: The Arduino's many GPIOs are used to control the UV-VIS EPS. Different banks of pins connect to switches and sensors on each board.

Most of the pins on the Arduino are GPIOs, and are used to interface with the various switching and sensing circuits in the EPS. The MOSFET control pins are grouped together on the main digital header, taking up pins 22 through 37, and on one of the analog headers, using pins

8-15. The ADC chip select pins are scattered, utilizing pins 10-12, 14 and 47-49, and the SPI bus for the ADCs is on pins 50-52. The rest of the GPIOs have various uses, including driving LEDs, two LCD screens, and the computer power and reset switches.

6.3.2 Mechanical Interface

The Arduino is intended to mate with other boards via the vertical headers on the board's perimeter. This footprint was used in the UV-VIS design to mate the Arduino to the rest of the EPS stack. Unfortunately, the vertical headers only extend upward; the EPS stack, on the other hand, requires the Arduino to integrate to the top of the stack. To fix this, the vertical headers were replaced by similar female headers with long, male tails extending from the bottom of the board. Each board in the stack (except for the bottom board) uses the footprint shown in Figure 6.4. The Main Power Board on the bottom just replaces the through-hole footprint with a surface-mount one.

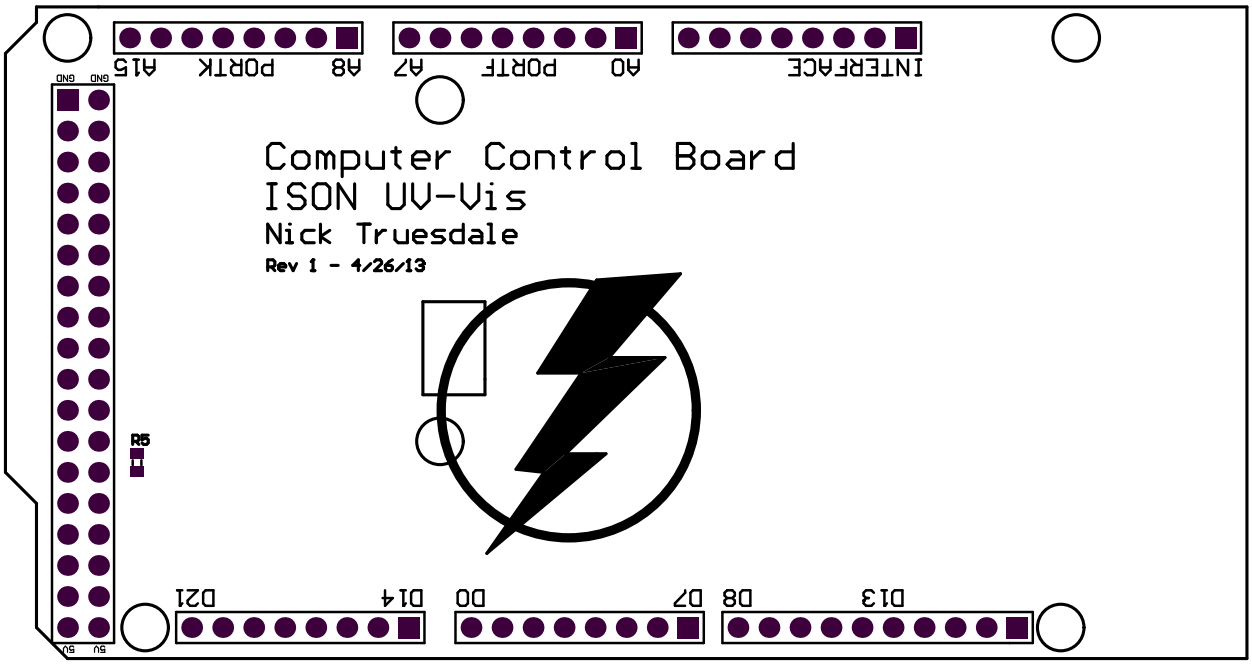

Figure 6.4: The footprint for the Arduino is present on all boards in the EPS stack. This allows the Arduino and any number of boards to be connected vertically, in any order.

6.3.3 Firmware Overview

Arduino software/firmware is written in C, using a large number of libraries supplied by the company. These libraries, and the predefined Arduino code structure, abstract many complex low-level tasks, making flight code development far simpler. The core Arduino libraries are also tested and robust, providing reliable functionality. As is the case with all microcontroller firmware, the code structure centers on a main loop, which runs indefinitely as long as the system is powered. Functions from the Serial, SPI and Timer libraries, along with native C functions, comprise the flight code running within the loop.

The most important function of the Arduino is its command and data USB interface. This protocol is based on a simple message structure specific to BRRISON, in which all messages are character arrays terminated by a newline character. At the end of every loop, the Arduino reads the incoming serial buffer. Once a newline is read, the command is parsed, and a response is given with a boolean – to indicate a successful or failed action – or with the requested data. Commands are supported from any host, so the EPS can be tested or monitored from any computer.

Because the serial monitoring is not interrupt driven, it is important that the main loop runs quickly to avoid serial timeouts. In the data-gathering functions, only one ADC channel is polled and checked per loop. This data is stored in a rolling buffer, so that the most recent value for each ADC channel is always available. Every other code function **is** interrupt driven, utilizing timers. These functions include a computer watchdog, timer interrupts and some serial responses that take a long time to complete.

Chapter 7

EPS Stack

The circuits described in the preceding chapters can be combined and configured to suit a variety of power needs. While the UV-VIS EPS is specialized to the BRRISON mission, its design is meant to showcase this flexibility. The system is divided into several independent circuit boards, each of which satisfies different requirements. This section will develop each board design using the circuit blocks from Chapters 3 to 6. In each case, the board specifications will be discussed. Then, the design will be shown in terms of the predefined circuits, and the overall performance of the circuitry will be analyzed.

In addition to being individually flexible, the combination of the boards into one comprehensive system is intended to address common balloon electronics requirements. Once the design of each board has been described, the performance of the entire EPS stack will be discussed. This will include the performance during testing and flight, applicability to future missions, and recommendations for design fixes and changes.

7.1 EPS System Overview

The UV-VIS EPS supports all of the electronics on the optical bench and inside the pressure vessel. These can be divided into three groups: the instruments and mechanisms, the computer, and the thermal control system. Because the EPS is space-constrained, supporting all three groups from a single circuit board is not possible. Thus, the different roles are divided amongst three circuit boards: the Main Power Board, the Computer Power Board, and the Heater Control Board.

In addition, the Arduino microcontroller board provides the controlling logic for the other three boards.

The four-board EPS is configured in a vertical stack as shown in Figure 7.1. Interfaces between boards are all supported by the Arduino header bus (discussed in Section 6.3.2). This stack layout has several advantages. First, each power board in the stack has independent battery inputs, which allows boards to be tested individually or together. Also, because each board has the same bus interface, the Arduino can be plugged into any board. This facilitates prototyping and testing, as any grouping of boards can be controlled by the same Arduino. Finally, the stack allows an entire power system to exist in a 5" by 6" by 3" volume.

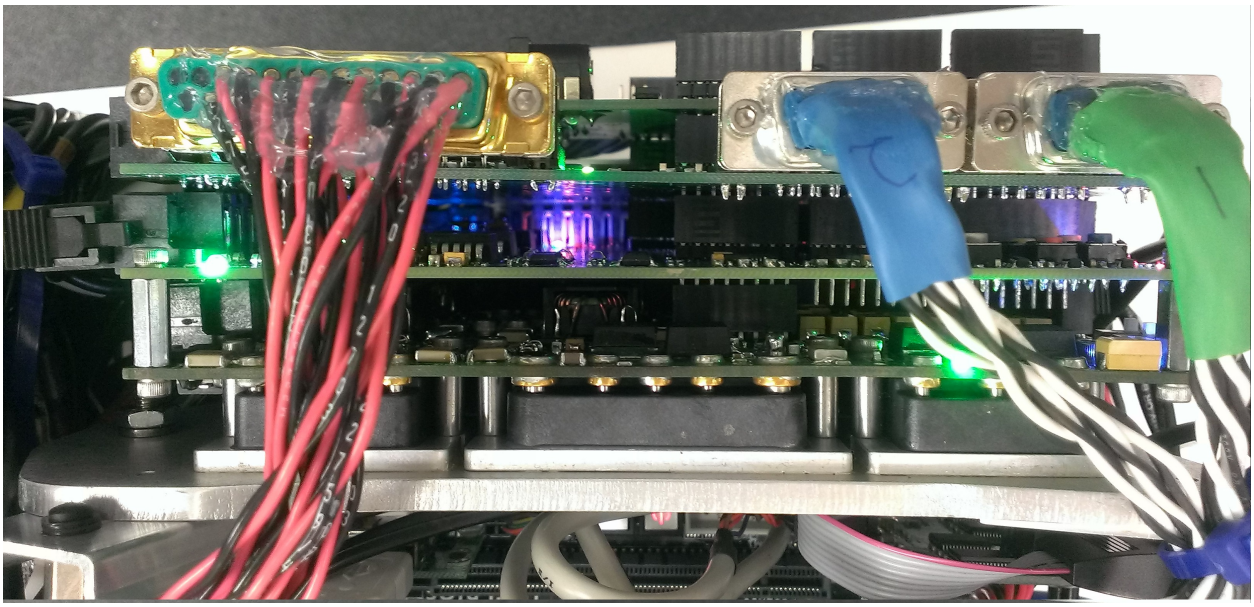

Figure 7.1: The UV-VIS EPS stack is nominally arranged with the Main Board on bottom, the Computer and Heater Boards in the middle, and the Arduino on top.

7.2 Main Power Board

The first board in the EPS stack is the Main Power Board. This board is by far the most complex, because it forms the base of the stack and powers everything except the computer. As the base, the Main Power Board has extra requirements for mounting to the baseplate and supplying

power to other boards in the stack. This, combined with the wide array of external loads, leads to a variety of voltage, current and grounding requirements, and drives the need for many components. This section begins with the board design from a schematic perspective, then covers layout and mechanical considerations.

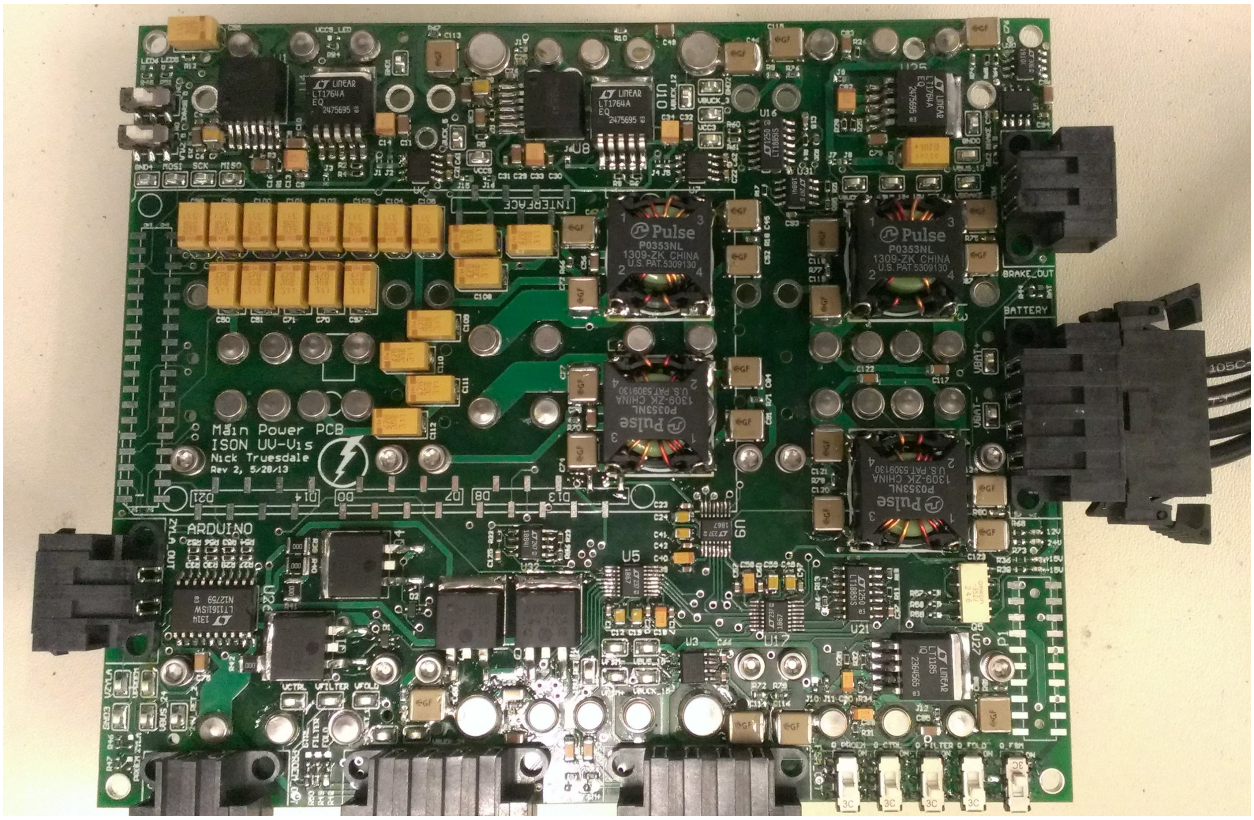

Figure 7.2: The Main Power Board, complete except for the Arduino headers (whose footprints are visible in the left center region of the PCB).

7.2.1 Design Specifications

The requirements for the Main Power Board include the power needs of the UV-VIS electronics, the needs of components and other boards in the stack, and specifications for mounting and stack assembly. While each of these drives minimum design requirements, the EPS requires considerable overhead to allow new boards or peripherals to be added to the system. Defining this overhead without specific add-ons is difficult; thus, many of the power requirements are based on

an arbitrary limit, or are capped by physical constraints.

The external loads for the Main Board, which include the cameras, motor controllers, heater controller and Arduino, are split into four voltage rails: 24V, 12V, +15V and -15V. While each component has different power and noise requirements, the design specifications for the four voltage rails are driven more by modularity. The general design philosophy for each rail is to supply extra power for at least one more large component, such as a new camera or motor. The ripple is also over-designed to accommodate all but the most sensitive components. Finally, the voltage converter designs are duplicated to improve simplicity.

Table 7.1 shows the specifications for the 24V rail. It supports the ProEM, the motor controllers and the heater controller. Of the four, the ProEM requires the most power. To accommodate additional hardware, a 250W converter was selected. Though a higher rating would be optimal, the size constraints of the board do not allow for larger converters. None of the components have strict ripple requirements, so a goal of 10mVpp was chosen to facilitate future hardware.

Table 7.1: 24V Rail Specifications

Component	**Ripple**	**Max Power**
ProEM	240mVpp (est.)	120W
Filter Wheel Motor	N/A	20W
Fold Mirror Motor	N/A	20W
Heater Controller	N/A	5W
Minimum Req:	240mVpp	165W
Design:	10mVpp	300W

The 12V rail, specified in Table 7.2, supports the Zyla, the brake for the Fold Mirror and the Arduino microcontroller board. It has the same design as the 24V rail: 250W maximum power and 10mVpp ripple. This is sufficient to support many other applications, which is useful since 12V is a common voltage for both low- and high-level electronics.

Table 7.2: 12V Rail Specifications

Component	**Ripple**	**Max Power**
Zyla	200mVpp	60W
Fold Mirror Brake	N/A	10W
Arduino	150mVpp (est.)	5W (est.)
Minimum Req:	150mVpp	75W
Design:	10mVpp	300W

Table 7.3 gives the power and ripple specifications for the ±15V pair of voltage rails. The only component on these rails is the FSM, which draws very little power in the BRRISON operational mode. However, the FSM can theoretically draw over 100W for very high accelerations, so the maximum power on **each** rail is 150W. This also allows for future applications, in which a third positive rail or a negative rail is needed for a high-power component.

Of all the the UV-VIS electronics, only the FSM has strict ripple requirements. The +15V and -15V rails should each have a ripple less than 10mVpp to prevent jitter in the analog control loop. While the vendor does not specify a frequency range, it is reasonable to assume that the mirror will not be disturbed by disturbance frequencies far greater than the control bandwidth, which is up to 5kHz. Thus, the ±15V rails have a strict ripple requirement below 100kHz, with a goal to achieve 10mVpp as high as 20MHz.

Table 7.3: ±15V Rail Specifications

Component	**Ripple**	**Max Power**
FSM	10mVpp	6W
Minimum Req:	10mVpp	6W
Design:	10mVpp	100W

In addition to the external loads, the power stack has a multitude of sensors, switches, control ICs, etc. that require power. These internal components were all selected to run off of a common 5V rail to simplify design and digital interfaces. However, to remain extensible to future designs, a 3.3V rail is also necessary, because it is common in low-level electronics. While the circuitry on the Main Board itself draws no more than 1W of power, other boards could conceivably require much more. For this reason, there is a loose requirement that both the 5V and 3.3V rails support several amperes of current.

The final requirements for the Main Board pertain to physical size and mounting. Due to the ECS pressure vessel design, the power stack is constricted to a 5 by 6 inch footprint, though there is room for connectors and wires on three of the sides of each board. The boards must also mount to the pressure vessel on the bottom, and the Computer Control Board on the top. This requires holes for standoffs, and the Arduino footprint which makes up the inter-board bus.

7.2.2 Schematic Design

Figure 7.3 is a block diagram of the Main Power Board. It consists solely of blocks that were defined in previous chapters, with the exception of connectors. These blocks are color-coded to differentiate the conversion, switching, sensing and logic circuits.

Every one of the conversion circuits discussed in Chapter 3 is used on the Main Board. Type I DC-DC circuits, which use a 250W Mini DC-DC converter and a MicroRAM filter module, create the 24V and 12V rails. A Type II circuit, which uses two 15V Micro DC-DC converters feeding into positive and negative linear regulators, creates the ±15V supply for the FSM. Each of the DC-DC circuits has a common mode filter on the input to reduce switching noise. Finally, downstream of the 12V converter, two buck/linear regulator pairs create the 5V and 3.3V rails.

Every external load is switched by a MOSFET (with the exception of the FSM, whose control is contained in the DC-DC circuit). MOSFET Type I and IV circuits are used for either single or quad switches. Overall, there are eight independent output voltages and the 5V and 3.3V internal voltages. These all have current sensors in line.

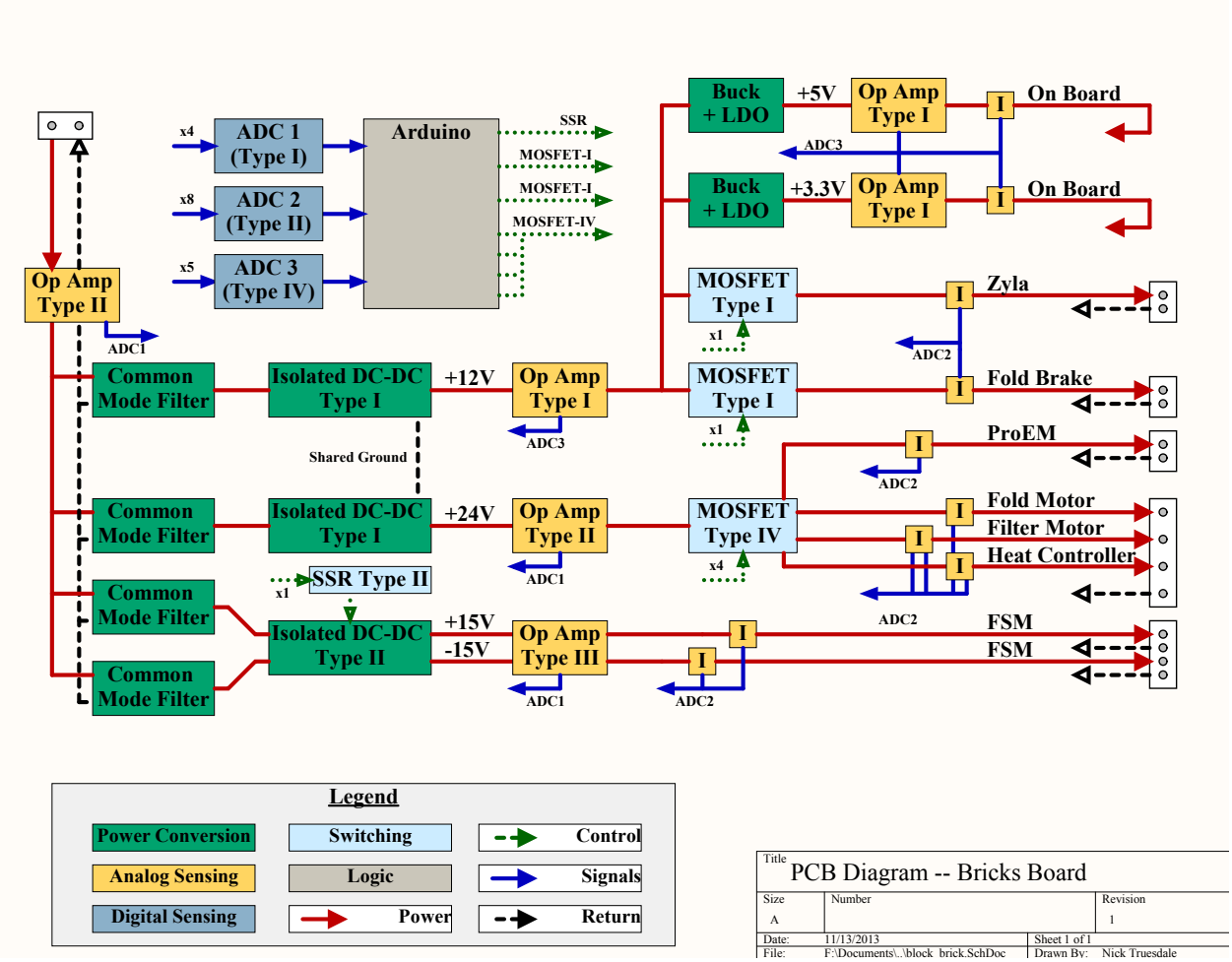

Figure 7.3: This block diagam of the Main Power Board shows how the 12V, 24V, ±15V, 5V and 3.3V rails are regulated, switched and sensed.

Each rail has a voltage sensing op-amp circuit directly after the converter. For the rails that share the Arduino ground (12V, 5V, 3.3V), single-ended Type I circuits are used. For voltages isolated from the Arduino (the battery, 24V and ±15V), differential Type II and III circuits are used instead. The outputs of these and the current sensors are fed to three ADCs, which are configured as single-ended or differential appropriately. These in turn send data to the Arduino, which is mounted via the stack.

7.2.2.1 Grounding

Grounding is an important consideration for the Main Board, because there are so many isolated voltages. First, it is important to notice that the 5V and 3.3V rails, which are not isolated, necessarily share a ground with the 12V rail. This is the same ground as the Arduino. Second, the isolation between the battery input return and the main voltage rail grounds is important, as it prevents noise and protects the UV-VIS hardware from an input failure. Finally, the input and outputs are both isolated from chassis ground; though not explicitly shown in Figure 7.3, the only connection to chassis is via decoupling capacitors in the common mode filter and DC-DC circuits.

In the first revision of the Main Board, **all** of the output voltages shared a ground. However, this caused too much noise contamination between rails. To remedy this, the second revision splits the 24V, 12V and ±15V grounds. However, a design error requires the 24V and 12V grounds to be connected; because the Type IV MOSFET circuit does not have isolating SSRs built in, its control lines require the same reference as the Arduino. In a future revision, SSRs must be added to isolate the Arduino control pins; this will allow the 24V ground to be truly separate. In the flight revision, since the grounds were linked at a single point (a commonly recommended way to isolate ground planes in PCBs), the amount of added noise was neglible.

7.2.3 Physical Layout

The layout of the Main Power Board is complicated by the DC-DC converter circuits. Between the four main rails, there are two Mini sized bricks and four Micro bricks. These fit snugly in the 5 by 6 inch board area, on the bottom of the board, as shown in Figure 7.4. Furthermore, the bricks require four mounting standoffs each, which serve to mechanically connect the board, bricks and chassis all together. They also are conductive paths to chassis ground.

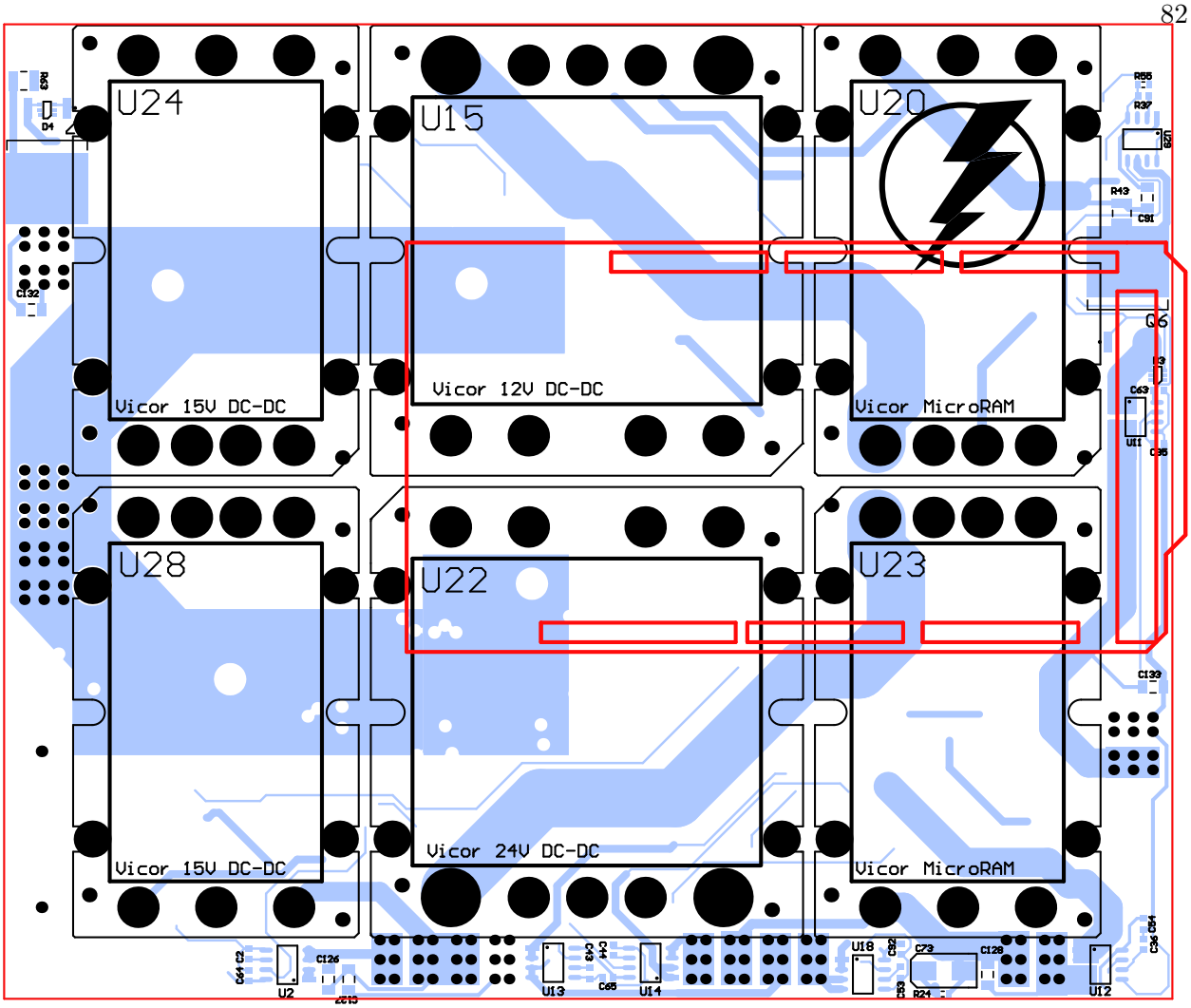

Figure 7.4: A back (**mirrored**) view of the Main Power Board, with holes in black, shows how the center and borders of the board are almost completely occupied. The addition of connectors on one side forces the Arduino (red) to straddle the holes on the right-center of the board.

Between all the bricks, there are 70 mounting holes in the Main Board, aligned in a grid. These interfere with the Arduino footprint, leaving only one possible location on the left side of the board. Between the Arduino and the bricks, the board is separated into rectangular sections. These are further constricted by connectors, which must lie on the perimeter. Finally, since the bottom of the board is filled by the bricks, almost all of the remaining circuitry must lie on the top of the board. This leads to a very tight, clustered layout, as shown in Figure 7.5.

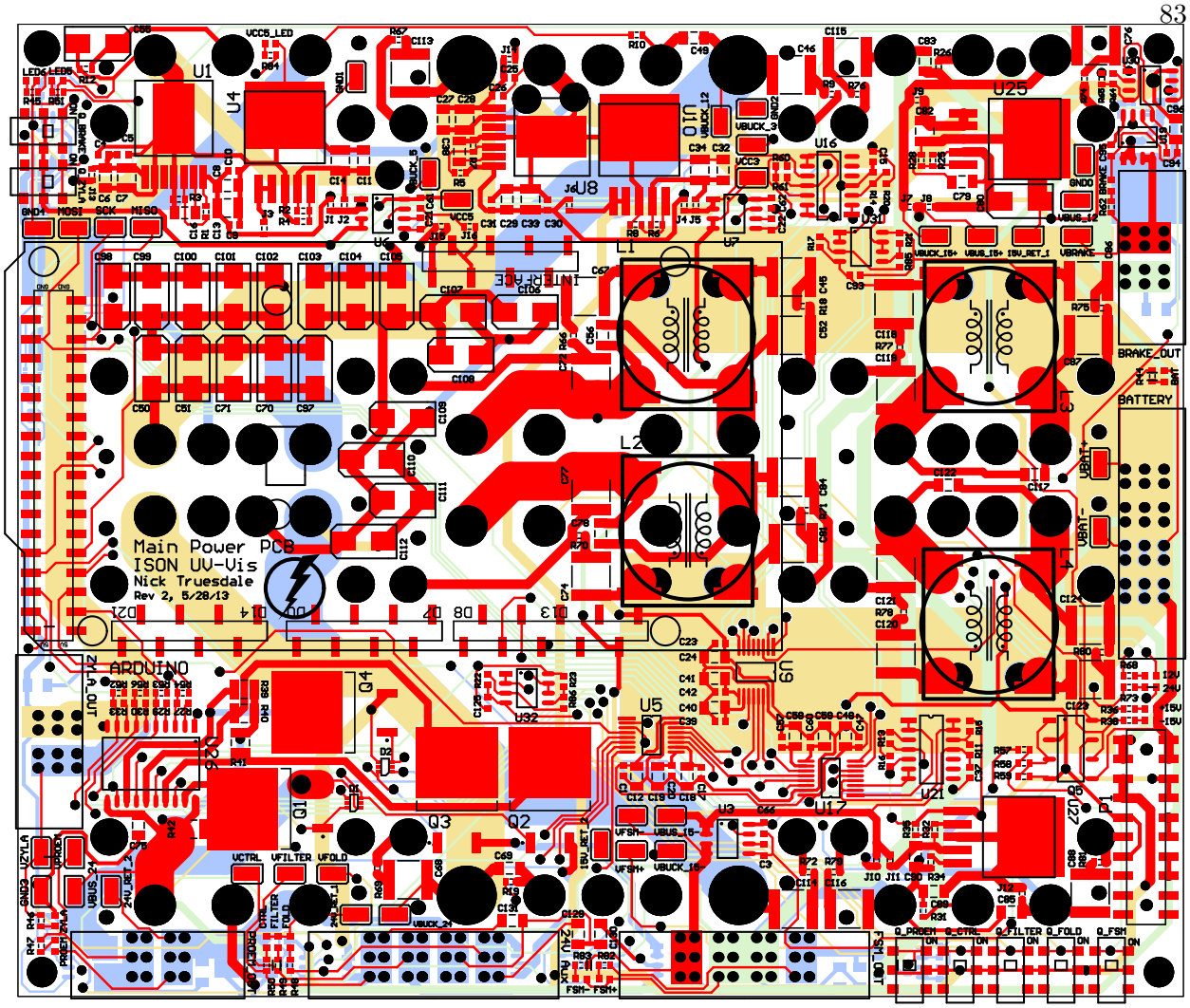

Figure 7.5: The Main Power Board consists of four layers. The top layer (red) holds most components that support the bricks. The second layer contains the remaining signal traces, and the bottom two layers hold the bricks and power traces.

7.2.4 DC-DC Converter Mounting

Unlike all the other components in the EPS stack, the DC-DC converter modules are not simply thru-hole or surface-mount components. Instead, the bricks require additional mounting hardware in the form of standoffs and sockets. Figure 7.6 shows how the bricks mount between the chassis (which is the very bottom of the EPS stack) and the Main Power Board. Standoffs hold the chassis and PCB together, sandwiching the brick in between and providing a chassis ground

connection. Thru-hole sockets, soldered into the PCB, allow the modules to be snapped in place. A module can be removed and replaced if it is faulty, or if the user wishes to insert a brick with a different output voltage or power rating.

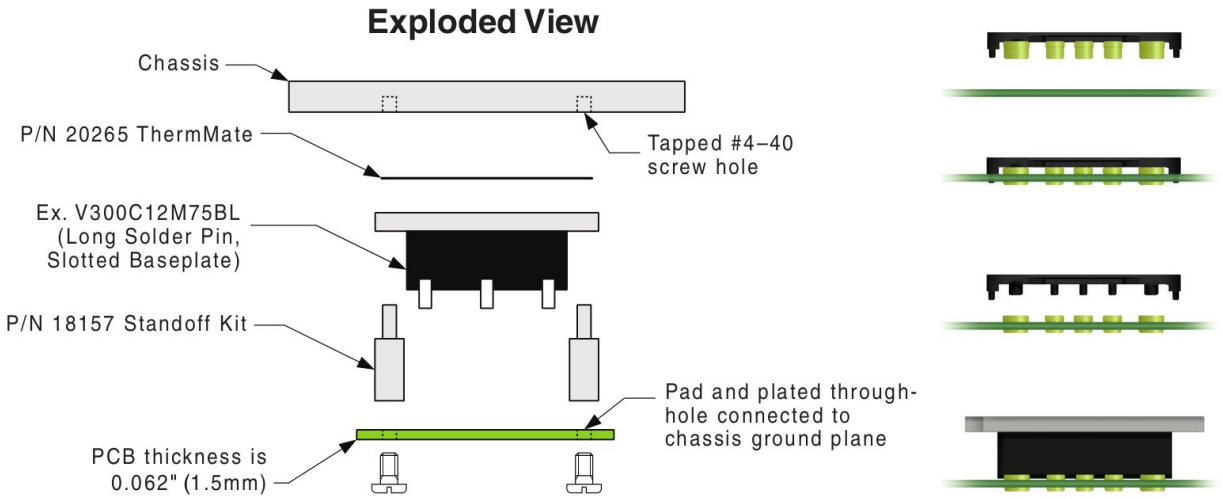

Figure 7.6: This diagram, taken from the Vicor Design Guide [30], shows the hardware necessary for mounting the DC-DC bricks. On the left, the brick is sandwiched between the PCB and the chassis, held in place by the sockets and with standoffs. On the right, sockets are inserted and soldered into holes in the PCB.

7.3 Computer Power Board

All of the electronics on the UV-VIS bench and the associated control circuitry run off of single DC inputs. The flight computer, however, is an ATX motherboard, and requires a much more complicated set of DC voltages and digital control signals. This functionality is supplied by the VME-550 power converter and the Computer Power Board. Together, these boards imitate a typical desktop computer's ATX power supply, allowing the flight computer to function as normal. This section will cover the ATX standard, which drives the design of the Computer Board. After detailing the schematic design and layout, a critical timing error and its solution will be discussed.

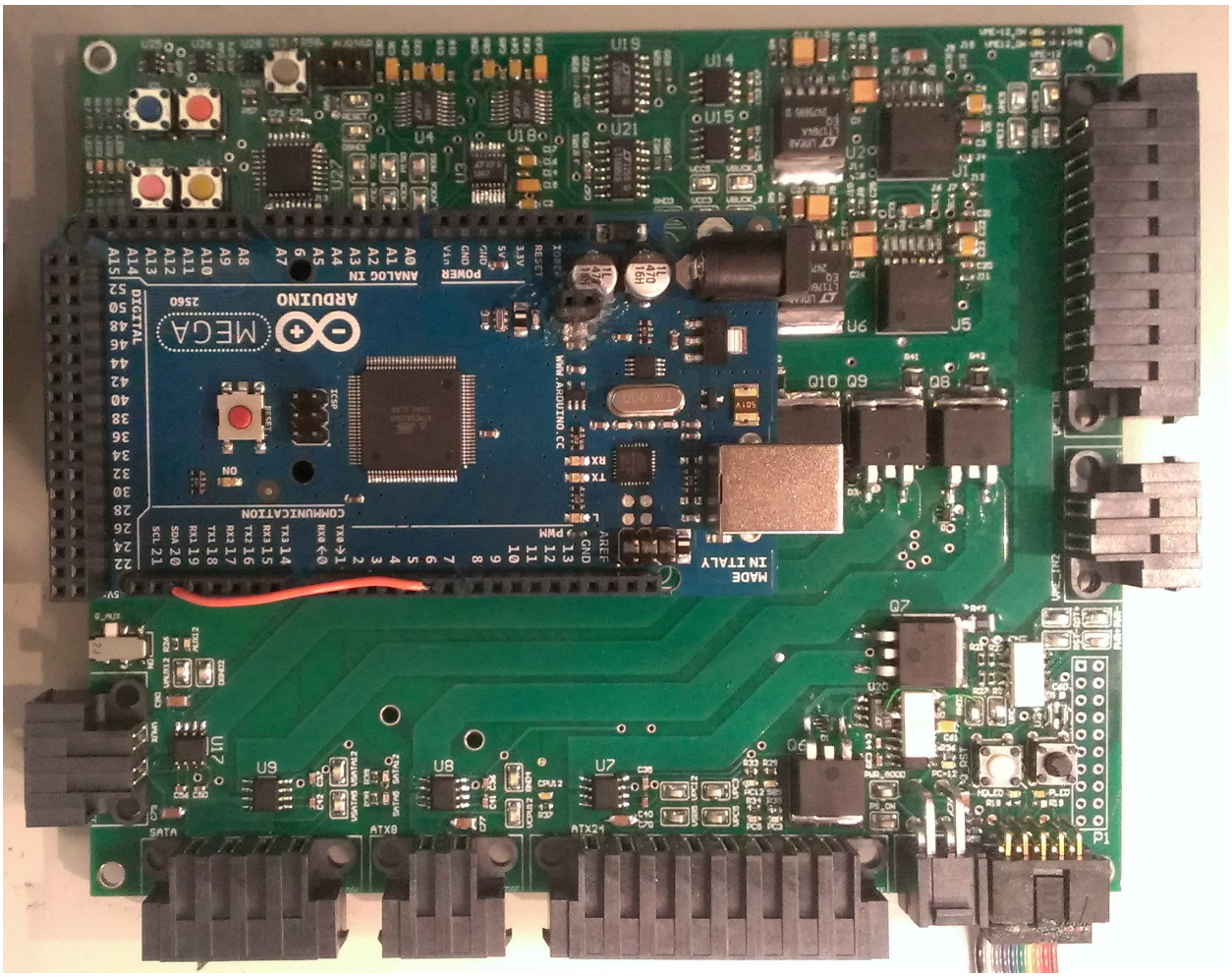

Figure 7.7: The Computer Power Board, assembled and mated with the Arduino in a testing configuration. Most sensing components are located at the top of the board, near the Arduino bus. Large current-carrying traces are visible on the bottom, leading to current sensors and connectors.

7.3.1 ATX Specification

One advantage of using an ATX motherboard over other COTS options is that the power specifications are very well documented. The ATX/ATX12V Power Supply Design Guide [1] defines the voltage and power requirements for every rail and the timing of the control signals. Following these specifications is imperative to ensure the safety of the motherboard; improper power handling can damage or destroy hardware on the motherboard (as discussed in Section 7.3.5).

ATX motherboards obtain their power from two connectors. The first, termed the main connector, carries 12V, 5V, 3.3V and a minimally used -12V. These four voltage rails power almost everything on the motherboard, with the exception of startup circuitry and the processor. A 5V standby voltage, which is present even when the rest of the computer is off, powers the boot circuits that need to run before the main voltage rails have been initialized. All five voltages share a common return, COM, which has 8 pins on the connector to provide sufficient current capacity. The connector pin designators are shown in Figure 7.8.

The other motherboard power connector is the CPU 12V connector. This connector, which carries a single 12V supply, powers the processor only. Like the main connector, it uses the Molex Mini-Fit Jr. form factor. A third connector, intended for peripherals like harddrives, is a Molex 4-pin connector that carries 12V and 5V. Both are also shown in Figure 7.8.

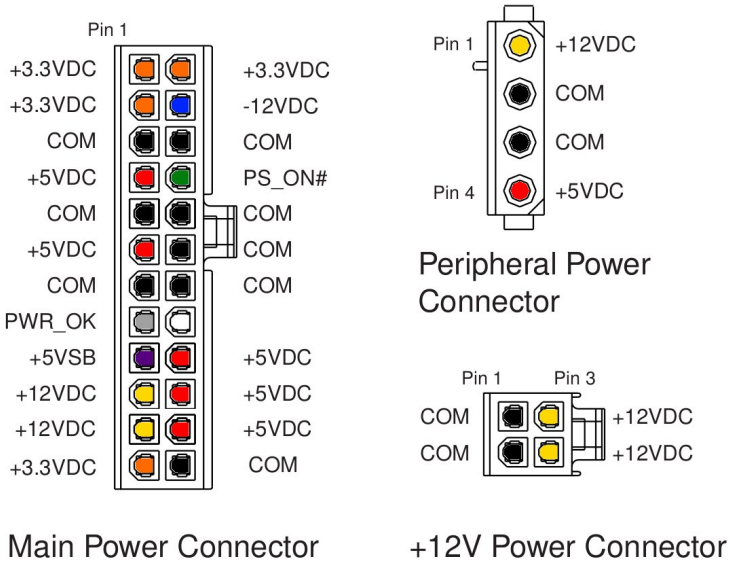

Figure 7.8: There are three important connectors in the ATX specification: a 24-pin main power connector, a 4- or 8-pin 12V connector for CPU power, and a 4-pin 12V and 5V connector for computer peripherals (such as hard drives).

Two 5V digital signals are also contained in the 24-pin main connector. PS_ON is a signal controlled by the motherboard, and is pulled low to request power from the power supply. It is sent

high when the motherboard is shut down. PWR_OK is a signal from the supply to the motherboard indicating that the voltages are clean and in range. During startup, the timing of the these two signals is important. Figure 7.9 shows how, after the motherboard requests power, the voltages ramp up and, once they are in range, PWR_OK is asserted.

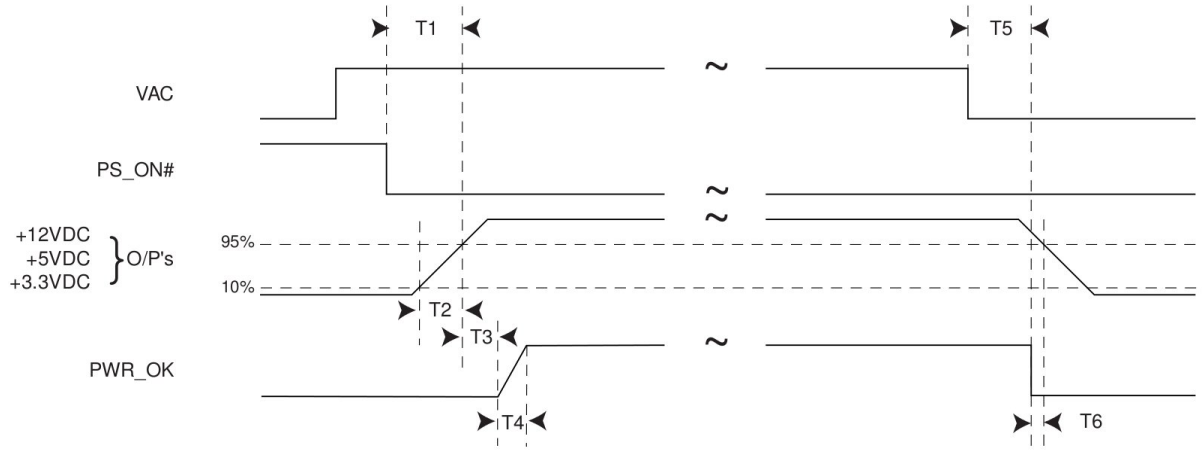

Figure 7.9: This diagram defines the timing of the PS_ON and PWR_OK signals relative to the voltage rails. Note that VAC would typically be the AC power input, but in this case is the EPS system power.

The time intervals in the diagram are given by the ATX Power Supply Design Specification [1], and have been replicated in Table 7.4. The most critical is T2. This specifies the ramp-up speed of the voltage rails, which in turn drives the inrush current as the motherboard powers up. If voltage is turned on too quickly, the amount of inrush current can be damaging. If it is too slow, the motherboard may not turn on correctly.

Table 7.4: ATX Signal Timing Intervals

Name	**Symbol**	**Min Value**	**Max Value**
Power-On	T1	-	500 ms
Voltage Ramp-Up	T2	0.1 ms	20 ms
PWR_OK Delay	T3	100 ms	500 ms
PWR_OK Risetime	T4	-	10 ms
PWR_OK Hold-Up Time After Power Loss	T5	16 ms	-
Power Down Warning	T6	1 ms	-

7.3.2 Design Specifications

The design specifications of the Computer Board are driven mostly by the ATX standard. The power rails themselves are handled entirely by the VME-550 converter, discussed in Section 3.3. This converter generates the 12V, 5V, 3.3V and -12V rails, all with the necessary power and noise ratings. The job of the Computer Board is to divide these as necessary and control the startup and shutdown of the computer.

The Computer Board must provide the main ATX voltages (VPC12, VPC5, VPC3, and VPC-12), the CPU voltage (VCPU12), and the two SATA voltages (VSATA12 and VSATA5). Each of these must be switchable, and the control must be timed by the Arduino. Each rail must be sensed as well; this dictates the need for current and voltage sensors. A final specification, which is not necessary for flight but facilitates testing, is for 5V and 3.3V rails mirroring those on the Main Board. These rails are used for prototyping, and must not affect the computer voltage during flight.

7.3.3 Schematic Design

A block diagram of the Computer Power Board is shown in Figure 7.10. Because the Computer Board itself does not need to convert voltage for the computer, its design is much simpler than the Main Power Board. Main power conversion occurs within the VME-550, and regulated power enters the board via two connectors. The only on-board converters create 5V and 3.3V rails for logic circuitry. These are the same buck/LDO circuits used on the Main Board, and are a backup so that the stack can be run with the Computer Board as its base during testing. The 5V and 3.3V are kept separate from the computer lines to prevent noise from coupling.

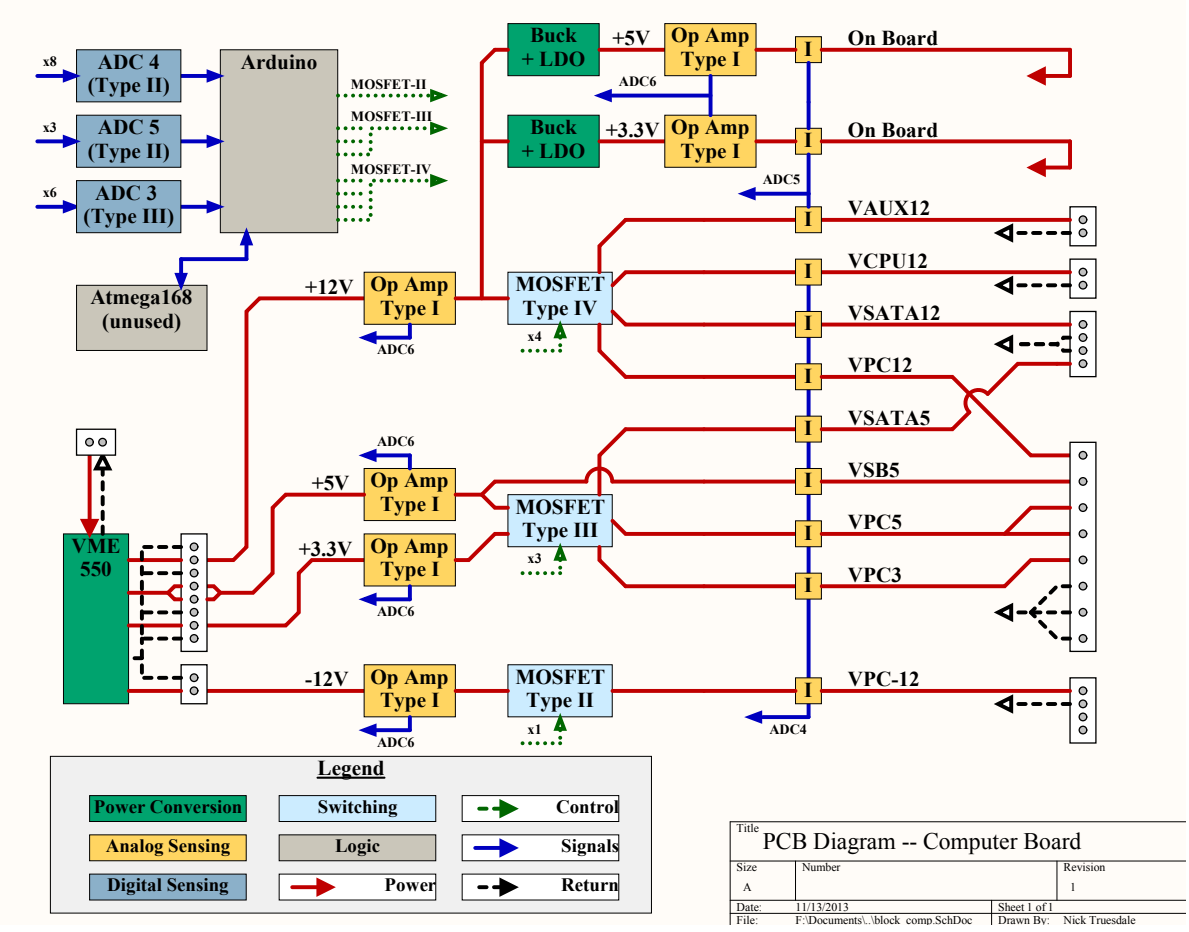

Figure 7.10: This block diagam of the Computer Power Board shows how the 12V, 5V, 3.3V and -12V rails from the VME-550 are split to generate the required computer voltages.

Power enters the board through two connectors that carry 12V, 5V, 3.3V and -12V from the VME-550. These lines are split into several independent rails, as specified by the ATX standard. The 12V line, in addition to powering the logic voltage converters, is divided into four lines: VPC12 is the main 12V line, VCPU12 is for CPU power, VSATA12 goes to the hard drives, and VAUX12 is an extra line. The 5V input is split into main (VPC5), standby (VSB5) and SATA (VSATA5) lines. The 3.3V and -12V are used solely on the main ATX connector.

Three different MOSFET driving circuits are used on the Computer Board. The four 12V lines are made using a Type IV circuit, the same design used to make the four 24V rails on the Main Board. The 5V and 3.3V lines are made using a low-voltage Type III circuit, which is unique to the Computer Board. Finally, the -12V requires the Type II circuit, since it is negative. Note that the 5VSB line is not switched; it powers the computer boot circuitry at all times.

Each of the six voltage rails are sensed using a Type I op-amp circuit. These voltages are read by a single, single-ended ADC. Two other ADCs, also in the single-ended configuration, are used to record the outputs of 11 current sensors, one on each independent rail.

7.3.4 Physical layout

Unlike the Main Power Board, whose complexity led to a very involved layout, the Computer Board is relatively simple. The only mounting considerations are for standoffs on the corners, and for the Arduino. The Arduino bus headers are placed in an identical spot as the Main Board, so the boards can stack evenly. The rest of the components are arranged about the Arduino, with most on the front of the board and some MOSFETs on the back.

Though the Computer Board does not convert power, it still must carry it. High current in the 3.3V and 5V traces especially can cause heating and, if the traces are not wide enough, damage to the board. For this reason, the 3.3V and 5V rails are routed on the back of the Computer Board, using large copper pours to mitigate heating. The 12V rails, which use less current, are routed on the front. Even these traces, though, take up much of the bottom of the board, forcing the rest of the components to the bottom-right corner and the top half.

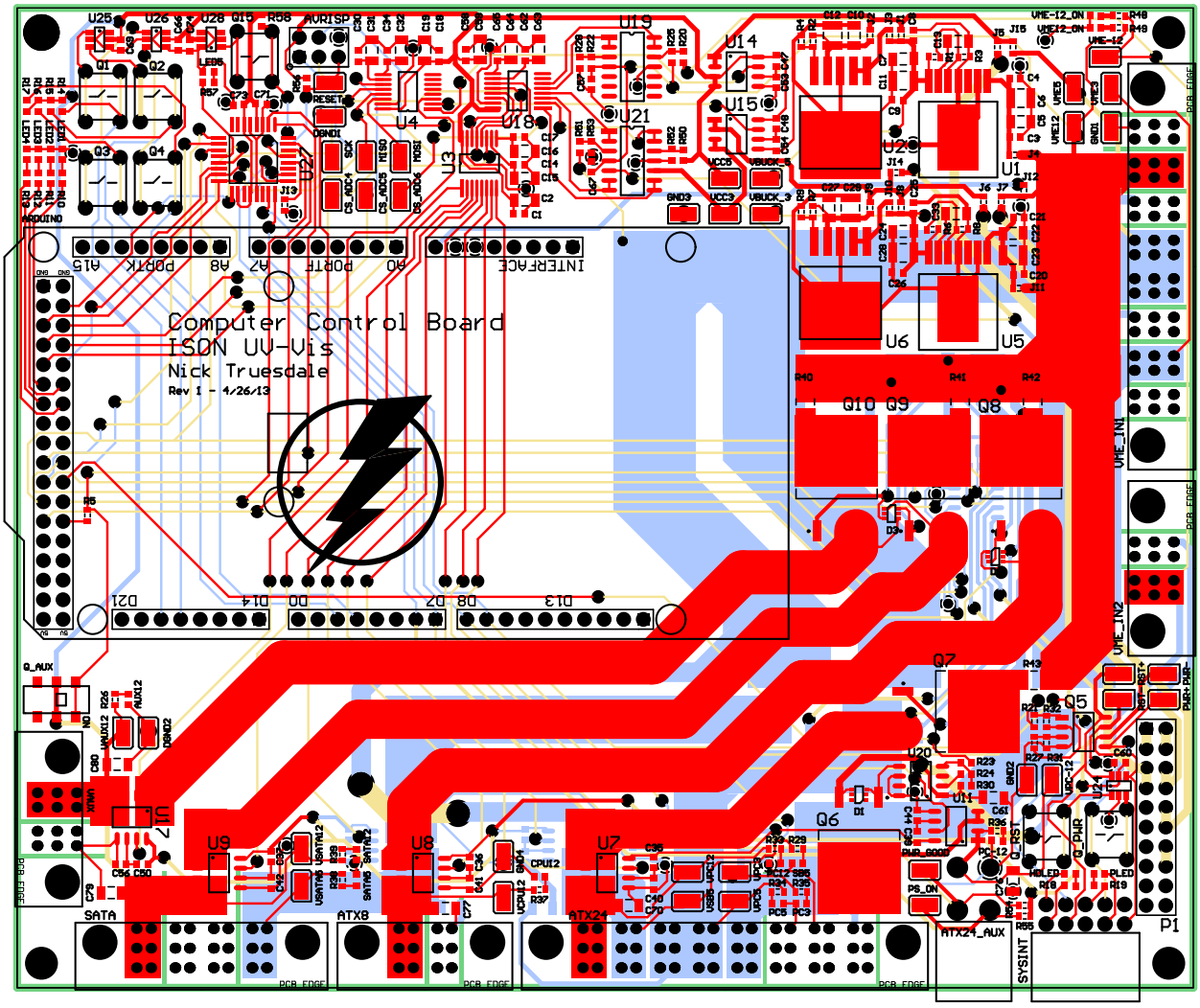

Figure 7.11: This view of the Computer Power Board, with the top layer in red and the bottom in blue, shows the clustering of logical circuits at top and bottom-right, with the rest of the board holding MOSFETs, sensors and thick power traces.

7.3.5 Timing Errors

During testing, a critical problem arose with the Computer Power Board. Motherboards receiving power from the system were slowly degrading and losing functionality. The problem was not due to steady state conditions; both voltage and current from the Computer Board are nominal during operation, and the voltage regulation surpasses the ATX specifications. Instead, the issue was found to be caused by transient currents on startup.

As discussed in Section 7.3.1, the startup timing for an ATX power supply is strictly defined. Specifically, the voltage ramp-up time, denoted T2, must be between 0.1ms and 20ms. One reason for the lower limit is that a steep voltage ramp causes a large inrush current. Even if the total ramp-up time is long, even small segments of the ramp with a sharper voltage increase can cause damage. While the Computer Power Board's total ramp-up time met the specification, the initial voltage gradient was 25 V/ms, enough to cause a potentially damaging inrush current. This was true for every voltage rail, but was by far worst on the VPC12 rail.

Figure 7.12 below shows three oscilloscope traces of the VPC12 rail on startup. The red curve is the original ramp-up from the Computer Board. The total time is roughly 2 ms, but the initial rise is 2V in only 60 µs. This sharp increase is the probable cause of the motherboard damage. In contrast, the blue trace, showing a COTS power supply's startup, is much smoother, taking 10 ms. The COTS supply was known to function properly, and acted as a control while troubleshooting.

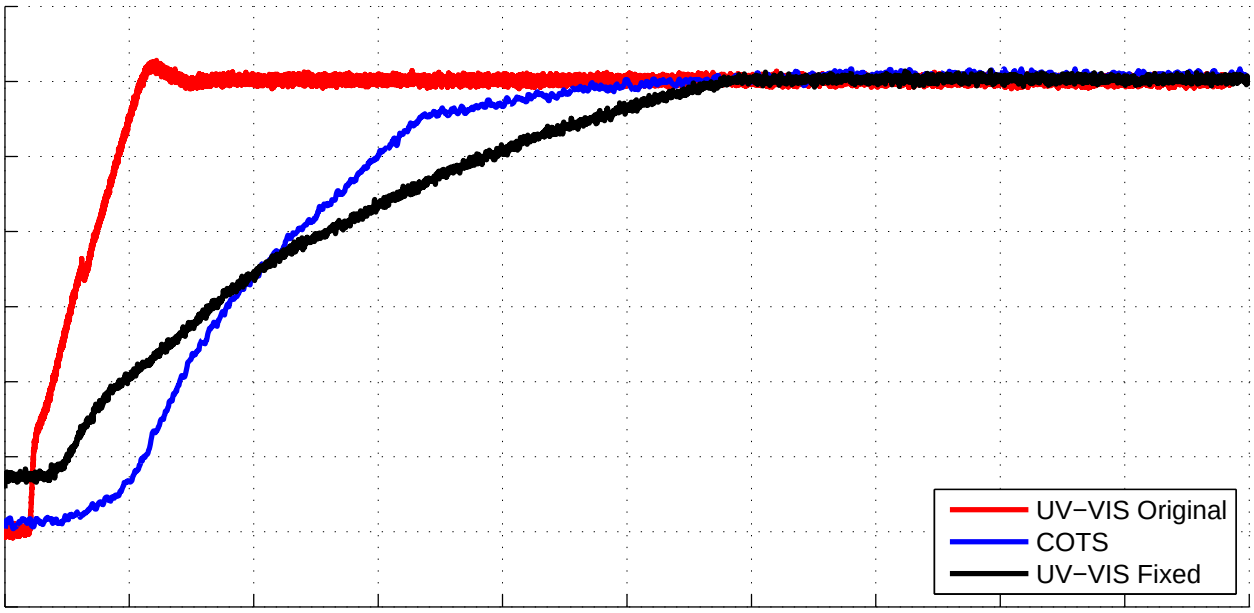

Figure 7.12: The voltage ramp-up of the VPC12 rail was tested for the UV-VIS EPS and compared to a COTS supply. The modified UV-VIS VPC12 rail was also tested and was shown to have the slowest turn on time.

Figure 7.13 shows the inrush current for the same startup data. The correlation between voltage slope and inrush current is apparent from the original Computer Board and COTS traces (red and blue). The UV-VIS EPS allows a peak of 35A to flow into the motherboard, while the COTS supply only allows 6A. In addition to the large current spike, which corresponds to the initial 2V rise, the UV-VIS permits a continuous flow of more than 10A over the entire 2ms rise. The brief spike and subsequent prolonged exposure is likely the cause of the motherboard damage, especially since many voltages on the motherboard are derived from this 12V rail.

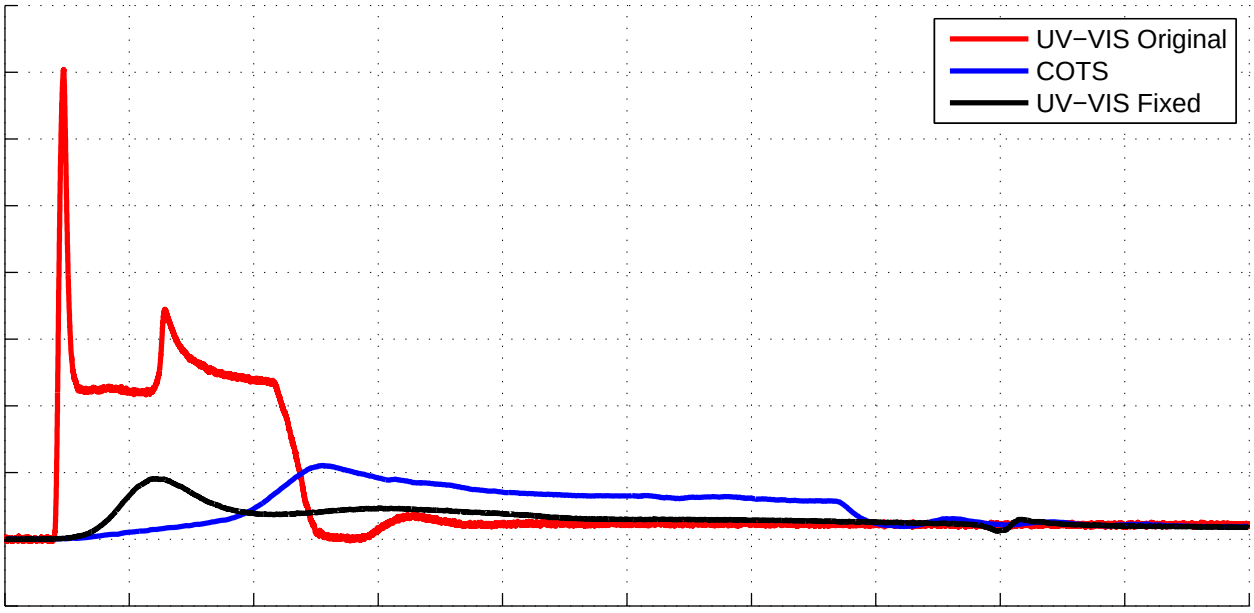

Figure 7.13: A plot of the inrush current on the VPC12 rail shows how the initial revision of the Computer Power Board allowed dangerous current spikes of 35A, and how modifications dropped these spikes below 5A.

To fix the problem, the turn-on times of the Computer Power Board's rails all had to be increased. This was accomplished by adding a low-pass resistor-capacitor filter to the MOSFET gate for each rail, per the recommendation of the LT1910 datasheet [27]. This filter slows the output of the LT1910 gate drive pin, which in turn slows the MOSFET turn-on time. There was no time for a new revision, so the fix was implemented by desoldering each MOSFET gate and

inserting a resistor between the gate and pad and adding a capacitor to ground.

In Figures 7.12 and 7.13 above, the fixed VPC12 rail is shown in black. The new rise time is now similar to the COTS power supply, as is the resulting inrush current. In fact, the modified Computer Power Board now provides a slower and more gentle turn on than the COTS supply, preventing damage to the flight computer.

7.4 Heater Control Board

The third board in the EPS stack is the Heater Control Board. This PCB is a perfect example of the modularity of the individual circuit designs and the stack concept itself. It was implemented two months after the Main and Computer Boards – just before final integration – to provide switching for the eight UV-VIS heater circuits. Because the MOSFET and current sensor circuits already existed, as well as the stack footprint, it was very easy to manufacture the new board and integrate it. This section discusses the design requirements, schematic and layout.

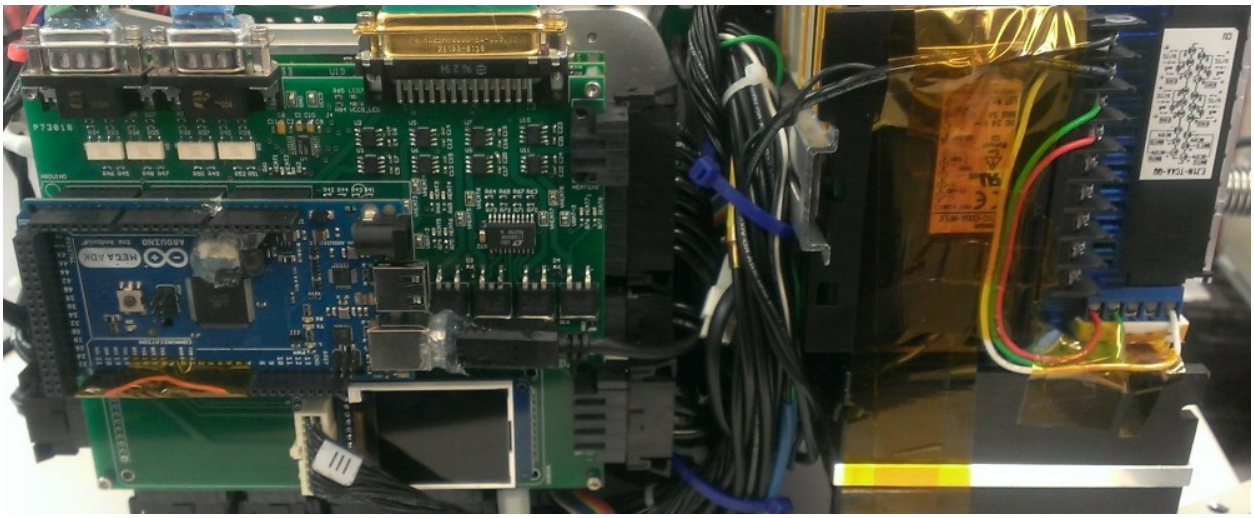

Figure 7.14: Because it was designed just before final integration, the Heater Board was integrated as soon as it was built. It is the topmost custom board and is controlled by the heater controller (right).

7.4.1 Design Specifications

The Heater Board acts as a complement to the Heater Controller, which is a COTS module that handles the PID control of the thermal system. The one hardware element that the module does not have is the actual switches for the heaters. Instead, the module outputs 12V logic signals, intended to turn relays on or off. There are several downsides to using relays, however. For one, they are much larger than MOSFETs, as discussed in Section 4.1. More importantly, though, isolated relays cannot be sensed, or turned off in case of an emergency. The Heater Board remedies all of these issues by providing MOSFETs that are integrated with the EPS stack.

The goal of the Heater Board is to rout battery power through eight switches, allowing eight separate heater zones to be controlled. These switches must respond to 12V logic, but should also be switchable from the Arduino for testing and as a backup. The heater rails' current must be sensed, especially so that the Arduino can monitor which heaters are on when it is not directly controlling them. Other than this, the Heater Board's extra space is usable for other applications.

7.4.2 Schematic Design

The Heater Board is the simplest of the three, as can be seen in Figure 7.15. Power directly from a DC battery input is passed through two Type IV MOSFET switching circuits. This splits the input into eight separately controlled heater rails, each having a dedicated current sensor. The eight rails are immediately routed off-board to the heaters. A single unipolar ADC reads the current sensors and reports to the Arduino.

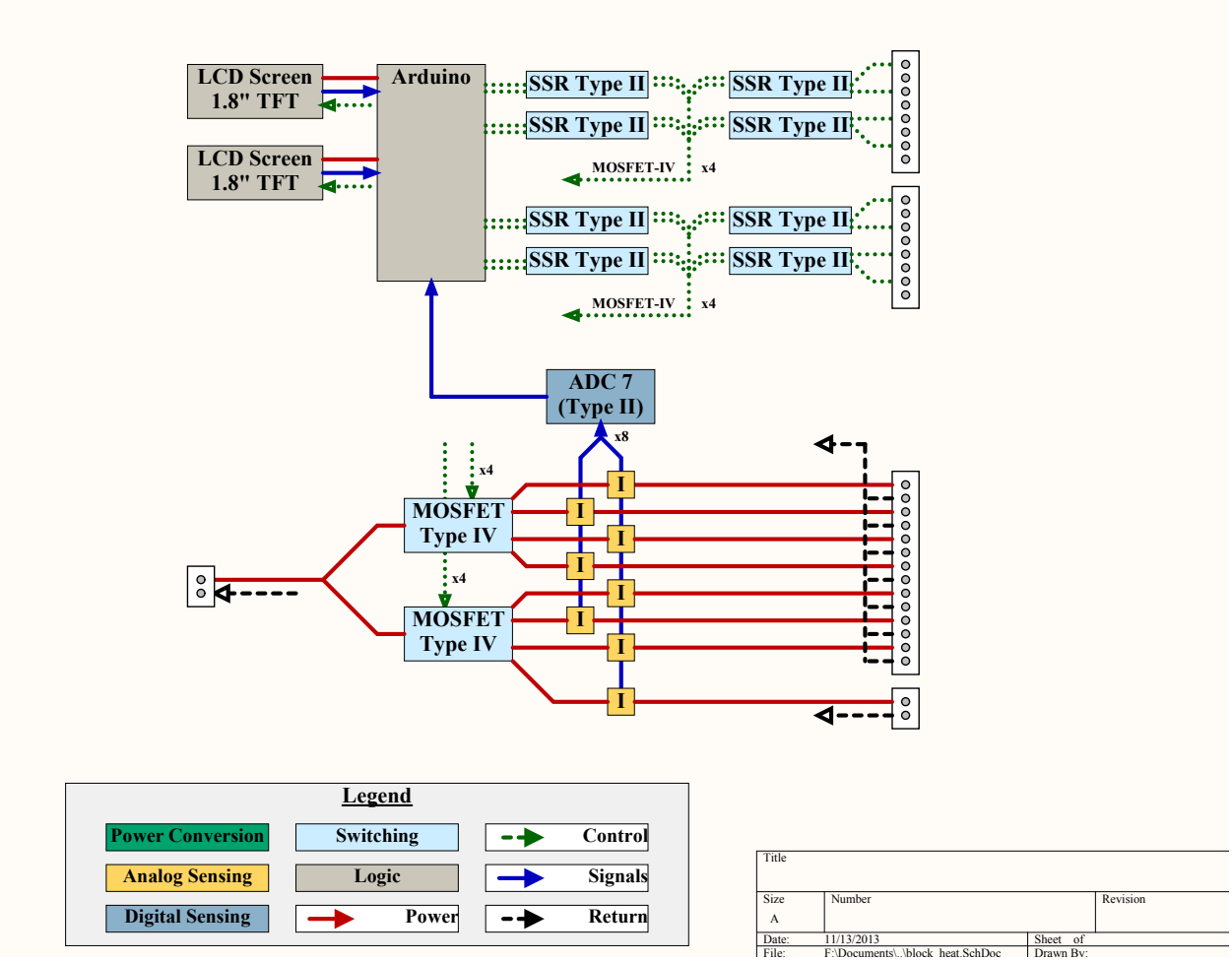

Figure 7.15: This block diagam of the Heater Control Board shows the eight heater control channels, and the shared control between the Arduino and the Heater Controller inputs.

The MOSFETs are controlled by the Heater Controller during flight. Signals from the controller, which are 12V logic and **not** referenced to the battery ground, must pass through SSRs for proper isolation. The SSRs in turn use the battery voltage as the logic driving the MOSFET drivers. In addition to this control scheme, the Arduino also has the ability to switch the heaters on and off. This was implemented for testing purposes, and is also a backup for flight in case of a failure in the Heater Controller. Similarly, the Arduino has an isolated ground. Thus, the 5V output pins drive SRRs, which in turn drive the MOSFET drivers using the battery voltage. Because the Arduino and Heater Controller **both** connect to the same control pins, the scheme is equivalent to a logical "and".

Due to the Heater Board's simplicity, there was room on the board for extra components. As integrated, the PCB was on top of the stack, so it provided a good location for system status indicators. Two LCD screens from Adafruit were selected to serve as displays and offer a degree of user interface. The screens, intended for use with an Arduino, simply mount to 0.1" headers on the Heater Board, or can be wired to the board and mounted separately. Figure 7.16 shows an LCD attached to the exterior of the ECS pressure vessel.

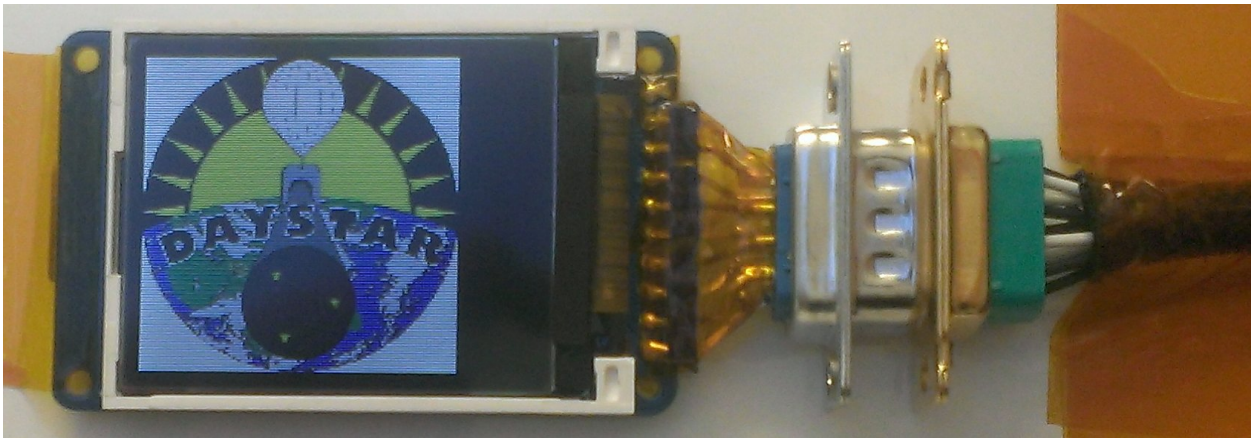

Figure 7.16: The 1.8" LCD screen from Adafruit can display text and images using a simple Arduino interface and software library.

7.4.3 Physical Layout

The layout of the Heater Control Board is as straightforward as the schematic, and only requires a 2-layer PCB. All components are on the front face of the board. Power flows from the bottom-right corner, where the battery power connector is, to the top-right corner, where a DB-25 sends seven of the eight heater rails off-board. Another connector, with more current capacity, controls the eighth line. This can be used for heaters, or can act as a switched battery supply for other components. At top-left, two DB-9 connectors accept inputs from the Heater Controller.

The Heater Board integrates to the stack using the standard Arduino footprint and four mounting holes at the corners for standoffs. Because there is no voltage conversion on-board, the Heater Board cannot independently power the Arduino. This does not prevent it from switching

the heaters, though; even without an Arduino, the Heater Board and the Heater Controller make a complete thermal control system. In the stack, though, the Heater Board gets 5V from either the Arduino or the Main Board, which adds the ability for current sensing, Arduino control and data output to the LCD screens.

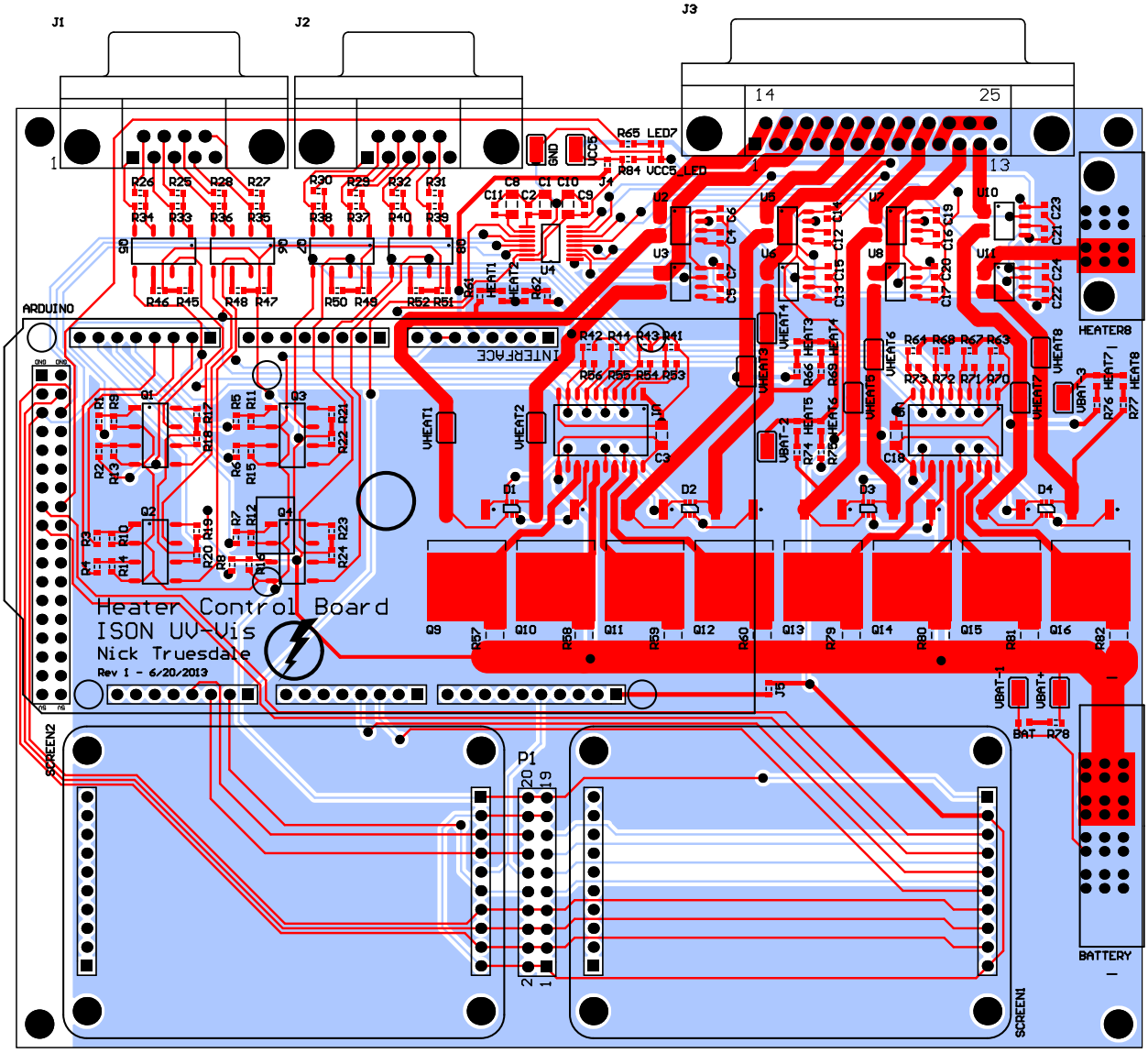

Figure 7.17: The Heater Control Board layout has all components and most traces on the front layer (red). The back layer (blue) is a ground plane, with cutouts for the remaining traces.

7.5 EPS Stack Assembly and Test

7.5.1 Assembly

Components on the three custom boards are almost entirely surface mount, and only the buck converters used to generate 5V and 3.3V require hot air to solder. The rest can be soldered by hand, making the EPS straightforward – if not at all fast – to manufacture. The most complex part of the stack assembly is not an electrical one but a mechanical one. As shown in Section 7.2.4, the Main Board's DC-DC converter bricks are mounted to an aluminum baseplate. A thermal compound such as Arctic Silver must be placed on the plate first, before the Main Board can be integrated. Once secured to the baseplate, the Main Board assembly is complete and the stack can be assembled.

The stack integration itself is made very simple by the Arduino vertical bus. Because the headers are press-fit, any sequence of boards can be placed on the Main Board just by pressing them together. In this way, the Computer Board, Heater Board and Arduino are all added. Once each board is on the stack, four standoffs between the corners of each board pair are used for added security and to take the load off of the electrical headers.

One design error became problematic during the BRRISON integration process. While the Main and Computer Boards fit together in most places, a physical interference between an inductor and a MOSFET caused a row of the vertical bus headers to be separated intermittently. The error was mitigated by removing the plastic casing of the inductor, as can be seen in Figure 7.18. This error illustrates the difficulty of designing the stack to such a short profile; care must be taken that parts have a maximum height, and the board layouts must be done in tandem.

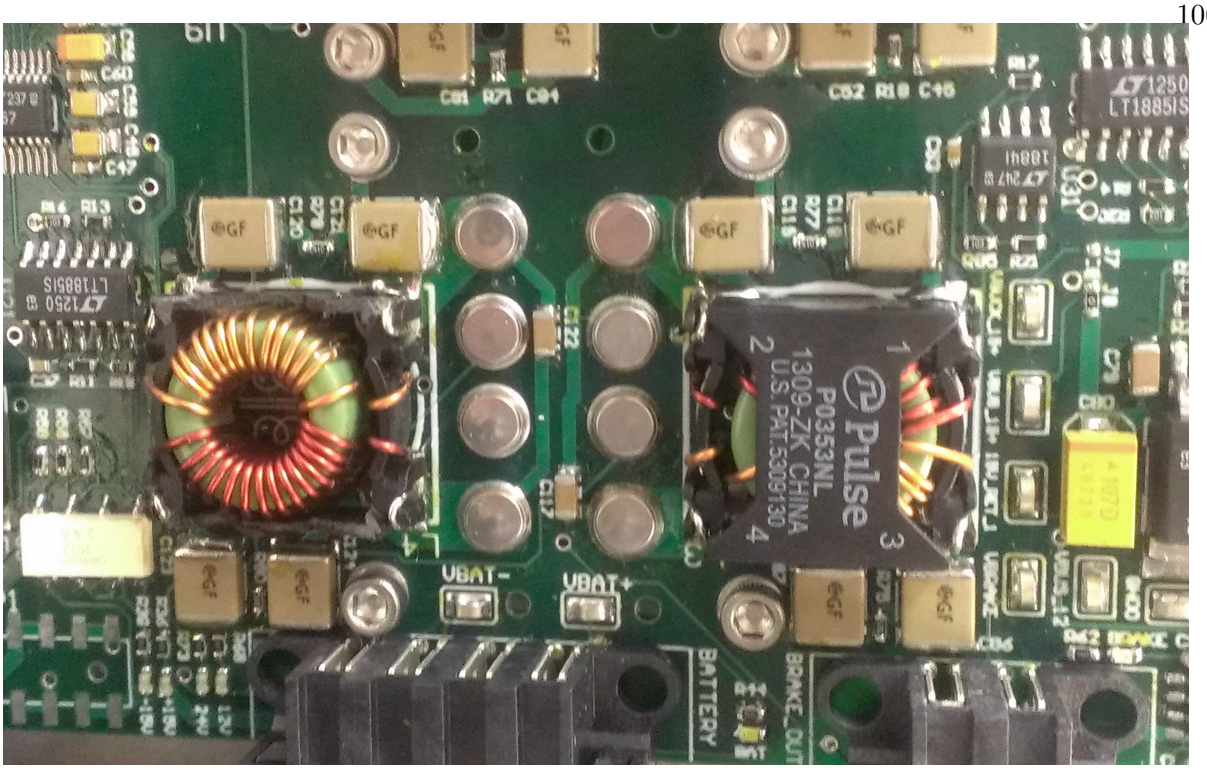

Figure 7.18: Interference between the Main and Computer Power Boards necessitated the removal of one of the inductor casings on the Main Board. This was the only assembly error in the final stack revision.

7.5.2 Voltage Conversion Results

The voltage conversion circuits on the Main Power Board saw little redesign throughout the BRRISON campaign. In the first board design, the 12V, 24V, and ±15V converter circuits produced the correct voltages, not only validating the DC-DC converters but also the filter modules and the LDOs on their respective circuits. The buck converters for 5V and 3.3V also produced the designed voltages, both on the Main Board and the Computer Board. Finally, the VME-550 worked out of the box, producing very accurate voltages with ripple below 10mVpp.

Unlike the VME-550 rails, oscilloscope measurements of the Main Board power rails were all noisy – about 100mVpp – despite the filtering and linear regulators. After the system was sealed in the flight configuration, it was learned that this is most likely due to excessive common mode noise, which, while harmless to most loads, can present itself on the oscilloscope as apparent differential

mode noise [32]. A second revision of the Main Board included the common-mode inductor filters shown in Section 3.2.3, and the improved grounding scheme discussed in Section 7.2.2.1. While this improved the measured noise, the design-to specifications could not be confirmed directly.

Without direct measurements, the converter noise on flight must be induced from the performance of the science instruments. Both cameras operated flawlessly throughout testing and flight. More importantly, though, the FSM was able to meet the designer's specification of 20 nanoradians of spatial resolution. This is only achievable with differential noise below 10mVpp. Though this does not prove concretely the performance of the converters, it indicates that common mode noise was indeed affecting measurements, and that the converter designs were effective in powering loads with strict ripple requirements. Further measurements must be taken when there is access to the system to determine the actual ripple of the converters.

7.5.3 Switching Results

Like the power conversion circuits, the MOSFET and SSR switching designs worked at a high level, though some errors needed correction before flight. The most glaring of these was the -12V computer MOSFET Type II switch, which was originally designed with an inadequate voltage divider for the input. As Section 4.2.2 notes, this was remedied by adding an SSR between the Arduino and the controller, allowing for a suitable control voltage.

Another error arose in the computer switches in the form of unintentional current limiting. With either the LT1161 or the LT1910, excessive trace length can trigger the current limit shutoff prematurely. This was causing the computer power to be cut off on start up, as the inrush current was up to 40A. To fix this, the gate sense pins were desoldered, removing this feature. Future revisions of the stack should shorten and widen the traces, so that current limiting can be used effectively.

7.5.4 Sensing Results

The current and voltage sensing circuits in the UV-VIS EPS were mostly successful, and the one major error is likely in software, not hardware. All of the current sensors output voltage correctly, though voltage offsets on the order of 50-100mV (corresponding to 250-500mA) required calibration prior to flight. The ADCs also work, both in terms of reading data and the SPI interface with the Arduino. Altogether, the data-taking chain was successful on flight, returning both current and voltage data efficiently to the Arduino. Future work on the system should address issues on specific ADC channels.

One of the Main Board's Type II ADC channels failed during testing, returning the maximum voltage of 4.096V for all readings. Whether this is due to a failed current sensor outputting 5V or a short on the ADC pin is unknown. However, all of the other Type II and Type III circuits return the correct values, indicating that the single-ended ADC design itself works.

The Type I ADC circuit used to measure the differential battery, 24V and $\pm$15V rails reads non-trivial data, but the conversion of that data to voltages returns incorrect values. Whether this is a circuit design issue or a software one is unknown, though a very similar voltage follower works well in the Type II and III circuits. Future designs should begin by verifying the differential measurement mode of the LTC1867; once this is confirmed to work, software errors are the most likely culprit.

7.5.5 Logic Results

The Arduino is the most flexible part of the EPS, because it is software configurable. However, several initial hardware modifications were required before the Arduino could be integrated with the stack. The first of these was the modification of the vertical headers described in Section 6.3.2. Additionally, a circuit on the board caused the microcontroller to restart when a USB host was introduced. While intentional in the design and necessary for programming, this led to the power system restarting as the computer booted up. An SSR was added to one of the Arduino's extra

GPIOs, so that the feature could be disabled during testing and flight. Finally, a jumper between pins 6 and 19 was added, allowing the PS_ON signal from the computer to act as a hardware interrupt.

Once it was integrated, the Arduino hardware worked flawlessly. The remaining design work was in the firmware, which is described in Section 6.3.3. The ability to configure the EPS at any time was invaluable for system testing, as it allowed the EPS to be integrated with minimal functionality early in the process. Once the computer power sequence was written, the flight computer could be used to monitor sensor outputs and test switches.

7.5.6 Overall Performance

Overall, the UV-VIS EPS was very successful during testing and the BRRISON flight. In the two months of testing between integration and flight, the power system reliably powered the optics bench without once experiencing an issue. The same reliability was seen during flight. This further validated the system, especially with regards to thermal performance. Despite the low temperatures experienced throughout all of flight – between -70°C and -40°C – the power system continued to operate within operational bounds. This was one of the key concerns that could not be truly tested on the ground, and the success of the EPS proves that a balloon power system can operate in a confined volume without requiring active thermal control.

The success of the EPS was due to the successful operation of each of the circuits discussed in this thesis. While the conversion, switching and sensing circuits all had minor issues, these were resolved during integration. The resulting circuits are now flight proven, and only minor modifications would be needed to implement them in new designs. By following the recommendations in this thesis, a fully functional EPS can be designed, manufactured, tested and flown, all in just five months or less.

Chapter 8

Conclusion

Over the past ten years, NASA's scientific balloon program has grown much closer to the goal of lofting an observatory to rival the Hubble Space Telescope. The ability to carry a 1-2 meter telescope has been proven by many payloads observing in the ultraviolet, visible and infrared. Pointing system accuracies have improved by several orders of magnitude, and are now approaching Hubble's 2-5 milliarcsecond precision thanks to the BRRISON mission's super-fine steering system on the UV-VIS optical bench. With many core technologies proven, NASA will soon be able to fly a wide array of high-performing balloon observing missions.

Future missions will feature many of the design elements of the BRRISON balloon telescope, which requires a large amount of supporting electronics. Much of this support hardware, such as cameras, actuators and thermal control, is common to all optical balloon payloads. Some electronics, however, continue to grow with system performance. Flight computers, for instance, will need to be more powerful as the complexity of imaging and pointing control increases. All of these electrical systems require power, and so all future missions will require a power system that supports both static and changing power demands.

The electrical power system for the BRRISON UV-VIS optics bench provides a foundation for future balloon electrical systems. Firstly, it supports the types of electronics that are common to balloon telescope designs. Cameras, mechanisms, and other DC instruments can be run on 12V and 24V rails. These rails are clean, with an estimated 10mVpp ripple (though this still remains to be proven directly), and have a high power capacity of up to 350W. Furthermore, the voltages

can be configured in a wide range, from 2-54V. This low-noise, high-power and configurable design allows the power system to be applied to nearly any single voltage instruments. Even in the case of a peripheral with more complex power requirements, the UV-VIS EPS provides a regulated and clean DC voltage to start from.

In addition to these main voltage rails, the EPS also supplies bipolar voltage rails. Nominally ±15V (but just as configurable as the previous rails), these power lines are intended for more complex mechanical control systems that need a negative power supply. The power capacity is up to 150W, and the ripple is again below 10mVpp. Thus, the EPS can power most individual control systems without contributing significant electrical noise. For the BRRISON mission, this is critical for driving the fast steering mirror, which provides the 10 milliarcsecond pointing accuracy. On future missions that use a mirror or similar fine pointing system, the UV-VIS EPS is a reliable, tested power source.

The third major capability of the UV-VIS EPS is the ATX computer power supply. As computational needs grow, motherboards and processors must get larger and more powerful. Fortunately, balloons support COTS electronics, and the ATX standard allows flight computers to utilize the fastest modern processors. The Computer Power Board on the EPS is a unique, DC-input power supply meant specifically for balloons. In addition to providing complex timing and switching critical to the startup and safety of ATX motherboards, the Computer Power Board also supports health and status data and programmable logic. Along with a 600W power capacity, these features make the UV-VIS applicable to almost any combination of ATX motherboard, processor, and PCIe card extensions, or even multiple computers running together. Effectively, any future mission now has the ability to select standard computer hardware to meet requirements, without worrying about the additional power needs.

While some applications can use the existing EPS hardware, others may require a new board, or a new system altogether. In this case, the circuits developed in this thesis can still be used to quickly create power designs while retaining some flight heritage. Designers in need of clean DC voltages can utilize the isolated switching converter, buck converter of linear regulator designs from

Chapter 3. If switching is needed, or if one desires to shrink a bulky relay design to a compact board-level design, the MOSFET and SSR circuits in Chapter 4 provide the means to switch any DC voltage rail below 60V. Finally, the current and voltage sensing schemes in Chapter 5 can be added to any voltage rail and are applicable to 30A.

Sometimes, a specific circuit may not be as needed as a more general design architecture. The UV-VIS EPS stack, with a vertical bus based on the COTS Arduino microcontroller, is a unique architecture that facilitates highly compact power systems. The stack provides power for the entire 600W optics bench and flight computer, all within a 5" by 6" by 3" envelope. The Arduino provides modernized embedded logic as well. Designers can transition from hardware configuration and multiple controller schemes to a simple, USB-programmable device. The Arduino condenses power system logic into a single plugable board that supports configurable software and standard serial communication. Thus, the EPS architecture reduces both design time **and** programming time.

While many of the circuits and boards in the UV-VIS EPS were proven to work before and during flight, several improvements can be made to future designs. In the power conversion circuits, common mode noise prevented definitive performance measurements. Designers should invest in differential probes and be cognizant of how noise permeates a voltage rail and load. The MOSFET switches worked, but more complex capabilities like overcurrent and inrush current protection require careful PCB layout and, in some cases, simple filters matched to the capacitance of the load. The sensing designs also performed on flight, but with some software errors that hampered current and voltage measurements. Future designs may require more complex op-amp conditioning circuits, both to improve voltage buffering and to remove noise from current sensor outputs. Finally, some of the mechanical design of the boards and stack needs to be reworked to prevent physical interference and loose connections.

The UV-VIS EPS is remarkable for two reasons. Firstly, and most tangibly, the system as-built supports the power requirements for a high-performance balloon telescope. It can be used for future flights of BRRISON, but is also extensible to new missions that use similar hardware. The

second achievement of the EPS lies in its potential to reduce design time and effort for brand new systems. The modularity of the power conversion, switching, sensing and logic circuits discussed in this thesis allows them to be dropped into new **or** existing board designs. Designers can use these flight-tested circuits in place of custom designs, alleviating much of the difficulty in building a balloon power system from scratch. Thus, whether the UV-VIS EPS flies again or is simply used as a reference, it stands to have a profound effect on NASA's future balloon observatories.

Bibliography

[1] ATX/ATX12V Power Supply Design Guide. http://www.formfactors.org/developer%5Cspecs%5CATX_ATX12V_PS_1_1.pdf, August 2000.

[2] Dwight Bawcom. A short history of the NSBF (CSBF). http://stratocat.com.ar/artics/nsbf-history-e.htm.

[3] Andy Cheng. Mission to catch comet ISON. www.boulder.swri.edu/NSRC2013/Site2/PDF/Cheng_abstract.pdf, 2013.

[4] NASA comet ISON observing campaign. http://www.isoncampaign.org/.

[5] Mark Devlin. BLAST: Balloon-borne Large-Aperture Submillimeter Telescope. http://blastexperiment.info/.

[6] C. K. Walker et al. The stratospheric tetrahertx observatory (STO): An LDB experiment to investigate the life cycle of the interstellar medium. In International Symposium on Space Tetrahertz Technology, volume 19, 2008.

[7] Charles A. Hibbitts et al. Stratospheric balloon missions for planetary science: A petition for the formation of a working group to study the feasibility of a facility platform to support planetary science missions. http://www.lpi.usra.edu/decadal/sbag/topical_wp/CharlesAHibbitts.pdf, 2009.

[8] J. W. Dankanich et al. Planetary science balloon based platform assessment. In Lunar and Planetary Science Conference, volume 44, 2013.

[9] Jason Rhodes et al. Space-quality data from balloon-borne telescopes: the High Altitude Lensing Observatory (HALO). Astroparticle Physics, 2012.

[10] Wallops Flight Facility. NASA super-TIGER balloon shatters flight record. http://www.nasa.gov/centers/wallops/news/supertiger-record.html, January 2013.

[11] Wallops Flight Facility. Super pressure balloons. http://sites.wff.nasa.gov/balloons/uldb.html, June 2013.

[12] Space Telescope Science Institute. HST pointing accuracy and stability.

[13] Texas Instruments. Buffer op amp to ADC circuit collection. http://www.ti.com/lit/an/sloa098/sloa098.pdf, March 2002.

[14] Henry M. Cathey Jr. and David L. Pierce. Development of the NASA ultra-long duration balloon, 2007.

[15] Gregory Kennedy. Stratolab, an evolutionary stratospheric balloon project. http://stratocat.com.ar/artics/stratolab-e.htm, September 2013.

[16] Tibor Kremic. Planetary science from a balloon-based observatory – an update. http://www.lpi.usra.edu/opag/jan2013/presentations/Friday/09_Balloon%20Status.pdf, January 2012.

[17] Tibor Kremic. Planetary science from a balloon-based observatory – an update. http://www.lpi.usra.edu/sbag/meetings/jan2013/presentations/sbag8_presentations/MON_1600_Balloon%20Status_RL.pdf, January 2013.

[18] Johns Hopkins University Applied Physics Laboratory. BRRISON: Balloon Rapid Response for ISON. http://brrison.jhuapl.edu/.

[19] Allegro MicroSystems. ACS712 Fully Integrated, Hall Effect-Based Linear Current Sensor IC with 2.1 kVRMS Isolation and a Low-Resistance Current Conductor. www.allegromicro.com/en/Products/Current-Sensor-ICs/Zero-To-Fifty-Amp-Integrated-Conductor-Sensor-ICs/ACS712.aspx.

[20] NASA. Columbia Scientific Balloon Facility. http://www.nsbf.nasa.gov/.

[21] NASA. NASA Stratospheric Balloons: Pioneers of space exploration and research. Technical report, NASA Scientific Ballooning Planning Team, October 2005.

[22] Aegis Power. VME550-001: VME DC-DC Power Converter Card. http://www.aegispower.com/images/product-spec-sheets/VME550-001%20Spec%20Sheet.pdf.

[23] Linear Technology. LMZ22005 5A SIMPLE SWITCHER Power Module with 20V Maximum Input Voltage. http://www.ti.com/lit/ds/symlink/lmz22005.pdf.

[24] Linear Technology. LT1185: Low Dropout Regulator. http://cds.linear.com/docs/en/datasheet/1185ff.pdf.

[25] Linear Technology. LT1764A: 3A, Fast Transient Response, Low Noise, LDO Regulators. http://cds.linear.com/docs/en/datasheet/1764afb.pdf.

[26] Linear Technology. LT1884/LT1885 Dual/Quad Rail-to-Rail Output, Picoamp Input Precision Op Amps. http://cds.linear.com/docs/en/datasheet/1884fs.pdf.

[27] Linear Technology. LT1910 Protected High Side MOSFET Driver. http://cds.linear.com/docs/en/datasheet/1910fa.pdf.

[28] Linear Technology. LTC1163/LTC1165 Triple 1.8V to 6V High-Side MOSFET Drivers. http://cds.linear.com/docs/en/datasheet/lt1163.pdf.

[29] Linear Technology. LTC1863/LTC1867 12-/16-Bit, 8 Channel 200ksps ADCs. http://cds.linear.com/docs/en/datasheet/18637fa.pdf.

[30] Vicor. Design Guide & Applications Manual for Maxi, Mini, Micro Family DC-DC Converter and Accesory Modules. http://cdn.vicorpower.com/documents/applications_manual/fas_trak_apps_manual.pdf.

[31] Vicor. MicroRAM Output Ripple Attenuation Module. http://www.vicorpower.com/documents/datasheets/Picor/ds_microram.pdf.

[32] David A. Weston. Electromagnetic Compatibility: Principles and Applications. Marcel Dekker, 2 edition, 2001.

[33] Don Woligroski. Power Supply 101: A Reference of Specifications. http://www.tomshardware.com/reviews/power-supply-specifications-atx-reference,3061.html, December 2011.

[34] Eliot F. Young. Sub-arcsecond performance of the ST5000 star tracker on a balloon-borne platform. http://www.boulder.swri.edu/~efy/efy_talks/ST5000_NSC_v01.pdf.

[35] Eliot F. Young. HST-like performance from balloon-borne telescopes. http://www.boulder.swri.edu/~efy/efy_talks/EFY_BalloonObs_v01.pdf, February 2012.

[36] Eliot F. Young, Charles Hibbits, Joshua Emery, Amanda Hendrix, William Merline, William Grundy, and Kurt Retherford. Balloon-borne telescopes for planetary science: Imaging and photometry. http://www.lpi.usra.edu/decadal/sbag/topical_wp/EliotFYoung.pdf.