A Methodology for Characterizing and Modeling Inverters for Grid Integration Studies using Power Hardware-in-the-Loop

by

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This thesis entitled:

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The final copy of this thesis has been examined by the signatories, and we find that both the content and the form meet acceptable presentation standards of scholarly work in the above mentioned discipline.

Abstract

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A Methodology for Characterizing and Modeling Inverters for Grid Integration Studies using Power Hardware-in-the-Loop

This thesis directed by Professor Dragan Maksimovic

A methodology is proposed and executed to characterize and model inverters for grid integration studies using Power Hardware-in-the-Loop. A Hardware-in-the-Loop system is configured using a Real-Time Data System (RTDS), grid simulator, load bank, photovoltaic inverter and bus system. A characterization scheme is developed on the RTDS that is based on the abnormal grid conditions and tests outlined in IEEE 1547 Standard for Interconnecting Distributed Resources with Electric Power Systems. The RTDS is then used to control both the grid simulator and load bank. It was found that it is possible to characterize the inverter's grid protection controller's response to abnormal voltage, abnormal frequency and islanding conditions without prior knowledge of intimate control algorithms or hardware configuration.

A model of the system was then created in Matlab Simulink using the data obtained from the characterization process. The inverter is modeled on a high level as a controlled current source and a controller for the inverter model is developed such that the detection and response to the stated abnormal grid conditions of the model directly mimics that of the actual inverter.

Dedication

This work is dedicated to those who expend tireless effort

making the world a more sustainable place,

for all living creatures.

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1 Introduction

An area electric power system (EPS) has traditionally consisted of a primary generation source, such as a coal-fired power plant, a transmission and distribution system and a distributed load. Changes to this system have become more prevalent as distributed resources (DR), such as wind turbines, diesel generators, natural gas turbines and photovoltaics (PV) have become more available and affordable. In order to preserve the safety and reliability of the EPS, testing of grid-connected devices is essential. Standards, such as IEEE 1547 and UL 1741, have been developed to provide requirements for grid-connected DR systems. IEEE 1547.1 defines methods for testing devices to determine if they comply with the standards. These tests can be used to characterize a DR without any knowledge of the controller or hardware that causes the DR to function. Once the DR has been characterized, a software model can be constructed from the results and used in a multitude of environments to test issues related to grid integration. Many different methods can be used to perform these tests and characterize DRs, each having its benefits and drawbacks, but Hardware-In-the-Loop (HIL) provides a unique methodology that is extremely flexible and powerful.

This chapter will introduce issues associated with DR integration, relevant research that has been conducted, a brief overview of the system used for this thesis, the motivation for this project and a summary of what will be completed.

1.1 The Changing Electric Power System

The electric grid was built in a way that strongly supports centralized generation. The high voltage lines that carry bulk power are focused around major generation centers. Regulation and financial incentives tend to benefit large-scale, consistent, dispatchable generation. These centralized generation sources use a narrow scope of fuels making them vulnerable to supply issues. A few of the

most prominent examples of fuel for electricity generation are coal, natural gas and nuclear. In 2010, coal accounted for 45% of electricity generation in the US. Natural Gas made up 23% and nuclear 20% for a total of at least 78% of electricity generation coming from centralized facilities [**1**]. The benefits of large-scale, reliable power plants are what has caused them to be such an attractive resource for so long. In the past, these fuels have been readily available and cheap, but wars in the Middle East and increased demand by quickly advancing nations, like China and India, are causing their supply to become stretched. Centralization reduces land permitting issues and eases operation and maintenance by having most of the machinery located in one place. Consistently available fuel yields a very controllable power source that can be increased or decreased on demand. These conditions have led to a successful EPS for most of the world for many years.

Environmental and security concerns are contributing to a change in the structure of EPS's. The Intergovernmental Panel on Climate Change, an international body of scientists, has been publishing reports since 1990 detailing the dangerous climactic impacts of burning large amounts of fossil fuels such as coal and natural gas. Also, procurement methods for coal, natural gas and nuclear fuel are well known environmental hazards. In addition to these environmental concerns, a number of security-related issues have become prominent. Unanticipated events, be they natural or unnatural, could have grave consequences for centralized generation sources because so many people rely on them. Of particular concern is the vulnerability of centralized generation sources to terrorists and mother nature. The recent earthquake in Japan demonstrated the vulnerability and repercussions of a failed nuclear power plant. In light of these issues, governments have begun to mandate increased usage of renewable energy resources through documents called Renewable Portfolio Standards in the US and Renewables Obligation in the UK. The goal of these policies is to mitigate many of the problems associated with centralized generation by increasing the amount of generation from renewable resources. These documents require a certain percentage of generation to come from renewable

resources such as solar, wind or geothermal. These resources, in addition to other generation and storage sources, are commonly labeled DRs because they are not part of a centralized power generation center. DRs are defined by IEEE 1547 as generation sources, such as synchronous machines, induction machines, or power inverters/converters with a power rating less than 10 MVA. Implementation of these DRs is contributing to a change in grid infrastructure and operation.

DRs are not meant to immediately replace centralized generation sources, but rather to gradually augment the system. They can have many benefits to the grid financially and technically. One example is load shaving. When the sun is shining during the day the temperatures are high and thus air-conditioner use is prevalent. The energy that the sun provides to heat the earth can also be captured to generate electricity, using Photovoltaics or Concentrated Solar Thermal Power (CSTP), and offset part of the high electricity demand used to cool buildings. This reduces the amount of costly ancillary services that are necessary to meet the load. Also, if the electricity produced by PV or CSTP from the sun was not being consumed, it may be stored and used at other times or as a backup resource during outages. Another example is easing augmentation of the grid. In a centralized generation scenario, if a new load center is built, transmission lines that have the capacity to support the demand of the new load center must be built. This can be a costly procedure that is complicated by land rights issues. DRs solve this by being easily geographically distributed. The energy can be generated on site, thus reducing the need for large transmission lines. This aspect, in addition to diversified fuel resources and modularity of generation systems, creates flexibility in power distribution and grid infrastructure.

Unfortunately, introduction of DRs to the grid can have unwanted effects that may jeopardize the reliability and quality of electricity on the grid. One area of distributed generation (DG) that is receiving a lot of attention is renewable. Recent political activity and public interest has caused an increase in the amount of renewable resources attached to the grid. The variability and

nondispatchable nature of these resources is a major concern to utility engineers. If the sun goes behind a cloud or the wind ceases to blow, generation will drop and if back up sources cannot react quickly enough grid instability could result and possibly causing the grid to fail. Many studies have been performed to identify and analyze the effects of DRs on the grid. One extensive report describes common grid problems such as, voltage fluctuations, voltage rise, reverse power flow, power fluctuation, impacts on power factor, frequency regulation, harmonics, unintentional islanding, fault currents and grounding issues and how they are associated with the interconnection of DRs [**2**]. This report also goes on to describe how DRs can be best implemented in the current grid structure with respect to said issues, though it states that much more research is needed. The National Renewable Energy Laboratory (NREL) commissioned a more technical report to analyze the impacts of high penetration of PV on the grid [**3**]. A wide range of relevant issues were studied including PV system design, effects on transmission, and distribution system voltage performance. Many gaps in the research are also identified. Other studies more focused on PV system design were also conducted. [**4**] examined the controls and storage necessary for optimization of PV systems. The common conclusion to all of these studies is that more research needs to be conducted to further determine the effects of higher penetrations of DRs. Each report specifically identifies inverters as a source of many unknowns. They state that more modeling tools to simulate these issues and determine their effects are required if high penetration of DRs is to be accomplished. Also, the amount of variability in an EPS with DRs is great. Since DRs can be installed at different points in the EPS, known as points of common coupling (PCC), an incredible number of variations in system configuration are possible. A model of one local EPS may not sufficiently model another. Testing must take place to prevent failures and identify issues introduced by DRs. A flexible testing and modeling system is needed to determine the effects of DRs on the grid.

Microgrids are another area where extensive modeling is required. A microgrid is a group of generation sources and loads that has the ability to disconnect from the EPS. The ability is referred to as islanding. Once the microgrid disconnects and becomes an island, the dynamics of power flow, power quality and control can change. Test beds have been constructed that model microgrids [**5**], [**6**]. It is clear that testing the variable configuration of microgrids is an issue that must be addressed by a flexible and powerful simulation system.

In an attempt to maintain quality and safety on the grid, IEEE and UL have both introduced standards, IEEE 1547 and UL 1741 that define regulations for grid-connected devices. These standards mandate that DRs must cease to energize the grid if various conditions such as abnormal voltages, abnormal frequencies or islanding conditions occur. DRs are not allowed to provide any type of voltage regulation [**7**]. This is a very important point as it requires DRs to act as current sources. The DRs are in effect, slaves to the voltage and frequency of the larger EPS. If a condition were to occur where the DRs were required to cease to energize the grid, a large drop in power could result and cause a cascading failure in other areas as described in [**8**]. These issues become more important as DRs become more wide spread. On the other hand, [**3**] suggest that if DRs were not required to disconnect whenever the grid experienced troubles they could provide support and possibly prevent outages. Before any new scheme can be implemented, though rigorous testing must take place to ensure that it will be safe, stable and reliable.

1.2 Relevant Research

Various grid integration testing has been conducted on PV systems. The authors in [**9**] modeled and simulated a grid-connected PV inverter using IsSPICE with the purpose of studying strategies for reducing total harmonic distortion (THD) and increasing power factor. An AC power supply was used to simulate the grid. Two different grid voltage models were used to control the power supply, one based

on an ideal sine wave and the other based on sampling of the actual utility grid. THD was measured for various power outputs of the inverter.

A model of an inverter using key performance parameters was developed by researchers at Sandia National Laboratories [**10**]. These parameters, mainly consisting of power and voltage ratings, were determined both from manufacturer's specifications and lab and field testing. The model that resulted was intended to be used for systems analyses and determining degradation of field inverters in real-time.

Since actual utility grids can rarely be used for testing, grid simulators are a key component to testing grid-connected PV inverters. In [**11**] the authors designed, in PSCAD, and constructed a grid simulator to produce waveforms to test grid-connected renewable energy systems. It provides an indirect connection to the utility grid so that DR can be connected safely. It was shown that abnormal grid conditions, balanced transient grid conditions, and unbalanced transient grid conditions could all be simulated using the grid simulator constructed.

A detailed model of inverters for studying transient issues related to grid integration was developed in [**12**]. Functionalities such as PWM switching, a current controller, a power controller and anti-islanding detection were all modeled in PSCAD/EMTDC. Also modeled were the grid, grid interface and PV array. Maximum power point tracking (MPPT), anti-islanding, current harmonics and fault conditions of the model were all analyzed.

In [**13**], a protection device for a grid-connected, transformerless PV inverter was tested. A real-time data system (RTDS) was used to simulate the output of a PV array and the utility grid, though how this was done was not discussed. MPPT, anti-islanding and voltage degradation capabilities of the protection device were all tested with a real inverter.

An RTDS was also used to study the effects of PV integration into a relatively small grid on the island of Lanai in [**14**]. The 5.5 MW grid was modeled in Simulink and stability and power flow control tests were performed for various control schemes and weather conditions.

1.3 Motivation

Each of these projects seeks to serve the need for modeling or testing integration of PV onto the utility grid. Most provide detailed modeling of switching control or power control. These control schemes are rarely available to users not affiliated with the developers. There needs to be a way to model these inverters interaction with the grid without the need to obtain detailed models of the inverters so that grid integration studies can be performed and PV can be integrated safely.

DRs can have a wide range of characteristics and thus integration with the larger EPS is rife with complex issues. To mitigate these issues, a separate simulated system can be built to test the effects of connecting new devices. These simulated systems function the same way as the actual system so results from the testing system may be reliably applied to the original system. At the power levels necessary to achieve this, cost of the components, space required to build a simulated system and the time it would take to ensure a safe and reliable system are three main prohibitive factors. Also, integrating the components in a way that mimics an actual EPS could create significant problems. The actual hardware could be used to obtain exact results. But if this approach were to be taken, the system would most likely be inflexible and limited in the scope of variations in testing. In contrast, a Hardware in-the-Loop (HIL) system provides an easily configurable and very flexible way to simulate and test an EPS that correlates well with actual utility systems. Rather than use the actual components, power amplifiers and load banks that can be easily controlled through HIL can be used to simulate them. With the correct set-up other equipment can be seamlessly integrated as if the HIL system were an actual EPS. In addition to a flexible hardware configuration, HIL makes simulating the components of the EPS easily

achievable by using common programming languages and centralized command. This reduces costs, space and time requirements.

1.4 HIL Overview

An HIL system generally consists of three main parts: the device being tested, the system being simulated and the interface between the two. An RTDS acts as the brain of the whole system. The simulation occurs in the RTDS which then outputs the simulated data or set points to the actual hardware. Power flow and feedback are two examples of parameters that can be controlled by the RTDS. HIL can be divided into two categories, Controller Hardware in the Loop (CHIL) and Power Hardware in the Loop (PHIL). CHIL systems generally simulate devices such as power electronics while keeping the controller hardware physically present in the loop. An example of which can be seen in [**15**]. PHIL systems differ from other HIL systems because the components require large amounts of power, generally in the kW range, which necessitates amplifiers and other interfacing devices capable of handling high voltage and current. An example of PHIL testing can be seen in [**16**]. Many different systems have been tested using HIL. Wind turbine controllers were tested in [**15**]. The HIL system allowed for these controllers to be tested with an actual wind turbine present. In [**17**] an HIL system was used to simulate dynamics in a DC zonal distribution system. Issues with scaling HIL systems up to high power are explored, as well as producing accurate time-domain software models of actual components. Another test using HIL was performed by a research team in France to determine the effects of distributed energy storage sources, such as ultra capacitors, on the power system of the small island of Guadeloupe [**18**]. Power electronics testing has also been performed using HIL in [**13**]. Finally, a study was conducted on the measurement accuracy of HIL [**19**].

The scope of a PHIL system is limited by the capabilities of individual components. Scaling systems up to larger power levels has been a topic of research since 1994 when one of the first PHIL

systems was developed by Mitsubishi and Tokyo Electric Power engineers. In [**20**], they describe the digital to analog interface between the power amplifiers and real-time digital simulator.

The large devices used to recreate an EPS for testing must be controlled in such a way that they act like the actual system. Programmable controllers with advanced user interfaces for system components such as a load bank or power amplifier have existed for a while. Unfortunately most contain their own proprietary software and are limited to controlling a specific piece of equipment. HIL eases the control of multiple devices by allowing the user to integrate all of these controllers into one program, using one software language, and one machine. The developer does not need to learn new programming languages or adapt to new interfaces with each new device. Control is centralized and co-mingled. Simple analog or digital input and output ports can be configured once and reused for multiple applications. Extensive libraries can be constructed and referenced easily by users with different skill levels and different application goals. These features make HIL a very attractive and approachable system for a wide range of users.

When the major components of an EPS have been successfully implemented in a simulated system, it is often desirable to introduce other elements. Power electronics, more specifically inverters, are of particular interest to many utility engineers due to the rapid increase of renewable resources. Conventional testing of renewable resources requires the presence a PV panel or wind turbine and sunshine or wind. The intermittent availability of solar irradiance or kinetic wind energy can greatly hinder testing. It also is very difficult to get repeatable scenarios. In HIL these systems can be characterized and modeled through software. Outputs from the software using a D/A channel can then be used to control an amplifier which will mimic the previously uncontrollable element. Many scenarios can then be simulated and repeated on command which will contribute to a flexible and powerful testing system. It is no longer necessary for PV or wind energy systems to be physically present or if

they are, for the weather to be in a desired state for testing to occur. This reduces infrastructure and reduces time required for testing, both of which save money.

Also, power electronics technology is constantly evolving at a rapid pace. New control algorithms and discrete components emerge constantly and must be tested before being implemented in an EPS. The inflexibility of utility scale test beds can be a great hindrance when it comes to frequent and somewhat unpredictable testing. With each new development in devices, the set-up may have to be modified, costing time and money. HIL provides a way to reduce these costs by using a software model developed for the power electronics. The model can be easily modified without making any costly hardware changes. The same applies for any generation source, etc. that can be modeled in software.

Device characterization and then modeling can be a tedious process that requires a lot of the person performing the characterization's time. For example, when characterizing a grid-connected inverter, there is a wait time before the inverter will make an electrical connection with the grid and begin to export power. This time can be on the order of five minutes for grid-tied PV inverters [**21**]. Each time a condition is created by the user that causes the inverter to trip offline, five more minutes must elapse before another test can be performed. This is valuable time that the engineer performing the tests could be using for other important tasks. HIL systems, through the use of scripting software, can fully automate tests. Feedback loops can be used to inform the software when to perform a new test or if the test needs to be repeated. A device can be characterized in a reduced amount of time because the machine will know exactly when to perform the tests. Also, minimal monitoring or interference is needed. Automation of the characterization process greatly reduces the amount of time and effort required.

In summation grid-interconnection characteristics must be tested to ensure safe and reliable operation of an EPS. Conventional testing systems can be bulky, costly and inflexible. HIL solves many

of these issues by creating a system where testing can be easily and efficiently performed. Characterization of hardware, and the software models that result, can greatly reduces cost in time, infrastructure, space and money. The impacts of these tests can lead to more robust and reliable systems. HIL provides an easy and flexible way to perform characterization. In addition to these benefits, HIL is also attractive because it has a wide range of applications, it is very versatile and it is easy to learn and develop powerful skills.

1.5 Statement of Work

This thesis documents the hardware configuration, software coding, testing performed and characterization and modeling of a grid-connected PV inverter using PHIL. It begins with information on PV systems and the IEEE 1547 interconnection standard in Chapter 2. It then describes the HIL set up and how the various components were simulated in the first part of Chapter 3. Chapter 4 details the testing procedures and shows results from characterization tests. The PV inverter characterization data is used to create a model of the system in Chapter 5. The model is validated against the results from the characterization tests in the later part of Chapter 5. Finally, conclusions and recommendations are made in Chapter 6. Additional information, such as software code and an index of abbreviations, is available in the appendix. The information from this thesis can be used to obtain valuable grid-integration information that could be of great use to utility, power electronics and system design engineers.

2 Photovoltaic Systems and IEEE Standard 1547

PV systems have recently been installed in large numbers. The interface between a PV system and the EPS is typically an inverter with certain controls that facilitate power flow between the PV panels and the EPS. Due to the high penetration of PV systems, a PV inverter will be characterized for grid integration studies.

There are many different issues that could be studied with PV inverters. The scope of the characterization and modeling performed in this thesis will be limited to a few of the main issues discussed in IEEE 1547 Std. This document has become the industry standard for requirements for grid-tied DR and thus most grid-tied DR have some sort of protection that meets these standards.

This chapter provides background on PV systems and IEEE 1547. Integration issues, system configurations and requirements will be explored.

2.1 PV Systems

PV panels convert radiation from the sun into electricity using semiconductors. They can be arranged in strings to obtain different voltage levels. These strings are then arranged in parallel to form an array. The electricity they produce is in the form of DC. The PV output DC current must be shaped into an AC waveform by a PV inverter. Its voltage, frequency and phase angle must be synchronized with the 60 Hz waveform of the grid and the total demand distortion must be kept less than 5% [**22**]. A typical configuration for realizing a grid-tied PV inverter system is to use a DC/DC power converter to step-up the voltage from a PV array and provide maximum power point tracking (MPPT). This higher DC voltage is then shaped into an AC waveform using an inverter. The output is filtered and synchronized with the grid in the final stage before being connected. There have been systems developed that accomplish all of these functions in a single stage [**23**].

2.1.1 Inverters

Inverters are electrical devices that convert direct current (DC) to alternating current (AC). They have a wide range of applications including, variable speed drives, power factor correction and grid-tied distributed resources. They also come in various configurations, such as single-level or multi-level, voltage source or current source, each yielding different features [**24**], [**23**]. One common application of inverters is with PV systems. The recent increase in penetration of PV generation on the EPS has driven higher levels of research and development of single-level grid-tied inverters [**25**].

2.1.1.1 Hardware

Inverters come in a wide variety of topologies, each having its own weaknesses and strengths. There are three high level categories for inverter topologies: central, string and module integrated inverters [**26**]. Central inverters are the most basic. The PV system consist of an array of PV panels that all feed through one centralized inverter to the grid. While the simplicity of this topology has its benefits, it also has a number of disadvantages. The entire system hinges on one inverter. If there is a problem with the inverter, the system goes offline until the inverter can be repaired. Another drawback is the lack of effective MPPT. Each PV panel could be shaded differently, but the centralized MPPT only functions for the whole array. Also, the lack of any localized inverter requires expensive DC cables to transport power between panels [**27**].

String inverters solve some of the problems associated with centralized inverters; while at the same time, utilize their cost reducing configuration. This topology is realized by placing an inverter on each set of series connected PV panels. This allows for the inverter control to be tailored to each string, rather than the whole array. Though this is still a subject of research [**28**], it is generally accepted that shading effects are reduced and more power can be extracted from the array. String inverters also reduce the amount of DC wiring needed compared to centralized inverters since the DC to AC conversion takes place at each string. These topologies typically do not need transformers [**27**]. Since

the PV panels are placed in series, various voltage levels can be achieved. Multi-string configurations present another alternative [**27**]. This topology involves placing DC-DC converters on each string, then feeding multiple strings into one inverter, thus allowing for localized MPPT and reducing the number of inverters needed.

Module integrated inverters, also called microinverters are intended to be used with individual PV panels instead of the whole system or a string of panels. This allows for more specific control schemes, smaller components and higher flexibility with PV array configuration. MPPT can be unique to a single panel, providing greater power extraction. The lower power level at which they operate allows for smaller components to be used. One of the most recent developments in module integrated inverters is to incorporate all of the components needed into one board that can be installed on the back of a PV panel. For example, [**29**] presented a 3 mm tall, 95% efficient microinverter to interface building integrated PV to the 120 V_{ac} single phase utility grid. As can be seen from this example, module integrated inverters operate at lower powers, but still yield high efficiencies.

Various types of transformers can be used in each of these topologies. Line frequency transformers are an older technology. They are used to step the output of the inverter up to utility scale voltages. Operating at line frequency, these transformers must be extremely bulky in order to prevent saturation. Also, line frequency transformers are known to operate with low power quality, which was a major factor in driving new topologies in inverters [**27**].

Another, more recent, design is to implement a multi-stage inverter that uses a DC-DC converter with a high frequency transformer. Multi-stage designs use DC-DC converters to boost PV panel voltages to utility voltages. This is especially useful in module integrated inverters that operate at lower voltages because it eliminates the need for larger line frequency transformers. The DC-DC stage can also be used for current shaping, as discussed in [**30**].

These converters can also be realized without a transformer. This is particularly attractive in string and multi-string inverters that already supply the necessary voltage to be put on the EPS. An unfortunate downside to transformerless topologies is that the design does not meet safety standards in some countries [**26**]. In the US, the NEC section 690 was recently updated to allow for ungrounded PV systems. This allows transformerless converters to be used, with a few protection requirements such as disconnects, overcurrent protection and ground-fault protection.

The grid-tied PV inverter, along with other devices, plays a crucial role in synchronization, protection, power quality and efficiency. Various interconnection issues must be addressed to protect the larger EPS from being affected by these inverters. IEEE 1547 outlines these issues and provides requirements for interconnection of distributed resources [**22**]. Number of stages, grid interconnection, and transformer type are considerations that allow for a multitude of inverter topologies. Many single phase inverter topologies can be found in [**23**], [**27**] and [**26**]. Converters are summarized in [**27**] and the most effective are identified for different situations. It recommends high frequency transformers for almost all topologies. Multi-stage configurations are recommended for inverters that need to increase the voltage output of PV panels or strings such as module integrated or string inverters.

2.1.1.2 Connection to EPS

Another issue that must be taken into consideration when designing a grid-tied PV system is how the inverter will connect to the grid. The type of connection dictates what kind of inverter can be used. Typical inverter configurations are single-phase and 3-phase. Single phase inverters are used for low power and residential applications. Homes are typically fed by a pole transformer that utilizes a split-phase configuration. Pole transformers are fed with a single phase of the 3-phase distribution system. Split-phase operation involves connecting three wires to the single phase transformer. Two wires are connected across the secondary and a third is connected to a center-tap on the winding. The waveforms V1 and V2 are 120 V_{rms} and 180° out of phase. Therefore, when they are summed 240 V_{rms}

results. This higher voltage reduces the current rating and thus the size of the wires necessary. A diagram of this concept can be seen in Figure 2-1.

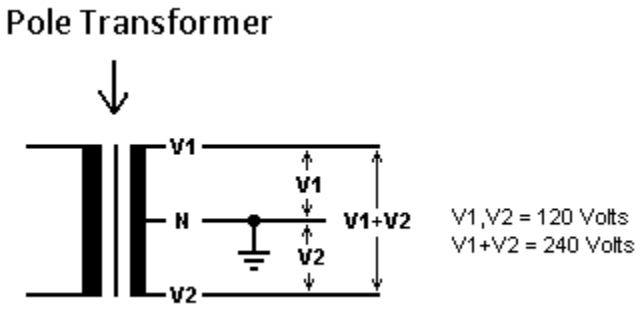

Figure 2-1 Residential Split-Phase Configuration

Larger installations, like solar farms, generate larger amounts of power. Also, they may have access to a 3-phase connection and thus can utilize a 3-phase inverter configuration. 3-phase inverters can be composed of three single phase inverters to handle larger amounts of power.

2.1.1.3 Controller

Grid-tied inverters also must have special control systems that constantly monitor grid conditions. IEEE 1547 explicitly states that inverters are not permitted to provide voltage regulation. If the EPS fails and an islanding condition occurs, the inverter must detect the failure and disconnect from the EPS. They accomplish this through an anti-islanding controller. These controllers may be either passive or active. Passive protection involves monitoring grid conditions while active protection involves injecting errors and measuring the response [**31**]. In the case of a microgrid, islanding inverters may be implemented. These inverters do not employ anti-islanding controls and will continue to provide power to the microgrid if the EPS fails.

A complete EPS failure is not the only reason a PV inverter must disconnect. Abnormal operation conditions can indicate problems. Limits on the amount of variation in operating conditions are defined by IEEE 1547. The inverter controllers must be able to detect, to a certain degree of

accuracy, parameters such as voltage and frequency and determine when to trip. In certain scenarios, where the voltage doesn't deviate a great deal, the inverter is allow to continue normal operation for a longer period of time. This function is called ride-through. The assumption is that this aberration is minor and likely temporary and therefore not sufficient enough to necessitate a disconnection.

2.2 IEEE 1547 Standard for Interconnecting Distributed Resources with Electric Power Systems

The recent interest in incorporating an increasing amount of DR such as, wind turbines, solar PV, natural gas generators, power electronics and batteries into the electric power grid has necessitated standards to ensure safety and power quality are maintained. IEEE published a family of these standards beginning in 2003 with the intention of consolidating the various standards and testing requirements for DR. The highest level standard is IEEE 1547-2003 The Standard for Interconnecting Distributed Resources with Electric Power Systems. It is accompanied by IEEE 1547.1 Standard Conformance Test Procedures for Equipment Interconnecting Distributed Resources with Electric Power Systems, IEEE 1547.2 Draft Application Guide for IEEE Std 1547-2003, IEEE 1547.3 Draft Guide for Monitoring, Information Exchange, and Control of Distributed Resources Interconnected with Electric Power Systems and IEEE 1547.4 Guide for Design, Operation and Integration of Distributed Resource Island Systems with Electric Power Systems. The requirements defined by IEEE 1547 and testing defined by IEEE 1547.1 are relevant to this thesis and thus will be discussed in further detail.

The requirements of IEEE 1547, found in chapter 4 of the document, are divided into four sections, General Requirements such as Voltage Regulation, Synchronization and Isolation, Response to Abnormal Conditions, Power Quality and Islanding. The tests used to determine the level of compliance with the standard are listed in chapter 5. They are the Design tests, Production tests, Interconnection Installation Evaluation, Commissioning tests and Periodic Interconnection tests. The Design, or Type, tests are intended to be performed on a representative unit in the lab or field. Production tests are not

meant to test IEEE Std 1547 requirements, but rather to verify the manufacturer's ratings. Interconnection Installation Evaluations are meant to verify that system designs meet IEEE Std 1547 requirements for grounding, fault detection, monitoring, reclosure functionality and isolation. Commissioning tests are to be performed before the initial connection is made or when any software or hardware changes are made to the system. They include testing the isolation device, the unintentional-islanding capabilities and cease to energize functionality. Finally, the group with authority over the DR is required to define Periodic Interconnection tests.

The requirements and tests defined above must be met at the connection point with the local EPS. Devices connected at this point could include the DR, local load, and the area EPS. This interconnection is more commonly known as the point of common coupling. IEEE 1547 assumes the EPS operates at 60 Hz and the DR is a synchronous machine, induction machine or static power inverter/converter less than 10 MVA.

2.2.1 Temperature Tests

Temperature stability is the first test listed in the Design category. There are two purposes of this test. The first is to confirm that the equipment under test (EUT) operates to a reasonable degree of accuracy within the manufacturer's specified temperature range. The second is to confirm that the EUT can still function properly after being stored in an environment where the temperatures remain in the manufacturer's specified range. Proper functionality during fluctuating temperatures is essential to DR because, by their nature, they will be operated in diverse environments.

2.2.2 Abnormal Voltage Tests

The next test assesses the EUT's response to abnormal voltage conditions. Overvoltage and undervoltage are deviations from nominal operating conditions that may occur on an area EPS. The EUT must be able to detect a certain amount of voltage deviation and it must respond in a reasonable

amount of time. In order to test for the response to voltage deviation, the magnitude of the EPS's voltage is slowly ramped at the terminals of the EUT. The rate of this ramp, m, is specified in Appendix A of IEEE 1547.1. The equation is shown below,

$$m = \frac{(0.5) * a}{2 * z}$$

Equation 2-1

where,

a is manufacturer's stated accuracy,

z is manufacturer's stated clearing time.

The magnitude at which the EUT trips is recorded and compared with the manufacturer's stated trip value.

The time response is tested by applying a stepped signal to the EUT and recording the duration of time between the step and EUT trip point. The clearing time must be between 0.16 – 2 seconds, depending on the voltage variation as a fraction of the base voltage. If multiphase units are to be tested, each phase must be tested individually. It is important when performing this test that only the voltage is modified to ensure that the DR does not trip for any other reason.

2.2.3 Abnormal Frequency Tests

Abnormal frequency conditions must also be tested. As in the abnormal voltage test, it is required that the EUT cease energizing the EPS if overfrequency or underfrequency conditions are detected. The magnitude response is tested by varying the frequency of the EPS waveform in one direction at a rate defined in equation 2.1, then recording the frequency at which the EUT trips.

The time response is tested by applying a step change in frequency and recording the time it takes for the EUT to trip. If multiphase units are to be tested, each phase must be tested individually. It

is important when performing this test that only the frequency is modified to ensure that the DR does not trip for any other reason.

The DR must detect these conditions and discontinue energizing the EPS, because the EPS is well regulated and if these conditions occur, it is likely that there is a serious problem, such as a fault. If the DR continues to supply power, dangerous conditions could become present that system operators or repairmen may not be aware of.

2.2.4 Synchronization

Synchronization is the next major test required. This test separates DR into two categories, devices that can generate voltage without using the grid, such as stand-alone inverters, and devices that must use the grid, such as induction machines. Each category of devices requires a specific form of testing. For independently excited equipment, it is required that the voltage, frequency and phase angle are synchronized with the EPS voltage, frequency and phase angle before a connection is made. Three different methods are specified for testing these conditions because different equipment synchronizes differently. A multifunction device that has the option of using a synchronizing function and controls when a connection is made can be tested with a simulated grid using method one. Synchronous generators are tested using method two. An actual grid interconnection is made and the paralleling device is monitored along with the generator and EPS voltage, frequency and phase angle. Devices that synchronize automatically, and cannot be disabled are tested using the third method.

In the second category, grid excited equipment, the concern lies with the magnitude of startup current. It must not create too much of a voltage fluctuation in the EPS when the device begins to energize the grid. The EUT is fed with a power source and startup currents are monitored to ensure they are within range. The EPS operates at a certain voltage, frequency and phase angle. In order to maintain power quality, interconnected devices must conform to this voltage magnitude, frequency and phase angle. Depending on the power rating of the DR, frequency must be within 0.1-0.3 Hz, voltage

within 3-10% and phase angle within 10-20° of the EPS. Deviations in any of these elements could damage equipment on the grid or on the DR.

2.2.5 Interconnection Integrity

The Interconnection Integrity test validates that the EUT conforms to standards in three areas, electromagnetic interference (EMI) protection, surge withstand performance and dielectric test. EMI is common in all electrical systems. It can interfere with the operation of equipment and potentially cause it to malfunction. Tests and standards for EMI performance are defined in IEEE Std C37.90.2. Surge withstand performance is another common feature that grid connected equipment must have. Surges can be unpredictable, such as those caused by lightning and can lead to very dangerous situations resulting from high currents. Control circuitry is tested using IEEE Std C37.90.1. Power circuitry is tested using IEEE Std C62.41.2 and IEEE Std C62.45. The dielectric test is defined for equipment that operates below 1000 V. It investigates performance at 1000 V_{rms} plus 220% of the rms nominal voltage. A 500 VA transform is used to apply the voltage for 60 seconds. The standard states that no flashover or damage can occurring during the test.

2.2.6 DC Injection

The next test regards the amount of DC injection allowed for non-isolated inverters. The EPS is designed for AC operation. It is important to limit DC current in the EPS because certain components, such as transformers or meters, can become damaged by excessive DC currents. The test specified for this standard requires measuring the DC current (< 1 Hz) of the EUT while the EUT operates under nominal conditions. The averaging window of the measurement must be no shorter than one line cycle and no longer than sixty line cycles. The average DC current over a five minute period must be less than 0.5% of the rated output current.

2.2.7 Unintentional Islanding

One of the most important tests defined in IEEE 1547 is the Unintentional Islanding test. Islanding is a condition that occurs when a local EPS operates independently of the area EPS. The local EPS regulates its own frequency and voltage in an islanded state and does not interact with the area EPS at all. While islanding can have many benefits such as security, improving power quality and reducing load of the area EPS, it can lead to dangerous conditions if the proper protection is not utilized. Since DRs are, by definition, distributed, no centralized control exists and therefore if the area EPS is de-energized, it is still possible that a local circuit could be energized by a DR. For example, if the area EPS suffers from a problem, it may be shut down so that it is safe for a technician to work on equipment. But if a solar panel and inverter connected to the area EPS continue to export power to the area EPS after it has gone down, the technician could be exposed to unexpected, dangerous conditions. Some DRs are specifically designed to operate in an islanded configuration, while others are not. The non-islanding DRs must therefore be tested to ensure that they disconnect from an EPS if an island is formed.

A simple test circuit is proposed in IEEE 1547.1 in which the EUT and an RLC load for a local EPS. They are then connected in parallel with a simulated area EPS. A switch (S3), inserted between the simulated area EPS and the local EPS, is used to simulate an islanding configuration by disconnecting the simulated EPS from the local EPS.

Since the local load could vary widely, the worst case condition must be tested. The load components must be chosen such that the resonant frequency of the RLC load is as close to the nominal operating frequency as possible. This will force the EUT to differentiate between a resonant circuit that mimics the EPS and the actual EPS. Constraints for the load are given in section 5.7.1.2 of IEEE 1547.1. They state that the quality factor of the load, calculated as

$$Q_f = \frac{\sqrt{P_{qC} * P_{qL}}}{P}$$

Equation 2-2

where,

P_{qC} is per phase inductive reactive power,

P_{qL} is per phase capacitive reactive power,

P is per phase real power.

must be equal to 1 +/- 0.05.

To perform the test, all switches are closed, the area EPS is simulated and the EUT is allowed to energized the circuit. Once this point is reached, S3 is opened and the time it takes for the EUT to de-energize must be less than two seconds. A diagram of this circuit taken from IEEE 1547 is shown in Figure 2-2. A similar test is defined for synchronous machines, but S1 and S2 are replaced with direct connections.

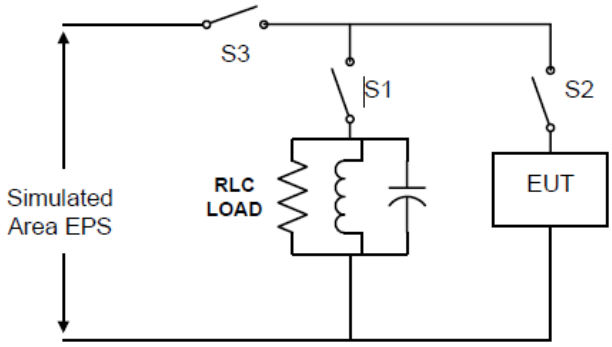

Figure 2-2 Anti-Islanding Test Circuit

2.2.8 Reverse Power

The reverse power technique requires that the EUT detect a change in the direction of power flow once it is disconnected from the EPS. This protection is tested by gradually changing the phase angle of the current powering the EUT until 180° is reached. The current is then ramped until the EUT

trips. A similar test, using a step instead of a ramp, can be performed to determine the amount of time it takes the EUT to trip.

2.2.9 Open Phase Test

Another test requiring the EUT to de-energize is the Open Phase test. If a device is operating on a three phase system and one phase is opened, it is necessary for the EUT to cease to energize the EPS on all phases. Unbalanced operation on a three phase system leads to harmonics and a reduction of power quality.

2.2.10 Reconnection

A majority of these tests have described the conditions that require the EUT to disconnect from the grid. Section 5.10 details the conditions required for the EUT to reconnect to the EPS. In this test, the EUT is allowed to operate under nominal conditions. A step change in the voltage is then applied to cause the EUT to trip and de-energize. The voltage is then returned to within the normal limits and the time it takes for the EUT to reconnect is measured. The voltage and frequency must both be within limits for the EUT to reconnect. To ensure that there is no malfunction with the reconnect circuitry once it is installed permanently, another test is required. As before, a parameter such as voltage is changed to a value outside of acceptable limits. Then, while the EUT is counting down to reconnection, the voltage is stepped outside of the limits. The device's reconnect timer should reset and start counting again. The reconnecting timer is critical because it allows for possible temporary excursions in voltage or frequency to be cleared before the device reconnects and begins energizing the grid again.

2.2.11 Harmonics

Waveform harmonics are phenomena that lead to reduced power quality due to increased distortion. These conditions lead to reduced efficiency and can damage equipment. Section 5.11 describes the tests used to determine the amount of both individual current harmonics and total rated-

current distortion for a DR. Multiple methods for testing are needed for different DR. While different tests set-ups are required, the requirements remain the same. The magnitude of the first 40 harmonics is to be measured. Acceptable values are listed in IEEE Std 1547 Section 4.3. The values are reproduced in Table 2-1 below.

Table 2-1 IEEE 1547 Harmonic Limits

Individual harmonic order h (odd harmonics)[a]	**h < 11**	**11 ≤ h < 17**	**17 ≤ h < 23**	**23 ≤ h < 35**	**35 ≤ h**	**Total demand distortion**
Percent (%)	4.0	2.0	1.5	0.6	0.3	5.0

[a]Even harmonics are limited to 25% of the odd harmonic limits above

The IEEE Std 1547, 1547.1 and 1547.2 are essential for maintaining safe and efficient EPSs. These standards define interconnection criteria for various types of distributed resources. Appendix A of 1547.1 defines specific test waveforms that are to be used to verify proper operation. While each test is important for proper functionality, this research will focus on testing abnormal voltage and frequency conditions, and anti-islanding.

3 Hardware-in-the-Loop System Realization

Introducing new elements onto the utility grid can be dangerous if these elements are untested for the many conditions that may occur. In order to perform these tests a system is needed that can simulate possible grid conditions repeatedly and accurately. HIL offers a unique and flexible way to simulate a grid environment in real time. During testing, the operator is able to retain control of system conditions and perform repeatable tests in an isolated environment, thus avoiding any damage to the utility grid that many consumers depend on. This chapter will describe how HIL can be used to simulate a grid environment in real-time.

3.1 Overview

The HIL system of this thesis consists of a power amplifier to simulate the utility grid, load bank, PV inverter, DC power source and RTDS. Four power amplifiers are present in the lab where this thesis was conducted in. They are each rated to 50 kW for a total of 200 kW. For the purposes of this thesis, 6 kW will be sufficient to test and characterize an inverter. A 162 kW RLC load bank is also present and is used to sink power. The real-time data system (RTDS) was developed by Opal-RT Technologies and consists of a Wanda 4U target machine and a Windows based host machine. The DC power source was constructed by AeroVironment, model AV-900. A block diagram of the PHIL system used in this thesis can be seen in Figure 3-1.

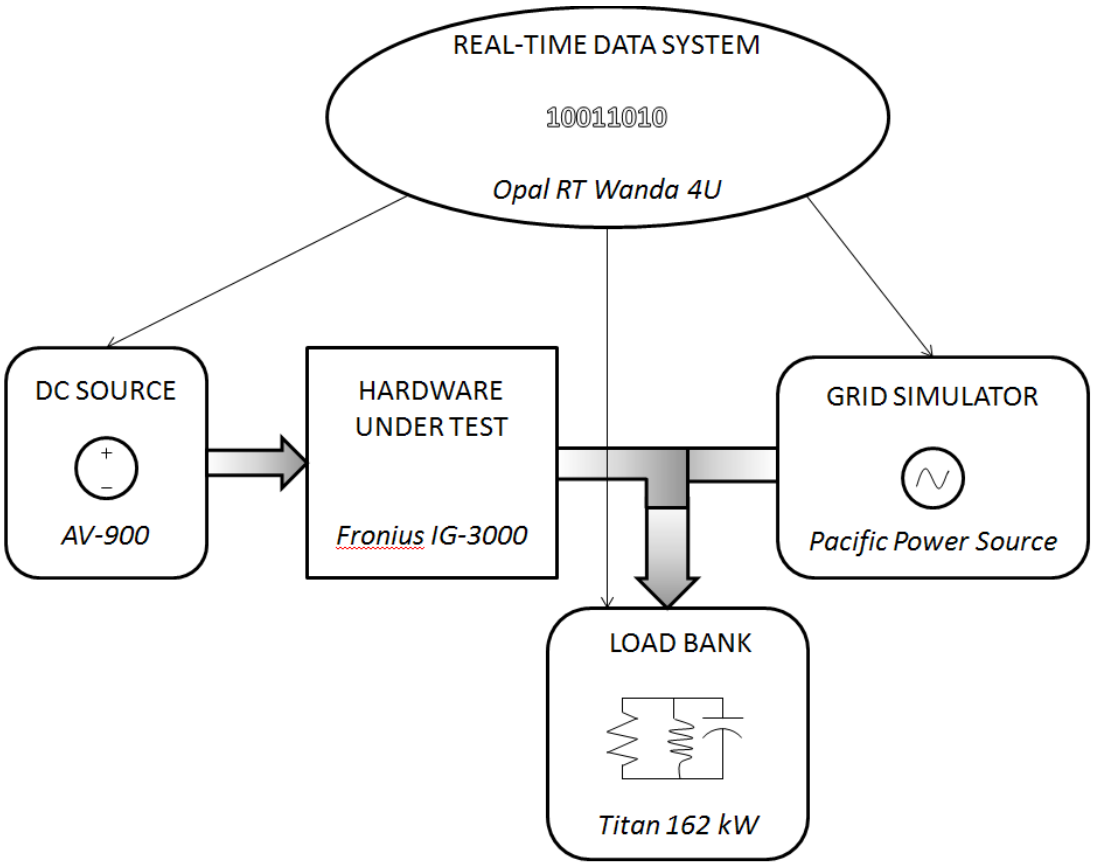

Figure 3-1 PHIL Set-Up

Thin lines coming from the RTDS represent control signals. Thick, gradient lines represent actual power flow between components.

3.2 Grid Simulator

Simulating generation sources is a key element of this project. In order to achieve the power levels and controllability required, one 50 kW Pacific Power Source power amplifier was used to simulate the utility grid. While four of these exist at the DERTF and may be operated in parallel to achieve 200 kW, only one was necessary for this project.

3.2.1 Hardware

The Pacific Power Source amplifier, model 3060-MS, is a 3-phase unidirectional power flow amplifier capable of up to 62.5 kVA and 50 kW. Input AC power from the actual utility grid is rectified, conditioned and then converted back to AC output power efficiently. This method allows for very

accurate and high quality power output with 1% regulation and 1% total harmonic distortion. It is a very fast system with response times of 300 µs for 100% load changes. Precision and controllability are crucial aspects when it comes to simulating an electric grid. Frequency and voltage deviations from set points must be minimal and harmonic content must be low in order to obtain valid results for interconnection testing. The 3060-MS will maintain output frequency within 0.01% and will regulate individual phase voltages within 0.5%. It has a frequency range of 47-500 Hz and a voltage range of 0-132 V_{L-N} and a slew rate of 1 V/µs [**32**].

Another important aspect for grid integration testing is the apparent stiffness of the simulated grid. A stiffness ratio is defined by the Electric Power Research Institute as the ratio of available utility fault current to maximum rated output current of the DR [**33**]. This value is important because some DR will determine islanding conditions by attempting to control the grid voltage or frequency [**34**]. The grid simulator must be powerful enough to source enough power for the given loads and not allow anything else to regulate the voltage or frequency. In the set-up for this thesis, the utility grid is simulated by an AC bus. It is fed by the grid simulator through three, single phase autotransformers connected in a grounded wye-configuration. The transformer ratio is 2.216, yielding a maximum output voltage of 292.5 V_{L-N}.

The grid simulator can be controlled locally or remotely. Local, front panel operation of the grid simulator, utilizes a knob to provide three discrete frequency settings and a screw to provide fine, per phase, voltage adjustment. This form of control is limited since frequency must remain constant and the variation of the voltage is constrained by how fast and precisely a screw can be turned by hand. For advanced testing, a greater deal of control is required. Remote control of the grid simulators is much more functional and can be implemented by use of an external oscillator input or serial communication. The Universal Programmable Controller, UPC-32, offers much more powerful control by means of analog and digital outputs from a remote location. Waveforms can be preprogrammed on the controller or

voltage levels can be modified in real-time. Limits can be set and metering is displayed on the front panel of the controller. During execution, the controller sends a scaled analog version of the waveforms to the 3060-MS external oscillator input which then amplifies the waveforms to actual power levels. In order to use this system as part of a larger HIL system, the UPC must be controlled by the RTDS. Waveforms from the RTDS are converted using a digital to analog converter and then sent to the UPC's auxiliary input port. These control signals are then sent from the UPC to the 3060-MS and amplified. A connection diagram showing the interface between the HIL Analog Out port and UPC Analog In port is shown below.

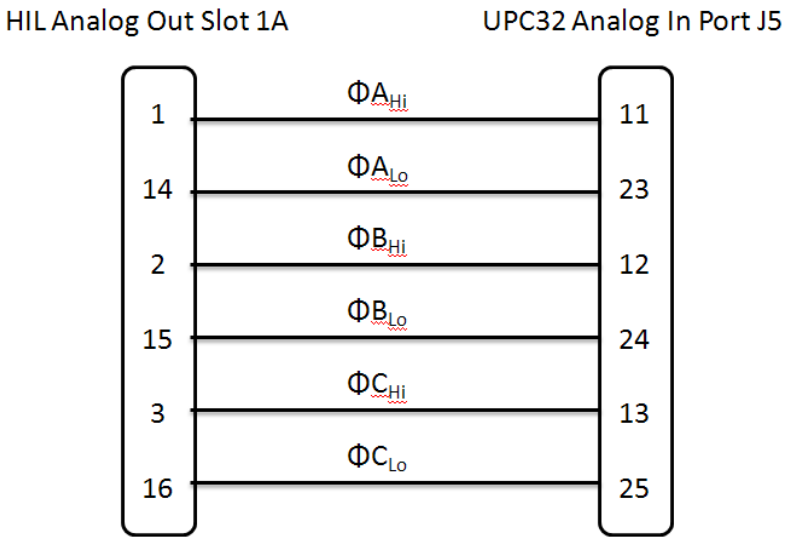

Figure 3-2 HIL to UPC-32 Connection Diagram

3.2.2 Software

Control of a simulated utility grid is necessary for performing integration tests. The grid, at the residential level where DRs less than 30 kVA might be installed, is normally a single phase 60 Hz sine wave at 120 $V_{L\text{-}N}$. If this waveform was all that was necessary for testing, the grid simulators could be controlled from the front panel and no further interaction would be necessary. In order to simulate abnormal conditions though, some type of predetermined programmatic input is required. In this HIL system, control of the amplifier ultimately stems from a software program that was developed for this

thesis. The development environment for the program was MATLAB's Simulink [**35**]. It was used because the models built in Simulink can be compiled into C code and then executed on the RTDS. Also the software environment is extremely powerful and easy to use.

The user connects blocks which represent signals, math functions or communication with peripherals to create a program. Large libraries with various waveforms and math functions come built-in and more specific libraries, such as SimPowerSystems which contains elements such as power electronics, transmission lines, generators, etc., can be added. Blocks are also available for custom C code if the user desires a certain function that is not available from the Simulink libraries. Once these blocks' inputs and outputs have been connected, they can be grouped into subsystems to facilitate organization and other functions such as enabling or triggering. This creates an extremely powerful and flexible environment for developing models of different devices.

Each block contains some parameters that the user may set. At times though, more control is needed. Some modifications to the standard blocks were necessary to generate the signals that were necessary for IEEE 1547 testing. These modifications are described in the following sections.

The Simulink program developed for this thesis consists of two subsystems and a set of global variables at the top level.

3.2.2.1 Global Variables

The global variables set both simulation parameters and testing parameters. They are the main point of control, along with choice of which test to perform, the user has in the program.

The simulation parameters are simulation step size and end time. The simulation step size is important for resolution. Since this program will be run in real-time on a digital simulator, a fixed step size and fixed step size solver is required. While the RTDS is capable of a step size as small as 10 µs [**36**], a 50 µs step size was sufficient for this project since smooth waveforms with a minimum period of 16.13 ms were used.

Test parameters include operating voltage, ramp rates, step amount and steady-state duration. The user may define operating voltages within the range of the power amplifier. The program and grid simulator are capable of three phase operation, but the inverter used for this thesis connects to the grid in a split-phase configuration. Therefore, the user will set the operating voltage variable, V_{rms}, to one half of the desired operating voltage, as dictated by the inverter specifications. The program is currently configured to control the grid simulator in split-phase automatically.

The ramp rate variables are used when either the frequency or voltage need to be ramped. Ramp rates are completely customizable in the program, though certain testing schemes generally set requirements. IEEE 1547.1 imposes constraints on the slopes in order to guarantee that the correct protection is tested. The formula for the slope is shown in Equation 2-1.

The steady-state duration parameter, *delay*, defines the amount of time, minus initial ramping (5 seconds), that a 60 Hz sine wave at the user-defined voltage will be output. The reconnect time setting on DRs is the reason for this variable. It a setting that prevents DRs from energizing the grid unless a quality (within voltage, frequency, harmonics, etc. limits) steady-state waveform is observed for that duration of the reconnect time. Once that constraint has been satisfied, a DR may begin energizing the grid and then testing can commence.

The duration of the test is defined by the end time variable, *endTime* minus the steady-state variable, *delay.* Once the simulation time is greater than the end time, the grid simulator waveforms are ramped down to zero so that re-energization by the inverter does not occur. Though there is protection built into the software, the user should still calculate what end waveform will result for the defined test duration and ramp rate to avoid any damage to equipment.

3.2.2.2 Subsystems

The network of subsystems in this program can be reduced to two high-level subsystems, the console and the master. This configuration is dictated by the RTDS. They are differentiated by their

functionality and purpose. The console is run from the host machine and is intended to be a user interface. The master is run on the target machine and is intended to perform computations and interface with peripherals such as an field programmable gate array (FPGA) or controller area network (CAN) communication card. Data is interchanged between the two subsystems via a connection between the target machine and the host machine. This allows the user to see feedback and perform control functions.

3.2.2.2.1 Console Subsystem

The console is the user interface. It is intended strictly for control signals and feedback displays. It is the only window that the user sees when the program is running in real-time. The console is used in this program for defining which test will be performed and to display errors that have occurred. There are two values that must be set by the user to determine which IEEE 1547 test will be run. One determines the parameter to be tested and the other determines what type of test will be performed. Instructions for the possible inputs are displayed on the console. Table 3-1 details the options that are available.

Table 3-1 Grid Simulator User Control Variables

	User Input	Corresponding Test
Box 1	1	Over Voltage
	2	Under Voltage
	3	Over Frequency
	4	Under Frequency
	5	Anti-Islanding
Box 2	0	Step
	1	Ramp

Also included in the console are displays for each phase that show possible errors that could occur. An error is displayed when the waveforms output by the RTDS do not conform to protection specifications defined in the program. The analog outputs of the RTDS that control the grid simulators

are looped-back to the analog inputs of the RTDS and then passed through an error checking block in the master subsystem. The errors include upper and lower frequency limits, upper voltage limits and volt second balance. These errors are derived from the capabilities of the grid simulator and output transformer.

3.2.2.3 Master Subsystem

The master subsystem is where all of the computation takes place and thus requires the computational power of the target machine. Since it is executed on the target machine while the program is running, no changes to the subsystem may take place during operation. The master subsystem is divided into five main functions, the Signals subsystem, the Test Selector subsystem, the signal conditioning subsystems, the communication blocks and the Protection subsystem. A screen shot of the master subsystem is given below:

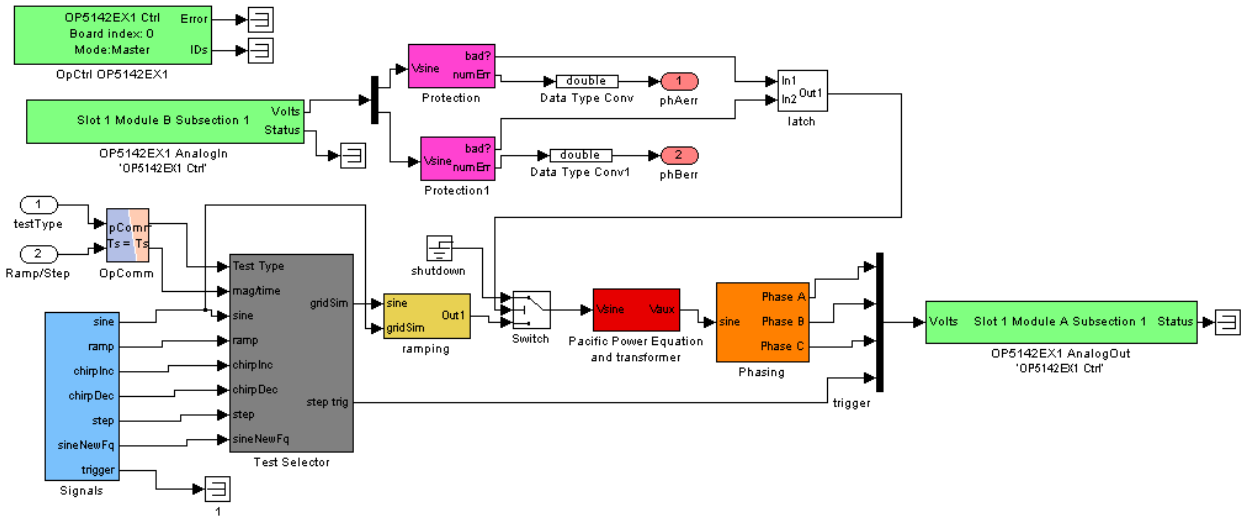

Figure 3-3: Grid Simulator Master Subsystem

3.2.2.3.1 Signals Subsystem

The first step in performing integration testing is to generate testing waveforms. These waveforms are generated in the Signals subsystem. The basis for all of the testing waveforms used in this program is a 60 Hz sine wave. Other waveforms in the Signals subsystem are ramps, variable

frequency sine waves and steps. A trigger signal is also implemented to aid in data acquisition and timing.

3.2.2.3.2 Test Selector Subsystem

These signals are then fed into the Test Selector subsystem, along with the user input. Inside this subsystem, each IEEE 1547 test is grouped into its own subsystem and then further into step or ramp subsystems. A switch case block accepts the user input and determines which test subsystem to enable. A diagram of the Test Selection subsystem is shown below:

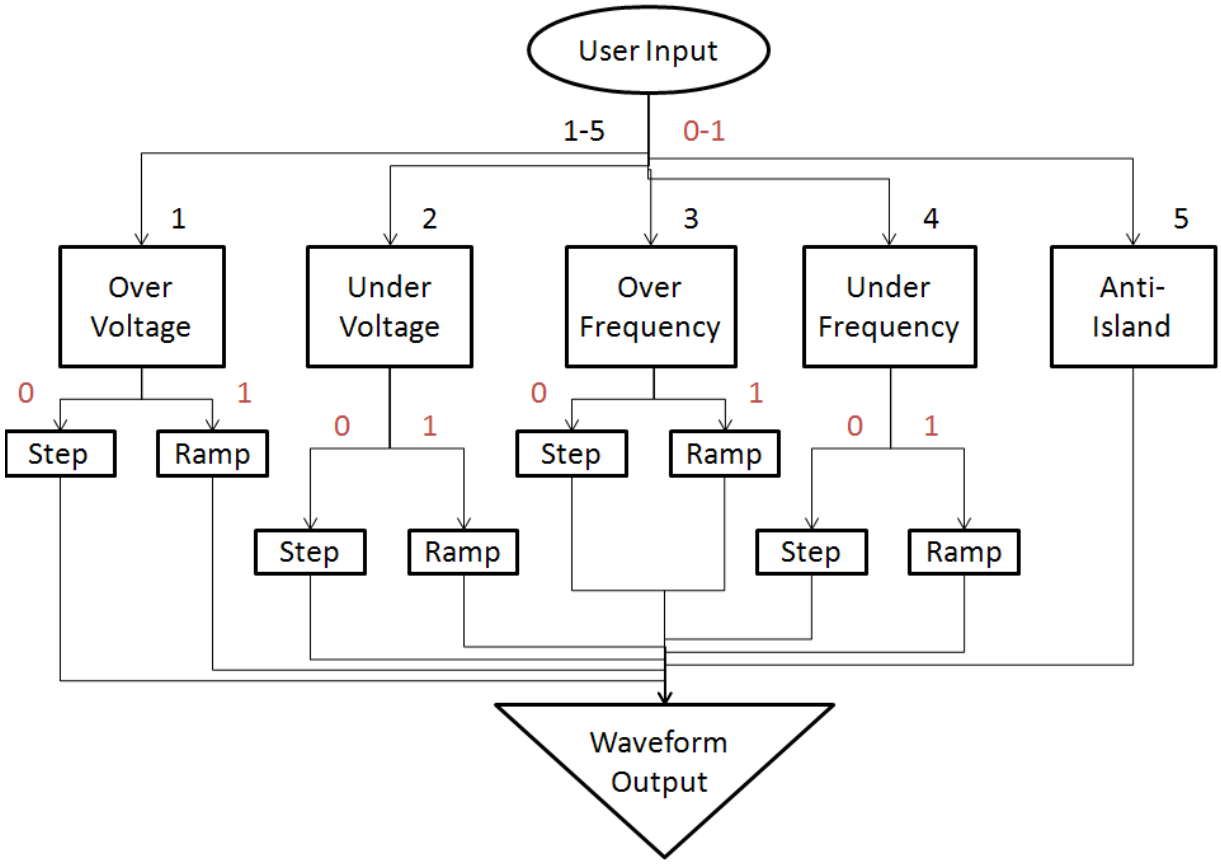

Figure 3-4: Test Selector Subsystem

Inside each test subsystem, either the original sine wave is modified, as in a voltage ramp, or an alternate signal, as in a frequency step, is selected and passed to the first signal conditioning subsystem called the Ramping subsystem.

3.2.2.3.3 Ramping Subsystem

The purpose of this subsystem is to ensure the grid simulators are operated safely. Here an initial increasing ramp is applied to the steady-state signal in order to safely bring the grid simulators up to the operating voltage and a final decreasing ramp is applied to the testing waveform to prevent the DR from re-energizing the grid once testing has completed.

3.2.2.3.4 Pacific Power Equation Subsystem

Once the signal passes the Ramping subsystem, it travels to the Pacific Power Equation subsystem. The UPC32 requires a certain input voltage range and thus a scaling factor is used. This subsystem scales the waveform to the specifications of the UPC32. The formula, provided by the UPC-32 manual, for converting from the input of the UPC-32 to the power output of the grid simulator is reproduced below.

$$Power\ Source\ OUTPUT\ VOLTAGE = Vprogram + (Vaux * 25 * XFMRratio)$$

Equation 3-1

where,

Power Source OUTPUT VOLTAGE (V_o) is the output of grid simulator after transformer,

$V_{program}$ is the offset that can be programmatically set,

V_{aux} is the peak voltage of the input waveform,

XFMRratio is the transformer ratio.

If $V_{program}$ is set to zero, the formula may be rearranged to determine what values must be output from the analog ports of the RTDS.

$$Vaux, pk = \frac{Vo, pk}{25 * XFMRratio}$$

Equation 3-2

As an example, if V_o = 120 V_{rms} (169.7 V_{pk}) is desired with a transformer ratio of $XFMR_{ratio}$ = 2.216, then the RTDS is required to output $V_{aux,pk}$ = 3.063 V. A saturation block is used in the Signals subsystem to protect the UPC-32's auxiliary input port which can only handle +/- 10V.

3.2.2.3.5 Phasing Subsystem

The final signal conditioning subsystem, Phasing, applies the proper phase orientation required by the system. It does this by using a delay and/or grounding one of the phases. The split-phase configuration for this thesis required that in the Phasing subsystem no modification be made to the waveform on Phase A, the Phase B waveform to be multiplied by -1 (equivalent to a 180° phase shift) and Phase C be grounded, which is equivalent to applying zero volts across the output.

3.2.2.3.6 Protection Subsystem

One of the most important parts in the master subsystem is the Protection subsystem. Since analog waveforms are used to control the grid simulators, much of the device's own protection is bypassed. Voltage and frequency limitations must be taken into account as well as slew rate to prevent damage to the grid simulators or transformer core saturation and ensure reliable operation. A hardware loop-back system is used to implement this. The analog outputs on the RTDS that are sending signals to the UPC-32 are looped-back to the analog inputs in the RTDS. Waveforms from each phase are captured and the frequency, voltage and volt seconds are monitored. Simulink does not have an included block for measuring the frequency so one had to be constructed. The custom built block captures the simulation time at each rising and falling edge zero crossing. It then holds that value until another zero crossing occurs. The two captured values of the simulation time are subtracted, multiplied by two and then inverted to give the frequency of the waveform.

Simulink also does not have a block for measuring the volt-seconds of a waveform. For this project, volt-seconds were measured by capturing the instantaneous voltage on the A/D channel,

multiplying it by the simulation step size and then adding it to a running sum of the previously captured values.

The measured values described above are checked against preset values to determine if an error has occurred. If an error is detected, the output of the program is immediately changed and latched to zero. It is important to note that the Protection subsystem does not monitor grid-level waveforms. It only monitors what is being output on the D/A channels of the RTDS that controls the UPC-32.

3.2.2.3.7 Communication Blocks

In order for the Simulink software model to generate any electrical signals, interface blocks for the RTDS are needed. Opal RT provides a library of generic I/O blocks for various communication schemes such as CAN, RS232/485 or GPIB. For grid simulator control, analog output was used. In the RTDS, an FPGA controls the digital to analog (D/A) card so blocks to interact with the FPGA were implemented. One block, OP5142EX1 Ctrl, sets the bitstream and board index of the FPGA. Other blocks, such as the OP5142EX1 AnalogOut or OP5142EX1 AnalogIn , instruct the FPGA to communicate with the D/A or A/D modules, respectively to either send or receive data.

In addition to these blocks, other blocks are needed to transfer information between the console and master subsystems. These blocks are called OpComm blocks and they facilitate data transfer between the real-time target and the host machine during operation. Though not used in this manner for the purposes of this thesis, OpComm blocks can facilitate the use of multiple cores. Programs that require a large amount of computational power, like a large power system, can be run in real-time though the parallel utilization of multiple processing cores. The user can define which parts of the program are handled by which core.

3.2.2.4 Program Operation

Characterizing an inverter with this program requires the knowledge of a few specific details before tests can be performed. The first step is to determine important electrical specifications about the inverter. The nominal operating frequency and voltage are provided by the manufacturer and usually printed on the side of the inverter. These values will determine the steady-state waveform of the program. Once these values are determined the *Vrms* global variable can be set. A frequency of 60 Hz is assumed in this program. This can be modified, though it requires more effort than just changing a global variable. For grid-tied PV inverters, both a DC operating range and an AC operating range are specified. These limits will determine what step sizes are required for testing grid abnormalities.

How the inverter connects with the grid is very important. Some inverters use a three phase configuration and some use split-phase. The phasing block in the master subsystem configures the phasing output and must be modified accordingly. A split-phase configuration between phases A and B is the default. The next step is to determine the simulation step size required. This is set by the variable *Ts*. A step size of 10 μs is possible, but since this thesis is focused on grid-tied applications with no waveforms faster than 62 Hz, a step size of 50 μs is more than sufficient. There are more variables that will be discussed later, but once the aforementioned variables have been set, the initial testing can begin.

3.2.2.5 Reconnection Time

One of the first tests that is necessary to perform is determining the reconnection time. Protection devices for grid-tied inverters should prevent the inverter from energizing the grid after a fault condition has occurred. Once proper operation of the grid has been restored, and the inverter senses this, the protection circuitry enters a wait time. The purpose of this is to verify that the grid is indeed stable and will remain so. Once the wait time has elapsed and the grid conditions are acceptable the inverter will connect to the grid and begin to export power. To characterize the inverter's reactions

to various grid conditions, a valid connection must first exist between the inverter and the grid and thus the reconnection time must be measured so the user knows when to begin a test waveform. The variable that sets the time before a test waveform is *delay*. In order to determine the reconnection time, the delay variable should be set to an arbitrarily large value (600 seconds) and the test parameters should be set to 5 for anti-islanding. The output current of the inverter should then be monitored to determine when the export of power has begun. It is important to note that the program uses a ramping function at the beginning that lasts for 5 seconds. A valid waveforms do not exist immediately, though it is usually not critical to determine the reconnection time to greater than few seconds of accuracy. Once the reconnection time has been determined and the *delay* variable set, variables corresponding the testing waveforms can be modified.

The testing waveforms used in this program are based off of those specified in IEEE 1547.1 Appendix A. In order to generate these waveforms in Simulink, some of the provided blocks had to be modified or combined with other blocks. All of the testing waveforms are based off of a 60 Hz sine wave with the RMS voltage specified by the user.

3.2.2.6 Voltage Test Waveforms

The voltage tests require that the magnitude of the grid voltage be changed gradually for the magnitude test and instantaneously for the time test while all other parameters are held constant [**37**].

3.2.2.6.1 Magnitude Test Waveform

In order to change the magnitude gradually, the generic sine wave was multiplied, in the case of overvoltage, and divided, in the case of undervoltage, by a linearly increasing waveform. As specified in Equation 2-1, the slope must be slow enough such that the control system in the inverter has time to respond to the applied voltage. If the information in Equation 2-1 is not obtainable, a very slowly increasing, usually less than 100mV/second waveform can be used.

Once the slope is set in the Signals subsystem and the Over or Under Voltage and Ramp options are selected, the test may be executed. The program will output a 60 Hz sine wave at the initial V_{rms} specified by the user until the user-defined *delay* time has passed. The program then begins to apply the ramping function and the voltage is either steadily increased or decreased until the *endTime* variable is reached. While protection measures do exist, it is important for the user to determine what voltage levels will be applied so that damage to any equipment does not occur. The following equations yield the final voltage.

$$V_{rms}(endTime) = V_{rms,i} * [m * (endTime - delay) + 1]$$

Equation 3-3

$$V_{rms}(endTime) = \frac{V_{rms,i}}{[m * (endTime - delay) + 1]}$$

Equation 3-4

where,

m is the ramp rate,

V_{rms} is the RMS voltage

$V_{rms,i}$ is the initial RMS voltage.

Equation 3-3 applies to overvoltage tests and Equation 3-4 applies to undervoltage tests.

The three waveforms, Simulink, HIL and grid simulator for each test can be seen below. The waveform in Figure 3-5 is the result of a Simulink simulation. It shows an example of how the voltage magnitude can be gradually increased with no discontinuities.

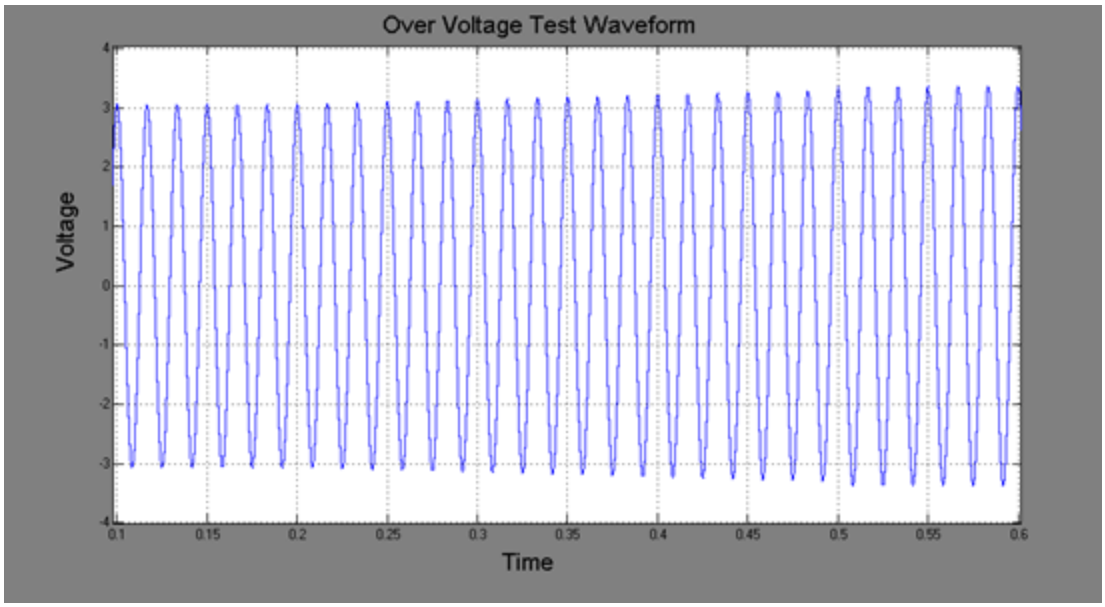

Figure 3-5: Overvoltage Ramp Waveform generated in Simulink

For the purpose of demonstration, this waveform was ramped very quickly. IEEE 1547 tests do not allow for waveforms to be ramped so quickly though. The waveform in Figure 3-6 shows the analog output of the HIL machine on a much more realistic time scale. The beginning of the testing waveform is signified by the step change shown by the bottom waveform. After this point, the RMS measurement of the test waveform begins to slowly increase, while the frequency remains constant.

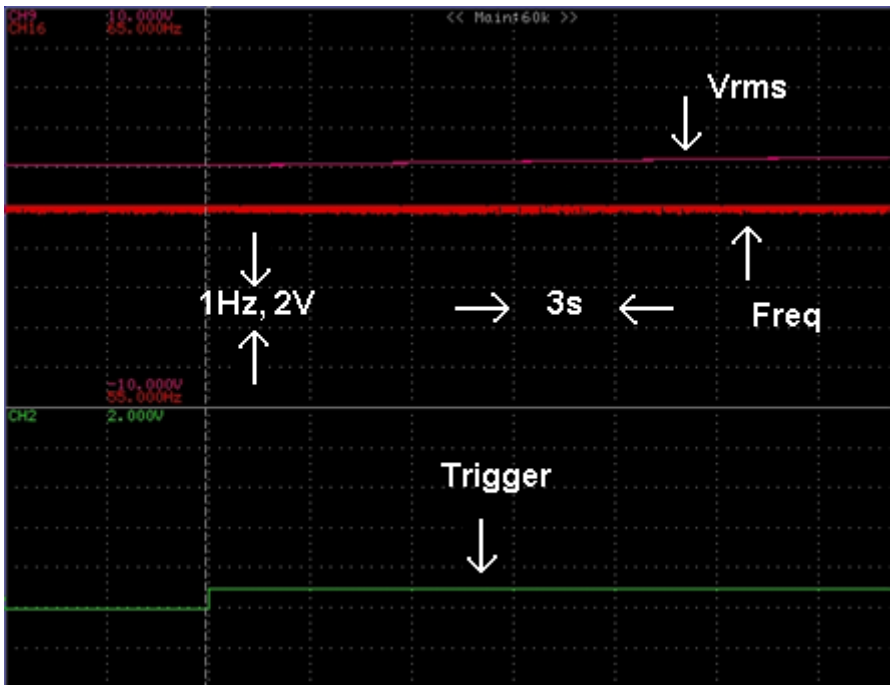

Figure 3-6: Overvoltage Ramp Analog Output of RTDS with Constant Frequency

Waveforms, similar to those shown in Figure 3-6, but at actual testing voltage can be seen in Figure 3-7.

These were measured from the grid simulator output.

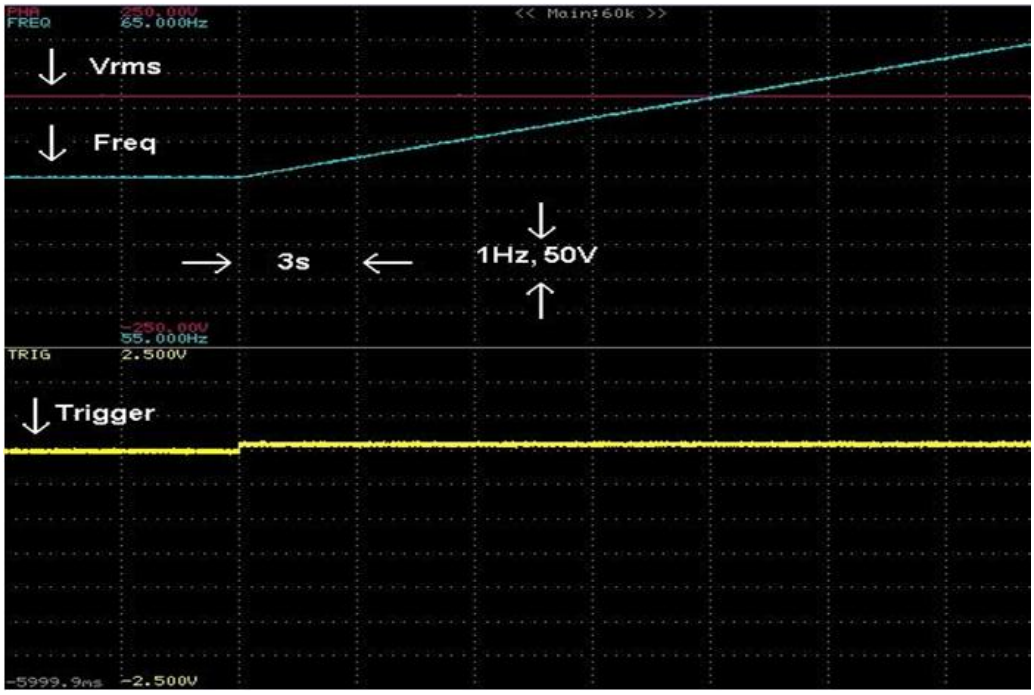

Figure 3-7 Overvoltage Ramp of Grid Simulator with Constant Frequency

3.2.2.6.2 Time Test Waveforms

A similar approach is used to generate the time test waveforms. The difference is that the generic sine wave is multiplied or divided by a step function instead of a ramp, as in the magnitude test. The value of the step function is controllable by the *stepSize* user variable. Since the user is permitted to set the *delay* variable to any value, care must be taken to ensure that smooth transitions occur. If this control was not implemented, discontinuous waveforms would result and possibly cause unexpected fault conditions that could cause the inverter to trip for incorrect reasons. An example of a time test waveform without smooth transition control can be seen in Figure 3-8.

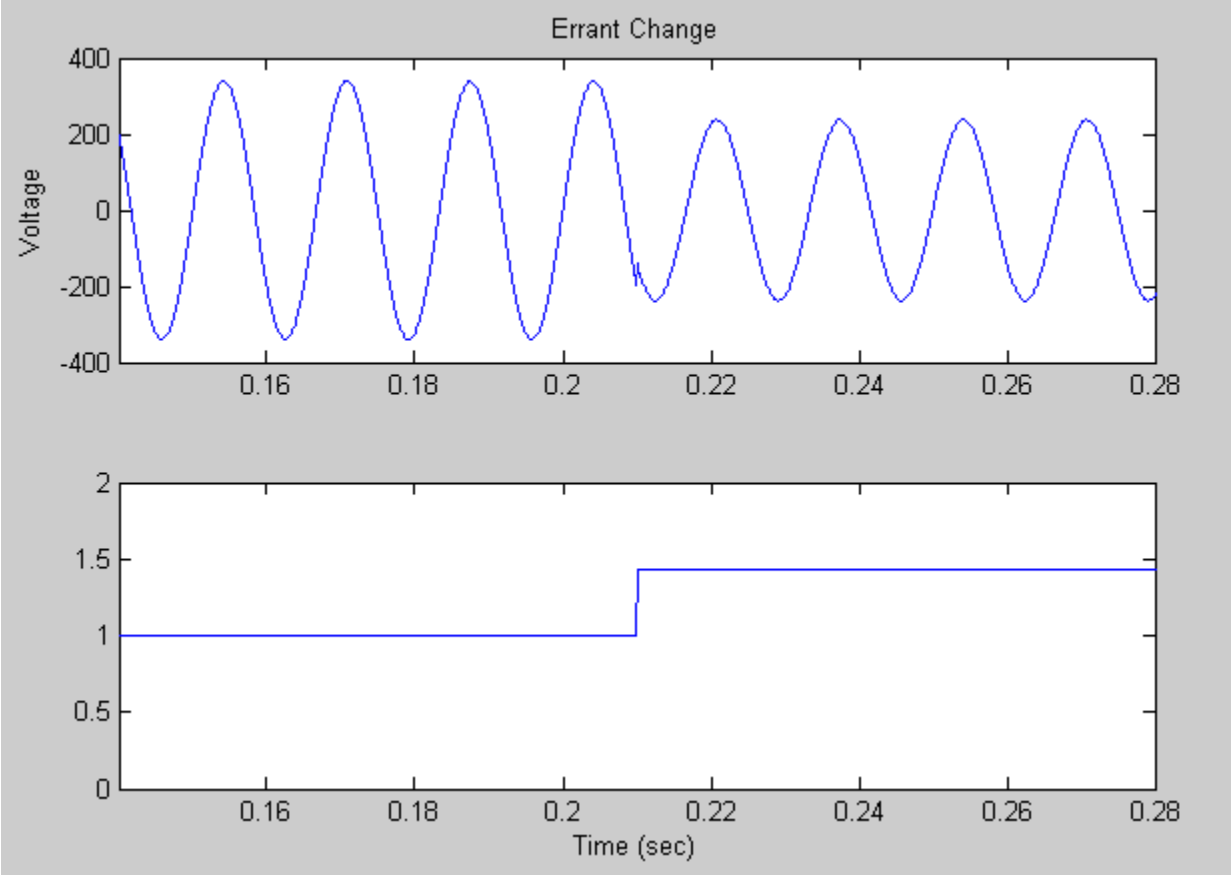

Figure 3-8 Errant Undervoltage Step in Simulink

To avoid this discontinuity, the step change must only be applied at zero crossings. The Simulink library includes a block called Hit Detection that outputs a pulse when a zero crossing is detected. A smooth transition can be achieved using this pulse to determine when to apply the step. The same waveform

that was shown in Figure 3-8 is now shown in Figure 3-9 with the smooth transition control implemented. Since the *delay* variable is set for a time that is not an integer multiple of the period of the waveform, this detection scheme causes the step to occur at a slightly later time.

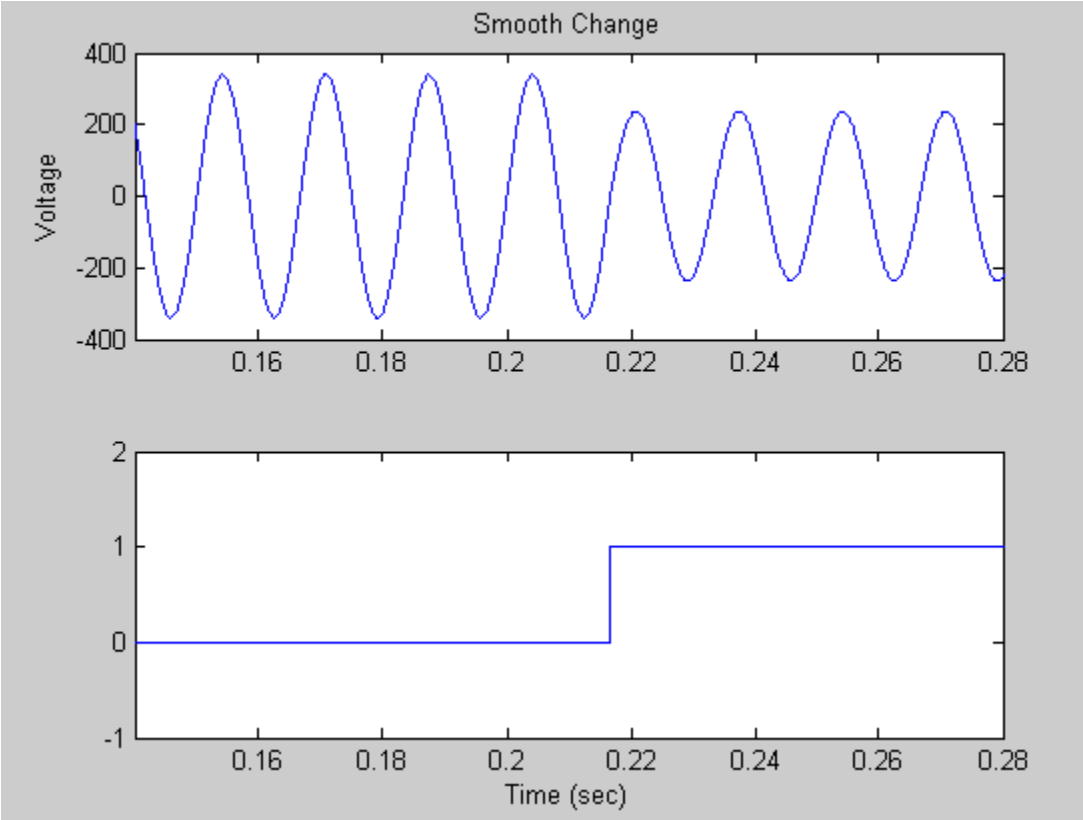

Figure 3-9 Undervoltage Smooth Transition in Simulink

3.2.2.7 Frequency Test Waveforms

The next IEEE 1547 tests included in the program are abnormal frequency tests. The waveforms generated vary in frequency while other parameters are held constant so that devices' response to abnormal frequency conditions can be tested. Like in the case of the abnormal voltage tests, the abnormal frequency tests are divided into two categories, magnitude and time tests.

3.2.2.7.1 Magnitude Test Waveform

In order to perform the magnitude test, the frequency must be varied gradually so that the amount of frequency deviation from the expected 60 Hz that causes the inverter to trip can be

determined. Simulink includes a Chirp block that performs this task by allowing the user to specify the initial frequency, target time and target frequency. It does not however, let the user specify when the frequency change will begin. It automatically begins at the start of program execution. This is a significant problem because most inverters require a period of steady-state grid operation before they will actively begin exporting power to the grid. Also, the user variable *delay*, that defines the duration of the steady state period, would be useless if the Chirp block was used.

To generate a waveform that has a gradual frequency change and can begin that change at any arbitrary time, a custom subsystem had to be developed. The basis of this subsystem is a Simulink block that generates a sine wave in a special way. It has parameters for frequency, amplitude, offset and phase angle the same way that the generic sine wave block does. What is special about it though is it has an input for the time signal used. During program execution, the block generates a sine wave with a frequency based on the frequency parameter and the input t. The block utilizes the generic sine wave equation,

$$f(t) = A * \sin(\omega * t + \phi) + C$$

Equation 3-5

where,

A is amplitude,

ω is frequency,

ϕ is phase angle,

C is offset.

The user must specify, before the program is executed, the amplitude, A, the frequency, ω, the phase angle, ϕ, and the offset, C. Since ω is defined before the program executes and cannot be changed during execution, the input t is used to vary the frequency. The first derivative of the function fed to the input t defines the frequency. If a constant frequency is desired, a first order function would be the

input t. If a linearly changing frequency is need, the input function would be a second order function. Hence, to generate the constant frequency waveform that changes to a waveform with gradually increasing or decreasing frequency, the input t is switched from a first order function to a second order function when the simulation time is equal to the *delay* variable.

Like the amplitude, frequency, phase angle and offset of the sine wave, the first order and second order functions' parameters must be set before program execution. Since the user cannot modify any of these parameters directly and the *delay* variable is not enough to control the rate of change of the frequency, user variables, *mFreqInc and mFreqDec,* are provided. These variables are incorporated into the parameter values of the blocks to give the said control. How a user might determine these parameters is described below.

In the case of increasing frequency, the first order function is a simple linear function,

$$y_1 = m_1 * t$$

Equation 3-6

while the second order function has a parabolic form,

$$y_2 = (t - mFreqInc)^2 + C_2$$

Equation 3-7

In the case of decreasing frequency, the first order function is the same as for the increasing frequency case,

$$y_3 = m_3 * t$$

Equation 3-8

while the second order function varies slightly from the increasing frequency case,

$$y_4 = -(t - mFreqDec)^2 + C_4$$

Equation 3-9

A smooth transition will occur if two conditions are met. The first condition is that the first order function and second order function have the same slope when the simulation time is equal to the time when the test waveform starts, defined by the user variable *delay*. For the case of increasing frequency,

$$\frac{dy_1}{dt} = \frac{dy_2}{dt}$$

Equation 3-10

$$m_1 = 2 * (t - mFreqInc)$$

If t = *delay*, then

$$m_1 = 2 * (delay - mFreqInc)$$

Equation 3-11

The second constraint is that the two functions must intersect at t=*delay*.

$$y_1 = y_2$$

Equation 3-12

$$m_1 * t = (t - mFreqInc)^2 + C_2$$

Solving for C_2 yields,

$$C_2 = -t^2 - mFreqInc^2 + m_1 * t + 2 * t * mFreqInc$$

and substituting t = *delay* and m_1 = 2*(*delay-mFreqInc*),

$$C_2 = delay^2 - mFreqInc^2$$

Equation 3-13

A graphical representation of this concept can be seen in 3-10. The red X in the image below denotes when the simulation time is equal to the *delay* time, 150. The green curve is the second order function and the blue curve is the first order function.

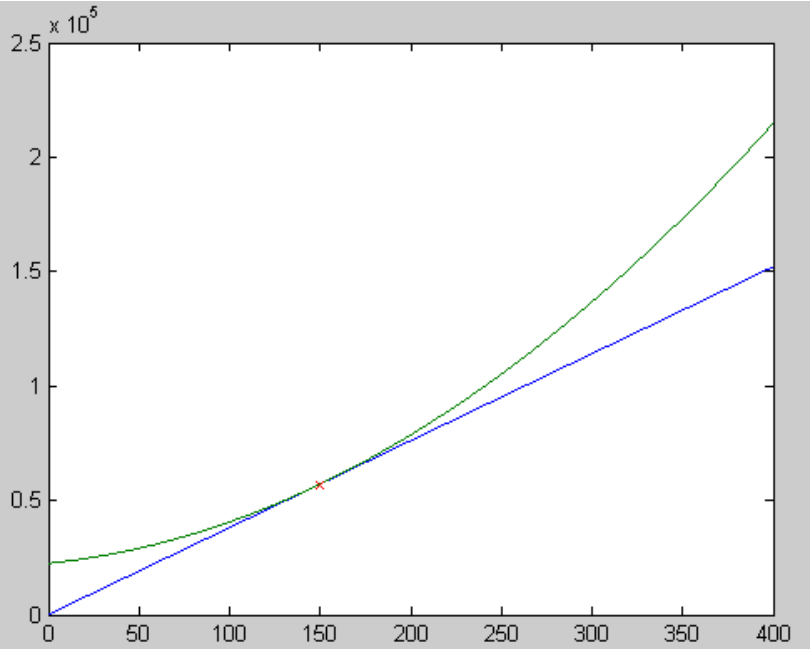

Figure 3-10 External Time Input for Increasing Frequency Sine Wave

The resulting sine wave can be seen below.

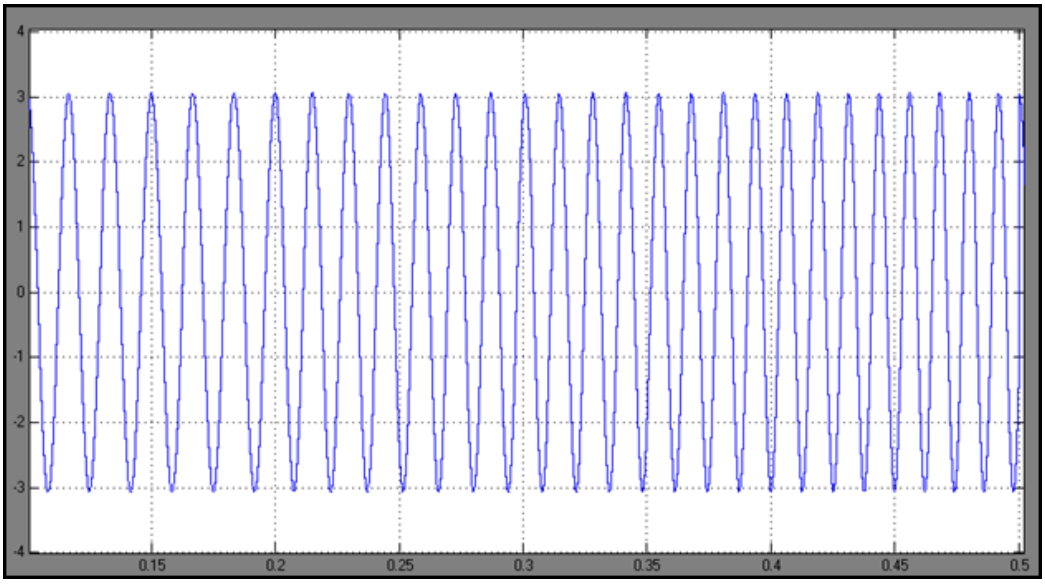

Figure 3-11 Sine Wave with Gradually Increasing Frequency

A similar approach is made for decreasing frequency. The results of this approach are,

$$m_3 = 2 * (mFreqDec - delay)$$

Equation 3-14

$$C_4 = mFreqDec^2 - delay^2$$

Equation 3-15

A graphical representation of these waveforms is shown in 3-12. As in 3-10, the green waveform represents the second order function, the blue waveform represents the first order function and the red X represents the time when the transition between the two occurs.

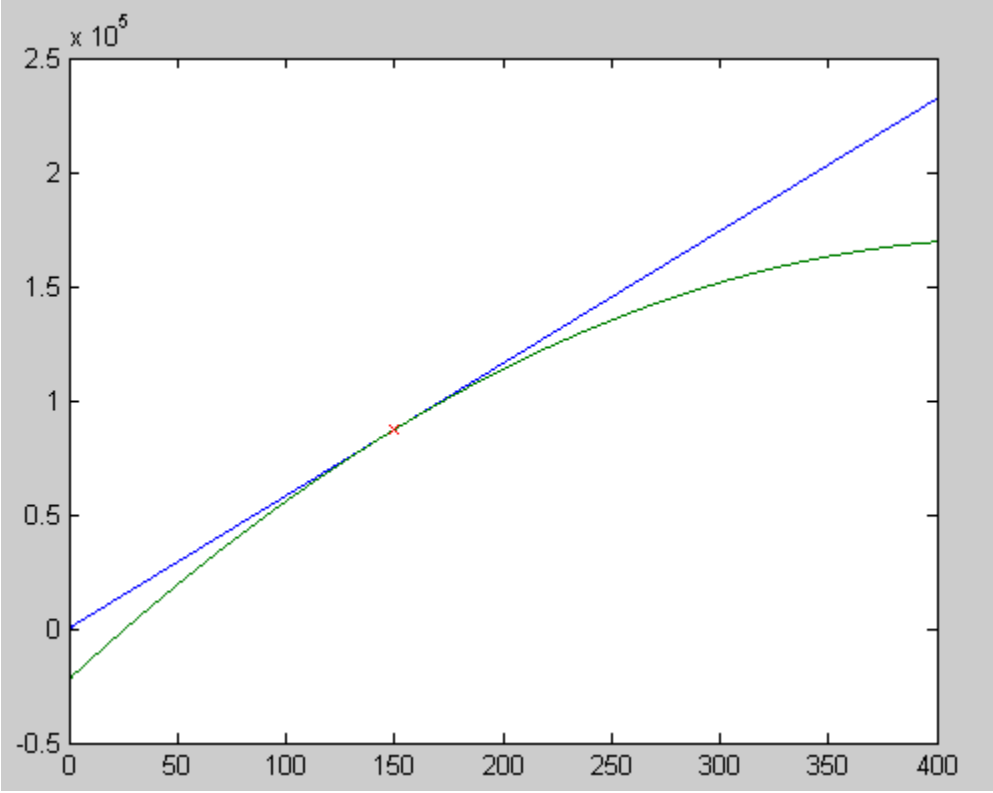

Figure 3-12 External Time Input for Decreasing Frequency Sine Wave

The resulting sine wave can be seen in Figure 3-13.

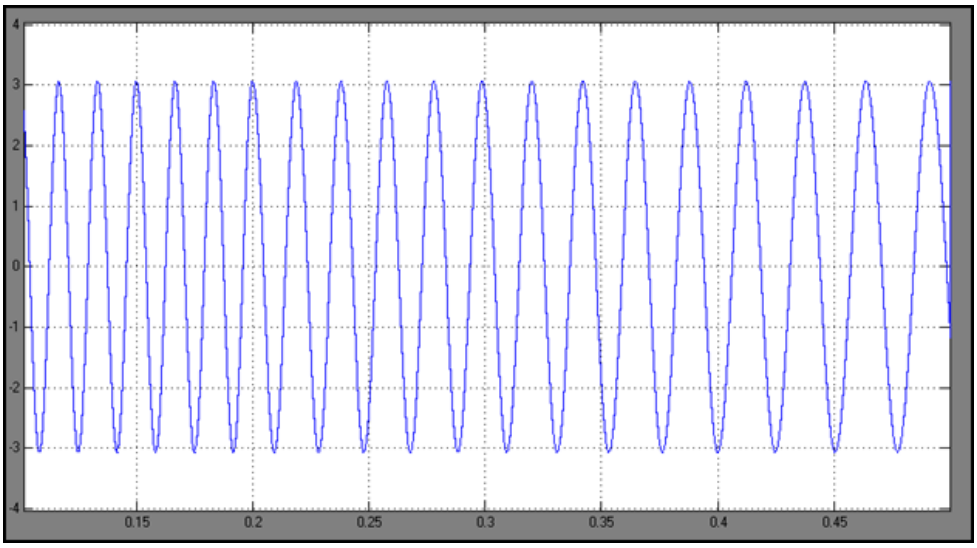

Figure 3-13 Sine Wave with Decreasing Frequency

The parameters for the sine wave block must then be set so that a constant frequency is output at first and then a ramping frequency is output after t = *delay*. The amplitude, phase angle and offset, also called bias, are trivial parameters and are set accordingly, A = 1, Φ = 0 and C = 1.

The frequency parameter is set to give a constant frequency before t = *delay*. For the case of increasing frequency,

$$frequency = \frac{60 * 2 * \pi}{m_1}$$

And decreasing frequency

$$frequency = \frac{60 * 2 * \pi}{m_3}$$

Since the user has the option to set *delay, mFreqInc* and *mFreqDec* to any arbitrary value one more constraint must be imposed to prevent negative frequencies,

$$mFreqInc < delay < mFreqDec$$

Equation 3-16

The linear ramp equation of the frequency can be determined by taking the derivative of ω*t. It can be seen that the slope of this equation is a function of the *delay* and either *mFreqInc* or *mFreqDec.* For increasing frequency ramps the rate is

$$\frac{d\omega_i}{dt} = \frac{60 * 2 * \pi}{delay - mFreqInc}$$

Equation 3-17

For decreasing frequency the ramp rate is

$$\frac{d\omega_d}{dt} = \frac{60 * 2 * \pi}{delay - mFreqDec}$$

Equation 3-18

The constraints imposed by Equation 3-16 cause $\frac{d\omega_i}{dt} > 0$ and $\frac{d\omega_d}{dt} < 0$.

Typical values for these parameters can be seen in Table 3-2.

Table 3-2 Typical Global Variable Values

Global Variable	Value	Ramp Rate
mFreqInc	-240	0.1 Hz/s
mFreqDec	960	-0.1 Hz/s
delay	360	N/A

3.2.2.7.2 Time Test Waveform

The time test for frequency deviations involves quickly changing the frequency of a waveform and measuring the amount of time it takes the inverter to trip. Two different waveforms are created and an instantaneous switch is used to select between the two. One of the waveforms is the generic 60 Hz sine wave and the other is a sine wave with a different, but still constant, frequency. When the simulation time becomes equal to the *delay* variable, the program changes its output from the steady-state 60 Hz waveform to the new waveform. The value of this new frequency is controlled using the *stepSize* global variable. As in the step change of voltage waveforms described earlier, care must be

taken to ensure a smooth transition between the two waveforms occurs. The consequences of not controlling the transition can be seen in Figure 3-14.

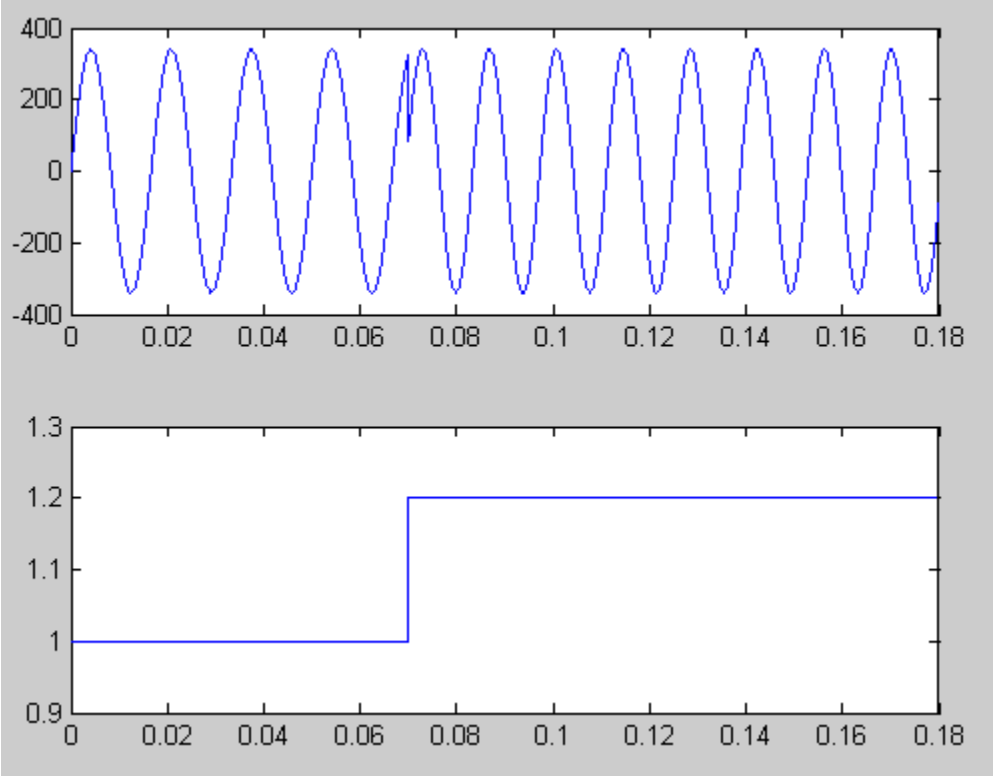

Figure 3-14 Frequency Step Discontinuous Transition

A custom subsystem was designed and implemented to provide smooth transitions. Like in the voltage step transition a zero crossing detection was used to ensure continuous waveforms, but since this test switches between two waveforms of different frequency rather than just amplifying or attenuating a waveform at a constant frequency, a slightly different method of zero crossing detection was used. The Hit Detection block used in the voltage time tests outputs a pulse that is high for the duration of the simulation step size, T_s. Since it is very rare for two sine waves at slightly different frequencies to cross zero during the same time step, a tolerance was used instead. For example, if both of the waveforms have a value between 1 and -1, then the step can occur. This method yields very smooth waveform most of the time. To have consistently smooth waveforms though, an extra layer of constraints had to be imposed. The extra constraint consisted of making sure the waveforms are also

travelling in the same direction. Once both of these constraints are met, the program will transition between the two waveforms yielding an output like that seen in 3-15. It can be seen that the transition does not occur at the same time as in 3-14. This is due to the program waiting until a point where a smooth transition can occur.

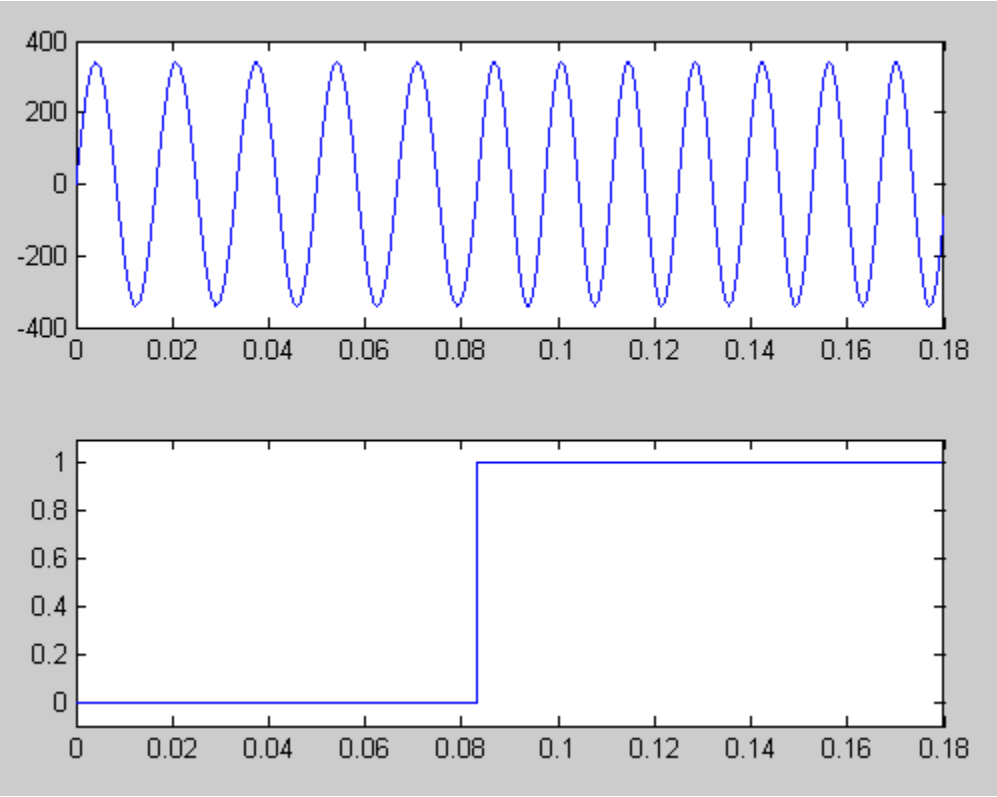

Figure 3-15 Frequency Step Smooth Transition

3.2.2.8 Anti-Islanding Test Waveform

The waveform necessary for the anti-islanding test is just the generic 60 Hz sine wave at the user-defined voltage, V_{rms} . This waveform is consistent until the simulation time is equal to the *endTime* variable. When the simulation time is equal to the *delay* variable, a signal is sent from the RTDS to a shunt-trip breaker that disconnects the grid simulators from the circuit, creating an islanding condition. It is then up to the controller of the inverter to detect the island and disconnect within the specified time limit.

3.3 Load Bank

The power amplifiers used as grid simulators are not bi-directional. This means that power can only flow out of the amplifiers. A place for power to flow is necessary if testing is to occur. A load bank was connected to the simulated grid to give the power a place to flow. The load bank used in this project is the Simplex Titan 162 RLC load bank. Its specifications are listed on page 2 of the Load Bank Technical Manual with relevant ones reproduced in Table 3-3.

Table 3-3 Titan 162kW Load Bank Specifications

Parameter	Value
Capacity	436KVA @ +/- 0.37 pf
Voltage	240/480VAC, 3ϕ
Connection	3 wire
Frequency	60 Hz

It consists of reactive and real elements that are either put into or taken out of the circuit through the use of contactors that are controlled by relays. The relays are controlled by two Analog Devices 6B50 digital I/O boards, each consisting of three modules. Each 6B50 board is controlled by a MicroDAC LT controller that communicates with an external computer via the RS-485 serial communication protocol. The real power settings can be controlled in a minimum of 125W steps, while the reactive power settings can be controlled in a minimum of 312.5VAR steps.

3.3.1.1 Serial Communication

Control of the load bank is necessary if different scenarios are to be tested. For this thesis it was controlled through the RTDS. This required the integration of a serial communication card into the RTDS, interfacing that card with the load bank controller and development of a model in Simulink to send the correct signals to the load bank controller.

The serial communications card used for this project was the BlueStorm/LP 8-port PCI card developed by Connect Tech Inc. It is capable of being configured for RS-232 or RS-422/485 in full-duplex

or half-duplex mode through a series of hardware jumpers. The BlueStorm card was initially installed on the RTDS with a QNX operating system. Since the MicroDAC LT controller in the load bank uses RS-485 in half-duplex mode, port 5 of the BlueStorm card was configured accordingly. This was accomplished by jumpering pins JE1, JE2, JE3 and JE4. The port then had to be configured in the operating system for RS-485 half-duplex communication. This was accomplished by first installing drivers provided by Connect Tech Inc. Then the rc.local file from the QNX operation system had to be modified to include the following lines to start the driver at boot up, disable flow control and configure the correct port.

```
# devc-serCtiPciUart -F &
# ctty +rts </dev/ser7
```

Since ports 1 and 2 are internal to the QNX system, there is an offset of 2. The ctty code setting ser7 (serial port 7) to half-duplex mode, corresponds to physical port 5. Once the port was configured correctly, it was tested using the "qtalk" program included with QNX. This program allows users to test the communication on a port. First, two ports were connected together in a loop-back configuration. This necessitated configuring port 6, or ser8, for RS-485 half-duplex mode in addition to port 5. Data was written to port 5 and read by port 6, then displayed to verify communication.

After loop-back communication was verified in QNX, it was then tested using an asynchronous communication example program developed by Opal-RT. Finally, communication with a LabVIEW program on a separate computer was tested. The reason for this was that there was an existing load bank control program developed in LabVIEW on another computer and it was necessary to validate communication. The serial communication between the load bank and the LabVIEW program used the National Instruments (NI) PCI-8431/2 card and the connections were configured to work with the DB-9 output on the NI card. Since the connections from the BlueStorm card were different, an intermediate

cable had to be fabricated to facilitate communication between the BlueStorm card and the load bank and NI card. The wiring diagram is shown in Figure 3-16.

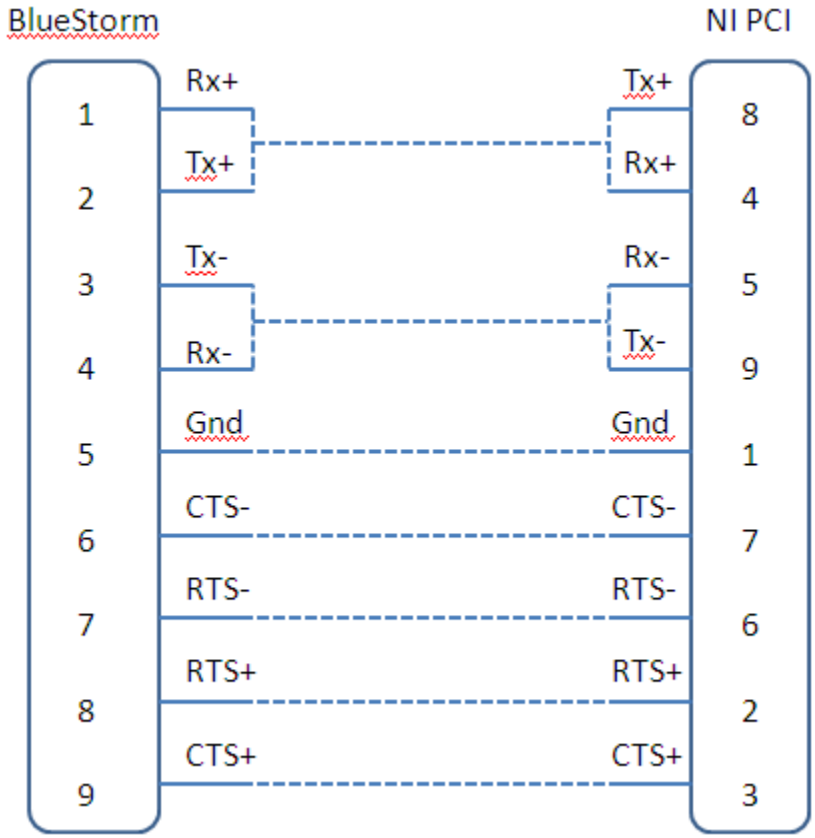

Figure 3-16 BlueStorm and NI PCI Connection Diagram

Once the wiring was completed, the qtalk program was used in conjunction with a simple LabVIEW serial communications program to verify that the wiring was correct. Next, communication between the RTDS and the LabVIEW computer was tested. RT-LAB [**38**], the program provided by Opal-RT to interact with the RTDS, was used to monitor the data instead of qtalk. The AsyncSerial Simulink example model was used to send data from the RTDS to the LabVIEW computer. After all of the basic communication had been verified, it was time to use the RTDS to communicate with the control boards in the load bank.

RS-485 protocol requires that both the sender and receiver communication parameters are configured the same way. The configuration parameters for the load bank controller are shown in Table 3-4.

Table 3-4 Load Bank Controller Serial Communication Parameters

Parameter	Value
Baud Rate	9600
Parity Bit	None
Stop Bit	1
Flow Control	None

The RTDS system must then be configured so that its parameters correspond to those of the load bank controller. In Simulink, Opal-RT provides an Application Programming Interface (API), called AsyncAPI, to facilitate serial communication. A library of blocks for interacting with the API are supplied. The three blocks provided are OpAsyncGenCtrl, OpAsyncSend and OpAsyncRecv. The OpAsyncGenCtrl block defines the controller ID, communications (comm) port number, baud rate, parity, data size, stop bit(s), flow control and name of the executable and starts an asynchronous serial process. The controller ID allows the user to implement more than one serial communication process in one model. All subsequent OpAsyncSend and OpAsyncRecv blocks are referenced to a controller through the controller ID. The parameters are shown in Table 3-5.

Table 3-5 Model Serial Communication Parameters

Parameter	Value
Controller ID	1
Comm Port Number	7
Baud Rate	9600
Parity	None
Data Size	8 bits
Stop bit(s)	1
Flow Control	None
Name of Executable	AsyncSerial

The OpAsyncSend block passes data to the shared memory which is then referenced by the AsyncAPI. The API then passes the data to the serial communication PCI card. The block has two input ports and one output port. The input ports are Data ready and Data. The Data ready port writes what is currently in the Data port to shared memory whenever the signal input is 1. The output port displays errors thrown by the AsyncAPI.

Using the OpAsyncSend block, two types of commands are sent to the MicroDAC LT load bank controllers using the ASCII data format. Both commands are structured by first sending a delimiter character, followed an address, then a command and finally an end character.

The first type of command is a query command. When the load bank controller receives this command, it will respond with the current values of the digital I/O boards that control the relays. The delimiter for a query command is '$' or '36' in ASCII. For example, if the status of the fan, cooling and operation was to be checked, '$016(cr)' or '36 48 49 54 13' would be fed to the Data port of an OpAsyncSend block and a signal of 1 to the Data ready port. '01' represents the address of board 1, where the fan, cooling and normal operation input modules are. '6' represents the status command and (cr) is the end character.

The second type is a set point command. This command tells the 6B50 board which relays to energize. The delimiter is '#' or '35' in ASCII. The addressing for a set point command requires that not only a board is specified, but also each module within a board. For example, if the 1kW contactor was to be closed, the command '#010B02(cr)' or '35 48 49 48 66 48 50 13' would be sent. This command sets board 1, module B, output module 2.

The OpAsyncRecv block reads the most current value from the shared memory. It has a timeout input port that can be used to detect if the data is not updating. It also has three output ports, error, status and data; used for throwing an error, showing the status and displaying the data [**39**].

Upon interfacing the AsyncSerial example program with the load bank, it was noticed that the response from the load bank was inconsistent. Only part of the character stream would be received. The 6B50 manual specifies that values sent from the 6B50 to the RTDS can vary in size, such as '>(cr)' for acceptable set point command or '!0F0000(cr)' for a status query. Since the response is important for validation of set points and status checks a modification of the included AsyncSerial.c source file was necessary. This file handles the communication protocol and structures the data accordingly. It was found that increasing the buffer size for the incoming data to 12 bytes resulted in a consistent response from the load bank.

Once this rudimentary communication was established, a model of the load bank needed to be developed in Simulink. The goal was to create a program where the user enters a set point for resistance or real power, capacitance, inductance or reactive power and the program sends the correct strings of data to the load bank to switch the necessary elements on or off the circuit upon the user's command. A model of the load bank had already been developed by Sudipta Charkraborty (NREL) and Seth Hopkins (Colorado School of Mines) using the SimPowerSystems library in Simulink [**40**]. Though this model was never developed to the point where it actually communicated and controlled the Titan 162, it provided a good reference.

The first step was to remove all components of this model except the embedded MATLAB functions that generated the character strings for commanding the load bank. Once this was completed, user control methods were added and the asynchronous serial blocks were implemented to facilitate communication with the load bank. In order to verify that the program worked, the output character strings were monitored and compared to those of the LabVIEW program. Also, the line-to-line resistance was measured and recorded. The output character strings and resistance values did not match for multiple set points. Upon investigating the embedded MATLAB blocks that were reused from original load simulator program, it was found that the delimiter and board addresses matched those of

the LabVIEW program, but the set point values were in reversed order. When these values were flipped, everything matched with the LabVIEW program.

For total assurance, the new load bank control program was tested with an 80kW Cummins Onan diesel generator. Output power of the diesel generator was monitored and is compared to user set points in the graph below for real power settings. It can be seen from this graph that the user set points and measured output power agree. The standard error was less than 1% from 1kW to 80kW.

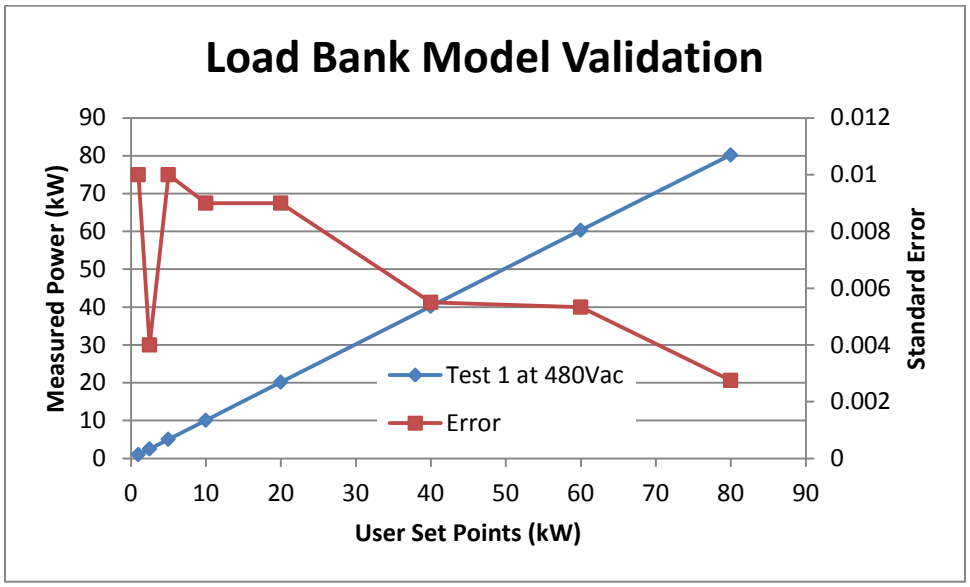

Figure 3-17 Programmed and Measured Values for Load Bank Set Points

Next a power factor setting was added to the console. If the value in this box is less than one, the real power value input is ignored. Instead, a subsystem calculates the real power value from the reactive power values and the power factor. The derivation for this calculation is given below.

Power factor is defined as,

$$pf = \frac{P}{S}$$

Equation 3-19

where,

pf = power factor,

P = real power,

S = apparent power.

Apparent power is defined as

$$S^2 = P^2 + Q^2$$

Equation 3-20

Where the reactive power Q is

$$Q = Q_L - Q_C$$

Equation 3-21

Q_L is inductive reactive power and Q_C is capacitive reactive power.

Substituting for S in Equation 3-19 and solving for P gives

$$P = Q * \sqrt{\frac{pf^2}{1 - pf^2}}$$

Equation 3-22

Then a control that lets the user set the operating voltage was also added to the console. The user may control whether the load bank is in 240V operation or 480V operation by use of the Operating Voltage switch. This switch controls a relay in the load bank that switches a different configuration of elements into the circuit based on which voltage is specified.

The final step in developing the load bank program was to add protection. The load bank has internal protection that removes all elements from the circuit if an error is detected, but another layer of protection was added on the user side for two reasons. One is increasing safety through redundancy and the second is to provide an indicator to the user for which error has occurred. Errors during load

bank operation can come from fan failure, over temperatures or abnormal operation. The program queries the controller for the fan status, cooling status and normal operation status. If an error is detected, the user set point is immediately overwritten with a value of 0 with the purpose of removing all elements from the circuit.

Implementing this protection scheme, whilst allowing the user to command a new set point value at an arbitrary time, required the use of a state machine. The diagram below shows how the state machine works.

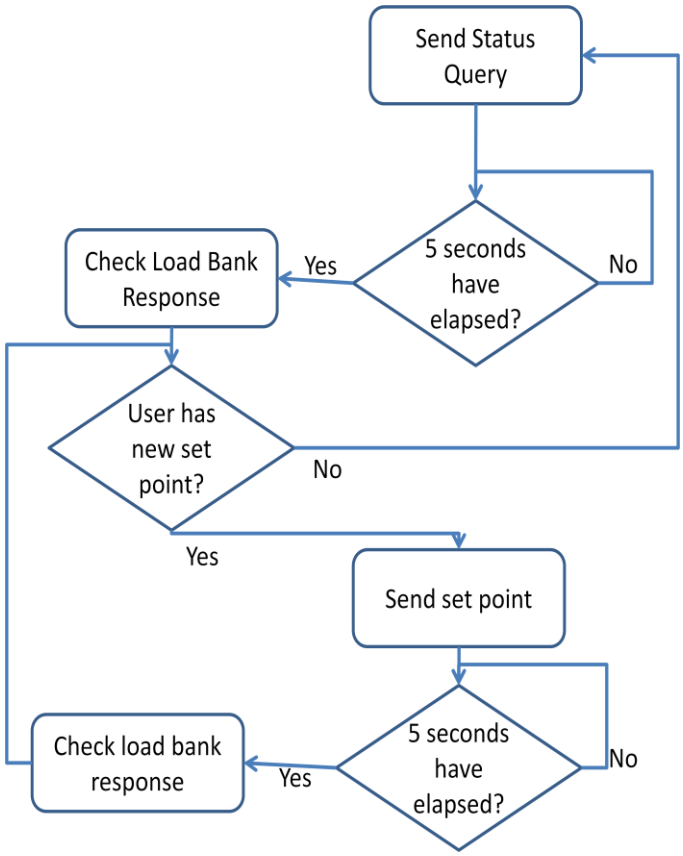

Figure 3-18 Load Bank Program Operation Flow Diagram

First a status query is sent. It was experimentally determined that the load bank takes 5 seconds, at the most, to respond. Checking the receive buffer before a response is received could cause an incorrect failure detection which would force the program to overwrite the set point to 0kW. Once the 5 seconds have elapsed a signal is sent to the Status Check triggered subsystem that masks the

values in the receive buffer for fan status, cooling status and normal operation status. If any of them are 0, then the program overwrites the set point to 0kW. If these values are all 1, then the program proceeds to check whether the user wants to send a new set point, indicated by the position of a switch on the console subsystem. If the switch is in position 1 then a new set point is sent, otherwise the state machine returns to the beginning. After sending the set point the program waits 5 seconds, and then sends a signal to trigger the Set Point Check subsystem. This subsystem checks the receive buffer to see if a valid command has been sent. This is indicated by a '>' or ASCII '62'. If the command is valid, then it is displayed to the user on the console and they may return the switch to position 0, returning the state machine to the beginning. If the switch remains in position 1, then the program will keep sending the set point and updating the user on whether a valid command was sent or not.

3.3.1.2 Program Operation

Like the grid simulator program, the load bank program is also divided into master and console subsystems. The console is where the user interacts with the model. User input is divided into three categories that may be modified independently or simultaneously. Each category has a box for numerical input and a switch for selecting what type of input. The first category is real power. The user may specify, by use of the switch, whether the value they have entered is for real power in kW or for resistance in Ohms. The second and third categories are reactive power. One can be switched between negative reactive power, in the absolute value of kW, and capacitance, in farads, while the other can be switched between positive reactive power, in kW, and inductance, in Henrys. There is also an input that allows the user to specify a power factor and operating voltage at either 240V or 480V.

When the program is running, it can be in one of two states. Steady state operation is signified by placing the Operating Mode switch in the 'Run' position. Transient operation, where the user's set points are sent to the load bank, is signified by placing the Operating Mode switch in the 'Set New Values' position.

The console also has two feedback displays. One shows the status of the load bank fan, temperature and normal operation. This display can be instructive if any problems occur with the load bank. The other shows the user when a valid set point has been commanded. Serial communication is not 100% reliable and sometimes it is necessary to send a command more than once. This display tells the user when a valid command has been sent and it is ok to move the Operating Mode switch back to the 'Run' position.

The order of operations for successfully controlling the load bank with this program are:

1. Energize control power to the load bank
2. Load LoadBank200kWnew on the RTDS
3. Execute the program
4. Wait for a value of '1' in 'Fan OK', 'Cool-1 OK', 'Cool-2 OK' and 'Normal Operation' displays
5. Set the Operating Voltage switch to desired position
6. Set the Load value desired
7. Change the Operating Mode switch to 'Set New Values'
8. Wait for a value of '1' in the 'Good Command' display
9. Change the Operating Mode switch to 'Run'
10. Repeat steps 5 through 9 for new set points

3.3.1.3 Load Calculations

Calculating the load settings is an important step because it will determine the quantity and type of power that will exist in the simulated grid. Certain modifications must be made for split-phase operation. IEEE 1547.1 defines what type of load must be used for anti-islanding testing.

3.3.1.3.1 Split-Phase Load Calculations

The load bank has a 3 phase configuration and the power set points in the load bank program assume 3 phase, 240V or 480V operation. But the PV inverter used for testing was split-phase, 240V nominal operation. To accommodate this, two changes have to be made. First, one of the fuses for one of the load bank phases was removed as a safety measure to prevent any unwanted circulating currents. Second, the load calculations have to be modified. In order to determine the conversion between three phase power, $P_{3\phi}$ and split-phase power, $P_{s\phi}$ it is instructive to look at how $P_{3\phi}$ is calculated.

A diagram of the basic 3 phase, balanced load, configuration is shown below.

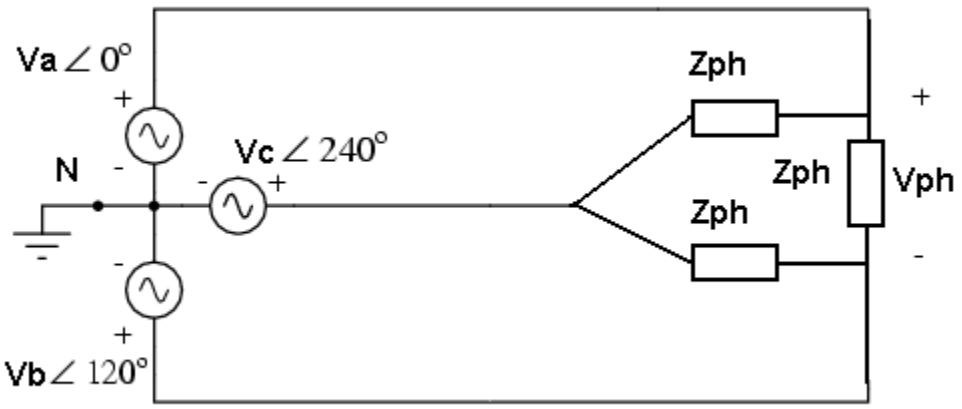

Figure 3-19 Typical 3-Phase Circuit with Delta-Connected Load

Three phase power is calculated as three times a single phase's power for a balance load,

$$P_{3\phi} = 3 * \frac{V_{ph}^2}{Z_{ph}}$$

Equation 3-23

Now the equivalent impedance seen from a split-phase configuration must be calculated. A diagram of the split phase configuration is shown below.

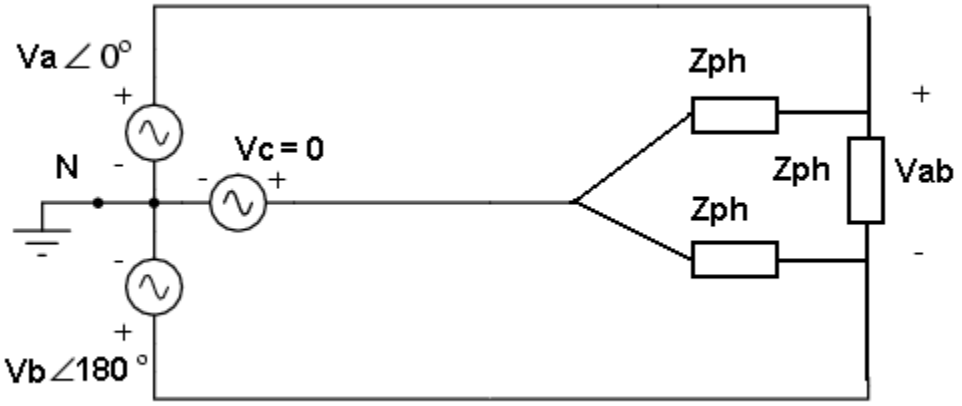

Figure 3-20 Split-Phase Circuit with Delta-Connected Load

In this configuration, the inverter is connected from Phase A to Phase B. Since the 120V waveforms, V_a and V_b, are 180° out of phase, a voltage of 240V will be present at V_{ab}. Holding Phase C to 0V and keeping Phase A and Phase B 180° out of phase effectively forces the node at the positive terminal of Phase C to 0V. Therefore the equivalent impedance, Z_{eq}, seen from Phase A to Phase B is

$$Z_{eq} = (Z_{ph} + Z_{ph})||(Z_{ph})$$

Equation 3-24

This can be reduced to form a simple equation for Z_{eq} in terms of Z_{ph}

$$Z_{eq} = \frac{2}{3} * Z_{ph}$$

Equation 3-25

Now calculating split-phase power from Phase A to Phase B gives,

$$P_{S\phi} = \frac{V_{ab}^2}{Z_{eq}}$$

Equation 3-26

Substituting Z_{ph} for Z_{eq} and V_{ph} for V_{ab} gives,

$$P_{S\phi} = \frac{V_{ph}^2}{\frac{2}{3} * Z_{ph}}$$

Equation 3-27

Finally, substituting Equation 3-22 into Equation 3-26 gives split-phase power in terms of three-phase power

$$P_{S\phi} = \frac{3}{2} * \frac{1}{3} * P_{3\phi}$$

$$P_{S\phi} = \frac{P_{3\phi}}{2}$$

Equation 3-28

If 6kW of load is desired for split-phase 240V configuration, a set point of 12kW must be entered into the load bank program with the Operating Voltage switch in the 240V position. Since the inverter's nominal voltage and the load bank voltage setting are the same, it was possible to substitute V_{ab} for V_{ph} in Equation 3-26. If the load bank was configured for a different voltage, a direct substitution would not be possible.

3.3.1.3.2 Anti-Islanding Test Load Calculation

A resonant circuit is to be used for anti-islanding testing. After the EPS disconnects, an island is formed with the resonant circuit and the DR. The circuit is to resonate at the nominal operating frequency of the simulated EPS so that the DR is forced to determine under the worst case scenario whether the simulated EPS is regulating the frequency or if it is just the ringing of the resonant circuit. A power factor of 1 is indicative of a resonant RLC circuit where the real power and reactive power are balanced. IEEE 1547.1 provides equations for determining the real power and reactive power settings required. Their method is very helpful for getting a general idea of what level of power will be required, but does not always yield the best results. Component tolerances or available load steps can cause the calculation to not work the way it is intended to. For this thesis, two iterative methods have been developed to obtain a resonant circuit with real world components that has a power factor very close to 1.

The first method involves determining how much real power will be necessary. It is important to properly size the load. Once the island is formed, the only device energizing the load will be the DR. If the load is too large, it could damage the DR. Likewise, if the load is too small and the DR has some

type of control algorithm, like MPPT, it may provide too much power to the load, causing the voltage to swell. It is appropriate to size the real power to meet the maximum real power output of the DR.

The next step is to determine how much reactive power is necessary. This program divides reactive power into inductive reactive power and capacitive reactive power. With the simulated EPS supplying real power to the load bank, the inductive reactive power should be incremented until a power factor of 0.707 is measured. This indicates that the real power is equal to the reactive power. Next the capacitive power should be incremented until a power factor of one is reached. This indicates that a resonant circuit has been configured because the grid simulator is supplying no reactive power.

If a power factor measurement is not available, it is also possible to determine the reactive power component values using a second method. First, set the values for inductive and capacitive reactive power equal to the real power setting and energize the load with the simulated EPS. Ideally this should make a perfect resonant circuit. In practice it most likely won't. The next step is to monitor the RMS of the current flowing out of the simulated EPS and increment or decrement either the inductive or capacitive reactive power setting until a minimum current is reached. In a perfect resonant circuit, no current needs to be supplied. If an amount of current is observed above the minimum achievable for a constant real power setting, it is reactive current that is supplying an unbalanced LC circuit.

3.4 Real Time Data System

The RTDS is at the heart of the HIL system. It can be used for control, data acquisition and computational power. The RTDS used for this thesis was manufactured by Opal RT Technologies. It's composed of a host machine and a target machine. The host machine has a Windows XP operating system and includes a program called RT-Lab 10.0.5 that is also developed by Opal RT Technologies. This program compiles a Simulink model into C code using the Real Time Workshop add-on from MATLAB and then transfers the C code to the target machine. It also handles real-time communication between the host and target machines over an Ethernet connection. It can be interfaced with Python to

automate execution and program control. Since MATLAB can also be installed on the host machine, development and testing can both take place on the same computer.

The target machine is the main computing power, signal processing and communications device. These machines are intended to be run in real-time. Typical concerns with real-time machines are processing speed, I/O capabilities, accuracy and stability [**41**]. These concerns are addressed by integrating multi-core processors, analog and digital patch panels and FPGAs all into one system. Fixed-step Simulink solvers can have small step sizes to give high resolution which improves accuracy. Models can be divided into subsystems that are each assigned their own CPU which improves speed. Multiple target machines may be paralleled to increase processing power. Patch panels make analog and digital input and output ports easily accessible. RT-Lab includes special library blocks for Simulink that facilitate easy and effective use of each of these components. These aspects make for a very powerful and easy to use system.

One target machine was used for this thesis. It is the Wanda 4U developed by Opal RT. Relevant technical specifications provided by Opal RT [**42**] are reproduced in Table 3-6.

Table 3-6 RTDS Target Machine Specifications

Items	Quantity	Description
Operating System	1	Linux RedHat 5.2
CPU	2	Intel Xeon QuadCore 3.2 GHz, 6.4 GT/s, 8M Cache
Total Core #	8	N/A
Memory	2	1GB
Motherboard	N/A	X8DAL-I-O Supermicro Motherboard Dual Xeon (i7)
Digital to Analog Card	2	OP5330 16-channel, 1MS/s per channel
Analog to Digital Card	2	OP5340 16-channel, 400 kS/s per channel
Digital In/Digital Out Card	1	OP5251 32-channel In and 32-channel Out
FPGA	1	OP5142 256-channel Digital I/O

A patch panel was used to send and receive analog signals for control of devices, trigger events and loop-back verification. The Table 3-7 details these connections.

Table 3-7 RTDS Patch Panel Connections

Patch Panel			Connecting Device	Purpose
Slot	Module	Channel		
1	A	0	UPC32 Port J5 Pins 11 & 23	Phase A control
1	A	1	UPC32 Port J5 Pins 12 & 24	Phase B control
1	A	2	UPC32 Port J5 Pins 13 & 25	Phase C control
1	A	3	PZ4000 Channel 5	Scope Trigger
1	B	0	Patch Panel Slot 1 Module A Channel 0	Loop-back Monitoring
1	B	1	Patch Panel Slot 1 Module A Channel 1	Loop-back Monitoring

3.5 Inverter

The inverter that was characterized in this thesis was the Fronius IG 3000 [**43**]. This is a grid-tied, full-bridge, PV inverter that utilizes a high frequency transformer to reduce its size and weight. It utilizes split-phase operation. Various control schemes are implemented to synchronize output with the grid, operate at the PV array's maximum power point, monitor the grid for conditions that may indicate a problem and automatically disconnect if a problem is detected. Voltage, frequency and islanding conditions are the grid conditions that are monitored for aberrant behavior [**43**]. It has been certified to comply with IEEE 1547 and UL 1741-2005 grid interconnection standards and NEC 690 building code requirements. A diagram of the inverter taken from a presentation by Fronius can be seen in Figure 3-21.

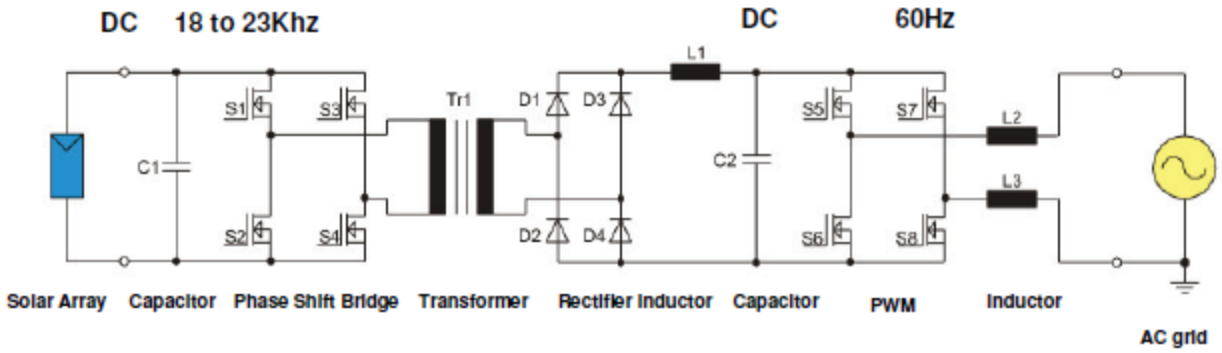

Figure 3-21 Schematic of Fronius Inverter with High Frequency Transformer

Specifications are given in the Fronius manual on pages 68-69 [**43**]. Relevant specifications are reproduced in Table 3-8.

Table 3-8 Fronius IG 3000 Specifications

Specification	Value
MPP-voltage range	150-400 V
Maximum Usable Input Current	18 A
Nominal Output Power	2.5 kW
Maximum Continuous Output Power	2.7 kW
Nominal AC output Voltage	240 V
Operating AC voltage range	212-264 V
Voltage trip limit accuracy	+/- 1.5 %
Maximum output current	11.25 A
Operating Frequency range	59.3-60.5 Hz
Frequency trip limit accuracy	+/- 0.02 Hz
Maximum Efficiency	95.2 %
Reconnect Time	305 s

There is a LCD screen on the front of the inverter that indicates the inverter's operating state and power output. A table describing the state codes is listed on page 63 of the Fronius manual [**43**]. The state codes relevant to this thesis are shown in Table 3-9.

Table 3-9 Fronius State Codes

State Code	Description
104	Grid frequency not within acceptable range
108	Islanding detected
221 or 223	Grid voltage exceeds admissible limits
222 or 224	Grid voltage below admissible limits
225	No grid voltage detected

These state codes were used to confirm the cause of trip for the inverter.

3.6 Connections

The different grid elements were connected together using the AC bus at the DERTF. The bus is a centralized connection point made of copper bars that are each rated to 400A. It is the main avenue for power flow and monitoring. At DERTF there are three different isolated AC busses to allow for different

experiments to be run at the same time. Fifteen different devices are ready to be connected at will to any one of the three busses. A computer program controls contactors that either connect or disconnect each device from the bus. For the purposes of testing inverters for this thesis, the Titan 162 load bank, AC Device #11, the Pacific Power grid simulators, AC Device #2 and the Power Electronics (PE) Bench, AC Device #14 had to be connected to the same AC bus. A diagram of the power connections can be seen below.

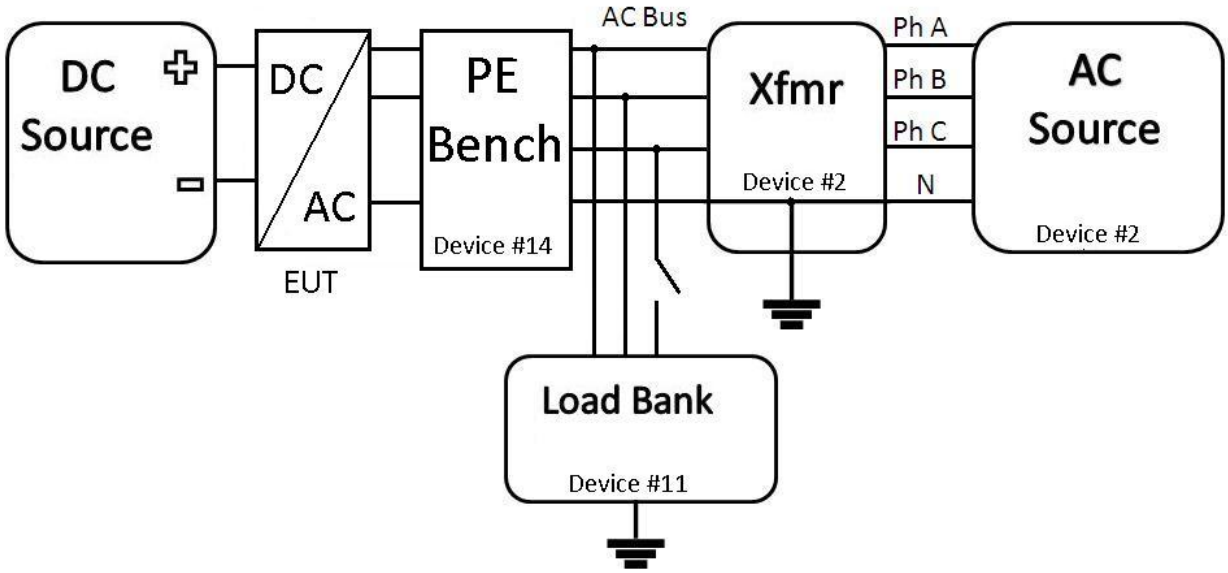

Figure 3-22 Simulated EPS Power Connections

The PE Bench was used because it provides a convenient connection point to the AC bus for the inverter. A female four-wire AC plug on the PE Bench was used to connect the inverter to the bus. Since the inverter operates in split-phase, a custom male plug had to be constructed. Line 1 and Line 2 from the inverter output breakers were connected to the plug's metal prongs corresponding to Phases A and B. Phase C was left unconnected and secured inside the plug housing. The ground terminal in the inverter was tied to the neutral terminal and a wire was connected to the neutral prong on the plug.

3.7 Data Acquisition

Five waveforms were captured for analysis. The purpose of analyzing these five waveforms was to determine the voltage or frequency magnitude at the trip point for ramp tests, the trip time for step

tests and verification of proper operation. The five waveforms measured were AC line to line voltage, AC phase current, DC voltage, DC current and RTDS trigger output. Each of these waveforms was captured and recorded using a Yokogawa PZ4000 Power Analyzer. This scope was chosen because it has both voltage and current sensor inputs and is easily interfaced with a PC using a GPIB communications interface. It has four voltage channels and four current channels which sample using an A/D converter [**44**]. The connections and resulting data files arrangements are shown in Table 3-10.

Table 3-10 PZ4000 Scope Channel Descriptions

PZ4000 Channel	Waveform
1	V_{AC}
2	I_{AC}
3	V_{DC}
4	I_{DC}
5	Trigger

3.7.1 Measuring Devices

Correctly determining the time when the inverter ceased to energize the grid required monitoring the AC current output of the inverter. This measurement was taken on the phase A line connecting the inverter to the PE Bench by a AEMC MN 261 AC current probe. The inverter's maximum current is listed at 11.25 A in the Fronius manual [**43**]. The probe has two possible settings, 100 A or 10 A. Since the output current of the inverter could be greater than 10 A, the 100 A setting was used. This will hinder the resolution of the probe to only 10mV/A, but it was sufficient for determining the trip point. The DC current was also measured using an AEMC MR 561 AC/DC current probe. The 150 A setting gives a resolution of 10mV/A. Each current probe can measure a minimum of 0.4 A.

A line-to-line voltage was measured from phase A to phase B on the AC bus. The peak expected voltage was 424 V so a setting of 600 V_{max} was used on channel 1. DC voltage was measured on the input terminals of the inverter using direct connections to the scope's voltage terminals. This voltage was a constant 350 V. The inverter does employ a MPPT algorithm, though with a constant voltage

source, it always operates at maximum power. Channel 3 was set to 600 V_{max} which put this waveform in the middle of the scope screen.

3.7.2 Triggering

For ramp tests, the scope was configured for a single capture using the falling edge of I_{DC} on channel 4 as the trigger. For step tests, single capture mode was also used, but a different channel was designated as the trigger. The rising edge of the HIL trigger analog output on slot 1 module A channel 3 indicated when a step change had occurred. Therefore, the waveform on scope channel 5 was used as a trigger. Depending on which test was being performed, different record lengths were used which also changed the sampling rate. The record lengths ranged from 400ms, with a sampling rate of 250 kS/s, for a fast trip to 2s, with a sampling rate of 50 kS/s, for a slow trip.

3.8 Integration of Components

Characterizing inverters using HIL requires the simultaneous use of all of the previously described components. Each subsystem was developed individually. The intent was to integrate the load bank program and grid simulator program into one program that can be centrally controlled. This has not yet occurred due to the unavailability of the system.

3.8.1 Power Flow

The grid simulators are the main source of power. They energize the AC bus throughout the entirety of testing. They scale back their power whenever the inverter begins to energize the AC bus. The power from the bus flows to the load bank where it is consumed.

For this thesis, the load was set to 6 kW to provide a stiff grid for when the inverter comes online. Some power calculations should be performed before testing begins to verify proper operation. An example of what was used for this thesis is provided below.

With the inverter offline the grid simulator current can be calculated as,

$$I_{gs} = \frac{P_{load}}{2 * V_{gs}}$$

Equation 3-29

where,

I_{gs} = grid simulator split-phase current,

V_{gs} = grid simulator split-phase voltage,

P_{load} = load bank split-phase power setting, calculated using Equation 3-27.

If V_{gs} = 240V and P_{load} = 12kW, then I_{gs} = 25A.

If the inverter is energizing the grid, the grid simulator current can be calculated as,

$$I_{gs} = \frac{P_{load} - 2 * P_{inv}}{2 * V_{gs}}$$

Equation 3-30

where,

P_{inv} = inverter AC output power.

If P_{inv} is assumed to be a maximum of 3kW, then the minimum I_{gs} = 12.5 A. If these values are not observed for the same set-up, it is possible that the load or the V_{rms} global variable have been configured improperly.

3.8.2 Control/Order of Operations

Operating this system requires a sequential set of steps.

1. Verify that all generation sources are off or disconnected
2. Inverter Set Up
    a. Remove the front cover of the inverter and disconnect the communication ribbon
    b. With the AC and DC plugs disconnected from the PE bench, connect one of the two phase lines from the plug to the inverter's AC output breaker L1
    c. Connect the other phase to the inverter's AC output breaker L2
    d. Connect the neutral line to the N terminal and tie this terminal to the inverter's ground terminal
    e. Place the AC probe on one of the phases
    f. Connect the positive wire from the DC plug and the positive DC voltage measurement wire to the PV+ terminal in the inverter
    g. Connect the negative wire from the DC plug and the negative DC voltage measurement wire to the PV- terminal in the inverter
    h. Feed all wires out of a hole in the chassis, reconnect the communication ribbon and replace the front cover
    i. Place the DC current probe on the positive DC power line with the arrow pointing towards the DC source.
3. Scope Set Up
    a. Make connections for AC voltage and current and DC voltage and current measurements
    b. Make connection for HIL trigger output
    c. Set appropriate settings for each channel
    d. Make GPIB connection with computer
4. Bus Set Up
    a. Verify that nothing is connected to the AC bus that will be used
    b. Close the contactors for grid simulator, load bank and PE bench
5. Load Bank Set Up
    a. Calculate the required load bank setting for split-phase operation
    b. Turn on the load bank
    c. Load and execute the load bank program "LoadBank200kWnew" on the QNX RTDS and verify normal operation
    d. Set the load bank to the set point calculated
    e. With the grid simulator transformer output circuit breaker open, verify that the expected value of resistance is measured at the PE bench
6. Grid Simulator Set Up
    a. Make connections between HIL analog outputs and Port J5 on UPC32
    b. Power up the grid simulators and verify proper operation
    c. Power up the UPC32 and verify proper operation
7. DC Source Set Up
    a. Power up the AV-900
    b. Set the appropriate limits on the front panel
    c. Verify that the proper voltage and polarity is applied at the DC female plug
8. Make Power Connections

a. With the DC source and grid simulators disconnected from the AC and DC female plugs, plug the male inverter plugs into their respective female plugs
b. Reconnect and power up the DC source and grid simulators
c. Verify that the inverter LCD screen reads “STATE XXX”

9. RTDS Set Up
    a. Connect Loop Back scheme
    b. Set the appropriate parameters for the desired testing scheme in “IEEE1547Tests”
    c. Compile the model into C code if necessary
10. Perform Tests
    a. Load grid simulator program “IEEE1547Tests” on the RedHat RTDS
    b. Execute the program
    c. Verify that inverter LCD screen reads “STARTUP”
    d. When the reconnection time has elapsed, the inverter should begin to draw current from the DC source and energize the AC bus
    e. When waveforms have ramped to zero, stop the program and save captured scope data
    f. Repeat from step 10a

3.9 Summary

This chapter described a methodology for characterizing an inverter using PHIL. The benefits of using PHIL for this purpose were detailed. The hardware configuration, including control and power connections, was described. Software programs developed for this project were described as were the steps for performing characterization tests.

The methodology explained in this chapter can be used to characterize a grid-tied device with relatively little knowledge about control algorithms or other internal operation aspects. This could be an extremely useful tool for engineers trying to study the effects of integrating DR in various configurations.

4 Test Results

When modeling a grid-tied inverter it is desirable to know how it will react to various conditions. It is likely that little information is provided about the inverter's controller or other embedded protection. The goal of performing these tests is to determine specific grid integration characteristics of an inverter by simulating various grid conditions and measuring the response of the inverter. The tests performed and results that are provided below include reconnection time, abnormal voltage, abnormal frequency and anti-islanding tests.

4.1 Reconnection Time

The first tests performed with the HIL system were to determine the reconnection time setting. The reconnection time setting in the inverter's controller dictates how long the inverter needs to measure consistent normal operating conditions before it will begin to export power. This setting is meant to provide a layer of safety. When fault conditions occur on an EPS, fixes can be incomplete or unsafe. The reconnection time control algorithm prevents grid-tied DR from reconnecting until safe conditions are established. Since the inverter will not operate until the reconnection time requirements have been met, it is necessary to determine this time so that tests can be performed while the inverter is operating normally. Section 3.1.2.5 details the procedure for determining the reconnection time. Results of these tests can be seen in Table 4-1 below.

Table 4-1 Reconnection Time Results

Test Iteration	Reconnection Time
1	307 s
2	306 s
3	306 s

The results were compared with the manufacturer's stated reconnection time to verify that they are correct. The Fronius IG 3000's default reconnection time is listed in the Annex on page 69 of the

Operation Manual as 305 seconds [**43**]. Thus these tests agree with the manufacturers specified reconnection time to a reasonable degree of accuracy.

4.2 Abnormal Voltage

The abnormal voltage waveforms are meant to test an inverter's ability to detect dangerous conditions and the time it takes to trip off. Small changes in grid voltage are common occurrences. Increasing load causes the voltage to dip and decreasing load causes the voltage to swell. These types of events are usually not dangerous and thus do not require an inverter to disconnect from the grid. Large voltage changes can be caused by fault conditions such as short circuits. If the voltage changes dramatically, it is imperative that the inverter detect the change and cease to energize the grid in a timely manner so that dangerous or damaging conditions are avoided. Two types of tests are performed to determine at what voltage level the inverter will trip and how quickly the inverter can detect abnormal voltages and trip.

4.2.1 Magnitude

The magnitude test, as described in Section 3.1.2.6.1, is meant to verify that the inverter trips at a level within the manufacturer's specified tolerance. The simulated grid voltage is ramped up or down slowly to test this feature. IEEE 1547 dictates that the slope of the ramp function must be slow enough that the inverter has time to detect the errant voltage and disconnect before the voltage changes very much. The rate of the ramp is defined by an equation given for the slope of the voltage ramp. It is shown in Equation 2.1. In some cases, the values necessary for calculating this slope namely, the detection time and delay time setting, are known and a safe value for the slope can be calculated. Other times, when these values are unknown, as in this thesis, a different method must to be used to determine the ramp rate.

At first, a trial and error approach was used to gauge what range of values would be acceptable. An initial ramp rate of 1 %/s was chosen. This rate yields an increase or decrease of 2.4 V/s or 40mV/cycle. Initial testing gave values nearly outside of the specified limits of +/-1.5% of the trip value. After performing the Time Tests, shown in Section 4.3.2, a valid ramp value was experimentally determined by using the maximum clearing time for the inverter. It was found in the time tests that the maximum trip time was 1.7s. Clearly, 1 %/s was too quick of a ramp rate. If the maximum trip time is assumed to be the worst case delay time setting plus the manufacturer's stated detection time, then a new ramp rate can be calculated according to Equation 2.1. A ramp rate of 0.22 %/s was used to yield a much slower rate of 0.53 V/s or 8.8mV/cycle. The trip values obtained from this new ramp rate were now agreeable with the manufacturer's stated values.

4.2.1.1 Matlab program for analyzing data

The tests described above can generate a high volume of data. A method for analyzing the data efficiently needed to be developed. First, the test data was captured by the scope using the DC current taken by the inverter as a trigger. Then the data was obtained from the scope using a GPIB connection. It was then saved in CSV format and imported into Matlab. A custom script was written to determine the magnitude of the simulated grid voltage the moment before the inverter trips.

First, the script identifies moments in time when the AC current out of the inverter dropped below a threshold dictated by the measurement range of the probes used. After each of these points, every future point for 3 cycles is evaluated to make sure it remains below the threshold. If no greater value is found, then the trip point has been found. The peak value of the AC voltage one half cycle before this point is then found, converted to RMS and displayed to the user in a Matlab figure. An image generated by this script for an undervoltage test is shown in Figure 4-1.

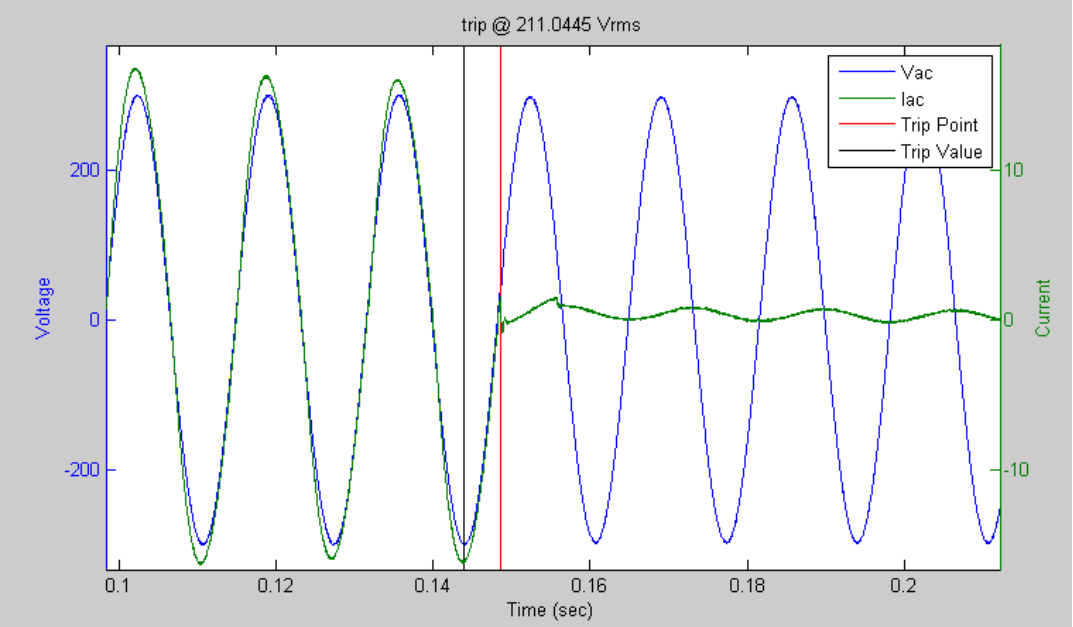

Figure 4-1 Abnormal Voltage Magnitude Test Analysis

The line labeled "Trip Point" indicates where the script found that the AC inverter current had ceased. The line labeled "Trip Value" indicates where the script found the magnitude of the voltage waveform just before the trip point.

4.2.1.2 Overvoltage Results

The test results for overvoltage magnitude test can be seen in Table 4-2 below.

Table 4-2 Overvoltage Magnitude Test Results

Test Iteration	Trip Value
1	264 V
2	263 V
3	265 V

These results can be validated by comparing them to the manufacturer's stated trip point. The default overvoltage trip point is stated as 264 V on page 68 of the Fronius Operation Manual [**43**]. The stated accuracy of +/- 1.5% yields a voltage range of [260V, 268V]. The test results agree to within +/- 0.38% of the manufacturer's stated trip point. This is well within the manufacturer's stated limits of +/- 1.5% and

thus confirms the test results as valid and shows that the inverter passes IEEE 1547 overvoltage magnitude test requirements.

4.2.1.3 Undervoltage Results

The test results for the undervoltage magnitude test can be seen in Table 4-3 below.

Table 4-3 Undervoltage Magnitude Test Results

Test Iteration	Trip Value
1	212 V
2	211 V
3	211 V

These results are compared with the manufacturer's stated trip point for validation. The default undervoltage trip point is stated as 212 V on page 68 of the Fronius Operation Manual [**43**]. The manufacturer's stated accuracy of +/- 1.5% yields a voltage range of [209V, 215V]. The test results agree to within 0.47% of the manufacturer's stated trip point, well within the +/- 1.5% range and thus confirms the test results and proves the inverter passes IEEE 1547 undervoltage magnitude test requirements.

4.2.2 Time

The time test is meant to ensure that the inverter ceases to energize the grid quickly enough after an abnormal condition has occurred. The test involves changing a parameter to a value outside of allowable range and measuring the time it takes the inverter to cease to energize the grid.

In order to determine the amount of time between the step change and when the inverter ceases to energize the grid, it was necessary to generate a waveform that indicated when the step change took place. Since the step change does not occur until a zero crossing is reached, a 1-10V signal was output from the RTDS analog out port that signified when the step change took place. This signal was used as a trigger for the scope capture. The time between the start of the abnormal condition,

denoted by this signal, and when the inverter AC current was less than a threshold is defined as the clearing time [**37**].

IEEE 1547 defines specific requirements for clearing time based on the amount of step change. The table given in Section 4.2.3 of IEEE 1547 is reproduced in Table 4-4 below.

Table 4-4 IEEE 1547 Clearing Time Requirements for Voltage Aberrations

Voltage range (% of base voltage[a])	Clearing time(s)[b]
V < 50	0.16
50 ≤ V < 88	2.00
110 < V < 120	1.00
V ≥ 120	0.16

[a]Base voltages are the nominal system voltages stated in ANSI C84.1-1995, Table 1.
[b]DR ≤ 30 kW, maximum clearing times; DR > 30kW, default clearing times.

Using these parameters as a guideline, it was possible to systematically characterize the inverter's behavior when voltage transients occurred without any prior knowledge from the manufacturer about the inverter's control algorithms. First, a generic sweep of voltage step tests was performed. It was noticed that clearing times were very different for different levels of steps. More specific tests were performed between the inconsistent values to reveal discontinuities. These sharp variations represent a protective algorithm programmed into the inverter's controller known as ride-through. The purpose of this function is to prevent the inverter from tripping off due to short-lived transients. If multiple inverters tripped when these short, unharmful variations occurred, significant generation could be lost unnecessarily. It was important to fully characterize the inverter's reaction to voltage transients because the results will later be used to develop a software model of the inverter that can be used to study larger systems.

4.2.2.1 Matlab program for analyzing data

A similar procedure to that described in Section 4.3.1.1 was necessary to analyze the testing data for the time tests. This analysis differs though because it is concerned with finding the time it takes

the inverter to trip, rather than the magnitude at which it trips. A custom script was developed to find the trip point and determine the elapsed time from the step change. Finding the trip point was done in a similar way as was done in Section 4.3.1.1.

The script also calculates the percent step change by finding the peak voltage before and after the step and displaying the ratio of the two to the user. Calculating the voltage level after the step change required some extra insight. When certain levels of step changes were performed, voltage transients occurred immediately after. In order to get an accurate value for the percent step change, the voltage calculation had to take place after the transient section. An image, shown in Figure 4-2, is generated by the script to help the user determine if the correct values were calculated.

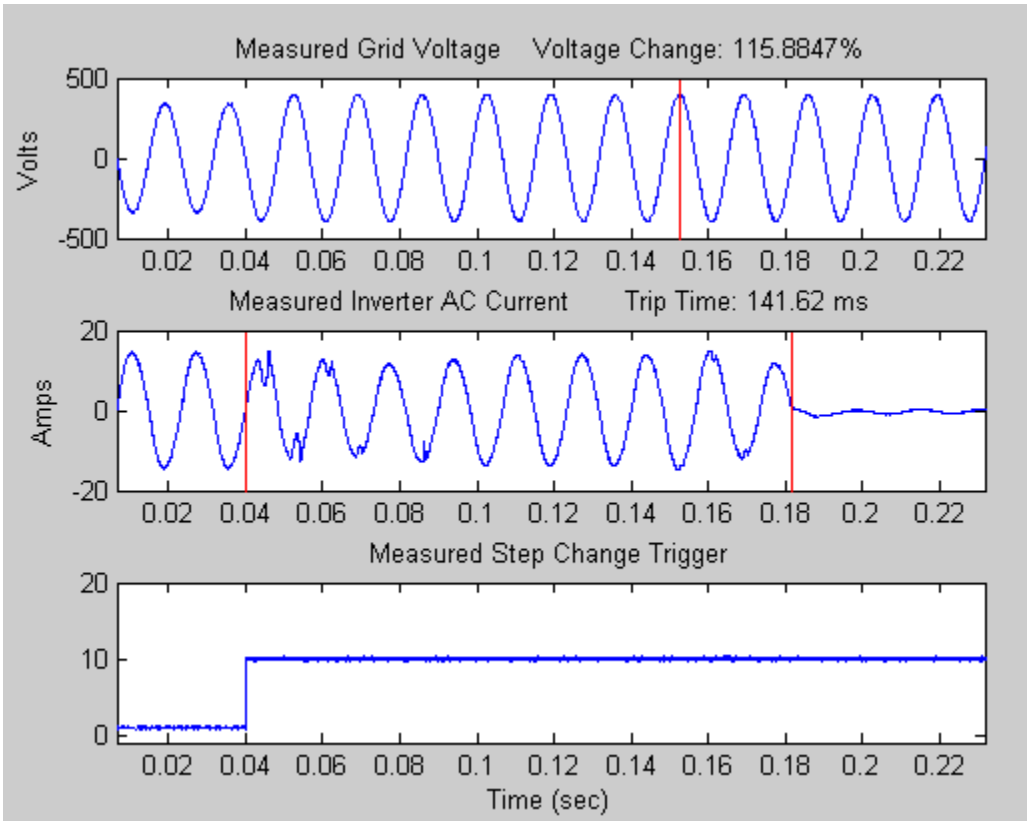

Figure 4-2 Measured Overvoltage Step Change

4.2.2.2 Overvoltage Results

Numerous overvoltage tests were performed to fully characterize the inverter's reaction to overvoltage transients. The results are shown in Table 4-5.

Table 4-5 Overvoltage Time Test Results

Test Iteration	Clearing Time	Amount of Step	Step (measured)	Amount of Step	Step (programmed)
	ms	% of base	V	% of base	V
1	682.98	109.82%	263.6	110.00%	264.0
2	682.96	112.82%	270.8	112.00%	268.8
3	682.98	114.27%	274.2	114.50%	274.8
4	682.94	115.17%	276.4	115.20%	276.5
5	682.99	115.76%	277.8	115.00%	276.0
6	141.62	115.88%	278.1	116.00%	278.4
7	141.60	116.20%	278.9	117.00%	280.8
8	141.60	116.29%	279.1	115.50%	277.2
9	105.88	119.44%	286.7	120.00%	288.0
10	114.76	120.24%	288.6	120.00%	288.0
11	115.06	120.36%	288.9	120.00%	288.0
12	114.94	120.36%	288.9	120.00%	288.0
13	99.65	124.39%	298.5	125.00%	300.0

This data is also displayed graphically, with the IEEE limits superimposed, below.

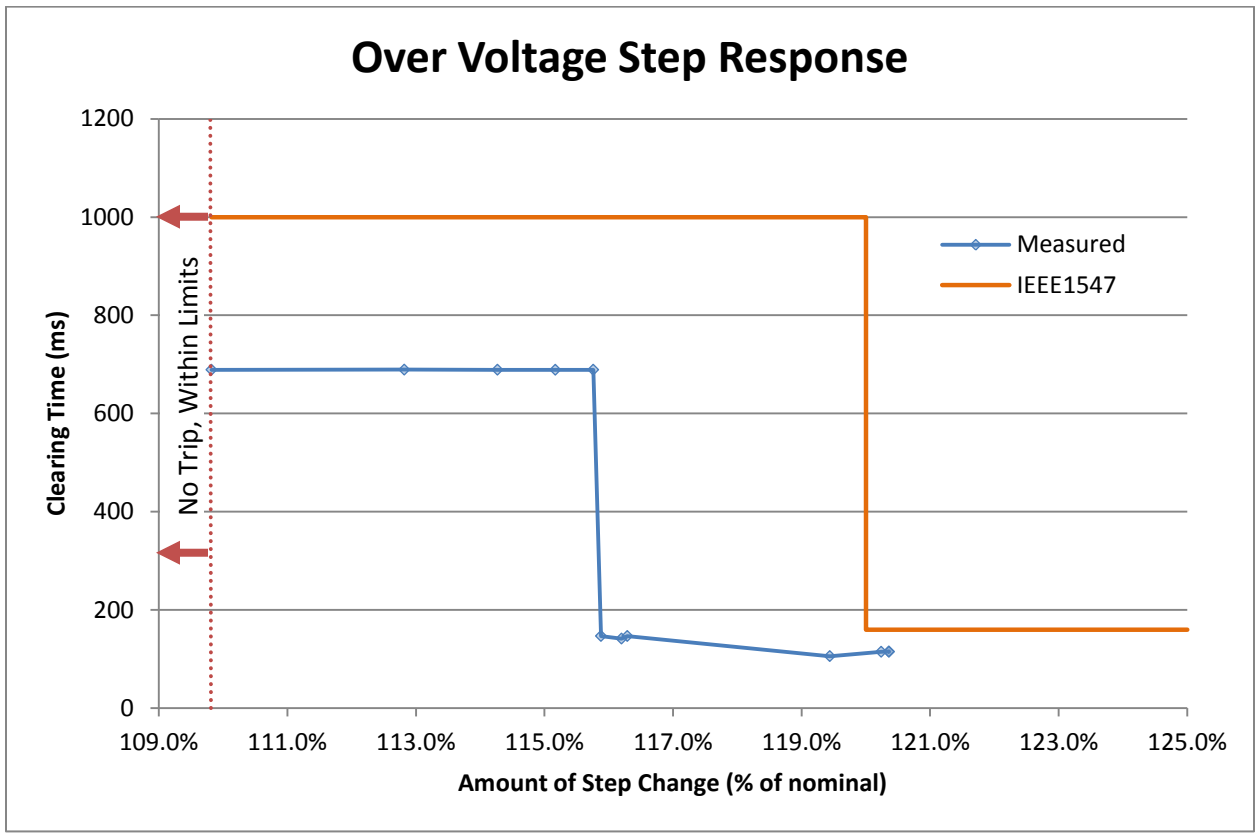

Figure 4-3 Overvoltage Time Test Results Graph

The orange line represents the IEEE requirements detailed in Table 4-5. The blue diamonds represent measured step values. The maximum error between the user set point and the measured value occurred at the 114.5% step value. The resulting measured value was 115.34%, which gives an error of 0.7% between programmed value and measured value.

The Fronius IG 3000 has certifiably passed all IEEE 1547 requirements. Therefore, compliance with IEEE 1547 requirements was used for validation of test results since little was known about the inverter's step response algorithm and information from the manufacturer was unobtainable. Interestingly, the effects of the ride-through algorithm can be seen at 115.8% of base voltage, or 278V. Given a smaller deviation from nominal operating conditions, the inverter will wait longer to trip than if

a larger deviation occurred, thus preventing unnecessary loss of the DR generation for short-lived overvoltage conditions.

4.2.2.3 Undervoltage Results

The undervoltage results showed more variability than the overvoltage results. This is likely due to the control algorithm inside the inverter allowing for more varied response options when undervoltage transients occur. The test results can be seen in Table 4-6 below.

Table 4-6 Undervoltage Time Test Results

Test Iteration	Clearing Time	Amount of Step	Step (measured)	Amount of Step	Step (programmed)
	ms	% of base	V	% of base	V
1	138.5	52.25%	125.4	52.00%	124.8
2	71.1	54.39%	130.5	54.00%	129.6
3	54.3	52.25%	125.4	52.00%	124.8
4	36.6	44.66%	107.2	45.00%	108.0
5	80.2	49.95%	119.9	50.00%	120.0
6	61.9	59.66%	143.2	60.00%	144.0
7	81.3	76.60%	183.8	76.00%	182.4
8	80.2	76.87%	184.5	77.00%	184.8
9	223.6	77.59%	186.2	77.00%	184.8
10	227.6	80.00%	192.0	79.00%	189.6
11	215.3	80.02%	192.0	80.00%	192.0
12	273.4	80.68%	193.6	80.00%	192.0
13	1689.4	81.39%	195.3	81.00%	194.4
14	1688.2	81.86%	196.5	81.50%	195.6
15	1689.2	82.39%	197.7	82.00%	196.8
16	1689.3	83.24%	199.8	83.00%	199.2
17	1689.2	85.36%	204.9	85.00%	204.0
18	1689.3	87.20%	209.3	87.50%	210.0

A graphical representation of these results is shown below with the IEEE 1547 requirements superimposed.

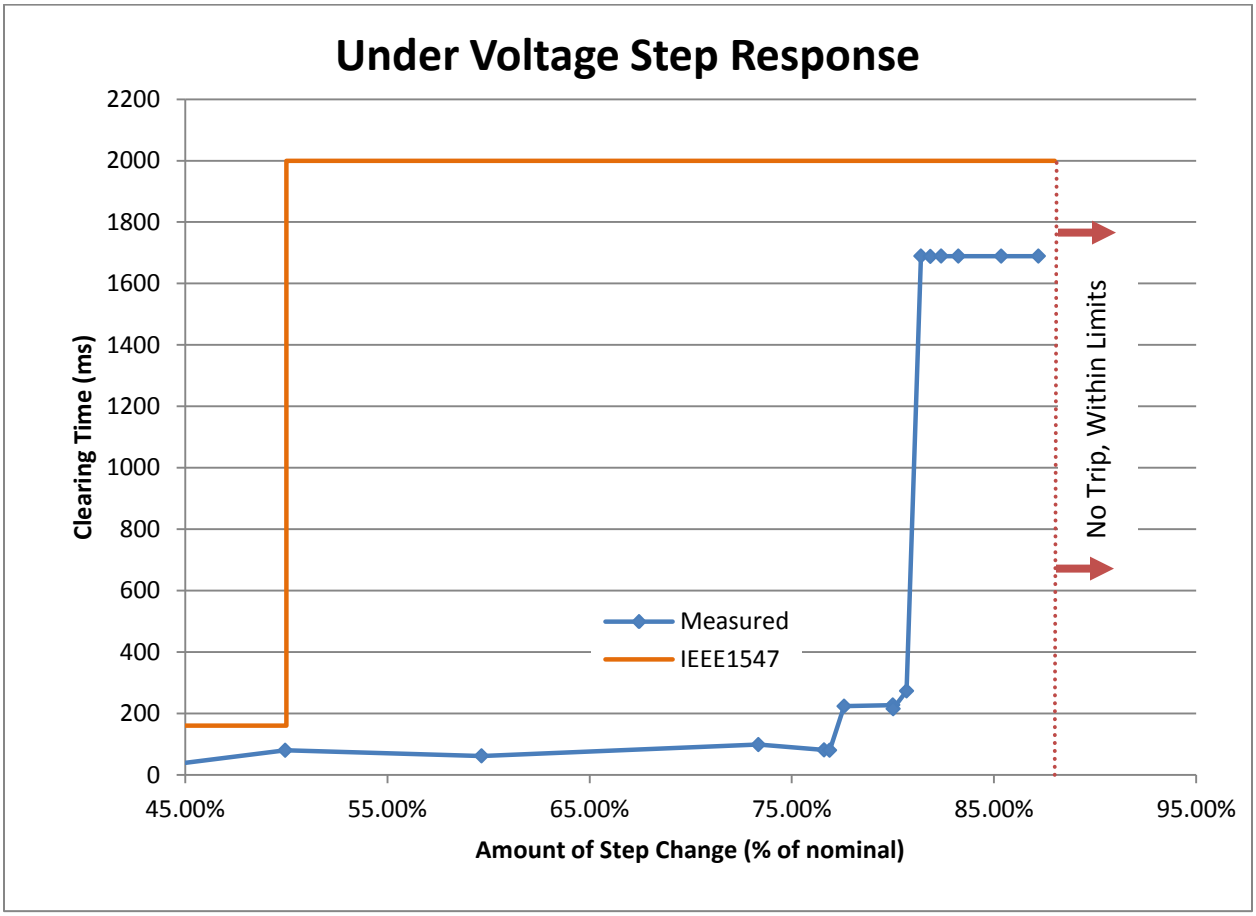

Figure 4-4 Undervoltage Time Test Results Graph

The format is the same as the overvoltage graph with the orange representing IEEE 1547 requirements and the blue representing measured values. The maximum amount of error between programmed values and measured values occurs at the 79% step point. A step of 80% was measured which gives an error of 1.27%.

Again, since little information was available about the step response algorithm of the inverter's controller, compliance with IEEE 1547 requirements was used for validation of test results.

The effects of the ride-through algorithm can be seen at 81% of base voltage, or 194V, and above.

4.3 Abnormal Frequency

Load and generation changes are common on an EPS. These changes are two common causes of changing frequency on the grid. Controllers are constantly working to balance the amount of power demanded and the amount of power supplied. While the grid frequency is never truly constant, changes of more than half of a Hertz from the nominal value could indicate a problem. Large swells in frequency could be indicative of a big load decrease or perhaps a short circuit. Large sags could be indicative a major generation source dropping offline. DRs need to be able to detect the grid frequency and determine, based on the amount of deviation from the nominal value of 60 Hz, whether a problem exists and if they should disconnect from the grid.

Two types of tests were performed to characterize the inverter's response to abnormal frequency conditions. The magnitude test determines at what level the inverter trips and the time test determines how long, from an instantaneous change in conditions, it takes the inverter to trip.

4.3.1 Magnitude

Each grid-tied inverter manufacturer specifies an operating range for frequency. If the AC waveform goes outside of this range, the inverter should cease to output AC current. The magnitude test involves slowly ramping the frequency up or down and determining at what level the inverter trips. A more detailed description of the testing procedure can be found in Section 3.1.2.7.

4.3.1.1 Matlab program for analyzing data

As in the voltage tests, the data was captured with a PZ4000, using the DC current taken by the inverter as a trigger, and saved to a CSV file. The data was then imported and analyzed in Matlab. Determining the frequency at the trip point required writing another custom script that found the trip point by monitoring the level of the AC current output by the inverter. Then the program calculates the frequency of the AC voltage waveform directly before the trip point using zero crossings.

The ramp rate issue, discussed in Section 4.2.1, was not a large concern for frequency tests. It was later found that abnormal frequency conditions cause the inverter to trip at a maximum time of 33.9 ms or about two cycles. The ramp rate used for the frequency magnitude tests was 0.0149 Hz/s. This ramp rate yields a maximum deviation of 0.0005 Hz before the inverter trips. If Equation 2.1 is to be used and 33.9 ms is assumed as a worst case scenario for the value of z, a ramp rate of 0.1475 Hz/s or below is sufficient.

To aid the user in obtaining the most accurate results, the script generates an image of what values were used to calculate the results. Two red vertical lines are superimposed on the voltage and current waveforms. These lines show which points the program found zero crossings at and thus used for calculating the frequency. Another red horizontal line is superimposed to show where zero voltage is. The user may adjust the zero crossing values after they have been found to obtain the most accurate frequency measurement. An actual screen shot from an overfrequency test is shown in Figure 4-5.

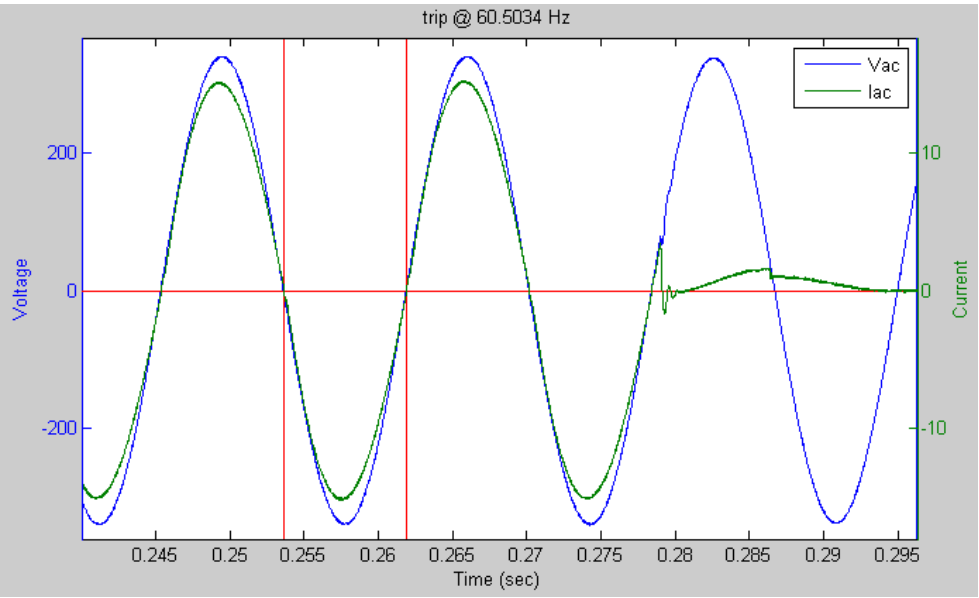

Figure 4-5 Abnormal Frequency Magnitude Analysis

4.3.1.2 Overfrequency Results

The results from the overfrequency magnitude test are shown in Table 4-7.

Table 4-7 Overfrequency Magnitude Test Results

Test Iteration	Frequency trip point (Hz)
1	60.49
2	60.51
3	60.50

These results were compared with the manufacturer's stated trip point of 60.5 Hz to determine whether they are valid. The manufacturer's stated accuracy for frequency trip limits is +/- 0.02 Hz, which gives a range of [60.48 Hz, 60.52 Hz].

Since frequency limits are very tight, the measurement accuracy of the PZ4000 can be a factor when determining the trip value. If the zero crossing used to determine the frequency occurred, in the worst case, one whole sample away then the error of the measurement can be calculated as

$$error = \frac{1}{\frac{1}{frequency} \pm \frac{1}{sampling\ rate}} - frequency$$

Equation 4-1

If a frequency of 60.5 Hz is expected and a sampling rate of 250kS/s is used, then the error can be calculated to be +/- 0.015 Hz. If a greater amount of accuracy is required, a faster sampling rate must be used.

4.3.1.3 Underfrequency Results

The results from underfrequency testing are shown in Table 4-8.

Table 4-8 Underfrequency Magnitude Test Results

Test Iteration	Frequency trip point (Hz)
1	59.33
2	59.33
3	59.33

These results were compared to the manufacturer's stated trip values to validate the findings. The stated range of accuracy for the trip limit is [59.28 Hz, 59.32 Hz] [**43**]. The accuracy of the PZ4000, calculated from Equation 4-1 using a frequency of 59.3 Hz and a sampling rate of 250kS/s, is +/-0.014 Hz. With this error accounted for each measured trip point is within the manufacturer's stated accuracy range.

4.3.2 Time

The purpose of this test is to measure the amount of time it takes an inverter to trip after an instantaneous frequency deviation has occurred. This time is defined as the duration between the time when the frequency changes and when the inverter AC current goes to zero. The limits are defined in Section 4.2.4 of IEEE 1547. The limits for DR less than 30kW are reproduced in Table 4-9 below.

Table 4-9 IEEE 1547 Clearing Times for Frequency Aberrations

Frequency Range (Hz)	Maximum Clearing Times (ms)
> 60.5	160
< 59.3	160

4.3.2.1 Matlab program for analyzing data

As in all other tests, data was captured with a PZ4000 scope, using the step signal as a trigger, and saved in a CSV file format. It was then imported into Matlab and analyzed with a custom script that was developed specifically for this purpose. The script works in a similar way to the voltage time test script, detailed in Section 4.3.1.1 in that it finds the time when a step change in the variable being tested occurs and the time when the inverter AC current goes below a threshold and subtracts the two to give the clearing time. An image, similar to Figure 4-2 is displayed to the user in order to confirm the right values were determined.

4.3.2.2 Overfrequency

Testing results for overfrequency were very consistent and only a few tests were necessary to characterize the inverter's overfrequency response. The results from these tests are shown in Table 4-10 below.

Table 4-10 Overfrequency Time Test Results

Test Iteration	Clearing Time	Amount of Step	Step (measured)	Amount of Step	Step (programmed)
	ms	% of base	Hz	% of base	Hz
1	33.8	100.89	60.53	100.83	60.5
2	33.8	100.94%	60.56	101.17%	60.7
3	33.8	101.02%	60.61	101.00%	60.6
4	33.7	101.35%	60.81	101.50%	60.9
5	33.8	102.02%	61.16	102.00%	61.2
6	33.8	102.43%	61.47	102.50%	61.5
7	33.8	102.83%	61.65	102.75%	61.65

These results are displayed graphically in Figure 4-6 with IEEE 1547 requirements superimposed.

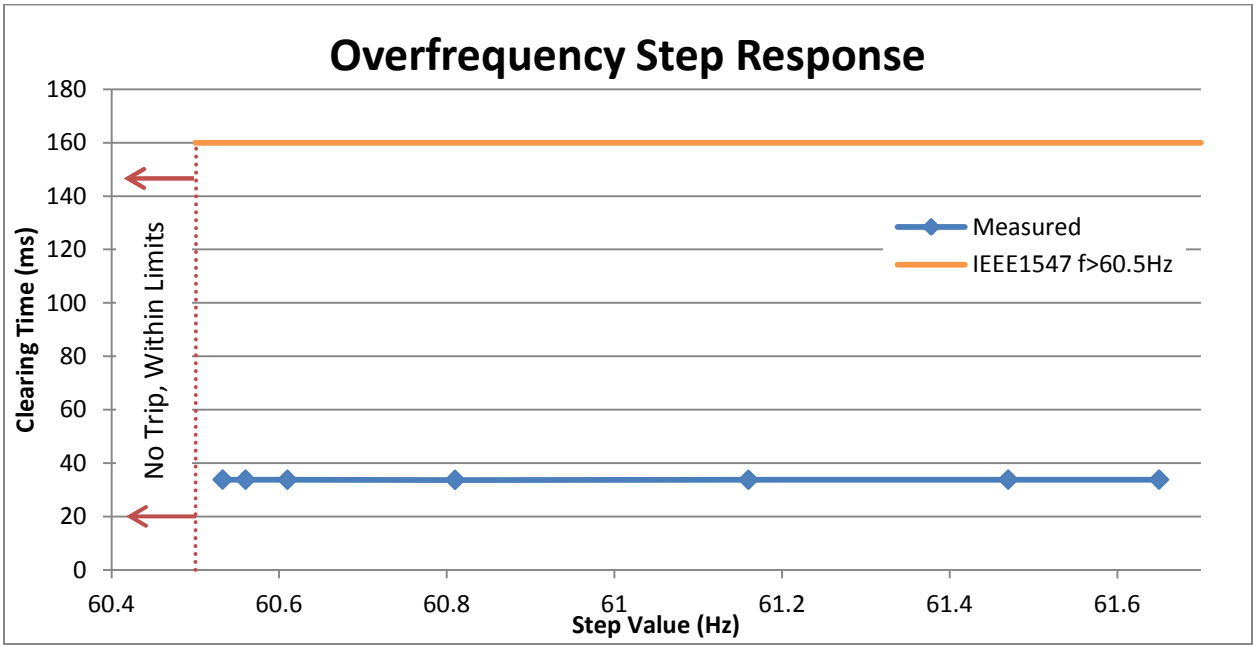

Figure 4-6 Overfrequency Time Test Results Graph

The orange line shows the maximum allowable clearing time dictated by IEEE 1547. It is clear that the inverter satisfies this requirement for practical frequency values. In theory, it would take the inverter a minimum of half a cycle to determine the frequency of the grid waveform, which for all practical purposes is about 8 ms. The rest of the clearing time is likely due to the speed of the controller and disconnection device. The blue line shows measured values. The maximum error observed between a user programmed value and a measured value was 0.23% for the 60.7 Hz set point.

4.3.2.3 Underfrequency

The results from the underfrequency time tests are also very consistent. The test results are shown in Table 4-11 below.

Table 4-11 Underfrequency Time Test Results

Test Iteration	Clearing Time	Amount of Step	Step (measured)	Amount of Step	Step (programmed)
	ms	% of base	Hz	% of base	Hz
1	33.9	95.39%	57.17	95.50%	57.3
2	33.8	96.45%	58.06	97.00%	58.2
3	33.8	97.03%	58.22	97.50%	58.5
4	33.8	98.09%	58.69	98.00%	58.8
5	33.8	98.55%	59.13	98.33%	59
6	33.8	98.85%	58.99	98.50%	59.1

These results are displayed graphically in Figure 4-7.

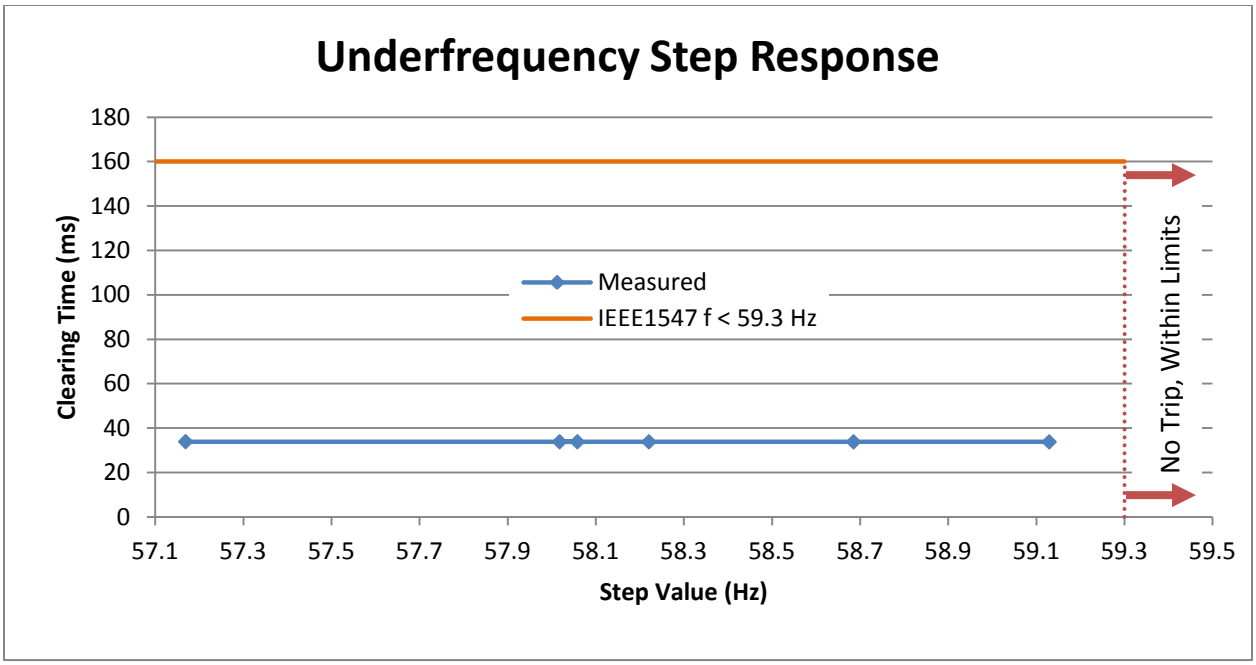

Figure 4-7 Underfrequency Time Test Results Graph

As in the other graphs, the orange line represents the limit imposed by IEEE 1547 for DR less than 30kW. Once again, the measured clearing times are well below the limit imposed by IEEE 1547. The blue diamonds are measured values. Underfrequency testing gave a maximum error of 0.48%, at 58.5 Hz, between measured and user programmed values.

4.4 Anti-Islanding

Islanding refers to a scenario when a specific region of an area EPS is disconnected from the rest of the area EPS and energized only by a local EPS [**7**]. The local EPS that is energizing the disconnected section can be made up of various DRs. Islands can be strategically created for situations such as critical loads. Unintentional islanding can be a serious problem though. Therefore, grid-tied DRs must include anti-islanding protection if no island should be formed. Section 4.4.1 of IEEE 1547 states that the DR must disconnect within 2 seconds of the formation of an island.

The test defined in IEEE 1547.1 Section 5.7 requires a resonant circuit to be configured for the load. Two methods for configuring the appropriate load are described in Section 3.2.1.3.2. The values

used for this resonant circuit were determined using the first method. First, the capacitive load was set equal to the resistive load. This yielded a power factor of 0.71 signifying that the resistive and capacitive loads are nearly matched. Then, the inductive load was modified until a power factor close to 1 was reached. The best values, determined experimentally and shown in Table 4-12, resulted in a power factor of 0.96 for Phase A and 0.98 for Phase B with a quality factor of 0.97.

Table 4-12 Resonant Circuit Settings for Anti-Islanding

Type of Power	Power Setting
Resistive	2.5 kW
Reactive, Capacitive	2.5 kVAR
Reactive, Inductive	2.34375 kVAR

Mathematically, these values do not equate to a power factor or quality factor of 1. Component tolerances and step values restrict the possible load combinations.

The results for the Fronius PV inverter's anti-islanding protection can be seen in Table 4-13.

Table 4-13 Anti-Islanding Test Results

Test Iteration	Clearing Time (ms)
1	58.16
2	58.06
3	58.04

It is clear that the measured clearing times are well below the limit of 2 seconds and thus compliant with IEEE 1547.

4.5 Summary of Test Results

These tests showed that a grid-tied inverter's controller can be characterized without prior knowledge of control algorithms or controller operation. As a means for validation, the results were compared with limits imposed by IEEE 1547, a standard this inverter certifiably adheres to. Also the trip values were compared with the manufacturer's stated values. Good agreement was seen between

results, limits, and stated values. The results from these tests can now be used to construct a model of a PV inverter with the same grid integration characteristics.

Beyond the characterization for the purposes of modeling, it is interesting to analyze what the purpose of a certain control algorithm might be. A clear difference can be seen in the voltage response times and the frequency response times. This may be because fault conditions will likely cause the voltage to deviate from the nominal value, while the frequency could remain relatively unchanged. Protective relays and reclosing devices used in power distribution systems are used to sense these faults and to clear the problem in less than a second. If the protective devices serve their purpose and the fault is cleared, there is no need for the inverter to trip. The voltage ride-through characteristics seen in the voltage time test results provide a method for the inverter to handle these short abnormalities without losing generation capacity.

On the other hand, a deviation in frequency on the order of 0.5 Hz can indicate a serious problem and immediate disconnection is necessary. The frequency clearing times observed are on the order of two cycles consistently, indicating a very fast disconnection.

5 Modeling the System

The goal of this thesis is to model an inverter's behavior for abnormal grid conditions. An inverter was chosen because many DR connect to the grid via an inverter. Electric power from the DR must pass through the inverter before it is put onto the grid. Since inverters represent a grid-interface for DR protection algorithms must be installed on grid-tied inverters that regulate power flow between the DR and the EPS.

Modeling inverters can be accomplished many different ways [**12**], [**45**], [**46**]. Most models involve IGBTs or FETs and focus on switching-level transients in the kHz range. Since the focus of this thesis is protection characteristics, a much lower range of frequencies was examined. The model developed performs the same as a real-world inverter at typical EPS frequencies.

This chapter will show how characterization data, taken from PHIL testing, can be used to construct a model of a grid-tied inverter. The model will then be tested in a software environment and the results will be compared with those obtained from real-world testing of an inverter.

5.1.1 PHIL for Modeling

PHIL offers a unique method for developing models of grid-tied inverters. It serves as a means for characterizing the real inverter and then also providing a platform for developing a model of the inverter based on the characterization all in one system. Programming for characterization tests and modeling is done in the same environment (Simulink).

PHIL also facilitates extending the testing environment. It can be very difficult to test multiple inverters at once in a real-world environment. If models can be constructed, then the user has the choice whether to use the model or real-world inverter when testing various EPS conditions. Analog and digital inputs and outputs to the RTDS allow for integration of real-world components with software

models. This is an extremely powerful testing method as it allows for replacing virtually any hardware with a software model while keeping the systems response the same.

5.1.2 Modeling Constraints

The modeling performed in this project is based on the grid-interconnection characterization of a PV inverter, as discussed in Chapter 4. The goal is to model an EPS with a PV inverter in software and have the model of the PV inverter perform the same way as an actual PV inverter would under abnormal grid conditions. Maximum power point tracking, harmonics and other sub-cycle transients are not the focus of this project, though they could be implemented in the future.

5.2 Approach

In order to accurately model the characterization system, a Simulink model had to be developed and tested to ensure that it agrees with the system used for characterization. Once the components were chosen to model the grid and inverter, they were tested and their results were compared to actual data.

5.2.1 Modeling Software

Simulink, version 7.3 (R2009a) was used to model the EPS. The SimPowerSystems library was used to model the inverter, grid simulator and load. The ode4 explicit fixed-step continuous solver was used in the modeling program. This solver uses the fourth-order Runge-Kutta formula to integrate the continuous states. A smaller simulation step size was used in the modeling program than was used in the characterization program described in Chapter 4. Limits that apply to real time systems like the characterization program do not necessarily apply to the system model. A smaller step size can be used to obtain greater accuracy. A 10 µs step size was used to give an accuracy of +/- 0.036 Hz at 60 Hz.

5.2.2 Modeling the Grid Simulator

The grid simulator was modeled in software by the Controlled Voltage Source block in SimPowerSystems. This block generates has a signal input port, a positive voltage terminal and a negative voltage terminal. It generates a voltage on the voltage terminals that mimics what is seen on the input signal port.

The output of the IEEE1547 test generator subsystem that was used in the HIL program for characterization to control the real grid simulator was fed to the signal input port of the Controlled Voltage Source block. The block was now capable of generating any of the test waveforms that were used in the characterization system.

5.2.3 Modeling the Inverter

Once the inverter's grid-interconnection behavior has been characterized, a software model can be developed. The Controlled Current Source block from SimPowerSystems was used to model the inverter. This block is similar to the Controlled Voltage Source block used for the grid simulator in that it has one input signal port, one positive terminal and one negative terminal. It converts the input signal into a current and outputs on the positive and negative terminals. This block was chosen because grid-tied inverters can provide no voltage regulation and therefore act like a current source.

5.2.3.1 Control of the Inverter Block

In a real inverter, measurement devices are used to monitor AC and DC power flow as well as frequency. The measurements are read by a controller that controls the output of the inverter. To get the modeled inverter to act like an actual PV inverter, a subsystem was created to simulate the inverter controller. This simulated inverter controller subsystem was then used to control the Controlled Current Source block that simulates the inverter.

A voltage measurement block and a constant block were the two inputs to the subsystem. The voltage measurement block measured the grid voltage and the constant block represented the amount of DC power being fed to the inverter. Using these two inputs and Equation 5-1, the subsystem generated a control signal that was fed to the input signal terminal of the Controlled Current Source block

$$I_{ac} = \frac{(P_{dc} * \eta_{inverter})}{V_{grid,RMS}} * \frac{V_{grid}}{V_{grid,RMS}}$$

Equation 5-1

where,

$\eta_{inverter}$	is the inverter efficiency
P_{dc}	is the DC input power to the inverter
$V_{grid,RMS}$	is the RMS value of the grid voltage
V_{grid}	is the sinusoidal grid voltage.

Equation 5-1 for I_{ac} applies only for loads with a power factor of 1. If loads of a different power factor were used, phasor math would be necessary.

5.2.3.1.1 Voltage

Inside the subsystem, the RMS voltage is calculated using the RMS block from the SimPowerSystems library. The output of the RMS block is used to determine the EPS voltage level. As long as the grid voltage is within an acceptable range, the subsystem will continue to generate a signal for the current source block using Equation 5-1.

A separate subsystem is used to determine when to trip if abnormal voltage conditions exist. This subsystem uses the RMS measurement as an input and outputs either a 1 or a 0, signifying a trip condition or a normal operating condition. The output is determined by a relational operator that compares the current simulation time to a time generated by the subsystem. This generated time comes from a user-defined look-up table that determines clearing times.

For example, if the measured RMS voltage goes outside of the specified range, a signal is sent to two switches signifying that a voltage aberration has occurred. The first switch controls the input to a look-up table that determines how long the subsystem should wait until sending the trip signal. The wait time represents the detection time, adjustable time delay, interposing device delay and interrupting device delay. These delays are collectively known as the clearing time. The values in the look-up table come from the inverter characterization procedure. The input to the look-up table is the ratio of the current grid RMS voltage to the base RMS voltage and the output is a clearing time. A slight modification, described in Section 5.5.2, must be made to this time to obtain accurate results.

The second switch controls what value is being compared to the current time. When the trip signal is sent, it is delayed by the same amount as the signal that controls the input to the look-up table. After this period, the switch changes from a dummy time that is always ahead of the current time, to a time that is ahead of the current time by an amount specified from the look-up table. Once the current time passes the time output by the look-up table, a trip signal is generated and sent up a level to the subsystem that controls the current source block.

5.2.3.1.2 Frequency

The grid frequency is calculated using the block described in Section 3.1.2.3.6. Since the controls system of the Fronius inverter dictates a constant trip time regardless of the amount frequency deviation, only the event of a frequency deviation need be detected. A simple delay block between the

detection and the trip signal can be used instead of a look-up table. Correct trip times require a modification described in Section 5.5.1.

5.2.3.1.3 Tripping

If either a frequency or voltage trip signal is generated, the subsystem will switch its output from the I_{ac} described above to a waveform that is similar, but greatly reduced in magnitude. The point of this is to mimic what is seen from the actual inverter. This small ripple is likely due to some reactive element inside the inverter. A contactor is opened when the inverter trips. While it cannot be known for certain without a schematic of the inverter's hardware, it is likely that some kind of filter containing reactive elements lies between the output breaker and the output contactor.

5.3 Results

Specific characterization tests were used to verify that the model performed in a similar manner to the actual inverter. The frequency step or voltage step measured from the characterization tests was programmed into the model. The results can be seen below. The model results are on the right and the characterization results are on the left.

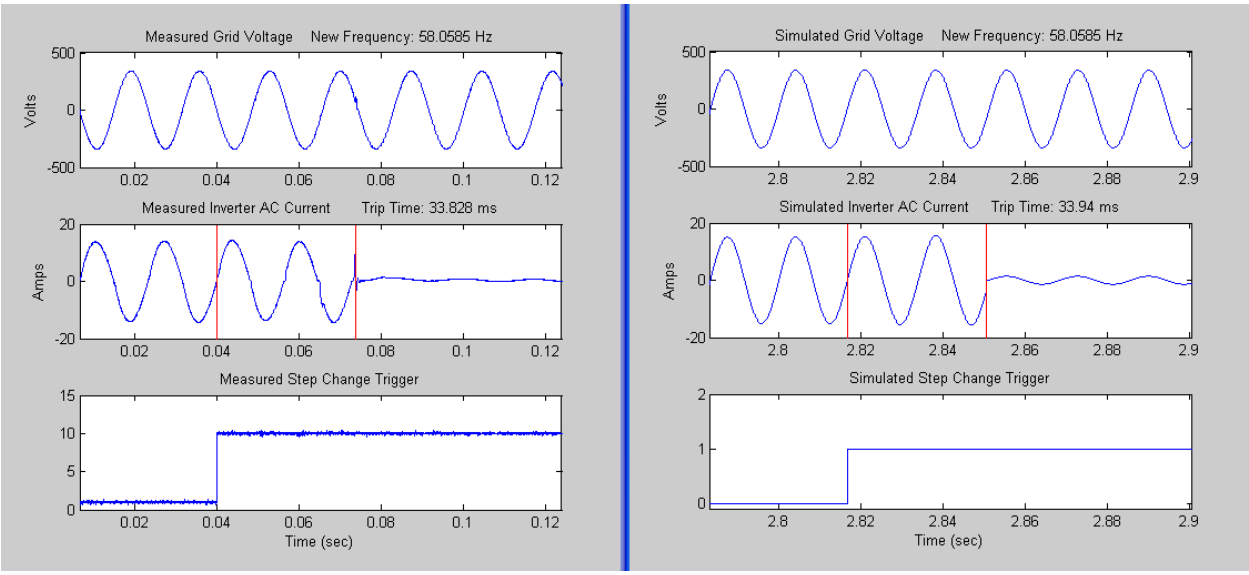

Figure 5-1 Underfrequency Test Measured and Simulated Comparison

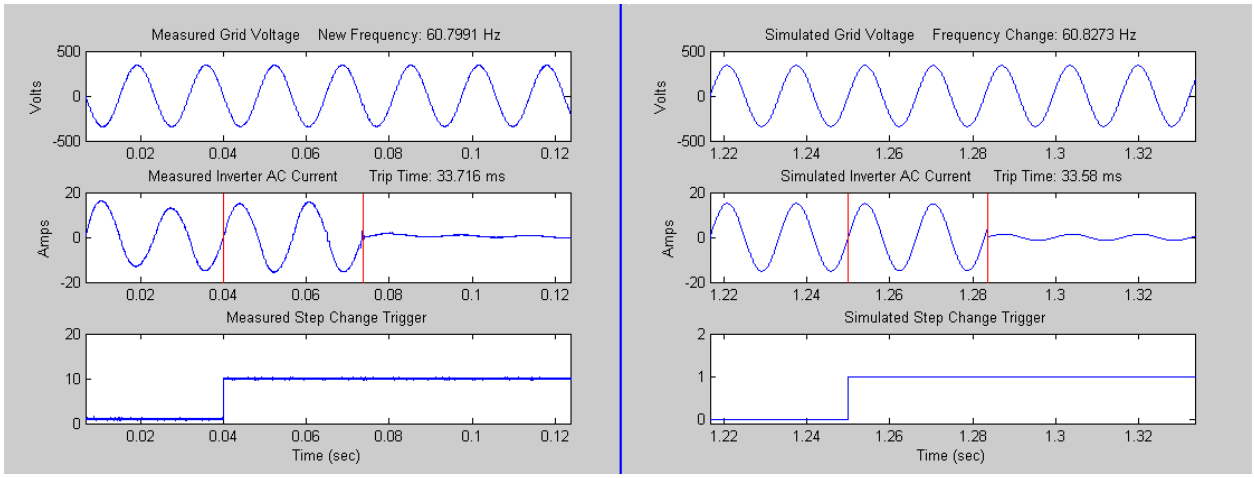

Figure 5-2 Overfrequency Test Measured and Simulated Comparison

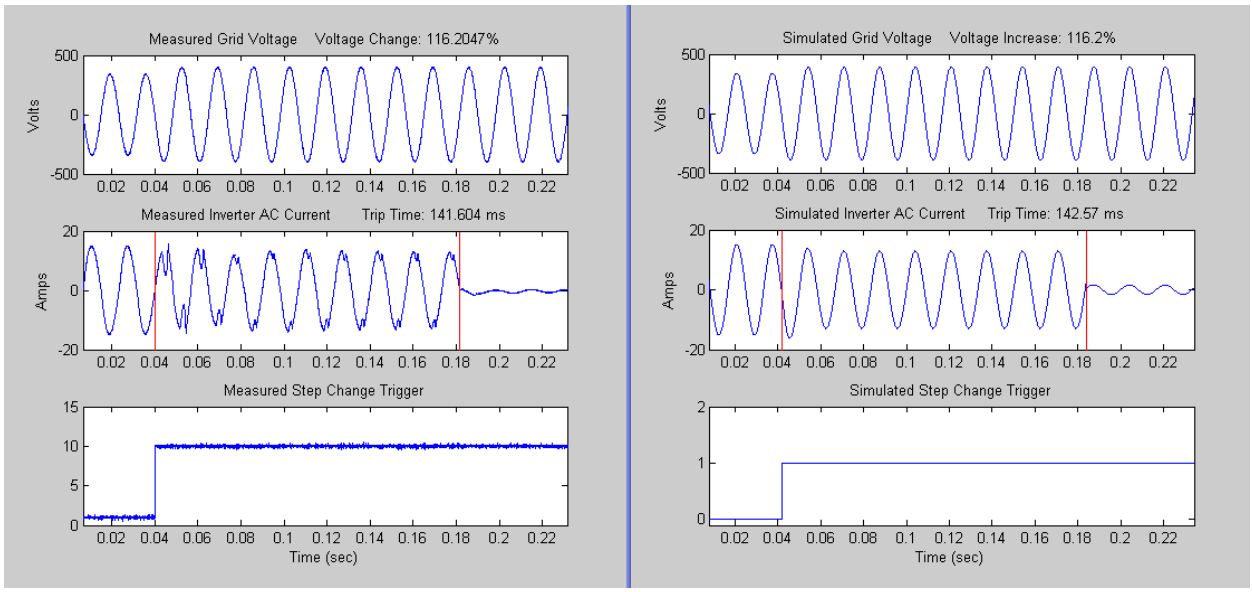

Figure 5-3 Overvoltage Test Measured and Simulated Comparison

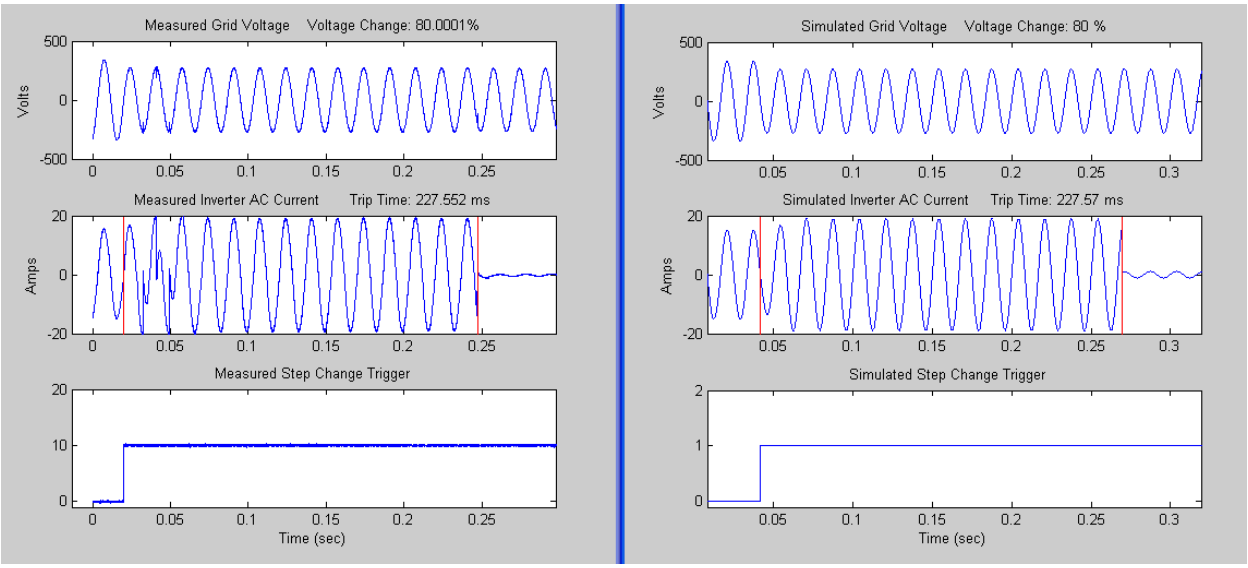

Figure 5-4 Undervoltage Test Measured and Simulated Comparison

5.4 Discussion of Results

It can be seen from Figure 5-1 through Figure 5-4 that the developed model performs nearly identically to the physical hardware. It trips at similar levels and has similar clearing times to the actual inverter for similar conditions. The model's responses to abnormal frequency conditions are within a few tenths of a millisecond. This degree of accuracy is possible because the response is constant no matter how far outside of the limits the frequency varies. The accuracy of responses to abnormal voltage conditions depends on a look-up table that interpolates between given data points. If a more accurate response was desired, more data points would need to be added to the table to reduce the amount of interpolation.

Transients in the inverter current have not been modeled as they can be somewhat unpredictable and are outside the scope of this thesis.

5.5 Modifications to the Model

Model performance initially was precise, but not accurate. Modifications had to be made to the inverter controller to account for delays introduced by certain Simulink blocks. After these changes were made, the models performance greatly improved.

5.5.1 Frequency

Firstly, the frequency measurement and step change have to occur at the same time. If the frequency measurement tool uses a zero crossing before the step change and after the step change, then an intermediate frequency is calculated and an errant value is output causing the inverter to trip at the wrong time. The scenario can be seen in Figure 5-5 below.

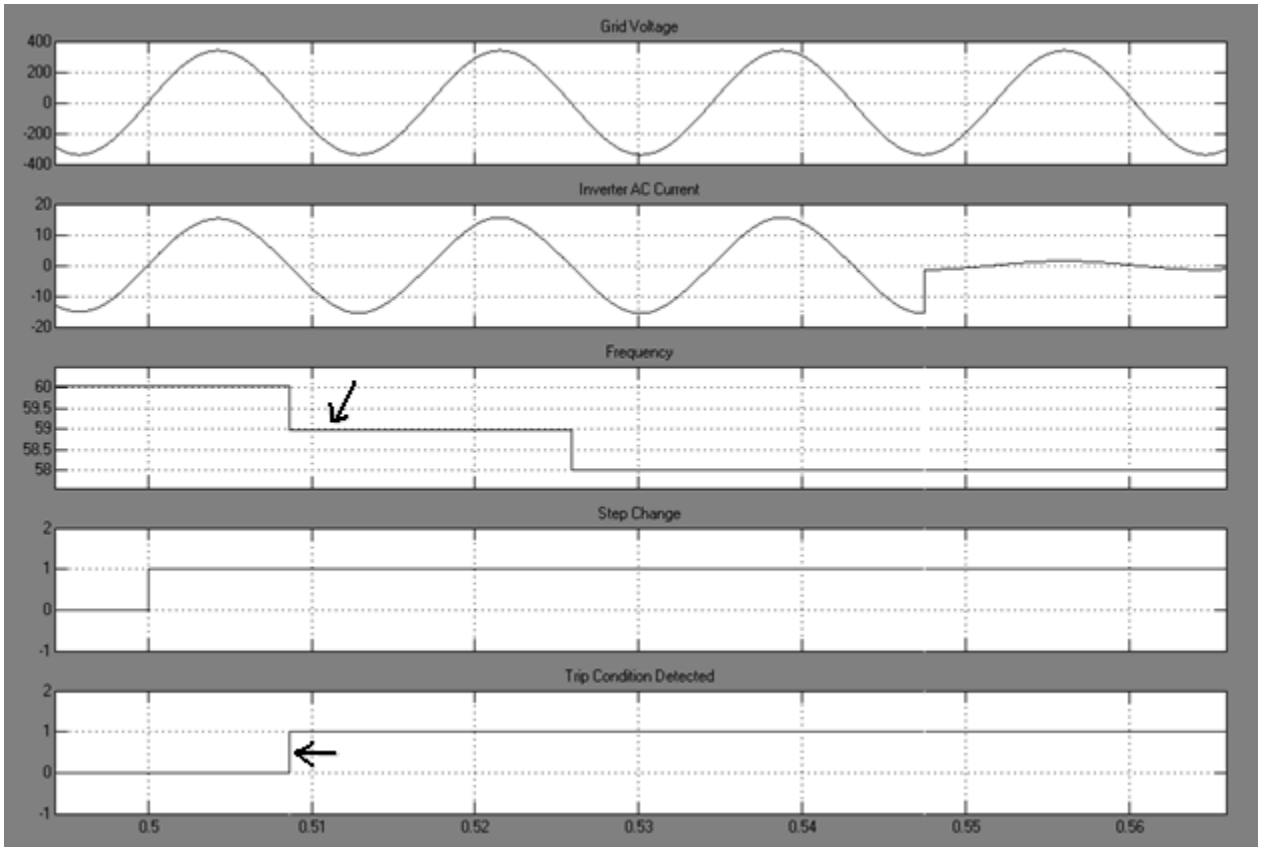

Figure 5-5 Waveforms Showing Errant Frequency Measurement Before and After Step

Since the user defines when the step change will occur, it may not occur the same way every time. The frequency measurement could be split between two different waveforms, or it could measure

just one. To account for this variability, the frequency measurements must occur on the same edge of the waveform as the step change does. When this was implemented, both of the zero crossings used to calculate the frequency belonged to the new waveform. The corrected results of the above image can be seen in Figure 5-6 below.

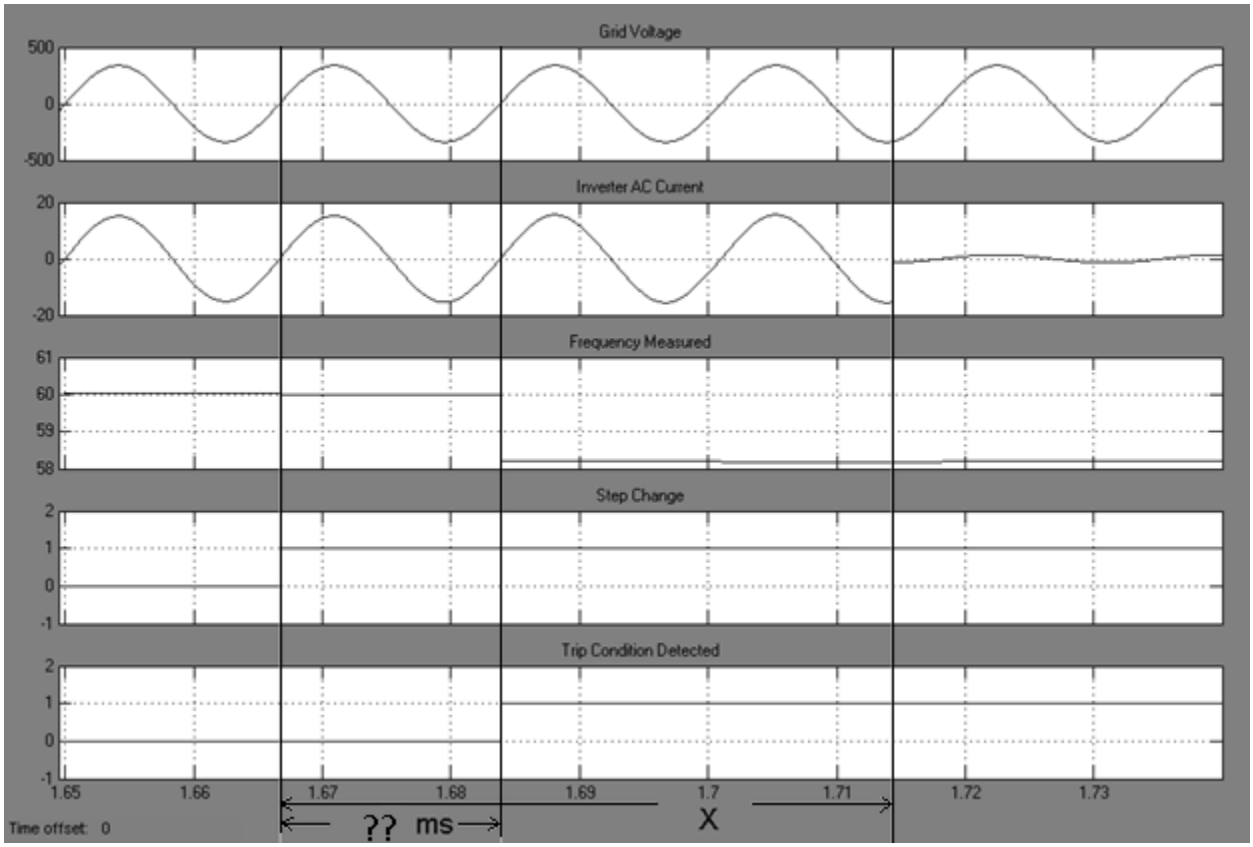

Figure 5-6 Waveforms Showing Correct Frequency Measurement

This methodology introduces a delay of one cycle into the frequency measurement. This delay must be taken into account when determining the clearing time, X. Since the new frequency is unknown to the program, the delay is also unknown. The delay can be calculated from the measured frequency, but a difficulty is introduced when using Simulink's delay block. The block cannot be edited on-the-fly during run-time execution. Currently 16.67 ms is used as the delay time until a better method can be implemented. The amount of error introduced to the clearing time is calculated as

$$clearing\ time\ error = \frac{1}{f_{old}} - \frac{1}{f_{new}}$$

Equation 5-2

where

f_{old} is the frequency before step,

f_{new} is the frequency after step.

Assuming the frequency range is 60 +/- 2 Hz, the maximum amount of error introduced is +/- 0.575 ms. This does not alter the inverter's ability to conform to IEEE 1547 limitations.

5.5.2 Voltage

Using only the clearing time look-up table to determine when to trip will yield inaccurate results. Calculating the RMS voltage takes a certain amount of time that must be subtracted out of the output of the clearing time look-up table before it is used to determine when to trip. Since all step changes are instantaneous, the time that it takes for the RMS voltage to rise above the threshold varies depending on how large of a step is executed. In order to determine the error introduced, practical voltage steps were performed and the response from the RMS block was measured. Another look-up table was then used to determine how much the clearing time from the first look up table must be adjusted to give an accurate value.

Another slight error is introduced by the clearing time look-up table. Interpolation and extrapolation methods are used to determine what values should be output when the input is not exactly equal to one of the data points in the look-up table. This can cause the clearing times to be slightly off. The region directly before the clearing times increase to greater than 1 second represents the most troublesome area. This could be improved by performing more characterization tests and getting more data points to reduce the amount of interpolation performed by the look-up table. As a point of reference, Simulink can plot the look-up table data, shown in Figure 5-7. This can be compared

with the voltage characterization graphs of Figures 4-3 and 4-4 to determine how much interpolation or extrapolation will occur.

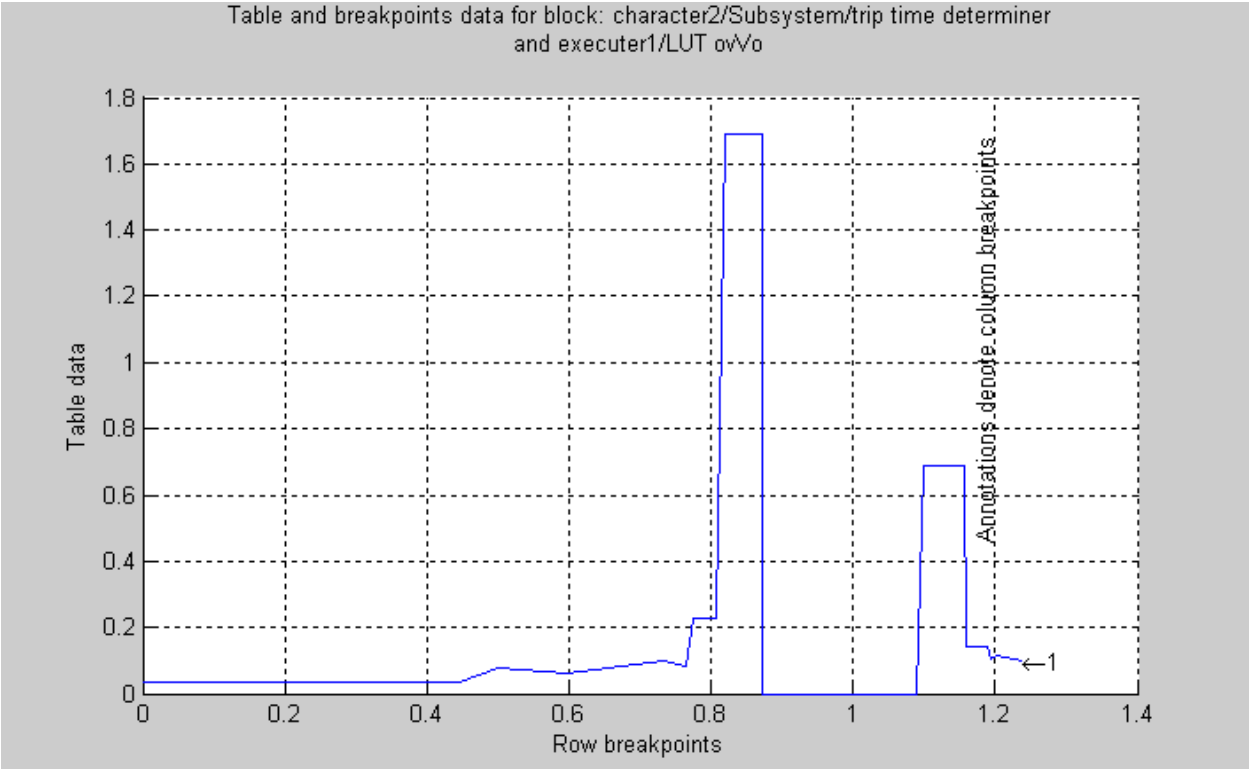

Figure 5-7 Clearing Time Look-Up Table

5.6 Summary

In this chapter, a method for modeling an EPS with a DR was described. The model focused on the embedded protection of the inverter that functions as the interface between the DR and the EPS. The results from the model were then compared to data taken from an actual inverter in a similar testing set up.

It was found that the model conforms, within a reasonable degree of accuracy, to the actual system. The clearing times for frequency trips are within about +/- 0.5 ms, while the accuracy of clearing times for voltage trips depends on the amount of data points in the look-up table, but are generally within 1 ms.

This model could be used to study the effects of implementing multiple DR onto an EPS. It could also be extended to more than just inverters. As the structure of an EPS changes, whether due to higher penetration of renewable resources or the formation of microgrids, the consequences for unanticipated interactions can only become graver. This model can reduce the amount of unanticipated interactions by allowing utility engineers to study various system configurations in a safe and flexible software environment.

6 Conclusions and Recommendations

6.1 Conclusions

The electric power system (EPS) infrastructure that generates, transports and distributes electricity is rapidly changing due to evolving sociopolitical, economic and technical climates. Distributed resources (DR) are constantly being integrated into the EPS. Some DR like wind and PV systems can be unpredictably intermittent. High DR penetration is expected to cause many difficulties. On the other hand, it also has the potential to be very beneficial by reducing pollution associated with carbon based fuels and possibly increasing grid stability. Tools are needed to model these DR and the changing grid infrastructure so that the effects of integration can be determined before installation takes place. If system designers can have a good understanding of how much DR to integrate and where on the grid to integrate it, a balance of large scale DR integration and a robust EPS can be achieved.

This thesis is focused specifically on grid-tied inverters because many DR, especially renewable resources, utilize an inverter when connecting to the EPS. These inverters typically have controllers that dictate how they interact with the grid. Often, information known about these controllers or other inverter details is limited to the user. If proper modeling of these devices is to occur, the inverter responses to variable grid conditions must be known.

There have been methods proposed for determining the interactions of grid-tied DR with the EPS, but none have achieved the characterization and modeling in such a flexible and powerful manner as what can be done with PHIL.

In this thesis, a methodology is proposed and executed for characterizing and modeling inverters for grid integration studies using PHIL. Modeling and characterization tools were developed for the purpose of providing a way to better understand the effects of integrating DR onto the grid. This methodology involved simulating a grid environment using a power amplifier, a load bank, an RTDS and an inverter.

The power amplifier was used to simulate an EPS and the load bank was used to simulate a load on an EPS. The RTDS was used to control both the power amplifier and the load bank in a manner that emulates an actual EPS. The IEEE 1547 Std. [**7**] was used as a guideline for simulating various abnormal grid conditions that were used to characterize the inverter. The inverter's responses to these conditions were monitored and compared to manufacturer's stated values as a method of validation.

These data were then used to construct a software model that reacted the same way as the actual inverter. This model was inserted into a software model of an EPS environment and the inverter model's response to certain conditions was validated against the data taken from the real inverter's response to similar conditions. It was found that the two responses agreed.

This testing and modeling scenario presents many opportunities to a range of engineers. It will allow utility engineers to simulate various grid configurations without having to construct complex and expensive test beds.

6.2 Recommendations

A variety of components could be characterized and modeled so that a wide range of systems can be simulated. Varying levels of DR penetration can be modeled to determine the possible benefits, such as improved grid support or drawbacks, such as cascading failure. Engineers who write technical standards could use this modeling to determine what requirements would be suite the EPS for different circuit configurations.

The scope of this thesis is limited to a grid-tied inverter's abnormal voltage, abnormal frequency and anti-islanding characteristics. It would be beneficial to extend this work to other characteristics, and to other grid-tied devices, such as a microgrid switch. This methodology could further be applied to more complex configurations, such as a real world microgrid.

The setup could be improved further to facilitate more detailed characterization and modeling of PV inverters. The constant DC input source could be replaced with a source capable of emulating PV

array characteristics. There are already various models available that will simulate a typical I-V curve of a solar panel. These models can be combined to form various PV array configurations. Code could then be added to the inverter control subsystem that simulates MPPT. Actual or simulated pyranometer data could then be used to control the DC input power to the PV inverter in a way that emulates a PV array. This would provide a simulation test bed for a whole PV system.

Another area this work could be improved upon is in the automation realm. The Opal-RT software used for characterizing grid-tied inverters is compatible with the Python scripting language. Code could be written that will automatically perform the characterization tests. Python not only has the capability to execute the Simulink software that was developed, but it can also modify parameters. Feedback from the previous test could be used to control what parameters are used for the next test. This would greatly reduce the amount of human involvement required in the process.

One very pertinent issue that could be tested using the work presented in this thesis is the concept of a cascading failure. The controllers in grid-tied DR are intended to protect both the DR and the grid from harmful conditions. If some sort of condition occurred that caused one DR to cease to energize the grid, could that DRs disconnection then cause other DR to disconnect and in effect greatly reduce the amount of generation on an EPS? This thesis aims to provide a method for testing this hypothesis with off-the-shelf inverters.

Another issue that could be addressed based on this thesis is the design of a microgrid. Microgrids can disconnect from the area EPS and form their own EPS. When this happens, the dynamics of power flow change on both the microgrid and the area EPS. The characterization and modeling method provided could be used to simulate such events and determine what types of problems may arise.

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8 Appendix

8.1 Index of Abbreviations

AC	Alternating Current
A/D	Analog to Digital
API	Application Programming Interface
CHIL	Controller Hardware-in-the-Loop
CSTP	Concentrated Solar Thermal Power
D/A	Digital to Analog
DC	Direct Current
DG	Distributed Generation
DR	Distributed Resource
EMI	Electromagnetic Interference
EPS	Electric Power System
EUT	Equipment Under Test
FPGA	Field Programmable Gate Array
HIL	Hardware-in-the-Loop
Hz	Hertz
MPPT	Maximum Power Point Tracking
ms	Millisecond
NI	National Instruments
NREL	National Renewable Energy Laboratory
PCC	Point of Common Coupling
PE	Power Electronics
PHIL	Power Hardware-in-the-Loop
PV	Photovoltaic
RMS	Root Mean Square
RTDS	Real Time Data System
THD	Total Harmonic Distortion

8.2 Software code

8.2.1 Anti-Islanding Analysis Script

```
%Danny Terlip 7/27/11
%Find the trip point and calculate time from grid disconnect

clear
clc

A = importdata('antiIsl9_26/AI3.csv', ',',26);
data = A.data;

obsTime = 400e-3;
sampFreq = 250e3;

t = 0:1/sampFreq:obsTime;
```

```
n = 1;
m = 1;
found = 0;

% find trip point
while found~=1
    if data(n,2) < .4   %potential trip
        found=1;          %initialize variables

        for  x  =  n:(n+(16.6667e-3*sampFreq*2))       %iterate  through  three
cycles
            if data(x,2)>2  %tolerance for trip condition, tighten if finding
trip point too early
                found = 0;
                break;
            end
        end
    else
        found = 0;  %just for debug purposes
    end
    n = n+1;
end


while abs(data(m,5)) < 5    %trigger
    m=m+1;
end

tripTime = (n-m)/sampFreq;
stepTime1m = m/sampFreq;
tripTime1m = n/sampFreq;

figure
subplot(3,1,1), plot(t,data(:,1)), title(['Measured Grid Voltage']),
    ylabel('Volts'),     xlim([stepTime1m-(16.6667e-3*2),tripTime1m+(16.6667e-
3*3)])

subplot(3,1,2),  plot(t,data(:,2)),  title(['Measured  Inverter  AC  Current
Trip Time: ' num2str(tripTime*1000) ' ms']),
    ylabel('Amps'),      xlim([stepTime1m-(16.6667e-3*2),tripTime1m+(16.6667e-
3*3)]), vline(stepTime1m,'r',''), vline(tripTime1m,'r','')

subplot(3,1,3), plot(t,data(:,5)), title('Measured Step Change Trigger'),
    xlabel('Time             (sec)'),             xlim([stepTime1m-(16.6667e-
3*2),tripTime1m+(16.6667e-3*3)])
```

8.2.2 Frequency Ramp Analysis Script

```
%Danny Terlip 7/25/11
%Find the trip point and calculate the frequency right before

A = importdata('UFR1.csv', ',', 26);
data = A.data;

sampFreq = 250e3;
obsTime = 400e-3;
```

```
t = 0:1/sampFreq:obsTime;
n=1;


found = 0;

while found~=1
    if data(n,2) < .4   %potential trip
        found=1;          %initialize variables
        %n/sampFreq
        for x = n:(n+(sampFreq/30))    %iterate through two cycles

            if abs(data(x,2))>2.1       %threshold
                found = 0;
                break;
            end
        end
    end
    n = n+1;
end

while abs(data(n,1))>.01
    n=n-1;
end

zC1 = n/sampFreq-.000004;
n = n-100;

while abs(data(n,1))>.5
    n=n-1;
end

zC2 = n/sampFreq-.000008;

freq = 1/2/(zC1-zC2);


[AX,H1,H2] = plotyy(t,data(:,1),t,data(:,2));
title(['trip @ ' num2str(freq) ' Hz']), xlabel('Time (sec)')
set(get(AX(1),'Ylabel'),'String','Voltage')
set(get(AX(2),'Ylabel'),'String','Current')
legend([H1,H2],'Vac','Iac')
vline(zC1,'r-',''), vline(zC2,'r-',''), hline(0,'r-','')
```

8.2.3 Frequency Step Analysis Script

```
%Danny Terlip 7/25/11
%calculate the trip time for a frequency step

clear
clc

A = importdata('dannyChar/OF18.csv', ',',26);
data = A.data;
```

```
obsTime = 400e-3;
sampFreq = 250e3;

t = 0:1/sampFreq:obsTime;
n = 1;
m = 1;
found = 0;

while found~=1
    if data(n,2) < .4   %potential trip
        found=1;          %initialize variables

        for  x  =  n:(n+(16.6667e-3*sampFreq*2))       %iterate  through  three
cycles
            if  data(x,2)>2.5    %tolerance  for  trip  condition,  tighten  if
finding trip point too early
                found = 0;
                break;
            end
        end
    else
        found = 0;  %just for debug purposes
    end
    n = n+1;
end


while abs(data(m,5)) < 5    %trigger
    m=m+1;
end

time = (n-m)/sampFreq;
i = m;
freq = [0 0];
for j = 1:2
    while abs(data(i,1)) > .4    %find freq after trigger
        i = i+1;
    end
    freq(1,j) = i;
    i = i + 50;
end

freq(1,1)  =  freq(1,1)/sampFreq  -  12e-6;       %made  adjustments  for  zero
crossing here
freq(1,2) = freq(1,2)/sampFreq - 5e-6;

freqFinal = 1/(2*(freq(1,2) - freq(1,1)));
stepTime1m = m/sampFreq;
tripTime1m = n/sampFreq;
figure
subplot(3,1,1),  plot(t,data(:,1)),  title(['Measured  Grid  Voltage       New
Frequency: ' num2str(freqFinal) ' Hz']),
    ylabel('Volts'),     xlim([stepTime1m-(16.6667e-3*2),tripTime1m+(16.6667e-
3*3)]),
```

```
    vline(freq(1,1), 'r-',''),vline(freq(1,2),'g-',''),hline(0,'r-','')

subplot(3,1,2),  plot(t,data(:,2)),  title(['Measured  Inverter  AC  Current
Trip Time: ' num2str(time*1000) ' ms']),
    ylabel('Amps'),      xlim([stepTime1m-(16.6667e-3*2),tripTime1m+(16.6667e-
3*3)]), vline(stepTime1m,'r',''), vline(tripTime1m,'r','')

subplot(3,1,3), plot(t,data(:,5)), title('Measured Step Change Trigger'),
    xlabel('Time              (sec)'),             xlim([stepTime1m-(16.6667e-
3*2),tripTime1m+(16.6667e-3*3)])
```

8.2.4 Voltage Ramp Analysis Script

```
%Danny Terlip 7/25/11
%Find trip point for Voltage Ramp

clear
clc

A = importdata('UVR211_01.csv', ',', 26);
data = A.data;

obsTime = 1000e-3;
sampFreq = 100e3;

t = 0:1/sampFreq:obsTime;
n=1;
check = 0;
found=0;

while found~=1
    if data(n,2) < 1   %potential trip
        found=1;         %initialize variables

        for  x  =  n:(n+(16.6667e-3*sampFreq*3))       %iterate  through  three
cycles
            if abs(data(x,2))>1.5   %tolerance for trip condition, tighten if
finding trip point too early
                found = 0;
                break;
            end
        end
    else
        found = 0;  %just for debug purposes
    end
    n = n+1;
end

tripPoint = n;

[tripValue,tripValueIndex] = max(abs(data((n-sampFreq/120):n,1)));   %find max
voltage in previous half cycle
tripValueIndex = tripValueIndex+(n-sampFreq/120);                    %index
of trip value
```

```
hold off
[AX,H1,H2] = plotyy(t,data(:,1),t,data(:,2));
title(['trip @ ' num2str(tripValue/sqrt(2)) ' Vrms']), xlabel('Time (sec)')
set(get(AX(1),'Ylabel'),'String','Voltage')
set(get(AX(2),'Ylabel'),'String','Current')

hold on
H3 = vline(tripPoint/sampFreq,'r','')
H4 = vline(tripValueIndex/sampFreq,'k','')
legend([H1,H2,H3,H4],'Vac','Iac','Trip Point', 'Trip Value')
```

8.2.5 Voltage Step Analysis Script

```
%Danny Terlip 7/25/11
%calculate the trip time for a voltage step

%clear
%clc

filename = 'tripTests/OV116';
obvTime = 400e-3;       %observation time in seconds
sampFreq = 250e3;   %Sampling frequency

A = importdata([filename '.csv'], ',', 26);
data = A.data;

t = 0:1/sampFreq:obvTime;
n = 1;
m = 1;
found = 0;


while found~=1
    if data(n,2) < .4   %potential trip
        found=1;         %initialize variables

        for x = n:(n+(sampFreq/30))    %iterate through two cycles

            if abs(data(x,2))>2.1       %threshold
                found = 0;
                break;
            end
        end
    end
    n = n+1;
end


while abs(data(m,5)) <5    %find trigger > -5
    m=m+1;
end
```

```
%calculate %step
newData1 = data(m+sampFreq/20:(end-sampFreq/10), 1);    %m+x gets you past
transients
newData2 = data(1:m,1);
[y1,i1]=max(newData1);
[y,i]=max(newData2);
perc = max(newData1)/max(newData2);

time = (n-m)/sampFreq;

stepTime1m = m/sampFreq;
tripTime1m = n/sampFreq;
figure
subplot(3,1,1), plot(t,data(:,1)), title(['Measured Grid Voltage     Voltage
Change: ' num2str(perc*100) '%']),
    ylabel('Volts'),     xlim([stepTime1m-(16.6667e-3*2),tripTime1m+(16.6667e-
3*3)]), vline((i1+m+sampFreq/10)/sampFreq,'r','')

subplot(3,1,2),  plot(t,data(:,2)),  title(['Measured  Inverter  AC  Current
Trip Time: ' num2str(time*1000) ' ms']),
    ylabel('Amps'),      xlim([stepTime1m-(16.6667e-3*2),tripTime1m+(16.6667e-
3*3)]), vline(stepTime1m,'r',''), vline(tripTime1m,'r',''), ylim([-20,20])

subplot(3,1,3), plot(t,data(:,5)), title('Measured Step Change Trigger'),
    xlabel('Time              (sec)'),             xlim([stepTime1m-(16.6667e-
3*2),tripTime1m+(16.6667e-3*3)]), ylim([-1,20])
```