Design and Control of a Modular Resonant DC-DC Converter for Point-of-Load Applications

by

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Design and Control of a Modular Resonant DC-DC Converter for Point-of-Load Applications

Thesis directed by Prof. Dragan Maksimović and Prof. Regan Zane

Point-of-load (POL) power supplies are high-output-current, low-output-voltage, DC-DC converters that are placed near the electronic components, such as memory chips and microprocessors, on a computer motherboard. They have to meet challenging requirements of high efficiency over a wide load range, and fast transient responses to very dynamic load profiles. The most popular POL topology is based on single-phase or multi-phase buck converters. Buck converters have limitations in large step-down applications due to very low duty cycle requirements for the control MOSFET(s), and relatively high switching losses at high frequencies.

This work proposes a new converter architecture and control method for POL applications - a modular converter based on active-clamp LLC resonant modules, designed to work with an on/off digital controller. The active clamp LLC converter inherits advantages of the standard LLC resonant converter, including soft-switching and 50%-duty-cycle operation of all switching devices. The active clamp addresses the voltage oscillation across the rectifier devices caused by transformer secondary-side leakage inductances and MOSFET output capacitances by clamping the voltage to approximately twice the output dc voltage. In addition, the active clamp helps to reduce the output capacitor current ripple. The converter is well suited for a multiple-parallel-module configuration in which each module, when on, operates at its maximum efficiency. The output voltage is regulated by turning on/off one module in a pulse-width-modulation (PWM) manner while the other modules are either fully on or fully off, depending on the load power demand.

Analysis, modeling, design and control methods are described for the modular active-clamp LLC converter and the results are verified on experimental prototypes. It is found that the proposed converter and the corresponding control approach yield high overall efficiency and fast step-load transient responses. The approach is suitable for single or multi-module high-frequency high-step-

down low-voltage point-of-load applications where secondary-side devices and control circuitry can be integrated in a low-voltage CMOS process.

Dedication

To my dear family - my father Tuan Nguyen, my mother Dan Tran and my sister Ngoc-Hien Nguyen.

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Introduction

1.1 Point-of-Load (POL) Converters

1.1.1 POL in Power Distributed System

In computing and communication systems, POL converters are on-board DC power supplies positioned near electronics components, which draw high current (tens to more than 100 A) at low voltage (3.3 V or less) [6, 7]. The name POL comes from the fact that the converter has to be placed as close to the load as possible for efficiency and regulation purposes. Fig. 1.1 shows an example of a typical server board. In this so-called distributed power system, the power supply unit (PSU) may consist of an AC-DC rectifier followed by a DC-DC converter, or only DC-DC converter(s), depending on the input voltage [6, 8]. The PSU typically provides voltage isolation between its input and its output, and feeds a lower intermediate bus voltage to various downstream power converters, mainly POLs. These POLs convert and finely regulate the proper output voltages to their corresponding electronic loads, such as microprocessors, memory chips and various peripherals. When the load is a microprocesor, a POL is specifically called voltage regulator module (VRM) because of the loads' special voltage and current demands, which are addressed briefly in Section 1.1.2.

The distribution bus voltage is usually 12 V, but a value of 8, 24 or 48 V are also in use, depending on the system configuration [6, 9, 10]. With current POL topology, a 7-8 V bus yields high POL's efficiency, but may cause additional cost if there are other substantial loads requiring

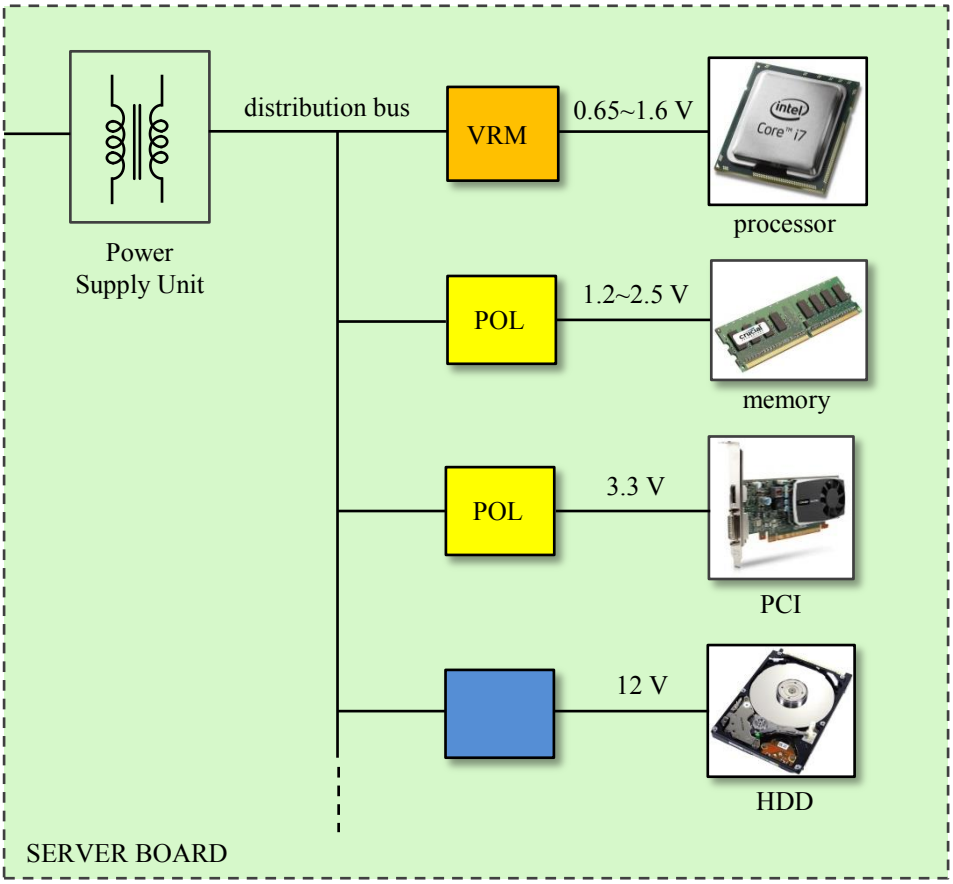


Figure 1.1: Typical power conversion and distribution on a computer server board

12 V supply. In very low-voltage high-current applications such as high-end workstations and data centers, a bus voltage as high as 48 V is more appealing because current at the distribution bus is lower, which means that conduction losses are reduced.

1.1.2 POL Design Challenges

1.1.2.1 System Level

An important system aspect to consider is the POL power level. The power level ranges from about 30 W for a laptop [11] to hundreds of watts per server board [1, 2, 12, 13]. In large data centers, the installation of multiple servers raises the power to kW level. At these power levels, any drops in efficiency cause increased power losses, which leads to undesirable consequences regarding

cooling and cost of electricity.

Another challenge in data center's power supply design comes from the significant difference between the worst-case power rating, i.e., the nameplate peak value, the actual peak, and the average power [1, 12]. The nameplate peak power is set conservatively by assuming all electronic components run at their rated power, and by adding a safety margin on top. However, this scenario rarely happens because of the nature of a server's workload, which usually demand the usage of some components more than the others. Besides, due to the dynamic change of the workloads, the average power is reduced further compared to the observed peak value. Fig. 1.2 demonstrates the difference among the aforementioned power values at different workloads in a data center. This suggests that POLs are often over-designed in order to handle the worst-case scenario. Moreover, designers need to optimize the converter efficiency over a range of lighter load, even at less than 36% of the rating. Since the load power is not easily predicted and changes dynamically over wide range, it is important that the converter maintains high efficiency over as wide load range as possible.

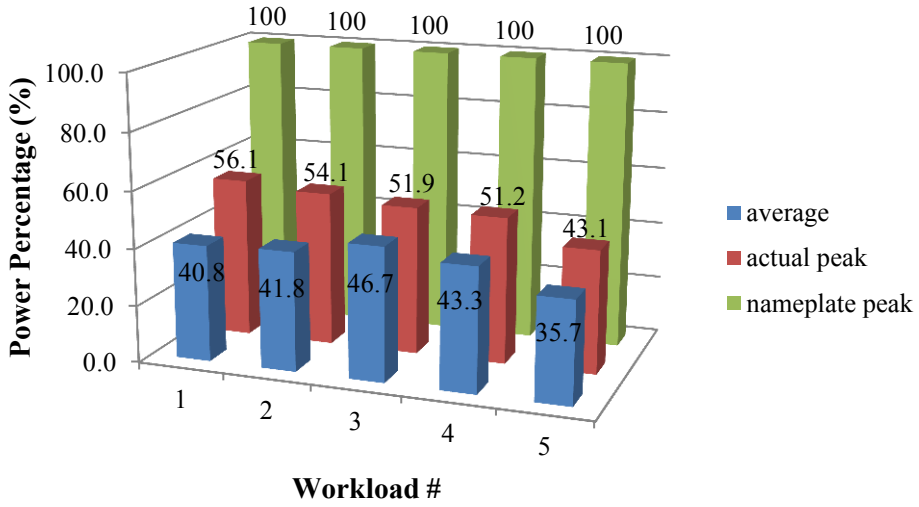


Figure 1.2: Normalized nameplate peak, actual peak and average power at different workloads in a data center [1]. Normalization is based on the nameplate peak power.

For each server, it is important to understand the power demand of different components. Fig. 1.3 shows the average power breakdown of a typical server board [2]. In general, CPU (central

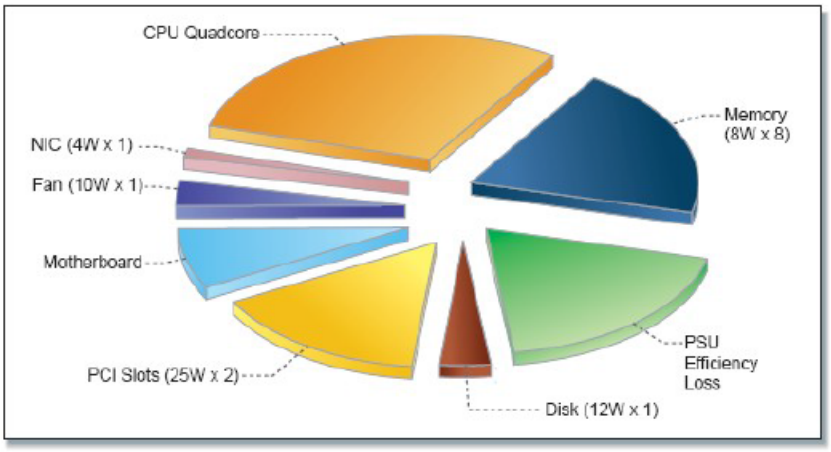


Figure 1.3: Average power breakdown for a server [2]

processing unit), or microprocessor, consumes the most power on average. Besides, its supply current demand can vary from about 1 A to about 130 A [10], which suggests the need to optimize converter efficiency over a wide load range. The second most power consuming component is memory. Along with the microprocessor, it is the main contributor to the dynamic power demand in a server [1, 14]. Memory usage is growing along with the number of processor cores, especially in data centers with memory intensive search applications such as in Facebook or Google data centers [2, 14].

1.1.2.2 Circuit Level

From the system point of view, maintaining POL's high efficiency over a wide load range is very important, especially in large data centers. At the circuit level, other POL design challenges include circuit parasitics, and strict voltage regulation requirements [15–17].

Data processing integrated circuits (ICs) have been demanding higher supply currents at lower supply voltages. In the next few years, it is expected that the microprocessor current demand will reach 200 A, with supply voltage reduced to as low as 0.5 V [7,18]. At high current and low voltage, a small parasitic resistance of the connection between the POL output and the load can cause a significant voltage drop. Fig. 1.4 shows a model of the supply-to-load connection, including trace

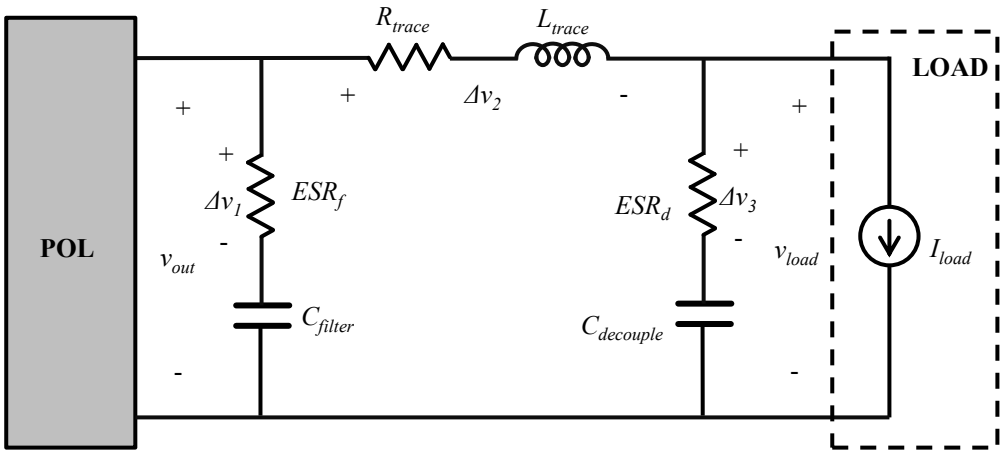


Figure 1.4: Model of the connection between a POL and its load

resistance R_{trace}, trace inductance L_{trace}, filter capacitor at the POL output C_{filter} in series with its parasitic resistance ESR_f, decoupling capacitance $C_{decouple}$ right across the load supply input and its parasitic resistance ESR_d. At a steady state load current $I_{load} = 10\ A$, the connection's parasitic $R_{trace} = 10\ m\Omega$ causes a voltage drop $\Delta v_2 = 100\ mV$. POL design typically requires steady-state output voltage regulation within 1% of the nominal value. In 3.3 V applications, a 100 mV voltage drop is already unacceptable. This also suggests that voltage sensing needs to be placed close to the load for accurate voltage regulation. In 1-2 V applications, even a 20 mV voltage drop due to the parasitic resistance results in 1-2% drop in efficiency [16].

For a large load step, parasitics play more important roles regarding dynamic output voltage regulation. It is typically required that the output voltage remains within 5% of the nominal voltage under all transients. A microprocessor's load current slew rate, which can be as high as 1.2 A/ns now, is expected to reach even higher values (e.g. 2.5 A/ns) in the near future [7]. A 1 cm trace has an approximate inductance $L_{trace} = 10\ nH$. Without a decoupling capacitor right across the load supply terminals, a load step at 1.2 A/ns will cause a voltage drop of $\Delta v_2 = L_{trace} di/dt = 12\ V$. Even with the decoupling capacitor, high parasitic ESR can cause significant change in the load voltage v_{load} upon a step load transient. It is the designer's task to choose proper supply decoupling, including low-ESR capacitors, to meet the strict voltage regulation. On the other hand, oversized

capacitors are subject to space limitations and cost concerns. In addition, a fast controller is also required to settle the voltage back to regulation as quickly as possible, with response times usually in the order of tens of micro-seconds [7].

In VRM applications, there is an additional requirement for voltage regulation related to adaptive voltage control. In order to reduce microprocessor's power consumption, manufactures have developed technology to adjust the supply voltage according on the load current. Therefore, the VRM is required to be able to modify the output voltage depending on the voltage command sent from the microprocessor [19, 20].

In summary, POLs are DC-DC converters that are placed closely to the electronic loads (microprocessor, memory, etc.). Because these loads demand low supply voltage, high current, and have large dynamic range and slew rate, POL design faces very challenging requirements of:

- High efficiency over wide load range;
- Proper choice and placement of output capacitors to maintain voltage within tight regulation window (e.g. within 5%) in transients, while considering cost and space limitations;
- A controller that responds quickly to rapid load steps.

1.2 Topology Considerations

1.2.1 Synchronous Buck Converter

Single- or multi-phase synchronous buck converter has been widely used as the POL topology of choice, thanks to its simple structure and control. This subsection gives a brief explanation of the converter operation, as well as design improvements and limitations in applications that have increasing demands for low voltage and high supply current.

1.2.1.1 Basic Operation

Fig. 1.5 shows the circuit diagram of a synchronous buck converter, its equivalent circuit in two subintervals, and typical waveforms, including switching node voltage v_{sw}, inductor voltage v_L

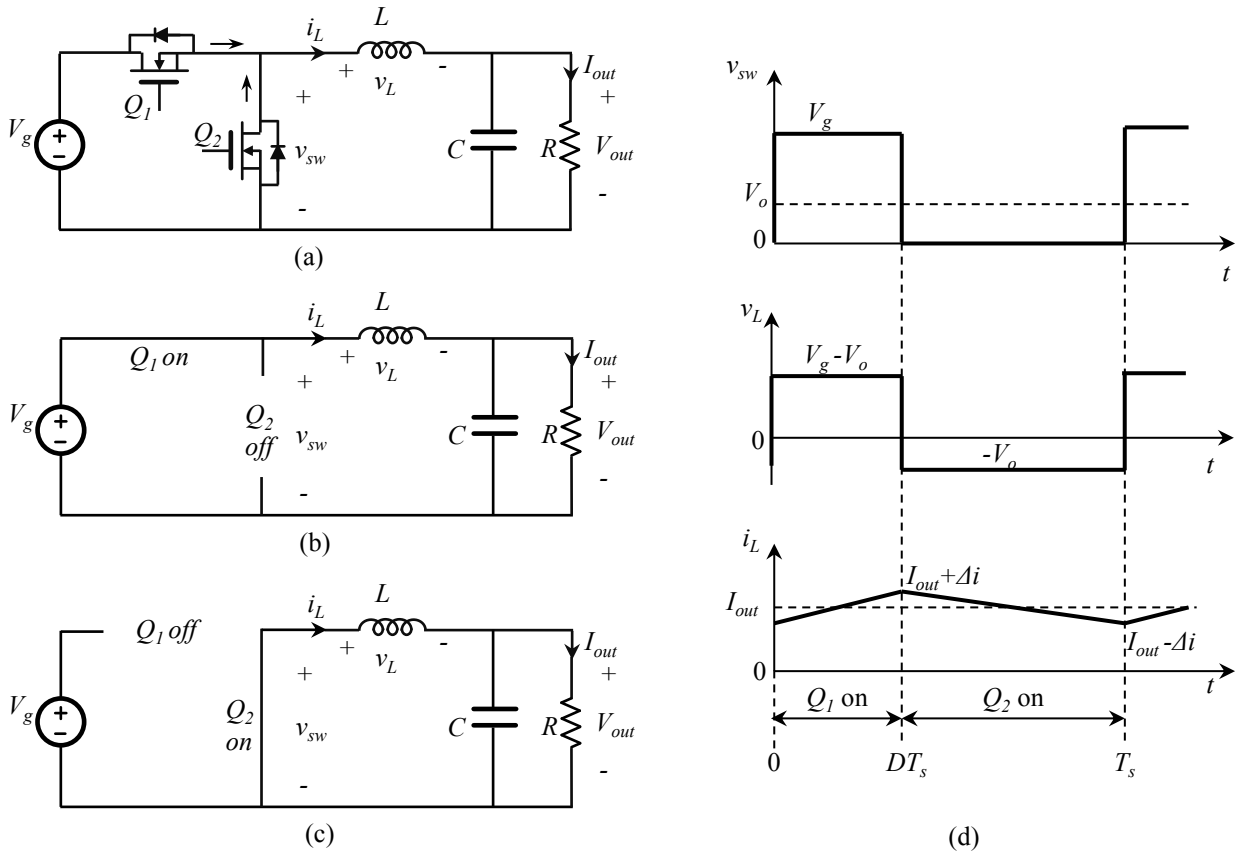


Figure 1.5: (a) Synchronous buck converter, its equivalent circuit in (b) subinterval 1, and (c) subinterval 2, and (d) typical waveforms during one switching cycle

and current i_L, during one switching cycle T_s. In the first subinterval, the control switch Q_1 is turned on for a duration of DT_s, transferring energy from input to the LC circuitry and the output. The percentage of time that Q_1 conducts is defined as duty cycle D. In the second subinterval, Q_1 is off and the synchronous rectifier switch Q_2 is on. The input is disconnected from the output, and the LC circuitry provides its stored energy to the load. In other words, the switching of Q_1 and Q_2 generates a square-wave voltage at the switching node. The inductor and the capacitor form a low-pass filter, filtering out most of the high-frequency components of the switching voltage v_{sw}. Therefore, the output voltage is the DC component of v_{sw},

$$V_{out} = DV_g \tag{1.1}$$

Depending on the application requirements, L and C have to be large enough to maintain

small switching ripples in the inductor current and the output voltage. However, a bulky inductor slows down converter's transient response when the output experiences a step in load. This is demonstrated in Fig. 1.6.

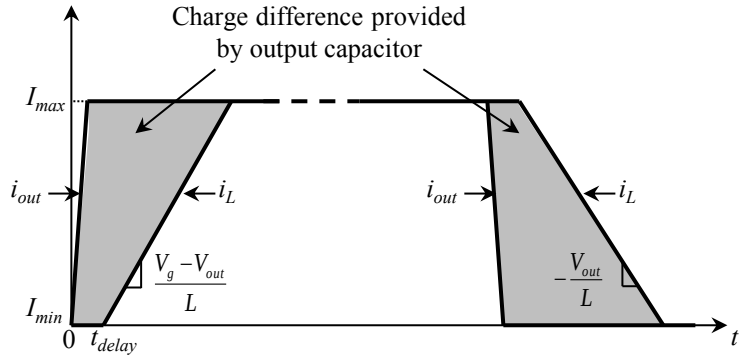


Figure 1.6: Simplified waveforms of imbalance between inductor and output currents during a load step transient

During a step change from light to heavy load, the inductor current i_L takes a certain delay time t_{delay} to start ramping up and supply additional current to the output. The ramping slope is limited to $(V_g - V_{out})/L$, which consequently limits the time it takes i_L to reach the new output current. During that transient time, the output capacitor is discharged to provide the load with the difference between the inductor and the output current. This causes a drop in the output voltage. Similarly, during a heavy-to-light load step, the inductor current ramps down at a limited slope of $-V_{out}/L$. The output capacitor is charged with the excessive current, causing an output voltage overshoot. As a result, the output capacitance has to be large enough in order to meet strict transient voltage regulation requirements. A larger inductor means slower transient response and larger output capacitor. As the load current and slew rate keep increasing, transient response presents a challenge for the buck converter design.

In the synchronous buck converter, switch Q_2 is implemented as MOSFET instead of a diode rectifier. At high load current, this helps to increase the converter efficiency by reducing the conduction loss caused by the voltage drop V_{diode} across the diode, $P_{loss} = V_{diode}I_{out}$. However, efficiency at light load is generally poor, which presents a challenge when the load demands very

high maximum current and operates over wide load range.

1.2.1.2 Interleaved Multi-phase Buck Converter

Interleaved multi-phase buck converter [21, 22] is a popular solution for transient response and efficiency issues in the synchronous buck converter in POL applications. Fig. 1.7 shows an example of a two-phase buck converter and its current waveforms during one switching cycle.

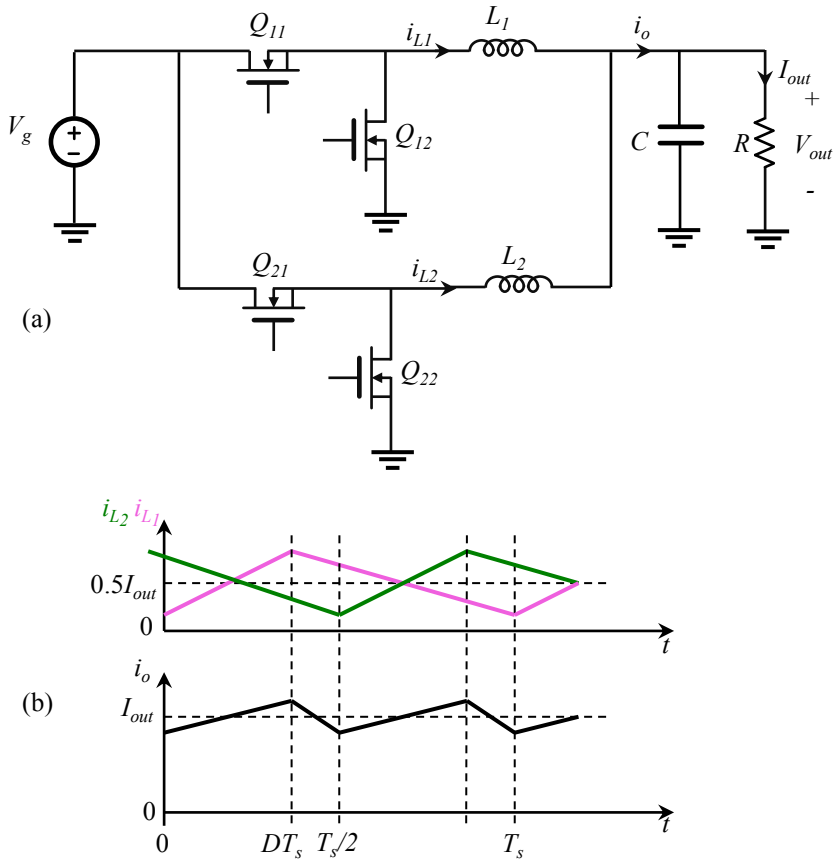


Figure 1.7: (a) Two-phase synchronous buck converter and (b) current waveforms during one switching cycle

By operating two buck modules at a phase shift of $T_s/2$, the ripples of individual inductor currents i_{L1} and i_{L2} cancel with each other. The result is a smaller ripple in the output current i_o seen by the output filter capacitor C. Given the same output current ripple requirement, the inductance in each phase can be reduced compared to the single-phase topology. Moreover, the

multi-phase converter's equivalent inductance is only $L/2$, where $L_1 = L_2 = L$, which helps improve the load-step transient response. In addition to a faster transient response, efficiency over wide load range can further be improved by phase shedding technique, in which some phases are turned off at lighter load levels [23].

1.2.1.3 Limitations

Although multi-phase synchronous buck converter demonstrates improvements in transient responses and efficiency, it still has some limitations associated with the original single-phase buck topology.

First, the step-down voltage range is limited because of the need to operate at low duty cycle. For example, a 48 V-to-1 V POL requires a duty cycle of 2.1%, which makes implementation of switching devices, drive circuitry, and controller difficult and costly, especially at higher switching frequencies. In a distributed power system with high load current, reducing the bus voltage (POL's input voltage), is not favored for efficiency reasons. Because the load voltage keeps decreasing while load currents become higher, the buck converter limitations may become more severe in the future.

Second, there are limited options for the synchronous switch Q_2 in high step-down-voltage applications. Since this switch conducts high output current most of the time, a MOSFET with low on-resistance is required to reduce conduction loss. However, Q_2 has to block a high input voltage during off-state, and there is trade-off between low on-resistance and high break-down voltage [24].

Third, the practical operating frequency f_s is limited because of low duty cycle and high switching losses. In every switching cycle, at the transition moments between one switch turning off and the other turning on, a certain amount of energy E_{sw} is lost due to various reasons: charging and discharging of device output capacitances, losses associated with reverse recovery the synchronous switch's body diode, finite switching speed, etc. [5, 25–27]. Since switching loss is proportional to switching frequency, $P_{sw} = f_s E_{sw}$, there are practical limits to how high the switching frequency can be (currently typically in the hundreds of kHz range). Consequently, there are limited opportunities to reduce the size of passive components (L and C) and to improve transient responses [7,21,28].

1.2.1.4 Hard-switching Example in the Buck Converter

The lossy turn-on and turn-off of power devices, for example in the buck converter, is commonly referred to as hard switching. This sub-section briefly analyzes the hard-switching mechanisms in the buck converter, as a motivation to examine alternative converter topologies.

Fig 1.8a illustrates losses caused by hard-switched turn-on of control switch Q_1 in a buck converter, assuming other circuit components are ideal and MOSFET's drain-to-source capacitance is neglected. In order to prevent shoot-through, or the cross-conduction of both switches Q_1 and Q_2, a short dead-time is added in between turn-off of one switch and turn-on of the other one. During the dead-time after Q_2 is turned off, its body-diode takes turn to conduct current i_L, which is approximately equal to the output current I_{out}. When Q_1 is turned on, its drain-to-source voltage v_{ds1} and current i_{ds1} do not change simultaneously. At first, the current rises from 0 to I_{out} to

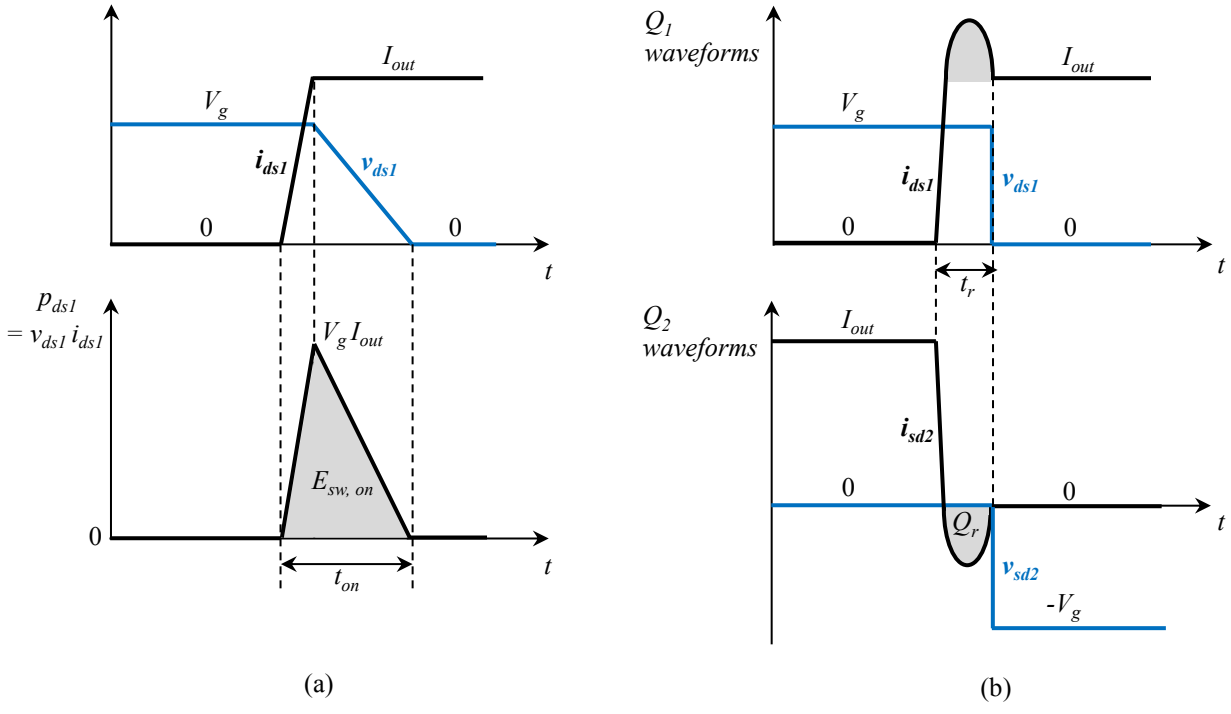


Figure 1.8: Switching loss in a buck converter caused by (a) hard-switched turn-on of Q_1 and (b) body diode reverse recovery during hard-switched turn-off of Q_2

reverse bias and turn off Q_2 body-diode. After that, v_{ds1} can start falling from V_g to 0. The overlapping of non-zero voltage and current during the transition time t_{on} results in a switching loss,

$$E_{sw,on} \approx 0.5 V_g I_{out} t_{on}. \tag{1.2}$$

Note that at Q_1 turn-on transition, the energy stored in the MOSFET's drain-to-source capacitor is dissipated, causing extra loss. The MOSFET's hard turn-off is similar but with the time axis reversed. However, the switching loss in this case is mitigated because part of the energy is useful in charging the drain-to-source capacitance.

Another source of loss is the reverse recovery of Q_2's body diode at hard-switched turn-off transition. Assume that all other components are ideal. When a diode is turned-off from a high-current forward-biased operating point, it requires a negative current to remove all the stored minority-carrier charge, which is called reverse recovery charge Q_r. The diode stays forward-biased during this recovery time t_r. After all the charge is removed, the diode becomes reverse-biased. Although there is insignificant loss dissipated in the body diode, this causes an overlapping of non-zero voltage and current in the control switch Q_1, as shown in Fig 1.8b. The loss energy caused by reverse recovery is,

$$E_{sw,r} \approx V_g (I_{out} t_r + Q_r). \tag{1.3}$$

In order to reduce switching loss in hard-switched power devices, soft-switching techniques can be implemented. In general, zero-voltage switching (ZVS) is preferred for the MOSFET's turn-on transition, while zero-current switching (ZCS) is more suitable at diode's turn-off transition [5].

1.2.2 LLC Resonant Converter

The LLC resonant converter shown in Fig. 1.9 has been investigated in 12 V to 48 V output DC-DC conversion applications [3, 29–36].

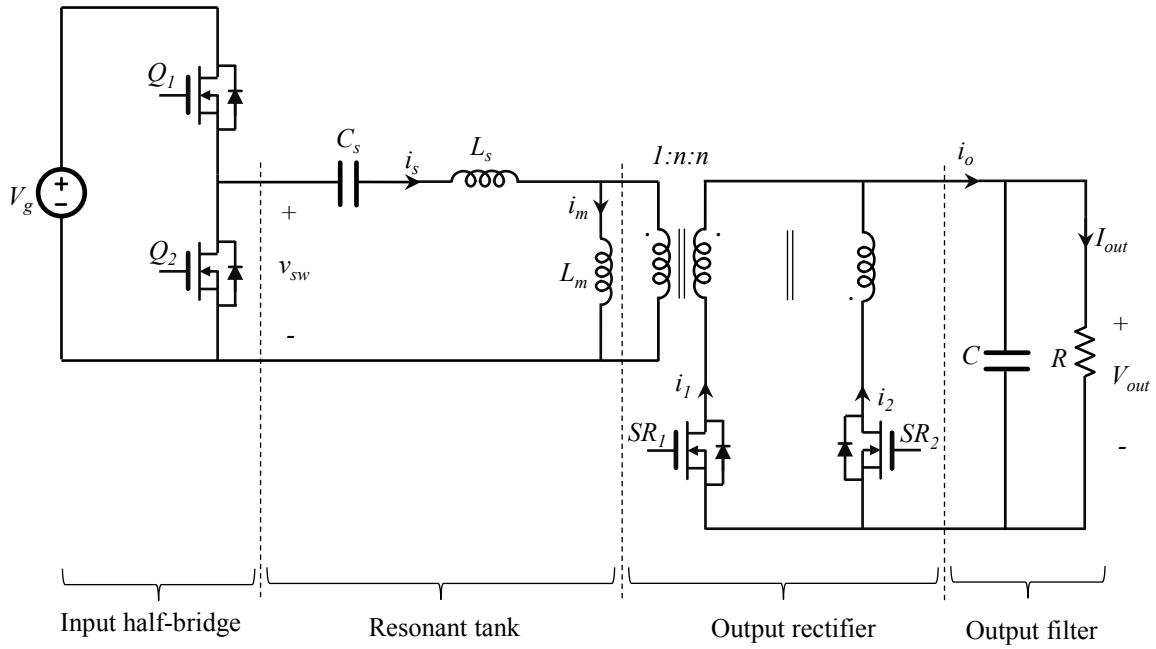


Figure 1.9: LLC resonant converter

While buck converter shows limitations in terms of low duty cycle and high switching loss, the LLC converter has capabilities of zero voltage switching (ZVS) of MOSFETs on the primary side, zero current switching (ZCS) of the rectifier MOSFETs, and almost 50% duty cycle switching of all devices. All of these benefits make it a good candidate for POL applications. This section explains the basic operations of this topology and considers it as a candidate for a low-voltage high-current power supply.

1.2.2.1 Basic LLC Operation

Fig. 1.10 shows the typical waveforms of the LLC resonant converter operating in ZVS region.

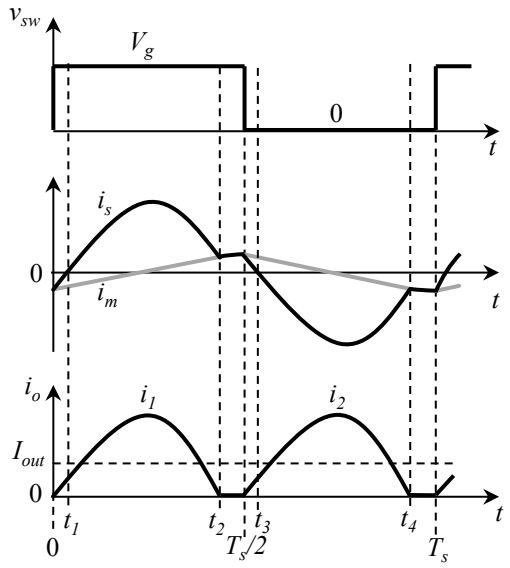


Figure 1.10: Typical waveforms of LLC resonant converter operating in ZVS region

As shown in Fig. 1.9, the converter contains a half-bridge that has two MOSFETs Q_1 and Q_2 switching at 50% duty cycle in complementary manner. A square-wave voltage v_{sw} is generated at the input switching node by the half-bridge, and fed to the resonant tank L_s-L_m-C_s. Different from the LC low-pass filter used in the buck converter, the LLC tank has a resonant frequency relatively close to the switching frequency. Therefore, it lets the tank inductor current i_s resonate with high ripple, enabling ZVS of the switches. A transformer is added to facilitate a large voltage step-down from input to output. Note that the transformer magnetizing inductance L_m and primary-side leakage inductance are included in the resonant tank. On the output side, a synchronous rectifier converts bi-polar current from the input into positive current i_o. Finally, the output capacitor filters the high-frequency components of i_o, allowing the DC component to supply the load.

LLC converter's soft-switching features are explained by looking at its operation during different intervals. Fig. 1.11 shows the conduction path during one half of a switching cycle T_s. At

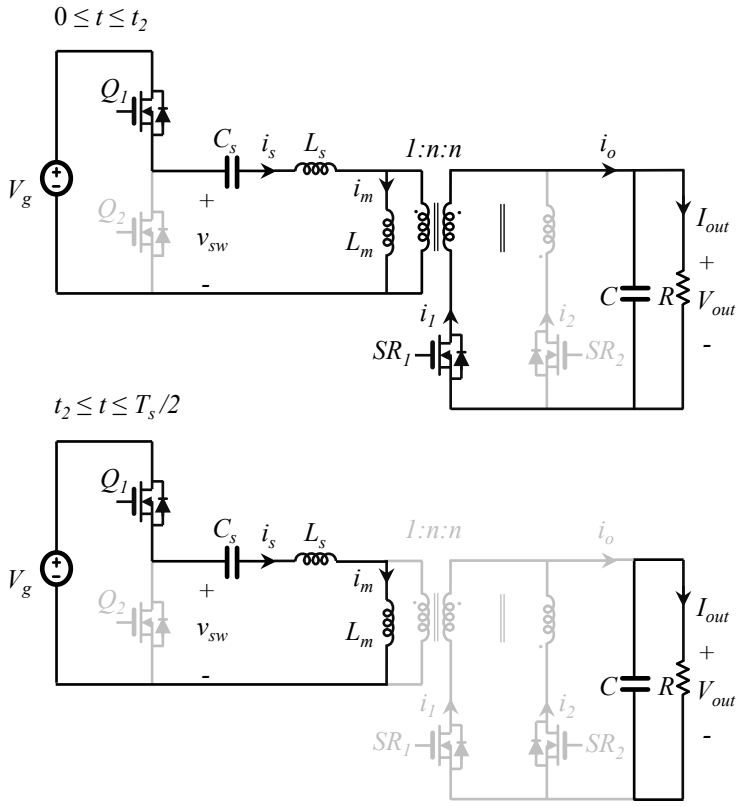


Figure 1.11: Schematics of LLC resonant converter during the first half of a switching cycle

the beginning of the switching cycle (time 0), the low-side switch Q_2 is turned off. The negative tank current i_s starts flowing through body diode of the high-side switch Q_1, setting its drain-to-source voltage close to zero. Before the tank current changes polarity at t_1, Q_1 is turned on at zero voltage, resulting in negligible switching loss. On the secondary side, the synchronous rectifiers are driven properly to behave like rectifier diodes with less conduction loss [37–40]. Because i_s becomes greater than magnetizing current i_m, current is transferred to the secondary side and SR_1 starts conducting. It clamps the voltage across transformer's magnetizing inductance to V_{out}/n, where n is the transformer turns ratio. Therefore, during the first interval, the magnetizing current i_m increases linearly, and the resonant tank consists of only C_s and L_s. This interval ends when $i_s = i_m$, making the secondary-side current $i_1 = 0$ and SR_1 is turned off at zero current with minimum loss.

In the second interval, from t_2 to $T_s/2$, there is no current conducting on the secondary

side, and the input is isolated from the output. The resonant tank now contains L_m, L_s and C_s. This interval ends when Q_1 is turned off and Q_2 is turned-on at zero voltage. As the switching frequency is closer to the L_s-C_s resonant frequency, this interval is shortened and does not exist in above resonance operation. The converter operation in the second half of a switching cycle is similar to the first half with SR_2 rectifying the secondary-side current, and being turned off at zero current.

In contrast to the buck converter, the voltage conversion ratio of the LLC resonant converter is a non-linear function of load and switching frequency, as shown in Fig. 1.12.

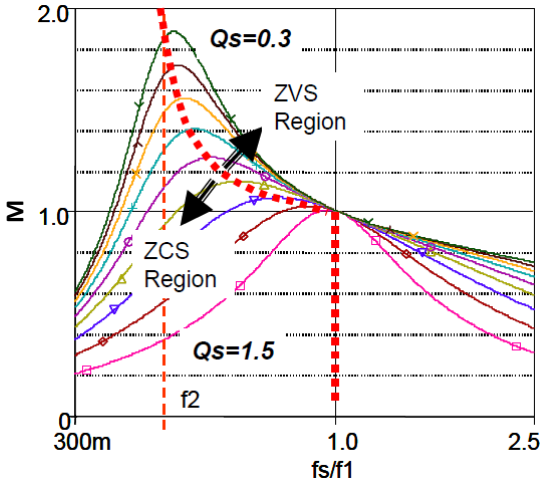


Figure 1.12: DC characteristic of LLC resonant converter [3]

Converter parameters are defined as follows,

$$M = \frac{V_{out}}{(0.5nV_g)} \qquad Q_s = \frac{n^2\sqrt{L_s/C_s}}{R}$$

$$f_1 = \frac{1}{2\pi\sqrt{L_sC_s}} \qquad f_2 = \frac{1}{2\pi\sqrt{(L_s+L_m)C_s}}.$$

At different loads corresponding to different Q_s values, the frequency needs to change in order to keep the same output voltage. The converter is usually designed to operate near resonant frequency f_1 in order to have a small range of frequency variation.

Similar to multi-phase buck architecture, paralleling multiple LLC converters can help increase the load capacity and efficiency [41–47], especially with phase shedding technique [46, 47]. Besides that, by interleaving LLC phases, the output current ripple can be further reduced.

1.2.2.2 Secondary-Side Voltage Ringing

There are very few works investigating LLC resonant converter in POL applications [48,49]. In large-step-down low-voltage applications, leakage inductance on the transformer secondary windings cannot be ignored, especially at high switching frequencies. As shown in Fig. 1.13, the leakage inductance interacts with the rectifier MOSFET output capacitance, causing voltage ringing and higher voltage stress across the secondary-side MOSFETs. In extreme cases, it even worsens the performance of synchronous rectifiers, inducing extra losses at heavy loads, and slows down transient response to load steps [48–52].

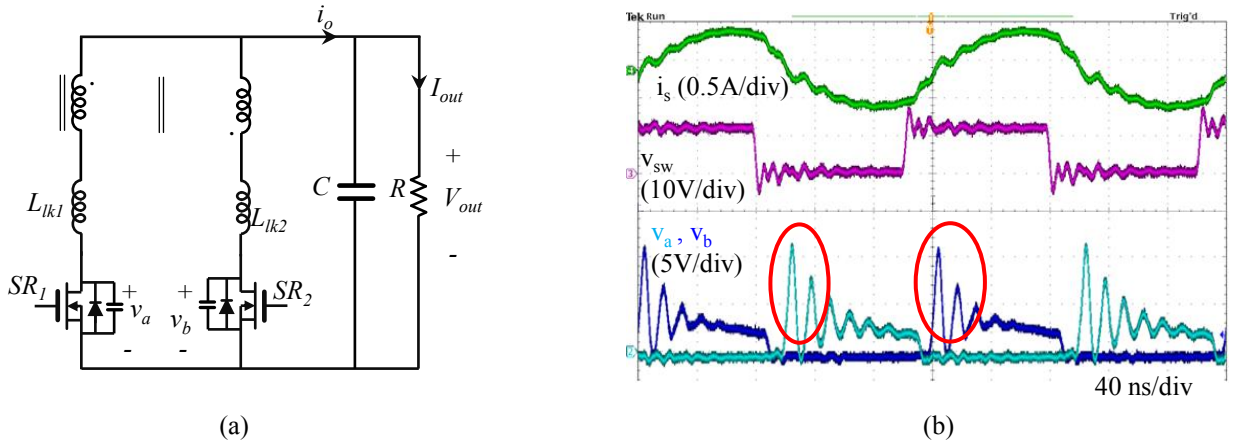


Figure 1.13: (a) Output side of the LLC resonant converter, including parasitic components, and (b) voltage ringing across the rectifier devices in a 12 V-to-1 V, 5 MHz LLC converter

A conventional full-bridge rectifier can effectively clamp the rectifier device voltage to the output voltage. However, an implementation with four rectifier devices means that conduction losses are doubled compared to the center-tap rectifier presented in this section. A simple clamping circuit is proposed in [53], but a later work points out that extra LC filter may be needed to meet a given output voltage ripple requirement [54]. The later work suggests a modified clamping circuitry,

but it requires a more complicated transformer design and rectifier driving scheme.

In summary, single- and multi-phase synchronous buck converter are the most popular POL topologies. However, they show limitations in high step-down-voltage, high current, high frequency applications because of low duty cycle and high switching losses. The LLC resonant converter is potentially a good candidate to address those limitations, thanks to its soft-switching capabilities and almost 50% duty cycle switching of all devices. Its disadvantage come from the secondary-side leakage inductance that causes voltage oscillation and higher stress to rectifier devices. Previously proposed clamping circuits are bulky and complicated.

1.3 Control Method Considerations

1.3.1 Existing Control Methods for Buck Converter

Control of single-phase and interleaved multi-phase synchronous buck converters is relatively simple. To improve transient responses, numerous methods have been pursued, and many are well supported by commercially available controller chips. In general, the output voltage can be regulated using either voltage-mode or current-mode control. In standard voltage-mode control, only the output voltage is sensed and the control variable is the switch duty cycle. In current-mode control, both the output voltage and the switch Q_1 (or inductor) current are sensed. In peak current-mode control, the control variable is the inductor peak current. In both control methods, small-signal modeling and controller design are straightforward and can be done analytically. However, because the control variable is updated at the switching frequency rate, the control bandwidth is limited. Furthermore, since the duty cycle cannot exceed 0 or 1, the large-signal response speed is limited, as shown in Fig. 1.6. Moreover, in multi-phase buck converters, there is a need to ensure equal sharing among the phases. Therefore, sensing of individual phase inductor currents is usually performed to achieve current sharing, to improve transient responses, and to implement overload protection features [28, 55–62].

Fig. 1.14 shows an example of current sharing control implemented in a two-phase buck

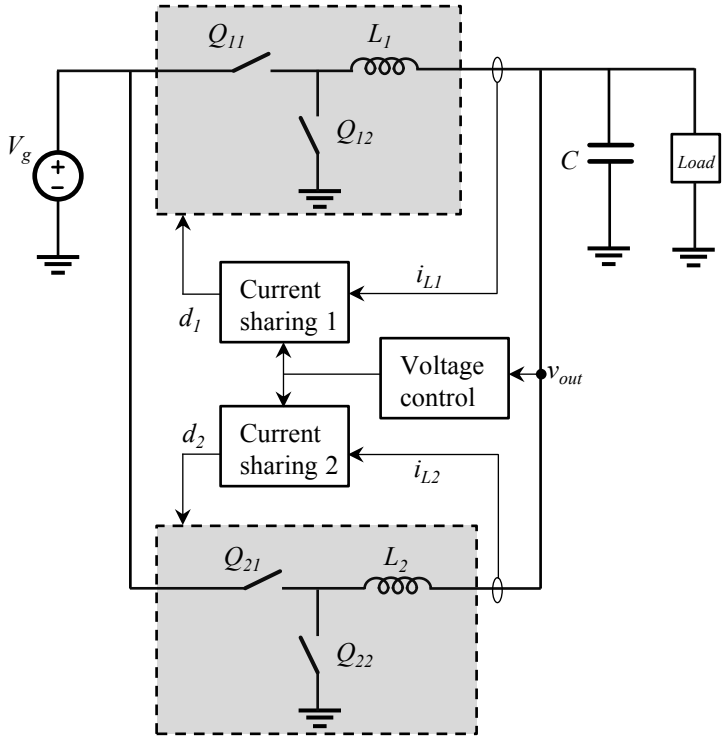


Figure 1.14: Example of current sharing control for interleaving multi-phase buck converter

converter. In addition to a voltage control block to regulate the output voltage, each phase has a current sharing control module to determine a proper duty cycle d_i, which compensates for any mismatches between the modules. In high-current applications, inductor current sensing adds cost and power losses.

1.3.2 Frequency Modulation of LLC Resonant Converter

Compared to multi-phase buck converter, current sharing among paralleled LLC converters is less susceptible to parasitic variations, but is still affected by resonant tank component mismatch [41–47]. The output voltage of LLC converter is regulated by voltage-mode control [63–65], or combined with current-mode control [66, 67]. Instead of pulse-width-modulation (PWM) method commonly employed in buck converters, the switching frequency is modulated while 50% duty cycle stays the same. A drawback is that the control-to-output transfer function varies with operating

point, and control design is generally more complicated. Another method, optimal trajectory control, is proposed for fast transient response [68], but the output current must be sensed, which is not favorable especially in POL applications.

1.3.3 Cell-Modulation-Regulated Architecture

In radio-frequency DC-DC power conversion applications, the approach of turning the number of modules (or phases) on or off has been proposed, not only to improve light load efficiency but also to facilitate output voltage regulation [4]. This cell-modulation-regulated approach is illustrated in Fig. 1.15.

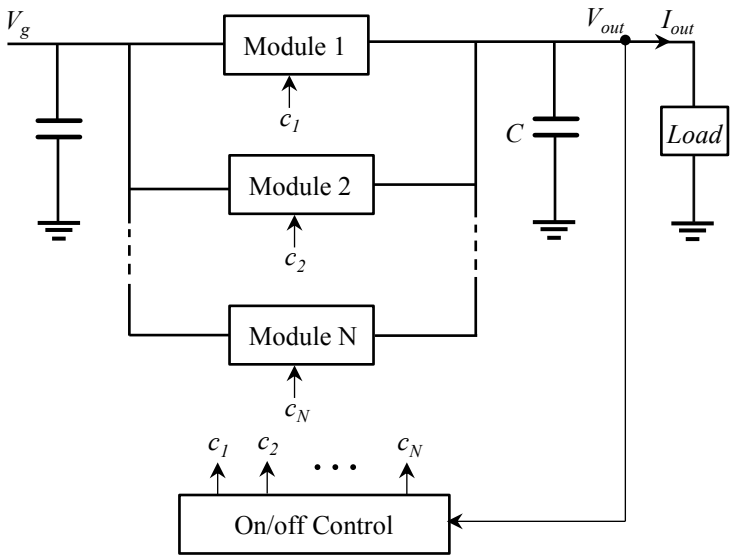


Figure 1.15: Cell-Modulation-Regulated Architecture [4]

Each module in the system is designed to operate at one operating point at its highest efficiency. In order to provide the required output power and to regulate the output voltage, the controller fully turns on a certain number of modules, while fine control is accomplished by turning one module on or off in a pulse-width-modulated (PWM) manner. For example, if each module can supply 1 A, at 2.5 A load current, the output voltage is regulated by fully turning on two modules, and turning on and off one module at 50% PWM duty cycle in order to provide the remaining

0.5 A current demand.

Such control method requires the converter modules to have quick turn-on/off feature and relatively high output impedance. This architecture has been verified by experiments using hysteretic control of one module [4, 69–74]. Fixed-frequency PWM with hysteretic override on one module is introduced by [75]. Their approach is to derive a first-order plant transfer function of the converter, then design a PI controller, using the PWM on/off duty cycle as control variable. However, this method is implemented on only one module, and extensions to multiple parallel modules is not considered. A sigma-delta modulator is suggested for multiple-module system control [4], but has not been studied in detail.

It should be noted that a similar approach has been pursued in POL applications [76–78] where an interleaved multi-phase buck converter is treated as a multi-level power digital to analog converter (DAC). In this case, each buck phase is equivalent to a voltage source in series with a low output impedance, leading to a second-order control-to-output transfer function of the system. Despite such effective and fast control methods, the converter choice implies limitations in future POL generations, as discussed in Section 1.2.1.3.

In summary, while the output voltage of a buck converter is regulated by pulse width modulation, LLC resonant converter is usually controlled by frequency modulation. The LLC converter's small-signal modeling and design process are more complicated. An alternative regulation method involves on/off control of multiple modules in parallel, each of which operates at one fixed operating point and at highest efficiency. This architecture has single-pole dynamics and shows promise in simple and effective controller design. Besides, it can result in good overall efficiency over wide load range.

1.4 Proposed Topology and Control Method

Fig. 1.16 shows the active clamp LLC resonant converter proposed in this thesis for POL applications [79]. The converter inherits advantages of the standard LLC resonant converter, including zero voltage switching (ZVS) of primary side MOSFETs, zero current switching (ZCS)

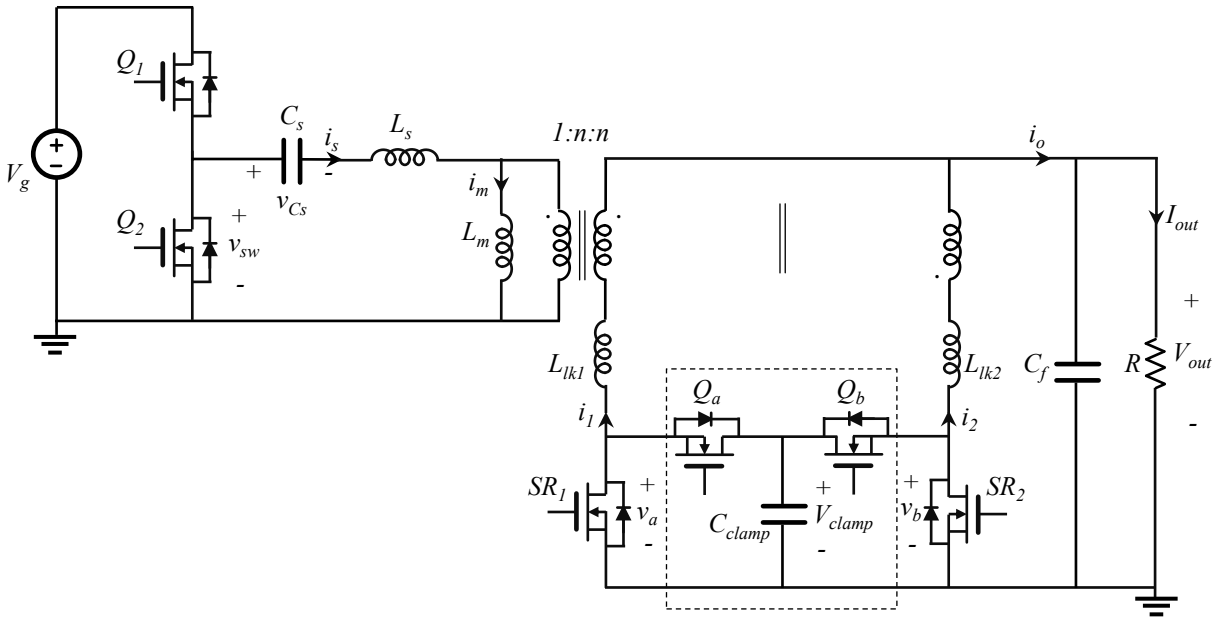


Figure 1.16: Active-clamp LLC resonant converter

of synchronous rectifier MOSFETs and 50% duty cycle operation of all switching devices. The active clamp addresses the voltage oscillation across the rectifier devices caused by transformer secondary-side leakage inductances and MOSFET output capacitances by clamping the voltage to approximately twice the output voltage. This modification also helps reduce the output capacitor current ripple.

The output voltage can be regulated by simple on/off control, and the converter is well suited for a multiple-parallel-module configuration [80]. The proposed on/off control method is a good candidate for POL applications because: (i) system modeling and compensator design are simple, (ii) current sensing is not required, (iii) it yields fast load-step transient response, and (iv) high frequency is maintained over wide load range.

The thesis is organized as follows. Chapter 2 explains operation and DC characteristics, and develops a design method for the active-clamp LLC resonant converter. Chapter 3 presents simulation and experimental results for on/off hysteretic control of one active-clamp LLC module. The on/off control of multi-module systems is investigated in Chapter 4. Chapter 5 demonstrates

design and testing results for a low-voltage custom CMOS IC that contains all secondary-side power devices and their gate drivers. Conclusions and future work directions are presented in Chapter 6.

Chapter 2

Active-Clamp LLC Resonant Converter

In this chapter, the active clamp LLC resonant converter is studied in detail. Section 2.1 explains the steady state operation of the converter. A simplified model is introduced in Section 2.2 to assist the converter analysis, which is performed by state-plane techniques and by the fundamental approximation in Section 2.3 and 2.4, respectively. Based on the analytical results, the converter properties are demonstrated in Section 2.5. After the converter operation and characteristics are analyzed, Section 2.6 presents design methods for the resonant tank elements and high-frequency magnetic components. Experimental results and loss analysis are shown in Section 2.7. The last section is the chapter summary.

2.1 Steady State Operation

Similar to the original LLC converter, the active clamp LLC converter always obtains zero-voltage switching (ZVS) on the primary side when the switching frequency is higher than the resonant frequency (above resonance). ZVS can also be obtained in some cases when the converter operates at a switching frequency lower than the resonant frequency (below resonance). The steady state operation of the converter in both operation regions are explained in this section.

2.1.1 Operation Above Resonance (AR)

Fig. 2.1 shows steady-state waveforms of input switching node voltage v_{sw}, primary side current i_s, voltage across resonant capacitor v_{C_s}, voltages across rectifier devices v_a and v_b, and

secondary-side currents i_1 and i_2. Three pairs of switches (Q_1, Q_2), (SR_1, Q_a) and (SR_2, Q_b) are

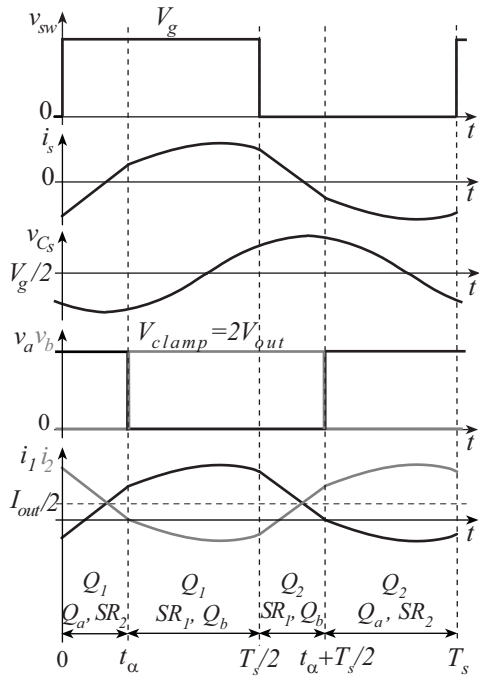


Figure 2.1: Typical steady-state waveforms of active clamp LLC converter in AR region

controlled by complimentary gate drive signals with dead times that are very short compared to switching period T_s. Therefore, the dead times are neglected in the waveforms shown in Fig. 2.1, and all devices are assumed to switch at 50% duty cycle.

The conduction paths during the first half of a switching cycle are highlighted in Fig. 2.2. During the first interval, Q_1, SR_2 and Q_a are on and capacitor C_{clamp} clamps v_a at twice the output voltage V_{out}. This interval ends at t_α, when SR_2 and Q_a are turned off and Q_b and SR_1 are turned on. Interval t_α can be found, as detailed in Sections 2.3 and 2.4, so that ZCS turning off of SR_2 and ZVS turning on of SR_1 and Q_b are obtained. During the second interval, voltage v_b across SR_2 is clamped at $2V_{out}$. This interval ends at $T_s/2$ when Q_1 is off and Q_2 is turned on at ZVS. The two remaining intervals are similar to the first two.

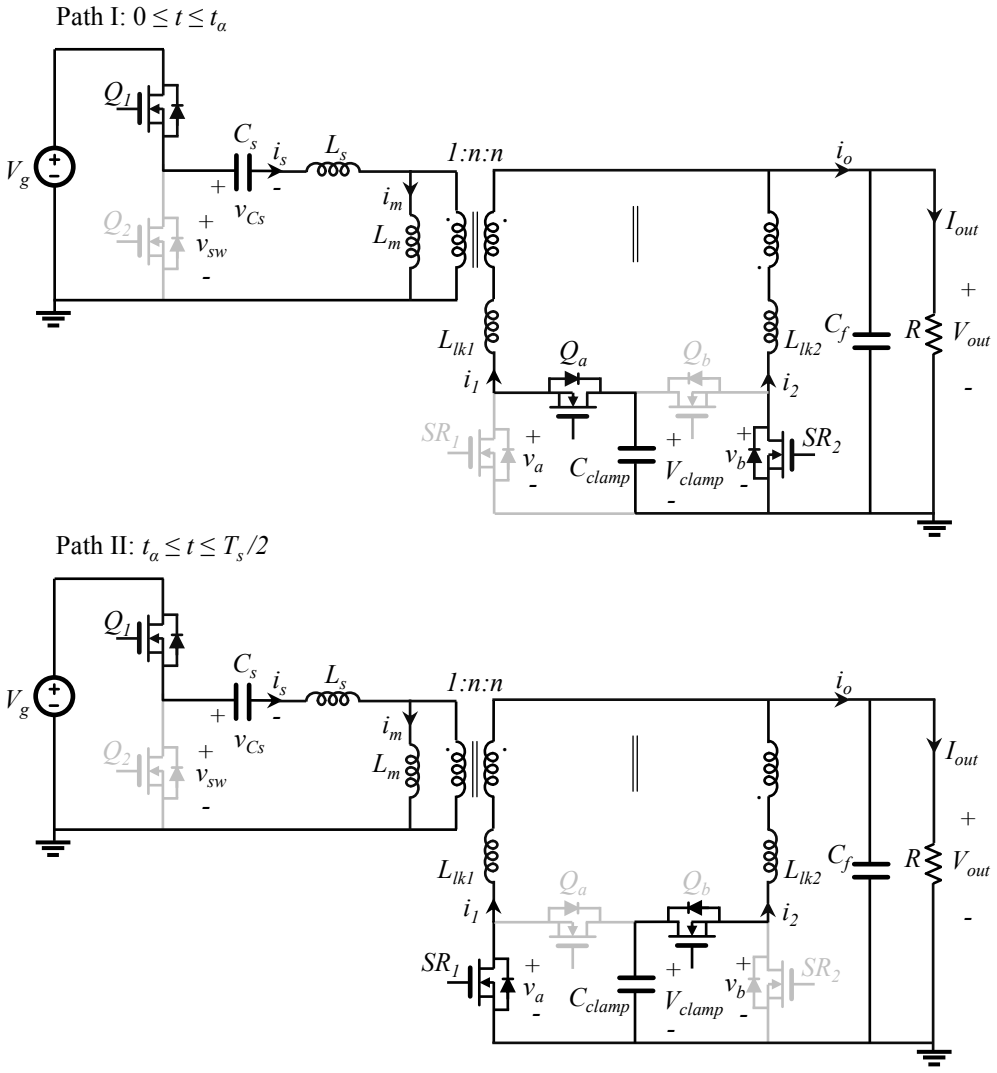


Figure 2.2: Conduction paths of active clamp LLC converter during the first half of a switching cycle. The converter operates in AR region.

As opposed to the standard LLC converter, the energy stored in leakage inductance L_{lk2} when SR_2 is turned off at t_α is not dissipated through oscillation, but is recycled by charging and discharging C_{clamp} via Q_b during one half of T_s. Similarly, the energy stored in leakage inductance L_{lk2} is recycled during the other half of T_s. In addition, since C_{clamp} allows secondary-side resonant currents to go through, there is significantly less current ripple on the output capacitor.

2.1.2 Operation Below Resonance (BR)

Fig. 2.3 shows steady-state waveforms of the active clamp LLC converter when it operates in the BR region with ZVS feature on the primary side.

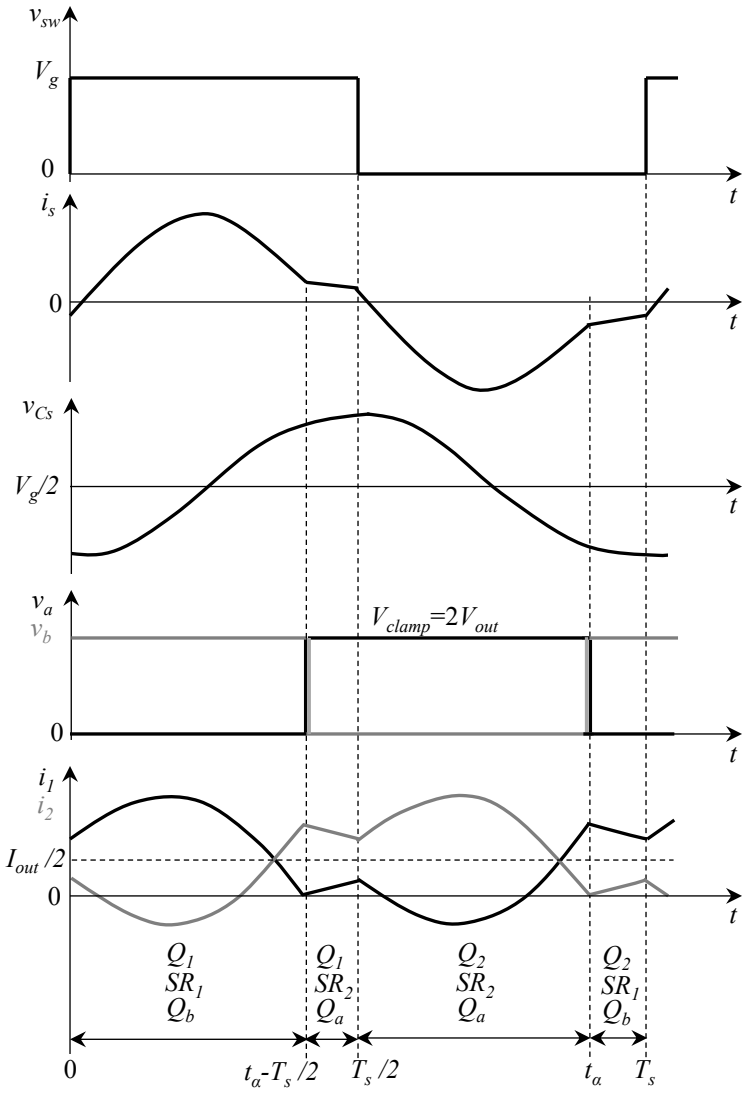


Figure 2.3: Typical steady-state waveforms of active clamp LLC converter in BR region with ZVS on primary side

In the first subinterval, Q_1, SR_1 and Q_b are on, and capacitor C_{clamp} clamps v_b at twice the output voltage V_{out}. This interval ends when SR_1 is turned off at zero current, along with Q_b turn-off. Interval 2 follows with SR_2 and Q_a are on and v_a is clamped at $2V_{out}$. At one half of the

switching cycle, this interval ends with Q_1 turned off and Q_2 turned on at ZVS. Compared to the AR operation, the conduction paths in the first two subintervals are swapped. Note that in this case the ZCS-turn-off moment of SR_2, t_α, occurs in the last half of the switching cycle, whereas in the AR region it happens in the first half of the switching cycle. This is explained further in Section 2.4.

2.2 Model Simplifications

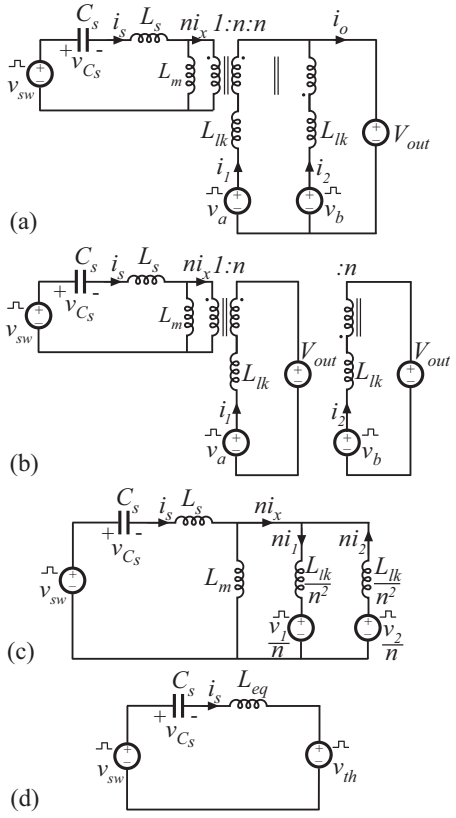


Figure 2.4: Steps to simplify converter model

It is important to derive a simple model of the active clamp LLC converter, to assist in the converter analysis. Fig. 2.4 illustrates steps taken to simplify the converter model. It is assumed that two secondary side windings are identical, $L_{lk1} = L_{lk2} = L_{lk}$, and that C_{clamp} and C_f are large enough so that voltage ripples across them can be neglected. First, in Fig. 2.4a, the converter is

simplified by replacing switches and capacitors by square wave voltage sources v_{sw}, v_a and v_b, and a constant voltage sink V_{out}, respectively. Fig. 2.4b shows the next step, in which two secondary sides are separated by splitting V_{out} between them [52], with the conditions

$$i_1 = 0.5(i_o + i_x) \tag{2.1a}$$

$$i_2 = 0.5(i_o - i_x). \tag{2.1b}$$

Note that the secondary side currents contain two components: i_x delivered from primary side and i_o, which is the sum of output capacitor C_f and load currents. Now the secondary sides are moved to primary side as in Fig. 2.4c, where $v_1 = V_{out} - v_a$ and $v_2 = v_b - V_{out}$. From this step, a relationship between i_s and i_x is found,

$$\frac{di_s}{dt} = nk\frac{di_x}{dt} + \frac{v_b - v_a}{2nL_m}\,, \tag{2.2}$$

where

$$k = 1 + \frac{L_{lk}/2n^2}{L_m}\,. \tag{2.3}$$

In the last step (Fig. 2.4d), the inductors and voltage sources are replaced by an equivalent circuit consisting of one inductor L_{eq} in series with a Thevenin equivalent square wave voltage sink v_{th} that lags v_{sw} by t_α, where

$$L_{eq} = L_s + \left[(L_{lk}/2n^2)//(L_m)\right]\,, \tag{2.4}$$

$$v_{th} = \frac{v_1 + v_2}{2nk} = \frac{v_b - v_a}{2nk}\,. \tag{2.5}$$

This model applies for both transient and steady state analysis as long as voltage ripples on v_{out} and v_{clamp} are small. In steady state, capacitor charge balance on C_{clamp} and C_f leads to:

$$\langle i_2\rangle_{t_\alpha \to t_\alpha + T_s/2} = 0\,, \qquad \langle i_o\rangle_{t_\alpha \to t_\alpha + T_s/2} = I_{out}\,, \tag{2.6}$$

and the relationship between i_s and i_x becomes:

$$i_s(t) = \begin{cases} nki_x(t) + \frac{V_{out}}{nL_m}\left[t - \left(t_\alpha + \frac{T_s}{4}\right)\right], & \text{if } t_\alpha \le t \le t_\alpha + \frac{T_s}{2} \\ nki_x(t) - \frac{V_{out}}{nL_m}\left[t - \left(t_\alpha + \frac{3T_s}{4}\right)\right], & \text{if } t_\alpha + \frac{T_s}{2} \le t \le t_\alpha + T_s. \end{cases} \tag{2.7}$$

2.3 State Plane Analysis

State plane analysis has been used to study complex operations of resonant converters [81–84]. It involves a graphical method that provides good insights into the resonant tank's behavior, and is a helpful tool to derive the converter's exact output characteristics. Section 2.3.1 introduces the state plane analysis for a basic LC resonant circuit. The method is applied to the active clamp LLC converter analysis in Section 2.3.2.

2.3.1 State Plane Analysis for a Basic LC Resonant Circuit

Fig. 2.5 shows an LC resonant circuit driven by a constant voltage source V_T and a constant current source I_T.

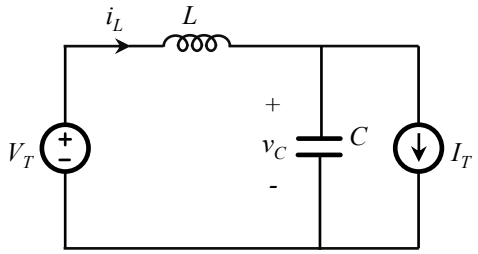


Figure 2.5: LC resonant circuit

This circuit has resonant frequency ω_0 and characteristic impedance R_0 that can be found as:

$$\omega_0 = \frac{1}{\sqrt{LC}} \qquad \text{and} \qquad R_0 = \sqrt{\frac{L}{C}}. \tag{2.8}$$

The state equations of this circuit are:

$$L\frac{di_L(t)}{dt} = V_T - v_c(t) \tag{2.9a}$$

$$C\frac{dv_C(t)}{dt} = i_L(t) - I_T, \tag{2.9b}$$

where the two states are capacitor voltage $v_C(t)$ and inductor current $i_L(t)$. Instead of solving the

differential equations directly, the state plane method first normalizes the variables [85],

$$m_C(t) = \frac{v_C(t)}{V_{base}} = \frac{v_C(t)}{V_T}, \tag{2.10a}$$

$$j_L(t) = \frac{i_L(t)}{I_{base}} = \frac{i_L(t)R_0}{V_T}. \tag{2.10b}$$

Define the angle corresponding to time t as $\theta = \omega_0 t$, and (2.9) becomes,

$$\frac{dj_L(\theta)}{d\theta} = 1 - m_c(\theta) \tag{2.11a}$$

$$\frac{dm_C(\theta)}{d\theta} = j_L(\theta) - J_T, \tag{2.11b}$$

with $J_T = I_T R_0 / V_T$. The solutions are of the form:

$$m_C(\theta) = 1 + A\cos(\theta + \theta_0), \tag{2.12a}$$

$$j_L(\theta) = J_T - A\sin(\theta + \theta_0). \tag{2.12b}$$

where A and θ_0 depend on the initial conditions $m_C(0)$ and $i_L(0)$. Fig. 2.6 shows the solution plotted in the normalized state plane, forming a circle of radius A and centered at $(1, J_T)$. The figure also demonstrates the time-domain solution $v_C(t)$ that is projected onto the normalized state plane. Starting from time zero, the capacitor voltage resonates around the dc solution V_T as t increases. Corresponding to that, the normalized state-plane trajectory starts at $\theta = 0$ and rotates counter-clockwise around its center as θ increases.

Using the trajectory's geometry, the normalized resonant amplitude, or radius A, and the initial phase angle θ_0 can be found,

$$A = \sqrt{(m_c(0) - 1)^2 + (j_L(0) - J_T)^2}, \tag{2.13}$$

$$\theta_0 = \arctan\frac{j_L(0) - J_T}{m_c(0) - 1}. \tag{2.14}$$

Finally, expressions for $i_L(t)$ and $v_C(t)$ can be easily derived from their normalized solutions in (2.12).

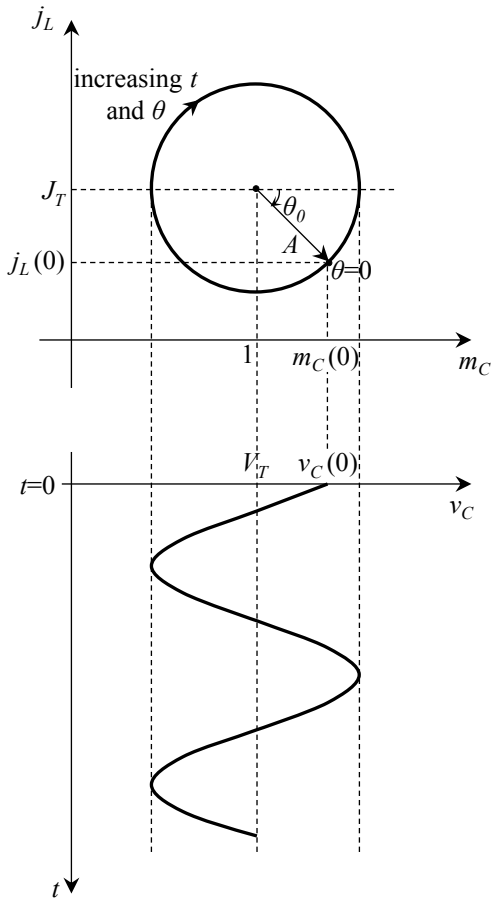


Figure 2.6: Normalized state-plane trajectory for the LC circuit in Fig. 2.5, along with the corresponding capacitor voltage waveform over time

2.3.2 State Plane Analysis for Active Clamp LLC Resonant Converter

The state-plane analysis presented in this section focuses on the steady-state operation of the active clamp LLC converter in both AR and BR regions. Notations of all the variables used in this section and their normalized values are summarized in Table 2.1.

Table 2.1: Notation of variables and their normalized values

Variable	Normalized variable	Explanation
f_s	F	switching frequency
V_{out}	M_{out}	output voltage
V_{out}/nk	$\bar{M}$	variable definition
I_{out}	J_{out}	output current
nkI_{out}	$\bar{J}$	variable definition
v_{eq}	m_{eq}	equivalent voltage in simplified model (Fig. 2.7)
v_{Cs}	m_{Cs}	absolute ac value of v_{Cs} at the beginning of subinterval 1
V_2	M_2	absolute ac value of v_{Cs} at the beginning of subinterval 2
i_s	j_s	resonant current on primary side
i_x	j_x	current transfered from primary to secondary side
I_1	J_1	absolute value of i_s at the beginning of subinterval 1
I_2	J_2	value of i_s at the beginning of subinterval 2
t_α	α	time (or angle) when SR_2 is turned off at ZCS, equal to duration of sub-interval 1 and 3 in AR operation
t_β	β	duration of sub-interval 2 and 4 in AR operation
t_γ	γ	duration of sub-interval 1 and 3 in BR operation
t_φ	φ	time lag between input switching node voltage v_{sw} and resonant current i_s

2.3.2.1 Above Resonance

The converter's simplified model in Fig. 2.4d is rearranged into an equivalent L_{eq}-C_s resonant circuit shown in Fig. 2.7, with the equivalent inductance L_{eq} found in (2.4). Fig. 2.7 also shows detailed waveforms with instantaneous values of the equivalent voltage v_{eq} that drives the resonant circuit, the inductor current i_s and capacitor voltage v_{Cs} over one switching cycle in steady state. This resonant circuit is similar to the one analyzed in Section 2.3.1, except for the drive voltage changing over four different subintervals. Note that because there is no current drive in this case, the resonant current i_s has no dc component. On the other hand, the voltage v_{Cs} resonates around a dc solution of $V_g/2$, which is the average value of the drive voltage v_{eq}.

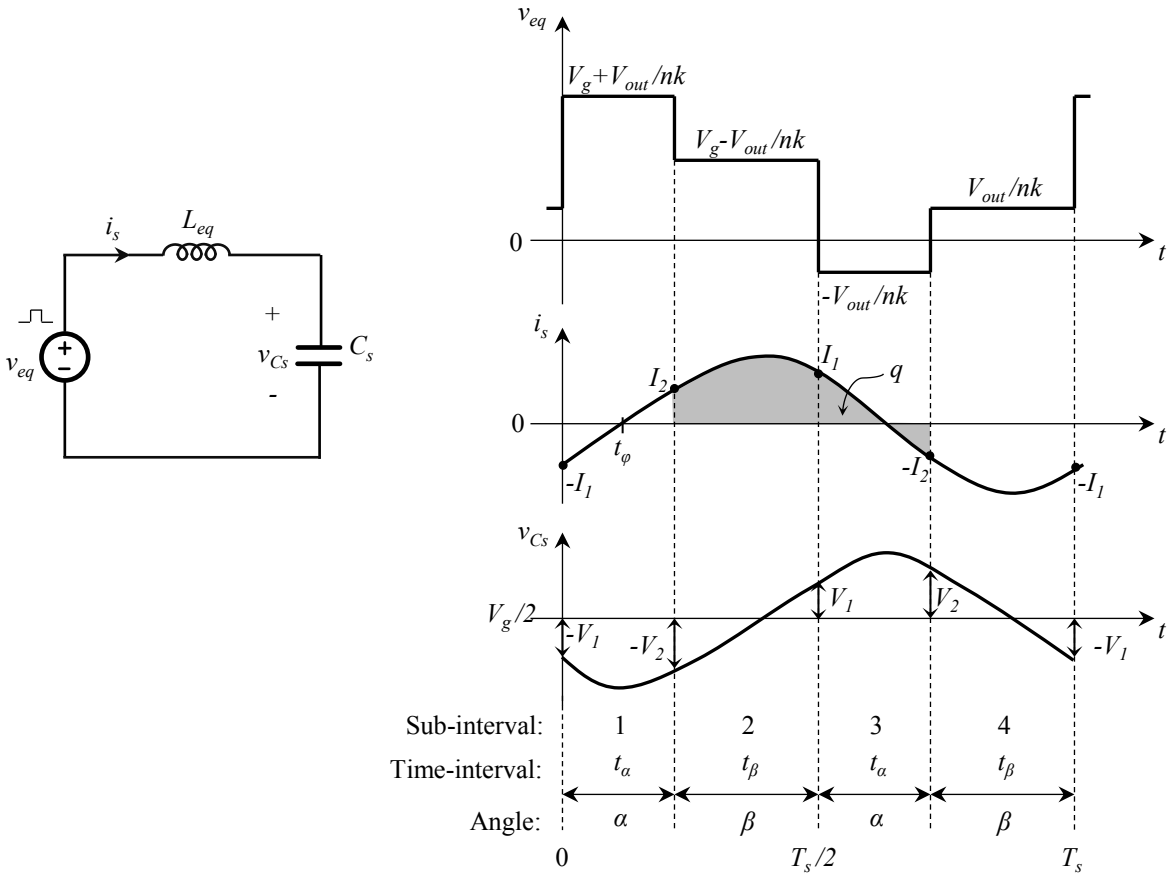


Figure 2.7: Active clamp LLC converter's equivalent circuit and detailed steady-state waveforms when the converter operates in AR region

For the active clamp LLC converter, the same method of Section 2.3.1 can be conveniently applied in four different sub-intervals in order to construct the normalized state-plane trajectory during one switching cycle. The first step is to normalize all the voltages, currents and switching frequency,

$$m = v/V_{base}, \qquad j = i/I_{base}, \qquad F = f_s/f_0, \tag{2.15}$$

where the base values are

$$V_{base} = V_g, \qquad I_{base} = V_{base}\sqrt{C_s/L_{eq}}, \qquad f_0 = \omega_0/2\pi = 1/2\pi\sqrt{L_{eq}C_s}. \tag{2.16}$$

In addition, the time intervals shown in Fig. 2.7 become angles, $\alpha = \omega_0 t_\alpha$ and $\beta = \omega_0 t_\beta$. Note that half of a switching cycle corresponds to an angle of π/F and the relationship between α and β is:

$$\alpha = \pi/F - \beta. \tag{2.17}$$

Since the output voltage is reflected to the primary side as discussed in Section 2.2, it is convenient to define two additional variables for normalized output voltage and current:

$$\bar{M} = M_{out}/nk, \qquad \bar{J} = nkJ_{out}, \tag{2.18}$$

where k is defined by (2.3).

Fig. 2.8 demonstrates how the state-plane trajectory is constructed, showing the relationship between normalized inductor current j_s and normalized capacitor voltage m_{C_s} in steady state. During the first sub-interval, the trajectory follows a circular arc centering at $(1 + \overline{M}, 0)$. It begins at $\theta = 0$ with the initial point $(0.5 - M_1, -J1)$, and ends at $\theta = \alpha$ with the second point $(0.5 - M_2, J_2)$. Starting at the end point of the first interval, the second interval trajectory rotates around a center at $(1 - \overline{M}, 0)$ until reaching the point $(0.5 + M_1, J_1)$ at one half of the switching cycle. In the last half, the remaining trajectory contains two arcs centering at $(-\overline{M}, 0)$ and $(\overline{M}, 0)$, respectively. All the four arcs form a closed trajectory in steady state as shown in Fig. 2.8d.

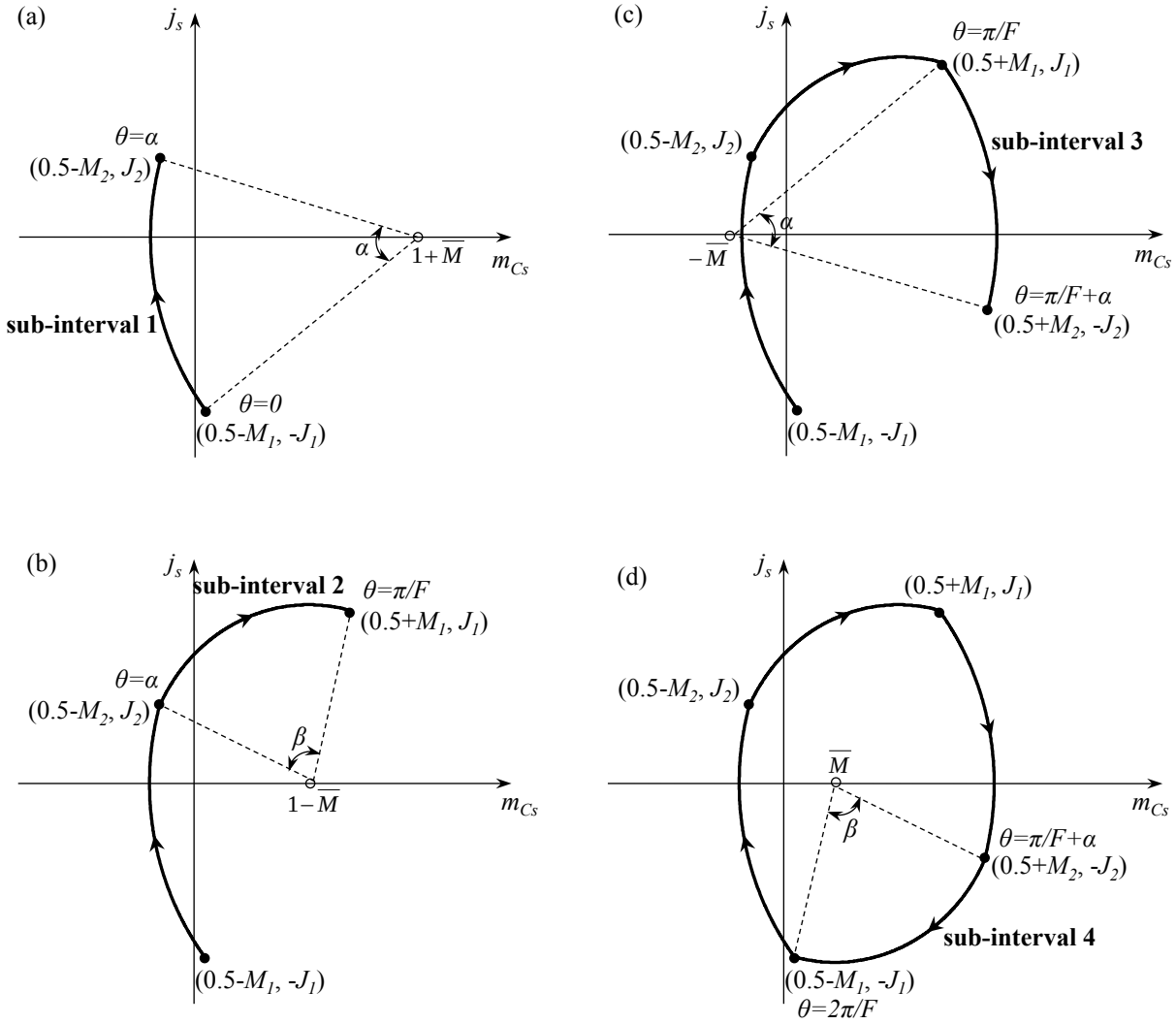


Figure 2.8: Steps to plot normalized steady-state inductor current j_s vs. capacitor voltage m_{C_s} on state plane. Converter operates at AR.

A set of equations are derived based on the geometry of the state-plane trajectory:

$$M_1 = 2M_2\overline{M} \tag{2.19a}$$

$$J_1^2 = J_2^2 + M_2(1+M_2)\left(1 - 4\overline{M}^2\right) \tag{2.19b}$$

$$\sin\left(\frac{\alpha}{2}\right) = \frac{1}{2}\sqrt{\frac{(J_1+J_2)^2 + (M_1-M_2)^2}{J_2^2 + (0.5+M_2+\overline{M})^2}} \tag{2.19c}$$

$$\sin\left(\frac{\pi}{2F} - \frac{\alpha}{2}\right) = \frac{1}{2}\sqrt{\frac{(J_1-J_2)^2 + (M_1+M_2)^2}{J_2^2 + (0.5+M_2-\overline{M})^2}} \tag{2.19d}$$

In order to obtain ZVS on the primary side, the resonant current at $\theta = 0$ has to be negative, which yields the ZVS condition:

$$J_1 > 0 \tag{2.20}$$

Note that the simplified LC equivalent circuit in Fig. 2.7 only assists the analysis of the input-side resonant current and voltage. The relationship between input and output-side currents from (2.1) and (2.7) should be included to fully model the converter's dc characteristics.

The next step is to derive another important equation using capacitor's charge arguments [85]. By averaging the currents in (2.1) and (2.7) from t_α to $t_\alpha + T_s/2$, and by applying the capacitor charge balance in (2.6), relationships between the resonant currents and the output current are found:

$$\langle i_x \rangle_{t_\alpha \to t_\alpha + T_s/2} = I_{out} \tag{2.21a}$$

$$\langle i_s \rangle_{t_\alpha \to t_\alpha + T_s/2} = nkI_{out}. \tag{2.21b}$$

The primary-side average current $\langle i_s \rangle_{t_\alpha \to t_\alpha + T_s/2}$ contributes to a total charge of the resonant capacitor C_s between t_α and $t_\alpha + T_s/2$:

$$q = \int_{t_\alpha}^{t_\alpha + T_s/2} i_s dt = 0.5T_s \langle i_s \rangle_{t_\alpha \to t_\alpha + T_s/2}. \tag{2.22}$$

This charge q is shown in Fig. 2.7 as the total area under the i_s curve. Besides, q relates to C_s's instantaneous voltages as follows,

$$q = C_s\left[v_{Cs}(t_\alpha + T_s/2) - v_{Cs}(t_\alpha)\right] = 2C_sV_2. \tag{2.23}$$

Combining (2.21b), (2.22) and (2.22) yields $V_2 = (nkI_{out}T_s)/(4C_s)$, and its normalized form is:

$$M_2 = \frac{\pi}{2F}\overline{J}. \tag{2.24}$$

The last step is to find the condition for ZCS on the secondary side. The synchronous rectifier SR_2 behaves like a diode if it is turned off at zero current when $t = t_\alpha$. Setting i_2 in (2.1) to zero results in $i_x(t_\alpha) = i_o(t_\alpha)$. Ideally, the clamp capacitor filters most of the ac component of the secondary-side resonant currents, and current i_o has insignificant ripple that can be neglected. Assume $i_o = I_{out}$ and combine with (2.7), ZCS turn-off on secondary side requires:

$$i_x(t_\alpha) = I_{out} \tag{2.25a}$$

$$i_s(t_\alpha) = nkI_{out} - \frac{T_s}{4nL_m}V_{out}. \tag{2.25b}$$

Given $i_s(t_\alpha) = I_2$, the normalized form of (2.25b) is:

$$J_2 = \bar{J} - \left(\frac{\pi}{2F}\right)\left(k\frac{L_{eq}}{L_m}\right)\bar{M}. \tag{2.26}$$

The set of equations (2.19), (2.20), (2.24) and (2.26) are solved numerically to find an exact solution for the converter dc output characteristics. Details for the output characteristics are presented in Section 2.5.1.

2.3.2.2 Below Resonance

The same procedure is applied to the converter steady state operation in the BR region. Fig. 2.9 shows current and voltage waveforms of the equivalent L_{eq}-C_s circuit, with details of the instantaneous values and subinterval durations. A new variable t_γ is introduced as the duration of subinterval 1 and 3. It relates to the time t_α when SR_2 is turned off at ZVS by: $t_\gamma = t_\alpha - T_s/2$, which has the normalized form of:

$$\gamma = \alpha - \frac{\pi}{F}. \tag{2.27}$$

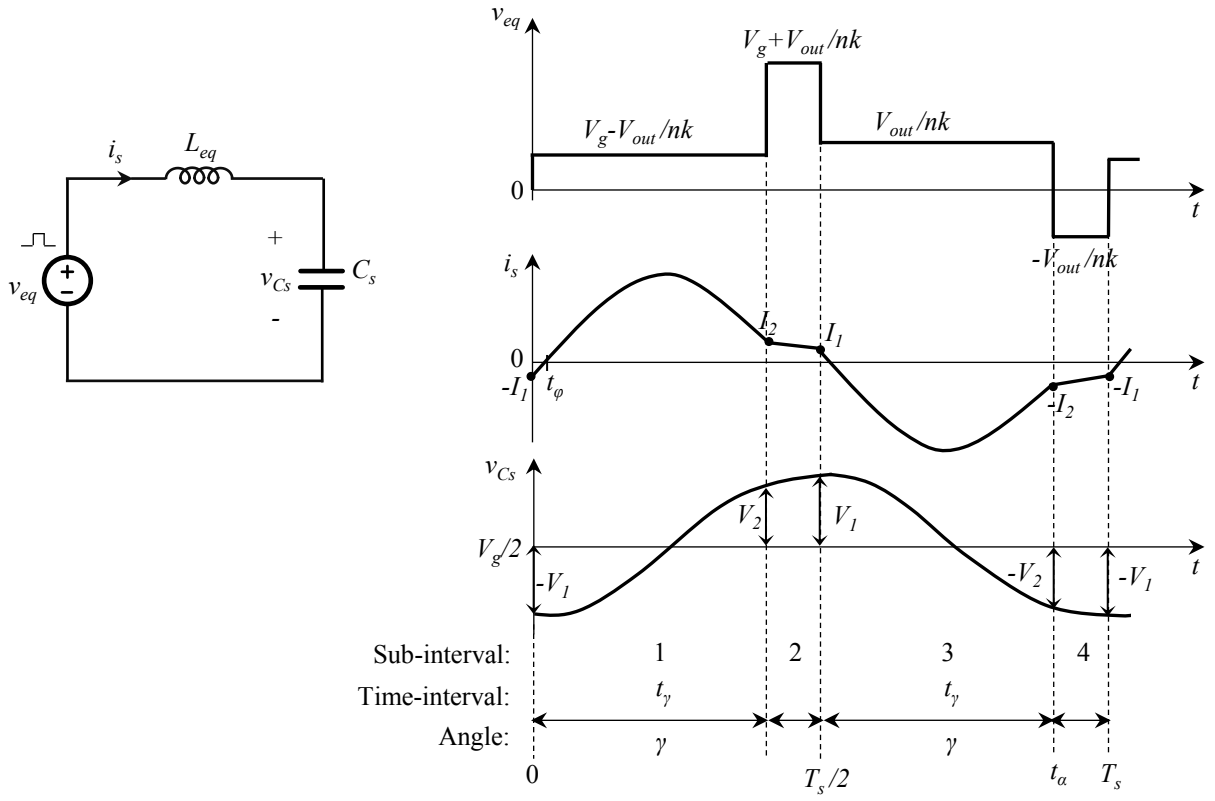


Figure 2.9: Active clamp LLC converter's equivalent circuit and detailed steady-state waveforms when the converter operates at BR with ZVS on primary side.

Following the same steps as in the AR operation, the state plane trajectory of normalized primary-side resonant current j_s and normalized capacitor voltage m_{Cs} is plotted in Fig. 2.10.

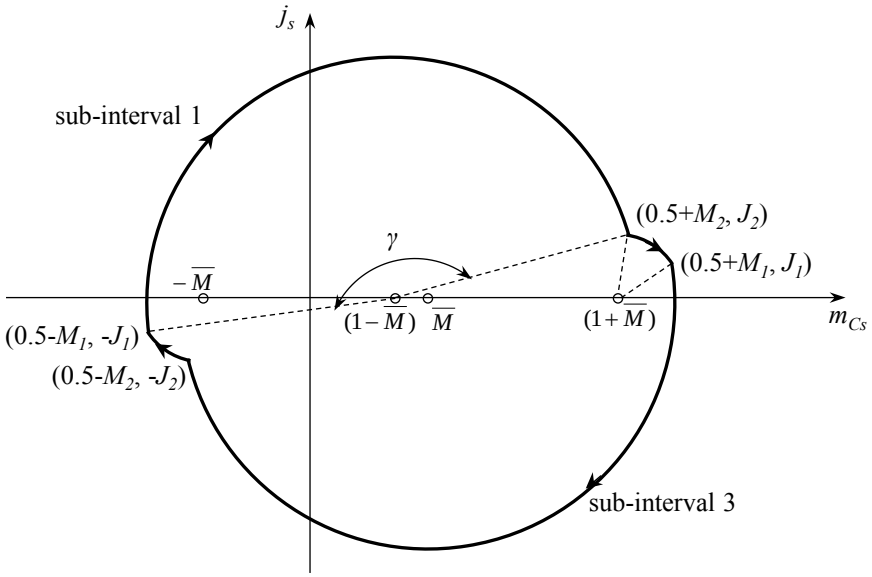


Figure 2.10: State plane trajectory of normalized resonant current j_s vs. normalized capacitor voltage m_{Cs} in BR operation

From the trajectory geometry, capacitor charge arguments, ZVS and ZCS conditions, a set of equations are derived for the BR steady-state operation:

$$J_1 \geq 0 \tag{2.28a}$$

$$J_2 = -\bar{J} + \left(\frac{\pi}{2F}\right)\left(k\frac{L_{eq}}{L_m}\right)\bar{M} \tag{2.28b}$$

$$M_2 = \frac{\pi}{2F}\bar{J} \tag{2.28c}$$

$$M_1 = 2M_2\overline{M} \tag{2.28d}$$

$$J_1^2 = J_2^2 - M_2(1-M_2)\left(1-4\overline{M}^2\right) \tag{2.28e}$$

$$\sin\left(\frac{\gamma}{2}\right) = \frac{1}{2}\sqrt{\frac{(J_1+J_2)^2+(M_1+M_2)^2}{J_2^2+(0.5-M_2-\overline{M})^2}} \tag{2.28f}$$

$$\sin\left(\frac{\pi}{2F}-\frac{\gamma}{2}\right) = \frac{1}{2}\sqrt{\frac{(J_1-J_2)^2+(M_1-M_2)^2}{J_2^2+(0.5-M_2+\overline{M})^2}}. \tag{2.28g}$$

2.4 Sinusoidal Approximation

As discussed in Section 2.3, state plane analysis is a useful tool to study the detailed behavior of a resonant converter during each switching cycle. However, because the exact output characteristics cannot be solved explicitly without computer aids, it limits the intuitive understanding of how circuit parameters affect the dc output voltage and current. This section applies the sinusoidal approximation, an alternative analytical method to help derive the dc solution explicitly.

In Fig. 2.11, the $L_{eq}-C_s$ equivalent circuit is excited by two square wave voltages v_{sw} and v_{th} that are phase shifted by $\omega_s t_\alpha$, where ω_s is the angular switching frequency. When the switching frequency f_s is close to the resonant frequency f_0, the LC tank resonates with approximately sinusoidal waveforms at frequency f_s. In this case, the two voltages can be approximated as their fundamental components [86–89]:

$$v_{sw}(t) \approx v_{sw1}(t) = \frac{2V_g}{\pi}\sin(\omega_s t), \tag{2.29a}$$

$$v_{th}(t) \approx v_{th1}(t) = \frac{4V_{out}}{\pi nk}\sin(\omega_s t - \omega_s t_\alpha). \tag{2.29b}$$

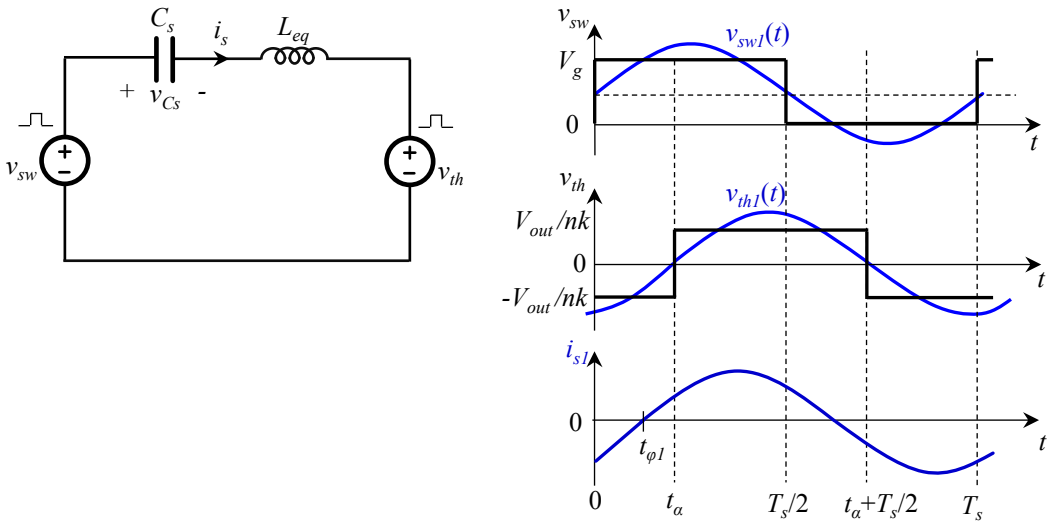


Figure 2.11: Demonstration of sinusoidal approximation for $L_{eq}-C_s$ equivalent circuit

From this point, the circuit can be analyzed using traditional phasor techniques [90]. In this technique, a sinusoidal function $x(t) = X\cos(\omega t + \phi)$ is represented by a phasor vector $\tilde{x}$ with magnitude X and angle ϕ. The relationship between the sinusoidal currents and voltages can be conveniently found using vector calculations.

By choosing the switching node voltage v_{sw} as the referenced zero-phase vector, the phasor diagram is plotted in Fig. 2.12 for v_{sw}, Thevenin voltage v_{th}, the equivalent voltage $v_{eq} = v_{sw} - v_{th}$, and primary-side current i_s, where the vector magnitudes V_{sw1}, V_{th1}, V_{eq1} and V_{s1} are their corresponding sinusoidal amplitudes.

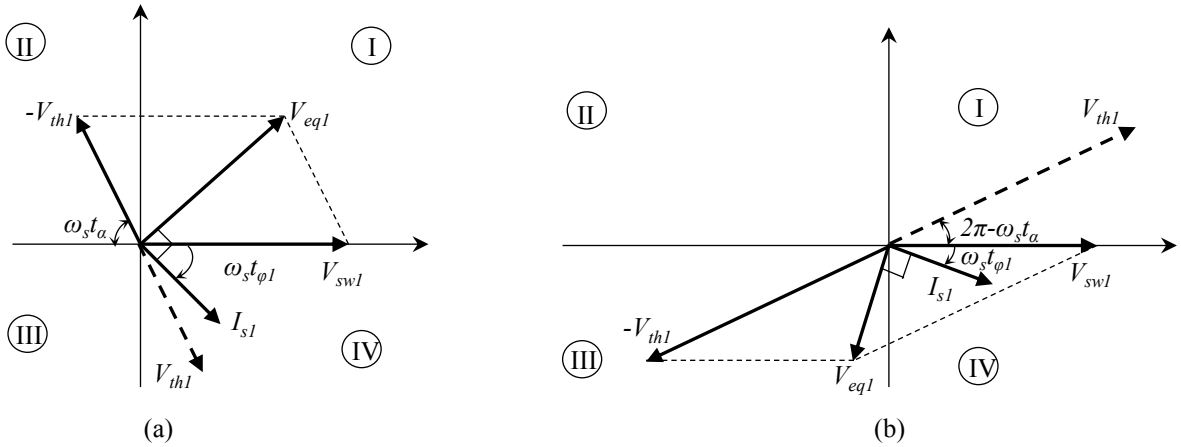


Figure 2.12: Phasor diagrams for: (a) AR operation and (b) BR operation

The total supply voltage v_{eq} and primary-side resonant current i_s are expressed in the angular notation as follows,

$$\tilde{v}_{eq} = \left(\frac{2V_g}{\pi}\right)\angle 0 - \left(\frac{4V_{out}}{\pi nk}\right)\angle -(\omega_s t_\alpha), \tag{2.30a}$$

$$\tilde{i}_s = \left(\frac{2V_g}{\pi Z}\right)\angle -\pi/2 - \left(\frac{4V_{out}}{\pi nkZ}\right)\angle -(\omega_s t_\alpha + \pi/2), \tag{2.30b}$$

where the impedance Z is:

$$Z = \omega_s L_{eq} - \frac{1}{\omega_s C_s}. \tag{2.31}$$

The calculations apply for both AR and BR operations. AR operation means the impedance is inductive ($Z > 0$) and i_s lags v_{eq} by $\pi/2$. The impedance becomes capacitive ($Z < 0$) in BR

operation and i_s leads v_{eq} by $\pi/2$. To obtain ZVS on the primary side, the resonant current i_s should lag the switching-node voltage v_{sw} by a phase of $\omega_s t_{\varphi 1}$. According to the diagram in Fig. 2.12, this requires the phasor vectors $\tilde{i}_{s1}$ to be located in the fourth quadrant, while $\tilde{v}_{eq1}$ is in quadrants I and III, for AR and BR operation, respectively. This means that an approximate ZVS condition can be found as:

$$\text{ZVS:} \begin{cases} V_g \geq \frac{2V_{out}}{nk}\cos(\omega_s t_\alpha) & \text{for AR} \\ V_g \leq \frac{2V_{out}}{nk}\cos(\omega_s t_\alpha) & \text{for BR} \end{cases} \tag{2.32}$$

Based on the calculation in (2.30b), the resonant current is expressed in time domain,

$$i_s(t) = \frac{2V_g}{\pi Z}\sin\left(\omega_s t - \frac{\pi}{2}\right) - \frac{4V_{out}}{\pi nkZ}\sin\left(\omega_s t - \omega_s t_\alpha - \frac{\pi}{2}\right) \tag{2.33}$$

By combining (2.33) with the relationship between the output current and average primary-side resonant current over one half of a switching cycle in (2.21b), the output current is found:

$$I_{out} = \frac{4V_g}{\pi^2 nkZ}\sin(\omega_s t_\alpha). \tag{2.34}$$

This is a useful formula to estimate the timing control parameter t_α in order to obtain a desired output current. It also explains why $0 \leq t_\alpha \leq T_s/2$ in AR region and $T_s/2 \leq t_\alpha \leq T_s$ in BR region. Furthermore, by applying the sinusoidal approximation of i_s in (2.33), the condition for ZCS on secondary in (2.25b) becomes:

$$\begin{aligned} \left(\frac{4}{\pi nkZ} + \frac{\pi}{2nZ_m}\right) V_{out} &= nkI_{out} + \frac{2V_g}{\pi Z}\cos(\omega_s t_\alpha) \\ &= \frac{4V_g}{\pi^2 Z}\left(\sin(\omega_s t_\alpha) + \frac{\pi}{2}\cos(\omega_s t_\alpha)\right), \end{aligned} \tag{2.35}$$

where $Z_m = \omega_s L_m$. The results in (2.34) and (2.35) provide an insight into how output current and voltage depend on the circuit parameters. Further derivations from the two equations proves that maximum power point (MPP) always occurs at:

$$\omega_s t_\alpha = \begin{cases} 61.2^\circ & \text{for AR} \\ 331.2^\circ & \text{for BR} \end{cases} \tag{2.36}$$

The fundamental analysis also helps to estimate the root-mean-square (RMS) currents of the converter. The primary-side RMS current can be easily derived from (2.33). On the secondary side, the current i_x transferred from primary side is approximated as a sinusoidal function:

$$i_x \approx I_{x1} sin(\omega_s t - \varphi_{x1}). \tag{2.37}$$

Applying this approximation to (2.21a) and (2.25a), the amplitude and phase of i_x are derived:

$$I_{x1} = \sqrt{1 + \frac{\pi^2}{4}} I_{out} = 1.86 I_{out}, \tag{2.38a}$$

$$\varphi_{x1} = \omega_s t_\alpha - \arcsin \frac{1}{\sqrt{1 + \frac{\pi^2}{4}}}. \tag{2.38b}$$

Consequently, the RMS currents on each secondary side, synchronous switch and clamp switch are found to be relatively low and linearly dependent on the output current:

$$I_{rms,sec} = 0.83 I_{out} \tag{2.39a}$$

$$I_{rms,SR} = 0.77 I_{out} \tag{2.39b}$$

$$I_{rms,Q_{a,b}} = 0.30 I_{out}. \tag{2.39c}$$

2.5 Converter Properties

This section studies the active clamp LLC resonant converter's properties in steady state, using the two methods developed in the previous sections - state plane analysis and sinusoidal approximation. To illustrate the converter properties, all the plots are generated using the following circuit parameters: 24 V input voltage, 11.6 nF resonant capacitor, 3.14 μH resonant inductance, transformer with turn ratio 5:2:2, 6.9 μH magnetizing inductance, and 320 nH leakage inductance on the secondary side. Section 2.5.1 analyzes the dc characteristics of the converter, given the rectifier devices behaving like ideal diodes and turning off at zero current. A comparison between the two analytical methods is also discussed. Section 2.5.2 demonstrates that the converter behaves approximately like a current source when it is not constrained by exact ZCS requirement on the secondary side.

2.5.1 Dc Characteristics

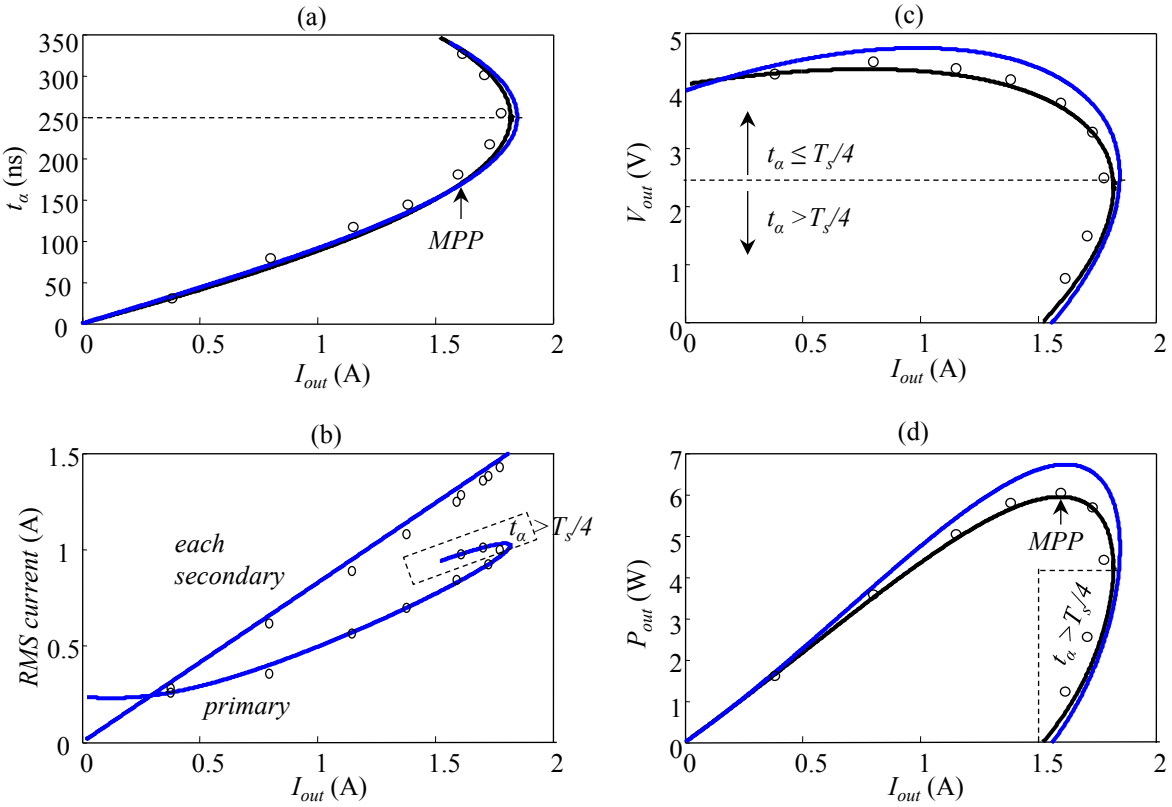


Figure 2.13: Prediction of (a) t_α, (b) RMS currents, and output characteristic for (c) output voltage vs. current, (d) output power vs. current, obtained by state plane analysis (black), sinusoidal approximation (blue) and experiment (circles)

Fig. 2.13 shows the converter output characteristic and prediction of t_α and RMS currents in AR operation (normalized frequency $F = 1.36$). With the aid of (2.34), one can see that depending on the control parameter t_α, the converter has the capability to generate up to an approximately maximum current of $(4V_g)/(\pi^2 nkZ)$. Corresponding to each output current within that range, there is a single solution for $t_\alpha \le T_s/4$. Although the solution for $t_\alpha \ge T_s/4$ exists, it is not preferred because of more circulating current on the primary side, resulting in a higher RMS current, as shown in Fig. 2.13b. In terms of the output characteristics, Fig. 2.13c shows that for each output current and its corresponding time control t_α, there is a unique output voltage to guarantee ZCS of synchronous switches SR_1 and SR_2, as predicted in (2.35). Based on the plot of output power

P_{out} vs. output current I_{out} in Fig. 2.13d, it is desired to operate the converter at $t_\alpha \leq T_s/4$ in order to obtain more possible output power, especially near the maximum power point (MPP).

Fig. 2.13 also compares the results obtained by sinusoidal approximation and state plane analysis. The derivation of output current in (2.34) involves averaging the approximated sinusoidal resonant current over half of a switching cycle. Over this time period, the average value of current harmonics at higher frequencies is zero, thus has insignificant effect on the average value of the fundamental component. This averaging process explains why the approximation method well predicts the relationship between the time control variable t_α and output current I_{out}. On the other hand, in finding the output voltage that meets ZCS requirement, the constraint in (2.25b) is applied for the instantaneous value of the resonant current's fundamental component at t_α. Due to effects of the resonant current's extra harmonics, this leads to a less accurate result compared to the state plane analysis. For example, at the MPP the sinusoidal approximation predicts the output voltage about 12% higher than the state plane analysis. However, it predicts t_α and I_{out} very well (within 3%), and is therefore useful in the design of resonant tank elements.

Fig. 2.14 shows the converter output characteristic at different normalized frequencies F in the AR operation region. The converter supplies more current when the switching frequency is closer to the resonant frequency, as predicted by the output current approximation in (2.34).

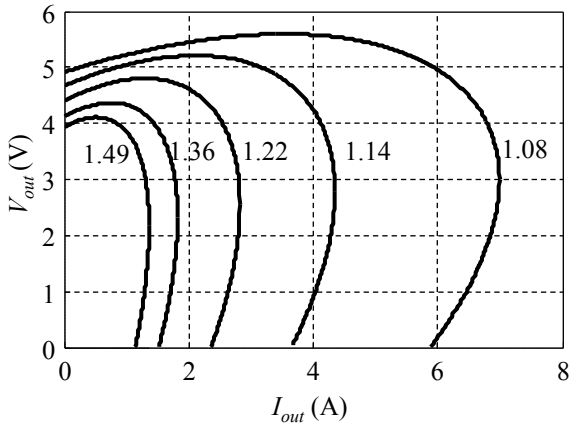


Figure 2.14: Prediction of active-clamp LLC converter's output characteristic at different normalized frequencies F

Moreover, at the same output current, the output voltage that guarantees ZCS condition for the rectifiers SR_1 and SR_2 is higher at a lower switching frequency.

2.5.2 Current Source Behavior

This section studies the converter behavior when the ZCS constraint is removed. In other words, the rectifier devices SR_1 and SR_2 do not need to turn off at zero current like ideal diodes. Calculations based on sinusoidal approximation suggest that the output current is a function of the input voltage, time control variable t_α and resonant circuit components, but is independent of the output voltage. The relationship between the output current and output voltage shown in Fig. 2.13c only applies when ZCS is required. Fig. 2.15 plots the output current at different output voltages while the input voltage and time variable t_α stay the same. The state plane method agrees with sinusoidal approximation about the output current's independence on output voltage. This means the active clamp LLC converter behaves similarly to a constant current source, which makes it suitable for the on/off control method in a multi-parallel-module system introduced in Section 1.3.3.

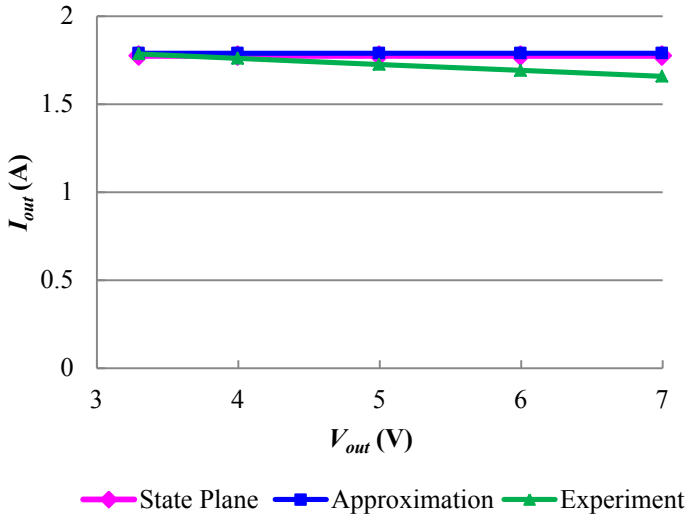


Figure 2.15: Output current vs. output voltage at the same $t_\alpha = 186$ ns

Although the converter can supply the same current at different output voltages, it is preferred to operate at the optimal output voltage that satisfies ZCS for a better efficiency. In the AR region, a lower output voltage causes the rectifier devices to turn off at a positive current, resulting in losses associated with body diode reverse recovery. Operating at an output voltage higher than the optimal value results in higher RMS currents, as shown in Fig. 2.16, which causes higher conduction losses.

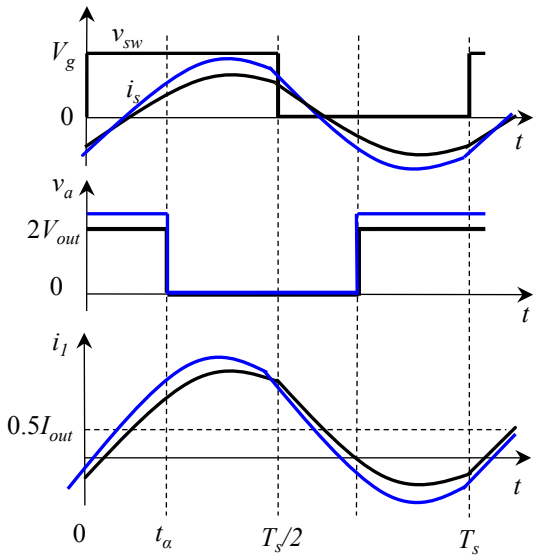


Figure 2.16: Converter waveforms at the optimal output voltage satisfying ZCS (black), and at a higher output voltage causing the rectifier devices to turn off at negative current (blue)

2.6 Converter Design

After the analytical methods are developed and the converter characteristics are analyzed, the next step is to design the converter. Section 2.6.1 explains how to select the resonant tank elements, given certain power and voltage requirements. The magnetics design considerations are presented in Section 2.6.2.

2.6.1 Resonant Tank Elements

The design specifications include input voltage V_g, output voltage V_{out}, output current I_{out} and switching frequency f_s. Using sinusoidal approximation at MPP in the AR operation, the values of n, k, and F need to be chosen in order to find the tank elements. Recall that n is the transformer turn ratio in the form $1:n$ and the two parameters k and F are defined as:

$$k = 1 + \frac{L_{lk}}{2n^2 L_m},$$

$$F = 2\pi f_s \sqrt{L_{eq} C_s},$$

where $L_{eq} = L_s + \left[\left(L_{lk}/2n^2\right) //L_m\right]$. The design approach is summarized in Table 2.2.

Table 2.2: Tank element design steps

Step	To do	Equations	Note
1	Choose n and k	$L_m = \left[\frac{V_g}{f_s I_{out}}\right] / \left[7.45n\left(nk\frac{V_g}{V_{out}} - 1.92\right)\right]$ $L_{lk} = 2n^2 L_m(k-1)$ $I_{s,rms}^2 = 1.61 I_{out}^2 \left(nk - 0.96\frac{V_{out}}{V_g}\right)^2 + \frac{\pi^2}{2}\left(\frac{I_{out}V_{out}}{V_g}\right)^2$	$nk \geq 1.92 V_{out}/V_g$ Higher $nk \rightarrow$ higher $I_{s,rms}$
2	Choose F	$C_s = 0.45nk\left(F^2-1\right)\frac{I_{out}}{f_s V_g}$ $L_s = \frac{F^2}{4\pi^2 f_s^2 C_s} - \left[\left(L_{lk}/2n^2\right) //L_m\right]$	Increase $F \rightarrow$ increase C_s and decrease L_s

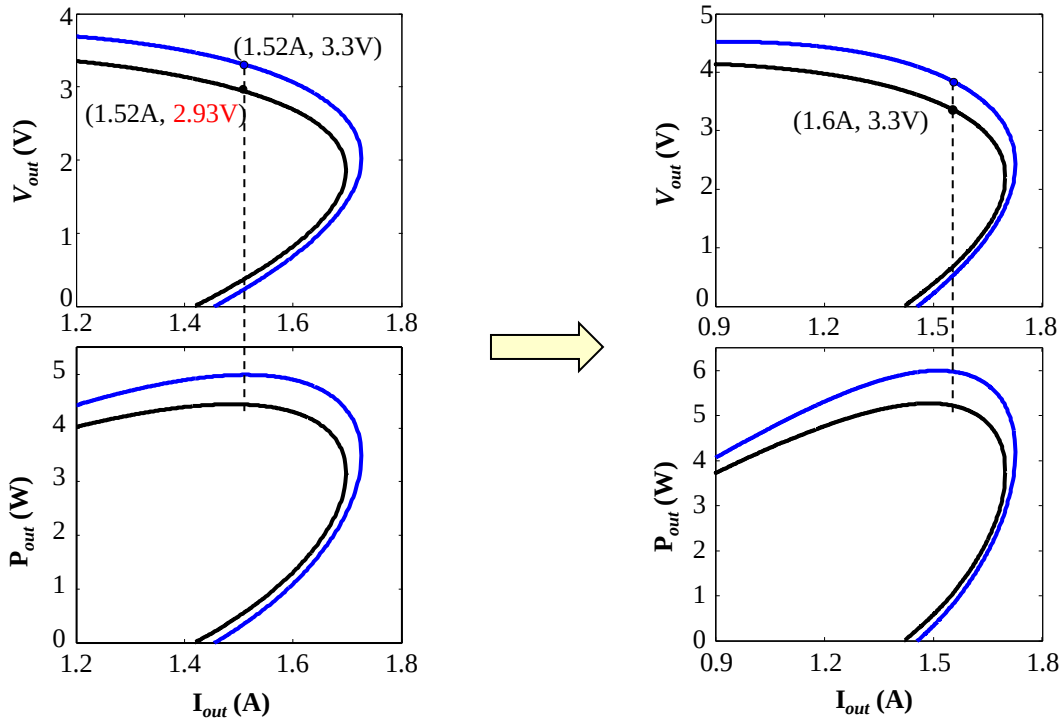
As an example, for a module operating near MPP with $V_g = 24$ V, $V_{out} = 3.3$ V, $I_{out} = 1.52$ A and $f_s = 1$ MHz, one practical design option is as follows:

- Step 1: Choose $n = 0.4$ and $k = 1.15$ to satisfy the condition $nk \geq 0.275$, which then gives $L_m = 3.7$ μH and $L_{lk} = 180$ nH. Note that a higher value of nk means a higher primary-side RMS current $I_{s,rms}$. However, if a significant leakage inductance on transformer's secondary side is expected, an nk value has to be large enough to obtain such leakage inductance.

- Step 2: Choose $F = 1.4$, which then results in $C_s = 12.5$ nF and $L_s = 3.5$ μH. Note that increasing F increases C_s and decreases L_s.

- Step 3 - verification: With the calculated parameters, state plane analysis shows that MPP occurs at 1.52 A and 2.93 V output. The output voltage is somewhat away from the target value. Therefore, steps 1 and 2 are redone with V_{out} set about 12% higher in the expressions obtained based on sinusoidal approximation.

Finally, the tank elements are chosen to be: $L_m = 6.2$ μH, $L_{lk} = 300$ nH, $L_s = 3.2$ μH and $C_s = 12.5$ nF, resulting in (3.3 V, 1.6 A) operating point near MPP. The verification steps for the first reiteration and the final design are demonstrated in Fig. 2.17.



(a) First iteration

(b) Final iteration

Figure 2.17: Verification step in selecting tank elements: (a) first iteration and (b) final design. State plane analysis is shown in black and sinusoidal approximation is in blue.

2.6.2 Magnetic Components

2.6.2.1 High-frequency Magnetics Design Considerations

The procedures to design inductors and transformers using solid wires have been well developed with details explained in [5]. For high-frequency magnetics, one needs to pay additional attentions to: (i) ac copper loss caused by skin and proximity effects, and (ii) core loss associated with non-sinusoidal excitation. The considerations for high-frequency magnetics design are discussed as follows.

Review of Ac Copper Loss: At low frequency, the copper loss in a winding is mainly caused by its dc resistance. When the frequency increases, additional loss occurs because of two mechanisms related to eddy currents in the conductor: skin effect and proximity effect [5,91]. These effects are illustrated in Fig. 2.18.

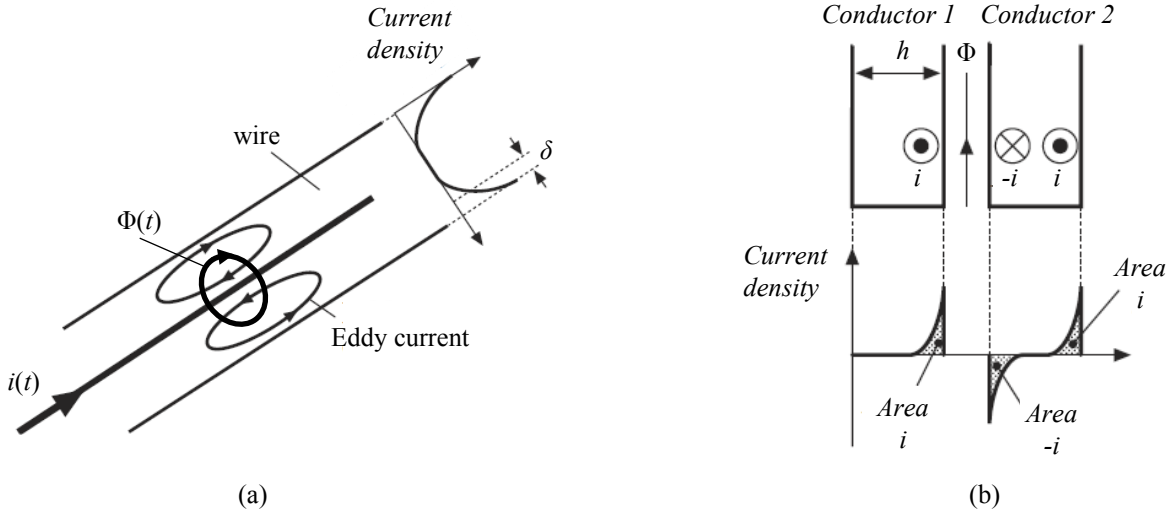


Figure 2.18: (a) Skin effect and (b) proximity effect in two adjacent copper foil conductors [5]

As shown in Fig. 2.18a, when a sinusoidal current $i(t)$ flows through a solid conductor, it induces an ac flux $\Phi(t)$, which in turn induces eddy currents flowing in a direction that tends to oppose the flux change. Because of the eddy currents, current density ρ is unevenly distributed: starting very small inside the conductor, and increasing exponentially when it comes closer to the

conductor surface. This exponential function has a characteristic length δ defined as the penetration depth or skin depth:

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}}, \tag{2.40}$$

where f is the frequency of the sinusoidal current, the permeability μ of copper is equal to $\mu_0 = 4\pi \times 10^{-7}$ H/m, and the resistivity ρ of copper is 2.3×10^{-6} Ω.cm at 100° C. At high frequency, the skin effect causes the current to concentrate near the surface of a large wire, therefore increases the wire resistance and the total copper loss.

In a multi-layer winding, a conductor's ac current can induce additional currents in an adjacent conductor. This mechanism is called proximity effect, causing uneven current distribution in large conductors, which consequently generates extra copper loss. A simple example is demonstrated in Fig. 2.18b. Two copper foil conductors are placed close to each other - one carries a high frequency ac current and the other is open circuit. The ac current i in conductor 1 induces an ac flux $\Phi(t)$ that attempts to penetrate into inductor 2. A current is induced on the left side of conductor 2 to oppose against this flux change. If the flux penetration depth is much smaller than the foil width h, this induced current has a value of $-i$. Because the total current in conductor 2 is zero, a current of $+i$ must exist on the other side of the foil. For more complicated winding structures, the proximity loss can be analyzed using the finite element method, which is available in softwares such as Finite Element Method Magnetics (FEMM) [92].

Wire Selection: The skin effect has to be considered when determining the wire size, especially for the active clamp LLC converter prototype operating at relatively high frequency (e.g. 1 MHz or above). At 1 MHz, the ratio between the skin depth at 100°C and a round wire's diameter is very small for AWG#18: $\delta/d = 0.07$. This ratio becomes more reasonable for AWG#46: $\delta/d = 1.9$. There are two possible wire options to minimize the skin effect: (i) Litz wire containing multiple insulated thin strands that are twisted or woven together, and (ii) thin PCB copper traces for planar magnetics. The Litz wire design is generally complicated because it includes the calculation of proximity loss among the strands, which may overcome the benefits

of skin effect reduction obtained by using smaller wire strands [93, 94]. In the scope of this work, the traditional magnetics design process is used to determine the size of a solid wire, taking into account more winding space for insulation. The number of Litz wire strands is then calculated to obtain an equivalent conduction area. The proximity effect in both Litz wire and PCB trace windings is evaluated by FEMM to verify that the total copper loss is within a practical value [92].

Review of Core Loss: When a sinusoidal current flows in a magnetic component's winding, the core loss per volume can be calculated by [95]:

$$P_v = kf^{\alpha}(\Delta B)^{\beta}, \tag{2.41}$$

where f is the sinusoidal excitation frequency, ΔB is the peak flux density, k, α and β are the parameters associated with the core material. These parameters are extracted by curve-fitting (2.41), usually called Steinmetz equation, to the manufacturer's core loss data. Given a periodical voltage $v_1(t)$ across a transformer or inductor winding of n_1 turns, the peak ac flux is:

$$\Delta B = \frac{\int_{\text{positive } v_1} v_1(t)dt}{2n_1 A_c}, \tag{2.42}$$

where A_c is the core cross-sectional area, and the integration is applied during the positive portion of the voltage. In the active clamp LLC converter, the voltages across the resonant inductor and the transformer primary-side are non-sinusoidal as illustrated in Fig. 2.19. A different approach is needed to calculate the core loss in this case.

A modification is suggested by introducing the term dB/dt to the original Steinmetz equation [96]. However, a continuous change of parameters in the flux density waveform results in a discontinuous change in the loss function, which is undesirable. This is also related to a mismatch between this modified Steinmetz equation (MSE) and measured data [97]. A different method - generalized Steinmetz equation (GSE) is developed by assuming that the core loss is a function of both dB/dt and the instantaneous value of the flux density $B(t)$. The limitation of this approach is that it oversimplifies the time-history of the flux waveform's effect to the core loss. To address

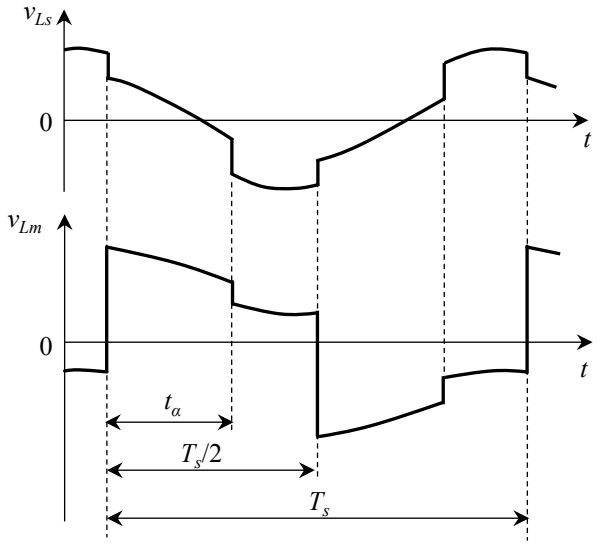


Figure 2.19: Waveforms of voltage v_{Ls} across resonant inductance and voltage v_{Lm} across transformer primary side when the converter operates in AR

this limitation, the improve GSE (iGSE) or natural Steinmetz equation (NSE) is proposed [98, 99]:

$$P_v = (\Delta B)^{\beta-\alpha} \frac{k_N}{T} \int_0^T \left| \frac{dB}{dt} \right|^\alpha dt, \tag{2.43}$$

where T is the operating period, and the coefficient k_N is chosen to make this equation consistent with the the Steinmetz equation:

$$k_N = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^\alpha d\theta}. \tag{2.44}$$

This approach is proved to be more accurate than the MSE or GSE. For the active clamp LLC converter, the core losses of both resonant inductor and transformer is calculated based on the iGSE:

$$P_v = \frac{k_N}{(4f_s)^{\beta-\alpha}(n_1 A_c)^\beta} \left(|v_1|_{avg}\right)^{\beta-\alpha} \left(|v_1|^\alpha\right)_{avg}, \tag{2.45}$$

where n_1 is the number of turn and v_1 is the voltage across a winding. The average values over one switching period of $|v_1|$ and $|v_1|^\alpha$ can be obtained conveniently by circuit simulation tools like Spice. Note that the core loss is reduced by increasing the number of turns, at the cost of increased copper loss.

Core Selection: The L material from Magnetics Inc is chosen for its low core loss and optimum frequency range from 0.5 to 3 MHz. Table 2.3 lists the material parameters useful for the magnetics design.

Table 2.3: Parameters of L material

Property	Symbol	Condition	Value
Initial permeability	μ_i	25°C; ≤10 kHz; ≤0.5 mT	900±25%
Maximum flux density	B_{max}	100°C	370 mT
Coefficients for Steinmetz equation		1-3 MHz	
	α		3.00
	β		2.24
	k		4.54×10^{-10}

Corresponding to the wire selection, two different cores are chosen for both inductor and transformer designs: (i) PQ20/20 core for Litz-wire winding, and (ii) EE1805 core for planar magnetics. The core parameters can be found in Table 2.4. Two active clamp LLC prototypes are built based on these two magnetics options, and the design details are described in the following sections.

Table 2.4: Core parameters

Core	PQ20/20	EE1805
Winding area (mm^2)	38.4	20
Cross sectional area (mm^2)	62.6	40.1
Magnetic path length (mm)	45.7	24.2
Core volume (mm^3)	2850	972

2.6.2.2 Inductor Design

As discussed in the previous section, there is a trade-off between copper and core loss. Increasing the number of turns helps reduce the core loss but adds extra conductor length, which

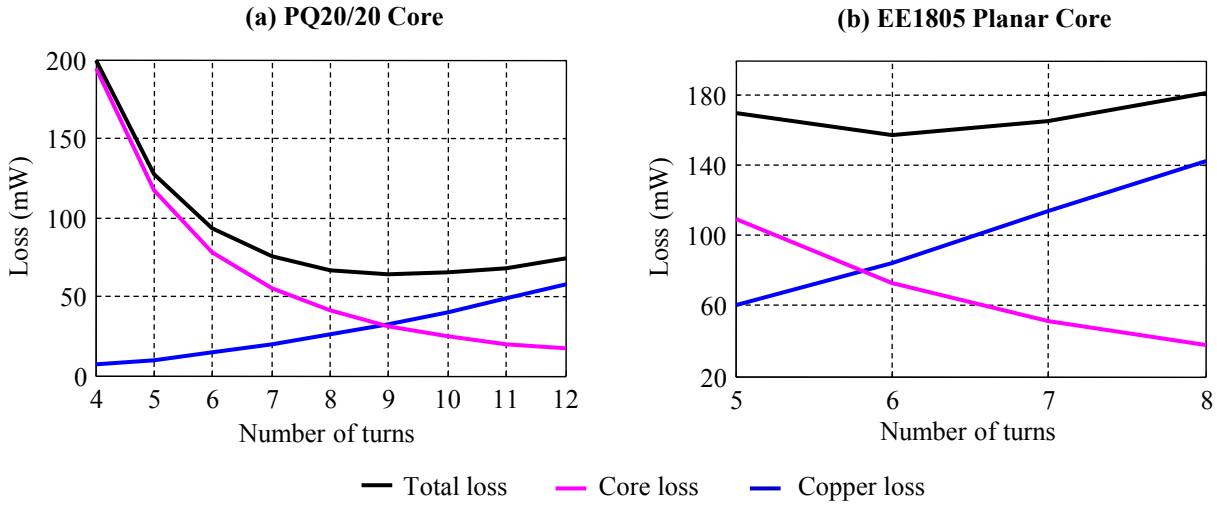


Figure 2.20: Inductor loss vs. number of turns, using (a) PQ20/20 core and (b) EE1805 planar core

causes more copper loss. Fig. 2.20 plots the core loss, dc and ac copper loss, and total magnetics loss at different number of turns for both PQ20/20 core and EE1805 planar core. For each case, the optimum number of turns is chosen to obtain the minimum total loss. Note that a smaller core results in a larger magnetics loss. The comparison between two designs using these cores is discussed further in Section 2.7. The winding configurations for both inductor designs are described in Table. 2.5.

Table 2.5: Two inductor designs using PQ and planar EE cores

Core	PQ20/20	EE1805
Wire	Litz wire,	PCB traces,
	450 AWG#46 trands	four 1-Oz Cu layers
Number of turns	8	6
Air gap[1] (mm)	1.81	0.31
Inductance (μH)	3.04	3.80

[1] The gap inserted in the middle of each core leg

The layer arrangement and PCB layouts for the planar inductor are included in Appendix A.

Although a maximum of eight copper layers is available, only four most outer layers are utilized to reduce copper loss caused by the fringing flux around the air gap [100–102]. This loss mechanism is demonstrated in Fig. 2.21 and is explained as follows. When there is no air gap, the magnetic flux is enclosed within the core volume. In order to obtain a lower desired inductance, an air gap is inserted in between two halves of the core. Around the air gap region, however, the magnetic flux finds a lower reluctance path to flow and some of the magnetic flux lines expand further into the winding window, as illustrated in Fig. 2.21. In this figure, each layer contains six turns of windings, and eight of them are connected in parallel. At a low frequency, paralleling more layers reduces the total dc resistance, thus helps reduce the dc copper loss. However, at a high frequency the fringing flux induces eddy currents in the conductors nearby. This causes significantly higher current density in those conductors compared to the other ones, resulting in a higher total copper loss. As an example, if the four middle layers were used in the planar inductor designed in this section, the total copper loss would increase by 54 mW, or 63%. This is well-known for planar magnetics, where the core's height is smaller than other core geometries, and copper loss related to fringing flux is more sensitive to the air gap length.

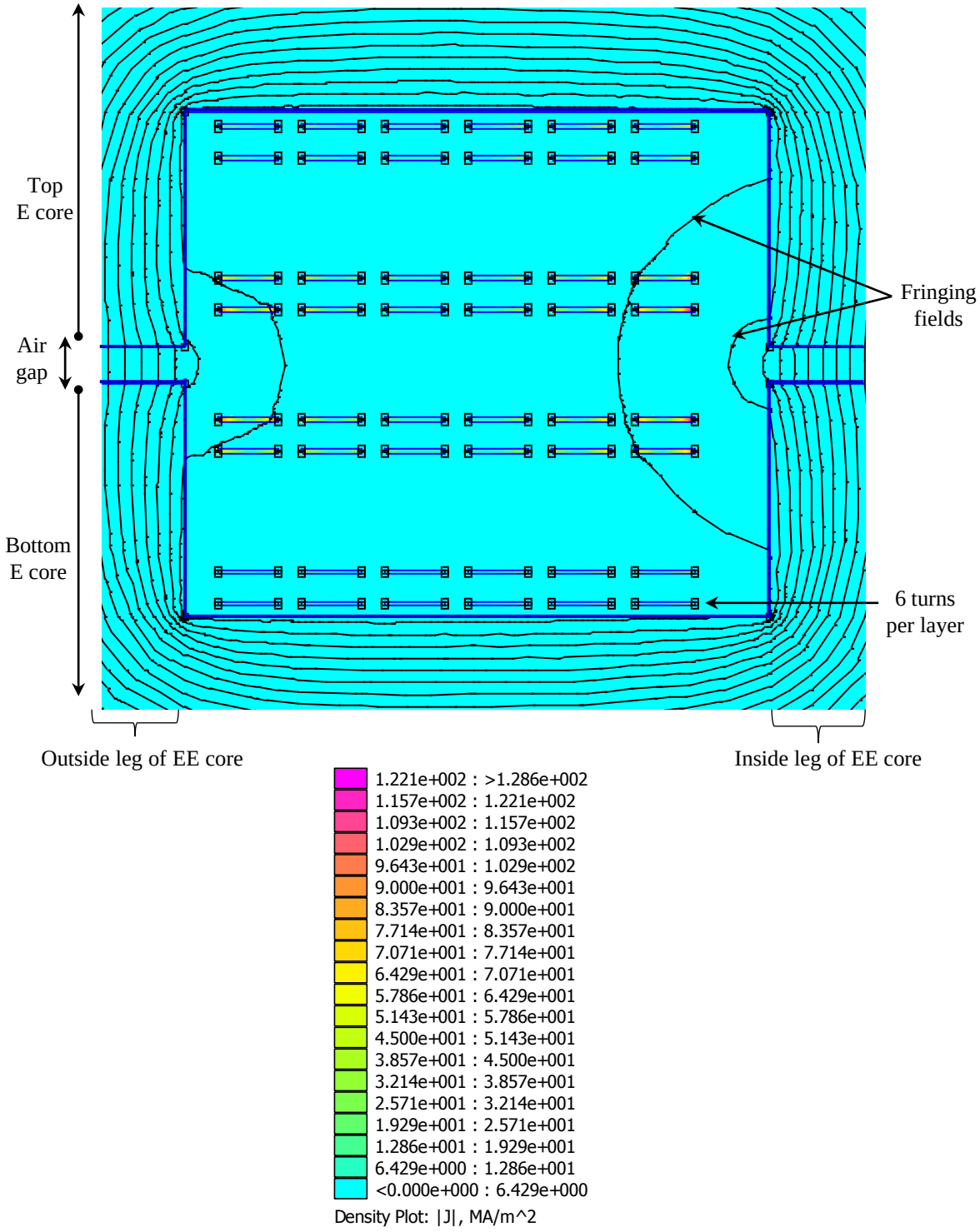


Figure 2.21: Fringing effect demonstrated by FEMM simulation of flux line and current density in a planar inductor. The winding consists of eight 1-Oz copper layers in parallel, each has six turns of winding.

2.6.2.3 Transformer Design

In transformer design, the secondary-side windings conduct higher RMS current and high copper loss is expected. The minimum possible number of turns are required to minimize this loss. The turn ratio of 1:0.4:0.4 is realized by five turns in the primary winding and two turns in each of the secondary windings. Table 2.6 describes the final transformer designs along with their measured inductances.

Table 2.6: Two transformer designs using PQ and planar EE cores

Core	PQ20/20	EE1805
Wire	AWG#46-strand Litz wire	1-Oz Cu PCB traces
Primary side	360 strands	four layers
Each secondary side	665 strands	two layers
Number of turns	5:2:2	5:2:2
Air gap (μm)	130	80
Inductance		
Magnetizing (μH)	6.90	7.15
Primary-side leakage (nH)	100	50
Each secondary-side leakage (nH)	320	46

Note that in the PQ-core transformer, the secondary-side leakage inductance includes the current measurement loop. The planar transformer requires a small air gap of 80μm. Therefore, the fringing flux has less effect on the total copper loss, and the maximum number of eight layers is used. Details of layer arrangement and PCB layouts for the planer transformer can be found in Appendix A.

2.7 Experimental Results

Two 1 MHz, 24 V-to-3.3 V, 6 W prototypes are built based on the two magnetics designs in the previous section. Prototype 1 uses PQ magnetic core with high transformer's secondary-side leakage inductance, including current measurement loops, to verify the converter operation and

analytical model. Prototype 2, as shown in Fig. 2.22, uses planar magnetics to reduce magnetics size and leakage inductance. Resonant tank values and device part numbers for each prototype are listed in Table 2.7.

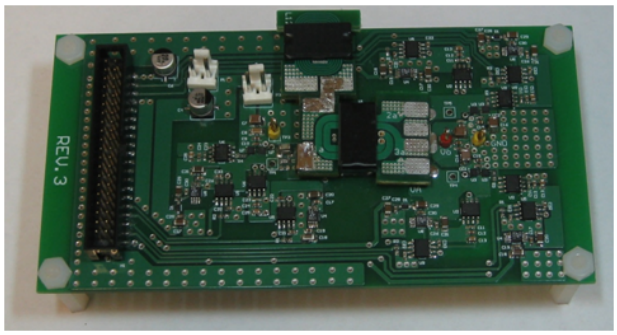


Figure 2.22: 1 MHz, 24 V-to-3.3 V, 6 W prototype 2 board using planar magnetics

Table 2.7: Prototype components list

	Prototype 1	Prototype 2
Q_1, Q_2	CSD17313Q2	
$SR_{1,2}, Q_{a,b}$	CSD16301Q2	
Gate drivers	EL7104	
n	0.4	
C_f (μF)	2.0	
C_{clamp} (μF)	2.0	
C_s (nF)	11.6	12.42
L_s (μH)	3.14	3.85
L_m (μH)	6.90	7.15
L_{lk} (nH)	320	46
Magnetic core	0L42020UG	CL41805EC

Fig. 2.23 shows the experimental waveforms of the the prototype 1 using PQ cores. It demonstrates the benefits of active clamp LLC converter: 50% duty cycle operation of all switches, ZVS on primary side, ZCS on secondary side, and v_a and v_b clamped to twice the output voltage.

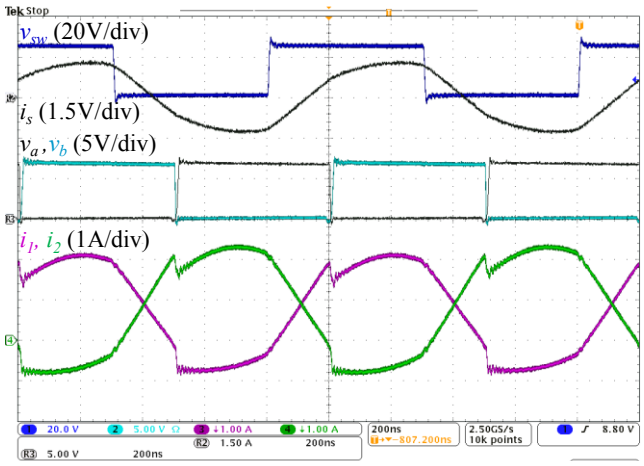


Figure 2.23: Experimental waveforms of the 1 MHz, 24 V-to-3.3 V, 5.7 W prototype 1 using PQ cores, shown at time scale of 200 ns/div

Compared to the ideal waveforms shown in Fig. 2.1, small sharp transitions can be observed in the secondary-side currents at t_α. These current glitches are due to the fact that when SR_1 or SR_2 is turned off at zero current, it pulls more current to charge its drain-to-source capacitor from both output capacitor C_f and the other secondary winding current. It has been verified that the glitches do not affect the converter efficiency significantly, which is 92.6% at full load. Experiments with the prototype 1 also validates the analytical model developed in Section 2.4 and 2.3. Referring back to Fig. 2.13, it can be observed that the converter theoretical output characteristics and predictions of t_α and RMS currents match well with experimental data. In Fig. 2.15, experiments verify that the converter behaves approximately like a current source, which supplies the same output current at different output voltage values. Compared with theoretical predictions, there is higher loss at higher output voltages, which results in a slight drop in output current.

The second prototype is built using planar magnetics, with a smaller size and lower transformer secondary-side leakage inductance. At a similar maximum output power, there is a trade-off between the size and losses of magnetic components: compared to the prototype with PQ cores, a reduction of core volume by a factor of 3 and core height by a factor of 2.5 results in an efficiency drop of about 2%. The reduction of magnetics size is especially important when there are multi-

ple modules in parallel. Therefore, planar magnetics are more suitable for multi-module system implementation, which is discussed in Chapter 4.

Loss Breakdown:

For both prototypes, component losses are calculated using the methods summarized in Table. 2.8.

Table 2.8: Summary of loss calculation methods

Type	**Method**	**Explanations**
Magnetics loss		
Core loss	Improved generalized Steinmetz equation	Refer to Eq. (2.45), (2.44)
Copper loss	Finite element analysis	Available in softwares such as FEMM [92]
Conduction loss	$P_{cond} = I_{RMS}^2 R_{par}$	I_{RMS}: RMS current R_{par}: parasitic resistance of MOSFETs, resonant capacitor's ESR or PCB trace
Switching loss [26] (at MOSFET turn-off)	$I_{drv} = \frac{V_{PL}}{R_{drv}+R_g}$	I_{drv}: gate driver current, assumed constant V_{PL}: plateu voltage in gate charge curve R_{drv}: gate driver output resistance R_g: MOSFET's gate resistance
	$t_{sw} = \frac{Q_{gd}+Q_{gs}-Q_{g(th)}}{I_{drv}}$	t_{sw}: switching loss duration Q_{gd}: gate charge - gate to drain Q_{gs}: gate charge - gate to source $Q_{g(th)}$: gate charge at threshold voltage
	$P_{sw} = 0.5 V_{sw} I_{sw} t_{sw} f_s$	I_{sw}: device current right before turn-off V_{sw}: drain-to-source voltage after turn-off
Gate driver loss	$P_{drv} = Q_g V_{drv} f_s$	V_{drv}: voltage supply for gate drivers Q_g: MOSFET's total gate charge

Since the converter features ZVS turn-on of all devices and ZCS turn-off of the rectifier devices, the majority of switching loss occurs when Q_1, Q_2, Q_a and Q_b are turned off at non-zero current. The switching loss derivations, along with device parameters can be found in Appendix. B.

Fig. 2.24 compares the loss breakdown of both prototypes. While the loss (mostly conduction loss) of secondary-side MOSFETs dominates in prototype 1, the magnetics loss, which is twice as large compared to prototype 1, dominates in prototype 2. Note that the measured and calculated losses do not take into account the gate driver loss, which is estimated to be 61 mW.

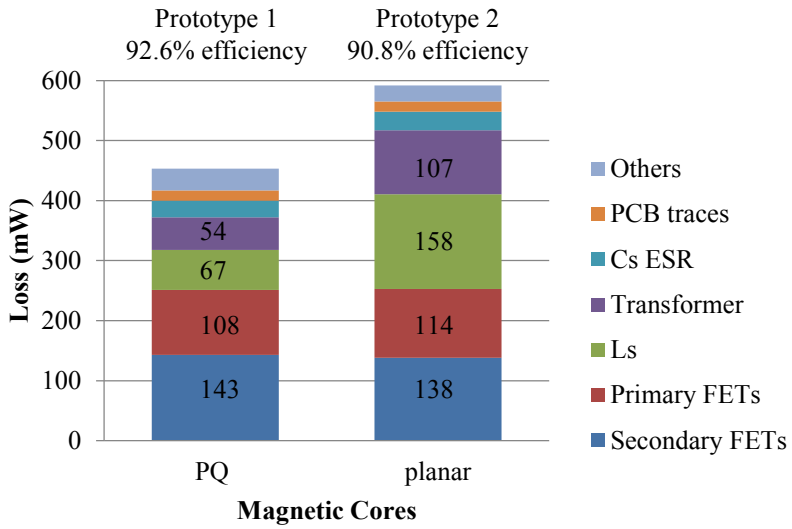


Figure 2.24: Loss break-down for prototype 1 using PQ cores and prototype 2 using planar magnetics

2.8 Summary

This chapter studies the steady-state operations and characteristics of the active clamp LLC resonant converter, which is proposed to address the voltage oscillation across rectifier devices in the traditional LLC converter. In the proposed converter, the voltage stress on the secondary-side devices is limited to twice the output voltage. In combination with LLC converter advantages, including primary-side ZVS, secondary-side ZCS and 50% duty-cycle operation, this makes the converter suitable for single or multi-module high-frequency high step-down low-voltage point-of-load applications where secondary side MOSFETs and control circuitry can be integrated in a low-voltage CMOS process. The modeling and design approaches are presented, based on a combination of state-plane and sinusoidal approximation techniques. Two 1 MHz, 24 V-to-3.3 V,

6 W experimental prototypes are built, using PQ and planar magnetic cores, respectively, to verify the analysis and design techniques.

Chapter 3

On/Off Control of One Module

The analysis and experimental results in the previous chapter proves that the active-clamp LLC converter behaves approximately like a current source in steady state. Moreover, the resonant tank stores insignificant energy, allowing the converter to be turned on or off quickly. These properties make the converter suitable for the on/off control method to regulate the output voltage against load variations. This chapter studies the on/off control for one active clamp LLC module. Section 3.1 introduces the converter models to understand its transient behavior. In Section 3.2, the controller implementation and experimental results are presented, then a simple averaged model is suggested to facilitate fast and efficient converter simulation. Finally, the chapter summary is given in Section 3.3.

3.1 Converter Modeling

The on/off control of the active clamp LLC resonant converter requires two types of models. The first one is a high-frequency model including details of the four subintervals in a switching cycle. This model helps determine the gate timing sequence to operate the converter close to a constant current source. The second one is an averaged model for the output current, as well as the output and clamp voltages. It provides an insight onto how the converter behaves under the on/off control method.

3.1.1 High-Frequency Model

In the previous chapter, the active-clamp LLC converter is proved to behave approximately like a constant current source in steady state. The output current value is controlled by the variable t_α that determines when to turn on or off the rectifier devices SR_1, SR_2 and their complimentary clamp devices Q_a, Q_b. The on/off control method also requires the converter to reach its steady state quickly when enabled, which demands a special turn-on sequence. The state plane analysis has been utilized to find an optimal trajectory and to obtain fast transient performance in resonant converters [68, 103–106]. This section demonstrates that the same approach can be applied for the active clamp LLC converter using the high frequency model.

Model Overview: According to Section 2.2, the active clamp LLC converter is equivalent to an L_{eq}-C_s resonant circuit shown in Fig. 3.1, where

$$L_{eq} = L_s + \left[(L_{lk}/2n^2)//(L_m)\right].$$

The voltage sources v_{sw} and v_{th} in the AR operation are also illustrated in Fig. 3.1, along with

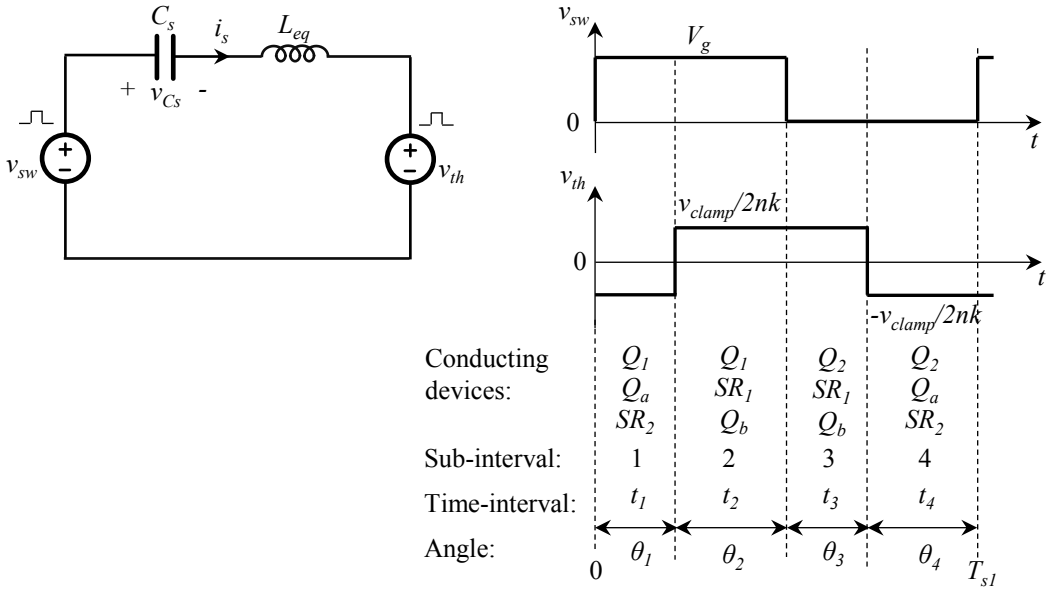


Figure 3.1: High frequency model to determine converter gate timing sequence in both transient and steady states

the redefinition of subinterval durations t_1, t_2, t_3, t_4, and their corresponding conduction angles θ_1, θ_2, θ_3, and θ_4. This definition applies for both transient and steady states, and the switching cycle T_{s1} is not necessarily the same as the nominal value T_s.

The equivalent circuit assists in the analysis of currents and voltages only on the primary side of the converter. In order to study the relationship between primary-side current i_s and current i_x transferred to the secondary sides, another equation is required to complete the high-frequency model:

$$\frac{di_s}{dt} = nk\frac{di_x}{dt} + k\frac{v_{th}}{L_m}, \tag{3.1}$$

where the coefficienty k is:

$$k = 1 + \frac{L_{lk}/2n^2}{L_m}.$$

Note that current i_x is a component of secondary side currents: $i_1 = 0.5(i_o + i_x)$ and $i_2 = 0.5(i_o - i_x)$, where i_o is the unfiltered output current. When the output voltage is well-regulated with small ripple, the clamp voltage v_{clamp} can be estimated to twice the constant output voltage $2V_{out}$, and the normalized form of (3.1) becomes:

$$\frac{dj_s}{d\theta} = nk\frac{dj_x}{d\theta} + \mathrm{sgn}(v_{th})k\frac{L_{eq}}{L_m}\bar{M}, \tag{3.2}$$

with $\bar{M} = M_{out}/nk$.

Trajectory Determination: With the complete high-frequency model, the state-plane trajectories of the normalized capacitor voltage m_{Cs}, primary-side current j_s and ac component of secondary-side current j_x can be constructed. As analyzed in Section 2.3, the trajectory of j_s vs. m_{Cs} in each subinterval is a circular path with a known center of rotation listed in Table 3.1.

Table 3.1: Centers of rotation for j_s vs. m_{Cs} trajectory

Subinterval	1	2	3	4
Center's coordinate	$(1+\bar{M}, 0)$	$(1-\bar{M}, 0)$	$(-\bar{M}, 0)$	$(\bar{M}, 0)$

The state-plane trajectory of j_x vs. j_s is constructed from various small linear segments that are calculated by:

$$\Delta j_s = nk\Delta j_x + \left[\mathrm{sgn}(v_{th})k\frac{L_{eq}}{L_m}\bar{M}\right]\Delta\theta. \tag{3.3}$$

This method can be implemented in softwares such as Matlab.

Fig. 3.2 shows the steady-state trajectories of j_s vs. m_{Cs} and j_x vs. j_s, along with the subinterval order and instantaneous values of the normalized variables. These values can be determined using the state plane analysis developed in Section 2.3.

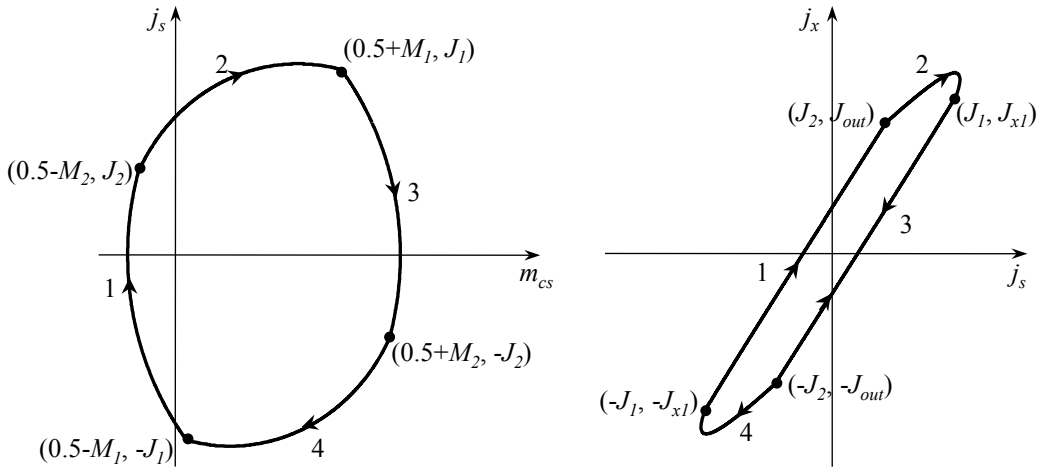


Figure 3.2: State-plane trajectories of j_s vs. m_{Cs} and j_x vs. j_s in steady state

When the converter is first turned on, the initial states are $m_{Cs}(0)$, $j_s(0) = 0$ and $j_x(0) = 0$. A transient trajectory can be found to reach steady state within the first switching cycle. As demonstrated in Fig. 3.3, the steady state is obtained at the end of either the second or third subinterval, depending on the initial capacitor voltage. The algorithm to determine the turn-on trajectory and its corresponding timing sequence is summarized Fig. 3.4.

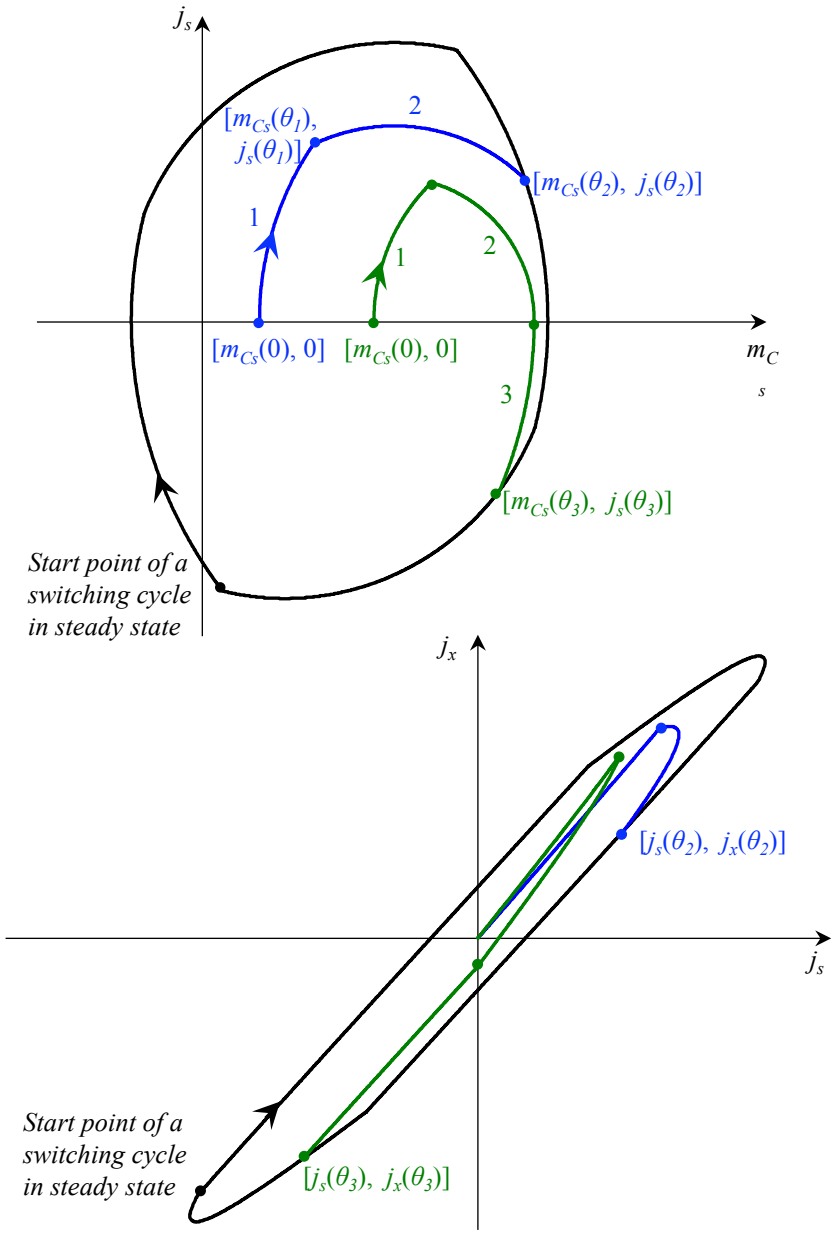


Figure 3.3: State-plane trajectories of j_s vs. m_{Cs} and j_x vs. j_s in steady state (black), turn-on transient that reaches steady state at the end of subinterval 2 (blue), and turn-on transient that reaches steady state at the end of subinterval 3 (green)

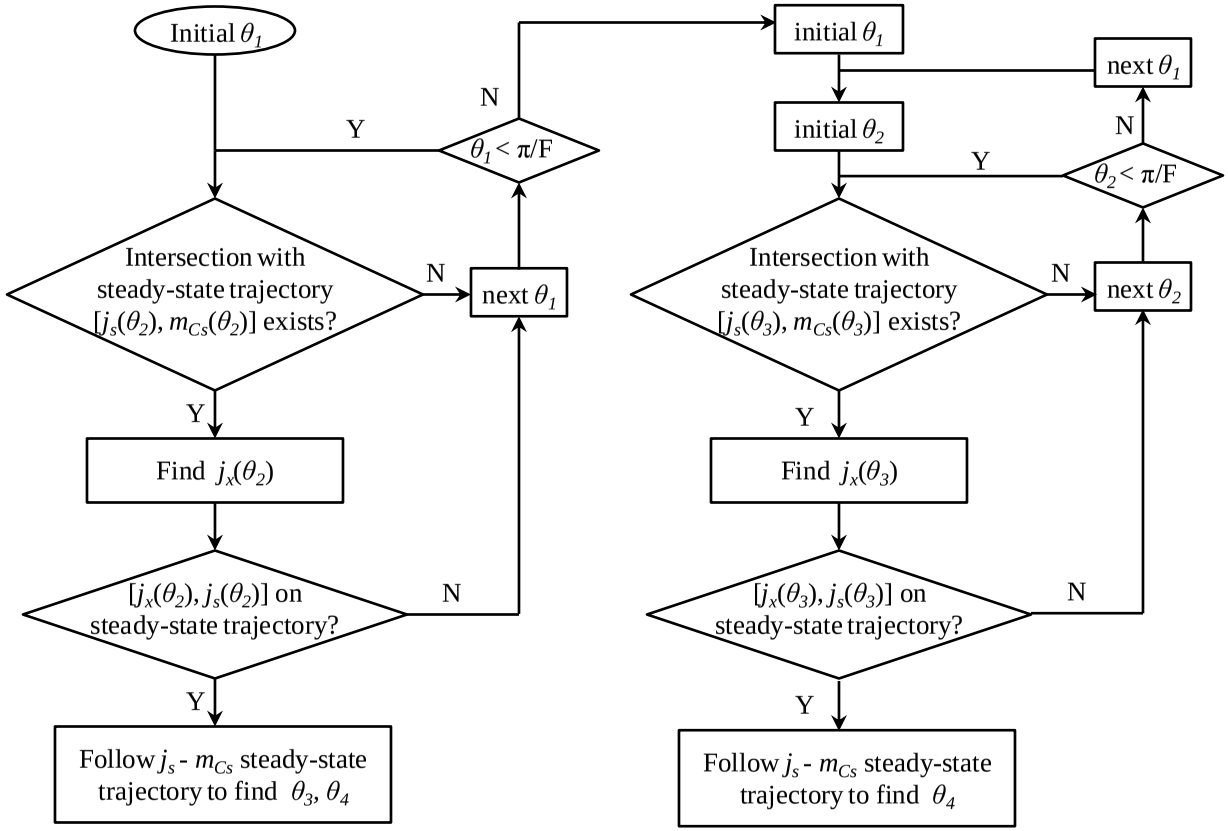


Figure 3.4: Computer algorithm to determine turn-on timing sequence

According to the flow chart in Fig. 3.4, the conduction angle θ_1 is swept when it takes the first two subintervals to reach steady state. For each value of θ_1, the state $[m_{Cs}(\theta_1), j_s(\theta_1)]$ at the end of subinterval 1 can be found easily, given the initial point and center of rotation. Subinterval 2 starts at this point with a new center of rotation listed in Table. 3.1. On the j_s vs. m_{Cs} normalized plane, the intersection of subinterval 2 transient trajectory and subinterval 3 steady-state trajectory, point $[m_{Cs}(\theta_2), j_s(\theta_2)]$, can be found using basic geometrical calculations. The corresponding state point $[j_x(\theta_2), j_s(\theta_2)]$ is then checked if it lies on the steady-state j_x vs. j_s trajectory. This can be done by determining the distance from this point to a set of steady-state data points stored in the computer memory. The solution of θ_1 is the value that satisfies steady state on both j_s vs. m_{Cs} and j_x vs. j_s planes. After that, the values of θ_3 and θ_4 are found by following the rest of the steady state trajectory.

A similar method is implemented for the case where it takes three subintervals to reach steady state, with the two conduction angles θ_1 and θ_2 being swept. The solution needs to satisfy steady state on both primary and secondary sides of the converter at the end of subinterval 3.

3.1.2 Averaged model

While the high-frequency model includes details of the converter operation within every switching cycle, the averaged model intends to study the converter's low-frequency behavior. This model is developed by averaging the unfiltered output current, the voltages and currents of the clamp and output capacitors over a switching cycle. As a result, the high-frequency harmonics in those voltage and current states are neglected, and their net change every switching cycle is the main concern in this model. The steps to derive the averaged model are described as follows.

Fig. 3.5 shows the converter model derived from the third simplification step in Section 2.2. The circuit on primary side is moved to secondary side, and the total parasitic resistance r_{sec} on each secondary side is added. In contrast to the L_{eq}-C_s equivalent model, this model shows the connection between the input and output sides of the converter. The waveforms of voltages $v_1 = v_{out} - v_a$ and $v_2 = v_b - v_{out}$ within one switching cycle are also included in the figure.

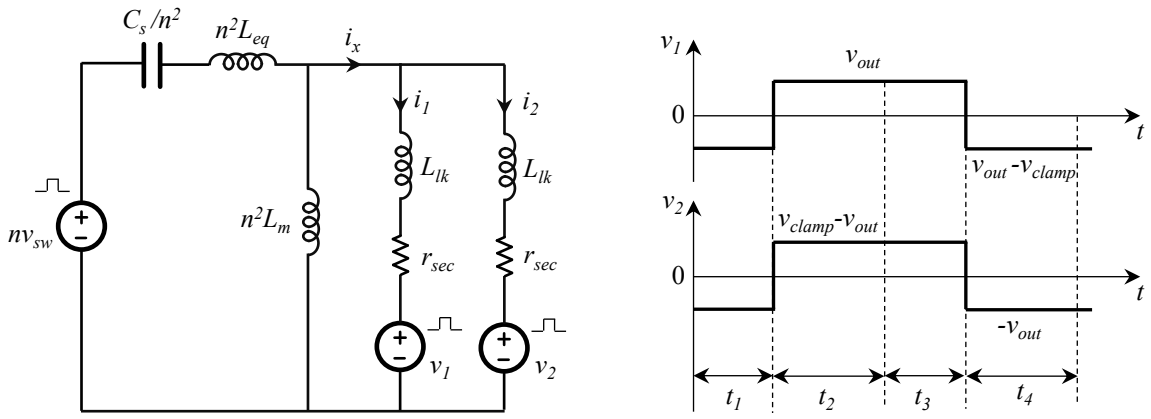


Figure 3.5: Rearrangement for step 3 of model simplification in Section 2.2. Waveforms of voltages v_1 and v_2 within one switching cycle are included.

Because the two parallel secondary sides in the model share the same voltage, it is found that:

$$L_{lk}\frac{di_1(t)}{dt} + v_1(t) + r_{sec}i_1(t) = -L_{lk}\frac{di_2(t)}{dt} + v_2(t) - r_{sec}i_2(t). \tag{3.4}$$

Substitute $i_1 = 0.5(i_o + i_x)$, $i_2 = 0.5(i_o - i_x)$, and the values of v_1 and v_2 shown in Fig. 3.5, (3.4) becomes:

$$L_{lk}\frac{di_o(t)}{dt} = v_{clamp}(t) - 2v_{out}(t) + r_{sec}i_o(t). \tag{3.5}$$

Besides (3.5), two other equations are needed before averaging all the currents and voltages. The first equation relates to the current i_f of the output capacitor:

$$i_f(t) = C_f\frac{dv_{out}(t)}{dt} = i_o(t) - I_{load}. \tag{3.6}$$

Note that the load current I_{load} is a constant value, ranging from 0 to the nominal current I_o supplied by the converter when it is running in steady state. The last equation is derived by noticing that the clamp capacitor current is equal to $-i_1$ during subinterval 1 and 4, and equal to $-i_2$ during subinterval 2 and 3:

$$i_{clamp}(t) = C_{clamp}\frac{dv_{clamp}(t)}{dt} = \begin{cases} 0.5\left[-i_o(t) - i_x(t)\right] & \text{for subinterval 1 and 4} \\ 0.5\left[-i_o(t) + i_x(t)\right] & \text{for subinterval 2 and 3.} \end{cases} \tag{3.7}$$

The currents and voltages in (3.5), (3.6) and (3.7) are averaged over one witching cycle, leading to a set of equations:

$$L_{lk}\frac{d\langle i_o(t)\rangle}{dt} = \langle v_{clamp}(t)\rangle - 2\langle v_{out}(t)\rangle - r_{sec}\langle i_o(t)\rangle \tag{3.8a}$$

$$C_f\frac{d\langle v_{out}(t)\rangle}{dt} = \langle i_o(t)\rangle - I_{load} \tag{3.8b}$$

$$C_{clamp}\frac{d\langle v_{clamp}(t)\rangle}{dt} = 0.5\left[\langle \bar{i}_x(t)\rangle - \langle i_o(t)\rangle\right], \tag{3.8c}$$

where the average variable $\langle \bar{i}_x \rangle$ is defined as:

$$\langle \bar{i}_x(t)\rangle = \frac{1}{T_s}\left(-\int_{t_1,t_4} i_x(t)dt + \int_{t_2,t_3} i_x(t)dt\right). \tag{3.9}$$

Using this equation set, an averaged circuit model is derived and shown in Fig. 3.6. A simpler averaged model based on this derivation is presented and verified in Section 3.2.2.

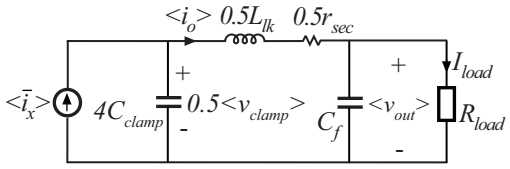


Figure 3.6: Converter averaged model

3.2 Hysteretic On/Off Control of One Module

This section demonstrates the hysteretic on/off control on an experimental prototype to verify the converter models introduced previously. The controller implementation and experimental results are presented in Section 3.2.1. Based on the experimental waveform observation, a simpler averaged model is suggested and validated in Section 3.2.2.

3.2.1 Experiment Setup and Results

Controller Implementation: The hysteretic on/off control of one module is evaluated on the prototype 1 presented in Section 2.7. It uses PQ-core magnetics and has the design specification of 1 MHz switching frequency, 24 V-to-3.3 V voltage conversion and 5.7 W output power. The clamp

and output capacitors are 8.8 μF and 47 μF, respectively. It is desired to regulate the output voltage at a ripple of $\pm$50 mV, using the controller implementation shown in Fig. 3.7.

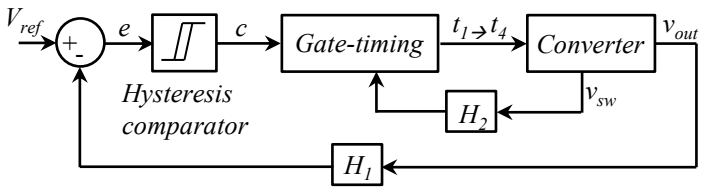


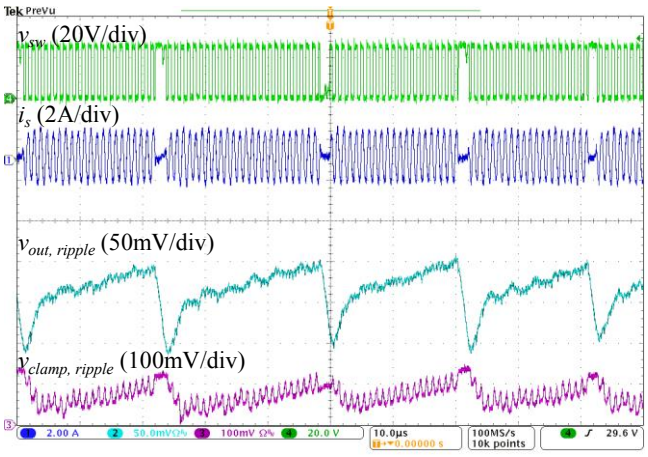
Figure 3.7: Hysteretic control diagram for one module

In this control diagram, the output voltage v_{out} is sensed and compared with the referenced voltage V_{ref}. The hysteresis band of the comparator determines the ripple $\pm\Delta V_{ripple}$ at the output voltage. When the sensed v_{out} reaches the preset maximum value $V_{ref} + \Delta V_{ripple}$, the control signal c is disabled and the converter is turned off. The output filter capacitor is discharged by the load current and the output voltage decreases until reaching the preset minimum value $V_{ref} - \Delta V_{ripple}$. The control signal c is enabled and the converter is turned on, starting to supply current to the load and charge the output capacitor. The output voltage increases up to the maximum value and the same process repeats to regulate v_{out}.

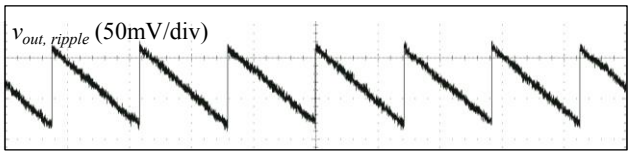
The gate-timing block is implemented as follows: at the rising edge of the control signal c, the gate-timing block reads the initial value of v_{C_s}, and uses a six-row look-up table to determine the turn-on timing sequence that brings the converter to steady state operation within the first switching cycle; after that, steady state timing is used. The timing intervals can be calculated offline using the high-frequency model presented in Section 3.1.1. The turn-on timing is more accurate when the lookup table contains more rows, but with the expense of a longer processing time. The initial v_{C_s} can be obtained easily by sensing the voltage v_{sw} across the input switching node. When the converter is off, the low-voltage oscillation across the rectifier devices is reflected to the primary side, and causes ringing at v_{sw} with a frequency of approximately 2.3 MHz. Therefore, a low-pass filter is required in order to sense the correct initial value of v_{C_s}.

The output voltage and switching node voltage are sensed by the ADC part number THS1030 and AD9280, respectively. The two blocks H_1 and H_2 in the feedback loop are required to scale the sensed voltages to within the ADC range.

Experimental Results: Fig. 3.8a shows experimental waveforms of the switching node voltage v_{sw}, primary-side current i_s, output voltage ripple $v_{out,ripple}$, and clamp voltage ripple $v_{clamp,ripple}$ at 90% load. It can be seen that i_s comes close to steady state in less than 1 μs. The output voltage varies from 3.25 V to 3.35 V at 45 kHz on/off (PWM) frequency. At mid-range load currents, the PWM frequency can reach up to 130 kHz. The controller is able to regulate the output voltage at no load as shown in Fig. 3.8b.



(a) 10µs/ horizontal div



(b) 10ms/ horizontal div

Figure 3.8: Experimental results for hysteretic control of one module at: (a) 90% load and (b) no load

The converter efficiency is recorded at various loads and is shown in Fig. 3.9. Compared to the fixed frequency on/off PWM, the hysteretic controller reduces the on/off frequency at light load, which helps improve the light-load efficiency. As an example, the efficiency at 10% load is 85% if a fixed 100 kHz on/off frequency is implemented, whereas the efficiency is close to 89% by using

hysteretic on/off control. Predicted overall efficiency of a system containing up to eight modules is also shown in Fig. 3.9, based on the fact that in steady state at most one module is operating in the on/off PWM mode while the others are either fully on or off. It is seen that systems of eight or more modules perform at efficiency higher than 90% over a wide load range.

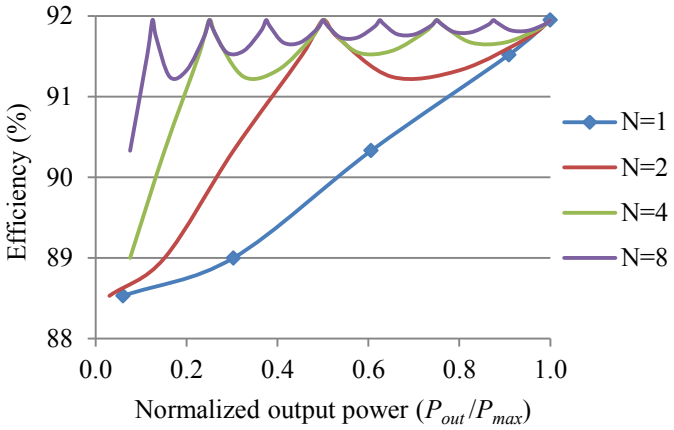


Figure 3.9: Efficiency at various loads of one module (experimental) and multiple-module systems (projected)

3.2.2 Simplified Averaged Model

The averaged model in Fig. 3.6 is a third-order system with the damping resistance equal to $0.5r_{sec}$. Based on the observation from experiments that the output voltage is well-damped, the leakage inductance in the averaged model can be omitted. Additionally, since $\langle \bar{i}_x(t) \rangle$ can quickly reach its steady state I_o (maximum supply current of the converter), the output is approximated as a constant current source controlled by the on/off control signal c. Based on these assumptions, a simpler model (Fig. 3.10) is then obtained and verified by experiments.

Figs. 3.11 shows an example of how the simple model predicts v_{out} and v_{clamp} similar to the experimental results. The waveforms are obtained for the same conditions: ± 50 mV hysteresis band and 90% load. The model explains why there is a fast ramp-up at the output voltage right after the converter is turned on. During the converter's off-time, the clamp capacitor is disconnected from the circuit and its voltage stays at approximately twice the programmed maximum output voltage.

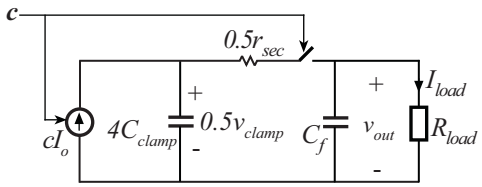


Figure 3.10: Simple averaged models of one module for simulation

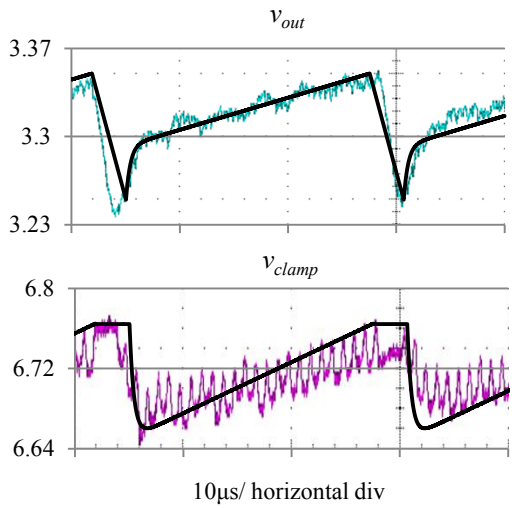


Figure 3.11: Output and clamp voltage waveforms from experiment (in colors), and simulation of simple averaged model (in black). The results are both obtained on the same conditions: ±50 mV hysteresis band and 90% load.

That means the voltage across $4C_{clamp}$ in the model stays at the maximum value $V_{ref} + \Delta V_{ripple}$. On the other hand, the output capacitor C_f is discharged until it reaches the programmed minimum value $V_{ref} - \Delta V_{ripple}$. Therefore, when the converter is turned on again, C_f is first charged by both $4C_{clamp}$ and the current source I_o. When the two capacitors reach an equilibrium voltage, they are both charged by I_o. Given the output voltage ripple of $\pm\Delta V_{ripple}$, a helpful approximation for PWM on/off frequency is:

$$f_{pwm} = M_i(1 - M_i)\left(\frac{I_o}{2C_f \Delta V_{ripple}}\right), \tag{3.10}$$

where $M_i = I_{out}/I_o$. The maximum PWM frequency happens at load current equal to $I_o/2$:

$$f_{pwm,max} = \frac{I_o}{8C_f \Delta V_{ripple}}. \tag{3.11}$$

The simplified model can be applied easily to the on/off control of a multi-module system to assist the controller design and provide a fast simulation speed. More details are provided in the next chapter.

3.3 Summary

On/off control is a simple yet efficient method to regulate the output voltage of an active clamp LLC module. In this method the module is either fully off, or operating at its maximum efficiency. Therefore, it maintains a high overall efficiency over a wide load range. Two converter models are introduced: (i) a high-frequency model to determine a gate timing sequence leading to fast module turn-on capability, and (ii) an averaged model to analyze the converter low-frequency behavior. The hysteretic on/off control is implemented to verify the models on an experimental prototype. Furthermore, experiments validate a simple averaged model that is helpful in designing the on/off controller for a multi-module system presented in the next chapter.

Chapter 4

On/Off Control of Multiple-Module System

This chapter analyzes and evaluates the on/off control method in the multiple-parallel-module architecture, using the active-clamp LLC resonant converter as the module topology. The chapter is organized as follows. Section 4.1 describes the system modeling, on/off controller design and implementations. Section 4.2 presents simulation and experimental results, using multiple 1 MHz, 24 V-to-3.3 V, 5 W module prototypes. Section 4.3 compares the proposed on/off-controlled multi-module system with a voltage-controlled synchronous buck converter in terms of output capacitor size. A discussion on hysteretic and fixed-frequency on/off control is also given. The chapter is summarized in Section 4.4.

4.1 System Modeling and Compensator Design

In this section, the model for a multi-module system is developed from the converter's simplified averaged model introduced in the previous chapter. Based on the system model, the plant transfer function is derived, and then standard PI or PID compensator is designed and implemented.

4.1.1 System Modeling

Fig. 4.1 shows the schematic of a system consisting of multiple active-clamp LLC modules. The simulation model of the system is set up as shown in Fig. 4.2a.

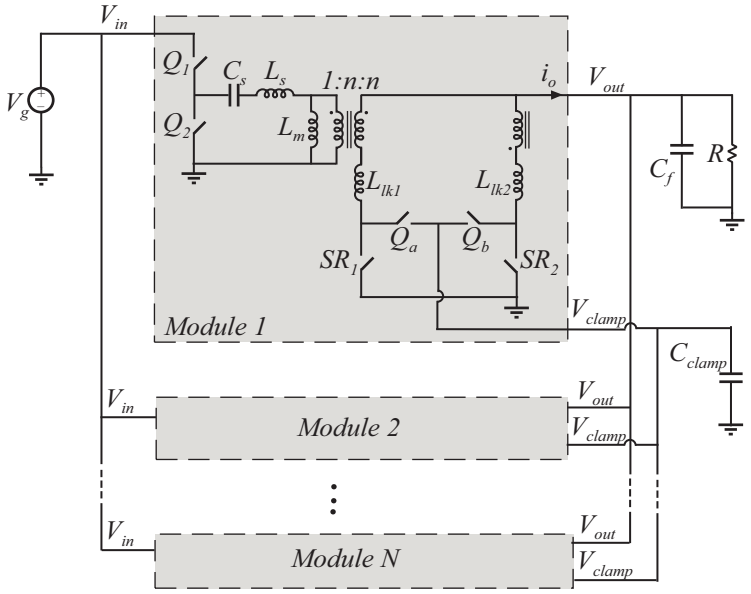


Figure 4.1: Schematic of N-module active-clamp LLC converter

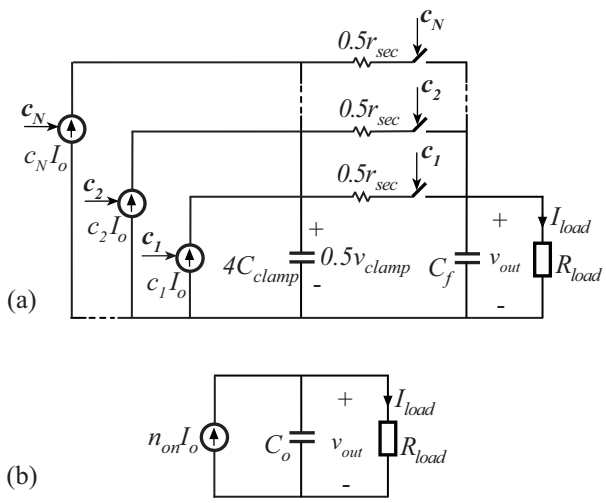


Figure 4.2: Simple averaged models of an N-module system for (a) simulation and (b) compensator design

As discussed in Section 3.2.2 for single-module control, the disconnection of the clamp capacitor from the output causes a fast ramp-up at v_{out} when the converter is turned on. In the multi-module system, because all modules share the same clamp and output capacitors, the fast ramp-up at v_{out} does not happen as long as there is at least one module fully on, or $4C_{clamp}$ is

always connected to C_f. Based on this simple averaged model, an ideal first-order model for an N-module system is derived and shown in Fig. 4.2b, where the capacitor C_o is defined as:

$$C_o = C_f + 4C_{clamp}. \tag{4.1}$$

The control variable for this system is the number n_{on} of on modules, and the control-to-output transfer function, from n_{on} to the output voltage v_{out} is found:

$$G_{vn}(s) = \frac{I_o R_{load}}{1 + \frac{s}{1/(C_o R_{load})}} = \frac{G_{vn0}}{1 + \frac{s}{2\pi f_{vn0}}}. \tag{4.2}$$

Note that at light load when $n_{on} \leq 1$, the transfer function expressed in (4.2) is only an approximation because $4C_{clamp}$ does not always participate in the circuit's operation in this case.

4.1.2 Compensator Design

After the control-to-output transfer function is derived, a controller can be designed and implemented. Fig. 4.3 demonstrates the control implementation for an N-module system.

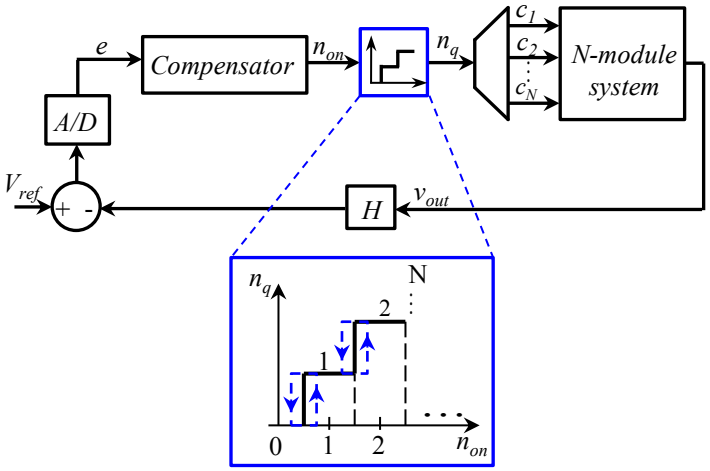


Figure 4.3: On/off control implementation for N-module system

In the diagram, the output voltage is sensed and compared to a reference voltage V_{ref}. An ADC samples the voltage difference, or error e, and sends it to a compensator to determine the number of on modules n_{on}. When the controller is implemented digitally, the compensator design

needs to take into account sensing and computational delay. A quantizer realizes on/off control by converting n_{on} into a quantized number n_q, and also by limiting the number range from 0 to N. In steady state, n_q alternates between two consecutive numbers, which generates PWM on/off control of one module while the others are either fully on or off.

Hysteresis is added to the quantizer block in order to obtain a practical on/off PWM frequency, preferably less than one fourth of the switching frequency. This practical value is chosen as follows. Assuming an ideal PI compensator, the output voltage ripple in steady state can be estimated as a product of the quantizer hysteresis band and the compensator's proportional gain. Given an approximately constant output voltage ripple, the same reasoning as in Section 3.2.2 shows that the maximum on/off frequency occurs when the load current is equal to one half of one module's current supply, or $I_o/2$. Since it takes the first switching cycle for a module to reach steady state upon turning on, a conservative choice of the module on time is $2T_s$. At the load current of $I_o/2$, the ideal on/off duty cycle is 50%, which results in the minimum PWM period of $4T_s$. This means the maximum on/off frequency is equal to one fourth of the switching frequency.

Finally, given the quantized number n_q, a multiplexer simply sends out individual on/off commands c_i to the modules. Each module is controlled by digital gate-timing with look-up table to determine start-up and steady-state sequence t_1 to t_4, as described in Section 3.1.1.

Design examples are described for a dc-dc system containing two modules in parallel, each being the same 1 MHz, 24 V-to-3.3 V, 5 W module. In order to avoid the effect of output voltage ripple at twice the switching frequency, the sampling rate is chosen to be 2 MHz. The total sensing and computational delay is $T_{delay} = 560\ ns$.

First, the values of output and clamp capacitors need to be determined. By setting the steady-state voltage ripple at ±30 mV and limiting $f_{pwm,max} \leq 200\ kHz$ in (3.11), C_f is found to be at least 32 μF. The choice for C_{clamp} is not as critical as C_f - it only needs to maintain the 6.6 V clamp voltage with less than 10% ripple in steady state. With $C_{clamp} = 2\ \mu$F and $C_f = 35\ \mu$F, the

DC gain and corner frequency of control-to-output transfer function at maximum load are

$$G_{vn0} = \frac{V_{ref}}{N} = 1.65 = 4.3\ dB,$$
$$f_{vn0} = \frac{NI_o}{2\pi C_o V_{ref}} = 3.4\ kHz\,.$$

Fig. 4.4 shows Bode plots of the system control-to-output transfer function, using the ideal $G_{vn}(s)$ expression in (4.2), the PLECS simulation of averaged model shown in Fig. 4.2a, and the PLECS simulation of switched converter implemented with turn-on timing sequence. The

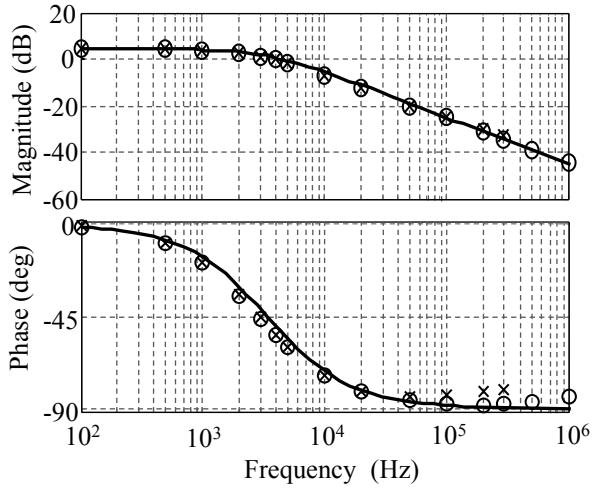


Figure 4.4: Bode plots of control-to-output transfer function, using the ideal $G_{vn}(s)$ expression in (4.2) (solid line), simulations of averaged model (o) and switched converter (x)

simulation data are obtained using a brute force method: adding perturbation to the control variable (number of on modules) at different frequencies, and recording the response at the converter output voltage. At perturbation frequencies closer to the switching frequency, the switched converter behaves non-linearly. This is due to the fact that each module is not an ideal current source, especially when the module on time is relatively close to the switching period. Therefore, the switched converter simulation results are shown in Fig.4.4 for up to 300 kHz. The simulation results validate both the averaged and ideal models presented in Fig. 4.2.

After the ideal control-to-output transfer function is validated, the next step is to design a digital controller for the system. Fig. 4.5 shows the block diagram of a digital controller for

the multi-module system, which is represented by the continuous-time transfer function $G_{vn}(s)$. Sensing and computational delay is included in the delay block. Output voltage error e is sampled by the ADC every T_{sample}. At the same rate, the controller $G_c(z)$ calculates and updates the digital command n^*_{on}, which is converted into analog value n_{on} by a zero-order-hold (ZOH). High resolution of n_{on} is assumed for the control model, and therefore, the quantization block is not included.

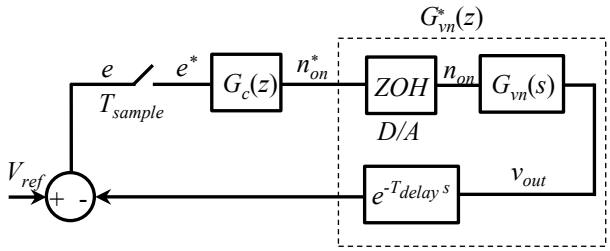


Figure 4.5: Block diagram of digital control for N-module system, including sensing and computational delay

According to [107], a continuous-time compensator $G_c(s)$ can be designed first for the ideal transfer function $G_{vn}(s)$. The equivalent discrete-time compensator $G_c(z)$ is found using the bilinear mapping from continuous-time to discrete-time domain, with prewarping at the cross-over frequency. In order to evaluate the compensator $G_c(z)$, z-transform of the continuous transfer function preceded by a ZOH is determined, taking delay into account,

$$G^*_{vn}(z) = (1 - z^{-1})\mathcal{Z}\left(e^{-T_{delay}s}\frac{G_{vn}(s)}{s}\right).$$

This can be found using ZOH mapping available in tools such as Matlab.

Fig. 4.6 shows Bode plots of the control-to-output transfer functions for ideal continuous-time system $G_{vn}(s)$, and discrete-time system with delay $G^*_{vn}(z)$. Compared to the ideal system, $G^*_{vn}(z)$ has a similar magnitude but its phase drops by 31° at 100 kHz. This should be considered when designing the compensator using standard frequency-domain techniques.

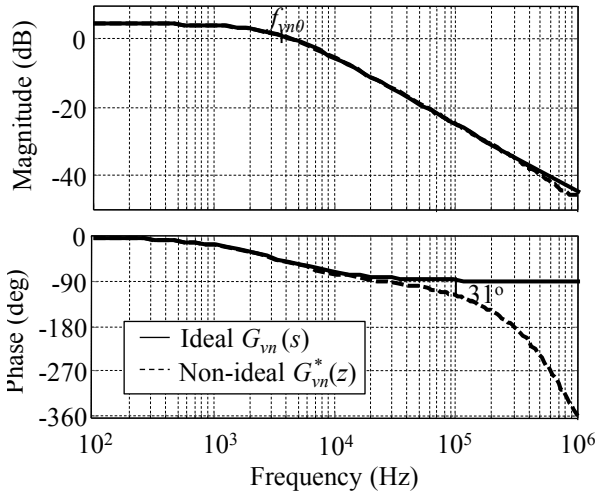


Figure 4.6: Bode plots of control-to-output transfer functions for ideal continuous-time system $G_{vn}(s)$, and non-ideal discrete-time system $G^*_{vn}(z)$

A compensator can be of PI or PID type,

$$G_{cPI}(s) = G_\infty \left(1 + \frac{2\pi f_L}{s}\right), \tag{4.3}$$

$$G_{cPID}(s) = G_0 \frac{\left(1 + \frac{2\pi f_L}{s}\right)\left(1 + \frac{s}{2\pi f_z}\right)}{\left(1 + \frac{s}{2\pi f_p}\right)}. \tag{4.4}$$

A PI compensator is simpler, while a PID compensator can result in faster response. For both controller designs, the cross-over frequency f_c is chosen to be 100 kHz (one-tenth the switching frequency), and the low-frequency zero f_L is set at 9 kHz (less than one-tenth of f_c). The PI compensator gain is given by:

$$G_\infty = \frac{f_c}{G_{vn0} f_{vn0}} = 17.9. \tag{4.5}$$

Considering the 31° phase drop of $G_{vn}(z)$ at 100 kHz , a phase margin φ_m is set to 79° for the analog PID compensator template. The methods in [5] yield the high-frequency zero, pole and dc

gain for the PID compensator:

$$f_z = f_c\sqrt{\frac{1+\cos\varphi_m}{1-\cos\varphi_m}} = 121 \text{ kHz} \tag{4.6a}$$

$$f_p = f_c\sqrt{\frac{1-\cos\varphi_m}{1+\cos\varphi_m}} = 82 \text{ kHz} \tag{4.6b}$$

$$G_0 = \frac{f_c}{G_{vn0}f_{vn0}}\sqrt{\frac{f_z}{f_p}} = 21.7. \tag{4.6c}$$

Fig. 4.7 plots the compensated loop gains for the ideal continuous-time system $T(s) = G_{vn}(s)G_c(s)$ and non-ideal discrete-time system $T^*(z) = G^*_{vn}(z)G_c(z)$. Because of time delay, the phase margins are 56° for PI and 45° for PID compensator.

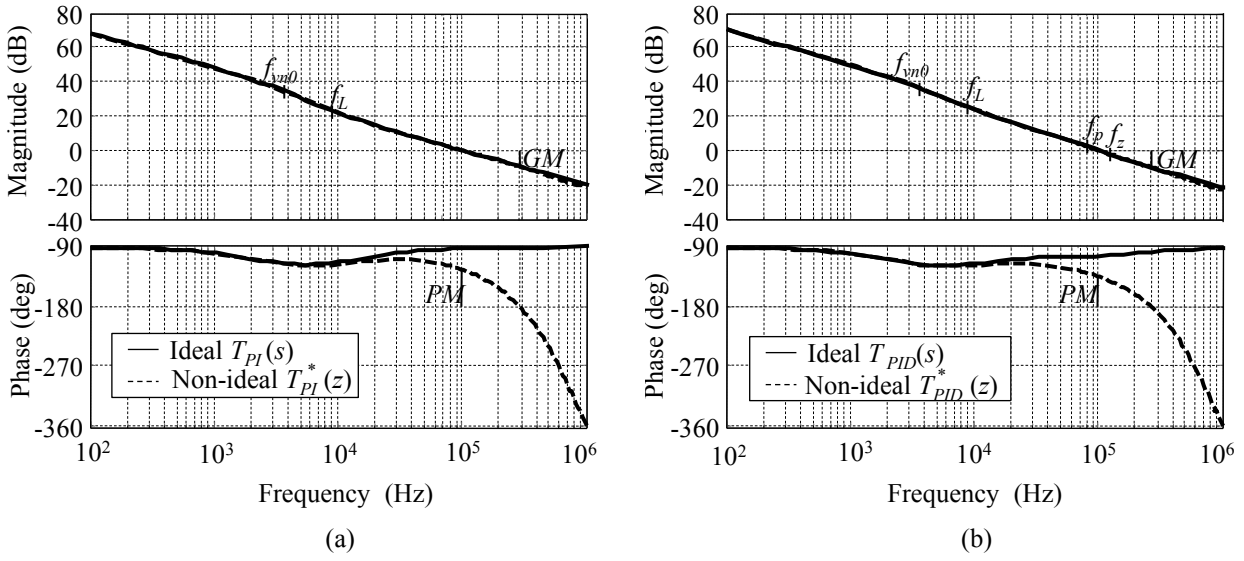


Figure 4.7: Compensated loop gain of ideal continuous-time system $T(s)$, and non-ideal discrete-time system $T^*(z)$ with: (a) PI compensator, non-ideal $PM = 56°$, $GM = 10$ dB and (b) PID compensator, non-ideal $PM = 45°$, $GM = 10$ dB

When there are very few modules in parallel, the PID controller may not be significantly more beneficial than the PI type because of the control variable saturation. A more detailed comparison between the two is presented in Section 4.2.

4.2 Simulation and Experimental Results

For multiple-module systems, both simulations and experiments use a 24 V-to-3.3 V, 5 W module prototype. As discussed in Section 2.7, planar cores are chosen for multi-module implementations to reduce the magnetics size. The revised resonant tank components and ADC part numbers are listed in Table 4.1.

Table 4.1: Prototype components list for multi-module system

n	C_s (nF)	L_s (μH)	L_m (μH)	L_{lk} (nH)	ADC for v_{out}	ADC for v_{sw}
0.4	15.52	3.60	6.90	30	THS1215	AD9280

This section is arranged as follows. In Section 4.2.1, experimental results are shown for a two-module system. The results are compared to simulations in order to validate the developed model. Further results on systems containing more than two modules are obtained by simulations in Section 4.2.2.

4.2.1 Two-module System

4.2.1.1 Simulation Results

In Matlab/Simulink with built-in PLECS library, the power stage is set up as shown in Fig. 4.2b. The control loop replicates the prototype digital controller, including ADC sampling, quantization and the estimated computational and sensing delay. Simulations are performed for a two-module system, using the values of C_{clamp}, C_f and compensators designed in Section 4.1.2.

Fig. 4.8 shows the simulation results in steady state for the two-module system controlled by the PI compensator. Two operating points are specifically studied in detail: 0.75 A output load corresponding to worst-case on/off frequency, and 1.5 A output load corresponding to worst-case voltage ripple.

The PWM on/off frequency is the highest at 0.75 A output (half of one module's current capacity). A hysteresis band of 0.2 is chosen to keep the frequency less than 250 kHz or one

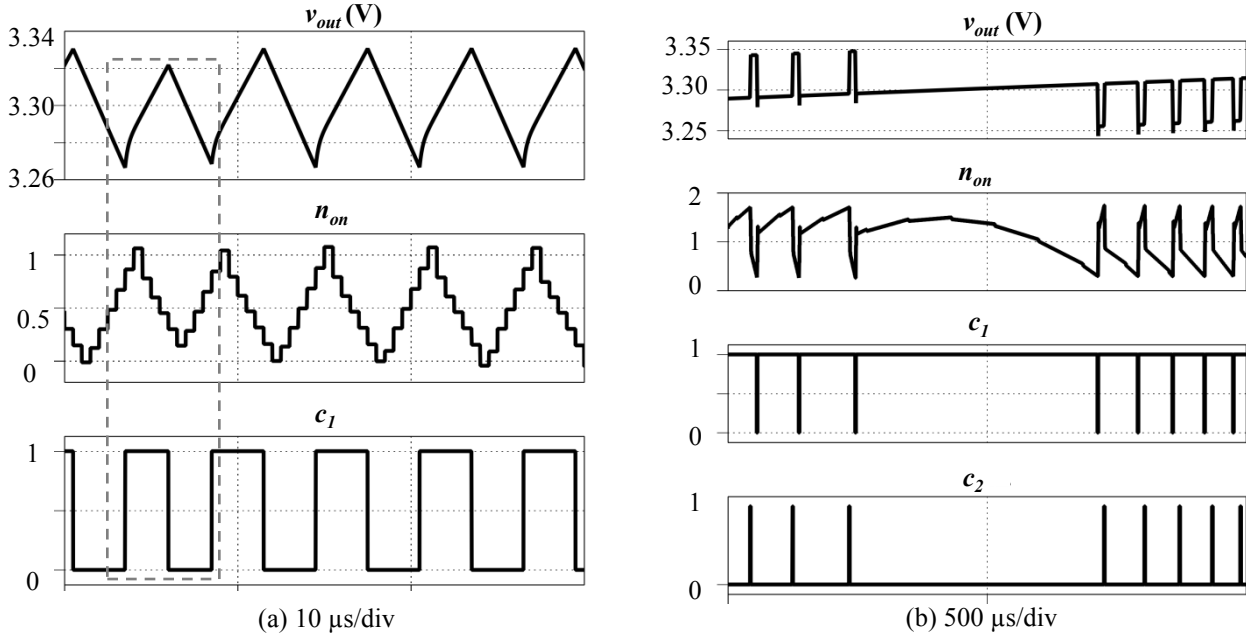


Figure 4.8: Simulation results for the two-module system controlled by PI compensator in steady state: (a) 0.75 A load current and (b) 1.5 A load current

fourth the switching frequency. The output voltage ripple stays within ±1% of the referenced 3.3 V output voltage. Ideally, the on/off frequency and duty cycle stay constant in steady state. However, Fig. 4.8a shows the frequency varies from 180 to 250 kHz and PWM duty cycles are not always 50%. This inconsistency also causes some smaller output ripple during a shorter PWM period. The reasons behind this behavior are related to power losses and PWM resolution. Because of power losses, the duty cycle is slightly different from 50%. Since the output voltage is sampled at 2 MHz, the PWM resolution is 500 ns, which is one-tenth of approximately 5 μs PWM period. The controller resolves this low resolution issue by adjusting the on and off times over a certain interval, resulting in an average duty cycle that meets the requirement. This variation in duty cycle can be considered a form of limit cycling [108].

The other special operating point is at 1.5 A load, very close to one module's current capacity of 1.52 A. A quick turn-off of module one, which lasts for at least 500 ns, causes a quick dip in output voltage. Both modules are then turned on to compensate for the voltage drop. Turning on module two causes the voltage to increase quickly, which consequently forces both modules to be

turned off, and so on. This explains why two, instead of one module, are on/off modulated. As a result, the voltage ripple is ±1.5% of the referenced voltage, not meeting the design specifications. However, with more modules in parallel, the output capacitor becomes larger, keeping the worst-case steady-state ripple within specifications.

The same capacitance value of 35 μF is used to study step-load transient responses, shown in Fig. 4.9. Along with the output voltage v_{out} and load current i_{out}, the compensator's output n_{on} and quantizer's output n_q are shown during both step-up and step-down transients between 5% load (0.15 A) and 95% load (2.89 A).

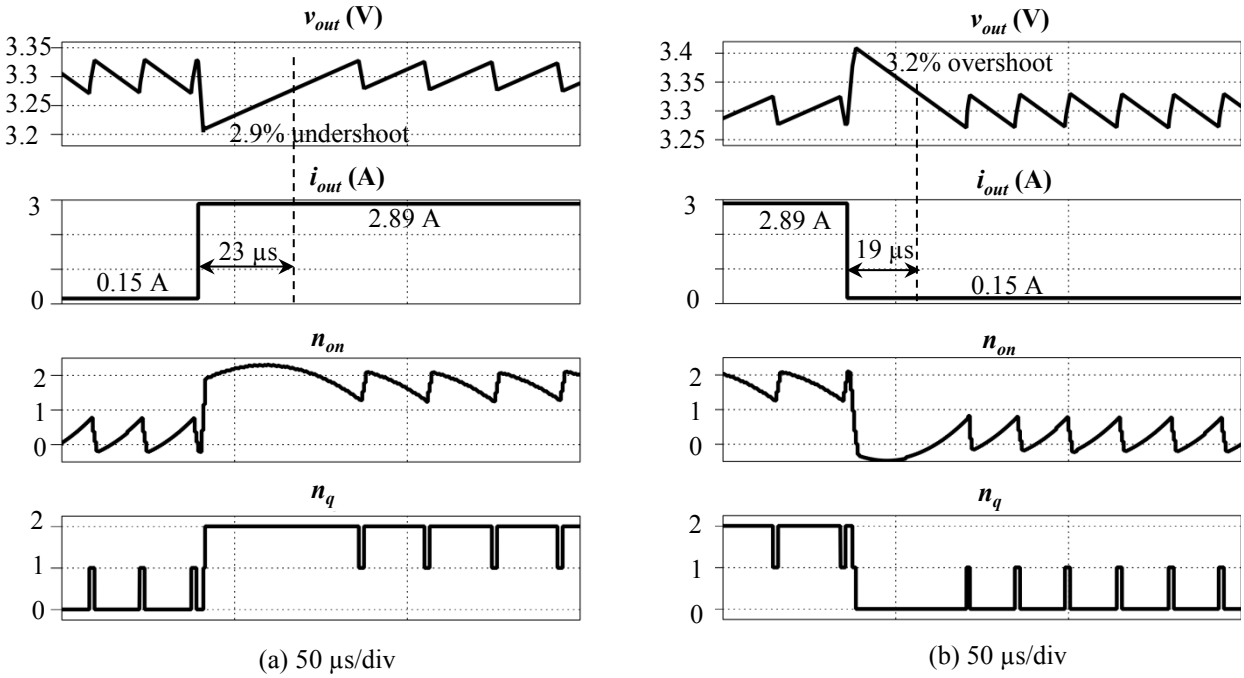


Figure 4.9: Simulation transient response of two-module system controlled by PI compensator: (a) load step-up from 5% to 95%, (b) load step-down from 95% to 5%

As shown in the figure, the output capacitor is sufficient to maintain output voltage within less than 5% of the nominal voltage. However, the transient-time is affected by the compensator output saturation. At load step-up, the compensator demands a higher n_{on}, corresponding to a higher current supply. However, the system is limited to only two modules, thus limiting the

transient performance. After two modules are fully turned on, the equivalent capacitor C_o is charged by a small difference between the supply and load currents. It takes 23 μs to return within 1% error in the output voltage. Similarly, at load step-down, the output capacitor C_f is discharged slowly by a small load current, resulting in 19 μs settling time. Because the participating capacitor in this case is only C_f, the step-down settling time is faster. In systems containing more modules, C_f is more dominant in the expression $C_o = C_f + 4C_{clamp}$, and the settling time difference between step-up and step-down transients becomes less significant.

Table 4.2 compares the step-load transient performance of two compensators. The PID compensator demands a higher n_{on} than the PI type. However, because the compensator output is saturated, the voltage change and settling time are similar in both cases. The minimum and maximum values of n_{on} suggest that if the system had three or more modules, the PID compensator would be more beneficial. For the two-module system, a simple PI compensator is sufficient.

Table 4.2: Comparison between PI and PID compensators for the two-module system

	PI	PID
5%load to 95% load		
- Voltage undershoot (%)	2.9	2.9
- Settling time (μs)	23	23
- Maximum n_{on}	2.3	2.7
95%load to 5% load		
- Voltage overshoot (%)	3.2	3.3
- Settling time (μs)	19	20
- Minimum n_{on}	-0.4	-0.9

When the load current is high, some electronics loads, such as microprocessors, demand a lower reference voltage in order to save the power consumption. As an example, Fig. 4.10 demonstrates the PI compensator's capability to regulate the output voltage upon a reference voltage step (3.3 V to 3.2 V) at 90% load.

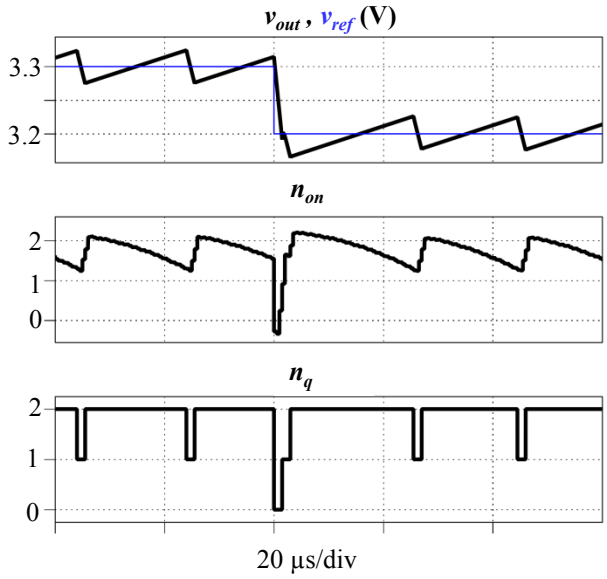


Figure 4.10: Simulation transient response of two-module system controlled by PI compensator. The reference voltage steps from 3.3 V to 3.2 V at 90% load.

4.2.1.2 Experimental Results

The designed PI controller, hysteretic quantizer and gate timing with look-up table are implemented digitally in Verilog HDL on a Virtex-IV FPGA board. The ADC samples the output voltage at 10 MHz with a latency delay of five clock cycles, output delay of 20 ns and the equivalent quantization of 2 mV. The controller reads the sensed voltage every five samples to avoid output ripple effects. This makes the equivalent sampling rate equal to 2 MHz. The experimental results are shown in Fig. 4.11.

Fig. 4.11a and b show the steady-state waveforms of the output voltage v_{out}, module on/off control signals c_1 and c_2 when the load current is 0.75 A and 1.5 A, respectively. As predicted by simulation at 1.5 A load, both modules are on/off modulated, causing the largest output voltage ripple of about ±50 mV. It is verified that PWM of two modules does not affect the system's efficiency in this case. At 0.75 A output, the PWM on/off frequency is the highest, ranging from 167 to 182 kHz, and the duty cycle does not stay constant. In general, the voltage ripples are somewhat larger than in simulations because each module does not behave exactly as an ideal current source

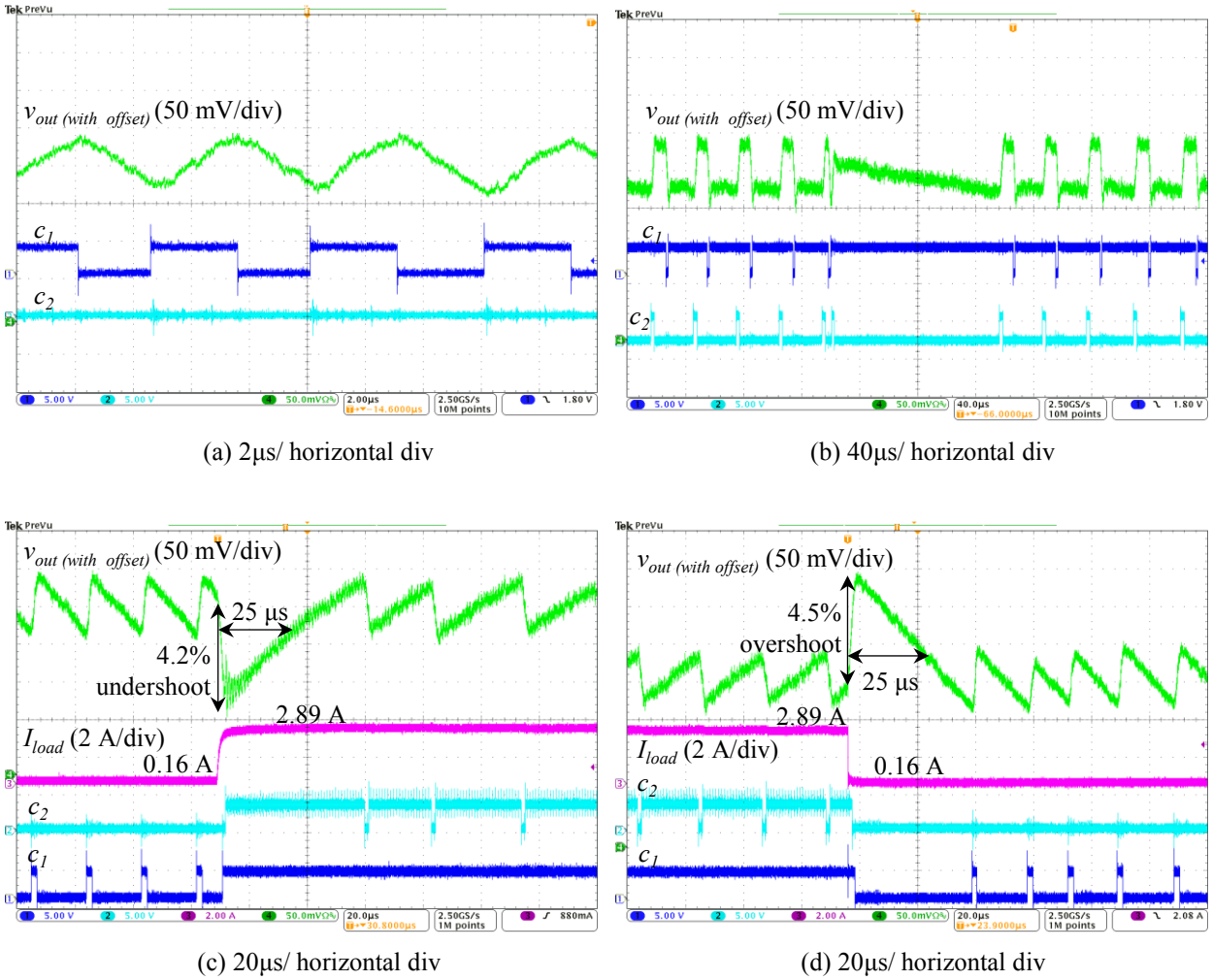


Figure 4.11: Experimental results of two-module system in: (a) steady state, 0.75 A load current, (b) steady state, 1.5 A load current, (c) load step-up transient, 5% to 95%, and (d) load step-down transient, 95% to 5%

that can be turned on/off instantaneously, as assumed in the model. When a module is turned off, depending on the resonant current direction, the body diode of one primary-side switch may keep conducting. The worst observed delay is approximately 300 ns, increasing v_{out} up to 10 mV. When a module is turned on, it takes the first switching cycle to reach steady state. The worst observed delay is about 600 ns, adding 16 mV to the output voltage ripple.

Transient responses at load step-up and step-down are shown in Fig. 4.11c and d, respectively. Because the modules are non-ideal current sources, the voltage change is larger than in simulations,

but it is still within 5% of the nominal voltage. The settling time in both load-steps is slightly longer than predictions because of the higher output voltage change of around 4.5% compared to 3% in simulation. Despite some differences between simulations and experiments, simulation remains a viable tool to verify a controller design for systems containing large number of modules in parallel.

4.2.2 Twenty-module System

This section evaluates compensators for a 90 W twenty-module system using simulations. Based on the previous design and verifications on the two-module system, the capacitance is scaled by the number of modules to guarantee a voltage change within 5% at large load steps, $C_{clamp} = N$ (μF) and $C_f = 17.5N$ (μF). For $N = 20$, the capacitor values are $C_{clamp} = 20$ μF and $C_f = 350$ μF. The PI and PID compensators are designed using the same method as in the two-module system. Assuming the same delay and keeping the same cross-over frequency and phase margin, all the poles and zeros in the compensator functions (4.3) and (4.4) are the same as in the two-module system. Only the gains are scaled by the number of modules,

$$G_{\infty(N-module)} = 0.5NG_{\infty(2-module)},$$

$$G_{0(N-module)} = 0.5NG_{0(2-module)}.$$

When there are more modules in parallel, the saturation effect of n_{on} and comparison between PI and PID compensators can be studied in more detail. Saturation at step-load transient happens when: (i) the steady-state value of n_{on} corresponding to the final load current reaches its minimum or maximum value (less than 1 or greater than N-1), and (ii) during transient interval, the compensator command is out of range ($n_{on} < 0$ or $n_{on} > N$). Consequently, the system reaches its limit, and cannot supply larger surplus current to charge or discharge the output capacitor upon sudden change in load. Given a certain output capacitor value and initial load value, the settling time depends on the compensator's capability and the final load value (i e. how close it is to the system's supply limit).

Different step-up scenarios, starting at the same 0.5 A load current, are examined in simulations for both PI and PID compensators. Fig. 4.12 compares the transient performance of the two compensators at different load steps: 80%, 90% and 95%. In the figure, Δv_{out} is the output voltage undershoot and t_{settle} is the time it takes v_{out} to reach within 1% error compared to its nominal value. For both compensators, saturation has little effect on transient voltage overshoot. At around 95% load step, the settling time is very sensitive to saturation. A small change to final load value from 28.5 A to 28.8 A results in 4-5 μs longer settling time. At load steps less than 95%, the PID compensator offers faster settling time, thanks to its capability to turn on more modules at a faster rate. Note that at 90% load step, the PID compensator can still out-perform the PI type even when a light saturation happens (n_{on} is 20 % higher than the maximum number of modules). The PID compensator looses its benefit when saturation is worse (n_{on} overshooting is higher than 33%).

Considering both step-up and step-down transients, if this system is designed to supply a load range from 5% to 95% of its power rating, the saturation effects during large load-steps can be minimized, and the PID compensator performs better. In a scenario when the sensing delay is reduced, the phase margin of the PI-compensated loop gain becomes higher compared to the analysis in Section 4.1.2. That means the PI controller updates n_{on} at a slower rate upon load steps, with less command undershoot or overshoot. Therefore, the PID controller will show more significant benefits over the PI type [80].

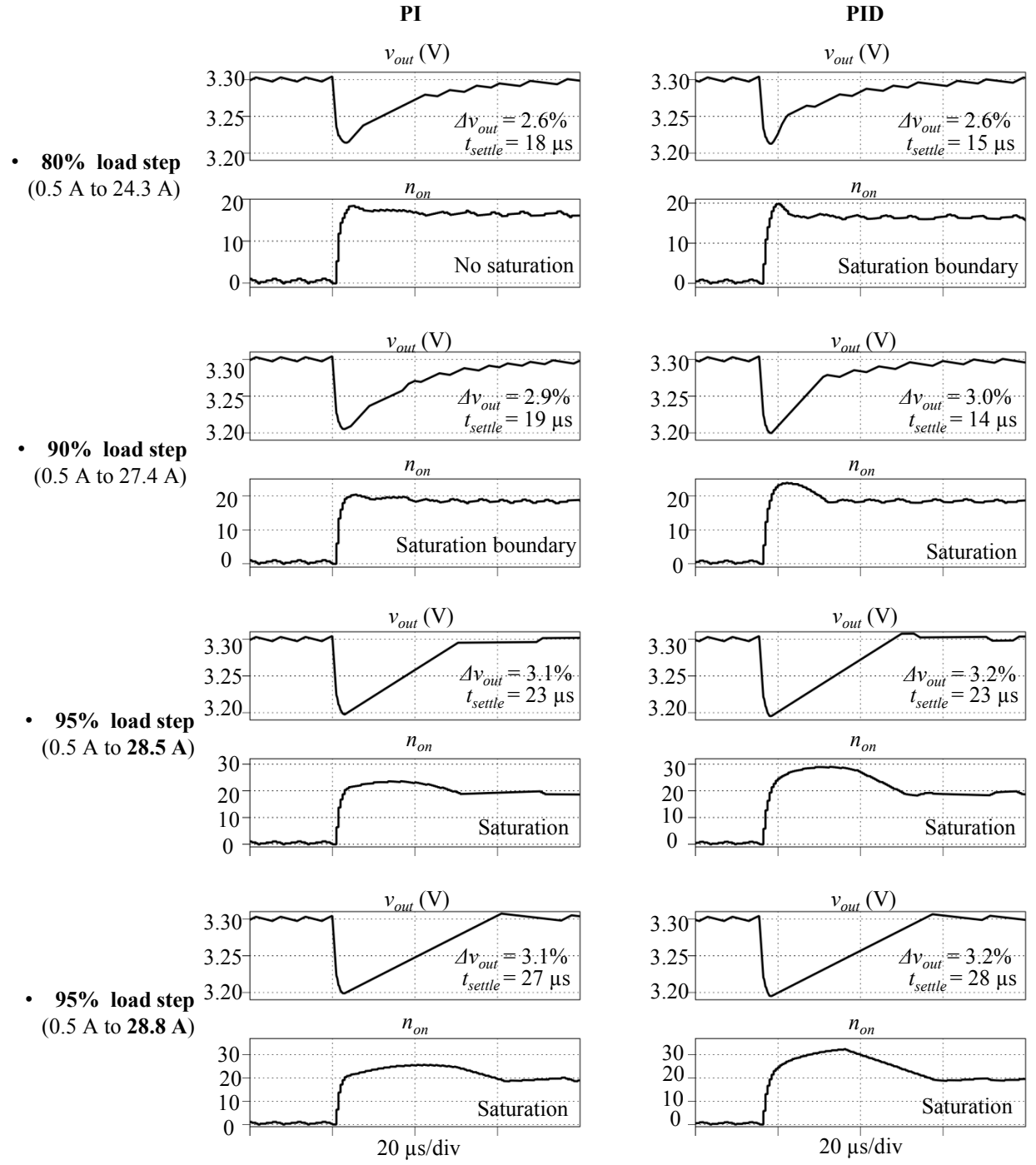


Figure 4.12: Comparison between PI and PID compensators for twenty-module system at different load steps

4.3 Discussions

4.3.1 Output Filter Capacitor Size

For systems based on 5 W modules presented in this thesis, it is shown that when the number of modules in parallel is small, the output capacitor is mainly determined by the output voltage ripple in steady state, not the voltage change during step-load transients. The output capacitance of 11.7 μF per 1 A load guarantees a voltage change of less than 5% at 100% step-load transient. However, at $N = 2$, such capacitance value yields large worst-case voltage ripple, $\pm 1.5\%$ of the nominal voltage. In order to meet a stricter voltage ripple requirement of less than $\pm 0.5\%$, a system of six or more modules is needed, or a larger output filter capacitor must be used.

Regarding step-load response only, a synchronous buck converter with digital PID voltage controller is considered in comparison with the proposed on/off controlled N-module active-clamp LLC converter. The purpose of the comparison is to evaluate the proposed architecture and the control method in terms of capacitor size and transient performance, using the buck converter as a reference. Fig. 4.13 shows the voltage control loop of a synchronous buck converter. The ADC's quantization, delay and sampling rate are the same as in the on/off controlled modular converter. The digital compensator, PWM and power circuit are set up and simulated in Matlab/Simulink with PLECS library. The duty cycle is updated right before the beginning of each switching cycle.

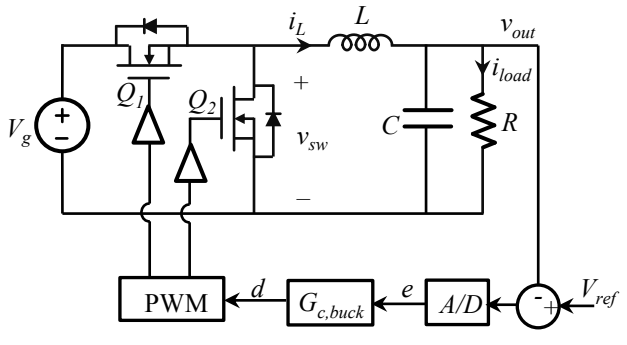


Figure 4.13: Control loop diagram for synchronous buck converter

Corresponding to any N-module active-clamp LLC system, an ideal buck converter is designed at the same power rating, converting 24 V input to 3.3 V output voltage, and operating at the same 1 MHz switching frequency. The design specifications are: ±0.5% output voltage ripple and ±5% transient voltage change, and compensator's cross-over frequency of 100 kHz. Following the same design process as in [109], the LC output filter is determined for the given design requirements.

First of all, given the 100 kHz cross-over frequency, the inductance L is chosen such that the PID compensator operates at the linear/saturation boundary upon large step load. The inductor value is found to be $L = 3.6/N$ (μH), which corresponds to ±25% inductor current ripple at full load. The smallest output capacitance is then derived as a function of N: $C = 13.5N$ (μF). To maintain the output voltage within 5% of the nominal value during step-load transients, the PI on/off control of the N-module converter requires 30% larger output capacitance than the PID voltage control of a single-phase buck converter. This is due to the fact that when turned on, each active-clamp LLC module takes the first switching cycle to reach its nominal output current. During that time the output capacitor keeps being charged or discharged.

The step-load settling time can be compared between the proposed system and a voltage-controlled buck converter that uses two different output capacitance values: the smallest design value $C = 13.5N$ (μF), and the same value as in the N-module active-clamp LLC converter $C = 17.5N$ (μF).

Corresponding to each output filter size, the control-to-output transfer function is found and a PID compensator $G_{c,buck}$ can be designed [5]. The designed compensator, taking into account computational and sensing delay, has a phase margin of 45° at 100 kHz cross-over frequency. An example is shown in Fig. 4.14 for a 10 W buck converter's step-load response. When the output current steps down from 95% to 5% load, the duty cycle saturates and the inductor current i_L ramps down quickly to zero (Fig. 4.14a). When the output current steps down from 95% to 5% load, the duty cycle reaches zero in the next switching cycle, allowing the inductor current i_L to ramp down quickly to zero (Fig. 4.14a). This proves that the compensator operates at the linear/saturation boundary. When the output current steps up from 5% to 95% load, the controller increases i_L to

no more than 50% of the 3 A rating (Fig. 4.14b). In practice, the inductor should be designed properly so that it is not saturated at a high overshooting current.

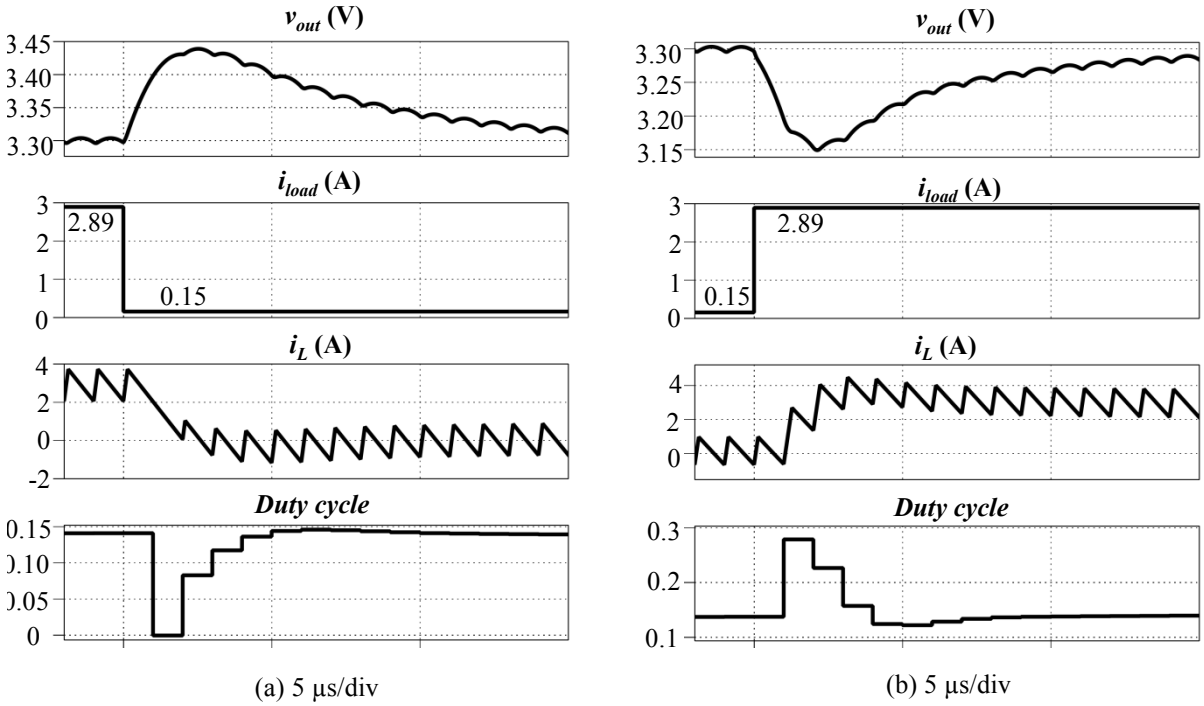


Figure 4.14: Simulation results of 10 W buck converter at (a) 95% to 5% load step down, and (b) 5% to 95% load step up

The performances can be compared in terms of step-load settling time obtained by simulations. Fig. 4.15 compares the settling time of the three configurations at different normalized power ratings P/P_0, where P_0 is the power of one active-clamp LLC module. The value of P/P_0 is also equal to the number of LLC modules in parallel. It is shown that the multi-module active-clamp LLC converter maintains the same settling time at any power rating. When the converter's power is at least 35 W, or $N \geq 7$, it settles the output voltage faster than the synchronous buck converter using the same output capacitance. Compared to the buck converter using the smallest allowed capacitance, the proposed system settles faster when the power level is at least 30 W, or $N \geq 6$. Note that the PI on/off controller's gain is scaled with the number of modules N. At larger N, the computational delay may be longer, but it is still insignificant compared to the dominant delay of

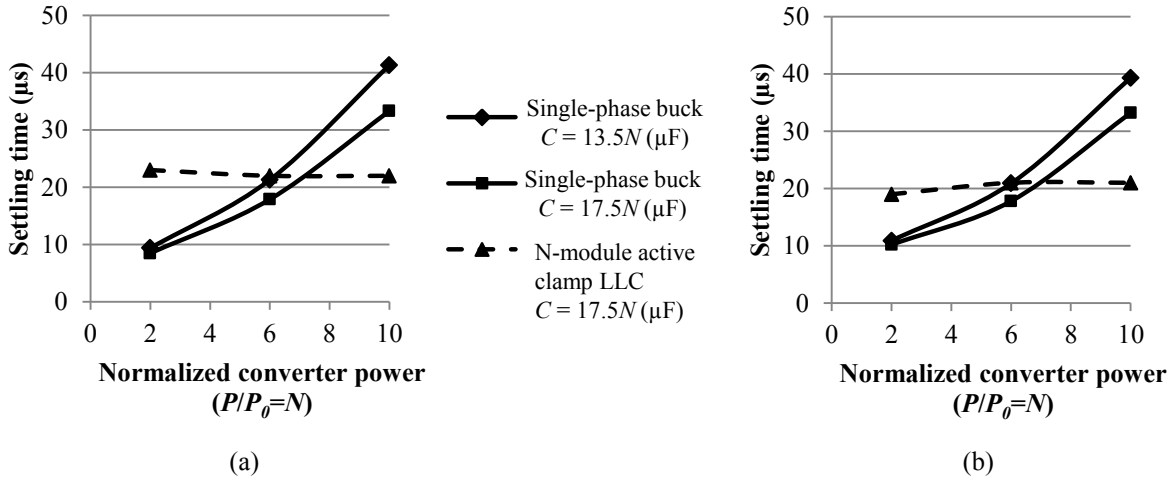


Figure 4.15: Settling time of synchronous buck and multi-module active-clamp LLC converters at different power ratings when: (a) load steps up from 5% to 95%, and (b) load steps down from 95% to 5%

the ADC. Therefore, the controller's performance will not be affected much.

There are other considerations for the comparison. It is well understood that an interleaving multi-phase buck converter with phase-shedding control presents advantages, especially at higher current levels [21–23]. Furthermore, due to current ripple cancellation, a smaller inductance can be used, which helps improve transient responses. A time-optimal controller for the buck converter could also be applied to obtain a faster settling time [110]. Nevertheless, the comparison is focused on a single-phase buck converter with conventional linear PID controller as a basic reference case. This comparison can serve as a starting point for more detailed comparative evaluations against multi-phase buck and other approaches suitable for point-of-load applications.

In summary, for systems containing at least six 5 W active-lamp LLC modules, the proposed on/off control method meets the strict voltage ripple requirement for POL applications. Compared to a single-phase buck converter with PID voltage controller, the proposed system requires 30% more output capacitance to maintain the same transient voltage deviation. This gap can be reduced by increasing the switching frequency of the active-clamp LLC modules since the modules take less time to reach steady state. In that case, the converter needs to be carefully designed to obtain high efficiency. When the single-phase buck converter uses the same output capacitance as the

multi-module active-clamp LLC converter, the LLC converter shows a competitively fast step-load transient response at an output current of 11 A or higher.

4.3.2 Hysteresis vs. fixed-frequency on/off control

Adding hysteresis to the n_{on} quantizer varies the on/off PWM frequency. This is helpful when the PWM time resolution is low and when there are few modules in parallel. In the two-module system example, the PWM time resolution is 500 ns. It limits the PWM duty cycle resolution over all load range, especially when the PWM is fixed at 200 kHz to maintain acceptable output voltage ripple. The fixed PWM frequency can only be reduced by increasing the output capacitor, which is not desirable. Hysteresis control yields two degrees of freedom, module's on time and PWM switching period. Therefore, it helps to minimize the duty cycle resolution issue at various loads. The fixed-frequency on/off control method is suitable when the PWM frequency is much smaller than the output voltage ripple frequency as in [75,76], or in systems consisting of more active-clamp LLC modules, allowing a larger output capacitor.

4.4 Summary

This chapter presents methods to model and design an on/off controller for a multiple-parallel-module dc-dc system using active-clamp LLC resonant converter modules. From the individual converter's averaged model, a system's first-order model is developed to assist the controller design. The standard frequency-domain techniques are proposed to design the system control loop, using the number of on modules as the control variable.

The models and the on/off control method are verified by experiments on a prototype containing two 1 MHz, 24 V-to-3.3 V, 5 W active-clamp LLC modules. Steady-state and transient responses are evaluated experimentally in the two-module system, and by simulations for a larger twenty-module system. The results show that, in a point-of-load dc-dc system consisting of at least six 1 MHz, 24 V-to-3.3 V, 5 W LLC modules operating in parallel, a standard PI or PID compensator can regulate the output voltage in steady state. However, compared to a synchronous buck

converter with PID voltage controller, the proposed system requires 30% more output capacitor in order to maintain the same transient voltage deviation (less than 5% of the referenced value). For systems rated at 11 A or more, the proposed architecture and control method perform with competitively fast step-load transient responses, compared to the voltage-controlled buck converter using the same output capacitor.

In the studied on/off controller, it is important to note the saturation effect of the control variable, which may limit the settling time upon large step-load transients. In the twenty-module system example, the PID controller can tolerate saturation of the control variable, and has a faster step-load response than the PI controller.

Chapter 5

Integration of Secondary-Side Power MOSFETs and Gate Drivers

In the active clamp LLC resonant converter, the voltage stress across secondary-side devices is limited to twice the output voltage. This feature provides an opportunity to integrate these power devices and control circuitry in a low-voltage CMOS process. An initial step to approach the integration goal is presented in this chapter. Section 5.1 introduces the methods to design a custom integrated circuit (IC) consisting of all four secondary-side MOSFETs and their gate drivers. Preliminary IC test results are demonstrated in Section 5.2. Section 5.3 summarizes the work presented in this chapter.

5.1 Design Method

The optimization design methods for a high-frequency monolithic buck converter have been discussed in literature [111–113]. The design approach is based on modeling losses in the power stage, and then selecting the device size to optimize efficiency. This section applies a similar method to the active clamp LLC converter, focusing on the secondary-side power stage's efficiency. In order to reduce the converter's complexities in the IC design process, Section 5.1.1 proposes a circuit setup that includes power devices on the secondary side only. Parameter-dependent loss models are derived in Section 5.1.2, leading to the design optimization in Section 5.1.3.

5.1.1 Circuit Setup

At the first glance, the operation of secondary-side power devices is in coordination with the primary-side devices, and is dependent on the LLC resonant tank including the transformer. This complex dependence may cause difficulties in designing and simulating separately the power stage on the converter's secondary side. However, the fundamental approximation in Section 2.4 suggests that the resonant current on each transformer secondary winding can be approximated as a sinusoidal current with a dc offset, whose values only depend on the output current I_{out}. For example, the current of the winding connected to switches SR_1 and Q_a is approximated to:

$$i_1 \approx I_{out}\left(0.5 + \sin \omega_s t\right), \tag{5.1}$$

where ω_s is the angular switching frequency of the converter.

Fig.5.1 illustrates the converter circuit diagram on the output side, and typical waveforms of the circuit branch containing the aforementioned winding in connection with SR_1 and Q_a.

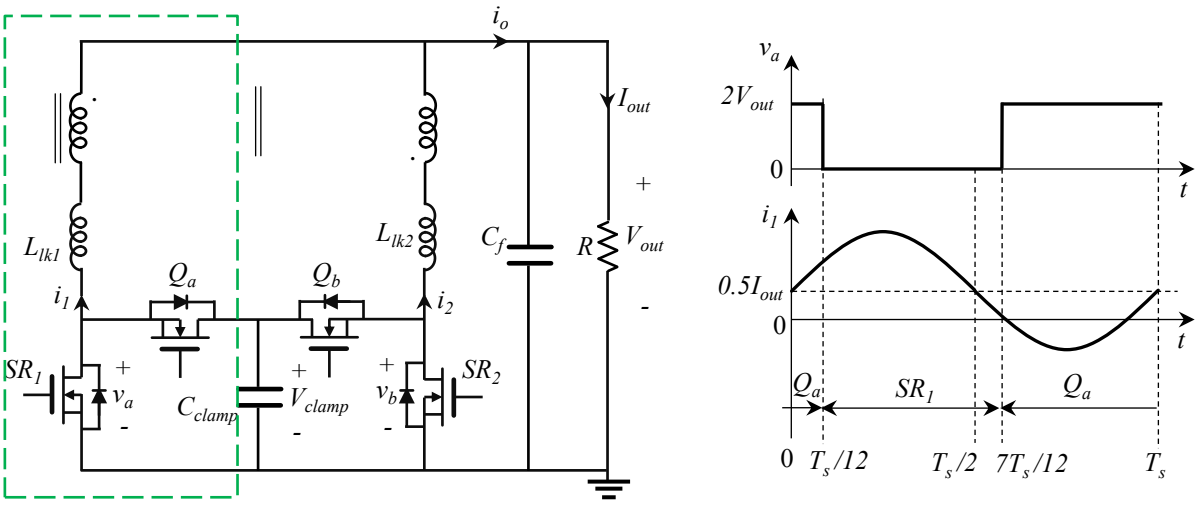


Figure 5.1: Review of converter circuit diagram on the output side, and typical waveforms of the highlighted secondary-side circuit

Assume the clamp and output capacitors are large enough to maintain insignificant voltage ripples, the switching node voltage v_a in steady state is a 50%-duty-cycle square wave, whose value alternates between zero and twice the output voltage V_{out}. The voltage rising edge happens when

SR_1 is turned off at zero current. By setting i_1 to zero in (5.1), the voltage v_a is found to lag the current i_1 by a duration of $7T_s/12$.

Since the current and switching node voltage of this secondary-side branch are approximately independent from the rest of the converter, a circuit setup is proposed to assist the IC design process, as shown in Fig. 5.2.

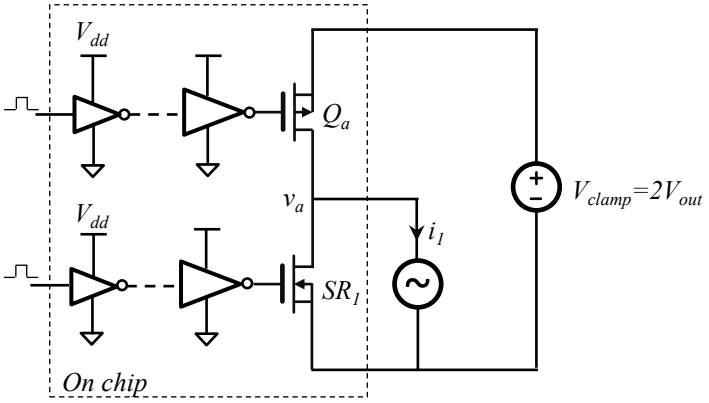


Figure 5.2: Proposed circuit setup to assist the design of secondary-side switches and their gate drivers

In this circuit setup, the ideal ac current sink has a value determined by (5.1), and the ideal voltage source supplies a dc voltage of $V_{clamp} = 2V_{out}$. The gate driver is a series combination of inverters that become larger near the power device. The gate driver supply voltage V_{dd} is provided by a linear regulator from outside the chip. The gate driver input signals control the switches SR_1 and Q_a to generate a switching node voltage similar to v_a waveform in a full converter, as illustrated in Fig 5.1. Because the currents and voltages on two secondary sides are identical but with 180° phase shift, this setup can be applied for the other secondary-side circuitry containing switches SR_2 and Q_b.

5.1.2 Parameter-Dependent Loss Modeling

In this section, conduction and gate driver loss models are derived for each pair of rectifier and clamp devices. Because both devices are ZVS turned on and the rectifier devices are ZCS

turned off, the switching loss is minimized and can be neglected in the model. The power losses are modeled as functions of the device gate channel area, which is determined by the channel length and width. For designs using Texas Instrument's 5V-CMOS process, the length is kept constant at its minimum value of 600 nm, and losses become dependent on the channel width only.

5.1.2.1 Conduction Loss

The RMS currents of the PMOS and NMOS devices can be derived from (5.1), and their total conduction loss is calculated as:

$$P_{cond} = I_{out}^2 \left(0.1 R_{on,P} + 0.65 R_{on,N}\right), \tag{5.2}$$

where $R_{on,P}$ and $R_{on,N}$ are the on resistance of the PMOS and NMOS, respectively. According to [113], a MOSFET's on resistance is a function of gate driver voltage V_{dd} and channel width W:

$$R_{on} = \frac{\bar{K}}{W(V_{dd} - T_{th})^{\alpha}}, \tag{5.3}$$

where V_{th} is the gate threshold voltage. Note that this model does not include the parasitic resistance of metal traces and bond wires. At a constant V_{dd}, the on resistance expression is reduced to:

$$R_{on} = \frac{K}{W}, \tag{5.4}$$

and the conduction loss is expressed as:

$$P_{cond} = I_{out}^2 \left(0.1 \frac{K_P}{W_P} + 0.65 \frac{K_N}{W_N}\right), \tag{5.5}$$

The coefficient K can be found by curve-fitting (5.4) into a data set of R_{on} vs. W obtained from simulations. Fig. 5.3 shows the simulation setups and plots the collected data for both types of MOSFETs. The coefficients are found to be $K_N = 2464\ \Omega.\mu$m for NMOS, and $K_P = 9503\ \Omega.\mu$m for PMOS, both obtained at 3 V gate driver supply voltage.

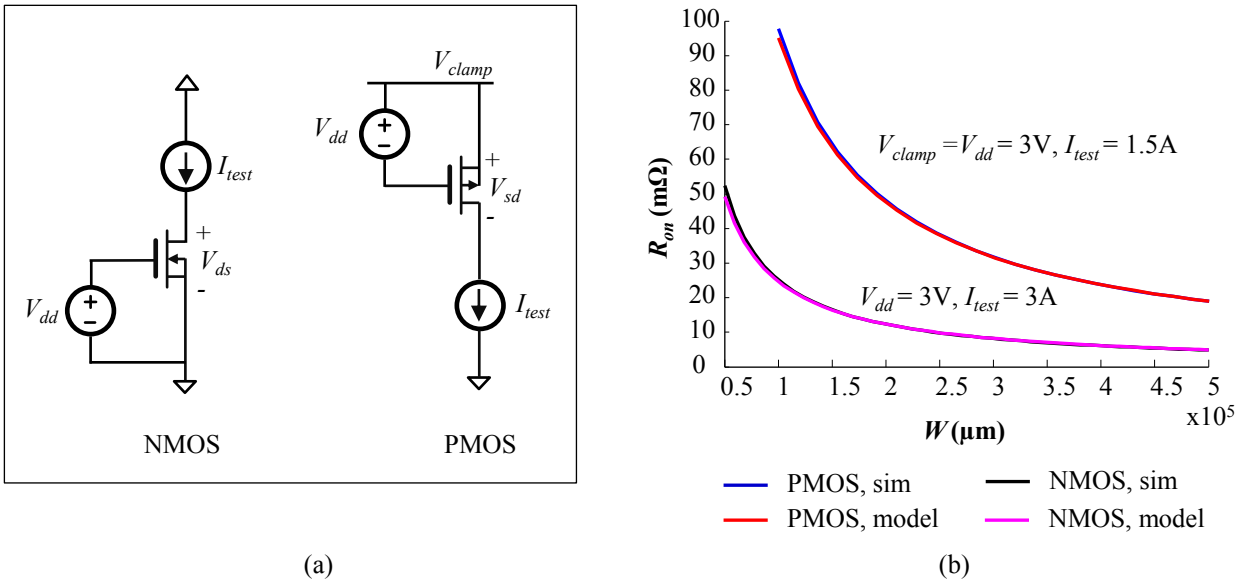


Figure 5.3: (a) Simulation setups to find R_{on} as a function of channel width W, and (b) data obtained from simulation and model curve-fitting

5.1.2.2 Gate Driver Loss

The gate driver is a chain of inverters with a tapering factor tf, as shown in Fig. 5.4.

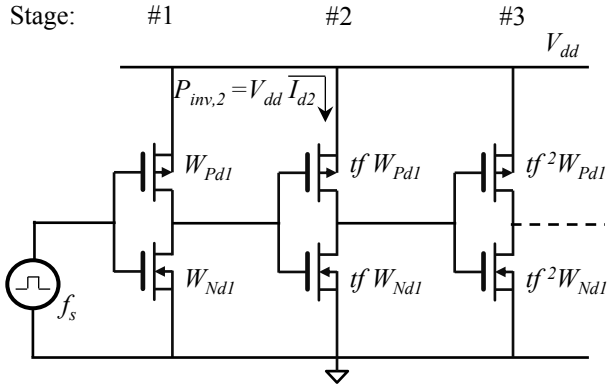


Figure 5.4: Gate driver schematic consisting of inverter chain

The first stage in the chain is a small inverter that can be charged or discharged quickly by a high-frequency logic source. The next stages are increasingly scaled by the factor tf until a desirable current is obtained in the last stage to sufficiently charge and discharge the gate of a

power MOSFET. The power dissipated in an i^{th} stage is modeled as:

$$P_{inv,i} = f_s V_{dd}^2 (W_{Pdi} + W_{Ndi})(C_x + tfC_y), \tag{5.6}$$

where C_x is the inverter's output capacitance per unit length, C_y is the input capacitance per unit length, W_{Pdi} and W_{Ndi} are the channel widths of the PMOS and NMOS in the i^{th} inverter, respectively. The expression represents the inverter's power loss from charging its output capacitor and the input capacitor of the following stage at a rate of f_s. Simulations are performed for the first three stages to obtain power loss P_{inv2} of the middle inverter at different tapering factors. The capacitor coefficients are extracted from curve-fitting (5.6) into the obtained data: $C_x = 1.00$ fF/μm and $C_y = 1.78$ fF/μm. Fig. 5.5 demonstrates that the loss model matches well with the simulation data.

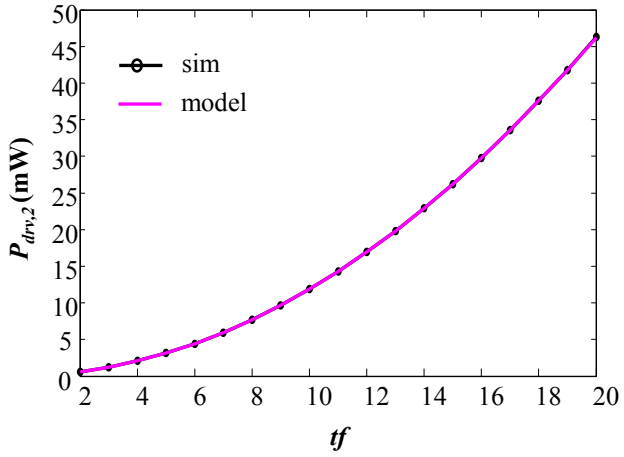


Figure 5.5: Power loss P_{inv2} of the middle inverter in a three-inverter chain at different tapering factors. The simulation parameters are: $W_{Pd1} = 500$ μm, $W_{Nd1} = 200$ μm, $f_s = 10$ MHz and $V_{dd} = 3$ V.

For an unloaded gate driver consisting of $(m+1)$ inverters, the total loss can be estimated by setting m to infinity [113]:

$$\begin{aligned} P_{drv,noload} &= \lim_{m\to\infty} f_s V_{dd}^2 (W_{Pd,last} + W_{Nd,last}) \left[C_x + (C_x + tfC_y) \frac{1 - tf^{-m}}{tf - 1} \right] \\ &= f_s V_{dd}^2 (W_{Pd,last} + W_{Nd,last})(C_y + C_x) \frac{tf}{tf - 1}, \end{aligned} \tag{5.7}$$

where $W_{Pd,last}$ and $W_{Nd,last}$ are the last inverter's PMOS and NMOS channel widths, respectively.

When the gate drivers are connected to the rectifier and clamp devices, the complete diagram of the integrated circuit is shown in Fig. 5.6.

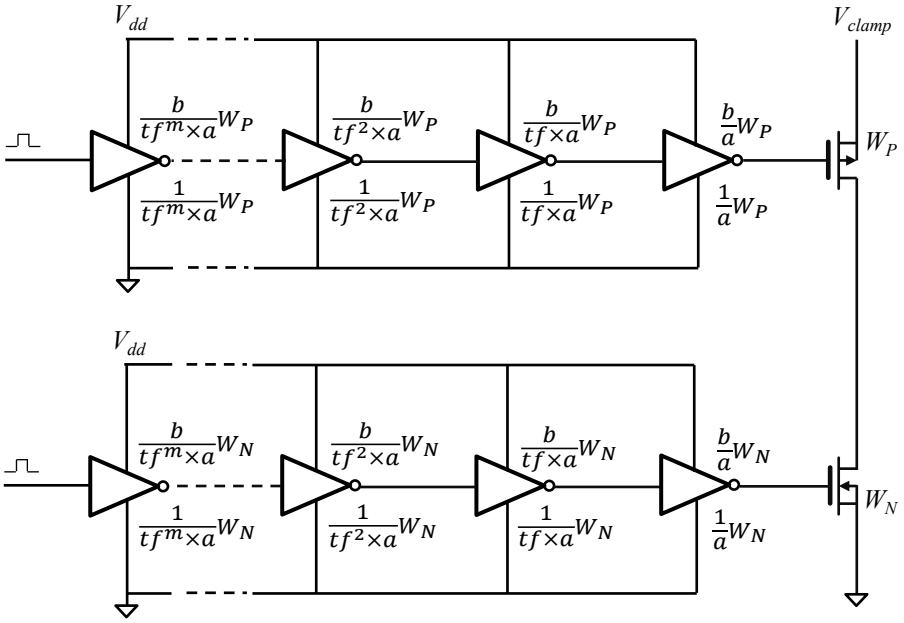


Figure 5.6: Circuit diagram of integrated power devices and their gate drivers

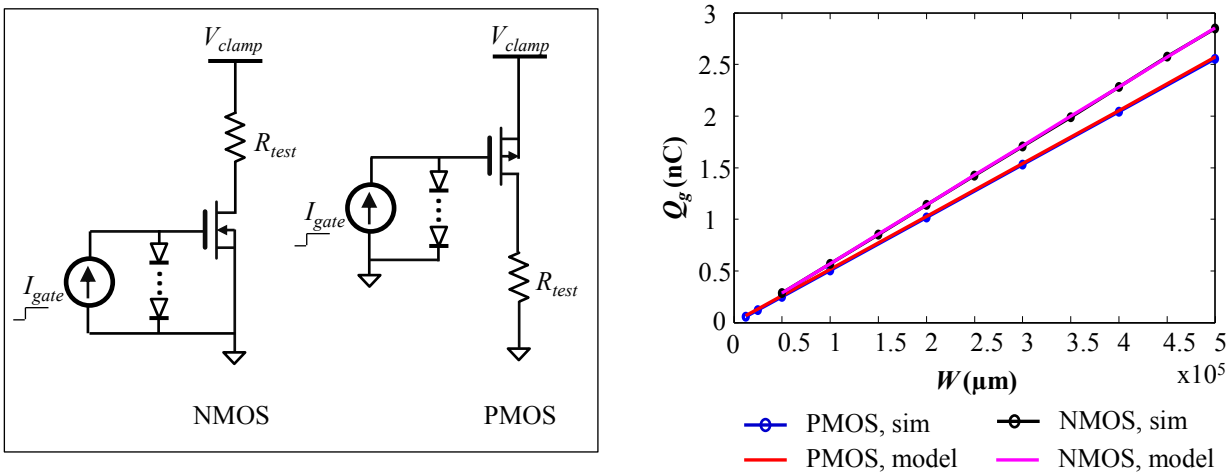
The design parameters shown in the figure are summarized as follows:

- W_P: channel width of power PMOS
- W_N: channel width of power NMOS
- a: scale factor from the power MOSFET to the NMOS in the last inverter stage
- b: ratio of PMOS channel width and NMOS channel width in the same inverter (W_{Pdi}/W_{Ndi})
- tf: tapering factor of the inverter chain in a gate driver circuit

The gate driver loss of this circuit needs to include the power loss due to each power device's gate charge Q_g:

$$P_g = f_s V_{dd} Q_g = f_s V_{dd} W Q, \tag{5.8}$$

where Q is the gate charge per unit length. The Q coefficients for both power PMOS and NMOS can be derived from the simulation setups shown in Fig. 5.7a.



(a) (b)

Figure 5.7: (a) Simulation setups to find gate charge Q_g as a function of channel width W, and (b) data obtained from simulation and model curve-fitting, using $I_{gate} = 100$ mA, $R_{test} = 1.5\ \Omega$ and $V_{dd} = 3$ V

In simulation, the gate is charged by a constant current source, and the series of ideal diodes are used to limit the maximum gate voltage. The total gate charge Q_g is the product of I_{gate} and the time period it takes for gate voltage to rise from zero to V_{dd}. The coefficient Q is found as the ratio between gate charge and channel width: $Q_P = 5.14$ fF/μm for PMOS and $Q_N = 5.71$ fF/μm for NMOS. Fig. 5.7b demonstrates that the model matches well with simulation results.

Finally, the total gate driver loss is calculated as the sum of power losses in the unloaded gate drivers and losses from power devices' gate charge:

$$P_{drv} = f_s V_{dd}^2 (W_P + W_N)(C_x + C_y)\frac{tf(1+b)}{a(tf-1)} + f_s V_{dd}(Q_P W_P + Q_N W_N). \tag{5.9}$$

5.1.3 Design Optimization

The design specifications are described as follows: switching frequency $f_s = 10$ MHz, output current $I_{out} = 1$ A $\rightarrow 5$ A, output voltage $V_{out} = 1.5$ V, clamp voltage $V_{clamp} = 3$ V, and gate driver supply voltage $V_{dd} = 3$ V.

For an IC containing two power NMOS(s), two power PMOS(s) and their corresponding gate drivers, the total loss is:

$$P_{loss} = 2(P_{cond} + P_{drv}), \tag{5.10}$$

where the expressions for P_{cond} and P_{drv} are given in (5.5) and (5.9), respectively. The design goal is to find a set of parameters a, b, tf, W_P and W_N that minimizes the IC total loss.

Scale factor b: This parameter is chosen to obtain the same falling and rising time at the inverter output. For this design, $b = 2.5$.

Scale factors a and tf: The partial derivative terms $\partial P_{loss}/\partial a$ and $\partial P_{loss}/\partial tf$ are found to be negative. This suggests that at higher scale factors, the loss - specifically the gate driver loss is lower. Fig. 5.8 plots the gate driver loss normalized by the power device channel width at different values of a and tf.

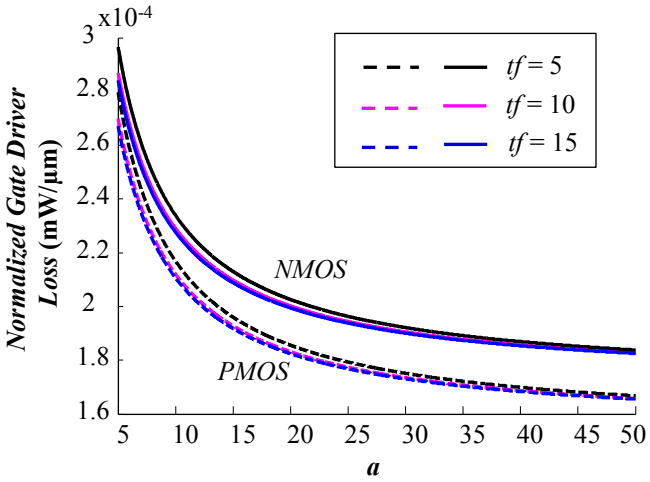


Figure 5.8: Gate driver loss normalized by power device channel width at different values of a and tf

It is found that the normalized gate driver loss for each power device does not change significantly at $tf \geq 10$ and $a \geq 20$. Note that for hard-switching topologies, the switching loss cannot be neglected and these scale factors need to balance between gate driver and switching losses [113]. For the studied resonant topology, switching loss is insignificant and there is more freedom to choose a and tf. One design option is $tf = 10$ and $a = 20$.

Power device channel widths W_P and W_N: The partial derivatives of total loss in respect to the PMOS and NMOS channel width are given by:

$$\frac{\partial P_{loss}}{\partial W_P} = 2\left[-0.1 I_{out}^2 \frac{K_P}{W_P^2} + f_s V_{dd} Q_P + f_s V_{dd}^2 (C_x + C_y) \frac{tf(1+b)}{a(tf-1)}\right] \tag{5.11a}$$

$$\frac{\partial P_{loss}}{\partial W_N} = 2\left[-0.65 I_{out}^2 \frac{K_N}{W_N^2} + f_s V_{dd} Q_N + f_s V_{dd}^2 (C_x + C_y) \frac{tf(1+b)}{a(tf-1)}\right] \tag{5.11b}$$

The optimized values of W_P and W_N are found by setting these partial derivative terms to zero. For $tf = 10$, $a = 20$ and $b = 2.5$, the optimized channel widths and total loss are plotted at different output currents, as shown in Fig. 5.9.

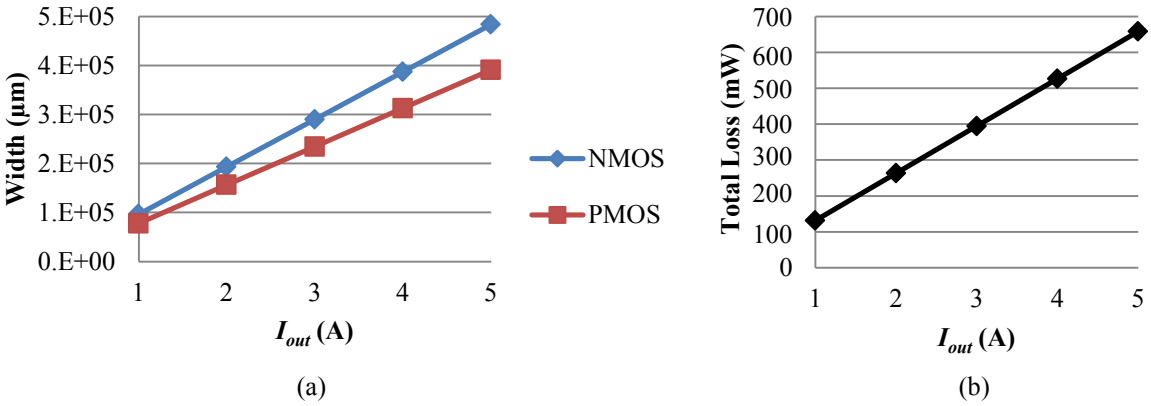


Figure 5.9: (a) Optimized channel widths and (b) total loss at different output currents

For all output current values, the best efficiency of the IC is 92%. The design is chosen for 3 A output current, corresponding to $W_P = 469 \times 500$ μm and $W_N = 580 \times 500$ μm, where 500 μm is the maximum single channel length allowed by the process. The 3 A design's loss budget obtained from simulation and model are demonstrated in Fig. 5.10.

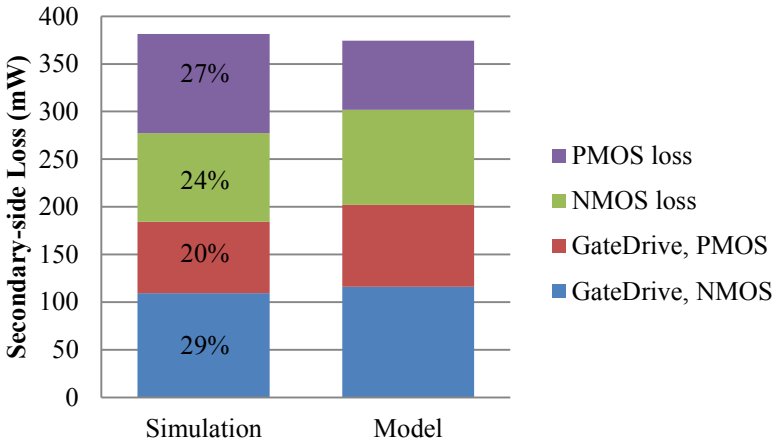


Figure 5.10: Loss budget of optimized design at 3 A output current

Compared to simulation results, the model does not cover about 30 mW switching loss of the two PMOS's, mainly caused by the non-ZCS turn off. However, this does not affect the overall efficiency prediction. Details on the IC layout and the chip package can be found in Appendix C.

5.2 Test Results

The IC is tested using two different setups. The first test is conveniently done as a buck converter operating at the continuous-conduction-mode/discontinuous-conduction-mode (CCM/DCM) boundary. After the basic functions of the IC are verified in this first test, the next test is performed on an active-clamp LLC converter.

5.2.1 Test Results on CCM/DCM Buck Converter

This section presents a quick method to test the IC without designing an active-clamp LLC converter. By noticing that the design circuit setup in Section 5.1.1 has a similar structure of a buck converter, each PMOS-NMOS pair of the IC can be tested as a buck converter, as shown in Fig. 5.11.

In order to replicate the high current ripple and ZCS-turn-off of rectifier device, the buck converter is designed to operate at the CCM/DCM boundary with 50% duty cycle. At 10 MHz

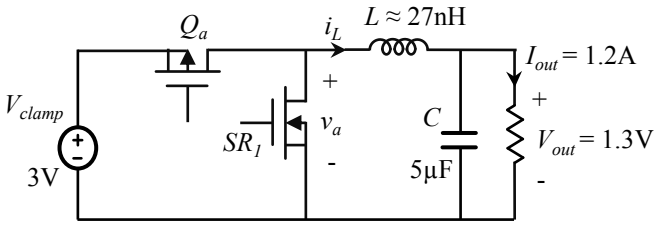


Figure 5.11: IC test setup for a 10 MHz buck converter

switching frequency, the iductor L simply consists of the PCB trace and current measurement loop. Due to the current limit of the PMOS device, the buck converter operates at 3 V input voltage, 1.3 V output voltage, 1.2 A load current and the gate driver power supply votlage is 3.3 V. Fig. 5.12 shows the experimental waveforms of the inductor current i_L, switching node votlage v_s and clamp voltage v_{clamp} right across the IC terminals.

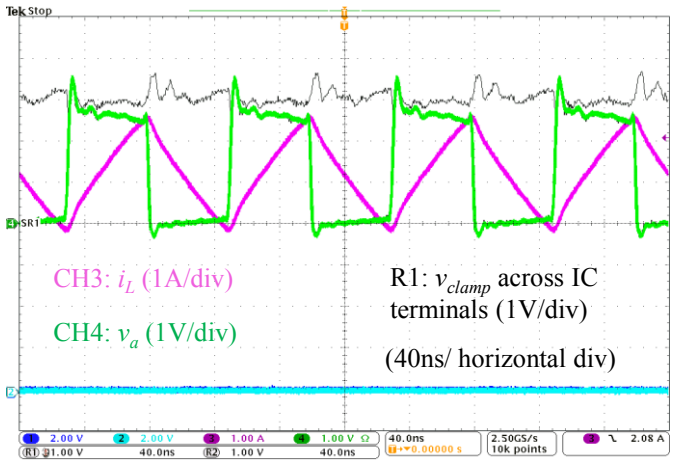


Figure 5.12: IC test results for the 10 MHz buck converter

Although the devices perform with fast switching at 10 MHz and can conduct relatively high current, the converter's efficiency is 71%, lower than expected. While the four gate drivers draw an average current of 65 mA, in agreement with the design model, dc measurements show the device on resistances significantly higher than expected. The additional resistance is caused by bond wires and internal metal layers, which were not included in the model. Such high on resistance explains

why the converter efficiency is lower than predicted. A comparison between the model and the measurements is summarized in Table. 5.1.

Table 5.1: Comparison between IC model and measurements

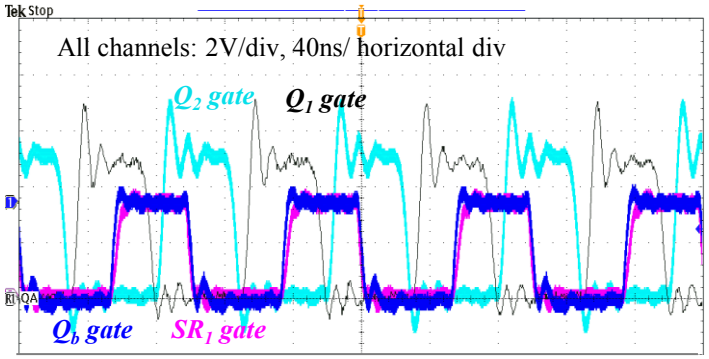
Parameter	Model	Measurement	Note
Gate driver supply current (mA)	57	65	$f_s = 10$ MHz
PMOS on resistance (mΩ)	40	150	$V_{sg} = 3$ V, $I_d = 1$ A
NMOS on resistance (mΩ)	8	75	$V_{gs} = 3.3$ V, $I_d = 2$ A

5.2.2 Test Results on Active Clamp LLC Conveter

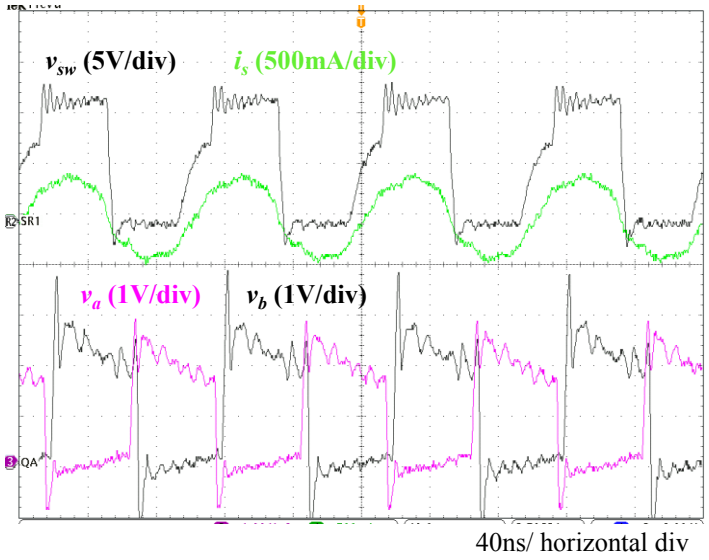
In order to further evaluate the design, the taped-out IC is tested on a 12 V-to-1 V, 1 A , 10 MHz active-clamp LLC converter. Since the actual parasitic resistance of the devices is higher than the designed value, the output current is reduced to 1 A instead of the 3 A design goal. Table 5.2 lists the device part numbers and resonant tank values for the converter under test.

Table 5.2: Components list of the active clamp LLC converter used for IC test

Component	Part number or value
Q_1, Q_2	CSD16301Q2
Gate driver for Q_1, Q_2	EL7158
n	1:5
C_f	0.22 μF
C_{clamp}	0.22 μF
C_s	700 pF
L_s (total of parasitic and external inductance)	230 nH
L_m	1 μH
L_{lk}	35 nH
External resonant inductor	Coilcraft 2222SQ-181 air-core
Transformer magnetic core	Ferroxcube P22/13 pot core
	4F1 material



(a)



(b)

Figure 5.13: Experimental results of IC test on active-clamp LLC converter: (a) devices' gate voltages, and (b) converter's current and voltage waveforms

Fig. 5.13a shows the gate voltages of the primary-side devices Q_1, Q_2 and secondary-side devices Q_b, SR_1. Note that the gate test pins for Q_a and SR_2 are not available on the IC. The converter experimental waveforms are shown in Fig. 5.13b, including input switching node voltage v_{sw}, primary-side resonant current i_s, and voltages v_a, v_b across the rectifier devices. While the secondary-side devices can switch fast at 10 MHz, the primary-side devices have a significantly large output capacitance for this application. The resonant current is not high enough to charge the output capacitor, thus ZVS cannot be obtained. The discrete parts for Q_1 and Q_2 are not designed for such high-frequency application, which limits capabilities of the experimental prototype

to operate at target 10 MHz frequency.

5.3 Summary

This chapter explores the opportunity to integrate power MOSFETs and gate drivers on the secondary side of active clamp LLC resonant converter. This is the first step to reach the ultimate goal of integrating the output-side power stage and control circuitry in the same low-voltage CMOS process. A simple circuit setup is proposed to assist the IC design process, which only requires information of the converter output voltage and output current. The IC components' loss is modeled, including conduction and gate driver loss. Based on the loss model, design parameters are specified and an optimization method is presented to obtain the best IC efficiency.

The taped-out IC is preliminarily tested on a 10 MHz, 3 V-to-1.3 V, 1.2 A buck converter operating in CCM/DCM mode with 50% duty cycle. Although the devices show fast switching behaviors with gate driver loss similar to predictions, the measured device on resistance is significantly higher than expected. This suggests that future designs need to include bond wire resistance model and to pay more attention to the power device layout and internal metal connections. The second test on a 12 V-to-1 V, 1 A, 10 MHz active-clamp LLC converter verifies the IC's fast switching capability. The test shows a challenging requirement for the primary-side devices: they also need to be able to support high-frequency ZVS.

Chapter 6

Conclusions

The design and control of POL converters are challenging due to special requirements imposed by evolving electronic loads: (i) high efficiency over a wide load range, (ii) fast transient response to load steps with high slew rates, and (iii) minimizing output capacitor size while maintaining voltage regulation in transients. With current advances in loads such as microprocessors and memories, the POL converters have to face increasing demands for lower supply voltages, higher load currents, with faster slew rates, and more stringent space, cost, voltage regulation and efficiency requirements. The interleaved buck converter is very popular in POL applications due to its relatively simple structure and well-developed control methods. However, it shows limitations in large step-down applications because of the small duty cycle. The high switching loss hinders opportunities to increase switching frequency, limiting abilities to increase the controller bandwidth and to reduce the size of passive filter components.

This thesis investigates an alternative solution for POL applications based on a multiple-parallel-module architecture with on/off control, where each module is an active clamp LLC resonant module topology. The architecture and the control method allow each module to operate at its maximum efficiency when on, and turn some of them off at light load to maintain high efficiency over wide range of loads. The modular architecture and the proposed control method support fast transient response at large load steps. The active clamp LLC topology features soft-switching and 50 % duty cycle operation of all devices, providing an opportunity to increase the switching frequency to high MHz range, which in turn may lead to smaller size of passive components, and

help further improve the controller speed and the system transient performance.

6.1 Contributions

The thesis contributions are as follows.

6.1.1 Active clamp LLC resonant converter

In terms of the converter topology, the thesis contributions include: (i) proposal of a topology suitable for the multiple-parallel-module architecture in POL applications, (ii) introduction of an active clamp circuit to the original LLC converter, and (iii) development of simplified modeling, analytical and design methods for the proposed topology.

The active clamp LLC resonant converter inherits advantages of the original LLC converter, including: ZVS turn-on of power MOSFETs on the input side (the transformer primary side), ZCS turn-off of power MOSFETs on the output rectifier side (the transformer secondary side), and 50% duty cyle operation of all devices. Besides, the transformer facilitates the converter's large step down ability, while contributing to the resonant tank to enable soft switching.

The active clamp circuit addresses the voltage oscillation across rectifier devices caused by a resonance between the transformer secondary-side leakage inductance and the drain-to-source capacitances of the rectifier MOSFETs. This modification provides two main benefits. First, it limits the voltage stress across all secondary-side devices to approximately twice the output voltage, enabling integration of these devices and control circuitry in a low-voltage CMOS process. With proper IC layout techniques, a power MOSFET rated at a lower voltage performs with smaller on resistance, which makes it suitable for switches carrying high RMS current, such as those in the output side of the LLC converter. In contrast, the rectifier MOSFET in the buck converter conducts high inductor current most of the time, but has to block a high input voltage, which means that opportunities to reduce conduction loss caused by the on resistance are more limited. The other benefit of the active clamp circuitry is that it helps reduce the large ac current in the output capacitor.

Since adding the clamp circuit changes the LLC converter operation, two techniques to analyze the active clamp LLC converter are introduced using a simplified circuit model. The sinusoidal approximation applies the current and voltage fundamental components in the calculations. It provides an intuitive tool to understand the converter characteristics, and helps to derive explicit expressions for output voltage and current. Based on these expressions, a design process is developed to find resonant tank values that allow the converter to operate around its maximum power point at maximum efficiency. Another analytical technique, state plane analysis, is used to to study the converter operation in more detail. The state plane analysis also serves as a more accurate method to verify the results obtained based on sinusoidal approximation. This technique is also used to determine the gate timing sequence so that the converter can reach its steady state within a switching cycle after it is turned on. The analytical and design methods are verified on two 1 MHz, 24 V-to-3.3 V, 6 W experimental prototypes, using PQ and planar magnetic cores, respectively. Both prototypes can obtain efficiency greater than 90%.

Analytical and experimental results shows a special characteristic of the active clamp LLC converter: it behaves similar to a current source, whose value is controlled by a gate timing variable. With the turn-on timing sequence implemented, the converter replicates an ideal current source that can be turned on or off quickly and can reach steady state within a minimum time.

All the aforementioned characteristics of the active clamp LLC converter make it suitable for single or multi-module high-frequency high step-down low-voltage point-of-load applications, where secondary side MOSFETs and control circuitry can be integrated in a low-voltage CMOS process.

6.1.2 On/off Control

On/off control is a relatively simple yet effective method to regulate the output voltage without current sensing. Although this approach has already been suggested for multiple-module systems where each module is approximated as a current source, the work presented in this thesis is the first one to implement the on/off controller in an experimental prototype consisting of more than one module.

In order to assist the on/off controller design and implementation, two converter models are introduced: (i) a high-frequency model based on state plane analysis to determine a gate timing sequence leading to fast module turn-on capability, and (ii) an averaged model to analyze the converter's low-frequency behavior. Based on the module averaged model, an ideal first-order system control-to-output transfer function is derived, where the control variable is the number of on modules.

Standard frequency-domain techniques are applied to design the system control loop, taking into account sensing and computational delay in digital implementation. The on/off control is realized in practice by a quantizer that converts the number of on module into a quantized number. Furthermore, hysteresis is added to the quantizer in order to obtain a practical on/off PWM frequency.

The models and the on/off control method are verified by experiments on prototypes containing one or two 1 MHz, 24 V-to-3.3 V, 5 W active-clamp LLC modules. Steady-state operations and transient responses are evaluated by experiments for the two-module system, and by simulations for larger systems consisting of up to twenty modules. The results show that, in a point-of-load dc-dc system consisting of at least six modules in parallel, a standard PI or PID compensator can regulate the output voltage within $\pm 0.5\%$ ripple in steady state, using a relatively small output capacitor. For systems rated at 11 A or more, the system performs with competitively fast step-load response compared to a synchronous buck converter using a PID voltage controller and the same output capacitance.

The decision to select a PI or PID type is also discussed. It depends on the maximum number of modules and a combined effect of sensing delay and control variable saturation. The PID compensator shows more advantage over the PI at smaller delay or in a larger system. In the twenty-module system example, the PID controller can tolerate saturation of the control variable, and has a faster response than the PI controller upon large step-load transients.

6.1.3 Integration of secondary-side power devices and gate drivers

This work presents design methods and preliminary test results for a 5V-CMOS IC that consists of all secondary-side power devices and their corresponding gate drivers. It is the first step to explore the opportunity to integrate both the output-side power stage and control circuitry in a low-voltage CMOS process.

A simple circuit setup is introduced to assist the design process. It generates a similar circuit operation on the secondary side of the converter, without involving simulation of the input-side power devices or resonant tank components. The only information required from the power stage is the switching frequency, output voltage and output current. Using the circuit setup and detailed power loss model, an optimization design method is presented to obtain the best IC efficiency. The optimized design finds a combination of transistor sizes for both power devices and gate drivers to minimizes the total loss.

A custom IC is designed and fabricated to operate in a 1.5 V output, 4.5 W, 10 MHz active clamp LLC converter. Preliminary tests are performed using a 10 MHz, 3 V-to-1.3 V, 1.2 A buck converter in CCM/DCM mode, which is used to evaluate the IC performance. The IC displays fast switching behaviors with gate driver losses similar to predictions. However, the measured on resistance of power devices is significantly higher than the model dur to parasitic resistances of the bond wire and internal metal connections. The IC test on a 12 V-to-1 V, 1 W, 10 MHz active clamp LLC converter verifies again the IC's fast switching capability.

6.2 Future Work

The work reported in this thesis can ne expanded in a number of directions.

Consideration of input voltage variation: The controller design and implementation in this thesis assume that the input voltage is well regulated by a previous converter stage. In a power distribution system, the bus voltage fed to the POLs may vary depending on the front-end converter design. The input voltage variation can be addressed by modifying the active clamp LLC

converter design to accommodate the worst-case input voltage, and by adding extra input voltage sensing in the control loop. In this modification, the gate timing look-up table and compensator coefficients can be determined according to the sensed input voltage.

Sensorless turn-on sequence: The gate-timing sequence is determined based on the value of resonant capacitor voltage right before the converter is turned on. This requires sensing of the input switching node voltage of each module, which adds additional hardware cost for a large multi-module system. One option to reduce the cost is to implement a turn-on sequence without the need for additional sensing. In fact, the resonant capacitor voltage right at the converter turn-on moment depends on its value when the converter is turned off. This value can be predicted off-line using state plane analysis, given that the controller only allows the converter to turn off at some certain time during its last switching cycle. When the turn-off moment is controlled, the turn-on sequence can be determined without any voltage sensing.

Further IC design improvements: For the next IC design, the loss model needs to consider the conduction loss caused by the resistance of bond wires and internal metal connections. The layout techniques, especially with the metal layers, should be investigated further to obtain the minimum possible parasitic resistance. Moreover, in order to increase the switching frequency, thus reducing the passive component size in the active-clamp LLC converter, a good secondary-side IC design is not the only requirement. Primary-side devices with low output capacitance and suitable gate drivers are also required to obtain ZVS. Emerging GaN devices and integrated circuits may be suitable for this application.

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Appendix A

Planar Magnetics Layouts

A.1 Planar Inductor

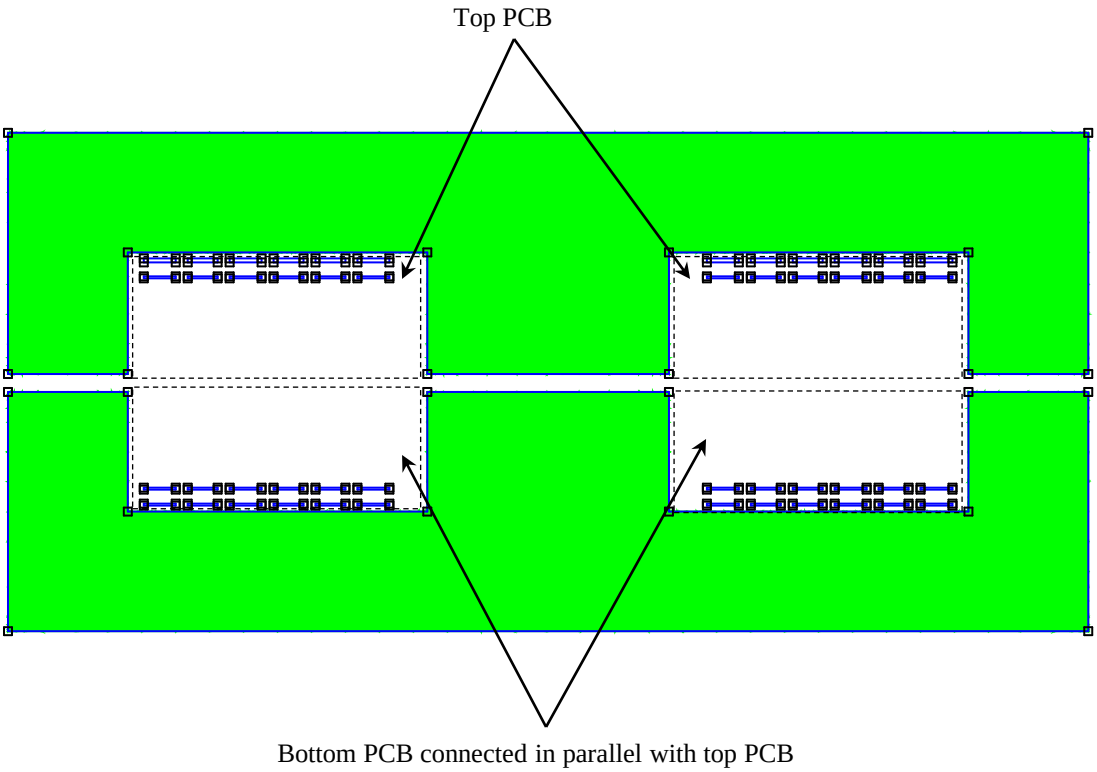


Figure A.1: Cross-sectional view of EE planar inductor. Two four-layer 1-Oz-Cu PCBs are stacked up to allow multiple parallel windings. The four middle layers are not utilized due to fringing effect.

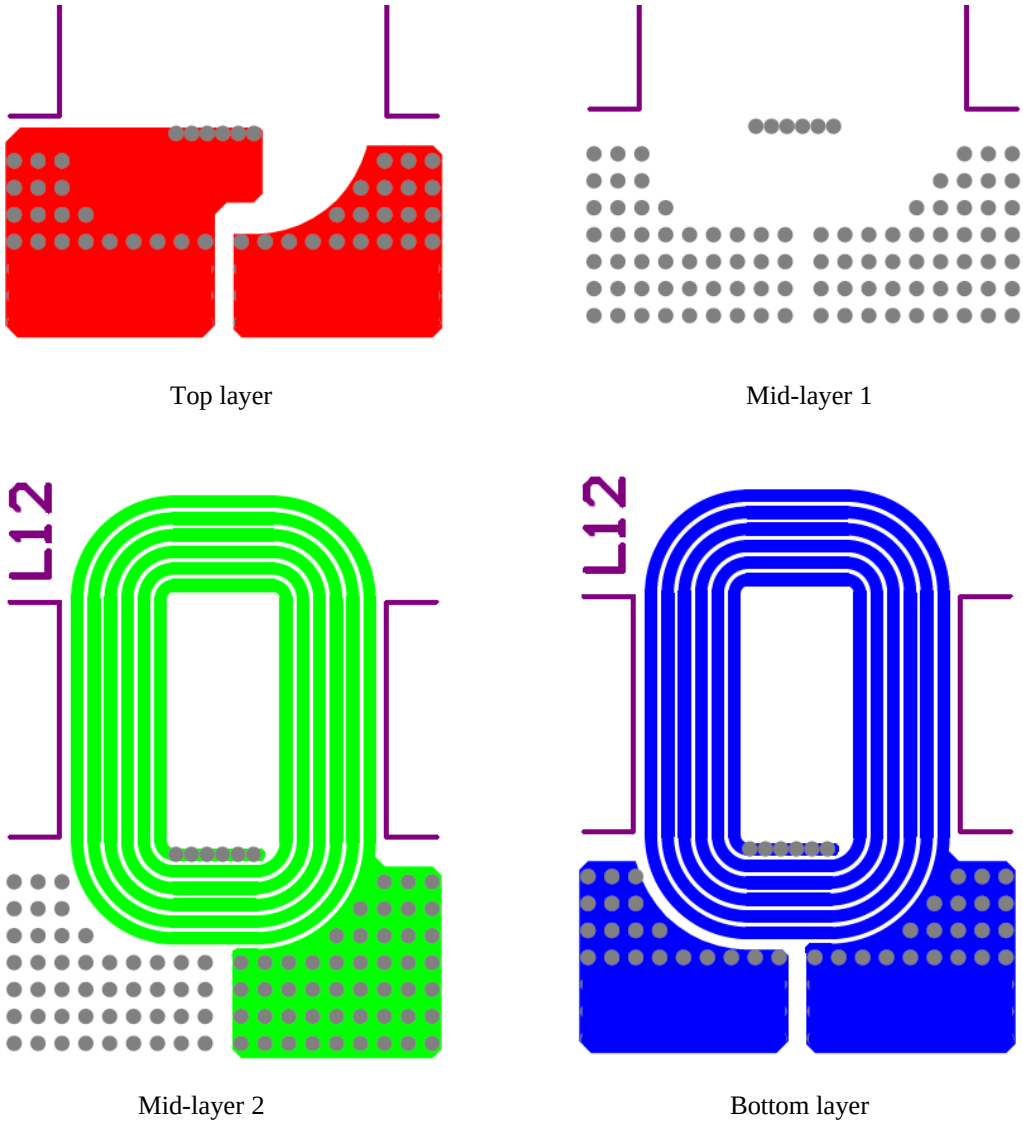


Figure A.2: Layout of the bottom PCB for planar inductor. The top PCB layout is similar with reverse layer order.

A.2 Planar Transformer

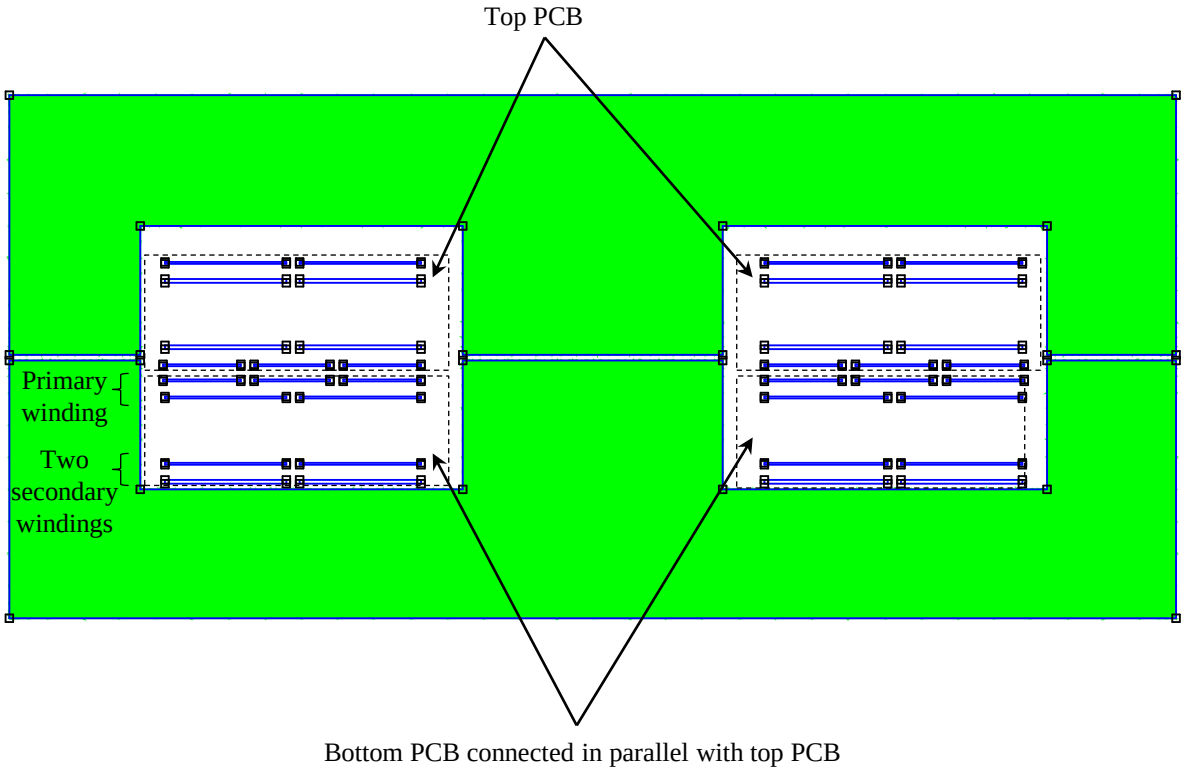
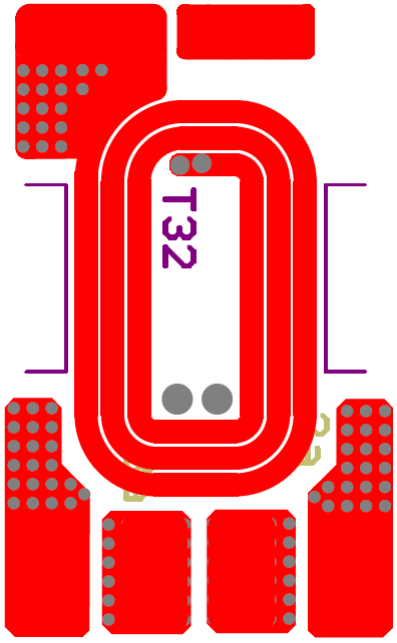
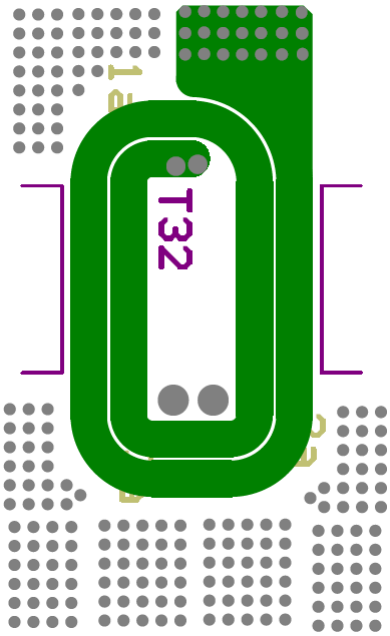


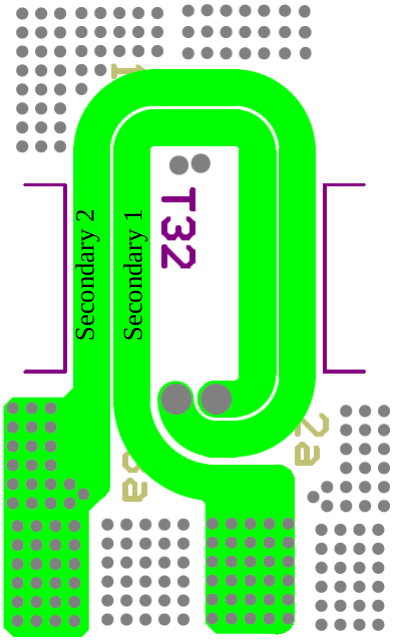
Figure A.3: Cross-sectional view of EE planar transformer. Two four-layer 1-Oz-Cu PCBs are stacked up to allow multiple parallel windings.



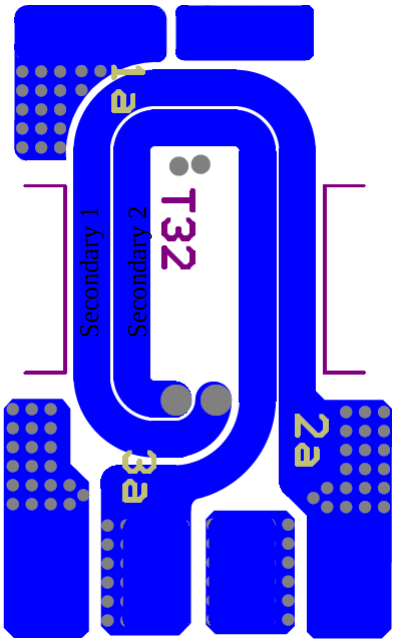
Top layer: three turns of primary winding



Mid-layer 1: two turns in series with top-layer winding



Mid-layer 2: first turn of secondary windings, wound together



Bottom layer: last turn of secondary windings, wound together

Figure A.4: Layout of the bottom PCB for planar transformer. The top PCB layout is similar with reverse layer order.

Appendix B

MOSFET Turn-off Switching Loss

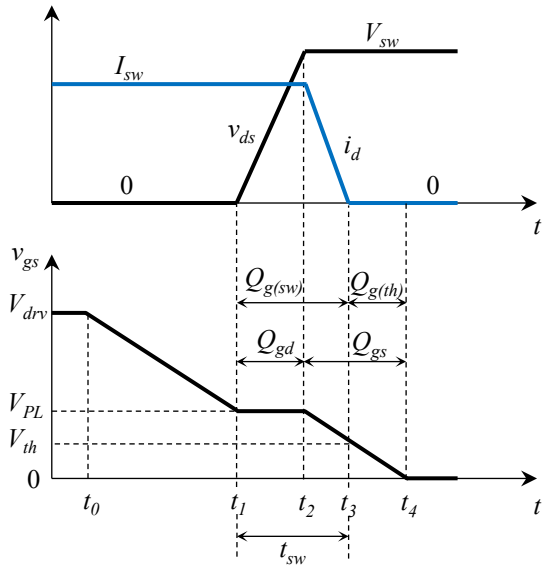


Figure B.1: Simplified waveforms at MOSFET turn-off

Fig. B.1 shows the simplified waveforms of a MOSFET when it is turned off, including the gate-to-source voltage v_{gs}, drain-to-source voltage v_{ds}, and drain current i_d. It is assumed that the turn-off duration is very short compared to the switching period so the MOSFET's current right before turn-off is a constant I_{sw}. The turn-off loss occurs when v_{ds} and i_{ds} do not change instantaneously, which correlates to the gate charge process as follows [26, 27]. At time t_0 the gate driver starts discharging the input capacitor, including the gate-to-source capacitor C_{gs} and gate-to-drain capacitor C_{gd}. When v_{gs} reaches the plateau voltage V_{PL} at t_1, it stays constant and all

the gate current is used to discharge the gate-to-drain capacitor. As a result, v_{ds} starts increasing until reaching its maximum value V_{sw} at t_2. The total gate charge in this duration is Q_{gd}. Now both v_{gs} and i_d start decreasing until the MOSFET is finally turned off at t_3, corresponding to zero drain current and v_{gs} reaching the threshold value V_{th}. The rest of the turn off process from t_3 to t_4 is to totally discharge the gate-to-source capacitor. The total gate charge from t_2 to t_4 is Q_{gs} and from t_3 to t_4 is $Q_{g(th)}$.

As shown in Fig. B.1, the switching loss happens from t_1 to t_3 when i_d and v_{ds} are non-zero. The total gate charge in this duration is given by:

$$Q_{g(sw)} = Q_{gd} + Q_{gs} - Q_{g(th)}. \tag{B.1}$$

Assume that the gate current is constant during this time:

$$I_{drv} = \frac{V_{PL}}{R_{drv} + R_g}, \tag{B.2}$$

where R_{drv} is the gate driver's output resistance and R_g is the gate parasitic resistance, the switching duration from t_1 to t_3 is estimated as:

$$t_{sw} = \frac{Q_{g,(sw)}}{I_{drv}} = \frac{Q_{gd} + Q_{gs} - Q_{g(th)}}{I_{drv}}. \tag{B.3}$$

By assuming linear changes of v_{ds} and i_d, the turn-off switching loss is found:

$$P_{sw} = 0.5 V_{sw} I_{sw} t_{sw} f_s, \tag{B.4}$$

where f_s is the switching frequency. In the active clamp LLC converter, the turn-off process is complicated by the fact that part of the energy during the overlapping of v_{ds} and i_d is useful in charging the drain-to-source capacitor. This calculation, however, is an attempt to approximate the upper bound of the switching loss. It is a convenient method since all the parameters can be found from the device datasheet. Below are the list of device parameters used in the loss calculations in Section 2.7.

Table B.1: Parameters of gate driver EL7104

Parameter	Symbol	Value
Supply voltage (V)	V_{drv}	5
Pull-down resistance (Ω)	R_{drv}	2

Table B.2: Parameters of power MOSFETs

Parameter	Symbol	Value	
		CSD17313Q2	CSD16301Q2
On resistance (mΩ)	R_{on}	32	29
Gate resistance (Ω)	R_g	1.3	1.3
Plateau voltage (V)	V_{PL}	2	2
Gate charge - gate to drain (nC)	Q_{gd}	0.4	0.4
Gate charge - gate to source (nC)	Q_{gs}	0.7	0.6
Gate charge at V_{th} (nC)	$Q_{g(th)}$	0.3	0.3
Gate charge - total (nC)	Q_g	2.1	2.0

Appendix C

Customized IC Layout and Package Information

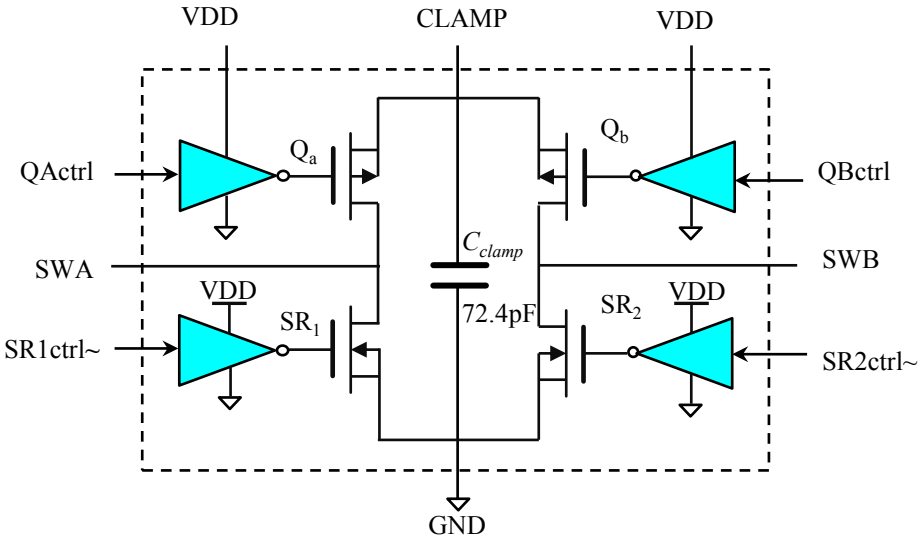


Figure C.1: IC schematic consisting of secondary-side power MOSFETs and gate drivers for the active clamp LLC resonant converter

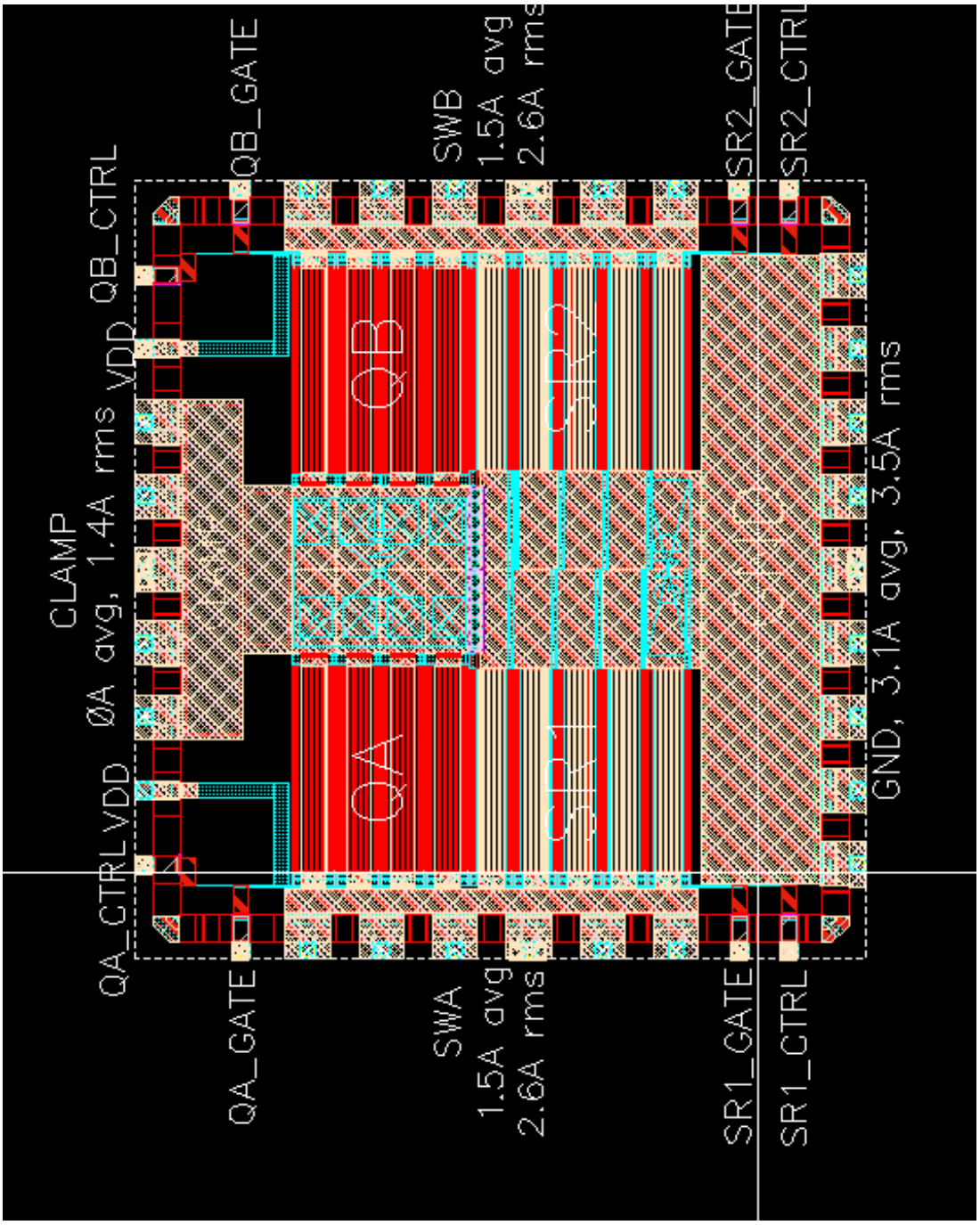


Figure C.2: Complete IC layout including active components and pad ring

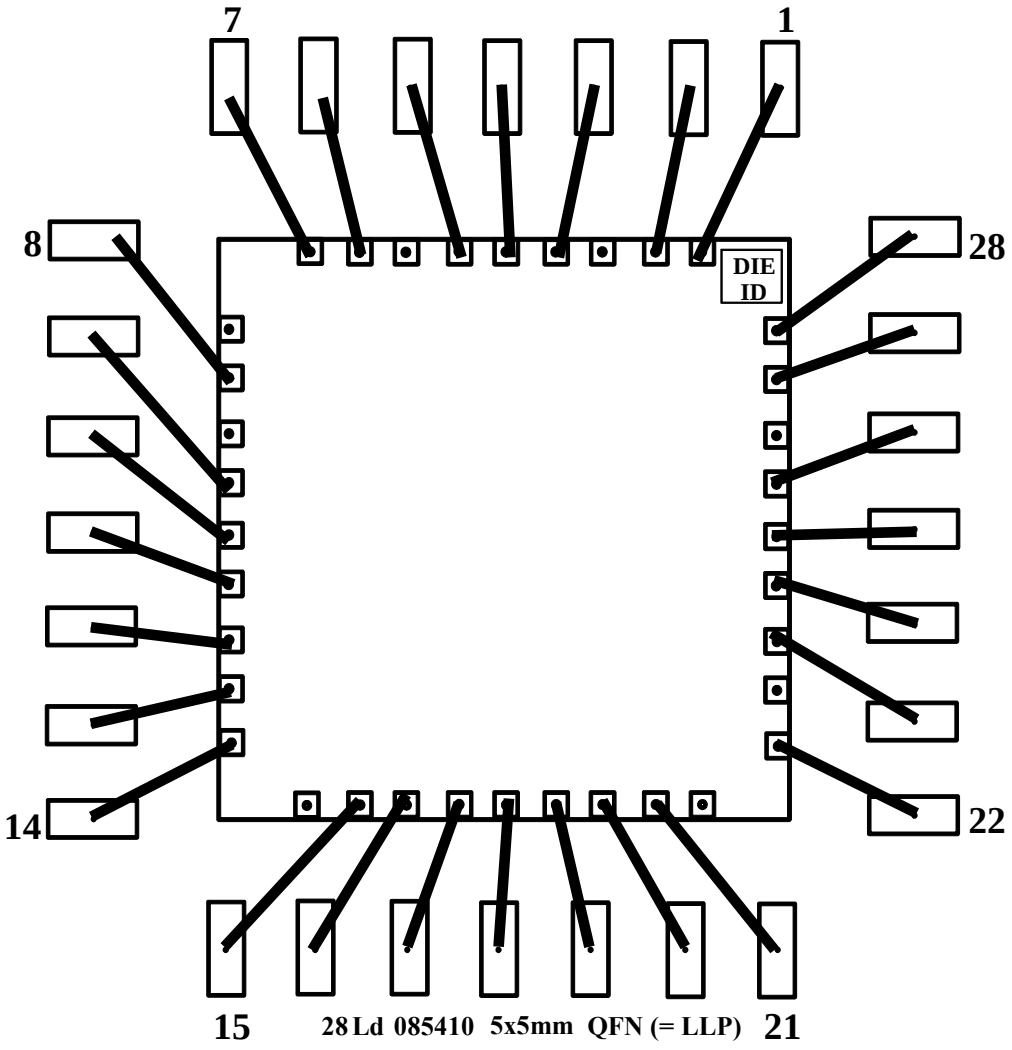


Figure C.3: Bonding diagram and package information