Low Profile, High Power Density and High Efficiency DC-DC Converters

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A thesis submitted to the

Faculty of the Graduate School of the

University of Colorado in partial fulfillment

of the requirements for the degree of

Doctor of Philosophy

Department of Electrical Electrical, Computer, and Energy Engineering

2018

This thesis entitled:
Low Profile, High Power Density and High Efficiency DC-DC Converters
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The final copy of this thesis has been examined by the signatories, and we find that both
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above mentioned discipline.

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Low Profile, High Power Density and High Efficiency DC-DC Converters

Thesis directed by Prof. Khurram K. Afridi

Due to the ever decreasing thickness and increasing battery size of modern cellphones, battery chargers inside cellphones are required to meet increasingly stringent power density requirements, including small printed circuit board (PCB) area and component height. This thesis is focused on low-profile, high-power-density, and high-efficiency dc-dc converters for battery charging applications.

This thesis investigates five topologies, including ZVS-QSW buck converter, three-level buck converter, four-level buck converter, a resonant switched capacitor converter, and a new reconfigurable hybrid switched capacitor converter. The operation principle of each topology is described, and the advantages and disadvantages of each topology are analyzed and compared in terms of efficiency and power density. To accurately evaluate the performance of each topology, this thesis utilizes the augmented state-space modeling method that efficiently calculates the steady-state waveforms of a converter. To accurately predict losses, the dynamic on-resistance of GaN transistors and core loss of inductors have been modeled. Furthermore, a comprehensive optimization methodology is utilized to select circuit and component parameters.

First, for nominal 2:1 step-down conversion ratio application for which the three-level buck converter is best suited, two prototypes of the three-level buck converter, one using GaN transistors and the other using low-voltage Silicon MOSFETs are designed, built and tested. Both converters are designed for an input voltage range of 5 V to 20 V, an output voltage range of 3 V to 4.2 V, and a maximum output current of 10 A. The prototype with the GaN transistors (EPC2023) occupies a PCB area of 358 mm^2 and has a component height of 1 mm. To maximize efficiency, the converter is designed to achieve ZVS at light-

to-medium loads, while sacrificing ZVS to reduce transistor conduction and inductor losses. This GaN-based prototype converter achieves a peak efficiency of 98.5% at 2:1 conversion ration and high efficiency at other operating conditions with a power density of 704 W/in^3 . The prototype using low-voltage Silicon MOSFETs (CPF03433) has a slightly smaller PCB area of 310 mm^2, but its efficiency at high output currents is substantially lower than that of the GaN-based prototype. Next, for a nominal 3:1 step-down conversion ratio application for which the four-level buck converter is best suited, a prototype of four-level buck converter with a PCB area of 410 mm^2 and a component height of 1mm, optimized for 3:1 step-down, is built and tested. Finally, for an extreme-power-density application, where the converter is required to deliver a maximum output power of 40 W at an output voltage in the range of 3 V to 4.2 V and an input voltage in the range of 5 V to 20 V, with its PCB footprint limited to only 80 mm^2 and its component height limited to 1 mm, a prototype 1-MHz ZVS-QSW buck converter is built and tested. This prototype converter achieves a peak efficiency of 96.7% and a power density of 3230 W/in^3.

Dedication

To all who have helped me.

Acknowledgements

I would like to express my sincere gratitude to my advisor, Prof. Khurram Afridi, for his guidance and support through out my Ph.D program at CU Boulder. He has very deep knowledge and understanding of various facets of power electronics, especially related to high-frequency resonant converters. He encouraged me to do hard work and be relentless. He has also taught me with academic writing and presentation. I would also like to thank my co-advisor Prof. Dragan Makismovic for importing his knowledge and providing guidance through my Ph.D years. His approach to isolating and solving problems really inspired me.

I would also like to acknowledge the support from the other members of my thesis committee: Prof. Robert Erickson, Prof. Hanh-Phuc Le and Prof. Daniel Costinett. Their advice has helped make this thesis stronger. I am also grateful to the sponsors of my research: Texas Instruments and Huawei Technologies. Of my colleagues at CoPEC, I especially thank Ashish Kurmar for his constant help in my Ph.D years. We have spent so many nights in discussions, conducting experiments and writing. This thesis would not be possible without his help. I also thank Fenglong Lu, Jie lu, Hua Chen, Yuanzhe Zhang, Fan Zhang, Yucheng Gao and Tianshi Xie for the discussions on power electronics. I also thank Saad Pervaiz, Prasanta Achanta, Sreyam Sinha, Ratul Das and Brandon Regensburger for their support in the lab, and thanks to Casey Hardy and Colin McHugh for their help on analog IC design.

I also thank Zhe Feng, Duanfeng Gao, my roomate Bo Ding and my other friends in Colorado for making the last few years so much more fun. Finally, I thank my parents for their help and support through out my entire life.

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Chapter 1

Introduction

1.1   Background and Motivation

Nowadays, in the highly competitive consumer electronics market, customers favor thinner cellphones with larger battery capacity. The battery chargers inside cellphones are required to meet increasingly stringent power density requirements, including small printed circuit board (PCB) area and limited component height. These battery chargers also need to maintain very high efficiency, since customers are very sensitive to the heat generated by the conversion power loss. Additionally, this high efficiency must be maintained across a wide range of input voltages, as enabled by the latest USB standard [1]. The new standard allows for fast charging using substantially higher charging power.

The power density of a converter is defined as the power delivered by the converter per unit of its volume. The volume of a switched-mode converter is dominated by its passive energy storage and transformation components, that is capacitors, inductors and transformers. To shrink the volume of the converter and meet the low-profile requirements, small yet efficient planar inductors need to be designed. One way to decrease the size of inductors and capacitors is to increase the switching frequency, which reduces the required inductance and capacitance values. However, increasing the switching frequency exacerbates switching losses, which are proportional to switching frequency [2–4]. Also, as the size of the power converter is reduced, it is more important to achieve high efficiency in order to maintain thermal stability of the converter as the surface area through wich the heat can be extracted

reduces [5]. Therefore, the design and optimization of high-power-density converters requires accurately loss and thermal models for its various components.

1.2   State of the Art and Thesis Objectives

Cellphone battery chargers need to achieve high power density and provide regulation capability, while remaining low profile, highly efficient across wide-range operating conditions in terms of input voltage, output voltage and output power. Conventional dc-dc converters suitable for cellphone battery charging applications do not simultaneously satisfy these three requirements. For instance, [6] achieves high power density and high efficiency, but does not provide the regulation capability. Others [7,8] provide regulation and can achieve relatively high power density, but do not maintain high wide-range efficiency. Enabled by the latest USB standard for fast charging, this battery charger is designed for an input voltage range of 5 V to 20 V, an output voltage range of 3 V to 4.2 V, and a maximum output current of 10 A. Many semiconductor companies have proposed their products of DC-DC converter for this battery charging application, as shown in Fig. 1.1.
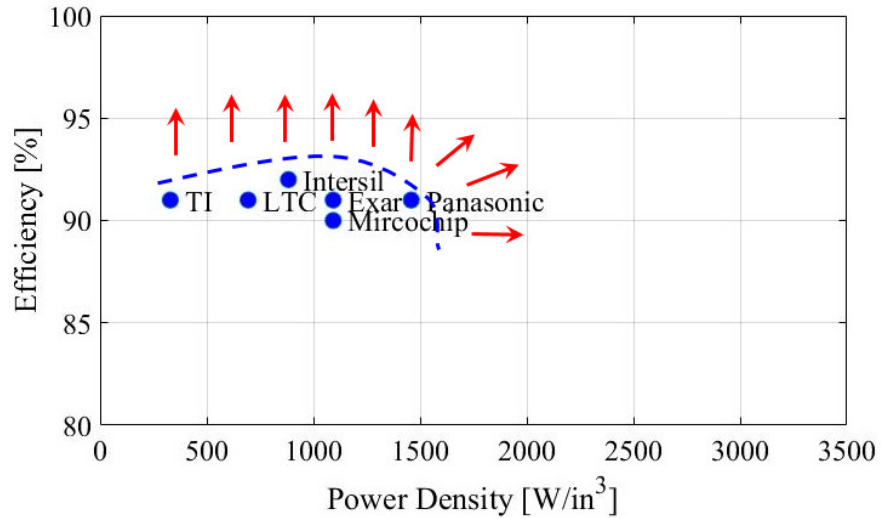
Figure 1.1: State-of-the-art commercial DC-DC converters, suitable for cellphone battery charging applicaion. Indicated efficiency is with input voltage of 12 V, output voltage of 4 V and output current of 10 A.

This thesis aims to push the limit of power density and efficiency of battery charger and focus on the design of DC-DC converter that achieves both high power density (including low profile) and high efficiency across a wide range of input voltages. The main challenge is the topology selection and magnetics design. There are so many topologies available for DC-DC converter, and each of them has its own advantages and disadvantages. The magnetics design is even more demanding, since the converter's component height is restricted within 1 mm and the inductor needs to handle large input voltage range (5 V to 20 V) and large output current (10 A). A thorough search of off-the-shelf inductors has been done, as listed in Tale. 1.1. It can bee seen that for large current capability (RMS current over 13 A), there is no inductor of height within 1 mm available. Therefore, we have to design the customized inductor, while choosing the proper topology to achieve the goal of high power density and high efficiency.

Table 1.1: Commercial Power Inductor Product List

Manufacture	Part Number	Inductance	I_{rms}	Dimension (mm)
Wurth Eletronics	732-773-010	1 μH	4 A	4×4.5×3.2
Wurth Eletronics	732-773-003	330 nH	10.8 A	5.2×5.8×4.5
Wurth Eletronics	110-001-150	1 μH	22.5 A	11.6×7.8×7.1
Wurth Eletronics	WW006	1 μH	30 A	10×10×8.1
Coil Craft	FA2769-AL	26 nH	5 A	3.65×3.65×1.5
Coil Craft	XAL4020-221	220 nH	5 A	4.3×4.3×1.8
Coil Craft	KA5013-AE	1.5 μH	5 A	4.3×4.3×1.8
Coil Craft	XEL4012-920	92 nH	16.2 A	4.3×4.3×1.5
Coil Craft	XEL3515-720	72 nH	18 A	3.65×3.65×1.5
Coil Craft	XEL4030-101	100 nH	18 A	3.65×3.65×1.5

1.3   Contributions of the Thesis

This thesis aims to design a low-profile, high-power-density and high-efficiency cell-phone battery charger. This converter delivers 40 W across input voltage range of 5 V to 20 V, with output voltage range of 3 V to 4.2 V. Five alternative topologies: zero-voltage

switching quasi-square-wave (ZVS-QSW) buck converter, three-level buck converter, resonant switched capacitor converter, reconfigurable hybrid switched capacitor converter and four-level buck converter are analyzed and compared in terms of efficiency and power density in this application.

The design methodology for these five converter topologies presented here utilizes the augmented state-space modeling approach to predict converter waveforms with high accuracy and computational efficiency. Conventional analytical method uses small-ripple approximation assuming that the capacitor voltage ripples are negligible, which sacrifices the accuracy. For topology such as resonant switched capacitor converter, it's very difficult to get the switch and inductor current analytical expression with small-ripple approximation. Another common way of predicting the converter waveforms is to utilize Spice simulation tools, such as LTSpice, Pspice, PLECS. With refined component model provided, the simulation results can be highly accurate. However, starting from initial conditions, the simulation takes considerable computation time to get settled and obtain the steady-state waveforms of the converter. This thesis introduces the augmented state-space modeling to predict steady-state waveforms of a given DC-DC converter in excellent agreement with the LTspice simulated waveforms, while requiring only 1/60 of the computation time. This enables a comprehensive optimization of the converters design by sweeping parameters such as switching frequency and inductor geometry over wide ranges.

Next, this thesis introduces loss model for the DC-DC converter, transistor loss, inductor loss, capacitor loss and trace loss. The transistor loss includes gating loss, switching loss and conduction loss. The planar inductor loss includes winding loss and core loss. To get a more accurate loss model for GaN transistors and inductor, this thesis utilizes converter waveforms measurement and component thermal measurement to calibrate the dynamic on-resistance of the GaN switch at high frequency(MHz) and planar inductor steinmetz parameters operated at large flux density($B_{max} > 500$ mT) scenario. Finite-Element-Analysis simulation tool Ansys Maxwell has also been used to calculate the inductor ac resistance

and PCB trace loss. With the modeling method and refined loss model, this thesis proposes converter design for three application scenarios: 2-to-1 conversion ratio, 3-to-1 conversion ratio, and extreme-power-density design.

The three-level buck converter achieves highest efficiency at 2:1 conversion ratio scenario (input voltage $V_{\mathrm{IN}} = 8\,V$, output voltage $V_{\mathrm{OUT}} = 4\,V$). The augmented state-space modeling has been utilized to predict the three-level buck converter waveforms, check the zero-voltage-switching (ZVS), and calculate the converter losses. To achieve high power density, a custom-shaped planar PCB-integrated inductor is designed, whose geometry is optimized using 3D finite-element analysis (FEA) to minimize losses. Two prototype three-level buck converter have been built. One prototype using EPC2023 GaN device with a PCB area of 358 mm^2 and component height of 1 mm designed is built and tested. This prototype converter achieves a peak efficiency of 98.5% at 2:1 conversion ratio and high overall efficiency at other operating conditions with a power density of 704 W/in^3. The other prototype using low-voltage silicon MOSFET (CPF03433) with a PCB area of 310 mm^2 is also built and tested. For GaN device prototype, to maximize efficiency, the converter is designed to achieve zero-voltage switching (ZVS) at light-to-medium loads, while sacrificing ZVS to reduce transistor conduction and inductor losses. For low-voltage silicon device prototype, ZVS is achieved across all load condition at ($V_{\mathrm{IN}} = 12\,V$, $V_{\mathrm{OUT}} = 4\,V$) to reduce the voltage stress on the device. Also, The on-resistance and output capacitance of the Silicon MOSFET (CPF03433) have been calibrated with experimental results, and the comparison of GaN transistor(EPC2023) GaN and Silicon MOSFET (CPF03433) has also been done.

The four-level buck converter and reconfigurable hybrid switched capacitor converter using six switches achieve high efficiency when the input voltage is high. The four-level buck converter reaches its maximum efficiency at 3:1 conversion ratio (input voltage $V_{\mathrm{IN}} = 12\,V$, output voltage $V_{\mathrm{OUT}} = 4\,V$), due to its minimized inductor current ripple. The augmented state-space modeling method is utilized to accurately predict the two types of converters' waveforms and calculate the loss. Also, a custom-shaped planar PCB-integrated inductor

is designed to achieve high power density and high efficiency. Based on the analysis, a prototype of four-level buck converter with EPC2023 GaN transistors has been built and tested.

Finally, this thesis introduces the design of a extreme-power-density battery charger. Specifically, the converter is required to deliver a maximum output power of 40 W across a 4:1 input voltage range, with its PCB footprint limited to $80\,\text{mm}^2$ and its component height limited to 1 mm. Due to the stringent area (80mm^2) requirement, three alternative topologies a zero-voltage-switching quasi-square-wave (ZVS-QSW) buck converter, a three-level buck converter, and a resonant switched capacitor converter are analyzed, designed and compared in terms of efficiency and power density in this application. Four-level buck converter and reconfigurable hybrid switched capacitor converter are not considered in this design for their overabundant switches quantity. The inductors in the three converter topologies are designed as planar PCB-integrated structures with custom-shaped ferrite cores, optimized using a 3D finite-element analysis (FEA) tool. The ZVS-QSW buck converter is predicted to achieve the highest efficiency under the specified area and height constraints. A prototype 40-W 1-MHz buck converter with a PCB area of 79.6 mm^2 and component height of 1 mm is built and tested. The prototype converter achieves a peak efficiency of 96.7% and a power density of 3230 W/in^3.

1.4   Thesis Organization

The remainder of this thesis is organized as follows: Chapter 2 introduces five alternative topologies: zero-voltage switching quasi-square-wave (ZVS-QSW) buck converter, three-level buck converter, resonant switched capacitor converter, reconfigurable hybrid switched capacitor converter and four-level buck converter for this battery charging application. The operation principle, advantage and disadvantage of each topology is stated in Chapter 2. Chapter 3 presents two design techniques, including augmented state-space modeling method and loss model for the dc-dc converter with calibrated dynamic on resistance for GaN de-

vice and Steinmetz parameters for 3F46 ferrite material to accurately predict the converter waveforms and estimate its loss. Chapter 4 describes a low-profile, high-power-density, and high-efficiency three-level buck converter fit for 2:1 conversion ratio. Two prototype of three-level buck converter have been built and tested, including one using GaN switches and the other using silicon MOSFET. Chapter 6 presents a high-efficiency four-level buck converter optimized for 3:1 conversion ratio application, with the prototype built. Chapter 7 shows the design of very tiny battery charger with PCB footprint limited to $80\,\mathrm{mm}^2$. Finally, the summary and conclusions of the thesis are presented in Chapter 8.

Chapter 2

Alternative Battery Charger Topologies

The stringent area and height specifications of the battery charging application considered in this thesis favor dc-dc converter topologies with limited switch count and small passive (inductor and capacitor) volume. This thesis considers five dc-dc converter topologies, described below. They are zero-voltage switching quasi-square-wave (ZVS-QSW) buck converter, three-level buck converter, resonant switched capacitor converter, four-level buck converter and reconfigurable hybrid switched capacitor converter. Advantages and disadvantages of each topology have been stated. The operation principle of each topology is also described in this chapter.

2.1   Zero-Voltage Switching Quasi-Square-Wave Buck Converter
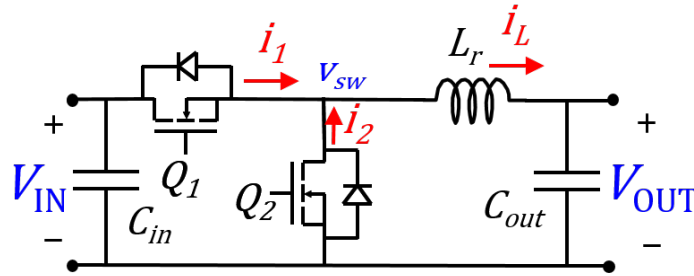
Figure 2.1: Zero-Voltage Switching Quasi-Square-Wave Buck (ZVS-QSW) converter topology.

The synchronous buck converter, shown in Fig. 2.1, utilizes only two switches, one

inductor and two capacitors, and is hence potentially volume-efficient. The size of this converters passive components can be reduced by operating at high switching frequencies. To achieve high efficiency at these high frequencies, a ZVS-QSW version of the buck converter can be employed, in which the converters inductance is small enough to allow the inductor current to go negative, enabling ZVS of the high-side transistor [9]. Similar to its conventional counterpart, the ZVS-QSW buck converter can regulate its output voltage using duty-ratio control. However, the increase in inductor current ripple required to achieve ZVS introduces additional inductor winding losses and transistor conduction losses. To maintain high efficiency in the presence of this tradeoff, a methodology to optimize the design of a ZVS-QSW buck converter in terms of its switching frequency and inductance is described in later chapter.

2.2   Three-Level Buck Converter
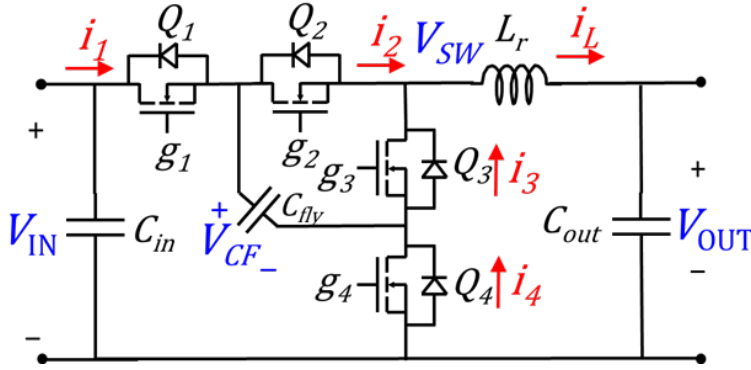
Figure 2.2: The three level buck converter topology.

The topology of a three-level buck converter is shown in Fig. 2.2. Compared to the synchronous buck converter, this converter utilizes three additional components two switches and a flying capacitor. The output voltage of this converter is also regulated using duty-ratio control. As can be seen from Fig. 2.3, the switches Q_1 and Q_4 are operated in a complementary manner with a duty ratio D. Similarly, the switches Q_2 and Q_3 operate in a complementary fashion with the same duty ratio. These two groups of switches, (Q_1, Q_4
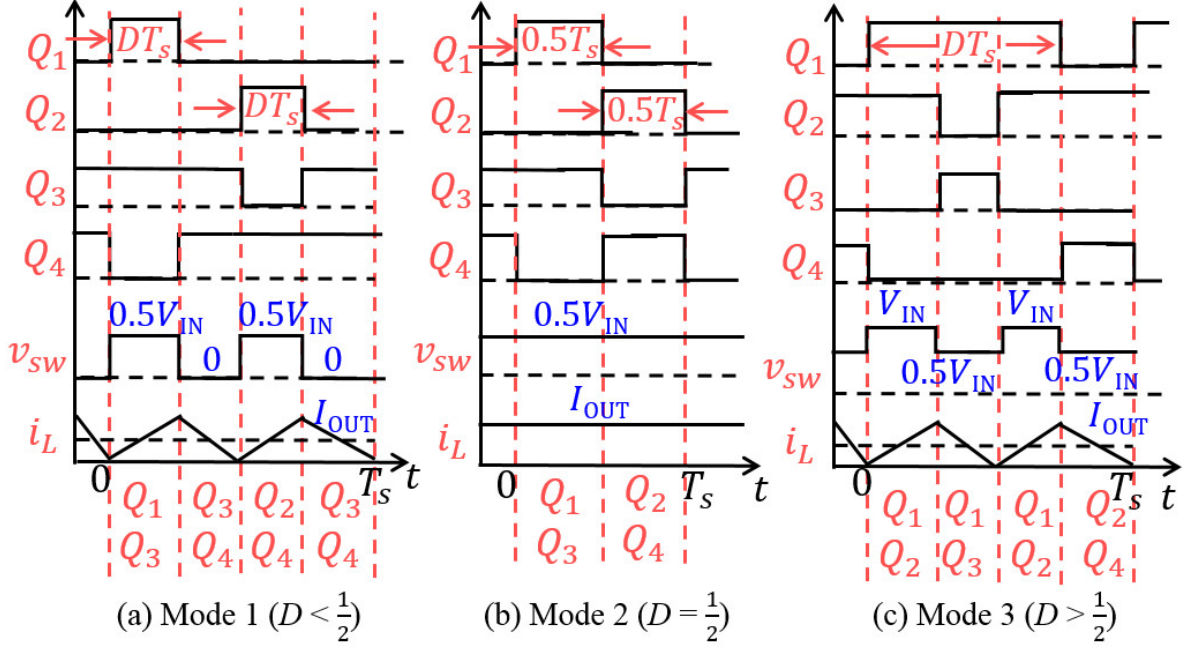
Figure 2.3: Gate signals of Q_1, Q_2, Q_3, Q_4 switch-node voltage and inductor current for duty ratio $D < 0.5, D = 0.5$, and $D > 0.5$.

) and (Q_2, Q_3), are switched with a time-shift of half a switching period $\frac{T_s}{2}$. The output voltage of the three-level buck converter is given by:

$$V_{\text{OUT}} = DV_{\text{IN}} \qquad (2.1)$$

Here, V_{IN} and V_{OUT} are the dc input and output voltages of the converter, respectively. With the switches operated as described above, the three-level buck converter operates in two different modes, as shown in Fig. 2.3: when the required conversion ratio ($V_{\text{OUT}}/V_{\text{IN}}$) is less than half, the duty ratio D as computed using (2.1) is also less than half, and the switch-node voltage v_{sw} alternates between 0 and $V_{\text{IN}}/2$. When the conversion ratio, and hence the duty ratio D, is greater than half, the switch-node voltage alternates between $V_{\text{IN}}/2$ and V_{IN}. In applications where a wide range of conversion ratios is required, such as the battery charging application considered here, this multi-mode operation of the three-level buck converter reduces the volt-seconds applied to the inductor, potentially reducing its losses

and size. Furthermore, by transferring some of the losses to the two additional transistors, this converter can offer a better thermal distribution than a synchronous buck converter. However, due to its three additional components compared to the buck converter, the three-level buck converter is more challenging to design for a high-power-density application, such as the one considered here. The design of a three-level buck converter is optimized and its performance compared to the ZVS-QSW buck converter in Chapter 6. Additional details of the operation and control of the three-level buck converter, including its soft-switching capabilities, can be found in [9–13].

2.3   Resonant Switched Capacitor Converter
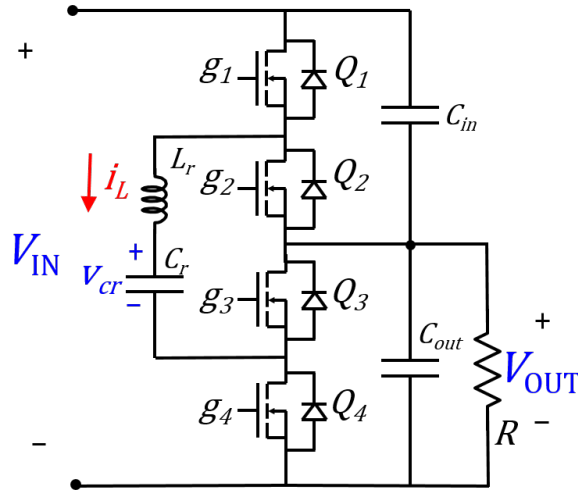
Figure 2.4: Four-switch ladder resonant switched capacitor converter topology.

Switched capacitor converters are a popular solution for high power density converter design, since these converters do not utilize any magnetic components. However, conventional switched capacitor converters are efficient only near the fixed conversion ratios inherent to their topologies. Adding a small appropriately-located inductor to a switched capacitor converter enables it to provide a wider range of conversion ratios while maintaining high efficiency [14–20]. Among such hybrid switched capacitor topologies, the four-switch ladder resonant switched capacitor (ReSC) converter, shown in Fig. 2.4, is a suitable alternative
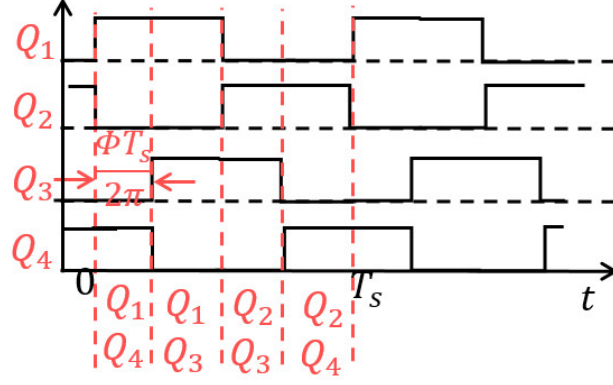
Figure 2.5: Gate signals of Q_1, Q_2, Q_3, Q_4 of the four-switch ladder resonant switched capacitor converter.

for the volume-limited application considered here. The output voltage of this converter can be regulated by controlling the phase-shift between its top and bottom half-bridges (as shown in Fig. 2.5), and/or by controlling its switching frequency [15, 16]. Using state plane analysis, and assuming lossless power conversion, the output voltage of this converter can be expressed as:

$$V_{\text{OUT}} = \frac{V_{\text{IN}} F_s}{2\pi Z_0} \left[\sin\left(\frac{\Phi}{F_s}\right) \tan\left(\frac{\pi}{2F_s}\right) - 1 \right] R \tag{2.2}$$

Here, F_s is the normalized switching frequency of the converter, given by $F_s = \dfrac{f_s}{f_0}$, where f_s is the switching frequency and f_0 is the resonant frequency of the tank formed by the inductor L_r and flying capacitor C_r in the ReSC converter of Fig. 2.4; Z_0 is the characteristic impedance of this resonant tank; Φ is the phase shift between the top and bottom half-bridges of the converter; and R is the value of the resistance modeling the converters load.

In practice, owing to the on resistance of the switches and inductor, the actual output voltage may deviate substantially from the ideal value given in (2.2). The augmented state-space modeling can be applied in the case of the resonant switched capacitor converter, wherein circuit behavior is conventionally predicted assuming lossless power conversion, as

stated in (2.2). However, the augmented state-space analysis utilized here demonstrates that the output voltage of this converter can be substantially different from that predicted by the conventional analysis, as shown in Fig. 2.6.
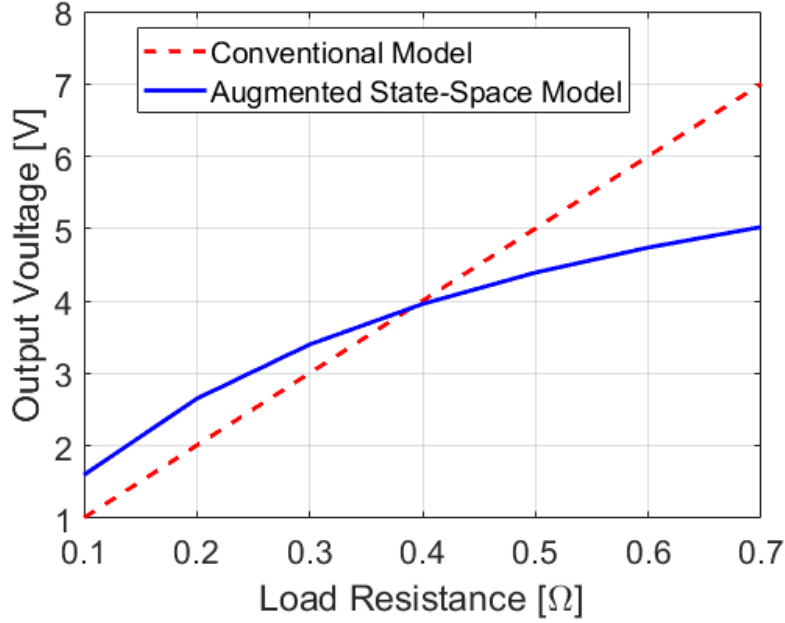
Figure 2.6: Comparison between the output voltage of the four-switch ladder resonant switched capacitor converter, as predicted by the conventional lossless analysis and augmented state-space analysis including losses.

Compared to the ZVS-QSW buck and three-level buck converters, the resonant switched capacitor converter requires a significantly smaller inductance. However, at conversion ratio other than 2:1, the energy is circulating in the converter tank thus the peak and RMS currents are significantly higher than those in the buck and three-level buck converters owing to its resonant nature. Thus this converter is suitable for application with fixed conversion ratio. The design of a four-switch ladder resonant switched capacitor converter is optimized and its performance is compared to the other two candidate topologies in later chapter. Additional details of the operation and control of this converter can be found in [14–18].
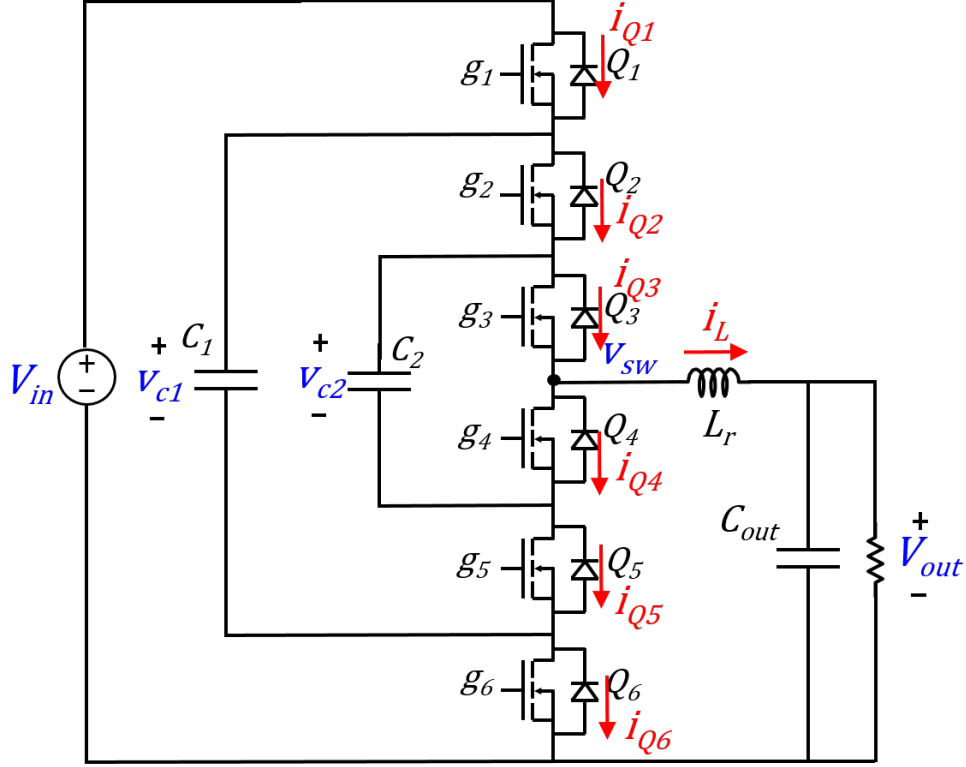
Figure 2.7: Four-level buck converter topology.

2.4 Four-Level Buck Converter

The topology of a four-level buck converter is shown in Fig. 2.7. Compared to the three-level buck converter, this converter utilizes three additional components two switches and a flying capacitor. The output voltage of this converter is also regulated using duty-ratio control. As can be seen from Fig. 2.8, the switches Q_1 and Q_6 are operated in a complementary manner with a duty ratio D. Similarly, the switches Q_2, Q_5 and Q_3, Q_4 operate in a complementary fashion with the same duty ratio. These three groups of switches, (Q_1,Q_6), (Q_2,Q_5) and (Q_3,Q_4) are switched with a mutual time-shift of a third of a switching period $\dfrac{T_s}{3}$. The output voltage of the four-level buck converter is given by:

$$V_{\text{OUT}} = DV_{\text{IN}} \tag{2.3}$$
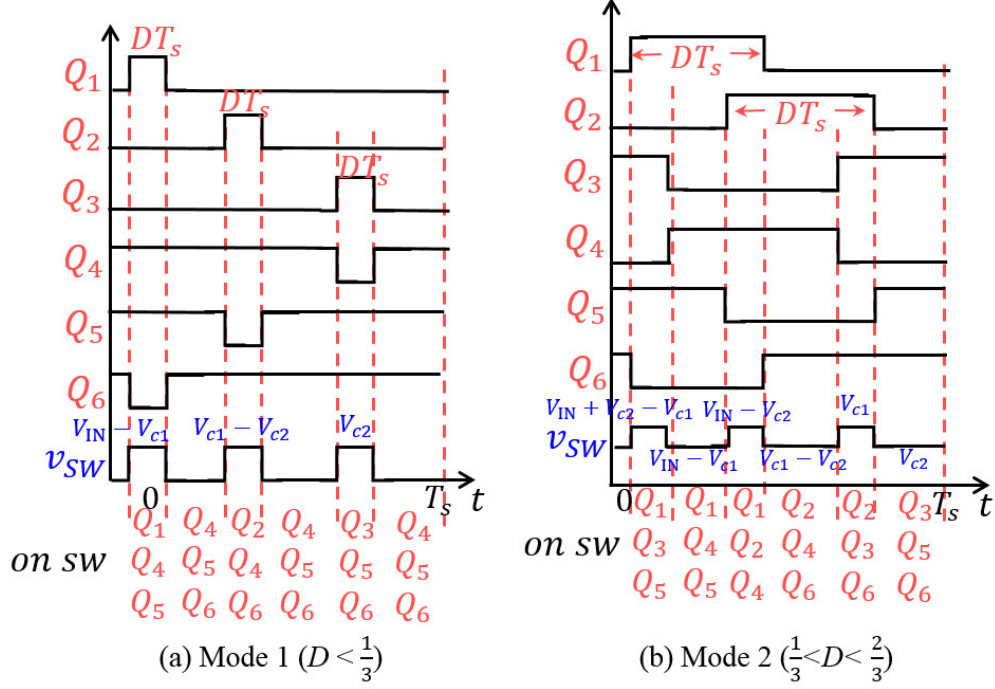
Figure 2.8: Gate signals of $Q_1, Q_2, Q_3, Q_4, Q_5, Q_6$ and switch-node voltage of four level buck converter when duty ratio $D < 1/3$ and $1/3 < D < 2/3$.

Here, V_{IN} and V_{OUT} are the dc input and output voltages of the converter, respectively. $V_{c1} = 2/3 V_{\text{IN}}$, $V_{c2} = V_{\text{IN}}/3$. With the switches operated as described above, the four-level buck converter operates in three different modes: when the required conversion ratio ($V_{\text{OUT}}/V_{\text{IN}}$) is less than $1/3$, the duty ratio D as computed using (2.3) is also less than $1/3$, and the switch-node voltage v_{sw} alternates between 0 and $V_{\text{IN}}/3$. When the conversion ratio, and hence the duty ratio $1/3 < D < 2/3$, the switch-node voltage alternates between $V_{\text{IN}}/3$ and $2/3 V_{\text{IN}}$, as shown in Fig. 2.8. When the conversion ratio, and hence the duty ratio $D > 2/3$, the switch-node voltage alternates between $2/3 V_{\text{IN}}$ and V_{IN}.

The inductor switching node V_{sw} varies from 0, $V_{\text{IN}}/3$, $2/3 V_{\text{IN}}$ and V_{IN} for four levels. Compared with three-level buck converter, the four-level buck converter further reduces the voltage stress on the inductor and also triple the switching node frequency, thus minimizes the inductor current ripple and the volt-seconds applied to the inductor, potentially reducing its losses and size. But the extra two switches result in more transistor conduction loss and

occupies more area. Therefore the four level buck converter is suitable for application with extremely small inductor, and not sensitive to the switches areas. Additional details of the operation and control of the four-level buck converter, can be found in [21–23]. More details of four-level buck converter,including augmented state-space modeling and loss model analysis and optimization will be provided in the Chapter 6.

2.5   Reconfigurable Hybrid Switched Capacitor Converter
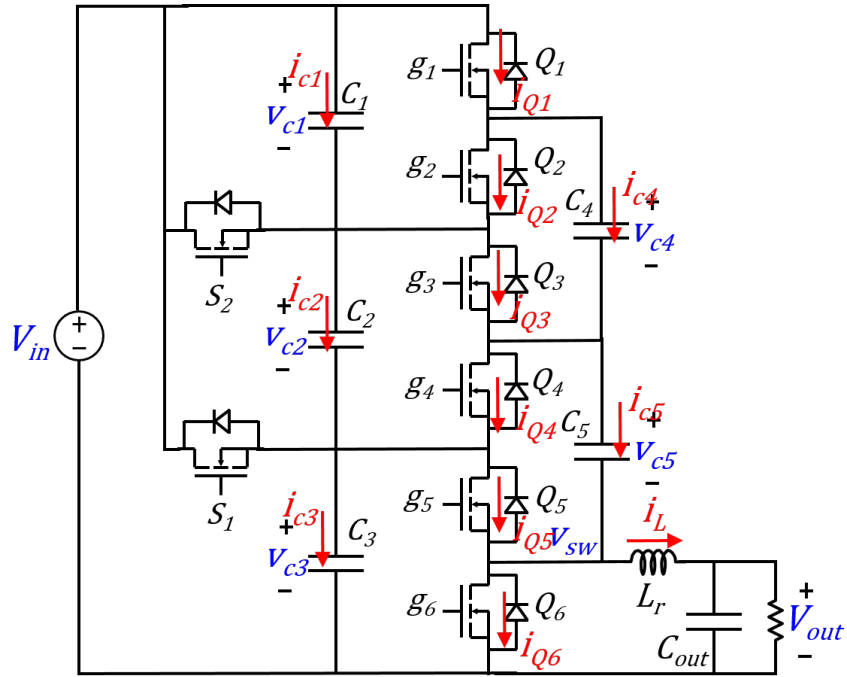
Figure 2.9: Reconfigurable hybrid switched capacitor converter topology.

This thesis also presents a new reconfigurable hybrid switched capacitor converter topology shown in Fig. 2.9. This converter is designed for various step-down ratio scenarios and operates in three different modes to achieves favorable trade-off between switch losses and inductor losses. When $V_{\text{OUT}} < \dfrac{V_{\text{IN}}}{3}$, mode selection switches S_1 and S_2 are off, These three groups of switches, (Q_1,Q_2), (Q_3,Q_4) and (Q_5,Q_6) operates in complimentary mode, with duty ration D. Three capacitors C_1, C_2, and C_3 equally split the input voltage V_{IN}, so

Figure 2.10: Gate signals of $Q_1, Q_2, Q_3, Q_4, Q_5, Q_6$ and switch-node voltage of reconfigurable hybrid switched capacitor converter when output voltage $V_{\text{OUT}} < \dfrac{V_{\text{IN}}}{3}$.

that $V_{c1} = V_{c2} = V_{c3} = \dfrac{V_{\text{IN}}}{3}$. V_{sw} toggles between 0 and $\frac{V_{\text{IN}}}{3}$ with a duty ratio of D, as shown in Fig. 2.10. The output voltage of the reconfigurable hybrid switched capacitor converter is given by:

$$V_{\text{OUT}} = D\frac{V_{\text{IN}}}{3} \tag{2.4}$$

When $\dfrac{V_{\text{IN}}}{3} < V_{\text{OUT}} < \dfrac{1}{2}V_{\text{IN}}$, mode selection switch S_1 is off, S_2 is on and (Q_1, Q_2) are off. Two groups of switches, (Q_3, Q_4) and (Q_5, Q_6) operate in complimentary mode, with duty ration D. Two capacitors C_2, and C_3 equally splits the input voltage V_{IN}, so that $V_{c2} = V_{c3} = \dfrac{V_{\text{IN}}}{2}$. V_{sw} toggles between 0 and $\frac{V_{\text{IN}}}{2}$ with a duty ratio of D. The output voltage of the reconfigurable hybrid switched capacitor converter is given by:

$$V_{\text{OUT}} = D\frac{V_{\text{IN}}}{2} \tag{2.5}$$

When $\dfrac{V_{\text{IN}}}{2} < V_{\text{OUT}} < V_{\text{IN}}$, mode selection switch S_2 is off, and S_1 is on. (Q_5, Q_6) operates in complimentary mode, with duty ratio D. The input voltage V_{IN} is applied on the C_3, therefore V_{sw} toggles between 0 and V_{IN} with a duty ratio of D. The output voltage of the reconfigurable hybrid switched capacitor converter is given by:

$$V_{\text{OUT}} = DV_{\text{IN}} \tag{2.6}$$

Depending on the output voltage and input voltage ratio, this reconfigurable hybrid switched capacitor converter operates in three modes and V_{sw} toggles between V_{IN}, $V_{\text{IN}}/2$, or $V_{\text{IN}}/3$ and 0. This multi-mode operation mitigates inductor volt-seconds and loss. Compared with four-level buck converter, it uses less switches in series when $D = V_{\text{IN}}/V_{\text{OUT}}$ is high, thus reduce the switch conduction loss. More details regarding this reconfigurable hybrid switched capacitor converter, including its loss modeling, optimization, and a comparison with the four-level buck converter will be provided in the Chapter 5.

Chapter 3

Design Techniques

To evaluate and compare the performance of the different topologies identified in Chapter 2, design techniques to accurately estimate the performance of the converter are needed. This chapter discusses the two design techniques used in this thesis. One is the augmented state-space modeling method to accurately calculate the converter waveforms, such as inductor current and capacitor voltage; the other is loss model for the dc-dc converter, specifically with calibrated GaN device dynamic on-resistance and Steinmetz parameters for 3F46 ferrite material. Based on these two design techniques, the efficiency and loss breakdown of converters with different topologies, including QSW buck, three-level buck, reconfigurable hybrid switched capacitor and four level buck converter, over full input voltage range is predicted and presented in the later section.

3.1   Augmented State-Space Modeling

Commonly, there are two ways to predict the waveforms of a converter. Conventional analytical method uses small-ripple approximation, which assumes that the capacitor voltage and inductor current ripples are small enough. This method is widely used in design, as it requires the designer to fully understand how the converter operates and how the parameters, such as frequency, phase shift and duty cycle, change the waveforms of the converter. There are two main drawback of the analytical method. One is that sometimes it sacrifices accuracy to get analytically solvable equations. For example, in PWM converters, it neglects voltage

ripple on the capacitor. The other issue is that in resonant and switched capacitor converter, the inductor current or capacitor voltage analytical expressions are very complicated and even sometimes impossible to get. Another common way to predict the converter waveforms is utilizing Spice simulation tools, including LTSpice, Pspice, PLECS and so on. The main advantage of the simulation method is its high accuracy. With accurate component model provided, the simulation results match the experimental results pretty well. The drawback of the simulation method is that it consumes considerable computation time and resources. To obtain the steady-state waveforms of the converter, the Spice simulation takes substantial time from initial condition to get settled. In cases when numerous values need to be swept, the total computation time of simulation might be unacceptable.
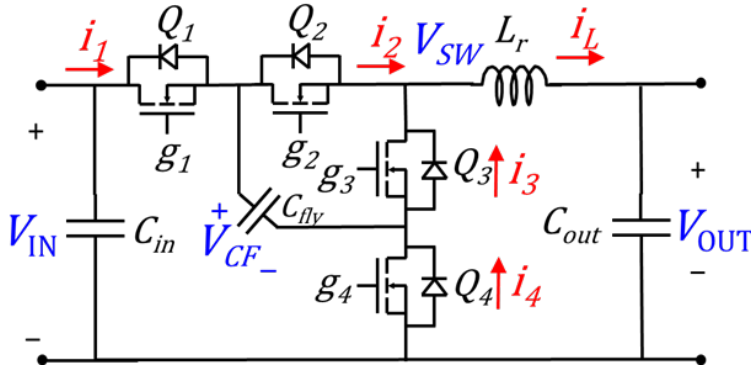
Figure 3.1: The three-level topology.

In this thesis, all the converter topologies utilize the augmented state-space modeling approach to predict converter waveforms with high accuracy and computational efficiency. A three-level buck converter is shown in Fig. 3.1 as an example.

The three-level buck converter has three modes ($D < 0.5, D = 0.5, D > 0.5$). In each mode, the converter's operation can be described using a sequence of equivalent linear circuits, with each equivalent circuit corresponding to a particular configuration (on/off) of the switches. As an example, the operation and corresponding equivalent circuits of the three-level buck converter operating in the $D < 0.5$ mode are shown in Fig. 3.2. To analyze these circuits, three state variables are considered: flying capacitor voltage V_{CF}, output
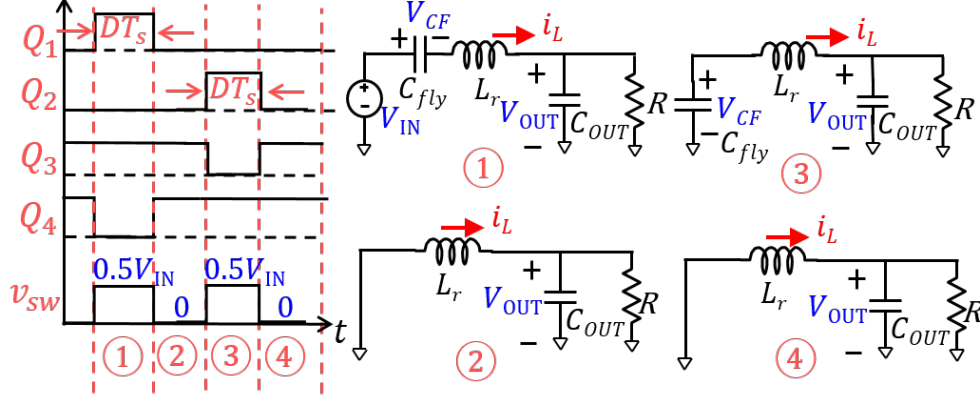
Figure 3.2: Operation and corresponding states of three level buck converter when $D < 0.5$.

voltage V_{OUT} and inductor current i_L and state equations are written for each equivalent circuit. For instance, for the first equivalent circuit, the state bn-space equation is given by:

$$
\underbrace{\begin{bmatrix} \dot{V_{CF}} \\ \dot{V_{OUT}} \\ \dot{i_L} \end{bmatrix}}_{\dot{x}} = \underbrace{\begin{bmatrix} 0 & 0 & 1/C_f \\ 0 & -1/(RC_{OUT}) & 1/C_{OUT} \\ -1/L_r & -1/L_r & -R_{on}/L_r \end{bmatrix}}_{A_1} \underbrace{\begin{bmatrix} V_{CF} \\ V_{OUT} \\ i_L \end{bmatrix}}_{x} + \underbrace{\begin{bmatrix} 0 \\ 0 \\ V_{IN}/L_r \end{bmatrix}}_{B_1} \tag{3.1}
$$

Here L_r is the inductance, C_f is the flying capacitance, C_{OUT} is the output capacitance, V_{IN} is the input voltage, R is the load resistance, and R_{tot} is the sum of the on-resistance of two of the converters switches, the ac resistance of the inductor and the equivalent series resistance (ESR) of the flying capacitor. Similar state-space equations can be written for the other three equivalent circuits. Therefore the converter behavior can be expressed in state-space equation as:

$$
\dot{x} = Ax + B \tag{3.2}
$$

For each state, there is $A_1, A_2..A_4$, $B_1, B_2..B_4$ state matrix. For $D < 0.5$ mode, the state matrix A and B can be expressed as:

$$A_1 = \begin{bmatrix} 0 & 0 & \frac{1}{C_f} \\ 0 & \frac{-1}{RC_{OUT}} & \frac{1}{C_{OUT}} \\ \frac{-1}{L_r} & \frac{-1}{L_r} & \frac{-R_{on}}{L_r} \end{bmatrix}, A_2 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & \frac{-1}{RC_{OUT}} & \frac{1}{C_{OUT}} \\ 0 & \frac{-1}{L_r} & \frac{-R_{on}}{L_r} \end{bmatrix} \tag{3.3}$$

$$A_3 = \begin{bmatrix} 0 & 0 & \frac{1}{C_f} \\ 0 & \frac{-1}{RC_{OUT}} & \frac{1}{C_{OUT}} \\ \frac{1}{L_r} & \frac{-1}{L_r} & \frac{-R_{on}}{L_r} \end{bmatrix}, A_4 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & \frac{-1}{RC_{OUT}} & \frac{1}{C_{OUT}} \\ \frac{-1}{L_r} & \frac{-1}{L_r} & \frac{-R_{on}}{L_r} \end{bmatrix} \tag{3.4}$$

$$B_1 = \begin{bmatrix} 0 \\ 0 \\ \frac{V_{IN}}{L_r} \end{bmatrix}, B_2 = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix}, B_3 = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix}, B_4 = \begin{bmatrix} 0 \\ 0 \\ \frac{V_{IN}}{L_r} \end{bmatrix} \tag{3.5}$$

Once the state matrix is obtained based on the operation of the converter, the state variable x in time domain can be solved as:

$$x(t) = e^{A_i(t-t_{i-1})} x_{t_{i-1}} + \int_{t_{i-1}}^{t} e^{A_i(t-\tau)} B_i d\tau \tag{3.6}$$

Here, t_{i-1} is the time at the end of $(i\text{-}1)$-th mode. $x_{t_{i-1}}$ is the state variable at the end of the $(i\text{-}1)$-th mode, that is the initial state variable for the i-th mode. Using (3.6), the state variable at the end of each mode can be expressed as:

$$x_i = e^{A_i d_i T_s} x_{i-1} + \int_{t_{i-1}}^{t_i} e^{A_i(t-\tau)} B_i d\tau = \Phi_i x_{i-1} + \Gamma_i \tag{3.7}$$

where d_i is the duty ratio of i-th mode, T_s is the converter's switching period. t_i is the time at the end of the i-th mode, $\Phi_i = e^{A_i d_i T_s}$ is the state-transition matrix for the i-th mode, and Γ_i is the term with integration and accounts for the effect of the input variable on the evolution of states. This involves lots of matrix integration and inversion, which takes tremendous amount of computation effort and time. To solve this issue, the augmented state-space modeling approach introduced in [24] is used in this thesis. The state variable and system matrix are augmented as follows:

$$\hat{x} = \begin{bmatrix} x \\ 1 \end{bmatrix} \tag{3.8}$$

$$\hat{A}_i = \begin{bmatrix} A_i & B_i \\ \Theta & 0 \end{bmatrix} \tag{3.9}$$

Here Θ is the zero row-vector of length equal to the size of the system matrix. A new state equation can now be written for the augmented system, and the solution be obtained as:

$$\dot{\hat{x}} = \hat{A}_i \hat{x} \tag{3.10}$$

$$\hat{x}(t) = e^{\hat{A}_i(t-t_{i-1})}\hat{x}_{i-1} = \hat{\Phi}_i \hat{x}_{i-1} \tag{3.11}$$

Here $\hat{\Phi}_i = e^{\hat{A}_i d_i T_s}$ is the augmented state-transition matrix for the i-th mode. As shown in Fig. 3.2, in one steady-state period, $0 < t < T_s$, the converter goes through four states, and the variable x value backs to its original value:

$$\hat{x}(t_0 + T_s) = \hat{\Phi}_m \hat{\Phi}_{m-1} \cdots \hat{\Phi}_1 \hat{x}(t_0) = \hat{x}(t_0) \tag{3.12}$$

At $t = t_0$, the state variable x value can be solved as:

$$x(t_0) = (I^n - \Phi_{tot})^{-1}\Gamma_{tot} \tag{3.13}$$

Where $\Phi_{tot} = \Phi_m \Phi_{m-1} \cdots \Phi_1$ and $\Gamma_{tot} = \Phi_m \Phi_{m-1} \cdots \Phi_2 \Gamma_1 + \cdots \Phi_m \Gamma_{m-1} + \Gamma_m$. The Φ_m and Γ_m represent the state-transition matrix and integration of m-th mode. In each mode, the state variable can be expressed as: $x_{t_1} = \hat{\Phi}_1 x(t_0)$, $x_{t_2} = \hat{\Phi}_2 x(t_1)$ ... and $x_{t_m} = \hat{\Phi}_m x(t_{m-1})$. The state variable x in time domain of each mode can be solved as : $x_{t_1}(t) = e^{\hat{A}_1 t_1 t} x_{t_0}$,

$x_{t_2}(t) = e^{\hat{A}_2 t_2 t} x_{t_1}$ ... and $x_{t_m}(t) = e^{\hat{A}_m t_m t} x_{t_{m-1}}$. x_{t_i} is the state variable at the end of the $(i-1)$-th mode, that is the initial state variable for the i-th mode. Therefore, the state variable $x(t)$ in the one steady-state switching period can be obtained as:

$$x(t) = [x_{t_1}(t), x_{t_2}(t) \cdots x_{t_m}(t)] \tag{3.14}$$

Using this approach, the periodic steady-state waveforms of the three-level buck converter can be directly predicted without need to go through the startup transients (as required in a circuit simulator like Spice), and without the need for matrix integration and inversion steps (which are required in other state-space based modeling techniques). Hence, this approach is computationally efficient. Furthermore, it predicts the converters waveforms with a high degree of accuracy, as shown Fig. 3.3, which compares example waveforms of the three-level buck converter as predicted by the augmented state-space modeling, LTspice simulations, and the conventional small-ripple approximation [25]. As can be seen, unlike waveforms predicted by small-ripple approximation, the augmented state-space predicted waveforms are in excellent agreement with the LTspice simulated waveforms, while requiring only 1/60 of the computation time. This enables comprehensive optimization of the converters design by sweeping parameters such as switching frequency and passive component values over wide ranges.

3.2   Loss Models for the DC-DC Converter

The loss model plays an important role in the power converter design. An accurate loss model helps to predict the loss distribution and performance of a converter, determine the suitable topology among the various candidates, and optimize the design parameters, such as switching frequency and components selection. In this high-power-density cellphone charger application where the total volume is so limited and the components, including switches, capacitor and inductor are so compact, an accurate loss model is even more in need. This
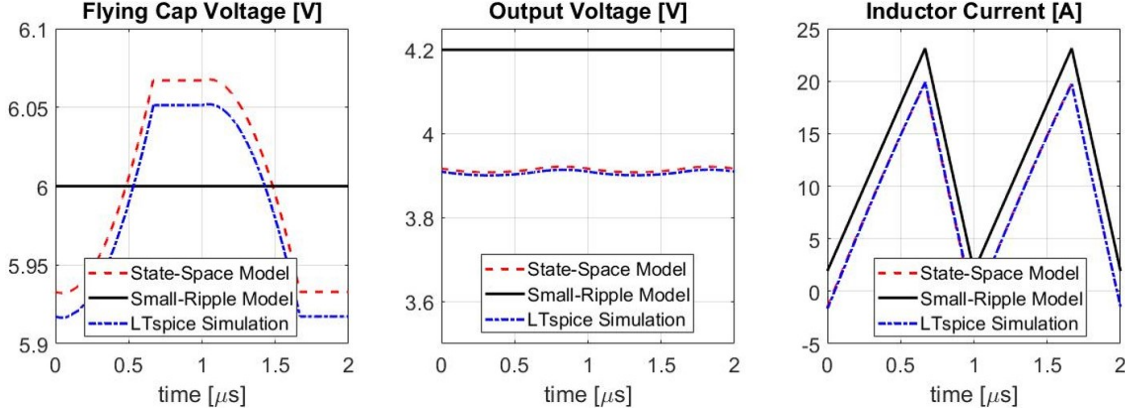
Figure 3.3: Comparison between example waveforms of three-level buck converter as predicted by augmented state-space modeling, small-ripple approximation and LTSpice simulations at input voltage $V_{\mathrm{IN}} = 12\,V$, output voltage $V_{\mathrm{OUT}} = 4\,V$, and output current $I_{\mathrm{OUT}} = 10\,A$.

section is focused on the loss model for GaN transistors switching at high frequency (MHz) and planar inductor operated at large flux density($B_{max} > 500$ mT) scenario. By using both converter waveforms measurement and component thermal measurement, a refined loss model of GaN devices and planar inductor is presented.

3.2.1   Theoretical Loss Model for the DC-DC Converter

The loss model of a switch-mode power converter includes three major parts: transistor loss, inductor loss, capacitor loss and trace loss:

$$P_{total} = P_{trans} + P_{ind} + P_{cap} + P_{trace} \tag{3.15}$$

The transistor loss includes gating loss, switching loss and conduction loss:

$$P_{trans} = P_{trans,gate} + P_{trans,sw} + P_{trans,cond} \tag{3.16}$$

The gating losses of each transistor are calculated using:

$$P_{trans,gate} = V_{gs}Q_s f_s \tag{3.17}$$

where V_{gs} is the gate-to-source voltage of the transistor, and Q_g is its total gate charge.

The switching loss of the transistor includes turn-on loss and turn-off loss:

$$P_{trans,sw} = P_{trans,off} + P_{trans,on} \tag{3.18}$$

The turn-off switching losses of each transistor are computed using [26]:

$$P_{trans,off} = \frac{I_{off}^2 t_{off}^2}{48 C_{oss}} f_s \tag{3.19}$$

Here, I_{off} is the current flowing through the transistor at the instant it is turned off, t_{off} is the fall time of the current, which is 3.5 ns, and C_{oss} is the output capacitance of the transistor. At operating points of the converter(s) where a transistor loses ZVS, its turn-on switching losses can be computed using:

$$P_{trans,on} = \frac{1}{2} C_{oss} V_{DS,on}^2 f_s \tag{3.20}$$

Here, $V_{DS,on}$ is the drain-to-source voltage of the transistor at the instant it is turned on.

The conduction losses in each transistor are calculating using:

$$P_{trans,cond} = I_{t,rms}^2 R_{ds,on} \tag{3.21}$$

Here, $I_{t,rms}$ is the RMS current through the transistor, and $R_{ds,on}$ is the on-resistance of the transistor.

The planar inductor loss includes winding loss and core loss:

$$P_{ind} = P_{winding} + P_{core} \tag{3.22}$$

The winding losses in the inductor are calculated from:

$$P_{winding} = I_{ind,dc}^2 R_{dc} + \sum_{i=1}^{20} I_{ind,rms,i}^2 R_{ac,i} \tag{3.23}$$

Here, $I_{ind,dc}$ is the value of the dc component and $I_{ind,rms,i}$ is the RMS value of the i-th harmonic of the inductor current. R_{dc} is the dc resistance and $R_{ac,i}$ is the i-th harmonic ac resistance of the inductor winding.

The inductor core losses are computed using the iGSE method [27]:

$$P_{core} = \sum_i \frac{1}{T_s} \int_0^{T_s} k_i |\frac{dB}{dt}|^\alpha |\Delta B(t)|^{\beta-\alpha} \, dt \, V \tag{3.24}$$

Where k_i is defined by:

$$k_i = \frac{k_{fe}}{(2\pi)^{\alpha-1} \int_0^{2\pi} |cos\theta|^\alpha 2^{\beta-\alpha} d\theta} \tag{3.25}$$

Here, T_s is switching period. k_{fe}, α and β are steinmetz parameters generally found empirically from the material's $B - H$ hysteresis curve by curve fitting. ΔB is the flux density from peak to peak.

The conduction losses in the capacitors are calculated using:

$$P_{cap} = I_{cap,rms}^2 R_{esr} \tag{3.26}$$

Here, $I_{cap,rms}$ is the RMS value of the capacitor current, and R_{esr} is the equivalent series resistance (ESR) of the capacitor.

Finally, the trace losses in the converter are calculated using:

$$P_{trace} = \sum_{i=1}^{n} I_{trace,rms,i}^2 R_{trace,i} \tag{3.27}$$

Here, $I_{trace,rms,i}$ is the RMS value of each trace, and $R_{trace,i}$ is the on-resistance of each trace.

3.2.2   Thermal Resistance of Switch, Inductor and PCB Traces

The theoretical loss model for the DC-DC converter is introduced in the previous section. However, there could be substantial discrepancy between the theoretical loss model and the experimentally measured results. For a synchronous buck converter, as shown in the Fig. 3.4, with the input voltage $V_{\text{IN}} = 5\,V$, and output voltage $V_{\text{OUT}} = 4\,V$, there is good match between the theoretically predicted loss and the measured loss at light load current. However, the theoretically predicted loss deviates greatly from the measured loss at large load current.
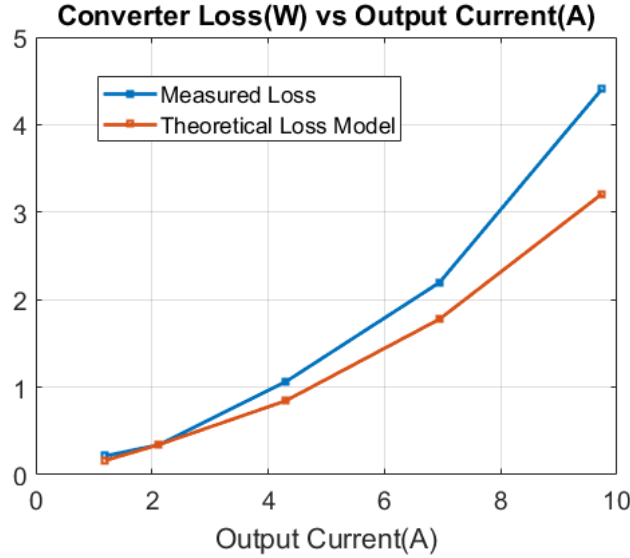
Figure 3.4: Comparison of loss model predicted and measured efficiency for QSW-ZVS buck converter over full range of output current.

This synchronous buck converter operates in Zero-Voltage-Switching (ZVS) condition, and the main mismatch between the theoretically prediected loss and experimentally measured loss comes from the converter's switch conduction loss, inductor loss and trace loss. To figure out the exact loss of each component (including the switch, inductor and trace), thermal experiments have been done to estimate the thermal resistance R_{th} of the switch, inductor and trace, and then calculate the loss of each component using:

$$P_{component} = \frac{\Delta T_{rise}}{R_{th}} \tag{3.28}$$
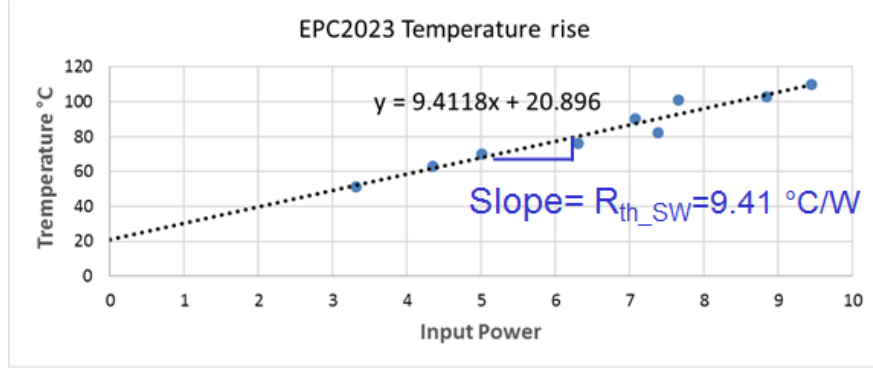
Figure 3.5: GaN transistor (EPC2023) thermal resistance measurement results.

To measure the thermal resistance of the GaN transistor (EPC2023). Certain input power is fed into the transistor and the surface temperature of the transistor has been measured with thermocouple sensor. The thermal resistance measurement results are plotted in Fig. 3.5. As can be seen, the temperature of the switch increases almost linearly with the increase of the input power. The thermal resistance is defined as the slope of the curve, which is $R_{th,sw} = 9.41°C/W$.
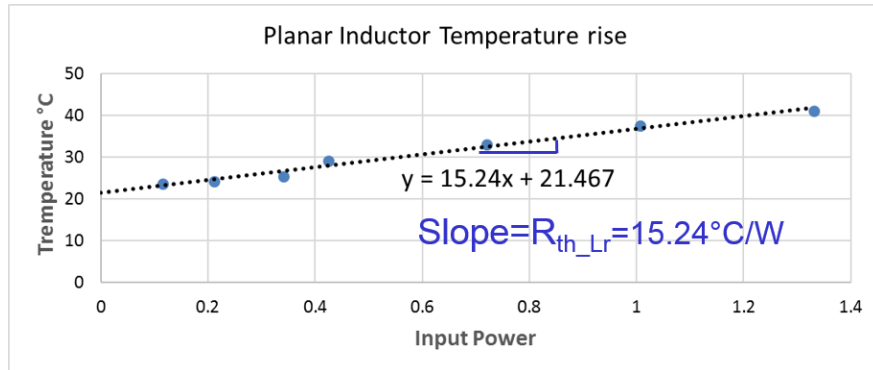
Figure 3.6: Customized planar inductor thermal resistance measurement results.

Similar experiments have also been done to measure the thermal resistance of planar inductor, as shown in Fig. 3.6. The thermal resistance of the inductor is $R_{th,ind} = 15.24°C/W$.
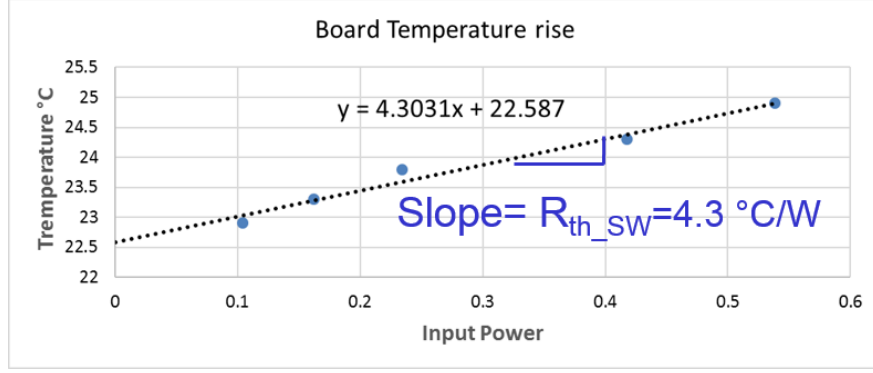
Figure 3.7: Printed circuit board thermal resistance measurement results.

Finally, the PCB thermal resistance has been measured with this method. The PCB thermal resistance measurement results are plotted in Fig. 3.7, which shows $R_{th,pcb} = 4.3°\text{C/W}$.

The next step is to measure the temperature rise of each component (switch, inductor and PCB trace) when the converter is operating, so that the loss of the each component can be estimated. Specifically, as shown in Fig. 3.8, the switches and inductor are thermally decoupled to eliminate the mutual thermal effect.
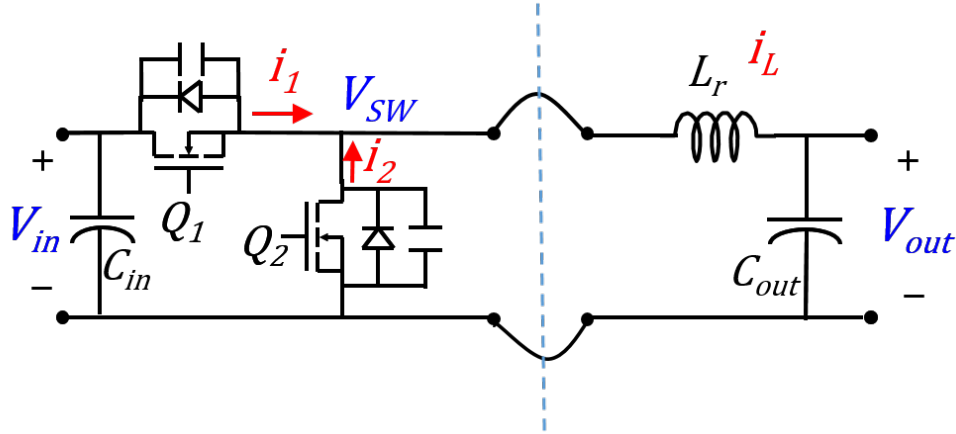
Figure 3.8: QSW-ZVS buck converter with switches and inductor thermally decoupled.

Table.3.1 shows the temperature of switches, planar inductor and PCB trace when the ZVS-QSW buck converter is operating at input voltage $V_{\text{IN}} = 5\,V$, output voltage $V_{\text{OUT}} = 4\,V$, for various load current conditions, with room temperature is 22.8°C.

Table 3.1: Temperature of switches, planar inductor and PCB trace when the ZVS-QSW buck converter is operated at input voltage $V_{\text{IN}} = 5\,V$, output voltage $V_{\text{OUT}} = 4\,V$, for various output current conditions, with room temperature is $22.8°C$.

$I_{\text{OUT}}(A)$	$Q_1\,Temp(°)$	$Q_2\,Temp(°)$	$L_r\,Temp(°)$	PCB $Temp(°)$
1.2	25.4	25.1	25.1	24.5
2.1	25.4	25.4	25.2	24.6
4.3	26.6	26	26	24.5
6.9	29.5	28.7	30.6	27.5
9.7	38.2	35.2	43.6	29.6
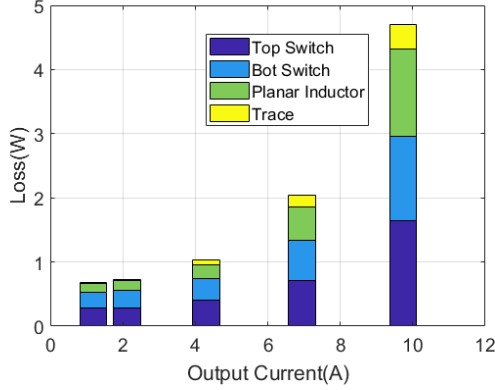
(a)

(b)
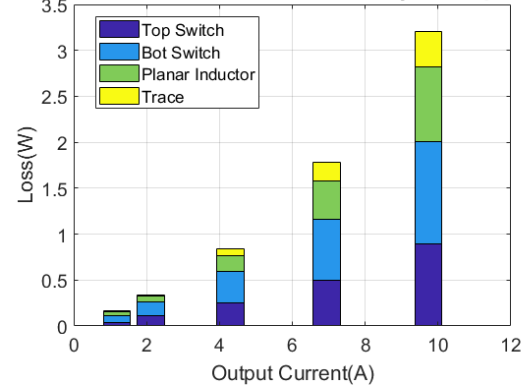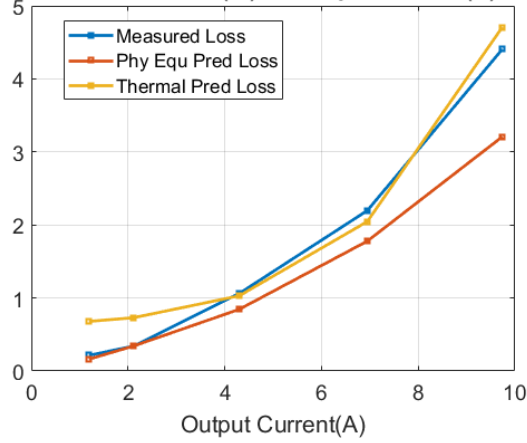
(c)

Figure 3.9: Loss breakdown of the ZVS-QSW buck based on (a) thermal results and (b) theoretical loss model and (c) the comparision with measured loss, when the converter is operating at input voltage $V_{\text{IN}} = 5\,V$, output voltage $V_{\text{OUT}} = 4\,V$, for various load conditions.

Therefore, the loss breakdown of the converter based on thermal experimental results can be obtained and is shown in the Fig. 3.9, with comparison of loss breakdown from theoretical loss model mentioned in the previous section. It can be seen that the thermal predicted loss has much better match with the theoretically predicted loss. Compared with the theoretical loss model, the thermal method predicts higher loss of the switches and inductor. This shows that the dynamic on-resistance of the GaN switches does play an important role in the switch conduction loss. Also the inductor core loss at large flux density scenario is worse than what the datasheet expects.

Similar experiments and measurements can also be done in other V_{IN}, V_{OUT}, I_{OUT} operating conditions and they also verify that the on-resistance of the GaN transistor switching at high frequency is higher than what the datasheet claims. And the steinmetz parameters calculating inductor core loss at large flux density scenario need to be calibrated.

3.2.3   Dynamic On Resistance of GaN Transistors

At high switching frequency, the dynamic on-resistance $R_{ds,on}$ will increase due to the charge trapping phenomenon in the HEMT structure [28–34]. The $R_{ds,on}$ value from manufacturer's datasheet are measured under DC condition. Therefore, at high switching frequency, the $R_{ds,on}$ value provided by the manufacturer is no longer accurate to calculate the switch conduction losses. This section uses the thermal measurement results to estimate the dynamic on-resistance of the GaN transistor, which is also verified by i-v waveform measurement results.

As stated in the previous section, the total loss of GaN transistor can be estimated with thermal measurement method:

$$P_{trans} = \frac{\Delta T_{rise}}{R_{th,sw}} \tag{3.29}$$

Where the transistor thermal resistance $R_{th,sw} = 9.41°\text{C/W}$, as mentioned in the above

section. At Zero-Voltage-Switching condition, the GaN switch loss contains turn-off loss and conduction loss:

$$P_{trans} = P_{conduct} + P_{off} \tag{3.30}$$

$$P_{trans} = I_{t,rms}^2 R_{ds,on} + \frac{I_{off}^2 t_{off}^2}{48 C_{oss}} f_s \tag{3.31}$$

For different operating conditions, the transistor loss P_{trans} can be measured from thermal experimental results. In this way, the dynamic on-resistance $R_{ds,on}$ can be calculated.

Also, the GaN transistor drain-to-source voltage V_{ds} can be measured with low-voltage differential voltage probe and the inductor current i_L can represent the switch current i_{ds}. In this way, the GaN transistor on-resistance $R_{ds,on}$ is calculated using:

$$R_{ds,on} = \frac{V_{ds}}{i_{ds}} - R_{trace} \tag{3.32}$$

Here R_{trace} is the trace resistance in series of the transistor. Fig. 3.10 shows the GaN transistor drain-to-soure voltage and current waveforms for synchronous buck converter at the operating point of $V_{\text{IN}} = 5\,V$, $V_{\text{OUT}} = 4\,V$, and $I_{\text{OUT}} = 6A$.

Besides dynamic on-resistance of the GaN switch, the trace resistance also contributes to the conduction loss. Since the trace is in series of the switch, Finite-Element-Analysis simulation tool Ansys Maxwell has been used to calculate the PCB trace on-resistance. Fig. 3.11 shows the piece of PCB trace in series of the transistor, and at 1 MHz switching frequency, the trace on-resistance is calculated as 1.6 mΩ.

In this way, the measured dynamic on-resistance of the GaN transistor(EPC2023) operated at 1MHz switching frequency with different drain to source voltage: $V_{ds} = 5V$, $V_{ds} = 8V$, and $V_{ds} = 12V$ can be calculated, as shown in Table.3.2.
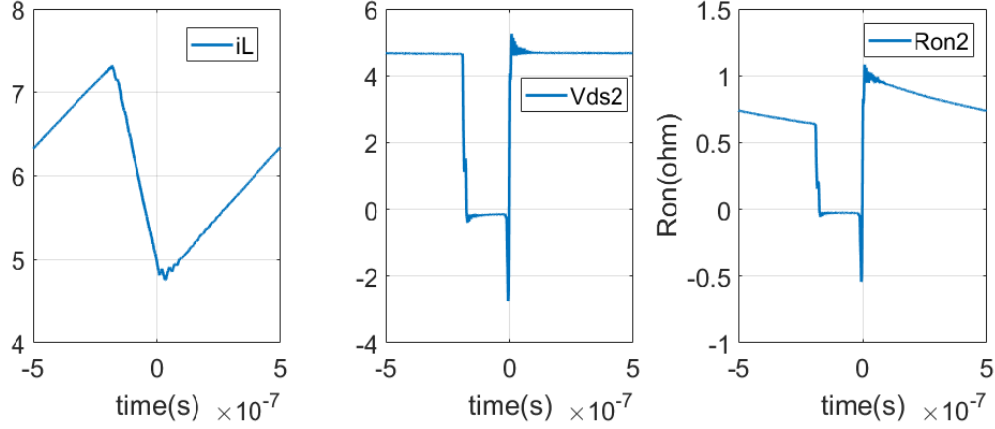
Figure 3.10: The GaN switch drain to source voltage V_{ds}, current i_{ds} and on resistance $R_{ds,on}$ at the operating point of input voltage $V_{\text{IN}} = 5\,V$, output voltage $V_{\text{OUT}} = 4\,V$, and output current $I_{\text{OUT}} = 6A$.
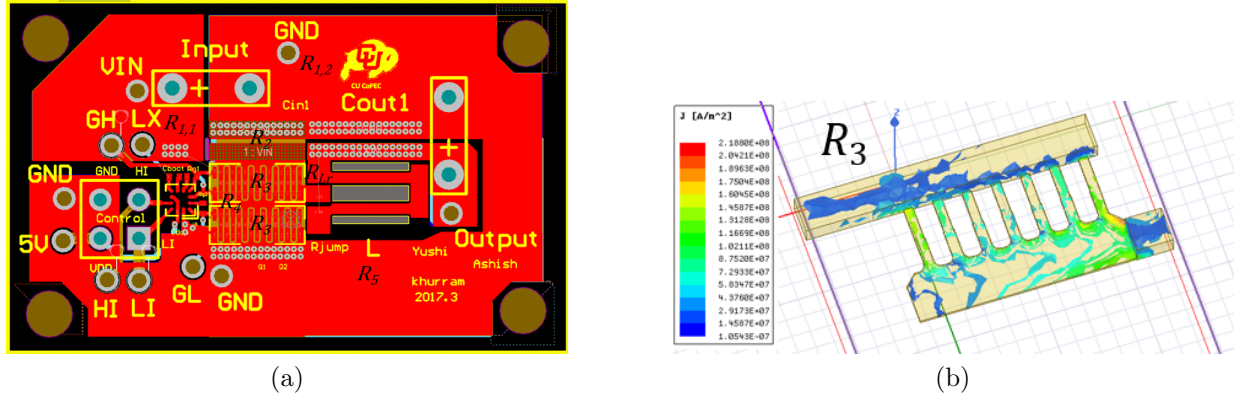
Figure 3.11: PCB trace on-resistance of the ZVS-QSW buck (a) PCB layout of buck converter (b) Finite-element analysis of PCB trace on-resitance.

Table 3.2: Measured dynamic on-resistance of EPC2023 GaN switch operated at 1MHz switching frequency with different drain to source voltage: $V_{ds} = 5V$, $V_{ds} = 8V$, and $V_{ds} = 12V$, compared with datasheet value.

Datasheet R_{on}	$R_{on}@V_{ds} = 5V$	$R_{on}@V_{ds} = 8V$	$R_{on}@V_{ds} = 12V$
$1.45\,m\Omega$	$3.2\,m\Omega$	$4.25\,m\Omega$	$5.35\,m\Omega$

3.2.4 Steinmetz Parameters for Core Loss

The planar inductor loss contains winding loss and core loss. The winding losses are calculated using:

$$P_{winding} = I_{ind,dc}^2 R_{dc} + \sum_{i=1}^{20} I_{ind,rms,i}^2 R_{ac,i} \tag{3.33}$$

Here, $I_{ind,dc}$ is the value of the dc component and $I_{ind,rms,i}$ is the RMS value of the i-th harmonic of the inductor current. R_{dc} is the dc resistance and $R_{ac,i}$ is the i-th harmonic ac resistance of the inductor winding. For a given planar inductor structure, the $R_{ac,i}$ can be obtained from Ansys Maxwell simulation, as shown in Fig. 3.12

<div align="center">(a)   (b)</div>
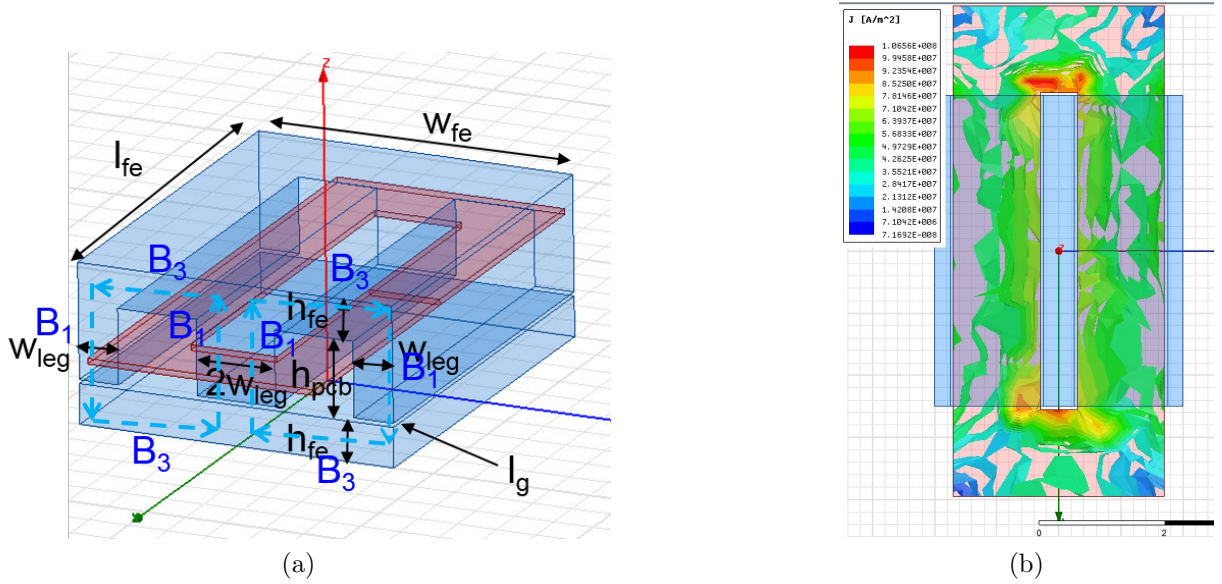
Figure 3.12: Planar inductor ac resistance simulation result: (a) core geometry; (b) finite-element analysis of winding ac resistance at 1MHz.

The inductor core loss is calculated using the iGSE method [27].

$$P_{core} = \sum_i \frac{1}{T_s} \int_0^{T_s} k_i |\frac{dB}{dt}|^\alpha |\Delta B(t)|^{\beta-\alpha} \, dt \, V \tag{3.34}$$

Where k_i is defined by:

$$k_i = \frac{k_{fe}}{(2\pi)^{\alpha-1} \int_0^{2\pi} |cos\theta|^\alpha 2^{\beta-\alpha} d\theta} \tag{3.35}$$

Here, T_s is switching period. k_{fe}, α and β are steinmetz parameters generally found empirically from the material's $B - H$ hysteresis curve by curve fitting. ΔB is the flux

density from peak to peak.

The steinmetz parameters k_{fe},α and β can be obtained from datasheet. However, the manufacturer only provides the core loss at low flux density scenario, where $\Delta B < 200$ mT. In this high-power-density application, due to the small size, the planar inductor is operated at large flux density ($B_{max} > 500$ mT). Therefore, the steinmetz parameters need to be calibrated with thermal experimental results.

The synchronous buck converter with decoupled indutor and switches, shown in Fig. 3.8, is operated at different input voltage, switching frequency and load current conditions. For each operating condition, the ac flux density ΔB, maximum flux density B_{max} and core loss P_{core} can be calculated using:

$$\Delta B = \frac{\mu_0}{2l_g}\Delta i_L \tag{3.36}$$

$$B_{max} = \frac{\mu_0}{2l_g}i_{Lmax} \tag{3.37}$$

$$P_{core} = P_{ind} - P_{winding} \tag{3.38}$$

Here, $\mu_0 = 4\pi e^{-7}$ H/m is the permeability of free space. l_g is the air gap of the inductor. Δi_L and i_{Lmax} is the inductor current ripple and maximum inductor current, respectively. For a given planar inductor geometry, the inductance and ac resistance can be got from the Ansys Maxwell simulation, and the Δi_L and i_{Lmax} is obtained with augmented state-space modeling method. P_{ind} is total inductor loss obtained from the thermal measurement. $P_{winding}$ is the inductor winding loss calculated by (3.23). Table 3.3, 3.4, and 3.5 show the measured P_{core}, ΔB and B_{max} value at various input voltage V_{IN}, output voltage V_{OUT}, output current I_{OUT} and switching frequency f_s conditions.

Based on the data points above, the steinmetz parameter k_{fe}, α and β for 3F46 ferrite material is swept to calculate the core loss P_{core} using (3.38) at each operating point. For each

Table 3.3: Core loss P_{core}, ac flux density ΔB and maximum flux density B_{max} at input voltage $V_{IN} = 5\,V$, output voltage $V_{OUT} = 4\,V$, and switching frequency $f_s = 1250\,\text{kHz}$.

$I_{OUT}\,(\text{A})$	$P_{core}\,(\text{W})$	$\Delta B\,(\text{mT})$	$B_{max}\,(\text{mT})$
1.43	0.042	63.9	123.4
4.92	0.067	64.2	275.9
8.61	0.526	64.1	446.3

Table 3.4: Core loss P_{core}, ac flux density ΔB and maximum flux density B_{max} at input voltage $V_{IN} = 8\,V$, output voltage $V_{OUT} = 4\,V$, and switching frequency $f_s = 2000\,\text{kHz}$.

$I_{OUT}\,(\text{A})$	$P_{core}\,(\text{W})$	$\Delta B\,(\text{mT})$	$B_{max}\,(\text{mT})$
2.62	0.284	100.2	218.4
5.23	0.294	101.2	343.9
7.63	0.587	104.6	446.3
8.54	0.67	101.6	510.8

Table 3.5: Core loss P_{core}, ac flux density ΔB and maximum flux density B_{max} at input voltage $V_{IN} = 12\,V$, output voltage $V_{OUT} = 4\,V$, and switching frequency $f_s = 1750\,\text{kHz}$.

$I_{OUT}\,(\text{A})$	$P_{core}\,(\text{W})$	$\Delta B\,(\text{mT})$	$B_{max}\,(\text{mT})$
2.46	0.931	159.7	270.6
5.12	0.753	158.5	400.2
7.99	1.055	157.34	546.4
8.50	1.25	164.8	581.7

steinmetz parameter, the theoretical core loss is compared with experimentally measured value, as $\Delta_e = P_{measure} - P_{core}$. Then the total errors E_{tot} for all measured points with this k_{fe}, α and β can be expressed as: $E_{tot} = \sum \Delta_e^2(k_{fe}, \alpha, \beta)$. The value of k_{fe}, α with minimal total errors E_{tot} for all operating points can be found. A flowchart summarizing the steps involved in the proposed calibrating approach is shown in Fig. 3.13. Fig. 3.14 shows the curve fitting of theoretical inductor loss and the measured data at different ΔB and P_{core} point. The blue curve shows the fit to a series of experimental measured data points (blue circles).
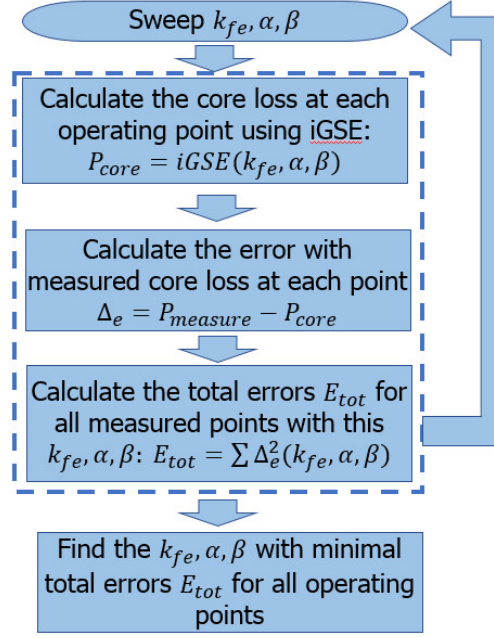
Figure 3.13: Flowchart detailing the proposed methodology to get steinmetz parameter k_{fe}, α and β for 3F46 ferrite material.
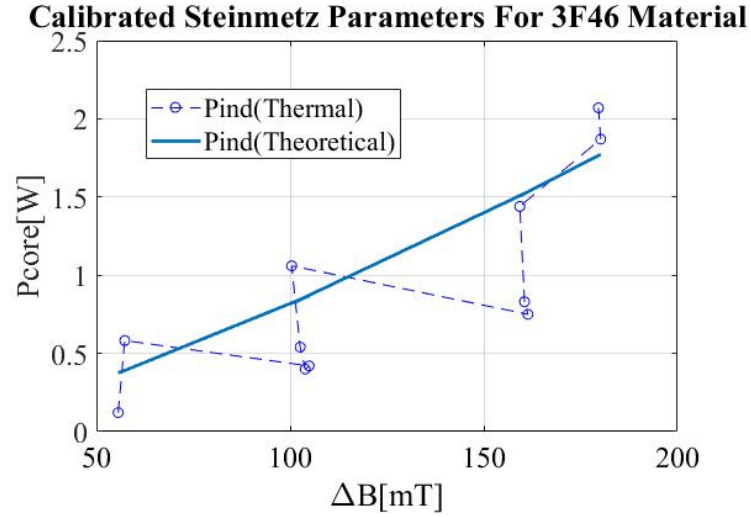
Figure 3.14: Calibrated steinmetz parameter k_{fe}, α and β for 3F46 material.

3.3 Predicted Efficiency Across Wide Input Voltage Range

Based on the augmented state-space modeling and the refined loss model, the predicted

efficiency and loss breakdown of four topologies, including QSW buck, three-level buck,

reconfigurable hybrid switched capacitor buck and four level buck converter, across full input range, are shown below.

All the converters utilize GaN transistors (EPC2023) and planar inductor design (6mm×7mm×1mm). The augmented state-space modeling is applied in these converters to obtain accurate converter waveforms. Loss model with calibrated dynamic on-resistance of GaN transistors and steinmetz parameter for 3F46 ferrite material are utilized to calculate the loss of converter for each operating condition. The input voltage range is 5 V to 20 V, the output voltage is 4 V, and the output current is 10 A.
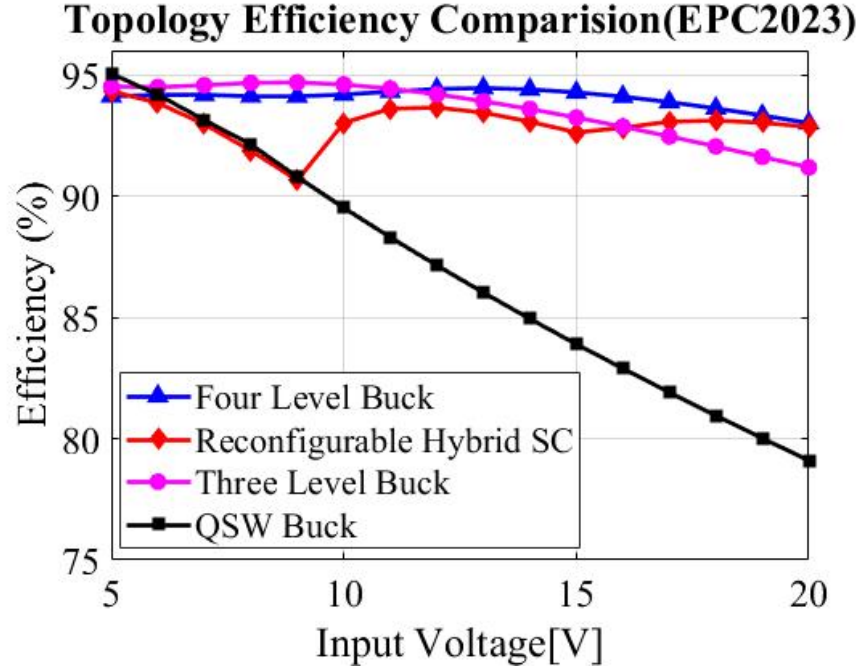
Figure 3.15: Predicted efficiency of QSW buck, three-level buck, reconfigurable hybrid switched capacitor and four level buck converter, across full input voltage range at output voltage $V_{\text{OUT}} = 4\,V$, output current $I_{\text{OUT}} = 10\,A$.

As shown in the Fig. 3.16, the QSW-ZVS buck converter achieves its highest efficiency when the input voltage is at minimum, but the efficiency drops quickly as input voltage rises due to the increasing core loss. The three-level buck converter achieves highest efficiency at 2:1 step-down conversion ratio where the inductor current ripple is minimized. The reconfigurable hybrid switched capacitor converter achieves high efficiency at minimum input
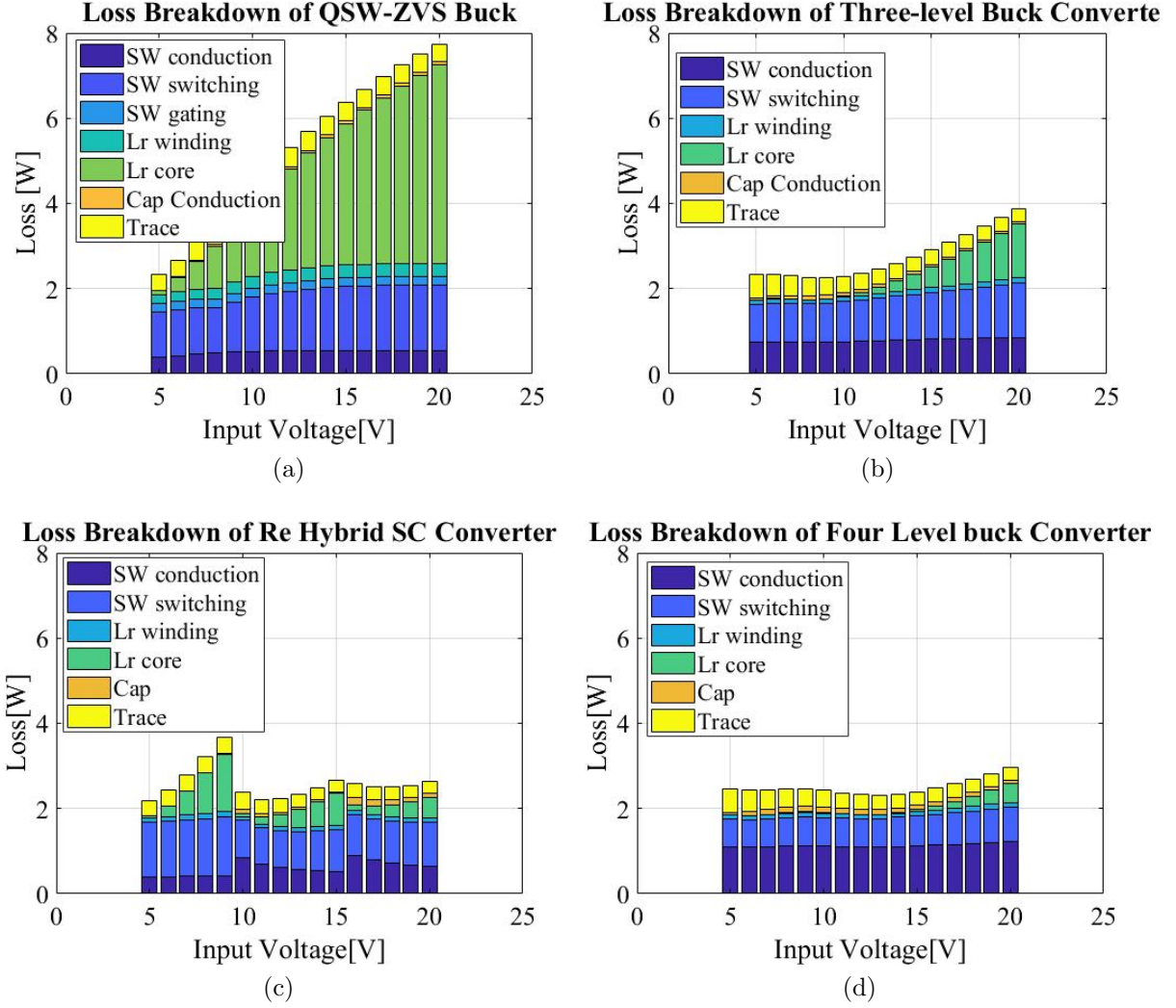
Figure 3.16: Loss breakdown of four buck converter topologies across full input voltage range at output voltage $V_{\text{OUT}} = 4$ V, output current $I_{\text{OUT}} = 10$ A: (a) QSW-ZVS Buck Converter; (b) Three-Level Buck Converter; (c) Reconfigurable Hybrid Switched Capacitor Converter; (d) Four-Level Buck Converter.

voltage. Its efficiency drops greatly at 2:1 step-down conversion ratio as it operates like a buck converter. For the four-level buck converter, its maximum efficiency is at 3:1 step-down conversion ratio with the minimum inductor current ripple.

Chapter 4

High-Efficiency Nominal 2-to-1 Step-Down Converter Design

As shown in the Chapter 3, among five topology candidates, the three-level buck converter achieves highest efficiency at 2:1 conversion ratio scenario, due to its minimum inductor current ripple. Therefore, for battery charger application with the nominal operating point (input voltage $V_{\mathrm{IN}} = 8.5\,V$, output voltage $V_{\mathrm{OUT}} = 4\,V$, and output current $I_{\mathrm{OUT}} = 10\,A$), the three-level buck converter is best candidate. This chapter presents a three-level buck converter design that achieves both high power density (including low profile) and high efficiency across a wide range of input voltages, especially at 2:1 conversion ratio. The design methodology utilizes the augmented state-space modeling to accurately predict the converter waveforms and performance. To achieve high power density, a custom-shaped planar PCB-integrated inductor is designed, whose geometry is optimized using 3D finite-element analysis (FEA) to minimize losses. A load-dependent variable-frequency operation approach is used to maximize efficiency under different loading conditions. Two prototypes of three-level buck converter have been built. One prototype using EPC2023 GaN transistor with a PCB area of 358 mm² and component height of 1 mm designed is built and tested. This prototype converter achieves a peak efficiency of 98.5% at 2:1 conversion ratio and high overall efficiency at other operating conditions with a power density of 704 W/in³. The other prototype using low-voltage silicon MOSFET (CPF03433) with a PCB area of 310 mm² is also built and tested. For GaN transistor prototype, to maximize efficiency, the converter is designed to achieve zero-voltage switching (ZVS) at light-to-medium loads, while sacrificing

ZVS to reduce transistor conduction and inductor losses. For low-voltage silicon MOSEFT prototype, ZVS is achieved across various load condition to reduce the voltage stress on the device. The on-resistance and output capacitance of the Silicon MOSFET (CPF03433) have also been calibrated with experimental results. Compared with GaN transistor (EPC2023), the silicon MOSFET(CPF03433) perform similar at low current condition, but at high load condition EPC2023 perform much better than the CPF03433.

4.1 Three-Level Buck Converter Topology and Operating Principles
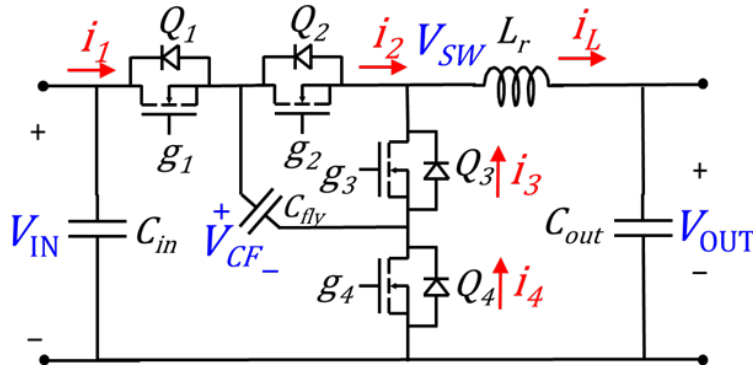
Figure 4.1: The three level buck converter topology.

Multilevel converter with flying capacitors, such as the three-level buck converter shown in Fig. 4.1, were originally proposed for high-voltage and high-power applications [10]. In this work, the three-level buck converter is selected for cellphone battery charging applications to achieve favorable tradeoffs in terms of limited switch count, small passive (inductor and capacitor) volume and high efficiency across a wide input voltage range. In the three-level buck converter of Fig. 4.1, the switches Q_1 and Q_4 operate in a complementary manner with a duty ratio D. Similarly, the switches Q_2 and Q_3 operate in a complementary manner with the same duty ratio. The two groups of switches (Q_1, Q_4) and (Q_2, Q_3) are time-shifted by half the switching period $(T_s/2)$. The output voltage of the three-level buck converter is given by:

$$V_{\text{OUT}} = DV_{\text{IN}} \tag{4.1}$$

Here, V_{IN} and V_{OUT} are the dc input and output voltages of the converter, respectively. With the switches operated as described above, the three-level buck converter operates in three different modes, as shown in Fig. 4.2. When the required conversion ratio ($V_{\text{OUT}}/V_{\text{IN}}$) is less than half, the duty ratio D as computed using (4.1) is also less than half, and the switch-node voltage V_{sw} alternates between 0 and $V_{\text{IN}}/2$. When the conversion ratio, and hence the duty ratio D, is equal to half, the switch-node voltage keeps constant at $V_{\text{IN}}/2$. When the conversion ratio, and hence the duty ratio D, is greater than half, the switch-node voltage alternates between V_{IN} and $V_{\text{IN}}/2$. By phase shifting the two pairs of the switches, the switch-node frequency is twice the switching frequency of the transistors. In applications where a wide range of conversion ratios is required, this multi-mode operation of the three-level buck converter reduces the volt-seconds applied to the inductor; hence, potentially reducing its losses when compared to a standard buck converter [11]. Furthermore, as can be seen from Fig. 4.2(a) and (c), the switch-node voltage pulsates at twice the frequency compared to the switching frequency of the transistors, allowing the inductor to be reduced in size.

4.1.1   ZVS Operation of Three-Level Buck Converter

ZVS operation of the three-level buck converter is conceptually similar to that of other ZVS quasi-square-wave (ZVS-QSW) converters [9]. The two bottom switches of the three-level buck converter, Q_3 and Q_4, can achieve ZVS turn-on simply by allowing a sufficiently long dead-time, as these switches commutate at the positive peak of the inductor current (see Fig. 4.2). However, for the top two switches Q_1 and Q_2 to achieve ZVS turn-on, in addition to sufficient dead-time, the inductor current must be allowed to go negative. Therefore, to achieve ZVS for all four switches, the inductor current ripple must be large enough. The

(a) Mode 1 $(D < \frac{1}{2})$ (b) Mode 2 $(D = \frac{1}{2})$ (c) Mode 3 $(D > \frac{1}{2})$
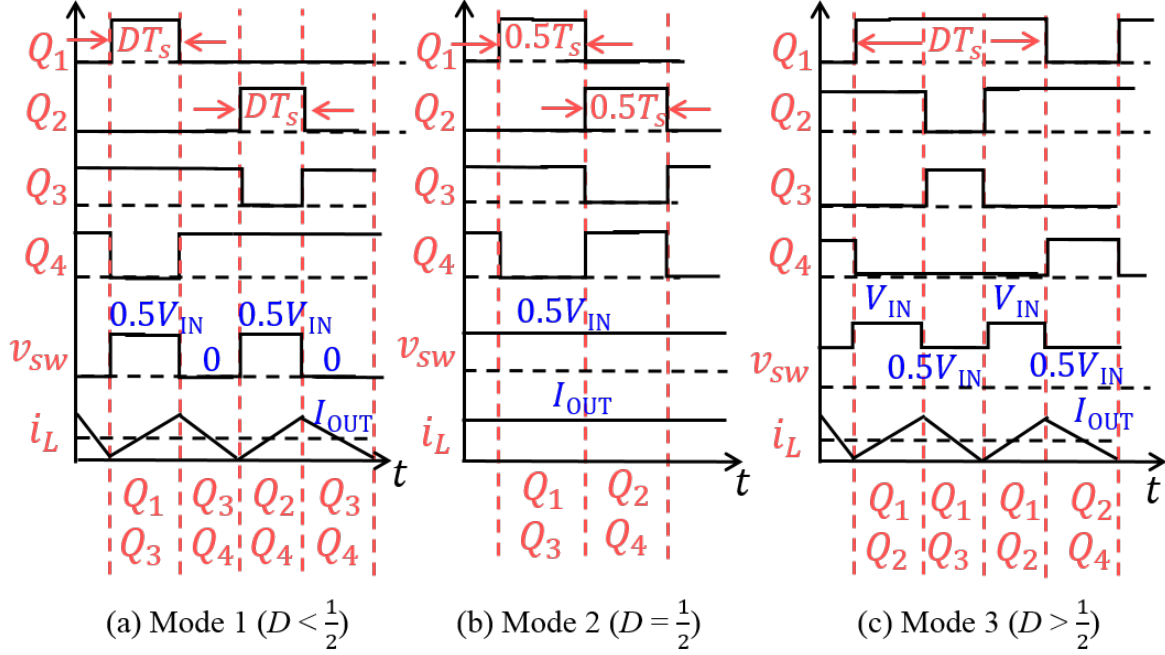
Figure 4.2: Gate signals of Q_1, Q_2, Q_3, Q_4 switch-node voltage and inductor current for duty ratio $D < 0.5, D = 0.5$, and $D > 0.5$.

required ripple value can be achieved through an appropriate combination of the converters inductance and switching frequency. However, the large current ripple required to achieve ZVS introduces additional inductor winding losses and transistor conduction losses. To maintain high efficiency in the presence of this tradeoff, a methodology to optimize the design of a three-level buck converter in terms of its inductance and switching frequency is described in next section.

4.2 Modeling, Design and Optimization Methodology

4.2.1 Augmented State-Space Modeling

The design methodology for the three-level buck converter presented here utilizes the augmented state-space modeling approach (as introduced in Chapter 3) to predict converter waveforms with high accuracy and computational efficiency. As shown in Fig. 4.2, the three-level buck converter has three modes ($D < 0.5, D = 0.5, D > 0.5$). In each mode,
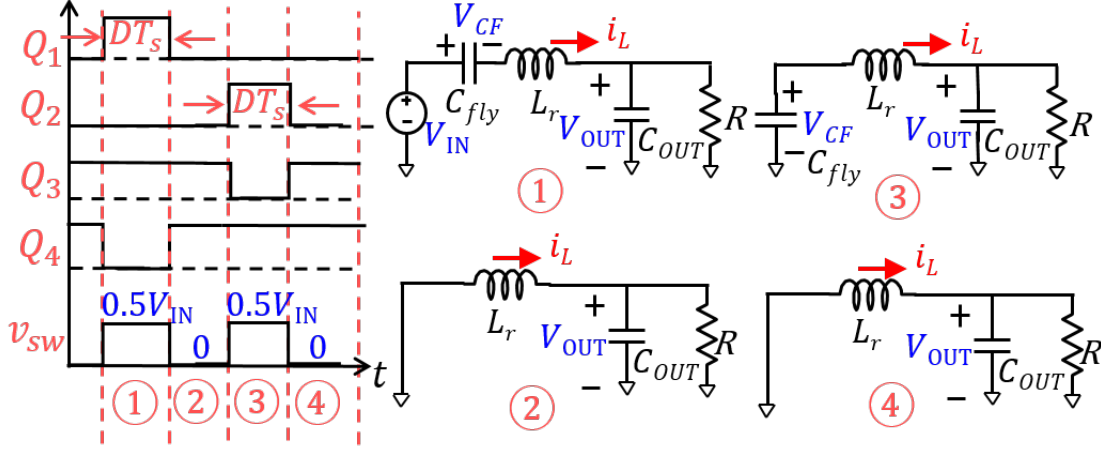
Figure 4.3: Operation and corresponding states of three level buck converter when duty ratio $D < 0.5$.

the converters operation can be described using a sequence of equivalent linear circuits. For example, in the $D < 0.5$ mode three-level buck converter corresponding equivalent circuits are shown in Fig. 4.3. To analyze these circuits, three state variables are considered: the flying capacitor voltage v_{CF}, output voltage v_{OUT}, and inductor current i_L, and state equations are written for each equivalent circuit. For instance, for the first equivalent circuit, the state-space equation is given by

$$
\underbrace{\begin{bmatrix} \dot{V_{CF}} \\ \dot{V_{OUT}} \\ \dot{i_L} \end{bmatrix}}_{\dot{x}} = \underbrace{\begin{bmatrix} 0 & 0 & 1/C_f \\ 0 & -1/(RC_{OUT}) & 1/C_{OUT} \\ -1/L_r & -1/L_r & -R_{on}/L_r \end{bmatrix}}_{A_1} \underbrace{\begin{bmatrix} V_{CF} \\ V_{OUT} \\ i_L \end{bmatrix}}_{x} + \underbrace{\begin{bmatrix} 0 \\ 0 \\ V_{IN}/L_r \end{bmatrix}}_{B_1} \tag{4.2}
$$

Here L_r is the inductance, V_{CF} is the flying capacitance, C_{OUT} is the output capacitance, V_{IN} is the input voltage, and R_{tot} is the sum of the on-resistance of two of the converters switches, the ac resistance of the inductor and the equivalent series resistance (ESR) of the flying capacitor. Similar state-space equations can be written for the other three equivalent circuits in Fig. 4.3. These equations are solved using the augmented state-space modeling approach described in Chapter 3. Using this approach, the periodic steady-state waveforms

of the three-level buck converter are directly predicted without having to go through the startup transients (as in a circuit simulator like Spice), and without the need for integration or matrix inversion (which are required in other state-space based modeling methods). Hence, this approach is computationally very efficient.
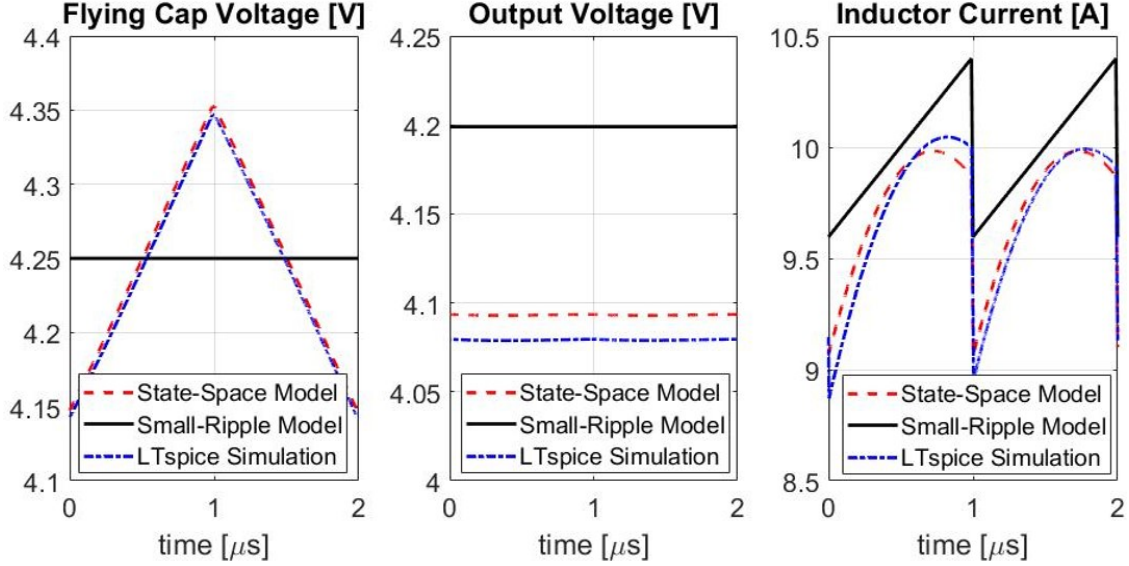
Figure 4.4: Comparison between example waveforms of three-level buck converter as predicted by augmented state-space modeling, small-ripple approximation and LTSpice simulations at input voltage $V_{\text{IN}} = 8.5$ V, output voltage $V_{\text{OUT}} = 4$ V, and output current $I_{\text{OUT}} = 10$ A.

Furthermore, it predicts the converters waveforms to a high degree of accuracy, as shown Fig. 4.4, which compares example waveforms of the three-level buck converter as predicted by the augmented state-space modeling, LTspice simulations, and the conventional small-ripple approximation [25]. As can be seen, unlike waveforms predicted by small-ripple approximation, the augmented state-space predicted waveforms are in excellent agreement with the LTspice simulated waveforms, while requiring only a fraction of the computation time. This enables comprehensive optimization of the three-level buck converters design by sweeping parameters such as switching frequency and passive component values over wide ranges.

4.2.2   Design and Optimization Procedure
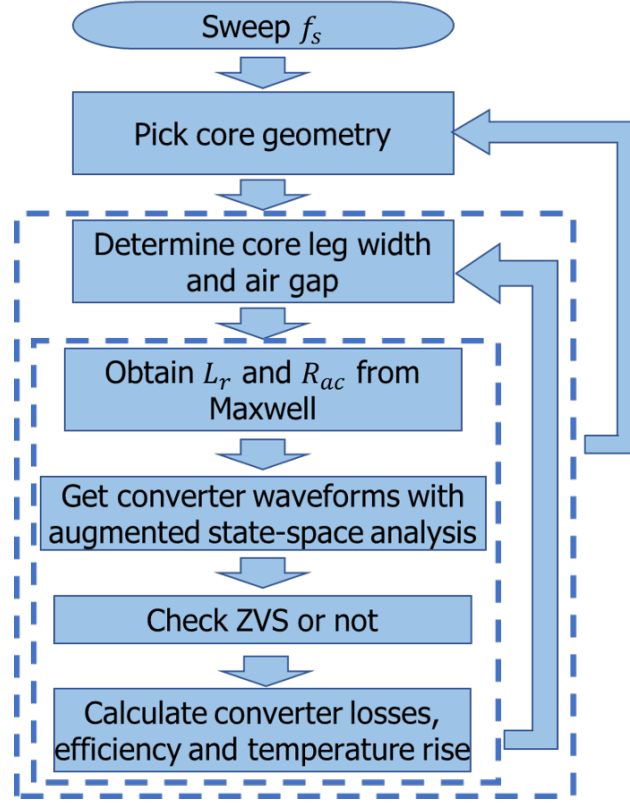
Figure 4.5: Design methodology flow chart.

The design of the three-level buck converter is optimized for its nominal operating point in the cellphone battery charging application considered here ($V_{\mathrm{IN}} = 8.5V$, $V_{\mathrm{OUT}} = 4V$, and $I_{\mathrm{OUT}} = 10A$). The design and optimization procedure is encapsulated by the flowchart shown in Fig. 4.5. The first step in the design methodology is to select the transistors and gate drivers. EPC2023 30-V, 60-A GaN transistors driven by TI LM5113 half-bridge gate drivers are selected. Next, a preliminary PCB layout of the transistors and gate drivers is performed to determine the area suitable for the passive components such as the inductor and capacitors. A range of switching frequencies (1 MHz to 3 MHz, determined by the Ferroxcubes 3F46 ferrite material characteristics) is then considered. For each switching frequency, one inductor core geometry is selected from four candidates EI, E, UI and U with dimensions that

conform to the available PCB area. Fig. 4.6 shows example 3D models of these inductors developed in Ansys Maxwell finite-element analysis (FEA) software. For each core geometry, the core leg width and air-gap are swept in Maxwell to obtain a range of inductances and corresponding ac resistances. The converter waveforms are then obtained using augmented state-space modeling with the Maxwell-obtained inductances and selected frequency. The obtained inductor current waveform is used to ascertain whether the transistors Q_1 and Q_2 achieve ZVS. This is illustrated for the transistor Q_1 in Fig. 4.7 during the dead time t_d, the negative valley of inductor current must be large enough to charge the output capacitance (C_{oss}) of the transistor Q_4 and discharge the output capacitance of Q_1. Assuming that the two transistors are identical and have the same output capacitance, the condition for Q_1 to achieve ZVS turn-on can be mathematically expressed as:

$$q = \int_0^{t_d} i_L(t)\, dt \geq 2C_{oss}\frac{V_{\text{IN}}}{2} \tag{4.3}$$
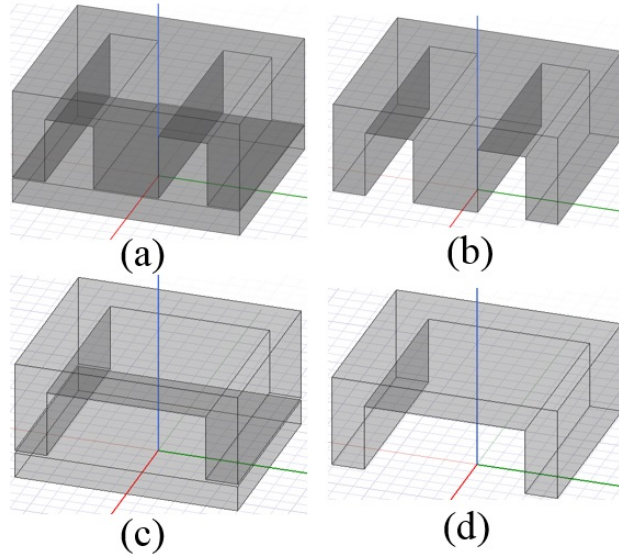
Figure 4.6: Four core geometries considered: (a) EI core; (b) E core; (c) UI core; (d) U core.

The augmented state-space modeling helps evaluate the above ZVS condition with high accuracy. Once the ZVS condition is evaluated, the converter losses including transis-
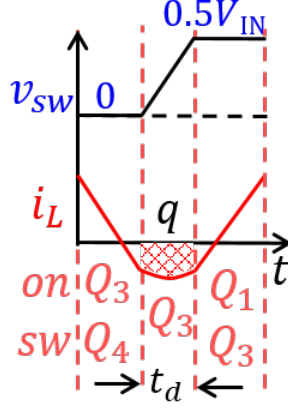
Figure 4.7: ZVS turn-on transition of Q_1.

tor switching and gating losses, capacitor conduction losses and trace losses are calculated based on datasheet. The transistor conduction uses calibrated dynamic on-resistance of GaN device from the previous chapter. The inductor winding losses are estimated using the Maxwell-obtained dc and ac winding resistances, and core losses are estimated using the improved Generalized Steinmetz Equation (iGSE) [25] with calibrated steinmetz parameters from previous chapter. This procedure helps select the inductance value and switching frequency that result in the lowest converter losses at the nominal operating point. The optimal switching frequency to achieve the highest efficiency at other operating points is also determined by applying the above design methodology with the already selected inductance. Through this methodology, it is found that achieving ZVS helps improve the converter efficiency at light-to-medium loads, but at heavy loads, it is more beneficial to sacrifice ZVS in favor of reducing transistor conduction and inductor losses. Also the three-level buck converter exhibits a more balanced loss distribution among its switches and inductor, with potentially easier thermal management.

4.3 Experimental Results

Two prototypes of three-level buck converter designed using this methodology have been built and tested for the following specifications: an input voltage range of 5 V to 20 V, an output voltage range of 3 V to 4.2 V, and a maximum output current of 10 A, corresponding to a maximum output power of around 40 W. One prototype uses GaN transistor (EPC2023), and the other prototype uses Coolstar Technology's CPF03433 14-V, 40-A low-voltage silicon MOSFET.

4.3.1 Three-Level Buck Converter with GaN Transistor

(a)

(b)
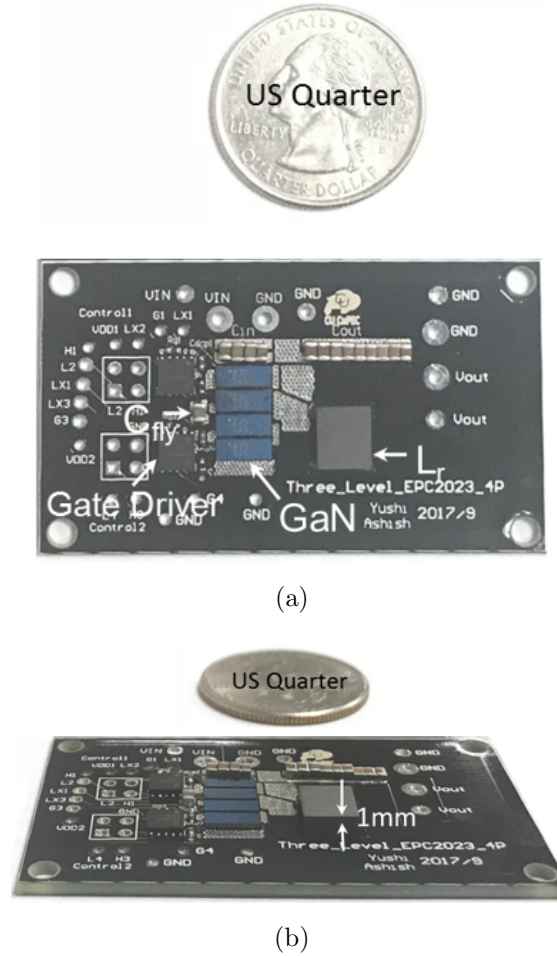
Figure 4.8: Photograph of the prototype three-level buck converter with EPC2023: (a) top view, and (b) side view.

The GaN transistor prototype converter occupies a PCB area of 358 mm^2 and maintains a maximum component height of 1 mm. A photograph of the prototype converter is shown in Fig. 4.8. Details of the components used in the prototype converter are provided in Table. 4.1.

Table 4.1: Components used in the power stage of the GaN prototype three-level buck converter.

Competent	Value	Description
Transistors	-	EPC2023 30-V/60-A eGaN FETs $\times$ 4
Gate Driver	-	TI LM5113 half-bridge gate driver $\times$ 2
L_r	106 nH	EI core, 1 turn, 6mm $\times$ 7m $\times$ 1mm
C_{in}	22 μF	35-V, JB, 0805 $\times$ 2
C_{in}	10 μF	25-V, JB, 0805 $\times$ 2
C_{out}	22 μF	35-V, JB, 0805 $\times$ 2
C_{out}	10 μF	25-V, JB, 0805 $\times$ 2
C_{out}	2.2 μF	25-V, JB, 0805 $\times$ 2

Fig. 4.9 shows the measured waveforms of the proposed three-level buck converter at different operating conditions. The switching node voltage v_{sw} frequency is twice that of the gate signal v_{GS1}, and the flying capacitor voltage v_{CF} remains fairly constant at half of the input voltage ($\frac{V_{IN}}{2}$). Fig. 4.9(a) and (b) shows the measured ZVS performance of the converter at nominal 3 : 1 conversion ratio (V_{IN}=12 V and V_{OUT}=4 V) for output currents of 2 A and 4 A, respectively. This converter achieves ZVS in both operating conditions at different switching frequencies to maximize the efficiency, which is determined by the design methodology. When the output current is higher (4 A), a lower switching frequency (600 kHz) is required to achieve the negative current necessary for ZVS, and vice versa. Fig. 4.9(c) shows the measured waveforms of the three-level buck converter operating at 2:1 conversion ratio (V_{IN}=8 V, V_{OUT}=4 V) with an output current of 1.6 A. As predicted in previous section, at this conversion ratio the switch-node voltage v_{sw} is nearly constant $\frac{V_{IN}}{2}$, while the inductor current ripple is relatively small (around 1A).

Fig. 4.10 shows the measured efficiency of the prototype three-level buck converter

across a wide output current range for two different input voltages and a fixed output voltage of 4 V. The converter achieves highest efficiency at 2 : 1 conversion ratio (V_{IN}=8 V), where the inductor current ripple is minimized. At 3 : 1 conversion ratio (V_{IN}=12 V), the ZVS technique improves the converter efficiency up to 3% higher at light-to-medium loads (5 A). At heavy load, it's better to sacrifice ZVS due to the increasing conduction losses caused by the large inductor current ripple. As can be seen in Fig. 4.10(b), there is an excellent match between the predicted and measured efficiencies. The loss breakdown of the prototype three-level buck converter with GaN transistors based on an analytical loss model is shown in Fig. 4.10(c).

4.3.2 Three-Level Buck Converter with Low-Voltage Silicon MOSFET

The prototype with low-voltage silicon MOSFET (CPF03433) is shown in Fig. 4.11. It occupies a PCB area of 310 mm² and also maintains a maximum component height of 1 mm. It should be noted that the low-voltage silicon MOSFET CPF03433 is a quarter size of EPC2023 GaN transistor. It also uses TI LM5113 half-bridge gate driver. Details of the components used in this prototype converter are provided in Table. 4.2.

Table 4.2: Components used in the power stage of the prototype three-level buck converter with low-voltage silicon MOSFET.

Competent	Value	Description
Transistors	-	CPF03433 14-V/40-A Silicon FETs $\times$ 4
Gate Driver	-	TI LM5113 half-bridge gate driver $\times$ 2
L_r	106 nH	EI core, 1 turn, 6mm $\times$ 7mm $\times$ 1mm
C_{in}	22 μF	35-V, JB, 0805 $\times$ 2
C_{in}	10 μF	25-V, JB, 0805 $\times$ 2
C_{out}	22 μF	35-V, JB, 0805 $\times$ 2
C_{out}	10 μF	25-V, JB, 0805 $\times$ 2
C_{out}	4.7 μF	25-V, JB, 0805 $\times$ 1

Since the breakdown voltage of CPF03433 transistor is 14 V, the converter need to achieve Zero-Voltage-Switching at all operating conditions, otherwise the ringing of the

switching node (v_{sw}) caused by the hard switching will destroy the transistors. Augmented state-space modeling introduced in the previous chapter is used to guarantee ZVS acorss wide load condition at $V_{IN} = 12$ V, $V_{OUT} = 4$ V. Fig. 4.12(a) shows the shows the measured waveforms of the converter at $V_{IN} = 12$ V, $V_{OUT} = 4$ V, and $I_{OUT} = 3$ A, confirming the Zero-Voltage-Switching of all transistors. A further expanded waveform is presented in Fig. 4.12(b) and (c). The switches Q_1 and Q_2 achieve ZVS as the inductor current is sufficiently negative during the dead time to discharge the output capacitor of the MOSFET.

The comparison of two prototypes with GaN transistor (EPC2023) and low-voltage silicon MOSFET (CPF03433) is shown in Table.4.3.

Table 4.3: The comparison of two prototypes with GaN transistor (EPC2023) and low-voltage silicon MOSFET (CPF03433).

Competent	Silicon Prototype	GaN Prototype
Switches	CPF03433 $\times$ 4	EPC2023 $\times$ 4
Switch Size	2.5mm $\times$ 1.25 = 3.1mm^2	6mm $\times$ 2 = 13mm^2
Switch Breakdown Voltage	14 V	30 V
Switch on-resistance R_{on}	1.6 mΩ	1.15 mΩ
Switch gate charge Q_g	11.5 nC	19 nC
Inductor	6mm $\times$ 7mm $\times$ 1mm	6mm $\times$ 7mm $\times$ 1mm
Power stage area	310mm^2	358mm^2

The efficiency comparison of two prototypes is shown in Fig. 4.13. GaN transistor (EPC2023) could operate at both ZVS and non-ZVS condition, for its 30-V breakdown voltage. While the low-voltage silicon MOSFET (CPF03433) can only operate at ZVS condition for its low breakdown voltage. At ZVS condition, silicon MOSFET perform similar to GaN transistor at low current level, but at high load current condition the EPC2023 perform much better than CPF03433.

Since the low-voltage silicon MOSFET (CPF03433) is so new, there is no output capacitance C_{oss} data available from the datasheet. To figure out the actual output capacitance C_{oss} of CPF03433, the total charge during the ZVS transition is calculated when the inductor current is negative, as:

$$Q_{oss} = \int_0^{t_d} i_L(t)\, dt = 2C_{oss}V_{\mathrm{DS}} \tag{4.4}$$

For CPF03433, $V_{\mathrm{DS}} = 6$ V, $Q_{oss} = 12.6$ nC, and $C_{oss} = 2.1$ nF.

The on-resistance R_{on} of CPF03433 is measured as the slope of the switching node voltage v_{sw}. The measured R_{on} is 3 mΩ. With the calibrated C_{oss} and R_{on}, the predicted efficiency based loss model matches well with the experimental measured results, as shown in Fig. 4.14(a). The loss breakdown of the three-level buck converter with CPF03433 based on an analytical loss model is shown in Fig. 4.14(b).
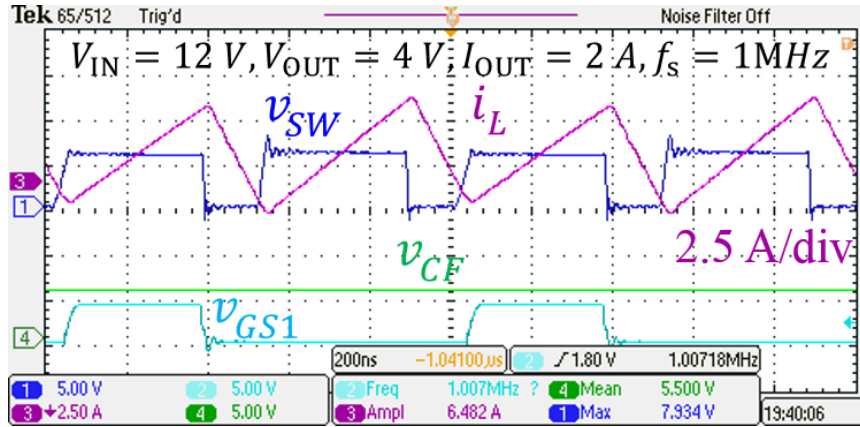
(a)
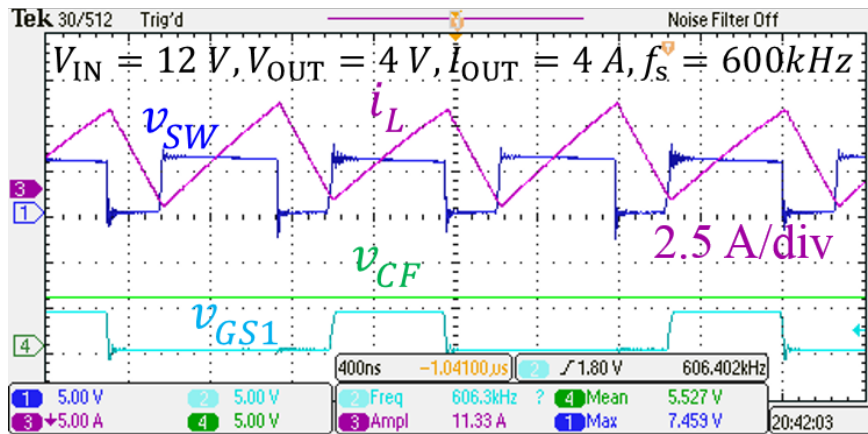
(b)
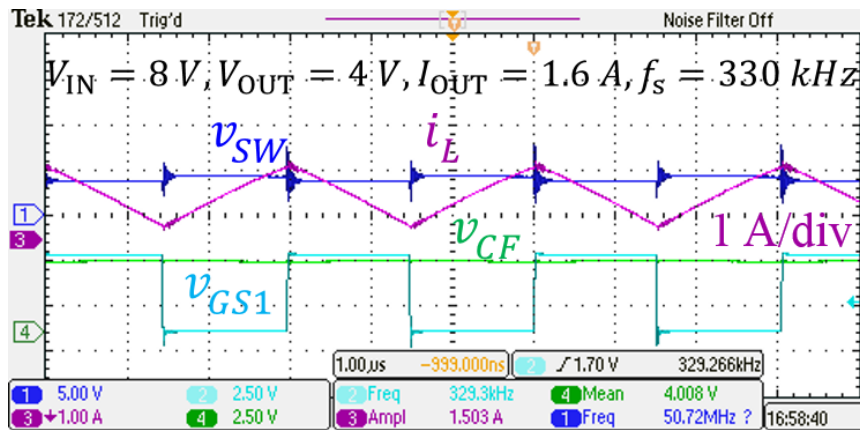
(c)

Figure 4.9: Measured waveforms of the three-level buck converter: (a) ZVS performance of the converter at input voltage V_{IN}=12 V, output voltage V_{OUT}=4 V, and output current I_{OUT}=2 A. (b) ZVS performance of the converter at input voltage V_{IN}=12 V, output voltage V_{OUT}=4 V, and output current I_{OUT}=4 A. (c) Measured waveforms of the converter at input voltage V_{IN}=8 V, output voltage V_{OUT}=4 V, and output current I_{OUT}=1.6 A.
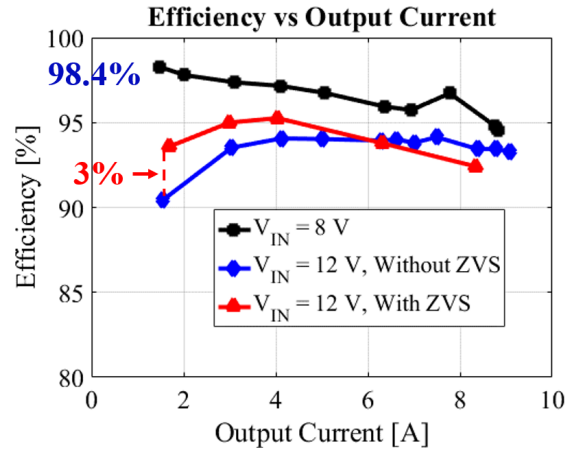
(a)
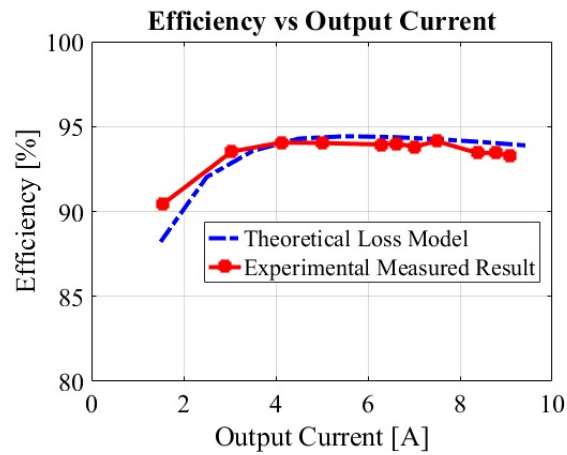
(b)
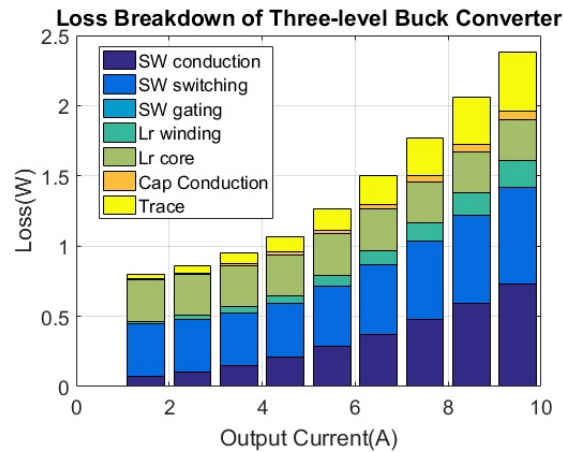
(c)

Figure 4.10: Measured efficiency and loss breakdown of the three-level buck converter: (a) measured efficiency at different operating conditions; (b) comparison of loss model predicted and measured efficiency; (c) loss breakdown of the converter at input voltage V_{IN}=12 V, output voltage V_{OUT}=4 V over full range of output current.
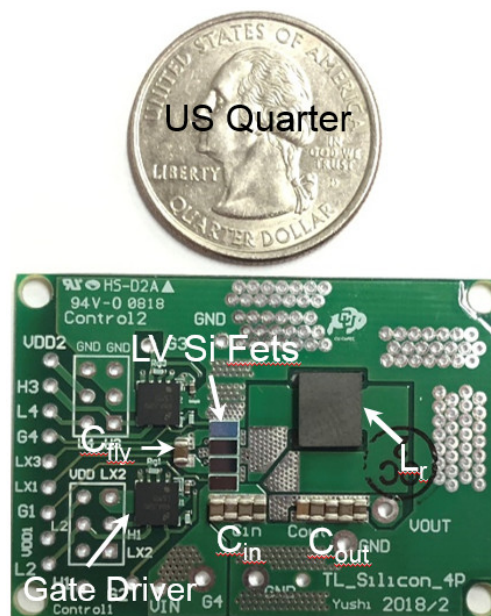
Figure 4.11: Photograph of the prototype three-level buck converter with silicon MOSFETs (CPF03433).
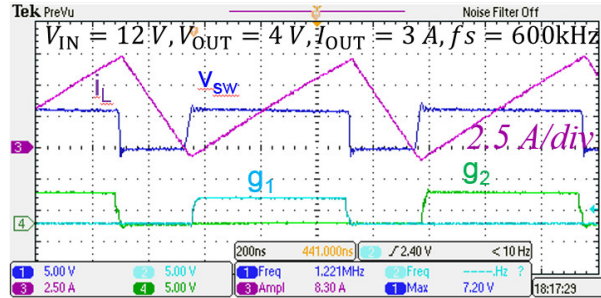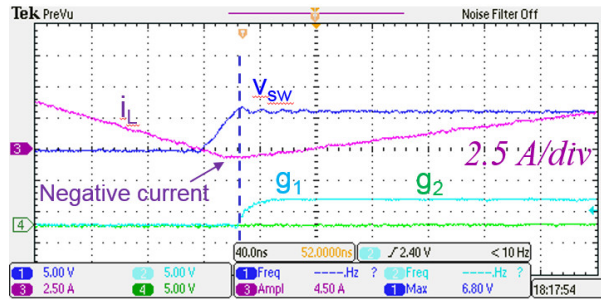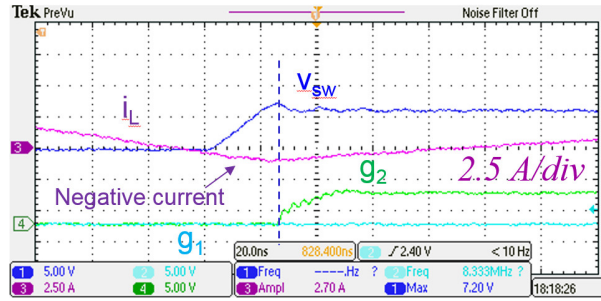
Figure 4.12: Measured waveforms of the three-level buck converter with CPF03433: (a) ZVS performance of the converter at input voltage V_{IN}=12 V, output voltage V_{OUT}=4 V, and output current I_{OUT}=3 A. (b) Expanded waveforms confirming ZVS turn-on of Q_1. (c) Expanded waveforms confirming ZVS turn-on of Q_2.
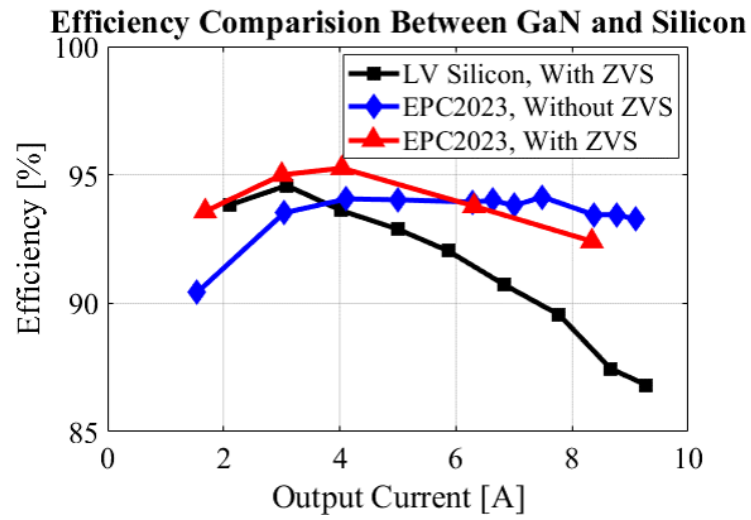
Figure 4.13: Efficiency comparison between GaN and silicon prototype at input voltage V_{IN} = 12 V, output voltage V_{OUT} = 4 V for full load condition.
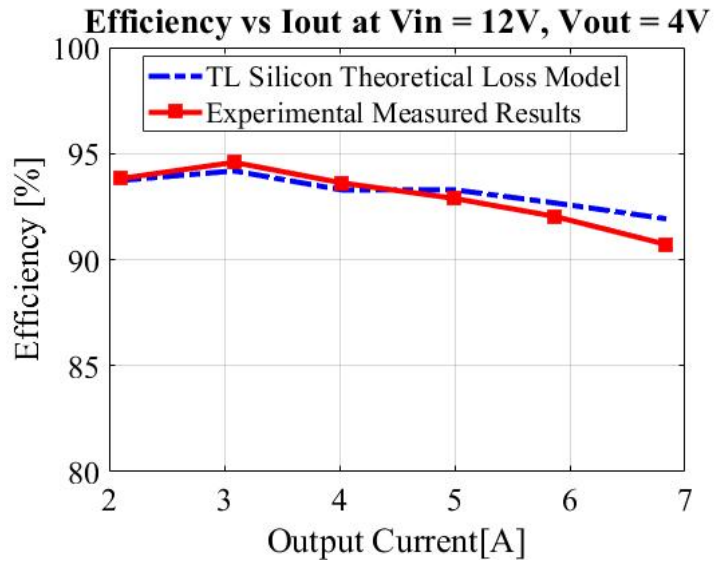
(a)
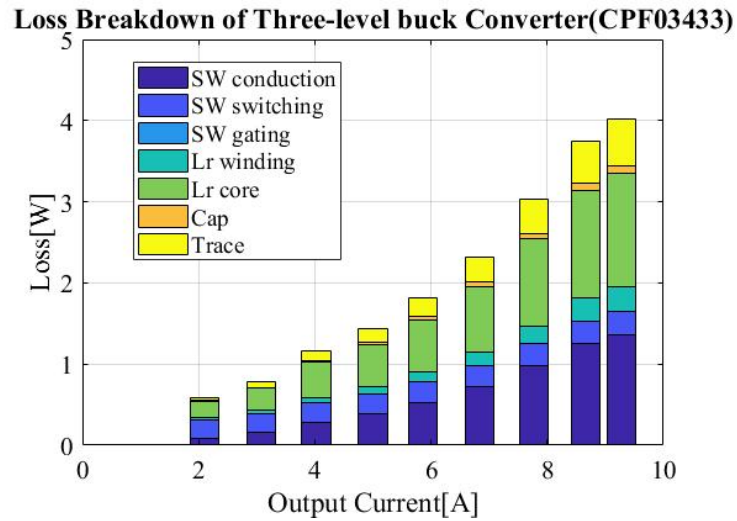
(b)

Figure 4.14: Measured efficiency and loss breakdown of the three-level buck converter with CPF03433: (a) Comparison of loss model predicted and measured efficiency. (c) Loss breakdown of the converter at input voltage V_{IN}=12 V, output voltage V_{OUT}=4 V over full range of output current.

Chapter 5

High-Efficiency Nominal 3-to-1 Step Down Converter Design

As shown in the Chapter 3, compared with other topologies, the four-level buck converter and reconfigurable switched capacitor converter achieve high efficiency when the input voltage is high. The four-level buck converter reaches its maximum efficiency at 3:1 conversion ratio, due to its minimum inductor current ripple. Therefore, for battery charger application with the 3:1 nominal operating point (input voltage $V_{\text{IN}} = 12\,V$, output voltage $V_{\text{OUT}} = 4\,V$, and output current $I_{\text{OUT}} = 10\,A$), the four-level buck converter and reconfigurable switched capacitor converter are good candidates to investigate. This chapter introduces four-level buck and reconfigurable switched capacitor converter topology, utilizes the augmented state-space modeling method to accurately predict the two converters' waveforms and calculate the loss. Also, a custom-shaped planar PCB-integrated inductor is designed to achieve high power density and high efficiency. The efficiency of four-level buck converter is overall above the reconfigurable switched capacitor converter across wide input voltage range, especially at 3:1 conversation ratio when its inductor current ripple is minimized. Due to its high efficiency at 3:1 conversion ratio and relatively flat efficiency curve across full input voltage range, the four-level buck converter topology has been chosen and a prototype with a PCB area of 410 mm² and component height of 1 mm has been built and tested. This converter is designed for an input voltage range of 5 V to 20 V, an output voltage range of 3 V to 4.2 V, and a maximum output current of 10 A.

5.1   Four-Level Buck Converter Topology and Operating Principles
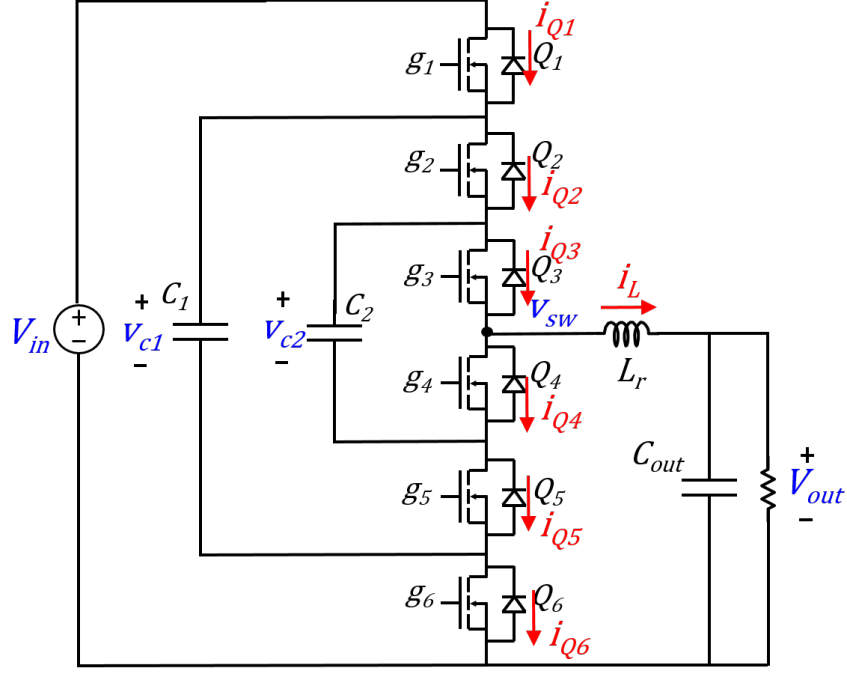
Figure 5.1: Four-level buck converter topology.

The four-level buck converter topology is shown in Fig. 5.1. It utilizes six switches (Q_1, Q_2 ... Q_6) and one inductor. It operates as a PWM converter with duty ratio control. As shown in Fig. 5.2, the switches Q_1 and Q_6 are operated in a complementary manner with a duty ratio D. Similarly, the switches Q_2, Q_5 and Q_3, Q_4 operate in a complementary fashion with the same duty ratio. These three groups of switches, (Q_1, Q_6), (Q_2, Q_5) and (Q_3, Q_4) are switched with time shift of $(\frac{T_s}{3})$. The output voltage of the four-level buck converter is expressed as:

$$V_{\mathrm{OUT}} = D V_{\mathrm{IN}} \tag{5.1}$$

Here, V_{IN} and V_{OUT} are the dc input and output voltages of the converter, respectively. With the switches operated as described above, the four-level buck converter operates in three different modes: when the required conversion ratio ($V_{\mathrm{OUT}}/V_{\mathrm{IN}}$) is less than 1/3, the

Figure 5.2: Gate signals of $Q_1, Q_2, Q_3, Q_4, Q_5, Q_6$ and switch-node voltage of four level buck converter when duty ratio $D < 1/3$ and $1/3 < D < 2/3$.

duty ratio D as computed using (5.1) is also less than $1/3$, and the switch-node voltage V_{sw} alternates between 0 and $V_{\text{IN}}/3$. When the conversion ratio, and hence the duty ratio $1/3 < D < 2/3$, the switch-node voltage alternates between $V_{\text{IN}}/3$ and $2/3V_{\text{IN}}$, as shown in Fig. 5.2. When the conversion ratio, and hence the duty ratio $D > 2/3$, the switch-node voltage alternates between $2/3V_{\text{IN}}$ and V_{IN}.

The inductor switching node V_{sw} vary from 0, $V_{\text{IN}}/3$, $2/3V_{\text{IN}}$ and V_{IN} for four levels. Compared with three-level buck converter, the four-level buck converter further reduce the volt-seconds on the inductor by decreasing the voltage stress and switching period of the inductor. The inductor volt-seconds of 4-level buck converter is $\frac{1}{9}$ of 2-level buck converter, resulting to $\frac{1}{9}$ of the inductor current ripple, thus greatly reduces its losses and size. Since the additional switches result in more switches conduction loss and occupies more area, the four-level buck converter is suitable for application with extremely small inductor.

5.2   Augmented State-Space Modeling of Four-Level Buck Converter

Some of literatures of the four-level buck converter analysis can be found in [21–23] and they are all based on small ripple assumption. Here, the augmented state-space modeling method is used to analyze the four-level buck converter waveforms and calculate its losses.

According to the duty ratio ($D = \frac{V_{\text{OUT}}}{V_{\text{IN}}}$), the four-level buck converter operates in three modes: $0 < D < \frac{1}{3}$, $\frac{1}{3} < D < \frac{2}{3}$ and $\frac{2}{3} < D < 1$. For each mode, there are six states of equivalent circuits, corresponding to a particular configuration (on/off) of the switches, as shown in Fig. 5.4. The converter behavior can be expressed in state-space equation (5.2).

$$\dot{x} = Ax + B \tag{5.2}$$

Here, x consists four state variables considered in the topology: flying capacitor C_1 voltage V_{C1}, flying capacitor C_2 voltage V_{C2}, output voltage V_{OUT} and inductor current i_L, as:

$$x = \begin{bmatrix} V_{C1} \\ V_{C2} \\ V_{OUT} \\ i_L \end{bmatrix} \tag{5.3}$$

For three modes, there are eight state matrix A and B describing the circuit in total:

$$A_{145} = \begin{bmatrix} 0 & 0 & 0 & \frac{1}{C_1} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{RC_O} & \frac{1}{C_O} \\ \frac{-1}{L_r} & 0 & \frac{-1}{L_r} & \frac{-R_{on}}{L_r} \end{bmatrix}, A_{456} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{RC_O} & \frac{1}{C_O} \\ 0 & 0 & \frac{-1}{L_r} & \frac{-R_{on}}{L_r} \end{bmatrix} \tag{5.4}$$

$$A_{246} = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{C_1} \\ 0 & 0 & 0 & \frac{1}{C_2} \\ 0 & 0 & \frac{-1}{RC_O} & \frac{1}{C_O} \\ \frac{1}{L_r} & \frac{-1}{L_r} & \frac{-1}{L_r} & \frac{-R_{on}}{L_r} \end{bmatrix}, A_{356} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{C_2} \\ 0 & 0 & \frac{-1}{RC_O} & \frac{1}{C_O} \\ 0 & \frac{1}{L_r} & \frac{-1}{L_r} & \frac{-R_{on}}{L_r} \end{bmatrix} \quad (5.5)$$

$$A_{135} = \begin{bmatrix} 0 & 0 & 0 & \frac{1}{C_1} \\ 0 & 0 & 0 & \frac{-1}{C_2} \\ 0 & 0 & \frac{-1}{RC_O} & \frac{1}{C_O} \\ \frac{-1}{L_r} & \frac{1}{L_r} & \frac{-1}{L_r} & \frac{-R_{on}}{L_r} \end{bmatrix}, A_{124} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{C_2} \\ 0 & 0 & \frac{-1}{RC_O} & \frac{1}{C_O} \\ 0 & \frac{1}{L_r} & \frac{-1}{L_r} & \frac{-R_{on}}{L_r} \end{bmatrix} \quad (5.6)$$

$$A_{236} = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{C_1} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{RC_O} & \frac{1}{C_O} \\ \frac{1}{L_r} & 0 & \frac{-1}{L_r} & \frac{-R_{on}}{L_r} \end{bmatrix}, A_{123} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{RC_O} & \frac{1}{C_O} \\ 0 & 0 & \frac{-1}{L_r} & \frac{-R_{on}}{L_r} \end{bmatrix} \quad (5.7)$$

$$B_{145} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ \frac{V_{IN}}{L_r} \end{bmatrix}, B_{456} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}, B_{246} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}, B_{356} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (5.8)$$

$$B_{135} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ \frac{V_{IN}}{L_r} \end{bmatrix}, B_{124} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ \frac{V_{IN}}{L_r} \end{bmatrix}, B_{236} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}, B_{123} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ \frac{V_{IN}}{L_r} \end{bmatrix} \quad (5.9)$$

Here L_r is the inductance, C_1 and C_2 is the flying capacitance, C_{OUT} is the output capacitance, V_{IN} is the input voltage, and R_{on} is the sum of the on-resistance of three switches, the ac resistance of the inductor and the equivalent series resistance (ESR) of the flying capacitor.

The A_{123}, B_{123} represents the state matrix of equivalent circuits when switches Q_1, Q_2 and Q_3 are on, as shown in Fig.5.3.
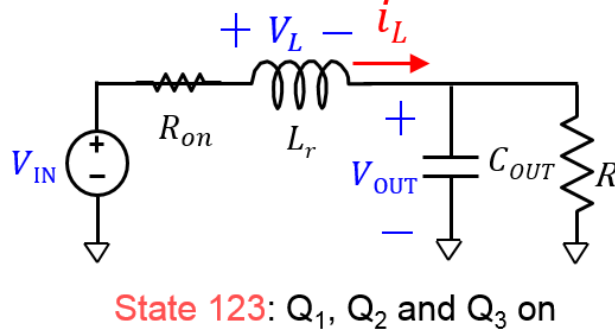
Figure 5.3: Equivalent circuits when switches Q_1, Q_2 and Q_3 are on.
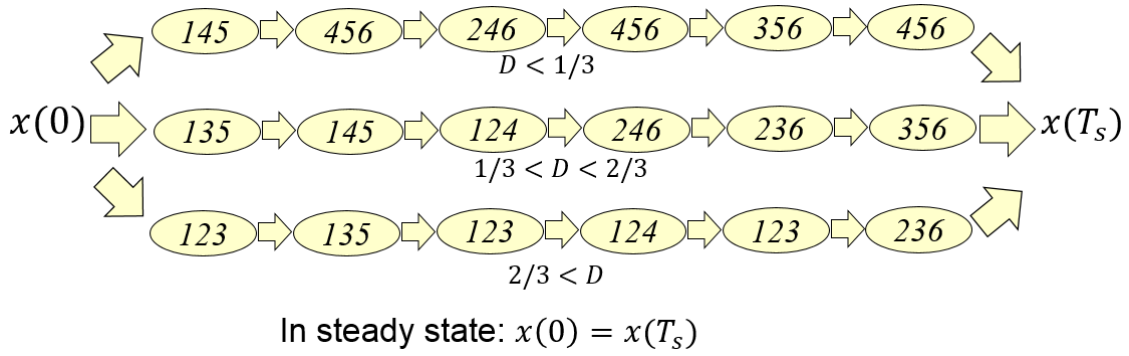
Figure 5.4: Operation and corresponding states of four-level buck converter for different duty ratio.

As shown in Fig. 5.4, in one steady-state period, $0 < t < T_s$, the converter goes through six states, such as Mode$_{135}$, Mode$_{145}$...Mode$_{356}$ when $1/3 < D < 2/3$, and the variable x value backs to its original value:

$$x(0) = x(T_s) \tag{5.10}$$

The state variable and system matrix are augmented as follows:

$$\hat{x} = \begin{bmatrix} x \\ 1 \end{bmatrix} \tag{5.11}$$

$$\hat{A}_i = \begin{bmatrix} A_i & B_i \\ \Theta & 0 \end{bmatrix} \tag{5.12}$$

Here Θ is the zero row-vector of length equal to the size of the system matrix. A new state equation can now be written for the augmented system, and the solution be obtained as:

$$\dot{\hat{x}} = \hat{A}_i \hat{x} \tag{5.13}$$

Using this approach, the steady-state waveforms of the four-level buck converter are directly predicted without having to go through the start-up transients, integration and matrix inversion. Hence, it predicts the converters waveforms efficiently and with high degree of accuracy. The Fig. 5.5 shows at $V_{\text{IN}} = 12V, V_{\text{OUT}} = 4V, I_{\text{OUT}} = 10A$, the switches ($Q_1$ to Q_6) current, the fly capacitor voltage V_{c1} and V_{c2}, corresponding fly capacitor C_1 current i_{c1} and inductor current i_L waveforms, based on the augmented state-space modeling method. It can be seen that the switches equally share the current. With the loss model proposed in the Chapter 3, the optimization design can be done by sweeping the design parameters, such as switching frequency and inductor geometry. Also the losses of the converter can be accurately predicted.

5.3   Reconfigurable Switched Capacitor Converter Topology and Operating Principles

Hybrid switched capacitor converter recently gains more and more interest in industry and academia due to its high-power-density and high efficiency in large step-down conversation ratio [35–40]. This section introduces a new reconfigurable switched capacitor converter topology, as shown in Fig. 5.6. This converter operates in three different modes, suitable for various step-down ratio scenarios, with the switching node V_{sw} toggling between 0, V_{IN}, $\frac{V_{\text{IN}}}{2}$ and $\frac{V_{\text{IN}}}{3}$. When $V_{\text{OUT}} < \dfrac{V_{\text{IN}}}{3}$, mode selection switches S_1 and S_2 are off, These three
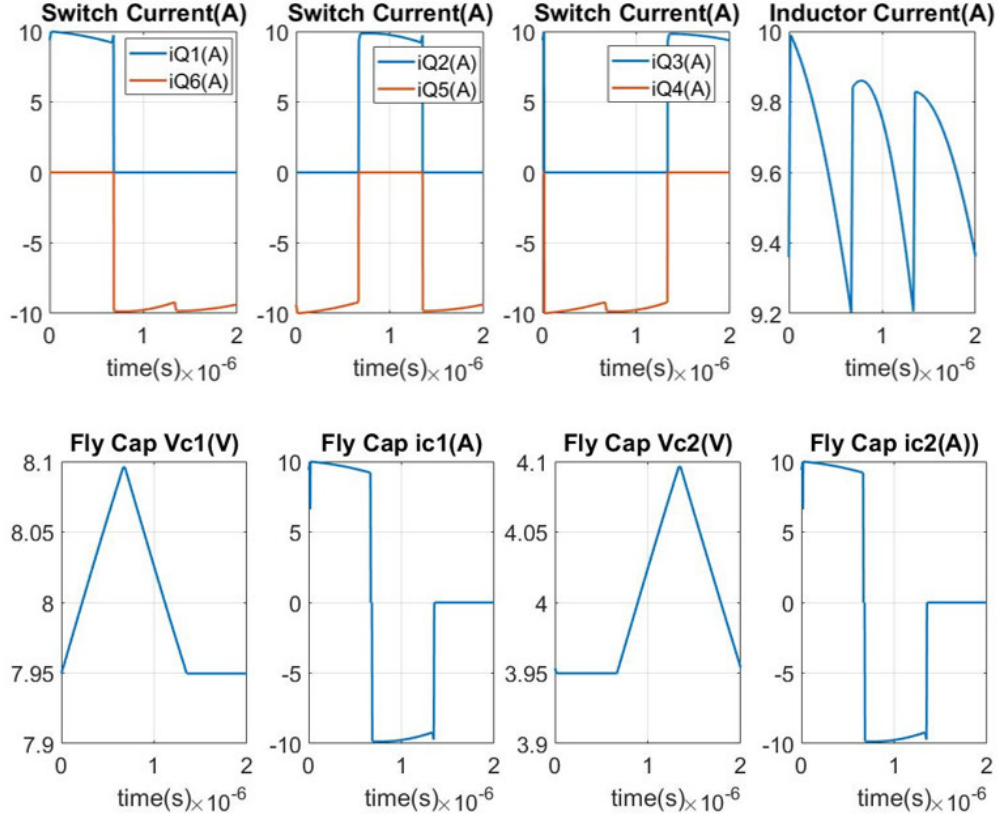
Figure 5.5: Example waveforms of four-level buck converter with augmented state-space modeling at input voltage $V_{\text{IN}} = 12\,V$, output voltage $V_{\text{OUT}} = 4\,V$, and output current $I_{\text{OUT}} = 10\,A$.

groups of switches, (Q_1,Q_2), (Q_3,Q_4) and (Q_5,Q_6) operates in complimentary mode, with duty ratio D. Three capacitors C_1, C_2, and C_3 equally split the input voltage V_{IN}, so that $V_{c1} = V_{c2} = V_{c3} = \dfrac{V_{\text{IN}}}{3}$. V_{sw} toggles between 0 and $\frac{V_{\text{IN}}}{3}$ with a duty ratio of D, as shown in Fig. 5.7. The output voltage of the reconfigurable switched capacitor converter is given by:

$$V_{\text{OUT}} = D\frac{V_{\text{IN}}}{3} \tag{5.14}$$

When $\dfrac{V_{\text{IN}}}{3} < V_{\text{OUT}} < \dfrac{1}{2}V_{\text{IN}}$, mode selection switch S_1 is off, S_2 is on and (Q_1,Q_2) are off. Two groups of switches, (Q_3,Q_4) and (Q_5,Q_6) operates in complimentary mode, with duty ratio D. Two capacitors C_2 and C_3 equally split the input voltage V_{IN}, so that $V_{c2} = V_{c3} = \dfrac{V_{\text{IN}}}{2}$. V_{sw} toggles between 0 and $\frac{V_{\text{IN}}}{2}$ with a duty ratio of D. The output voltage of the reconfig-
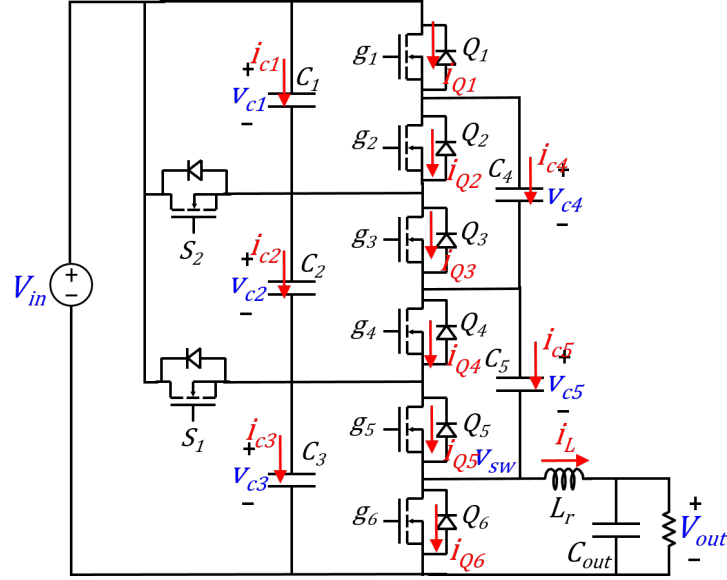
Figure 5.6: Proposed reconfigurable switched capacitor converter topology.
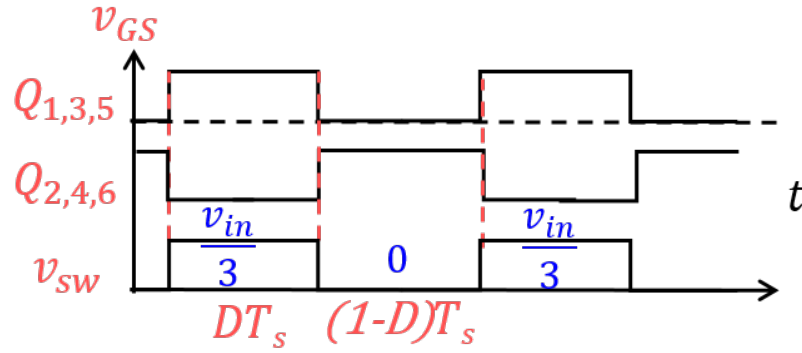
Figure 5.7: Gate signals of $Q_1, Q_2, Q_3, Q_4, Q_5, Q_6$ and switch-node voltage of reconfigurable switched capacitor converter when $V_{\mathrm{OUT}} < \dfrac{V_{\mathrm{IN}}}{3}$.

urable switched capacitor converter is given by:

$$V_{\mathrm{OUT}} = D\frac{V_{\mathrm{IN}}}{2} \tag{5.15}$$

When $\dfrac{V_{\mathrm{IN}}}{2} < V_{\mathrm{OUT}} < V_{\mathrm{IN}}$, mode selection switch S_2 is off, and S_1 is on. (Q_5, Q_6) operates in complimentary mode, with duty ratio D. The input voltage V_{IN} is applied on the C_3, therefore V_{sw} toggles between 0 and V_{IN} with a duty ratio of D. The output voltage of

the reconfigurable switched capacitor converter is given by:

$$V_{\text{OUT}} = DV_{\text{IN}} \tag{5.16}$$

Depending on the input and output voltage ratio, the V_{sw} toggles between V_{IN}, $V_{\text{IN}}/2$, or $V_{\text{IN}}/3$ and 0. This multi-mode operation mitigates inductor volt-seconds and loss. Compared with four-level buck converter with three switches in series, it utilizes less switches in series, thus reduces the switch conduction loss. More details of the loss model for the reconfigurable switched capacitor converter is provided in the next section.

5.4 Augmented State-Space Modeling of Reconfigurable Switched Capacitor Converter

There are many literatures discussing the loss model of the hybrid switched capacitor converter [41–43]. A common way to estimate the capacitor and switches conduction loss is to utilize the average current through the capacitor and switches during the operation as the component RMS current [44]. The capacitor hard charging/discharging loss is estimated with charge flow analysis [44]. Unfortunately, it's quite difficult to derive the analytical expressions to calculate the losses, especially for the hybrid switched capacitor converter topology. The augmented state-space modeling, which numerically estimates the capacitor voltage and inductor current waveforms, can be applied in this hybrid switched capacitor converter to calculate the loss of converter.

When $V_{\text{OUT}} < \frac{V_{\text{IN}}}{3}$, with the S_2 and S_1 mode switch off, the converter is operated in two modes: Mode$_{135}$ with Q_1, Q_3, Q_5 on and Mode$_{246}$ with Q_2, Q_4, Q_6 on. The equivalent circuit of Mode$_{135}$ and Mode$_{246}$ is shown in Fig.5.8. The state-space equation describing the equivalent circuit can be expressed as:

$$A\dot{x} = Bx + C \tag{5.17}$$
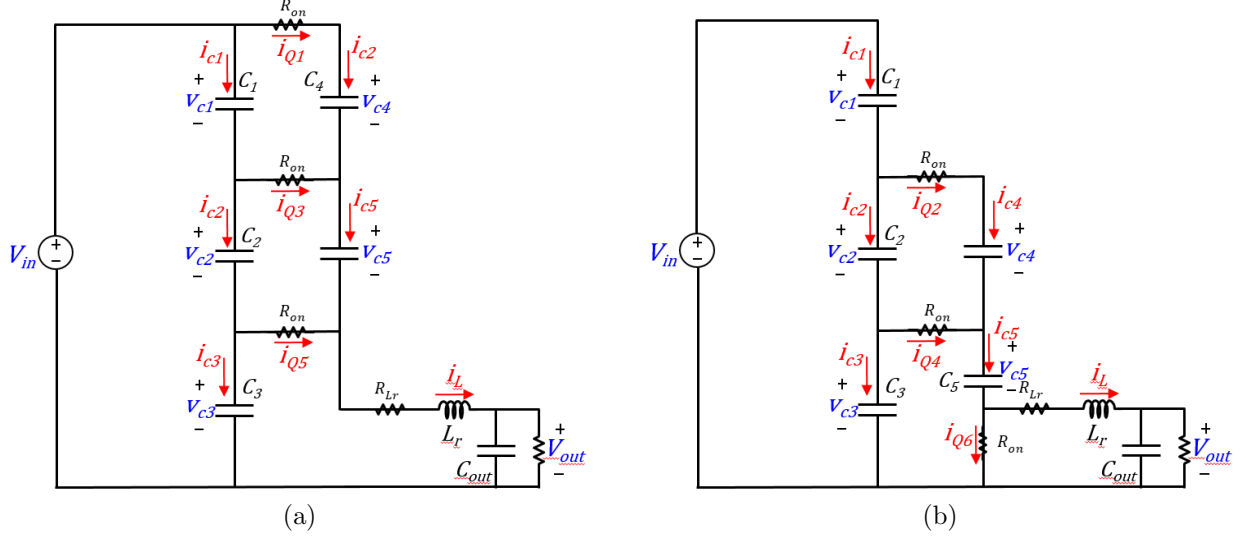
Figure 5.8: The equivalent circuit of (a) Mode$_{135}$ and (b) Mode$_{246}$.

$$\dot{x} = A^{-1}Bx + A^{-1}C \tag{5.18}$$

Here, x includes six state variables in this converter: capacitor C_1 voltage V_{C1}, capacitor C_2 voltage V_{C2}, capacitor C_3 voltage V_{C3}, capacitor C_4 voltage V_{C4}, capacitor C_5 voltage V_{C5}, inductor current i_L and output voltage V_{OUT}:

$$x = \begin{bmatrix} V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \\ V_{C5} \\ i_L \\ V_{OUT} \end{bmatrix} \tag{5.19}$$

State matrix A, B and C are got from six KVL and KCL equations and they are:

$$
A_{135} = \begin{bmatrix}
C & 2C & 0 & C & 0 & 0 \\
C & -C & C & -C & 0 & 0 \\
-R_{on}C & R_{on}C & R_{on}C & 0 & 0 & 0 \\
0 & -3R_{on}C & 0 & 0 & 0 & 0 \\
R_{on}C & 2R_{on}C & 0 & 0 & L_r & 0 \\
0 & 0 & 0 & 0 & 0 & C_o
\end{bmatrix}
\tag{5.20}
$$

$$
B_{135} = \begin{bmatrix}
0 & 0 & 0 & 0 & 1 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 \\
1 & 0 & -1 & 0 & 0 & 0 \\
0 & 1 & 0 & -1 & 1 & 0 \\
-1 & -1 & 0 & 0 & -R_{Lr} & -1 \\
0 & 0 & 0 & 0 & 1 & \frac{-1}{R}
\end{bmatrix}, C_{135} = \begin{bmatrix}
0 \\ 0 \\ 0 \\ 0 \\ V_{\text{IN}} \\ 0
\end{bmatrix}
\tag{5.21}
$$

$$
A_{246} = \begin{bmatrix}
1 & -1 & -1 & C & 0 & 0 \\
1 & 2 & 1 & -1 & 0 & 0 \\
-R_{on}C & -2R_{on}C & R_{on}C & 0 & 0 & 0 \\
R_{on}C & 2R_{on}C & 0 & R_{on}C & 0 & 0 \\
0 & 0 & 0 & R_{on}C & -L_r & 0 \\
0 & 0 & 0 & 0 & 0 & C_o
\end{bmatrix}
\tag{5.22}
$$

$$
B_{246} = \begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 \\
0 & 1 & -1 & 0 & 0 & 0 \\
-1 & -1 & 0 & -1 & R_{on} & 0 \\
-1 & -1 & 0 & 0 & -R_{Lr} & -1 \\
0 & 0 & 0 & 0 & 1 & \frac{-1}{R}
\end{bmatrix}, C_{246} = \begin{bmatrix}
0 \\ 0 \\ 0 \\ V_{\text{IN}} \\ 0 \\ 0
\end{bmatrix}
\tag{5.23}
$$

Here L_r is the inductance, C_1, C_2, C_3, C_4 and C_5 is the flying capacitance, respectively.

C_O is the output capacitance, V_{IN} is the input voltage, R_{on} is the sum of the on-resistance of switch and the equivalent series resistance (ESR) of the flying capacitor, and R_{Lr} is the ac resistance of the inductor.

The steady-state waveforms of each flying capacitor voltage (V_{c1}, V_{c2}... and V_{c5}) and inductor current (i_L) is obtained with augmented state-space modeling mentioned in the Chapter 3. Each capacitor current (i_{c1}, i_{c2}... and i_{c5}) and each switch current (i_{Q1}, i_{Q2}... and i_{Q6}) can be expressed:

$$i_{c,i} = C_i \frac{dV_{c,i}}{dt}$$

$$i_{Q1} = i_{c4}$$

$$i_{Q2} = i_{c4}$$

$$i_{Q3} = i_{c1} - i_{c2} \tag{5.24}$$

$$i_{Q4} = i_{c2} - i_{c3}$$

$$i_{Q5} = i_{c2} - i_{c3}$$

$$i_{Q6} = i_{c5} - i_L$$

The Fig. 5.9 shows at $V_{\mathrm{IN}} = 20$ V, $V_{\mathrm{OUT}} = 4$ V, $I_{\mathrm{OUT}} = 10$ A, the reconfigurable switched capacitor converter's fly capacitor voltage V_{c1}, V_{c2}... and V_{c5}, output voltage V_{OUT}, inductor current(i_L) and each switch current(i_{Q1}, i_{Q2}... and i_{Q6}). Once these voltage and current waveforms are obtained, the loss of the converter can be calculated accurately with loss model introduced in Chapter 3. It can be seen that the RMS value of i_{Q6} is largest among all the switches, which means the bottom switch Q_6 carrying the most current should be designed to have minimum on-resistance. Compared with conventional average charge flow analysis, the augmented state space modeling calculates the ESR conduction loss of capacitors and switches conduction and switching loss in numerical (simulation) way. This is more accurate and easier to apply in various dc-dc converter topologies.
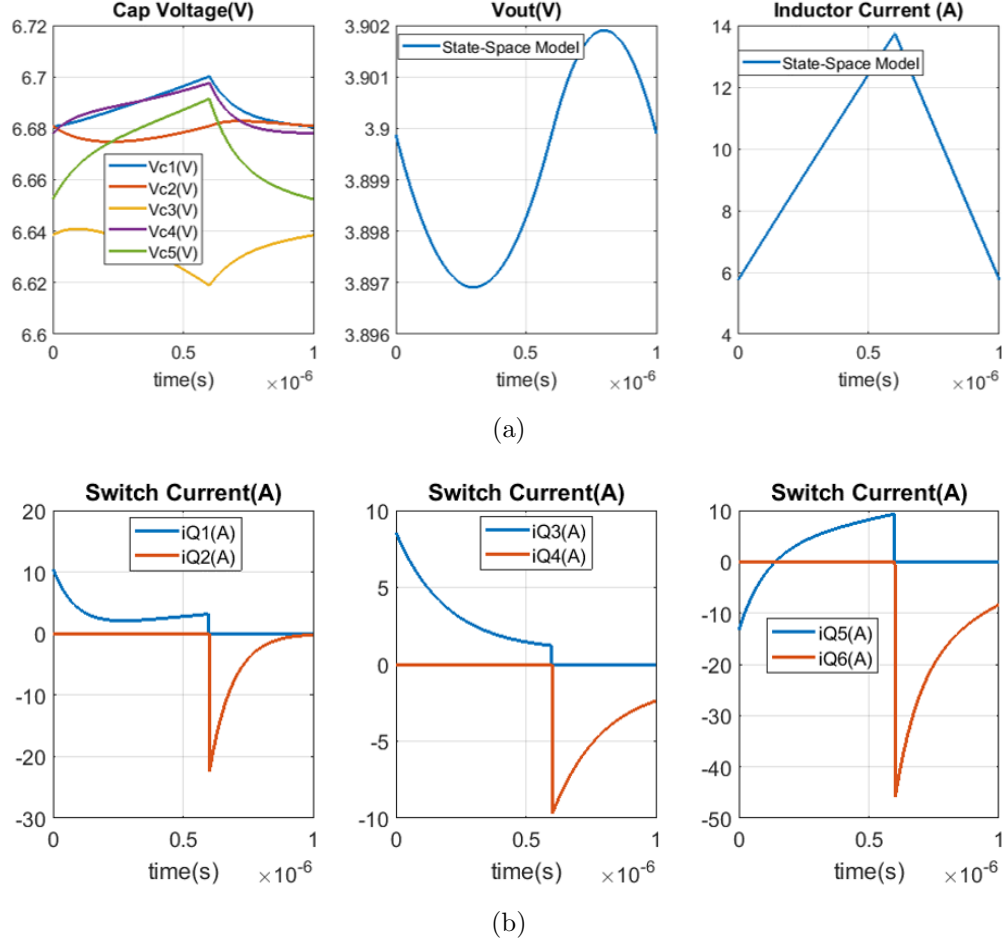
Figure 5.9: Example waveforms of reconfigurable switched capacitor converter with augmented state-space modeling at input voltage $V_{\text{IN}} = 20V$, output voltage $V_{\text{OUT}} = 4V$, and output current $I_{\text{OUT}} = 10A$: (a) flying capacitor voltage (V_{c1}, V_{c2}... and V_{c5}), output voltage V_{OUT}, and inductor current i_L; (b) each switch current (i_{Q1}, i_{Q2}... and i_{Q6}).

5.5   Comparison of Four-Level Buck and Reconfigurable Switched Capacitor Converter

The efficiency calculation and loss model analysis of four-level buck and reconfigurable switched capacitor converter across full input voltage range has also been done and the efficiency plot is shown in Fig. 5.10. Two converters utilize EPC2023 GaN transistors and the same customized planar inductor (6mm×7mm×1mm). The input voltage range is 5 V to 20 V, the output voltage is 4 V, and the output current is 10 A. The loss model of the two converters are shown in Fig.5.11. For four-level buck converter, it achieves maximum effi-
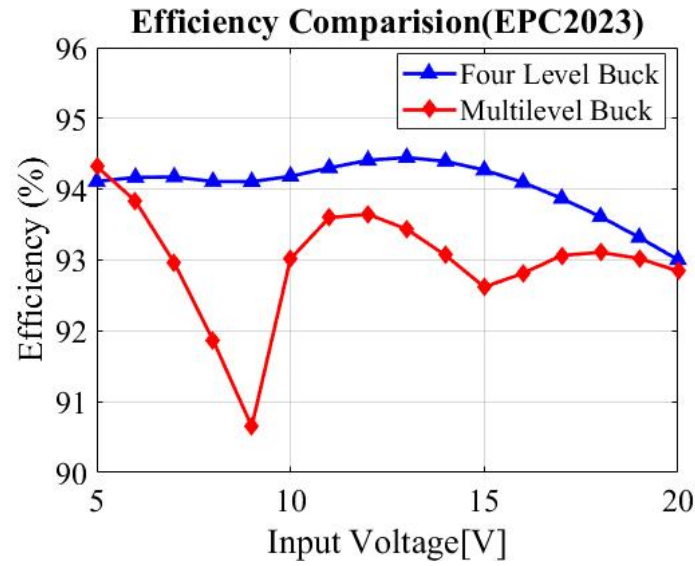
Figure 5.10: Predicted efficiency of reconfigurable switched capacitor and four level buck converter, across full input voltage range at output voltage $V_{\mathrm{OUT}} = 4\,V$, output current $I_{\mathrm{OUT}} = 10\,A$.
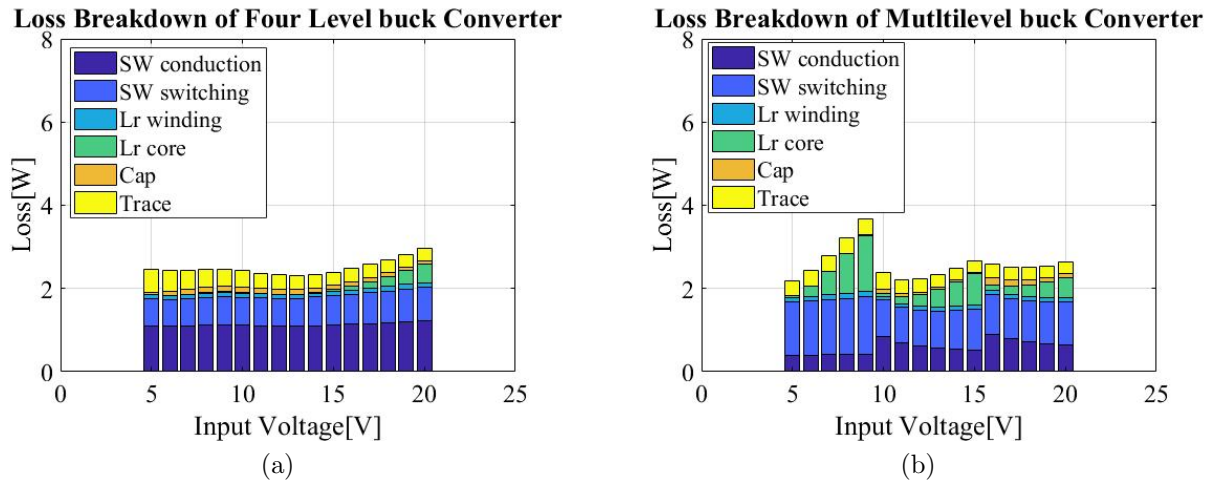

Figure 5.11: Loss breakdown of two buck converter topologies across full input voltage range at output voltage $V_{\mathrm{OUT}} = 4V$, output current $I_{\mathrm{OUT}} = 10A$: (a) Four-Level Buck Converter; (b) Reconfigurable Switched Capacitor Converter.

ciency at 3:1 conversion ratio with the minimum inductor current ripple. The reconfigurable switched capacitor converter converter efficiency drops due to hard charging/discharging of the capacitors and relatively large inductor current ripple. The four-level buck converter's

efficiency is overall above the reconfigurable switched capacitor converter's across wide input voltage range.

5.6   Prototype and Experimental Results
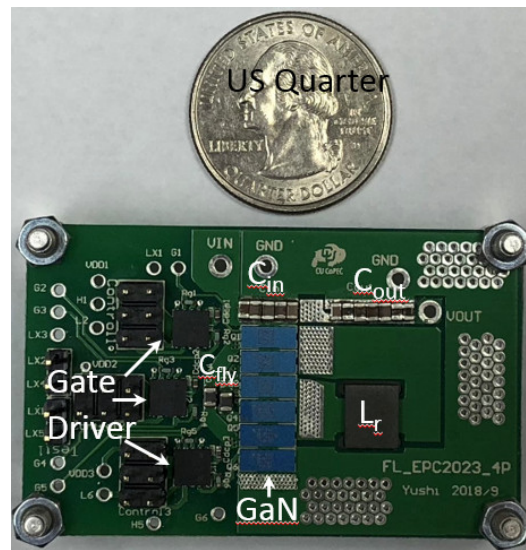
(a)
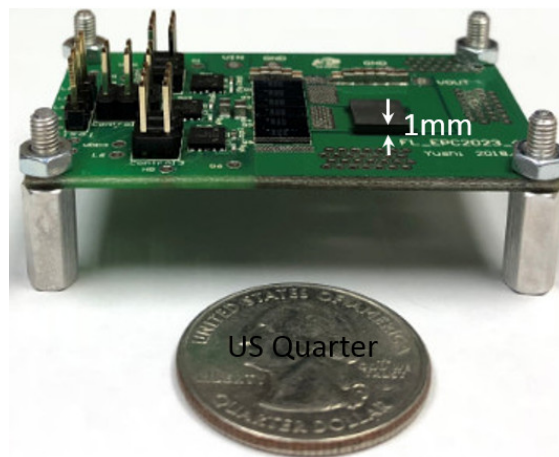
(b)

Figure 5.12: Photograph of the prototype four-level buck converter with EPC2023: (a) top view, and (b) side view.

Based on the above analysis, a prototype of four-level buck converter is designed, built and tested for the following specifications: an input voltage range of 5 V to 20 V, an output

Table 5.1: Components used in the power stage of the four-level buck converter prototype.

Competent	Value	Description
Transistors	-	EPC2023 30-V/60-A eGaN FETs × 6
Gate Driver	-	TI LM5113 half-bridge gate driver × 3
L_r	92 nH	EI core, 1 turn, 6mm × 7m × 1mm
C_{in}	22 μF	35-V, JB, 0805 × 2
C_{in}	10 μF	25-V, JB, 0805 × 2
C_{out}	22 μF	35-V, JB, 0805 × 2
C_{out}	10 μF	25-V, JB, 0805 × 2
C_{out}	2.2 μF	25-V, JB, 0805 × 2

voltage range of 3 V to 4.2 V, and a maximum output current of 10 A, corresponding to a maximum output power of around 40 W. This prototype converter occupies a PCB area of 410 mm^2 and maintains a maximum component height of 1 mm^2. A photograph of the prototype converter is shown in Fig. 5.12. Details of the components used in the prototype converter are provided in Table. 5.1.

Fig. 5.13 shows the measured waveforms of the proposed three-level buck converter at two operating conditions. The switching node voltage v_{sw} frequency is triple that of the gate signal v_{GS1}, and the flying capacitor voltage v_{C1} remains fairly constant at one third of the input voltage ($\frac{V_{IN}}{3}$). Fig. 5.13(a) shows the measured ZVS performance of the converter at V_{IN}=15 V and V_{OUT}=4 V for output currents of 2 A, when the inductor current goes negative. Fig. 5.13(b) shows the measured waveforms of the four-level buck converter operating at 3:1 conversion ratio (V_{IN}=12 V, V_{OUT}=4 V) with an output current of 2 A. As predicted in previous section, at this conversion ratio the switch-node voltage v_{sw} is nearly constant $\frac{V_{IN}}{3}$, while the inductor current ripple is relatively small (around 1A).

Fig. 5.14 shows the measured efficiency of the prototype four-level buck converter across a wide output current range for two different input voltages and a fixed output voltage of 4 V. The converter achieves highest efficiency (97.8%) at 3 : 1 conversion ratio (V_{IN}=12 V), where the inductor current ripple is minimized. As can be seen in Fig. 5.14(b), there is an good match between the predicted and measured efficiencies. The loss breakdown of the
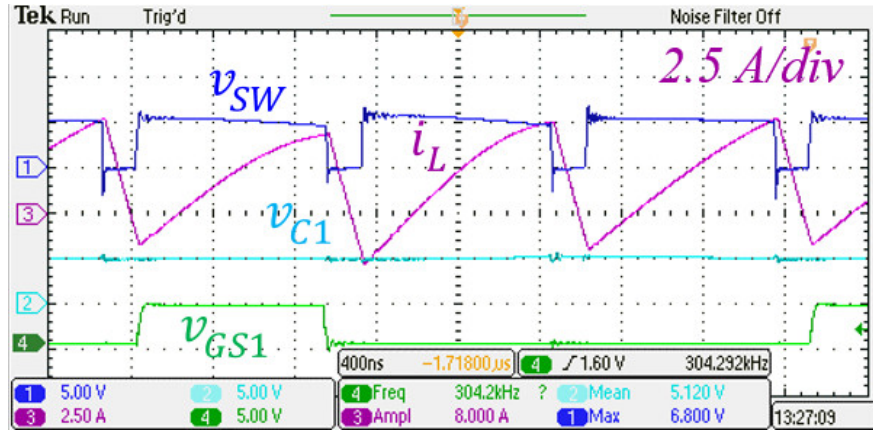
(a)
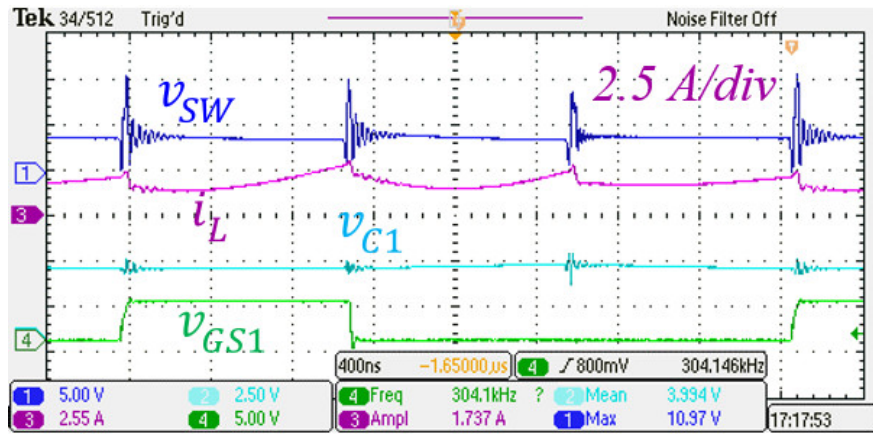
(b)

Figure 5.13: Measured waveforms of the four-level buck converter: (a) ZVS performance of the converter at input voltage V_{IN}=15 V, output voltage V_{OUT}=4 V, output current and I_{OUT}=2 A. (b) Measured waveforms of the converter at input voltage V_{IN}=12 V, output voltage V_{OUT}=4 V, and output current I_{OUT}=2 A.

prototype four-level buck converter with GaN transistors based on an analytical loss model is shown in Fig. 5.14(c). Due to three transistor in series, the conduction loss dominate at large load current condition. The ringing caused by the layout of three switches decreases the efficiency. The measured thermal image of four-level buck converter when operating at V_{IN}=12 V, V_{OUT}=4 V, and I_{OUT}=8 A is shown in Fig. 5.15. The maximum temperature is 45.5°.
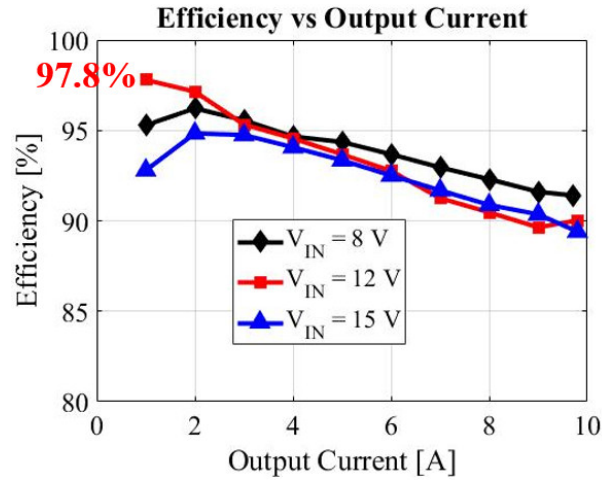
(a)
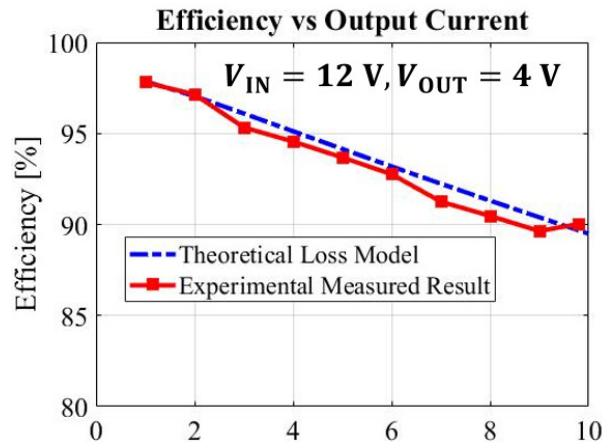
(b)
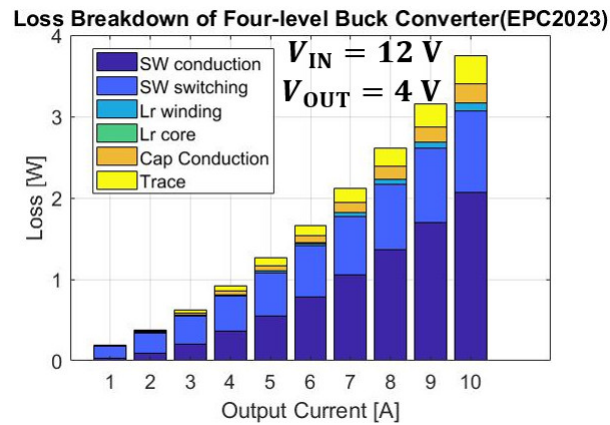
(c)

Figure 5.14: Measured efficiency and loss breakdown of the four-level buck converter: (a) measured efficiency at different operating conditions. (b) Comparison of loss model predicted and measured efficiency. (c) Loss breakdown of the converter at input voltage V_{IN}=12 V, output voltage V_{OUT}=4 V over full range of output current.

Figure 5.15: The measured thermal image of four-level buck converter when operating at input voltage V_{IN}=12 V, output voltage V_{OUT}=4 V, and output current I_{OUT}=8 A.

Chapter 6

Extreme-Power-Density Battery Charger Design

This chapter introduces the design for a extreme-power-density dc-dc converter for fast cellphone battery charging application. Specifically, the converter is required to deliver a maximum output power of 40 W across a 4:1 input voltage range, with its PCB footprint limited to $80\,\text{mm}^2$ and its component height limited to 1 mm. Due to the stringent area (80mm^2) requirement, three alternative topologies a zero-voltage-switching quasi-square-wave (ZVS-QSW) buck converter, a three-level buck converter, and a resonant switched capacitor converter are analyzed, designed and compared in terms of efficiency and power density in this application. Four-level buck converter and multi-level buck converter are not considered in this design for their overabundant switches numbers. An augmented state-space analysis approach is utilized to accurately predict the converter waveforms. The inductors in the three converter topologies are designed as planar PCB-integrated structures with custom-shaped ferrite cores, optimized using a 3D finite-element analysis (FEA) tool. The ZVS-QSW buck converter is predicted to achieve the highest efficiency under the specified area and height constraints. A prototype 40-W 1-MHz buck converter with a PCB area of $79.6\ \text{mm}^2$ and component height of 1 mm designed for an input voltage range of 5 V to 20 V, an output voltage range of 3 V to 4.2 V, and a maximum output current of 10 A is built and tested. The prototype converter achieves a peak efficiency of 96.7% and a power density of 3230 W/in^3.

6.1 Design Methodology
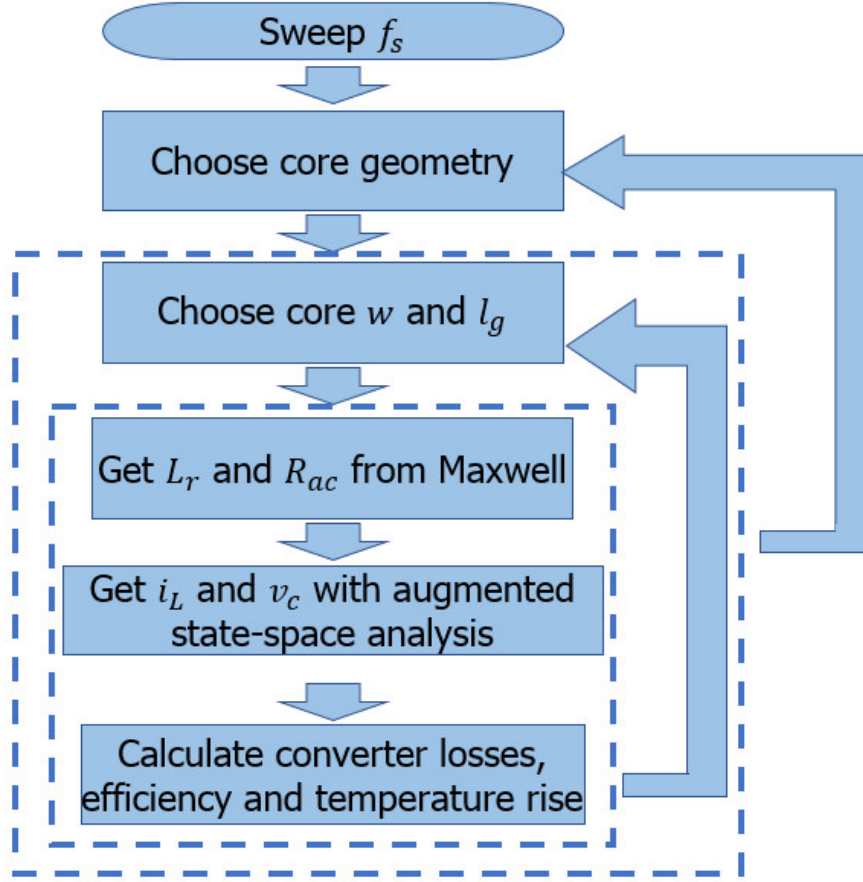
Figure 6.1: Design methodology for 80 mm^2 battery charger design.

The design methodology presented here utilizes augmented state space analysis stated in the previous chapter to predict converter waveforms with high accuracy and computational efficiency. The design of the three candidate converters is optimized for the nominal operating point of the application (input voltage $V_{\text{IN}} = 12\,V$, output voltage $V_{\text{OUT}} = 4\,V$, and output current $I_{\text{OUT}} = 10\,A$). As shown in Fig. 6.1, the first step in the design methodology is to select the transistors and gate drivers to be used in the three converters. EPC2023 30-V, 60-A enhancement-mode GaN transistors driven by a TI LM5113 half-bridge gate driver are selected for the ZVS-QSW buck converter. Since the three-level buck and ReSC converters require two additional switches, these are designed using smaller EPC2015C 40-

V, 53-A GaN transistors driven by two LM5113 drivers. A preliminary PCB layout of the transistors and gate drivers is performed to determine the PCB area available for the passive components. For the design of the ZVS-QSW buck and three-level buck converters, a range of switching frequencies (1 MHz - 3 MHz) is considered. For each switching frequency, the inductors of the two converters are designed using four candidate core geometries EI, E, UI and U with dimensions that conform to the available PCB area. Fig.6.2 shows example 3D models of these inductors developed in Ansys Maxwell finite-element analysis (FEA) software. For each core geometry, the core leg width and air-gap are swept in Maxwell to obtain a range of inductances and the corresponding ac resistances. The converter waveforms are then obtained using augmented state-space analysis with the Maxwell-obtained inductances. Following this, the inductor winding losses are estimated using the Maxwell-obtained dc and ac winding resistances, and core losses are estimated using the improved Generalized Steinmetz Equation (iGSE) [27]. The core material considered in this analysis is Ferroxcube's 3F46, which is optimized for low-loss operation in the frequency range of 1 MHz to 3 MHz. Based on these estimated losses, the thermal performance of the inductors is also evaluated, as shown for an example inductor design in Fig. 6.3. The converter waveforms predicted by augmented state-space analysis are also used to estimate the losses in the other circuit components, including transistor conduction, switching and gating losses, and capacitor conduction losses. The loss model used to compute all the above losses is provided in Chpater 2. By estimating the converter efficiency at the nominal operating point for each switching frequency and core geometry, the optimal combination of switching frequency and core geometry for the ZVS-QSW buck and three-level buck converters is identified, as shown in the next section.

A similar procedure is utilized to design the resonant switched capacitor converter. As described in Chapter 2, the output voltage of the resonant switched capacitor converter can be regulated using its switching frequency and the phase-shift between its top and bottom half-bridges. Given values for the inductance L_r and flying capacitance C_r of the
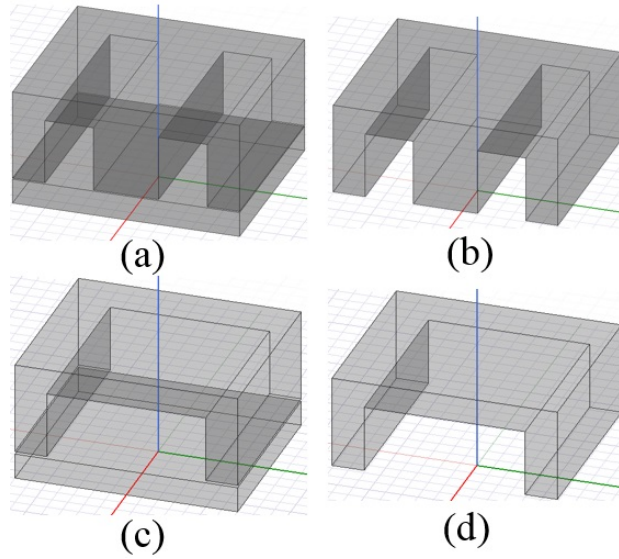
Figure 6.2: Four core geometries considered: (a) EI core; (b) E core; (c) UI core; (d) U core.
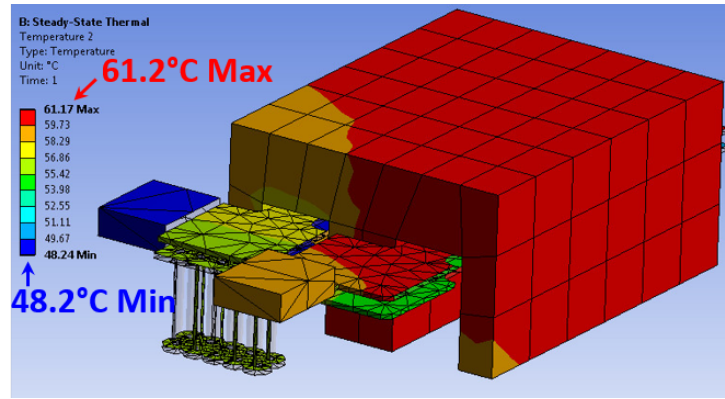

Figure 6.3: Finite-element analysis based thermal map of an example inductor design.

resonant switched capacitor converter, various combinations of phase-shift and frequency can provide the same conversion ratio. However, each combination exhibits different power losses. Therefore, augmented state-space analysis is utilized to identify the optimal phase-shift and switching frequency for each conversion ratio. The inductor of this converter is designed using a 3D FEA-based procedure similar to that described above for the ZVS-QSW buck and three-level buck converters. Details of the resonant switched capacitor converters final optimized design are also provided in the next section.

6.2 Performance Comparison

The performance of the three candidate converter topologies is compared in terms of efficiency and size in Table 6.1. As can be seen, the ZVS-QSW buck converter achieves the highest efficiency at the nominal operating point of the application, while also meeting the area specification of 80 mm^2. The optimized inductor geometry for each topology is shown in Fig. 6.4, and the floor plan for each topology to fit the 80 mm^2 area is shown in Fig. 6.5. A loss breakdown analysis of the three designs is provided in Fig. 6.6. Due to the size limit, the three-level buck and resonant switched capacitor converter can only utilize EPC2015C as transistors with smaller size and larger on-resistance. Although the three-level level buck converter achieves lower efficiency and power density than the ZVS-QSW buck converter, it exhibits a more balanced loss distribution, with potentially easier thermal management. The resonant switched capacitor converter exhibits lower efficiency at this operating point than the other two converters, but offers the most balanced distribution of losses. It may be noted that the performance of these converters, especially the three-level buck and ReSC converter, is limited in the current design by the losses and size of the transistors. These converters can achieve significantly improved performance by utilizing emerging low-voltage transistor technologies featuring superior figures of merit and monolithic integration.

Table 6.1: Predicted performance of the ZVS-QSW buck, three-level buck and resonant switched capacitor converters at the nominal operating point of input voltage $V_{\text{IN}} = 12$ V, output voltage $V_{\text{OUT}} = 4$ V, and output current $I_{\text{OUT}} = 10$ A.

|	ZVS-QSW buck	three-level buck	ReSC
Power Stage Area	79.6mm^2	89.6mm^2	89.6mm^2
Component Height	1mm	1mm	1mm
inductor	180nH, EI core $5 \times 4 \times 1$mm^3	72nH, UI core $4 \times 3.2 \times 1$mm^3	20nH, UI core $4.2 \times 2 \times 1$mm^3
Efficiency	94.7%	93.54%	92.3%
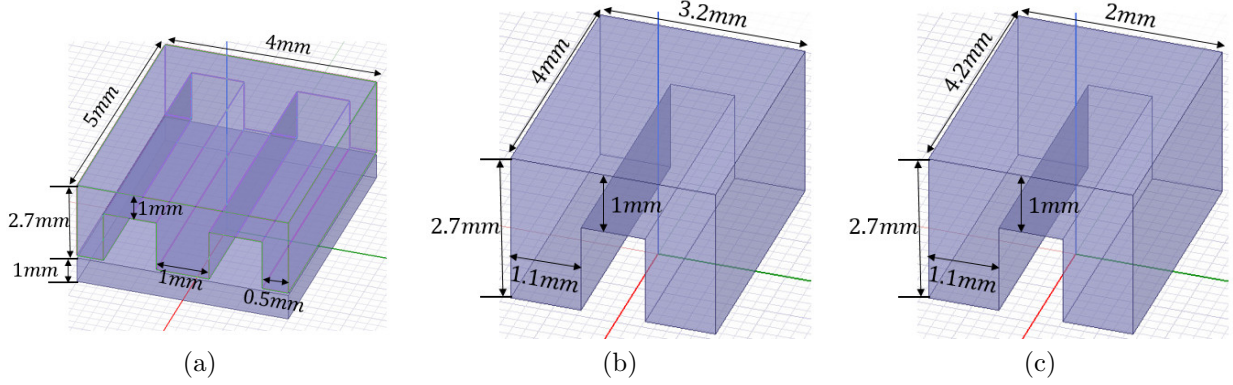
Figure 6.4: Inductor geometry for (a)ZVS-QSW buck, (b)three-level buck and (c)resonant switched capacitor converters.
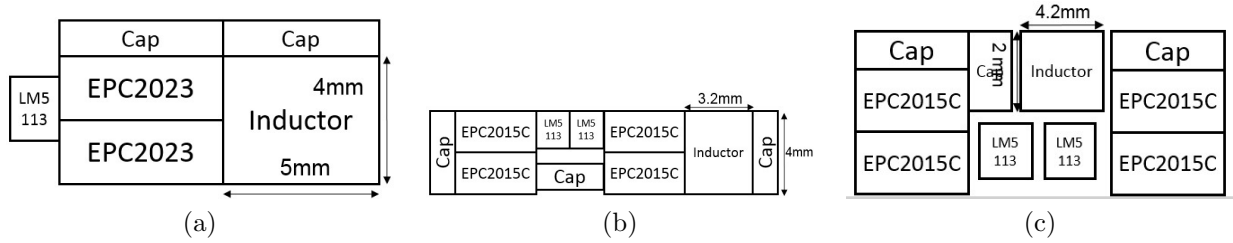

Figure 6.5: Floor plan of the (a)ZVS-QSW buck, (b)three-level buck, and (c)resonant switched capacitor converters.
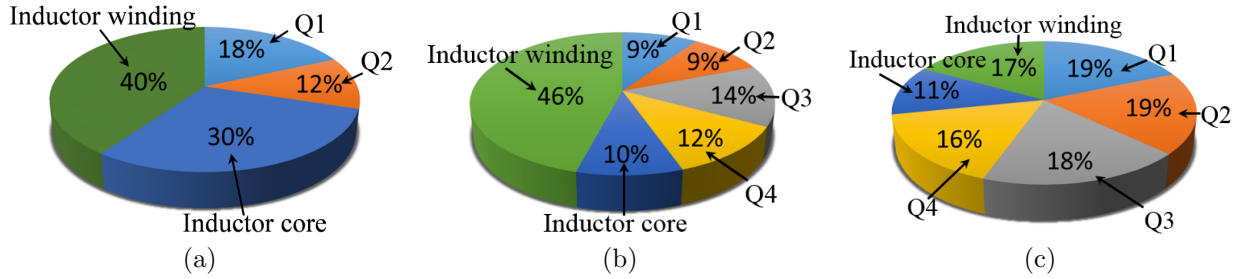

Figure 6.6: Loss breakdown of the (a)ZVS-QSW buck, (b)three-level buck and (c)resonant switched capacitor converters at the nominal operating point of input voltage $V_{\text{IN}} = 12$ V, output voltage $V_{\text{OUT}} = 4$ V, and output current $I_{\text{OUT}} = 10$ A.

6.3   Experimental Result

A prototype ZVS-QSW buck converter designed using the methodology outlined in the previous section is built and tested for the following specifications: an input voltage range of
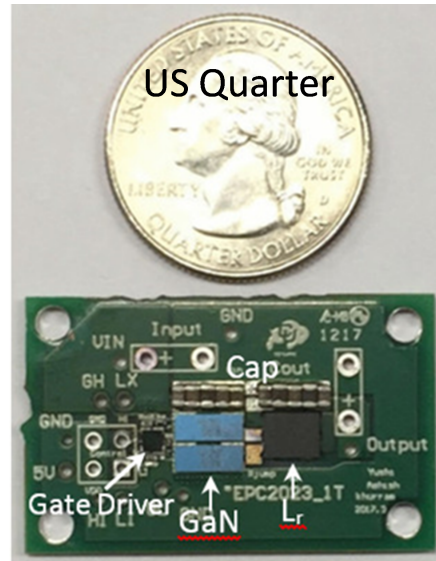
(a)
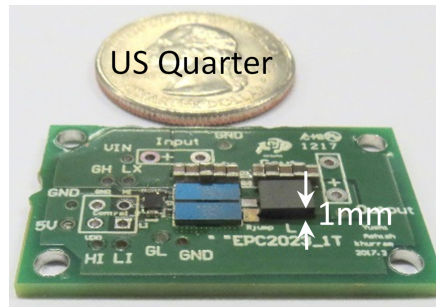
(b)

Figure 6.7: Photograph of the prototype ZVS-QSW buck converter: (a) top view, and (b) side view. Also shown for size comparison is a US Quarter.

5 V to 20 V, an output voltage range of 3 V to 4.2 V and a maximum output current of 10 A, corresponding to a maximum output power of 42 W. This prototype converter occupies a PCB area of 79.6 m^2 and maintains a maximum component height of 1 mm. A photograph of the prototype converter is shown in Fig. 6.7. Details of the components used in the prototype converter are provided in Table. 6.2. Fig. 6.8 shows the measured waveforms of the switch node voltage and inductor current of the prototype converter when operating at its nominal input voltage of 12 V, nominal output voltage of 4 V and output current of 3.5 A. It can be seen that the inductor current is allowed to become negative, enabling ZVS of the top

Table 6.2: Components used in the power stage of the prototype ZVS-QSW buck converter

Component	Value	Description
Transistors	-	EPC2023 30-V/60-A eGaN FETs
Gate Driver	-	TI LM5113 half-bridge gate driver
L_r	184 nH	EI core, 1 turn 5mm × 4mm × 1mm
C_{in}	22 μF	35-V, JB, 0805 × 1
C_{in}	10 μF	25-V, JB, 0805 × 2
C_{in}	2.2 μF	25-V, JB, 0805 × 2
C_{out}	22 μF	35-V, JB, 0805 × 2
C_{out}	10 μF	25-V, JB, 0805 × 2
C_{out}	2.2 μF	25-V, JB, 0805 × 1

transistor. ZVS of the bottom transistor is ensured by appropriately selecting the dead-time between the high-side and low-side gate signals. The measured efficiency of the prototyped converter at four different conversion ratios is shown in Fig. 6.9. The converter achieves a peak efficiency of 96.7% and a power density of 3230 W/in^3.
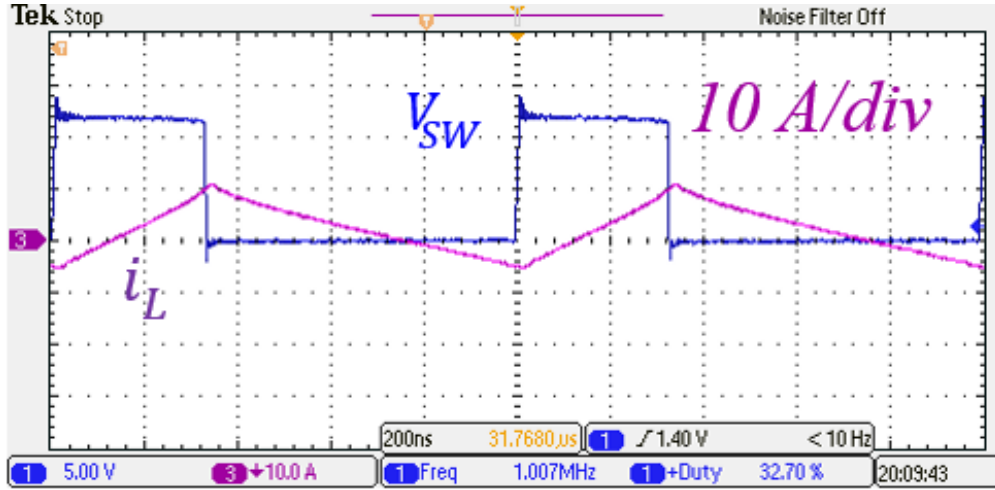
Figure 6.8: Measured waveforms of switch node voltage and inductor current when operating at input voltage $V_{\text{IN}} = 12$ V, output voltage $V_{\text{OUT}} = 4$ V, and output current $I_{\text{OUT}} = 3.5$ A.
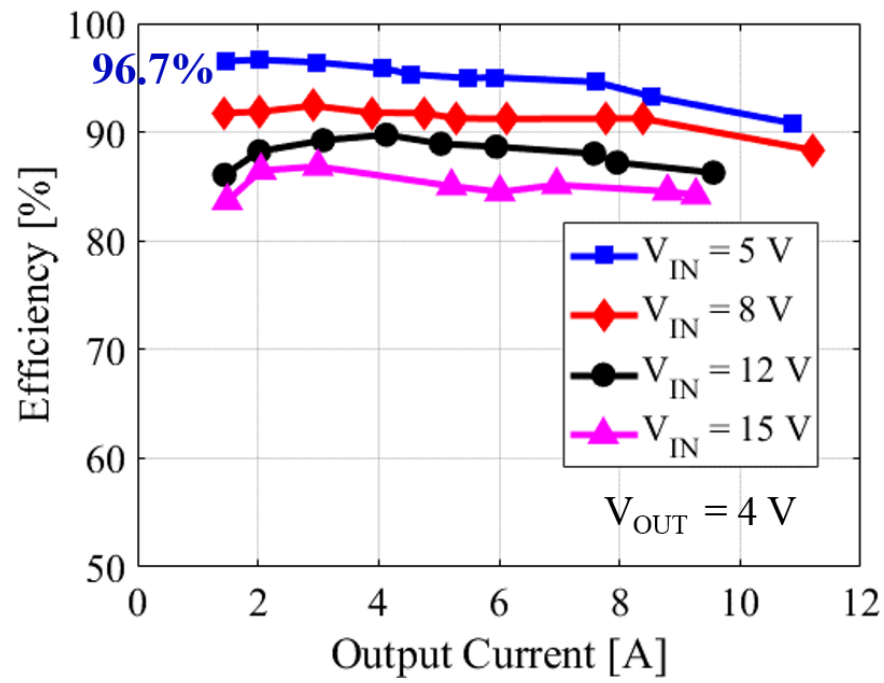
Figure 6.9: Measured efficiency of the prototype ZVS-QSW buck converter at different input voltage with output voltage $V_{\mathrm{OUT}} = 4$ V across full load conditions.

Chapter 7

Conclusions and Future Work

7.1   Summary

This thesis has investigated five topologies, including zero-voltage-switching quasi-square-wave (ZVS-QSW) buck converter, three-level buck converter, four-level buck converter, a resonant switched capacitor converter, and a new reconfigurable hybrid switched capacitor converter for low-profile, high-power-density, and high-efficiency dc-dc converters for battery charging applications. This thesis has also designed, built and tested prototypes of three of these topologies: QSW-ZVS (2-level) buck converter, 3-level buck converter and 4-level buck converter. These prototypes utilize GaN transistors (EPC2023) and their measured efficiency at different operating conditions are evaluated and compared, as shown in Fig. 7.1. It can be seen from Fig. 7.1(a) that at 2:1 step-down conversion ratio the 3-level buck converter is the most efficient of the three converters across the full output current due to its minimum inductor current ripple. At 3:1 step-down conversion ratio (Fig. 7.1(b)), the 4-level buck converter is the most efficient at light loads and but its efficiency drops below that of the 3-level buck converter at heavy loads due to larger conduction losses in its three series switches. Even at 3.75:1 step-down conversion ratio (Fig. 7.1(c)), the 3-level buck converter is the most efficient of the three topologies under heavy load conditions, with the four-level buck converter more efficient below 40% load. The 2-level buck is the least efficient of the three under all the operating conditions considered.

A comparison of commercial products with the prototypes proposed in this thesis is

shown in Fig. 7.2. It can bee seen that the ZVS-QSW buck converter achieves the highest power density; however, at large conversion ratio(input voltage 12 V, output voltage 4 V, output current 10 A), its efficiency is poor due to the large inductor ripple. The 3-level buck converter using GaN transistors (EPC2023) achieves relatively high power density, while maintaining highest efficiency among the state-of-the-art commercial products. The 3-level buck converter using Silicon MOSFET (CPF03433) achieves reasonably high power density compared with commercial products; however, its efficiency is low due to the significant conduction loss caused by large inductor current ripple to achieve ZVS. The 4-level buck converter using GaN transistors (EPC2023) achieves similar power density and efficiency compared with commercial products.

Therefore, the 3-level buck converter is the most suitable topology for this low-profile, high-power-density and high efficiency battery charger application. Texas Instruments has also recently proposed a 3-level buck converter (bq25910) for fast battery charging [45]. The comparison in terms of area, efficiency and specifications of our GaN based 3-level buck converter prototype with TI's bq25910 is shown in Table 7.1. The efficiency comparison for two operating conditions is shown in Fig. 7.3. The TI's bq25910 occupies one third of area compared with our 3-level buck converter prototype. Our prototype using GaN transistors and a customized inductor can handle load current up to 10 A and achieve much higher efficiency at heavy load.

Table 7.1: Comparison of TI's bq25910 and EPC2023 based prototype

|	TI's bq25910	GaN Prototype
Power Stage Area	120 mm^2, 5.9 mm^2(chip)	358 mm^2
Component height	1 mm(L_r), 0.62 mm(chip)	1 mm
Maximum Output Current	6 A	10 A
Input Voltage Range	4 V to 14 V	5 V to 20 V
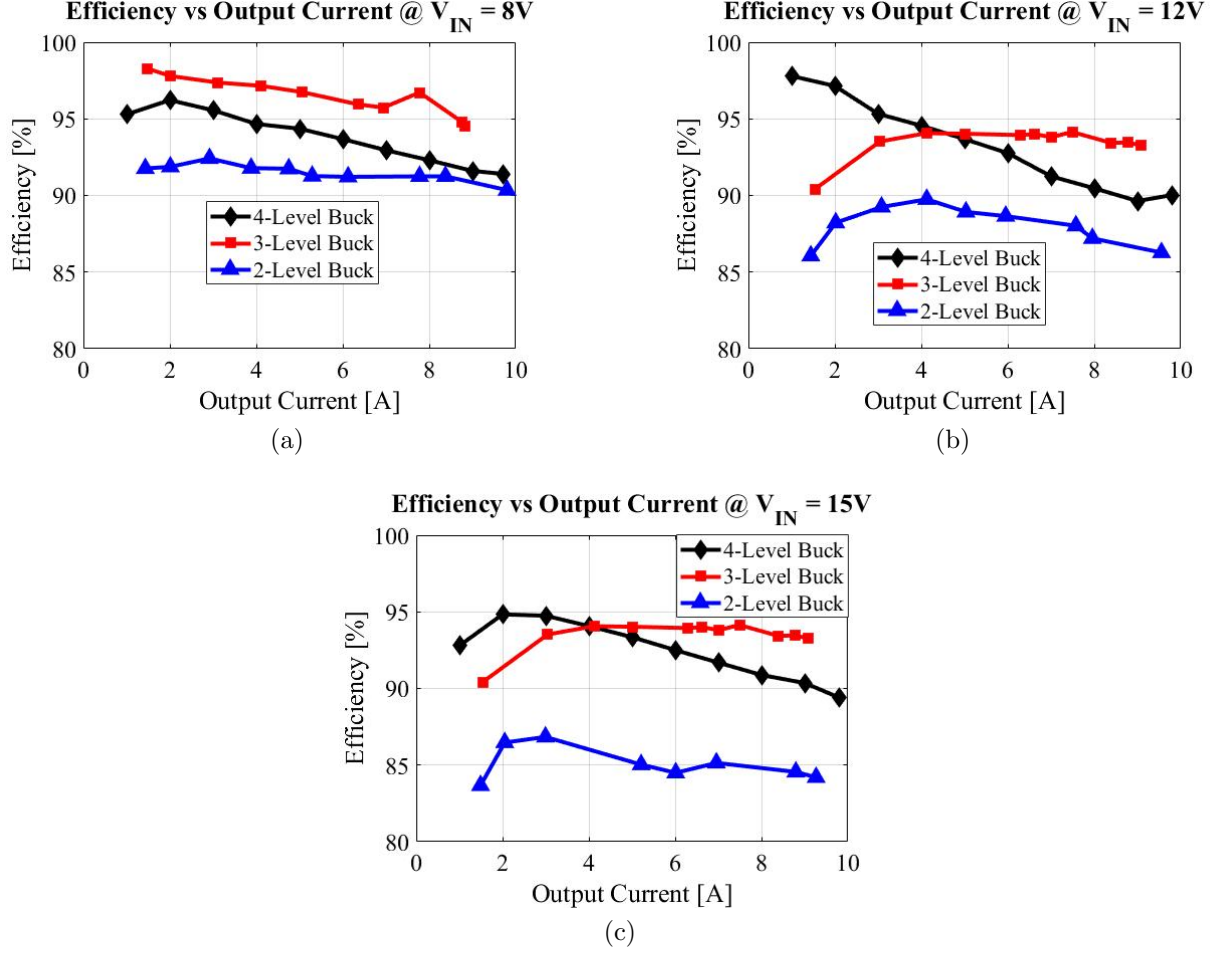
Figure 7.1: The measured efficiency of GaN-based 2-level (ZVS-QSW) buck, 3-level buck and 4-level buck converters at different operating conditions over full load range: (a) input voltage $V_{\mathrm{IN}} = 8$ V, output voltage $V_{\mathrm{OUT}} = 4$ V; (b) input voltage $V_{\mathrm{IN}} = 12$ V, output voltage $V_{\mathrm{OUT}} = 4$ V; (c) input voltage $V_{\mathrm{IN}} = 15$ V, output voltage $V_{\mathrm{OUT}} = 4$ V.

7.2   Conclusions

This thesis is focused on high-power-density, low-profile and high-efficiency DC-DC converters for battery chargers inside the cellphone. Nowadays, there is demanding need of thinner thickness and large battery capability for the cellphone from the customers. Also, enabled by the latest USB standard, the input voltage of the cellphone battery charger extends to 20 V, allowing fast battery charging capability. Therefore, there is need to design a high-power-density battery charger with input voltage range of 5 V to 20 V, output voltage
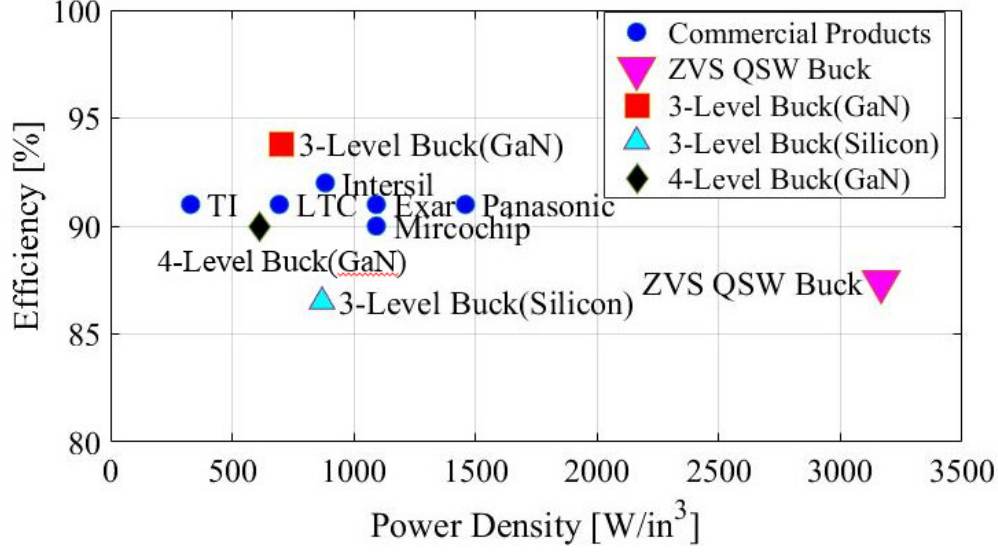
Figure 7.2: Comparison of state-of-the-art commercial DC-DC converter with the prototypes proposed in this thesis: ZVS-QSW buck, 3-level buck using GaN transistor, 3-level buck using Silicon MOSFET, 4-level buck using GaN transistor. Indicated efficiency is with input voltage of 12 V, output voltage of 4 V and output current of 10 A.
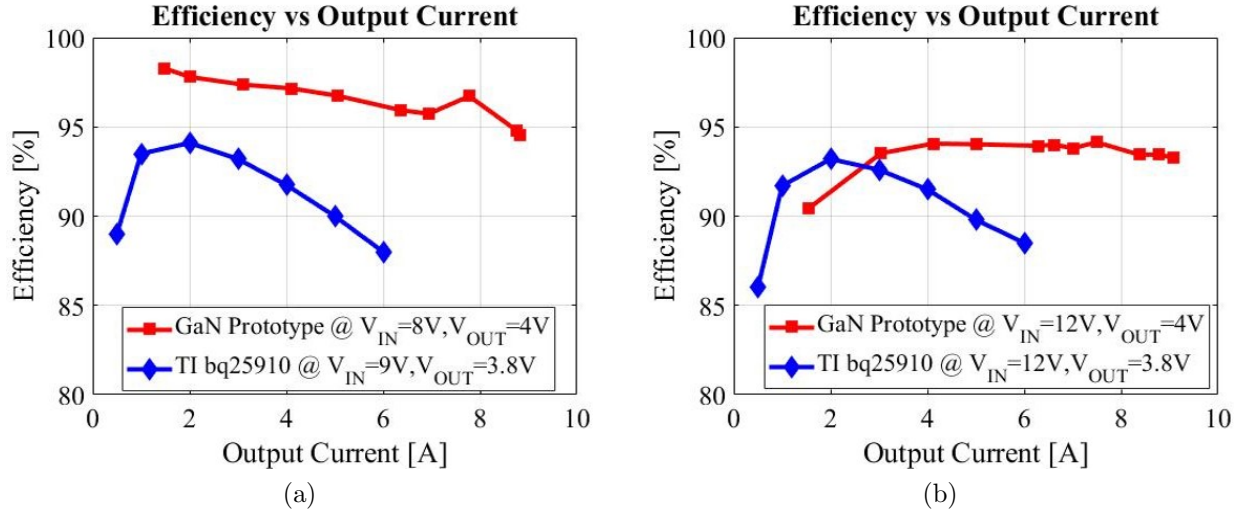
Figure 7.3: The efficiency comparison of TI's bq25910 and GaN transistor (EPC2023) based prototype for two operating conditions across different load current at (a) input voltage $V_{IN} = 8\,V$, output voltage $V_{OUT} = 4\,V$; (b) input voltage $V_{IN} = 12\,V$, output voltage $V_{OUT} = 4\,V$.

range of 3 V to 4.2 V (Lithium-ion battery operating voltage), and maximum output current of 10 A. The thickness of the component is limited to 1 mm. Conventional state-of-the-

art solutions based on buck converter topology with commercial inductors do not meet the height requirement.

To push the limit of power density and efficiency of the conventional battery charger solutions, this thesis investigates five topologies, including zero-voltage switching quasi-square-wave (ZVS-QSW) buck converter, three-level buck converter, resonant switched capacitor converter, reconfigurable hybrid switched capacitor converter and four-level buck converter, as described in Chapter 2. The operation principle, advantage and disadvantage of each topology is stated, analyzed and compared in terms of efficiency and power density in this application.

To get accurate waveforms of each converter topology, the augmented state-space modeling is introduced in Chapter 3. Without state matrix inversion and waiting for star-up transition, this method can efficiently calculate the steady-state waveforms of the converter numerically. Its results match well with LTspice simulation results, while only takes 1/60 of the computation time. This enables comprehensive search and optimization for the design parameters of the converter, such switching frequency, transistor size, inductor geometry and airgap. Chapter 3 also introduces the loss model of DC-DC converter, including transistor loss, inductor loss and capacitor loss. To make the loss model more accurate, the dynamic on-resistance of GaN transistor at high switching frequency and core loss of inductor has been studied. Both experimentally measured waveforms and thermal measurement results have been used to calibrate the dynamic on-resistance of GaN transistor at MHz, and the steinmetz parameters of 3F46 ferrite material operated at large flux density($B_{max} > 500$ mT) scenario.

Chapter 4 introduces the design of a high-power-density and low-profile three-level buck converter optimized for 2:1 conversion ratio application scenario (now published in [46]). This three-level buck converter can also regulate its output voltage/current using pulse-width modulated (PWM) control. The design methodology utilizes the augmented state-space modeling to accurately predict the converter waveforms and performance. To achieve high

power density, a custom-shaped planar PCB-integrated inductor is designed, whose geometry is optimized using 3D finite-element analysis (FEA) to minimize losses. Two prototypes using GaN transistors (EPC2023) and low-voltage Silicon MOSFET (CPF03433) are designed, build and tested for an input voltage range of 5 V to 20 V, an output voltage range of 3 V to 4.2 V, and a maximum output current of 10 A. The zero-voltage switching (ZVS) operation over wide range of output current is verified by experiments. The prototype with GaN transistors (EPC2023) occupies a PCB area of 358 mm^2 with component height of 1 mm. To maximize efficiency, the converter is designed to achieve ZVS at light-to-medium loads, while sacrificing ZVS to reduce transistor conduction and inductor losses. This prototype converter achieves a peak efficiency of 98.5% at 2:1 conversion ratio and high efficiency at other operating conditions with a power density of 704 W/in^3. The prototype using low-voltage Silicon MOSFET (CPF03433) with a PCB area of 310 mm^2 is also built and tested. Due to the low breakdown voltage (13 V) of Silicon MOSFET, ZVS is achieved across various load condition to reduce the voltage stress on the device. Also, The on-resistance and output capacitance of the Silicon MOSFET (CPF03433) have been calibrated, and the comparison of GaN transistor(EPC2023) GaN and silicon MOSFET (CPF03433) has been done.

Chapter 5 of the thesis focus on the design of high-power-density and low-profile converter for 3:1 conversion ratio application scenario. Two topologies suitable for large conversion ratio, including the four-level buck converter and reconfigurable hybrid switched capacitor converter, has been analyzed. The augmented state-space modeling method is utilized to accurately predict the two converters' waveforms and calculate each one loss. Also, a custom-shaped planar PCB-integrated inductor is designed to achieve high power density and high efficiency. The four-level buck converter's efficiency is overall above the reconfigurable hybrid switched capacitor converter's across wide input voltage range, especially at 3:1 conversation ratio when its inductor current ripple is minimized. Based on the analysis, a prototype of four-level buck converter using GaN transistor (EPC2023) with a PCB area of 410 mm^2 and component height of 1 mm has been built and tested.

Finally, the chapter 8 of this thesis introduces the design for extreme-power-density battery charger (now published in [47]). Specifically, the converter is required to deliver a maximum output power of 40 W across a 4:1 input voltage range, with its PCB footprint limited to $80\,\mathrm{mm}^2$ and its component height limited to 1 mm. Due to the stringent area ($80\mathrm{mm}^2$) requirement, three alternative topologies a zero-voltage-switching quasi-square-wave (ZVS-QSW) buck converter, a three-level buck converter, and a resonant switched capacitor converter are analyzed, designed and compared in terms of efficiency and power density in this application. The augmented state-space modeling has been used to predict the converter waveforms efficiently and accurately. With the refined loss model mentioned on Chapter 2, the geometry and airgap of the inductor in the three converter topologies are optimized. The ZVS-QSW buck converter is predicted to achieve the highest efficiency under the specified area and height constraints. A prototype 40-W 1-MHz buck converter with a PCB area of 79.6 mm^2 and component height of 1 mm is built and tested. The prototype converter achieves a peak efficiency of 96.7% and a power density of 3230 $\mathrm{W/in}^3$.

7.3   Future Work

This thesis is focused on the low-profile, high-power-density and high-efficiency battery charger. The design methodology based on augmented state-space modeling method is utilized to optimize the inductor design and converter operation that enables high power density, low profile and high efficiency. A number of directions can be pursued from the basis of this thesis.

Other hybrid switched capacitor topology.

This thesis investigates five topologies, including zero-voltage switching quasi-square-wave (ZVS-QSW) buck converter, three-level buck converter, resonant switched capacitor converter, reconfigurable hybrid switched capacitor converter and four-level buck converter. There are many other DC-DC converter topologies fit the battery charger application with wide input voltage range. Hybrid switched capacitor converter topologies need small inductor

for voltage regulation [48, 49], which is suitable for this high-power-density and low-profile application requirement. Chapter 2 and Chapter 7 discusses the design and operation of one example of hybrid switched capacitor topology (2:1 ladder resonant switched capacitor converter). It needs less inductance compared with other PWM converter topologies, such as QSW-ZVS buck and three-level buck converter; but it is efficient at certain operating conditions. Other hybrid switched capacitor topology with voltage regulation capability might utilize more components, such as transistors and capacitors, which occupy more area. Also, the augmented state-space modeling can be used in hybrid switched capacitor topology to predict the converter waveforms and calculate the loss.

Closed loop control of three-level and four-level buck converter.

The experimental results shown in Chapter 4 are done with the converter operating in open loop. A closed-loop control scheme for three-level buck converter needs to be developed to precisely control the output voltage and current in the presence of input and output voltage variations, as shown in [50]. Also, to achieve ZVS, variable-frequency control techniques are promising. For four-level buck converter, there is also need for a closed-loop control scheme and duty-ratio control technique looks promising.

Other customized planar inductor shape.

This thesis considers four customized planar inductor shapes candidates EI, E, UI and U. The inductance and ac on-resistance of the planar inductor is obtained from Ansys Maxwell finite-element analysis (FEA) simulation tool, as shown in Chapter 4 and Chapter 6. There are many other planar core shapes, such as ER, EC, UR, and they are also worth investigating. Their inductance and ac on-resistance can also be got from Ansys Maxwell.

Integration of the transistors and gate driver.

All the design and prototypes in this thesis are built with discrete components. The switches and gate driver can be integrated in monolithic chip, which greatly increases the power density. Also it decreases the parasitic inductance and resistance in the gate driver loop, improving its performance. The prototypes built with discrete components are for

validation of the topology and magnetic design. Integrated Circuit will be the final product.

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Appendix A

Matlab Script for Augmented State Space Modeling for Each Topology

A.1   Matlab Script for QSW-ZVS Buck Converter

This section includes example Matlab code implementing augmented state space modeling for QSW-ZVS buck converter.

```matlab
A1 = [−RL/L  −1/L;  1/C  −1/(R∗C) ];
B1 = [ Vin/L;   0 ];
A2 = [−RL/L  −1/L;  1/C  −1/(R∗C) ];
B2 = [ 0 ;   0 ];
phi1 = expm(D∗Ts∗A1) ;
phi2 = expm((1−D)∗Ts∗A2) ;
phiTot = phi2∗phi1 ;
dummyRow = zeros (1 ,3) ;
A1aug = [A1 B1;  dummyRow ];
A2aug = [A2 B2;  dummyRow ];
phi1Aug = expm(A1aug∗D∗Ts) ;
phi2Aug = expm(A2aug∗(1−D)∗Ts) ;
phiTotAug = phi2Aug∗phi1Aug ;
gamma1 = phi1Aug (1:2 ,3) ;
gamma2 = phi2Aug (1:2 ,3) ;
gammaTot = phi2∗gamma1 + gamma2 ;
```

```matlab
17  mInv = eye(2)−phiTot;
18  xper0 = mInv \ gammaTot;
19  xper0Aug = [xper0; 1];
20  xper1Aug = phi1Aug * xper0Aug;
21  xper2Aug = phi2Aug * xper1Aug;
22
23  tres = Ts/1000;
24  t1 = 0:tres:D*Ts;
25  t2 = (t1(end)+tres):tres:Ts;
26  t = [t1 t2];
27  xper_t1Aug = zeros(3,numel(t1));
28  xper_t2Aug = zeros(3,numel(t2));
29  for i=1:1:numel(t1)
30  xper_t1Aug(:,i) = expm(A1aug.*t1(i))*xper0Aug;
31  end
32  for i=1:1:numel(t2)
33  xper_t2Aug(:,i) = expm(A2aug.*(t2(i)−t2(1)))*xper1Aug;
34  end
35  xper_Aug = [xper_t1Aug xper_t2Aug];
36  xper = xper_Aug(1:2,:);
37  iL = xper(1,:);
38  vCo = xper(2,:);
39
40  tdend = find(t>=D*Ts,1);
41  td2end = length(t);
42
43  iQ1 = iL;
```

```
44  iQ2 = iL;

45  iQ1(tdend:end) = 0;

46  iQ2(1:tdend) = 0;
```

A.2   Matlab Script for Three-level Buck Converter

This section includes example Matlab code implementing augmented state space modeling for three-level buck converter.

```
1   %% System Matrices

2   A12 = [0 0 0; 0 −1/(R*Co) 1/Co; 0 −1/L −RL/L];

3   A13 = [0 0 1/Cf; 0 −1/(R*Co) 1/Co; −1/L −1/L −RL/L];

4   A24 = [0 0 −1/Cf; 0 −1/(R*Co) 1/Co; 1/L −1/L −RL/L];

5   A34 = [0 0 0; 0 −1/(R*Co) 1/Co; 0 −1/L −RL/L];

6

7   %% Input Matrices

8   b12 = [0 0 Vin/L]';

9   b13 =  [0 0 Vin/L]';

10  b24 = [0 0 0]';

11  b34 = [0 0 0]';

12

13  %% Duty Ratio

14  d = 0.494;

15

16  %% Mode Sequence

17  if d <= 0.5

18  A1 = A13;

19  b1 = b13;
```

```matlab
20  A2 = A34;
21  b2 = b34;
22  A3 = A24;
23  b3 = b24;
24  A4 = A34;
25  b4 = b34;
26  d1 = d;
27  d2 = 0.5 - d;
28  d3 = d;
29  d4 = 0.5 - d;
30  elseif d > 0.5
31  A1 = A12;
32  b1 = b12;
33  A2 = A13;
34  b2 = b13;
35  A3 = A12;
36  b3 = b12;
37  A4 = A24;
38  b4 = b24;
39  d1 = d - 0.5;
40  d2 = 1 - d;
41  d3 = d - 0.5;
42  d4 = 1 - d;
43  end
44
45  %% State Transition Matrices
46  phi1 = expm(d1*Ts*A1);
```

```matlab
47  phi2 = expm(d2*Ts*A2);

48  phi3 = expm(d3*Ts*A3);

49  phi4 = expm(d4*Ts*A4);

50  phiTot = phi4*phi3*phi2*phi1;

51

52  dummyRow = zeros(1,4);

53  A1aug = [A1 b1; dummyRow];

54  A2aug = [A2 b2; dummyRow];

55  A3aug = [A3 b3; dummyRow];

56  A4aug = [A4 b4; dummyRow];

57

58  phi1Aug = expm(d1*Ts*A1aug);

59  phi2Aug = expm(d2*Ts*A2aug);

60  phi3Aug = expm(d3*Ts*A3aug);

61  phi4Aug = expm(d4*Ts*A4aug);

62  phiTotAug = phi4Aug*phi3Aug*phi2Aug*phi1Aug;

63

64  gamma1 = phi1Aug(1:3,4);

65  gamma2 = phi2Aug(1:3,4);

66  gamma3 = phi3Aug(1:3,4);

67  gamma4 = phi4Aug(1:3,4);

68  gammaTot = phi4*phi3*phi2*gamma1 + phi4*phi3*gamma2 + phi4
        *gamma3 + gamma4;

69

70  mInv = eye(3)-phiTot;

71  xper0 = mInv \ gammaTot;

72  xper0Aug = [xper0; 1];
```

```matlab
xper1Aug = phi1Aug*xper0Aug;

xper1 = xper1Aug(1:3);

xper2Aug = phi2Aug*xper1Aug;

xper2 = xper2Aug(1:3);

xper3Aug = phi3Aug*xper2Aug;

xper3 = xper3Aug(1:3);

xper4Aug = phi4Aug*xper3Aug;

xper4 = xper4Aug(1:3);


tres = 0.5e-9;

t1 = 0:tres:d1*Ts;

t2 = t1(end):tres:(d1+d2)*Ts;

t3 = t2(end):tres:(d1+d2+d3)*Ts;

t4 = t3(end):tres:(d1+d2+d3+d4)*Ts;

t = [t1 t2 t3 t4];


xper_t1Aug = zeros(4,numel(t1));

xper_t2Aug = zeros(4,numel(t2));

xper_t3Aug = zeros(4,numel(t3));

xper_t4Aug = zeros(4,numel(t4));


for i=1:1:numel(t1)

xper_t1Aug(:,i) = expm(A1aug*t1(i))*xper0Aug;

end

for i=1:1:numel(t2)

xper_t2Aug(:,i) = expm(A2aug*(t2(i)-t2(1)))*xper1Aug;

end
```

```matlab
100  for i=1:1:numel(t3)
101  xper_t3Aug(:,i) = expm(A3aug*(t3(i)-t3(1)))*xper2Aug;
102  end
103  for i=1:1:numel(t4)
104  xper_t4Aug(:,i) = expm(A4aug*(t4(i)-t4(1)))*xper3Aug;
105  end
106
107  xper_Aug = [xper_t1Aug xper_t2Aug xper_t3Aug xper_t4Aug];
108  xper = xper_Aug(1:3,:);
109
110  vCf = xper(1,:);
111  vCo = xper(2,:);
112  iL = xper(3,:);
113
114  td1end = find(t>=d1*Ts,1);
115  td2end = find(t>=(d1+d2)*Ts,1);
116  td3end = find(t>=(d1+d2+d3)*Ts,1);
117
118  iQ1 = iL;
119  iQ2 = iL;
120  iQ3 = iL;
121  iQ4 = iL;
122
123  if d <= 0.5
124  iQ1(td1end:end) = 0;
125  iQ2(1:td2end) = 0;
126  iQ2(td3end:end) = 0;
```

```
127  iQ3(td2end:td3end) = 0;
128  iQ4(1:td1end) = 0;
129  elseif d > 0.5
130  iQ1(td3end:end) = 0;
131  iQ2(td1end:td2end) = 0;
132  iQ3(1:td1end) = 0;
133  iQ3(td2end:end) = 0;
134  iQ4(1:td3end) = 0;
135  end
```

A.3   Matlab Script for Four-Level Buck Converter

This section includes example Matlab code implementing augmented state space modeling for four-level buck converter.

```
1   %% System Matrices For Four level buck converter
2   A145 = [0 0 0 1/C1;...
3   0 0 0  0;...
4   0 0 -1/(R*Co) 1/Co;...
5   -1/L 0 -1/L -Ron/L];
6   A456 = [0 0 0 0;  ...
7   0 0 0 0;  ...
8   0 0 -1/(R*Co) 1/Co;  ...
9   0 0 -1/L -Ron/L];
10  A246 = [0 0 0 -1/C1;...
11  0 0 0 1/C2;...
12  0 0 -1/(R*Co) 1/Co;...
13  1/L -1/L -1/L -Ron/L];
```

```
14  A356 = [0 0 0 0; ...
15  0 0 0 -1/C2; ...
16  0 0 -1/(R*Co) 1/Co; ...
17  0 1/L -1/L -Ron/L];
18  A135 = [0 0 0 1/C1; ...
19  0 0 0 -1/C2; ...
20  0 0 -1/(R*Co) 1/Co; ...
21  -1/L 1/L -1/L -Ron/L];
22  A124 = [0 0 0 0; ...
23  0 0 0 1/C2; ...
24  0 0 -1/(R*Co) 1/Co; ...
25  0 -1/L -1/L -Ron/L];
26  A236 = [0 0 0 -1/C1; ...
27  0 0 0 0; ...
28  0 0 -1/(R*Co) 1/Co; ...
29  1/L 0 -1/L -Ron/L];
30  A123 = [0 0 0 0; ...
31  0 0 0 0; ...
32  0 0 -1/(R*Co) 1/Co; ...
33  0 0 -1/L -Ron/L];
34
35  %% Input Matrices
36  b145 = [0 0 0 Vin/L]';
37  b456 = [0 0 0 0]';
38  b246 = [0 0 0 0]';
39  b356 = [0 0 0 0]';
40  b135 = [0 0 0 Vin/L]';
```

```matlab
41  b124 = [0  0  0  Vin/L]';
42  b236 = [0  0  0  0]';
43  b123 = [0  0  0  Vin/L]';
44
45
46  %% Mode Sequence
47  if d < 1/3
48  A1 = A145;
49  b1 = b145;
50  A2 = A456;
51  b2 = b456;
52  A3 = A246;
53  b3 = b246;
54  A4 = A456;
55  b4 = b456;
56  A5 = A356;
57  b5 = b356;
58  A6 = A456;
59  b6 = b456;
60  d1 = d;
61  d2 = 1/3 - d;
62  d3 = d1;
63  d4 = d2;
64  d5 = d1;
65  d6 = d2;
66  elseif (d > 1/3)&&(d < 2/3)
67  A1 = A135;
```

```
68  b1 = b135;
69  A2 = A145;
70  b2 = b145;
71  A3 = A124;
72  b3 = b124;
73  A4 = A246;
74  b4 = b246;
75  A5 = A236;
76  b5 = b236;
77  A6 = A356;
78  b6 = b356;
79  d1 = d - 1/3;
80  d2 = 2/3 - d;
81  d3 = d - 1/3;
82  d4 = 2/3 - d;
83  d5 = d - 1/3;
84  d6 = 2/3 - d;
85  elseif d > 2/3
86  A1 = A123;
87  b1 = b123;
88  A2 = A135;
89  b2 = b135;
90  A3 = A123;
91  b3 = b123;
92  A4 = A124;
93  b4 = b124;
94  A5 = A123;
```

```
95   b5 = b123;
96   A6 = A236;
97   b6 = b236;
98   d1 = d − 2/3;
99   d2 = 1 − d;
100  d3 = d − 2/3;
101  d4 = 1 − d;
102  d5 = d − 2/3;
103  d6 = 1 − d;
104  elseif d == 1/3
105  A1 = A145;
106  b1 = b145;
107  A2 = A145;
108  b2 = b145;
109  A3 = A246;
110  b3 = b246;
111  A4 = A246;
112  b4 = b246;
113  A5 = A356;
114  b5 = b356;
115  A6 = A356;
116  b6 = b356;
117  d1 = d/2;
118  d2 = d/2;
119  d3 = d/2;
120  d4 = d/2;
121  d5 = d/2;
```

```matlab
122 | d6 = d/2;
123 | elseif d == 2/3
124 | A1 = A135;
125 | b1 = b135;
126 | A2 = A135;
127 | b2 = b135;
128 | A3 = A124;
129 | b3 = b124;
130 | A4 = A124;
131 | b4 = b124;
132 | A5 = A236;
133 | b5 = b236;
134 | A6 = A236;
135 | b6 = b236;
136 | d1 = 1/6;
137 | d2 = 1/6;
138 | d3 = 1/6;
139 | d4 = 1/6;
140 | d5 = 1/6;
141 | d6 = 1/6;
142 | end
143 |
144 | %% State Transition Matrices
145 | phi1 = expm(d1*Ts*A1);
146 | phi2 = expm(d2*Ts*A2);
147 | phi3 = expm(d3*Ts*A3);
148 | phi4 = expm(d4*Ts*A4);
```

```matlab
149  phi5 = expm(d5*Ts*A5);

150  phi6 = expm(d6*Ts*A6);

151  phiTot = phi6*phi5*phi4*phi3*phi2*phi1;

152

153  dummyRow = zeros(1,5);

154  A1aug = [A1 b1; dummyRow];

155  A2aug = [A2 b2; dummyRow];

156  A3aug = [A3 b3; dummyRow];

157  A4aug = [A4 b4; dummyRow];

158  A5aug = [A5 b5; dummyRow];

159  A6aug = [A6 b6; dummyRow];

160

161  phi1Aug = expm(d1*Ts*A1aug);

162  phi2Aug = expm(d2*Ts*A2aug);

163  phi3Aug = expm(d3*Ts*A3aug);

164  phi4Aug = expm(d4*Ts*A4aug);

165  phi5Aug = expm(d5*Ts*A5aug);

166  phi6Aug = expm(d6*Ts*A6aug);

167  phiTotAug = phi6Aug*phi5Aug*phi4Aug*phi3Aug*phi2Aug*
         phi1Aug;

168

169  gamma1 = phi1Aug(1:4,5);

170  gamma2 = phi2Aug(1:4,5);

171  gamma3 = phi3Aug(1:4,5);

172  gamma4 = phi4Aug(1:4,5);

173  gamma5 = phi5Aug(1:4,5);

174  gamma6 = phi6Aug(1:4,5);
```

```
175  gammaTot = phi6*phi5*phi4*phi3*phi2*gamma1 + phi6*phi5*
          phi4*phi3*gamma2 +...
176  phi6*phi5*phi4*gamma3 + phi6*phi5*gamma4 + phi6*gamma5 +
          gamma6;
177
178  mInv = eye(4)-phiTot;
179  xper0 = mInv \ gammaTot;
180  xper0Aug = [xper0; 1];
181  xper1Aug = phi1Aug*xper0Aug;
182
183  xper1 = xper1Aug(1:4);
184  xper2Aug = phi2Aug*xper1Aug;
185
186  xper2 = xper2Aug(1:4);
187  xper3Aug = phi3Aug*xper2Aug;
188
189  xper3 = xper3Aug(1:4);
190  xper4Aug = phi4Aug*xper3Aug;
191
192  xper4 = xper4Aug(1:4);
193  xper5Aug = phi5Aug*xper4Aug;
194
195  xper5 = xper5Aug(1:4);
196  xper6Aug = phi6Aug*xper5Aug;
197
198  xper6 = xper6Aug(1:4);
199
```

```matlab
200   tres = Ts/1000;
201   t1 = 0:tres:d1*Ts;
202   t2 = (t1(end)+tres):tres:(d1+d2)*Ts;
203   t3 = (t2(end)+tres):tres:(d1+d2+d3)*Ts;
204   t4 = (t3(end)+tres):tres:(d1+d2+d3+d4)*Ts;
205   t5 = (t4(end)+tres):tres:(d1+d2+d3+d4+d5)*Ts;
206   t6 = (t5(end)+tres):tres:(d1+d2+d3+d4+d5+d6)*Ts;
207   t = [t1 t2 t3 t4 t5 t6];
208
209   xper_t1Aug = zeros(5,numel(t1));
210   xper_t2Aug = zeros(5,numel(t2));
211   xper_t3Aug = zeros(5,numel(t3));
212   xper_t4Aug = zeros(5,numel(t4));
213   xper_t5Aug = zeros(5,numel(t5));
214   xper_t6Aug = zeros(5,numel(t6));
215
216   for i=1:1:numel(t1)
217   xper_t1Aug(:,i) = expm(A1aug*t1(i))*xper0Aug;
218   end
219   for i=1:1:numel(t2)
220   xper_t2Aug(:,i) = expm(A2aug*(t2(i)-t2(1)))*xper1Aug;
221   end
222   for i=1:1:numel(t3)
223   xper_t3Aug(:,i) = expm(A3aug*(t3(i)-t3(1)))*xper2Aug;
224   end
225   for i=1:1:numel(t4)
226   xper_t4Aug(:,i) = expm(A4aug*(t4(i)-t4(1)))*xper3Aug;
```

```matlab
227  end
228  for  i=1:1:numel(t5)
229  xper_t5Aug(:,i) = expm(A5aug*(t5(i)-t5(1)))*xper4Aug;
230  end
231  for  i=1:1:numel(t6)
232  xper_t6Aug(:,i) = expm(A6aug*(t6(i)-t6(1)))*xper5Aug;
233  end
234
235  xper_Aug = [xper_t1Aug xper_t2Aug xper_t3Aug xper_t4Aug
          xper_t5Aug xper_t6Aug];
236  xper = xper_Aug(1:4,:);
237
238  vC1 = xper(1,:);
239  vC2 = xper(2,:);
240  vCo = xper(3,:);
241  iL = xper(4,:);
242  ic1 = gradient(vC1,t)*C1;
243  ic2 = gradient(vC2,t)*C2;
244
245  td1end = find(t>=d1*Ts,1);
246  td2end = find(t>=(d1+d2)*Ts,1);
247  td3end = find(t>=(d1+d2+d3)*Ts,1);
248  td4end = find(t>=(d1+d2+d3+d4)*Ts,1);
249  td5end = find(t>=(d1+d2+d3+d4+d5)*Ts,1);
250  td6end = length(t);
251
252  iQ1 = iL;
```

```matlab
253  iQ2 = iL;
254  iQ3 = iL;
255  iQ4 = -iL;
256  iQ5 = -iL;
257  iQ6 = -iL;
258
259  if d < 1/3
260  iQ1(td1end:end) = 0;
261  iQ2(1:td2end) = 0;
262  iQ2(td3end:end) = 0;
263  iQ3(1:td4end) = 0;
264  iQ3(td5end:end) = 0;
265  iQ4(td4end:td5end) = 0;
266  iQ5(td2end:td3end) = 0;
267  iQ6(1:td1end) = 0;
268  elseif (d > 1/3)&&(d < 2/3)
269  iQ1(td3end:end) = 0;
270  iQ2(1:td2end) = 0;
271  iQ2(td5end:end) = 0;
272  iQ3(td1end:td4end) = 0;
273  iQ4(1:td1end) = 0;
274  iQ4(td4end:end) = 0;
275  iQ5(td2end:td5end) = 0;
276  iQ6(1:td3end) = 0;
277  elseif (d > 2/3)
278  iQ1(td5end:end) = 0;
279  iQ2(td1end:td2end) = 0;
```

```matlab
280  iQ3( td3end : td4end ) = 0;
281  iQ4( 1 : td3end ) = 0;
282  iQ4( td4end : end ) = 0;
283  iQ5( 1 : td1end ) = 0;
284  iQ5( td2end : end ) = 0;
285  iQ6( 1 : td5end ) = 0;
286  elseif (d == 1/3)
287  iQ1( td2end : end ) = 0;
288  iQ2( 1 : td2end ) = 0;
289  iQ2( td4end : end ) = 0;
290  iQ3( 1 : td4end ) = 0;
291  iQ4( td4end : end ) = 0;
292  iQ5( td2end : td4end ) = 0;
293  iQ6( 1 : td2end ) = 0;
294  elseif (d == 2/3)
295  iQ1( td4end : end ) = 0;
296  iQ2( 1 : td2end ) = 0;
297  iQ3( td2end : td4end ) = 0;
298  iQ4( 1 : td2end ) = 0;
299  iQ4( td4end : end ) = 0;
300  iQ5( td2end : end ) = 0;
301  iQ6( 1 : td4end ) = 0;
302  end
```

A.4   Matlab Script for Reconfigurable Hybrid Switched Capacitor Converter

This section includes example Matlab code implementing augmented state space modeling for reconfigurable hybrid switched capacitor converter.

```matlab
%% System Matrices
A1 = [ -1/(3*C*Ron),                    0,   1/(3*C*Ron),
                0,                  1/(3*C)                  0;...
0,  -1/(3*C*Ron),                0,   1/(3*C*Ron),
                        0,                      0;...
2/(3*C*Ron),    1/(3*C*Ron),   -2/(3*C*Ron),   -1/(3*C*Ron),
                1/(3*C),                    0;...
1/(3*C*Ron),    2/(3*C*Ron),   -1/(3*C*Ron),   -2/(3*C*Ron),
                2/(3*C),                    0;...
-2/(3*L),       -1/(3*L),       -1/(3*L),       -2/(3*L),  -(3*
    RLr + Ron)/(3*L),                  -1/L;...
0,              0,              0,              0,
                1/Cout,  -1/(Cout*Rout)];
A2 = [ -1/(3*C*Ron),                    0,  -1/(3*C*Ron),  -1/(3*C*
    Ron),                  1/(3*C)                  0;...
0,  -1/(3*C*Ron),    1/(3*C*Ron),                  0,
                        0,                      0;...
-1/(3*C*Ron),    1/(3*C*Ron),   -2/(3*C*Ron),   -1/(3*C*Ron),
                1/(3*C),                    0;...
-2/(3*C*Ron),   -1/(3*C*Ron),   -1/(3*C*Ron),   -2/(3*C*Ron),
                2/(3*C),                    0;...
-2/(3*L),       -1/(3*L),       -1/(3*L),       -2/(3*L),  -(3*
    RLr + Ron)/(3*L),                  -1/L;...
```

```matlab
13  0,                    0,                    0,                    0, ...
                         1/Cout,  -1/(Cout*Rout)];

14

15  %% Input Matrices
16  b1 =          [0; ...
17  0; ...
18  0; ...
19  0; ...
20  Vin/L; ...
21  0];
22  b2 =          [Vin/(3*C*Ron); ...
23  0; ...
24  Vin/(3*C*Ron); ...
25  (2*Vin)/(3*C*Ron); ...
26  (2*Vin)/(3*L); ...
27  0];

28

29  %% Mode Sequence
30  d1 = d;
31  d2 = 1-d;
32  %% State Transition Matrices
33  phi1 = expm(d1*Ts*A1);
34  phi2 = expm(d2*Ts*A2);
35  phiTot = phi2*phi1;
36  dummyRow = zeros(1,7);
37  A1aug = [A1 b1; dummyRow];
38  A2aug = [A2 b2; dummyRow];
```

```matlab
phi1Aug = expm(d1*Ts*A1aug);
phi2Aug = expm(d2*Ts*A2aug);
phiTotAug = phi2Aug*phi1Aug;

gamma1 = phi1Aug(1:6,7);
gamma2 = phi2Aug(1:6,7);
gammaTot = phi2*gamma1 + gamma2;

% mInv = [4951.63 -3957.5 24.1844; -0.195095 0.639972
%      0.0975477; 9901.78 -7960.65 49.1079];
% xper0 = mInv*gammaTot;
mInv = eye(6)-phiTot;
xper0 = mInv \ gammaTot;
% xper0 = pinv(mInv)*gammaTot;
xper0Aug = [xper0; 1];
xper1Aug = phi1Aug*xper0Aug;
xper1 = xper1Aug(1:6);
xper2Aug = phi2Aug*xper1Aug;
xper2 = xper2Aug(1:6);
tres = Ts/1000;
t1 = 0:tres:d1*Ts;
t2 = (t1(end)+tres):tres:Ts;
t = [t1 t2];
xper_t1Aug = zeros(7,numel(t1));
xper_t2Aug = zeros(7,numel(t2));

for i=1:1:numel(t1)
```

```matlab
65    xper_t1Aug(:,i) = expm(A1aug*t1(i))*xper0Aug;
66    end
67    for i=1:1:numel(t2)
68    xper_t2Aug(:,i) = expm(A2aug*(t2(i)-t2(1)))*xper1Aug;
69    end
70
71    xper_Aug = [xper_t1Aug xper_t2Aug];
72    xper = xper_Aug(1:6,:);
73
74    Vc1 = xper(1,:);
75    Vc2 = xper(2,:);
76    Vc4 = xper(3,:);
77    Vc5 = xper(4,:);
78    % iL = xper(3,:)+Vout/Rout;
79    iL = xper(5,:);
80    Vco = xper(6,:);
81    Vc3 = Vin-Vc1-Vc2;
82    tdend = find(t>=d1*Ts,1);
83    td2end = length(t);
84    ic1 = gradient(Vc1,t)*Cin;
85    ic2 = gradient(Vc2,t)*Cin;
86    ic3 = gradient(Vc3,t)*Cin;
87    ic4 = gradient(Vc4,t)*Cin;
88    ic5 = gradient(Vc5,t)*Cin;
89    iQ1 = ic4;
90    iQ3 = ic1-ic2;
91    iQ5 = ic2-ic3;
```

```matlab
92
93  iQ2 = ic4 ;
94  iQ4 = ic2−ic3 ;
95  iQ6 = ic5−iL ;
96
97  iQ12 = ic4 ; % Current out of Switching node of Q1 and Q2
98  iQ34 = ic5−ic4 ;% Current out of Switching node of Q3 and
        Q4
99  iQ56 = iL−ic5 ;% Current out of Switching node of Q5 and Q6
100 iQ1(tdend:end) = 0;
101 iQ3(tdend:end) = 0;
102 iQ5(tdend:end) = 0;
103 iQ2(1:tdend) = 0;
104 iQ4(1:tdend) = 0;
105 iQ6(1:tdend) = 0;
106 iCin = Iin−iQ1 ;
```