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Drain Biasing for High Linearity Power Amplifiers

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DRAIN BIASING FOR HIGH LINEARITY POWER AMPLIFIERS

by

WILLIAM P. SEAR

B.S., University of Colorado at Boulder, 2018

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Faculty of the Graduate School of the
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This thesis entitled:
Drain Biasing for High Linearity Power Amplifiers
written by William P. Sear
has been approved for the Department of Electrical, Computer, and Energy Engineering

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The final copy of this thesis has been examined by the signatories, and we find that both the content and the form meet acceptable presentation standards of scholarly work in the above mentioned discipline.
In RF and Microwave communication and RADAR systems it is critical that the transmitter generates sufficient RF output power. In order to achieve that output power amplifiers capable of reaching that output power with linearity such that the signal can be received without significant distortion. In addition to the output power and linearity constraints this amplifier must have high power efficiency to enable their use in power-constrained systems and to prevent thermal issues that can be present in the device. These conflicting requirements form the basis for power amplifier design. The design of RF and microwave power amplifiers (PAs) at RF and microwave frequencies is well understood, but effectively supplying dc bias points to the transistor at the heart of a PA while achieving high output power, linearity and efficiency is poorly documented.

In this thesis the practical effects associated with PA bias line design will be investigated with the CGH27015F transistor, a Gallium Nitride (GaN) based device. This theses will focus on three conflicting design parameters present in bias line design: the RF loss induced in the bias, nonlinear effects due to the impedance presented at low frequencies, and self-modulation effects.

To understand these parameters four PAs were designed that were biased with either quater-wave or shorted stub transmission lines of 50 Ω or 30 Ω characteristic impedance. These lines were tested under two-tone excitation of 5 MHz, 10 MHz, and 20 MHz tone spacing. The presence of a IMD3 "sweet spots" was linked to the nonlinear behavior of the baseband impedance in all four amplifiers. Between the amplifiers the 50 Ω shorted stub design exhibited the lowest IMD3 tone powers of the four designs with the 30 Ω quarter wave line showing the next lowest IMD3 tone powers. The 50 Ω lines exhibited worse self-modulation of the current waveform over the same range of input powers and tone spacings compared to the 30 Ω lines.
DEDICATION

To the many people who have helped carry me to this point.

My parents, Kevin and Karen,

and my sister, Hannah.
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1.1 Motivation and Background

In order for any RF or microwave transmitter to operate it must generate sufficient output power to ensure sufficient "illumination" of the receiving aperture. In communications systems this process is referred to as "making link" and is the driving consideration behind the design of all modern communication and RADAR systems. A block diagram of a typical microwave transmitter system for communications or RADAR is shown in Figure 1.1.

When designing transmitters the RF output power is often heavily constrained by both the antenna and to a greater extent the final amplifier in the transmit chain. This final stage amplifier constrains the overall
output power of the system due to its limited efficiency. Given that this amplifier will involve the greatest total output power its efficiency will drive the overall efficiency of the transmitter system. In order to improve the power efficiency of the final amplifier so that the total transmitter chain can be implemented on power constrained platforms it is designed such that it has less gain than earlier amplifiers in the transmit chain in order to increase efficiency. This design strategy is well understood by the RF and microwave community and this special amplifier is referred to as a "power amplifier" as shown in Figure 1.1.

Most research into power amplifiers conducted today is focused on resolving the "linearity-efficiency compromise" which describes how in conventional power amplifier design any increase in efficiency is paid for by increasing the power of distortion products present at the output of the power amplifier [4]. Most research in this arena focuses on improving the efficiency of a power amplifier relying on digital predistortion (DPD) techniques to reduce the power in intermodulation distortion products [5] [6] [7]. In power amplifiers used on practice, however, the linearity (or how strong the intermodulation distortion terms are) is a far more critical parameter to ensuring effective system operation than power efficiency. Figure 1.2 visualizes the build up of the critical power amplifier parameters. In this work I will attempt to improve the efficiency and linearity of a power amplifier simultaneously by tuning the low frequency behavior of the output of the amplifier which will allow elements of the linearity-efficiency compromise to be circumvented.
1.1.2 Power Amplifier Design Process

Any solid-state based amplifier is designed using one or more non-linear active devices, typically a transistor or transistors. At low frequencies (lower than around 100MHz) these active devices can be used to design operational amplifiers (Op-Amps) which can be used to easily and accurately shape signals in a variety of different ways [8]. Op-Amps are common in most electrical designs at low frequencies. At RF and microwave frequencies, however, each individual transistor has much lower gain. Given that an Op-Amp will have lower gain than any individual transistor it is often impractical to implement any kind of usable Op-Amp. As a result almost all RF and microwave amplifiers (power amplifier and otherwise) are implemented as a single transistor; most commonly in common source configuration (if they are FET-type) or in common emitter configuration (if they are BJT-type).

In a conventional single transistor (also called single-ended) amplifier, the difference between an amplifier designed for maximum gain (a "gain matched amplifier") and a power amplifier is given by the selection of the gate and drain bias voltages and the input and output network impedances at RF frequencies. Figure 1.3
Figure 1.3: Conventional single solid-state transistor PA block diagram showing gate and drain bias tees.

shows a basic block diagram for these main sub-components of a power amplifier. The process by which the output and input matching networks are designed is well understood and can be found in detail in [9].

In this work the analysis, design, and testing will focus on varying the drain biasing implementation to understand how the implementation of that bias perturbs the nonlinear response and efficiency of the power amplifier. The perturbation of the system response due to the bias network will be considered under the effects from the "biasing triangle" shown in Figure 1.4. The tradeoffs associated with the RF loss present in the bias network are already well understood, but the efficiency and linearity of a given bias network design are very poorly understood, making this investigation a valuable addition to the existing body of power amplifier research.

1.2 Thesis Organization

This thesis is organized into seven chapters. In Chapter 2 "weak" and "strong" nonlinear effects in power amplifiers will be investigated and their interactions explained based on existing results from the literature. "Weak" nonlinear effects will be investigated using the Volterra-Wiener nonlinear transfer function model to demonstrate the baseband dependency present in those nonlinear effects. "Strong" nonlinear effects will be briefly discussed using a describing function model which will give some basic guidelines for how those nonlinear effects behave in their limit. Using these results it will be possible to understand how the interaction
between "weak" and "strong" nonlinear behavior can be understood and used from a design perspective.

In Chapter 3 self-modulation and RF loss associated with the bias and supply lines will be considered. The observed gain hysteresis and degraded power added efficiency of a real power amplifier will be explained in terms of the self-modulation of the bias voltage and current waveforms.

In Chapter 4 several single-ended power amplifier designs based on the CGH27015F GaN fifteen watt transistor from Cree (now Wolfspeed) will be designed to test the bias line effects explained in Chapters 2 and 3.

In Chapter 5 the testing methodology used to characterize the performance of the amplifier designs proposed in Chapter 4 will be discussed. The required test bench specifications to characterize the power amplifiers under test will be derived for the four classes of measurement that need to be performed; single tone (CW) measurements, two tone measurements, drain voltage and current waveform measurements, and complex modulation signal measurements. The calibration process and calibration results will also be
discussed.

In Chapter 6 the results of testing four of the amplifiers described in Chapter 4 using the test bench described in Chapter 5 will be presented. Networks F, G, H, and I will be tested under CW, two tone, and complex modulation conditions and the effects of self modulation and "soft" nonlinearity driven by baseband terminations will be discussed as a function of the different bias designs.

In Chapter 7 the key results of this work will be drawn. Several interesting applications of this work will be discussed along with proposed future research.
CHAPTER 2

UNDERSTANDING AMPLIFIER NONLINEARITY

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2.1 Conventional Nonlinearity Measurements and Metrics

Characterizing the linearity of a given power amplifier is very important to ensuring that the output signal will behave as a minimally perturbed scaled copy of the input signal. In general the best measurement approach when dealing with linearity is to generate a waveform similar to the one the PA will operate on in practice, pass that signal through the PA, and receive and decode that signal at the output. This measurement allows the "error-vector-magnitude" (EVM) or the bit error rate (BER) to be calculated. The BER is a more common measurement in industry as it directly relates to the quality of the link. A higher BER will result in the loss of more signal data which will require more retransmissions thus lowering the effective data rate of the link [10]. The EVM is a more general measurement which determines how much the IQ
vector has been perturbed from its desired value by the power amplifier [10]. Both BER and EVM are good evaluation criteria for power amplifiers, but their usefulness as design parameters is limited by their very strong dependence on the modulation waveform.

In order to model the nonlinear behavior of a power amplifier in a more arbitrary way the "two-tone" test measurement is used. In a two-tone test two single-frequency tones around a center frequency with some spacing are applied to the DUT as the RF excitation. The use of two-tones provides a complex signal envelope (as opposed to the static signal envelope present in a single tone) that will induce harmonic distortion in the power amplifier. A two-tone signal can be modeled at the input of the PA as two cosine functions with frequencies that differ by the tone spacing. When these tones are fed to the PA they are frequency multiplied against each other due to the nonlinear response of the transistor active device. The resulting signal can be understood by taking a Taylor series expansion of the multiplication of the two-tones. The mathematics behind this model are well known in the PA community and can be found in textbooks such as [9]. The resulting Taylor series expansion gives rise to a handful of key terms as shown in Figure 2.1; in addition to the fundamental two-tones a DC term, second harmonic terms, and third order intermodulation terms are generated. The relative strength of each of these terms is proportional to the power of the two input tones (each tone is defined to have equal power) and to the selected bias point for the device. The bias point dependency of the intermodulation products is such that for lower quiescent drain currents (and associated lower waveform conduction angle) the intermodulation tone power increases due to the efficiency-linearity compromise previously described [4]. In general the DC and second harmonic terms are ignored as they are outside of the RF bandwidth of interest. The intermodulation terms cannot be ignored because they lie right beside the fundamental tones at $2\omega_{c1} - \omega_{c2}$ and $2\omega_{c2} - \omega_{c1}$. In a practical PA which must conform to FCC rules on adjacent channel power (usually specified as "adjacent channel power ratio" ACPR) these terms are very difficult to eliminate without backing off the RF output power to reduce their magnitude. Intermodulation terms of both even and odd orders are generated, but the primary contributors to in-band distortion are the third order components. The two-tone test lacks the complexity of a real signal waveform, but a complex modulated waveform can be modeled as a larger sequence of adjacent tones with intermodulation products that are the sum of the intermodulation responses of each tone pair as shown for the case of a three tone
Figure 2.1: two-tone amplifier test theoretical output spectrum up to second harmonic component showing the third order intermodulation product.

excitation in Figure 2.2. This result indicates that the intermodulation distortion seen in the ACPR of a real complex modulated signal will vary proportionally to the intermodulation product magnitudes measured in the two-tone case [11] [12].

To provide a metric for the relative strength of these third order intermodulation products of different PAs the third order intercept point (commonly abbreviated as "IP3") is used in industry [13]. The IP3 is a small signal measurement that relies on the expected performance of the fundamental tone power and third order distortion tone power as a function of input tone power. In general the fundamental tone is assumed to experience a 1:1 output:input power relationship (assuming constant gain as a function of power) until the output power of the device begins to compress as the transistor is no longer capable of providing that constant gain. The third order intermodulation product can be modelled with the Taylor series approximation to experience a 3:1 output:input power relationship that starts with significantly less tone power than the fundamental tone. Assuming this behavior holds it is possible to measure the one fundamental tone power and one intermodulation product tone power (either upper or lower tones) and then draw a line from each with a slope of one or three respectively until they meet. The point where those two lines intersect is the IP3. The IP3 can be expressed in terms of the output power of the PA that would be present at that point assuming
no gain compression (OIP3) or in terms of the input excitation at that point (IIP3). Figure 2.3 shows this assumed relationship graphically.

Unfortunately, real PAs do not follow the ideal power curves from the Taylor series expansion under large-signal excitation. In many real PAs a "sweet spot" in the intermodulation response occurs where the power of the third order intermodulation product is reduced significantly from the modelled, ideal intermodulation power curve [14]. This "null" in intermodulation response is accompanied by an observed gain expansion for the fundamental tone if the "null" occurs close to when the PA will begin to compress [15]. This more typical amplifier response compared to the ideal model is shown in Figure 2.4.

The Taylor series approximation commonly used to understand the nonlinear response of PAs and its associated IP3 metric are insufficient to completely characterize the nonlinear response of a PA. In order to better understand the nonlinear behavior of a given PA and its associated transistor active device the nonlinear performance can be treated as a function of two different types of nonlinearity. The first type of nonlinearity is "weak" nonlinearity. Weak nonlinearity describes the nonlinear response of a transistor due to its variation in $g_m$, $g_d$, and output capacitance as a function of frequency and power. In section 2.2 a simple...
Figure 2.3: $P_{out}$ versus $P_{in}$ response of an ideal amplifier under two-tone excitation as assumed in the IP3 calculation. $P_{out}$ and $P_{in}$ are typically plotted for one of the fundamental tones (lower or higher) and one of the $IM_3$ tones (lower or higher).

Figure 2.4: $P_{out}$ versus $P_{in}$ response of an amplifier exhibiting "sweet spot" response in its $IM_3$. $P_{out}$ and $P_{in}$ are typically plotted for one of the fundamental tones (lower or higher) and one of the $IM_3$ tones (lower or higher).
model will be used to characterize and describe the observed PA distortion at low signal powers where weak nonlinearity dominates. The second type of nonlinearity is "strong" nonlinearity. Strong nonlinearity arises from clipping effects in the PA that occur when the dynamic RF waveforms are limited by some aspect of the transistor (most commonly the waveform clipping into the knee voltage). These nonlinear effects are at the center of the linearity-efficiency compromise described previously. In Section 2.3 a process for modelling strong nonlinear behaviour and some useful results of that model will be discussed. Finally in Section 2.4 key results from the weak and strong nonlinear behavior of a transistor will be used to understand the nonlinear behavior in the region where the PA is just beginning to compress and neither soft nor hard nonlinearity is dominant.

2.2 "SOFT" NONLINEARITY

A transistor’s magnitude and phase response to excitation will exhibit distortion due to variations in the transconductance, drain conductance, and output capacitance of the device which collectively form the channel nonlinearity. In the weak nonlinear domain the channel response can be reasonably approximated as a linear system. This approximately linear response indicates that a Volterra-Wiener nonlinear transfer function model is appropriate [16]. The Volterra-Wiener nonlinear transfer function model block diagram is shown in Figure 2.5 where each transfer function beyond the first has terms including the previous transfer functions.

In [17] Nuno Borges Carvalho and José Carlos Pedro use a variation of this modelling approach to extract the appropriate transfer functions to describe the transistors channel nonlinearities using the circuit model shown in Figure 2.6. In the circuit model shown in Figure 2.6 the transistor ideal output current source \( i(t) \) is placed in parallel with the load admittance \( Y_L(\omega) \) and the bias point dependant nonlinearities are modelled as a parallel capacitance and resistance. Using this simple circuit model of the transistor the nonlinear component of the output current \( i_{nl}(t) \) can be extracted as a function of the nonlinear elements and presented load impedance. The nonlinear current can be used in nonlinear current volterra analysis to derive a Volterra-Wiener model [16].
Volterra-Wiener Model of Nonlinear Systems

Figure 2.5: Block diagram of the Volterra-Wiener nonlinear transfer function model for N frequency excitation frequencies.

Ideal Transistor Model with Nonlinearities

Figure 2.6: Equivalent transistor model for applying the nonlinear current method of Volterra series.
In this analysis we will consider a nonlinear current of the form shown in Equation 2.1 which incorporates second and third order nonlinear terms in the channel. Higher order nonlinear terms will not be present in the Volterra-Wiener nonlinear model for a third order intermodulation product and they can therefore be dropped for this analysis. Following the definition of the Volterra-Wiener nonlinear model the first, second, and third order nonlinear transfer functions are given by Equations 2.2, 2.3, and 2.4 respectively [17].

\[
i_{nl} = G_2V^2(t) + G_3V^3(t) + \frac{d}{dt}(C_2V^2(t) + C_3V^3(t)) \quad (2.1)
\]

\[
H_1(\omega) = \frac{1}{I_L(\omega)} = Z_L(\omega) \quad (2.2)
\]

\[
H_2(\omega_a, \omega_b) = -Z_L(\omega_a + \omega_b)[G_2 + j(\omega_a + \omega_b)C_2][H_1(\omega_a)H_1(\omega_b)] \quad (2.3)
\]

\[
H_3(\omega_a, \omega_b, \omega_c) = -\frac{Z_L(\omega_a + \omega_b + \omega_c)}{6}\left\{ 2[G_2 + j(\omega_a + \omega_b + \omega_c)C_2][H_1(\omega_a)H_2(\omega_b, \omega_c) + H_1(\omega_b)H_2(\omega_a, \omega_c) + H_1(\omega_c)H_2(\omega_b, \omega_a)] + [G_3 + j(\omega_a + \omega_b + \omega_c)C_3][H_1(\omega_a)H_1(\omega_b)H_1(\omega_c)] \right\} \quad (2.4)
\]

With closed-form equations that model the nonlinear amplitude and phase response of a real transistor under low power excitation we can substitute the appropriate frequency excitations to model the third order intermodulation product into Equation 2.4. Equations 2.5 and 2.6 show the resulting terms for the lower and higher frequency intermodulation products respectively.

\[
H_3(\omega_1, \omega_1, -\omega_2) = -\frac{Z_L(2\omega_1 - \omega_2)}{6}\left\{ 2[G_2 + j(2\omega_1 - \omega_2)C_2][H_1(\omega_1)H_2(\omega_1, -\omega_2) + H_1(\omega_1)H_2(\omega_1, -\omega_2)] + H_1(-\omega_2)H_2(\omega_1, \omega_1) + [G_3 + j(2\omega_1 - \omega_2)C_3][2H_1(\omega_1)H_1(-\omega_2)] \right\} \quad (2.5)
\]

\[
H_3(\omega_2, \omega_2, -\omega_1) = -\frac{Z_L(2\omega_2 - \omega_1)}{6}\left\{ 2[G_2 + j(2\omega_2 - \omega_1)C_2][H_1(\omega_2)H_2(\omega_2, -\omega_1) + H_1(\omega_2)H_2(\omega_2, -\omega_1)] + H_1(-\omega_1)H_2(\omega_2, \omega_2) + [G_3 + j(2\omega_2 - \omega_1)C_3][2H_1(\omega_2)H_1(-\omega_1)] \right\} \quad (2.6)
\]

Equations 2.5 and 2.6 are complex with dependencies on the load impedances presented to every harmonic term present under a two-tone excitation. In order to simplify these equations and gain more
valuable insight into how these nonlinear terms behave we will make what Pedro and Carvalho call the "narrowband approximation." The narrowband approximation assumes that the load impedance presented to each fundamental tone and the load impedance presented to each intermodulation product are approximately the same ($Z_L(\omega_1) \approx Z_L(\omega_2)$, $Z_L(2\omega_1 - \omega_2) \approx Z_L(2(\omega_2 - (\omega_1))$). Using this approximation we can see that only one term in Equations 2.5 and 2.6 differs; $H_2(-\omega_2, \omega_1)$ in Equation 2.5 and $H_2(-\omega_1, \omega_2)$ in Equation 2.6. The resulting second order transfer functions that differ in Equations 2.5 and 2.6 are given in Equations 2.7 and 2.8 respectively. In both equations we can see that there is a clear baseband term dependency that is influenced directly by the third order channel nonlinearities $G_3$ and $C_3$ and by the fundamental RF component termination. Given that $\omega_1$ and $\omega_2$ have opposite signs in each equation and if we assume $\omega_2 > \omega_1$ then $\omega_1 - \omega_2$ which appears in Equation 2.7 will be a negative frequency component which "folds back" in the frequency domain. This means that the two second order nonlinear transfer functions that include the baseband dependency are complex conjugates of each other ($H_2(-\omega_2, \omega_1) = H_2(-\omega_1, \omega_2)^*$).

\[
H_2(-\omega_2, \omega_1) = -Z_L(\omega_1 - \omega_2)[G_3 + j(\omega_1 - \omega_2)C_3]H_1(\omega_1)H_1(-\omega_2) \tag{2.7}
\]

\[
H_2(-\omega_1, \omega_2) = -Z_L(\omega_2 - \omega_1)[G_3 + j(\omega_2 - \omega_1)C_3]H_1(\omega_2)H_1(-\omega_1) \tag{2.8}
\]

Given this new relationship between the two different terms we can go back to the "top level" third order nonlinear transfer function to understand how the presence of the baseband impedance perturbs the overall weak nonlinear response. In Equation 2.5 the immediate context for the baseband term is given by Equation 2.9 (Equation 2.6 has identical context under the narrowband approximation). Equation 2.9 can be further simplified by factoring out the baseband-dependent nonlinear transfer function as shown in Equation 2.10. From Equation 2.10 we can see that the baseband term is multiplied against a term that varies with the impedance presented to the fundamental RF signal and subsequently added to a term that varies with the impedance presented to the fundamental RF signal and the second harmonic impedance. Given that the terms shown in Equation 2.10 are then multiplied against all other terms in Equation 2.5 to determine the overall intermodulation product strength, we can see that selecting a baseband impedance such that the two sets of terms cancel will minimize the strength of the intermodulation product in the weak nonlinear regime.
\[ H_1(\omega_2)H_2(\omega_2, -\omega_1) + H_1(\omega_2)H_2(\omega_2, -\omega_1) + H_1(-\omega_1)H_2(\omega_2, \omega_2) \]  
(2.9)

\[ H_2(\omega_2, -\omega_1)[H_1(\omega_2) + 1] + H_1(-\omega_1)H_2(\omega_2, \omega_2) \]  
(2.10)

Given that the lower and higher frequency intermodulation products are dependant on the baseband impedance and its complex conjugate respectively we can clearly see that a complex fundamental harmonic and second harmonic impedance will give rise to an asymmetric third order intermodulation response. Using the above relationships Pedro and Carvalho extend this analysis to provide the necessary system conditions for asymmetric intermodulation tone magnitudes to appear as below.

**Necessary Device Conditions for Asymmetric Third Order Intermodulation Terms [17]:**

1. Third order direct mixing due to waveform clipping (strong nonlinearity) cannot be larger than second degree coefficients \( G_2 \) and \( C_2 \).

2. The baseband Termination \( Z_L(\omega_2 - \omega_1) \) must have a "significant" reactive part.

3. The real part of the second harmonic termination and baseband terminations must be greater than their reactive parts.

4. Imaginary parts of second harmonic terminations and baseband termination should have comparable magnitudes.

5. If the second harmonic termination is purely resistive, IMD asymmetry can still be observed in the presence of a large reactive nonlinearity.

The above mathematics also give rise to a vector graphic interpretation of the intermodulation magnitude as a function of input power that was originally proposed by John Sevic [18]. This depiction of intermodulation was expanded on by James Brinkhoff et. al. and will be discussed in more detail in Section 2.4 [1].
2.3 "Hard" Nonlinearity

Under large-signal power excitation the transistor output waveform will exhibit clipping effects that will dominate the intermodulation product response over the weak nonlinear behaviors previously discussed [9]. Under large-signal excitation the Volterra-Wiener model cannot hold and another nonlinear model must be used. Currently a describing function is the preferred nonlinear model for describing intermodulation response under large-signal excitation [19]. Unfortunately, the describing function model does not provide a closed form set of solutions that can be used to gain insight into how the intermodulation products vary. However, by assuming the transistor device obeys power conservation it is possible to relate the response of the intermodulation product to the fundamental tones in their saturation limit. This analysis approach was first developed by E. Ballesteros et. al. in [20] who developed a relationship between the fundamental tone power and the intermodulation tone power and took their excitations to an infinite input power.

To conduct this analysis we first consider how the intermodulation power ($I$) varies as a function of RF fundamental power ($S$) as a function of input drive power ($A$). This relationship can be approximately modelled as in Equation 2.11 [20]. Given a relationship between the signal and intermodulation powers we assume that the signal power will saturate at a given power level (as described by Equation 2.12). With a finite signal output power, in the limit of large-signal excitation it is possible to solve Equation 2.11 as a function of $S_s$ (the signal saturation power) as shown in Equation 2.13. From Equation 2.13 we get that the intermodulation power will tend to one third that of the signal power and, more importantly, that it will be one hundred eighty degrees out of phase with the signal tones.

$$I(A) = S(A) - \frac{4}{A^3} \int_0^A x^2 S(x) dx$$  \hspace{1cm} (2.11)

$$\lim_{A \to \infty} S(A) = S_s$$  \hspace{1cm} (2.12)

$$I(A) = -\frac{1}{3} S_s$$  \hspace{1cm} (2.13)
2.4 **Baseband Impedance and Nonlinearity**

Now that we have some intuition as to how the intermodulation product behaves in the weak and strong nonlinear regimes of operation we must now consider the transition region where both sources of nonlinearity are equivalent in their effect. The transition region of input powers is also critical as this is the point where the "sweet spot" behavior can appear, and in fact we can show that the sweet spot response is due to the interaction of these two types of nonlinearity.

In order to induce a sweet spot it is well known that the selection of the device bias point is critically important [14]. A bias point that exhibits a sweet spot is characterized by low channel nonlinearities (G and C) such that the dominant contributors to the intermodulation distortion response are the impedance terminations discussed in Section 2.2. If the baseband termination (and other terminations) are selected such that the weak nonlinear response is in-phase with the fundamental RF tones then at some point in the transition region the near one hundred eighty degree out of phase strong nonlinearity will additively cancel with the weak nonlinearity response [21].

Given that the ability to generate sweet spot responses at suitable bias points is a potentially valuable capability we need to consider how to optimally select the baseband impedance. Assuming that the PA we are designing is a conventional Class-A to Class-B power amplifier, the fundamental frequency impedance is already constrained to provide maximum output power and efficiency, and the subsequent harmonic impedances should be shorted. Given that the second harmonic impedance should be shorted, from Equation 2.10 we can determine that the baseband impedances up to the maximum signal bandwidth should also be shorted. Figure 2.7 visualizes the overall desired $Z_L$ that should be presented to the transistor drain.

In the more general case of a power amplifier where the termination of the second harmonic is some arbitrary non-zero value we may need another baseband response. James Brinkhoff et. al. have developed a graphical representation for intermodulation product response as a function of two vectors, a $K_C$ vector that is dependent on the fundamental and second harmonic termination impedances and a pair of $K_D$ and $K_D^*$ vectors that are dependent on the baseband termination impedance and its complex conjugate [1]. Figure 2.8 visualizes the typical behavior of this plot for a complex second harmonic termination as compared
Figure 2.7: Ideal bias line impedance presented to the drain ($Z_{in}$) over frequency for a Class-A to Class-B power amplifier.

Figure 2.8: Vector-based graphical representation of IMD3. Graphic reproduced from [1].

to a purely real termination. Here the asymmetric response of lower and upper intermodulation products can be clearly seen to arise from the complex conjugate relationship discussed in Section 2.2. Using this visualization tool it is also very clear that the lowest possible intermodulation product (for a passive baseband termination) is given by making the magnitude of the $K_D$ (and associated $K'_D$) vector zero. This occurs when Equation 2.10 tends to zero magnitude, just as in the Class-A to Class-B amplifier design case.
CHAPTER 3

BIAS NETWORK EFFECTS

Contents

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3.1 RF Loss

Conventional bias lines are implemented either with inductors or with quarter wavelength long transmission lines. Each of these biasing techniques is used for their ability to pass dc power and to prevent RF loss down the dc biasing path. With the inductor, RF loss is prevented by the high reactive impedance presented at the fundamental RF frequency, and with the quarter wavelength transmission line a short termination at the dc feedpoint is transformed into an open circuit at the transistor drain. RF loss down the bias network is conventionally the only engineering constraint applied to amplifier design [22]. While the RF loss in the drain bias path is certainly a critical design parameter, these two design approaches suffer when the nonlinearity response modelled in Chapter 2 is considered. To compensate for the "bias line memory effect," the standard approach is to apply digital predistortion (DPD) without regard to the underlying analog parameters causing the nonlinearity [23].
This issue associated with focusing bias line design around only RF loss is exceptionally pronounced in broadband bias chokes such as the 4310LC from Coilcraft. The impedance response of this device over frequency can be seen in Figure 3.1 and is representative of the impedance response of broadband inductor bias chokes. While the inductor does provide a large impedance over a wide RF bandwidth and therefore has low RF loss at those frequencies, it presents as much as 150 $\Omega$ impedance at the 10 MHz baseband frequency. This impedance is significant compared to the small impedances usually presented to the fundamental and second harmonic impedances which means that, as discussed in Chapter 2, we would expect the intermodulation products for a power amplifier implemented with this component to be significantly perturbed by the weak nonlinearity response of the transistor.
3.2 Drain Voltage Bias Point Self-Modulation

In addition to RF loss and weak nonlinearity response, there is a third critical engineering design parameter: the self-modulation of the drain voltage. The self-modulation of the drain voltage is best understood by modelling a real inductor that is used as an RF choke as shown in Figure 3.2. The dc component of the voltage applied to the drain of the transistor ($v_{d0}$) is given in Equation 3.1 where $i(t)$ is the current passing through the ideal inductor and winding loss resistor $R_l$ [24]. Under CW tone excitation the power amplifier drain voltage dc component will be the non-time varying quantity $V_{DD} - R_l i(t)$. Under two tone (or complex modulation) the current drawn by the transistor will vary with the complex modulation envelope [25].

$$v_{d0} = V_{DD} - L \frac{di(t)}{dt} - R_l i(t) \tag{3.1}$$

In a simple two tone complex envelope there are two periods of interest that happen for identical amounts of time, an exponentially increasing drain current period and an exponentially decreasing drain current
Figure 3.3: The ideal drain current waveform \((v_{d0})\) compared to a real drain current waveform with inductance present in the bias line. The voltage-limited region of operation is called out in the dashed box.

period. In the exponentially increasing case the actual drain voltage will be lowered from that applied by an external supply proportionally to the inductance value and to the input excitation strength. In the exponentially decreasing case the actual drain voltage will be greater than that applied by an external supply proportionally to the inductance value and the input excitation strength. Figure 3.3 captures the ideal drain current waveform described above against a highly inductive bias line’s current waveform.

When this "self-modulation" of the drain bias voltage is present the gain response of an amplifier is shifted as the available power periphery of the device is being modulated by the shifting \(i(t)\) and \(v_{d0}\) waveforms. For low input signal powers the gain will not be changed because the current drawn by the device is low, and therefore the effective drain bias voltage will be shifted at most by tens of millivolts. For high input signal
powers the output gain will tend towards the saturated output power as the signal power approaches the power limits of the device. For intermediate powers, however, the measured gain response becomes hysteric. The hysteric response occurs because the current waveform affects the instantaneous dc component of the voltage waveform enough that it lowers the available power of the device and in the process lowers the gain [3]. In Figure 3.4 this behaviour is shown for a input power sweep with a complex modulation envelope.

In addition to the gain hysteresis the instantaneous power added efficiency of the amplifier will be degraded. Specifically, in the period where the drain current increases the voltage is reduced and the transistor is fundamentally voltage limited. This causes the actual current to be lower than predicted by the ideal model which results in a lower instantaneous efficiency [26]. Conversely when the drain current is diminishing the instantaneous efficiency approaches that found in the ideal model. In this case the transistor is current limited as the current reaches the modelled level determined by the complex modulation envelope.
Chapter 4

CGH27015F Amplifier Design

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4.1 Device Selection and Context

Historically power amplifiers were designed using vacuum tube systems such as travelling wave tubes, still produced for a variety of designs in industry [27]. However, the high design risk to mechanical failure, difficult production process, and large size of tube-based power amplifiers has pushed the focus of power amplifier research towards solid state devices. Over the past fifty years semiconductor devices made of Germanium (Ge), silicon (Si), gallium arsenide (GaAs), indium phosphide (InP), gallium nitride (GaN), and a myriad combinations of those component elements have been evaluated for use in power amplifiers [28]. Of these, GaN has proven to be the most promising for power amplifier future development due to its high electron mobility and very high breakdown voltage (usually in the range of 100V) which allows significantly higher output power from a smaller transistor device [29].

For this work the GaN CGH27015F 15 W Cree (now Wolfspeed) device optimized for operation at S-band frequencies is used. This particular transistor was selected due to the presence of a potentially more powerful device model developed by Professor Patrick Roblin of the Ohio State University for the device [30] and due to personal previous design experience with this particular device [31]. Given these factors and the test bench equipment described in Section 5.2.2 we consider the CGH27015F device to be an appropriate candidate device for this work.

4.2 Mechanical Heat-sink Interface Design

In order to effectively interface with the CGH27015F transistor and ensure that the power dissipated within it is effectively managed an aluminum block heat-sink was designed and fabricated. This heat-sink was implemented on spare aluminum 6061 block measuring approximately two inches by five inches by one inch. Tapped and chamfered mounting points for 14 #2-56 screws capable of securing two side-by-side CGH27015F flange mounted devices and separate input and output matching structures. The mechanical
The CGH27015F device was originally selected by Professor Patrick Roblin for additional modeling because the device design at the semiconductor level is optimized for operation in a "deep" Class-B bias.
between 2.1 GHz and 2.5 GHz [30]. Given the focus on operating the device within this frequency range with a bias of 28 V on the drain and -3 V on the gate the transistor has several oddities in its performance that are worth exploring.

We begin the analysis of the CGH27015F by considering the IV curve of the device. The modelled IV curve from the Angelov-based device model can be seen in Figure 4.2. In Figure 4.2 the characteristic IV "sag" of a GaN transistor is clearly visible [33]. For gate voltages close to -2 V, the current draw at high powers are closely clustered as the device is designed to draw larger currents at lower drain voltage biases and thus mitigate potential current collapse in the device [22]. The device exhibits the characteristic 7 V GaN dc knee voltage. Because the CGH27015 is designed for operation at low drain bias voltages, it will be sensitive to "knee walkout" effects. This exhibits a similar gain compression response caused to that by self-modulation effects [24] [34]. As a result, these two effects cannot be independently characterized for the CGH27015F with the experimental setup used here.

Given the device’s simulated IV curve and the manufacturers recommendations all amplifier designs will be done assuming a nominal drain bias of 28 V and -3 V as shown in Figure 4.2.

![Figure 4.2: Simulated DC IV curve of CGH27015F Transistor assuming 8 Ω thermal resistance and operation at room temperature.](image-url)
With nominal gate and drain bias voltages defined it is now valuable to understand the device response to perturbations from that bias selection and the appropriate transistor parameters associated with that derivation. We begin by exploring the basis of the current describing function associated with a drain bias of 28 V. The dc drain current response to changing $V(t)_{gs}$ is shown in Figure 4.3. This curve shows the near Class-B current response as -3 V that is expected from the dc IV curve measured in Figure 4.2 and also shows some significant "ripple" present in the current response. In an ideal transistor device the drain current draw from $V(t)_{gs}$ would be purely linear (following $g_m V_{gs}$) but the presence of increased current draw between -2.5 volts and -1.5 volts indicates the presence of higher order $g_m$ (or potentially $g_d$ and $g_{md}$) terms.

![Figure 4.3: Instantaneous $I_{DS}$ response due to $V_{gs}(t)$ excitation.](image)

In order to understand the $g_m$ response on its own as a function of dc $V_{gs}$ selection the simulated value of $g_m$ was extracted from the Angelov model under the described operating conditions for a range of frequency points around 2.2 GHz. The resulting $g_m$ is plotted in Figure 4.4. The $g_m$ plots that show significant "ripple" above the -3 volt bias correspond to frequencies below 2.1 GHz with the curve with a $g_m$ response of 10 occurring at 2 GHz. These $g_m$ functions have significant higher order nonlinearities that will dominate the baseband response as described in Section 2.2. This result can be most clearly seen in Figure 4.5 where the
$g_m$ response is plotted explicitly over frequency as $V_{gs}$. It can be clearly shown that the device exhibits a high transconductance response around 2 GHz which would normally suggest operation in that region, but Figure 4.4 clearly shows that this high transconductance is also associated with increased "weak" nonlinearity which will degrade the performance of a practical amplifier.

![Transconductance vs. Gate Bias and Frequency](image)

Figure 4.4: Transconductance as a function of gate bias point voltage over carrier frequency.

One further important characteristic of this device is its stability as a function of frequency. As previously described the CGH27015F is designed to operate in the 2 GHz to 2.5 GHz range and internally tuning to such a narrow frequency range usually has stability effects. The default stability response as measured by the k-factor of the device terminated in 50 Ω is shown over frequency and $V(t)_{gs}$ at $V_{DD} = 28$V in Figure 4.6. It is immediately obvious that this device’s operational dynamic performance will be limited by its stabilization networks as the k-factor is low over the entire band up to the maximum frequency of the device. The higher k-factor exhibited between 4 GHz and 6 GHz is indicative of the device having highly reactive second harmonic termination response at its input which will likely make both stabilization and termination at those frequencies difficult.
Figure 4.5: Transconductance as a function of frequency over gate bias point voltage.

Figure 4.6: K-factor of CGH27015F at $V_{DD} = 28V$ over frequency for $V(t)_{gs}$ from -3.5V to -2.5V.
4.4 Determination of Fundamental RF Frequency

Load and Source Impedances

With nominal bias points selected and the basic response of the device characterized we move to determine the fundamental harmonic terminations of the input and output matching networks at the gate and drain respectively. The optimum load and source impedances are found using the load- and source-pull methods commonly used in industry [9]. Load- and source-pull simulations were run simultaneously to determine the device response to changing load and source impedances. The ideal source impedance was determined to be $Z_S = 1.75 - j2.6 \, \Omega$ for maximum power added efficiency and delivered power as shown in Figure 4.7.

When the source impedance is fixed at the ideal value we consider the effect of shifting the load impedance. The resulting device response for power added efficiency and delivered power is shown in Figure 4.8. The maximum power delivered to the load by this transistor at 1 dB of output power compression is 43 dBm (19.95 watts) at $Z_{L,P_{max}} = 13.5 - j3.45 \, \Omega$. However, this output power would require a large RF input power to reach this output power which would complicate the final test setup as I did not have access to a driver amplifier capable of linear operation up to the needed source power. As a result the actual source impedance was selected to be $Z_L = 13.45 + j6.5 \, \Omega$ to improve the device PAE, reduce the 1 dB output power compression point to 41 dBm (12.59 watts), and improve the maximum available gain of the device (thereby lowering the input power needed in final test). This limitation in available test equipment does not affect the conclusions drawn in this study. All PAs will be designed such that this impedance (or some very similar value) will be presented at the fundamental frequency such that the only significant difference in the PA designs are the baseband impedance they present.
Before considering the RF frequency matching it is critical that a stability network or networks be implemented such that the power amplifier as a whole exhibits a k-factor greater than one across all frequencies. To first attempt to stabilize the network at low frequencies, a 6.8 pF blocking capacitor was placed in parallel with a resistor $R_1$ and then placed in series with the gate of the CGH27015F. The resulting stability response
Figure 4.8: Simulated load-pull delivered power $P_{\text{del}}$ and power added efficiency (PAE) curves of CGH27015F with optimum source termination into a 50 $\Omega$ nominal load under 1dB output power compression at 2.2 GHz.

of the amplifier with optimal component values is captured in Figure 4.9.

The simple stability network shown in Figure 4.9 was insufficient to ensure stability at low frequencies as the k-factor is simulated to be smaller than one around 500 MHz and between 2 GHz and 3 GHz. To further improve the network response an additional resistor $R_2$ was placed in series with the RC network on the gate of the CGH27015F device. The resulting power amplifier stability and matching response with optimal component values is captured in Figure 4.9. The addition of $R_2$ can be seen to improve the k-factor response.
Figure 4.9: Simulated (a) k-factor and (b) power amplifier input and output matching response over critical frequency range of (c) two element stability network.

around 500 MHz but does not improve the k-factor between 2 GHz and 3 GHz.

The three element network shown in Figure 4.9c is insufficient to ensure overall device stability indicating an additional stability network should be introduced. Given the stability problem no centering on the 2 GHz to 3 GHz frequency band a series RC circuit ($R_3$ and $C_2$) was placed between the signal line and ground.
at the input to the previously designed stability network. The k-factor and matching response of the power amplifier with optimal component values is shown in Figure 4.11. We can see that the k-factor is greater than one at all frequencies (as desired) and that the k-factor is close to one near 2.2 GHz to ensure maximum available transistor gain [35]. The “dip” in the k-factor response around 500 MHz is concerning, but the addition of resistance in $R_2$ can resolve instability issues in test should they arise. For design we avoid a
large $R_2$ value if at all possible as it will adversely affect both the gain and PAE of the amplifier.

Figure 4.11: Simulated (a) k-factor and (b) power amplifier input and output matching response over critical frequency range of (c) final stability network.

4.5.2 RF Impedance Matching Network Design

With an adequate stability network designed the fundamental frequency impedance match at the gate of the CGH27015F can be designed. Given the target $Z_S = 1.75 - j2.6 \ \Omega$ impedance and the final stability
network shown in Figure 4.11c it was decided to implement the bias line as a simple 50 Ω characteristic impedance $\lambda/4$ line at the input to the stability network with a linear, triangular taper matching the circuit to a 6.8 pF bypass capacitor and a 50 Ω input SMA edge-mounted female connector. The taper was used in an attempt to ensure that the network behaved sufficiently like a low pass network over all RF frequencies for large tone spacings that it introduced no new memory response that could potentially dominate over the baseband response [36]. The resulting optimized layout for Rogers 4350b with a height of 20 mil is shown in Figure 4.12.

![Figure 4.12: Final input matching network with stability network layout.](image-url)

The input impedance response of the network shown in Figure 4.12 was simulated as a function of frequency to find impedance looking into the input matching network from the CGH27015F gate as shown in Figure 4.13. A 2.2 GHz the designed input matching network presents an impedance of $Z_{S,\text{real}} = 6.46 - j3.88$ Ω rather than the desired $Z_S = 1.75 - j2.6$ Ω. The computed $Z_{S,\text{real}}$ is sufficient to match the gate of the transistor without significant loss of gain or efficiency (as we can see by comparing the two loads on Figure 4.7) given the inherent matching quality tradeoff that was introduced in the selection of the tapered matching approach [37].
Given that the input matching network shown in Figure 4.12 is sufficient for the needs of this study it was fabricated on Rogers 4250b and copper plated using LPKF equipment available to the RF power and analog laboratory (RFPAL). The resulting network was populated as shown in Figure 4.14 and used to test a variety of output matching network biasing implementations as described in Chapter 5 to find the results shown in Chapter 6.
4.6 Bias Network Configurations Under Test

With nominal bias voltages for the gate and drain selected and desired RF impedances’ determined it is now important to consider the potential bias line implementations and how those bias lines would perturb an RF match. Table I shows the nine potential bias line implementations that will be considered in this work.

Table 4.1: Proposed Bias Line Implementation Networks.

<table>
<thead>
<tr>
<th>Network</th>
<th>Bias Line Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>&quot;Small&quot; Inductor</td>
</tr>
<tr>
<td>B</td>
<td>&quot;Large&quot; Inductor</td>
</tr>
<tr>
<td>C</td>
<td>Coilcraft Conical Inductor</td>
</tr>
<tr>
<td>D</td>
<td>Piconics Conical Inductor</td>
</tr>
<tr>
<td>E</td>
<td>&quot;Resonating&quot; Inductor (parallel LC tank)</td>
</tr>
<tr>
<td>F</td>
<td>50 $\Omega \lambda/4$ Line</td>
</tr>
<tr>
<td>G</td>
<td>30 $\Omega \lambda/4$ Line</td>
</tr>
<tr>
<td>H</td>
<td>50 $\Omega$ Shorted Stub</td>
</tr>
<tr>
<td>I</td>
<td>30 $\Omega$ Shorted</td>
</tr>
</tbody>
</table>

Figure 4.14: Final input matching network with stability network as fabricated installed on heat-sink.
Each network will be described in detail in upcoming sections. In Chapter 6 networks F-I will be tested in detail. Networks A-E were designed and fabricated but due to a lack of testing time were not tested.

4.7 Output Match Design

4.7.1 Network A-E: Inductor Based Bias Design

4.7.1a General Network Design

We begin by considering Networks A through E which are biased through various flavors of inductor. For every design considered in this section the goal is to implement the design such that $\Gamma_{fo}$ seen looking into the output matching network is equal for every output network. In an inductor-based bias the impedance of the inductor is zero at dc and some high impedance at the fundamental RF frequency because the impedance of an inductor varies as Equation 4.1. From this result there is a straightforward design trade where a low inductance value will present a lower impedance over a greater baseband frequency range thereby improving the linearity and reducing the self-modulation response of the transistor, but that same inductance value will have more RF loss than a higher inductance value.

$$Z_L = \omega L = 2\pi f L$$ (4.1)

In this approach inductors of 1 $\mu$H (network A) and 10 nH (network B) will be connected to the CGH27015F transistor drain. Networks C and D will involve conical biasing inductors designed by CoilCraft [2] and Piconics [38] respectively for low RF loss over wide bandwidths, but those networks exhibit very high impedances at base band. The use of broadband conical inductors is common on modern microwave power amplifier designs [9].

In order to match the desired drain impedance of $Z_L = 13.45 + j6.5 \ \Omega$ it was decided to implement the match using a open stub that could be tuned for operation with each of the different inductor configurations. The design results shown here were recorded for the nominal case of Network A which also exhibited the furthest load impedance from the desired load impedance. The resulting optimized layout with block
capacitor and female SMA edge mounted connector with mechanical interface context is shown in Figure 4.15.

Given the circuit layout shown in Figure 4.15 the impedance presented to the drain of the CGH27015F transistor is reported in Figure 4.16. At the center frequency of 2.2 GHz Network A presents $Z_{L,A} = 10.75 - j10.57 \ \Omega$ compared to the target $Z_L = 13.45 + j6.5 \ \Omega$. Despite the difference from the target impedance from the results reported in Figure 4.8 we can see that the output power will be similar while the PAE of the device is degraded by 12 percentage points.

The network shown in Figure 4.15 was simulated in the Keysight ADS EM planar 2.5D solver with the input matching network developed in Section 4.5. The resulting output power response for the first and third
harmonic tones as a function of input power are shown in Figure 4.17. We can see that, as expected from load-pull analysis, the output power 1dB compression point occurs at approximately 41 dBm of output power for 16 dBm to 17 dBm of input power. This curve results in the large signal gain and gain compression reported in Figure 4.18. From these simulation results we can see a very clear 1 dB gain expansion with some "ripple" that occurs between 20 dBm and 40 dBm which is indicative of an IMD3 "sweet spot" as described in Section 2.2. We can also see that the transistor exhibits between 11.5 dB and 12.5 dB of large signal gain which is in line with the expected response of the network given the impedance presented by the network shown in Figure 4.16.
The last concern for this network implementation is having a model for the expected dc drain current draw and associated drain and power added efficiency. The simulated drain current draw for a given output power is shown in Figure 4.19. Based on these results the device will draw around 900 mA at the 1 dB compression point, a result that is consistent with the dc IV curve reported in Figure 4.2. Another key result of this simulation is that the device is expected to draw a minimum of 100 mA of current for output powers lower than 20 dBm. Using these results the drain efficiency and power added efficiency can be found as reported in Figure 4.20. As expected from the load-pull previously conducted and the modelled drain impedance found in Figure 4.16 the PAE peaks at approximately 57% and an output power of 41 dBm.

Based on the results presented above the network laid out in Figure 4.15 was fabricated on 20 mil thick
4.7.1b Network E Special Considerations

Network E involves the use of a “resonating” drain bias that reduces the inductance value of an inductor bias while maintaining the RF loss performance by placing a capacitor in parallel with the inductor such that the two elements resonate at the fundamental RF frequency [39] [40]. This network can be implemented identically to networks A through D as described above.

Rogers 4350b with LPKF equipment available to the RFPAL. The resulting network as integrated can be seen in Figure 4.21.

Figure 4.19: Network A drain current dc component at 2.2 GHz as a function of input power.

Figure 4.20: Network A power added efficiency at 2.2 GHz as a function of input power.
The next network under test to consider is Network F which is biased through a 50Ω λ/4 transmission line. In this approach a transmission line that is a quarter wavelength long is connected to the CGH27015F transistor drain. The other end of the line is then shorted at the fundamental using bypass capacitors such that an open circuit is presented at the transistor drain and, ideally, no RF power is lost down the bias path. As the RF short is realized using capacitors the DC bias can be freely applied at the shorted end of the transmission line. This bias technique is incredibly common on modern microwave power amplifier designs.
due to its simplicity and low RF loss [9].

In order to match the desired drain impedance of $Z_L = 13.45 + j6.5 \, \Omega$ it was decided to implement the match using a transmission line with $Z_0 = 13.45 \, \Omega$ that is linearly tapered to $Z_0 = 50 \, \Omega$ while using transmission line offsets to cancel the reactive part of the load. The quarter wave long bias line will be introduced at an approximately five millimeter offset from the CGH27015F drain to ensure that it does not interfere with the mechanical interface discussed in Section 4.2. The resulting optimized layout with block capacitor and female SMA edge mounted connector with mechanical interface context is shown in Figure 4.22.

![Figure 4.22: Network F Layout](image)

Given the circuit layout shown in Figure 4.22 the impedance presented to the drain of the CGH27015F transistor is reported in Figure 4.23. At the center frequency of 2.2 GHz Network F presents $Z_{L,F} = 15.08 + j10.12 \, \Omega$ compared to the target $Z_L = 13.45 + j6.5 \, \Omega$. Despite the difference from the target impedance from the results reported in Figure 4.8 we can see that the output power will be similar while the PAE of the device is degraded by 5 percentage points.
Figure 4.23: Network F (a) real impedance and (b) imaginary impedance at CGH27015F transistor drain over the frequency range of interest.

The network shown in Figure 4.22 was simulated in the Keysight ADS EM planar 2.5D solver with the input matching network developed in Section 4.5. The resulting output power response for the first and third harmonic tones as a function of input power are shown in Figure 4.24. We can see that, as expected from load-pull analysis, the output power 1dB compression point occurs at approximately 41 dBm of output power for 16 dBm to 17 dBm of input power. This curve results in the large signal gain and gain compression reported in Figure 4.25. From these simulation results we can see a very clear 1 dB gain expansion that occurs between 25 dBm and 40 dBm which is indicative of an IMD3 "sweet spot" as described in Section 2.2. We can also see that the transistor exhibits between 13.5 dB and 14.5 dB of large signal gain which is
in line with the expected response of the network given the impedance presented by the network shown in Figure 4.23.

Figure 4.24: Network F output power at 2.2 GHz as a function of input power.

Figure 4.25: Network F large signal gain and gain compression at 2.2 GHz as a function of input power.

The last concern for this network implementation is having a model for the expected dc drain current draw and associated drain and power added efficiency. The simulated drain current draw for a given output power is shown in Figure 4.26. Based on these results the device will draw around 650 mA at the 1 dB compression point, a result that is consistent with the dc IV curve reported in Figure 4.2. Another key result of this simulation is that the device is expected to draw a minimum of 50 mA of current for output powers lower than 20 dBm. Using these results the drain efficiency and power added efficiency can be found.
as reported in Figure 4.27. As expected from the load-pull previously conducted and the modelled drain impedance found in Figure 4.23 the PAE peaks at approximately 70% and an output power of 41 dBm.

Based on the results presented above the network laid out in Figure 4.22 was fabricated on 20 mil thick Rogers 4350b with LPKF equipment available to the RFPAL. The resulting network as integrated can be seen in Figure 4.28.
4.7.3 Network G: 30Ω λ/4 Line Design

The next network under test to consider is Network G which is biased through a 30Ω λ/4 transmission line. In comparison with network F this network is characterized by a smaller characteristic impedance. The smaller characteristic impedance means that the inductance of the line will be smaller than that of network F. Given the theory behind self-modulation presented in Chapter 3 and we would expect this network to have lower self-modulation than network F as the characteristic impedance of a transmission line varies as Equation 4.2.

\[ Z_0 \propto \sqrt{\frac{L}{C}} \]  

In order to match the desired drain impedance of \( Z_L = 13.45 + j6.5 \, \Omega \) it was decided to implement the match using a transmission line with \( Z_0 = 13.45 \, \Omega \) that is linearly tapered to \( Z_0 = 50 \, \Omega \) while using transmission line offsets to cancel the reactive part of the load just as in Network F. The quarter wave long bias line will be introduced at an approximately five millimeter offset from the CGH27015F drain to ensure that it does not interfere with the mechanical interface discussed in Section 4.2. The resulting optimized layout with block capacitor and female SMA edge mounted connector with mechanical interface context is
shown in Figure 4.29.

![Network G Layout](image)

Figure 4.29: Network G Layout

Given the circuit layout shown in Figure 4.29 the impedance presented to the drain of the CGH27015F transistor is reported in Figure 4.30. At the center frequency of 2.2 GHz Network F presents $Z_{L,G} = 15.18 + j6.24 \ \Omega$ compared to the target $Z_L = 13.45 + j6.5 \ \Omega$. Despite the difference from the target impedance from the results reported in Figure 4.8 we can see that the output power will be similar while the PAE of the device is degraded by 2 percentage points.

The network shown in Figure 4.29 was simulated in the Keysight ADS EM planar 2.5D solver with the input matching network developed in Section 4.5. The resulting output power response for the first and third harmonic tones as a function of input power are shown in Figure 4.31. We can see that, as expected from load-pull analysis, the output power 1dB compression point occurs at approximately 41 dBm of output power for 25 dBm of input power. This curve results in the large signal gain and gain compression reported in Figure 4.25. From these simulation results we can see a very clear 0.5 dB gain expansion that occurs between 25 dBm and 40 dBm which is indicative of an IMD3 "sweet spot" as described in Section 2.2. We can also see that the transistor exhibits between 13.5 dB and 14 dB of large signal gain which is in line with
Figure 4.30: Network G (a) real impedance and (b) imaginary impedance at CGH27015F transistor drain over the frequency range of interest.

the expected response of the network given the impedance presented by the network shown in Figure 4.30.

The last concern for this network implementation is having a model for the expected dc drain current draw and associated drain and power added efficiency. The simulated drain current draw for a given output power is shown in Figure 4.33. Based on these results the device will draw around 800 mA at the 1 dB compression point, a result that is consistent with the dc IV curve reported in Figure 4.2. Another key result of this simulation is that the device is expected to draw a minimum of 100 mA of current for output powers lower than 15 dBm. Using these results the drain efficiency and power added efficiency can be found as reported in Figure 4.34. As expected from the load-pull previously conducted and the modelled drain
impedance found in Figure 4.30 the PAE peaks at approximately 60\% and an output power of 42 dBm.

Based on the results presented above the network laid out in Figure 4.29 was fabricated on 20 mil thick Rogers 4350b with LPKF equipment available to the RFPAL. The resulting network as integrated can be seen in Figure 4.35.

4.7.4 Network H: 50Ω Shorted Stub Design

The next network under test to consider is Network H which is biased through a 50Ω shorted "stub" transmission line. In this approach a transmission line matching network composed of a series line section and a parallel shorted "stub" is used to match the CGH27015F transistor drain to 50 Ω [9]. As in the quarter
wavelength line an appropriate RF short at the fundamental is realized using bypass capacitors such that an open circuit is presented at the transistor drain and, ideally, no RF power is lost down the bias path. As the RF short is realized using capacitors the DC bias can be freely applied at the shorted end of the transmission line. In order to match the desired drain impedance of $Z_L = 13.45 + j6.5 \, \Omega$ a single shorted stub was implemented. The resulting optimized layout with block capacitor and female SMA edge mounted connector with mechanical interface context is shown in Figure 4.36.

Given the circuit layout shown in Figure 4.36 the impedance presented to the drain of the CGH27015F transistor is reported in Figure 4.37. At the center frequency of 2.2 GHz Network F presents $Z_{L,H} = 15.02 + j10.41 \, \Omega$ compared to the target $Z_L = 13.45 + j6.5 \, \Omega$. Despite the difference from the target
impedance from the results reported in Figure 4.8 we can see that the output power will be similar while the PAE of the device is degraded by 7 percentage points.

The network shown in Figure 4.36 was simulated in the Keysight ADS EM planar 2.5D solver with the input matching network developed in Section 4.5. The resulting output power response for the first and third harmonic tones as a function of input power are shown in Figure 4.38. We can see that, as expected from load-pull analysis, the output power 1dB compression point occurs at approximately 40 dBm of output power for 25 dBm of input power. This curve results in the large signal gain and gain compression reported in
Figure 4.37: Network H (a) real impedance and (b) imaginary impedance at CGH27015F transistor drain over the frequency range of interest.

Figure 4.39. From these simulation results we can see a very clear 1 dB gain expansion that occurs between 25 dBm and 40 dBm which is indicative of an IMD3 "sweet spot" as described in Section 2.2. We can also see that the transistor exhibits between 13.5 dB and 14.5 dB of large signal gain which is in line with the expected response of the network given the impedance presented by the network shown in Figure 4.37.

The last concern for this network implementation is having a model for the expected dc drain current draw and associated drain and power added efficiency. The simulated drain current draw for a given output power is shown in Figure 4.40. Based on these results the device will draw around 650 mA at the 1 dB compression point, a result that is consistent with the dc IV curve reported in Figure 4.2. Another key
result of this simulation is that the device is expected to draw a minimum of 75 mA of current for output powers lower than 25 dBm. Using these results the drain efficiency and power added efficiency can be found as reported in Figure 4.41. As expected from the load-pull previously conducted and the modelled drain impedance found in Figure 4.37 the PAE peaks at approximately 65% and an output power of 41 dBm.

Based on the results presented above the network laid out in Figure 4.36 was fabricated on 20 mil thick Rogers 4350b with LPKF equipment available to the RFPAL. The resulting network as integrated can be seen in Figure 4.42.
Figure 4.40: Network H drain current dc component at 2.2 GHz as a function of input power.

Figure 4.41: Network H power added efficiency at 2.2 GHz as a function of input power.

Figure 4.42: Networks H layout as fabricated on 20mil thick Rogers 4350b in the amplifier with the common λ/4 line based input matching network.
4.7.5 Network I: 30Ω Shorted Stub Design

The next network under test to consider is Network H which is biased through a 30 Ω shorted "stub" transmission line. As with network G the lower characteristic impedance will have lower inductance than network G due to Equation 4.2. In order to match the desired drain impedance of $Z_L = 13.45 + j6.5 \, \Omega$ a single shorted stub was implemented. The resulting optimized layout with block capacitor and female SMA edge mounted connector with mechanical interface context is shown in Figure 4.43.

![Figure 4.43: Network I Layout](image)

Given the circuit layout shown in Figure 4.43 the impedance presented to the drain of the CGH27015F transistor is reported in Figure 4.44. At the center frequency of 2.2 GHz Network F presents $Z_{L,I} = 15.02 + j9.8 \, \Omega$ compared to the target $Z_L = 13.45 + j6.5 \, \Omega$. Despite the difference from the target impedance from the results reported in Figure 4.8 we can see that the output power will be similar while the PAE of the device is similar.

The network shown in Figure 4.43 was simulated in the Keysight ADS EM planar 2.5D solver with the input matching network developed in Section 4.5. The resulting output power response for the first and third harmonic tones as a function of input power are shown in Figure 4.45. We can see that, as expected from load-pull analysis, the output power 1dB compression point occurs at approximately 38 dBm of output power for 25 dBm of input power. This curve results in the large signal gain and gain compression reported in Figure 4.46. From these simulation results we can see a very clear 1 dB gain expansion that occurs between 25 dBm and 40 dBm which is indicative of an IMD3 "sweet spot" as described in Section 2.2. We can also
see that the transistor exhibits between 13.5 dB and 14.5 dB of large signal gain which is in line with the expected response of the network given the impedance presented by the network shown in Figure 4.44.

The last concern for this network implementation is having a model for the expected dc drain current draw and associated drain and power added efficiency. The simulated drain current draw for a given output power is shown in Figure 4.47. Based on these results the device will draw around 650 mA at the 1 dB compression point, a result that is consistent with the dc IV curve reported in Figure 4.2. Another key result of this simulation is that the device is expected to draw a minimum of 50 mA of current for output powers lower than 20 dBm. Using these results the drain efficiency and power added efficiency can be found.
as reported in Figure 4.27. As expected from the load-pull previously conducted and the modelled drain impedance found in Figure 4.44 the PAE peaks at approximately 70% and an output power of 41 dBm.

Based on the results presented above the network laid out in Figure 4.43 was fabricated on 20 mil thick Rogers 4350b with LPKF equipment available to the RFPAL. The resulting network as integrated can be seen in Figure 4.49.
Figure 4.47: Network I drain current dc component at 2.2 GHz as a function of input power.

Figure 4.48: Network F power added efficiency at 2.2 GHz as a function of input power.
Figure 4.49: Network I layout as fabricated on 20mil thick Rogers 4350b in the amplifier with the common λ/4 line based input matching network.
CHAPTER 5

TESTING PROCESS AND METHODOLOGY

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5.1 TESTING REQUIREMENTS

The PA's under test will require four key testing capabilities: generation and measurement of single tone (CW) signals, two-tone signals, complex real signal waveforms, and measurement of transistor drain voltage and current waveforms. In order to realize this testing capability a test bench was laid out that would be capable of meeting all of the above capabilities in four separate test configurations.

The PAs will be tested under CW excitation in order to verify the simulated output power, input power, gain, and efficiency results found in Chapter 4. This first order verification will ensure the amplifier design is accurate. This verification will entail the determination of the amplifier output power, gain, drain efficiency, and power added efficiency over a range of input powers, frequencies and bias points. Determination of these parameters drives the CW testing requirements enumerated below.

**CW Testing Requirements:**

1. Measure the output power of a single CW tone at a variable, specified frequency (2 GHz - 2.5 GHz)

2. Apply a desired single CW tone at a variable, specified frequency (2 GHz - 2.5 GHz) with a variable, specified power (up to 36 dBm)

3. Apply a variable, specified drain voltage (28 V, 30 W)

4. Measure the dc component of the drain voltage (28 V, 30 W)

5. Apply a variable, specified gate voltage (2.5 V - 3.5 V, 5 W)

6. Measure the dc component of the gate voltage (-2 V - -5 V, 5 W)

After the CW test procedures have been completed and the resulting amplifier performance has been calculated two-tone testing can begin. Two-tone testing will allow the nonlinear effects discussed in Chapter 2 to be quantitatively assessed in a controlled measurement environment. In order to verify the results presented in Chapter 2 the power of each fundamental frequency tone and the power of each third order intermodulation tone will need to be computed so that the amplifier output power, gain, drain efficiency,
power added efficiency, and intermodulation ratio (IMR3) over a range of input powers, fundamental tone spacings, and center frequencies. Determination of these parameters drives the two tone testing requirements enumerated below.

Two Tone Testing Requirements:

(1) Measure the output power of two fundamental output tones and two intermodulation product tones at variable, specified frequencies (2 GHz - 2.5 GHz)

(2) Apply a desired pair of signals tones at a variable, specified center frequency (2 GHz - 2.5 GHz) with variable, specified spacing with a variable, specified identical power (up to 36 dBm)

(3) Apply a variable, specified drain voltage (28 V, 30 W)

(4) Measure the dc component of the drain voltage (28 V, 30 W)

(5) Apply a variable, specified gate voltage (2.5 V - 3.5 V, 5 W)

(6) Measure the dc component of the gate voltage (-2 V - -5 V, 5 W)

In order to verify the self-modulation effects described in Chapter 3 the instantaneous drain voltage and current waveforms will need to be evaluated under two tone excitation. In order to verify the results presented in Chapter 3 the power of each fundamental frequency tone and the power of each third order intermodulation tone will need to be computed so that the amplifier output power, gain, drain efficiency, power added efficiency, intermodulation ratio (IMR3), instantaneous drain voltage, and instantaneous drain current over a range of input powers, fundamental tone spacings, and center frequencies. Determination of these parameters drives the drain waveform testing requirements enumerated below.

Drain Waveform Measurement Testing Requirements:

(1) Measure the output power of two fundamental output tones and two intermodulation product tones at variable, specified frequencies (2 GHz - 2.5 GHz)
(2) Apply a desired pair of signals tones at a variable, specified center frequency (2 GHz - 2.5 GHz) with variable, specified spacing with a variable, specified identical power (up to 36 dBm)

(3) Apply a variable, specified drain voltage (28 V, 30 W)

(4) Measure the dc component of the drain voltage (28 V, 30 W)

(5) Apply a variable, specified gate voltage (2.5 V - 3.5 V, 5 W)

(6) Measure the dc component of the gate voltage (-2 V - -5 V, 5 W)

(7) Measure the instantaneous voltage at the drain terminal of the CGH27015F transistor

(8) Measure the instantaneous current to the drain terminal of the CGH27015F transistor

Once the full range of CW and two tone tests have been completed the next step is to pass a real communications signal through the PA to determine how it would perform in practice when the simple two tone waveform is replaced by a complicated waveform. In order to determine the performance of the amplifier the adjacent channel power ratio (ACPR) will be measured along with the amplifier drain efficiency and PAE. Determination of these parameters drives the complex modulation testing requirements enumerated below.

Complex Modulation Testing Requirements:

(1) Measure the ACPR of a specified complex modulation signal (2 GHz - 2.5 GHz)

(2) Generate a specified complex modulation signal (2 GHz - 2.5 GHz)

(3) Apply a variable, specified drain voltage (28V, 30W)

(4) Measure the dc component of the drain voltage (28V, 30W)

(5) Apply a variable, specified gate voltage (2.5V - 3.5V, 5W)

(6) Measure the dc component of the gate voltage (-2 V - -5 V, 5 W)
5.2 POWER AMPLIFIER MEASUREMENT TEST BENCH

5.2.1 TEST PROCEDURE FLOW

In order to meet the above requirements for each of the four tests to characterize the device under test (DUT) we will sweep the center frequency of operation, tone spacing (if a two tone test), $V_{DD}$, $V_{GG}$, and $P_{in}$ at the DUT input plane. A test bench was developed such that each core test could be conducted with a standard set of equipment and calibrations over those sweep parameters. The automated measurement process for the CW and two tone measurements is described in Figure 5.1. The majority of test steps are common between CW and two tone testing with only one additional step associated with measuring the tone power of each intermodulation product. When the drain waveform measurements are made an additional test step is introduced to the two tone testing process.

In general the process described in Figure 5.1 can be broken down into three general phases, a "setup" phase, a "sweep and measure" phase, and a "clean up" phase. The "setup" phase includes the configuration, calibration, and biasing the device under test (DUT) steps. The configuration step involves connecting the control computer to each piece of the test equipment and setting the initial test values. The calibration step involves either loading a pre-measured set of calibration data or running the calibration routines discussed in Section 5.4. The biasing DUT step involves biasing up the CGH27015F transistor safely to its initial bias point under test.

In the "sweep and measure" phase the measure dc power, measure fundamental frequency power, measure intermodulation products, and measure drain waveform steps are conducted. Each of these steps is conducted as part of a nested set of sweeps that are a function of the center frequency ($F_0$), difference frequency ($F_{diff}$ if testing a two tone signal), drain-to-source voltage ($V_{DS}$), gate-to-source voltage ($V_{GS}$), and input power ($P_{in}$). In the measure dc power step the voltage and currents being supplied to both the gate and the drain are measured so that the instantaneous power draw from both supplies can be calculated as $P_{dc} = V_{DS}I_D + V_{GS}I_G$ where $V_{DS}$, $V_{GS}$, $I_D$, and $I_G$ are all the dc components of those waveforms. In the measure fundamental frequency power step the power of the CW tone or each of the fundamental two tone signals will be
Figure 5.1: Process Flowchart for common amplifier characterization test bench capable of making CW, two tone, and drain waveform measurements. Two tone testing and drain waveform measurement tests require unique steps not present in CW testing.

determined. In the measure intermodulation products step the power of each of the third order modulation products will be determined if a two tone test is being conducted. Finally the measure drain waveforms step involves measuring the instantaneous drain voltage and current waveforms under two tone excitation and will only be conducted for some two tone measurements.

In the "cleanup" phase the bias off DUT, safe test equipment, and calculate results steps will be taken
before the final results of the test are displayed and recorded. In the bias off DUT step RF excitation power will be turned off and the CGH27015F amplifier will be biased down into pinch-off before the power supplies are turned off. In the safe test equipment step all test equipment default values (such that a device accidentally turning on will not damage the DUT or other equipment) will be set and the control computer will relinquish control over all instruments. Finally in the calculate results stage the resulting data will have the calibration applied to it to determine the previously described performance criteria of the amplifier before the results are displayed and saved.

In order to implement the described test bench flow a MATLAB scripting approach was used to automate the testing process. MATLAB was selected as the implementation language of this project as it has native GPIB connection support (a communication protocol available to all test equipment in our lab except our oscilloscope). In order to make the testing process as easy and flexible as possible a series of MATLAB "wrapper" functions were developed. These "wrapper" functions encapsulate a GPIB command to an instrument in a MATLAB-style function that allows commanding of either a single action (e.g. change frequency response of equipment, power levels, etc.) or a more complicated procedure (e.g. instrument setup, generate two-tones of a given frequency spacing, etc.). The usage of these scripts will be discussed in detail in the following sections.

5.2.2 Bench Overview

Based on the process flow described in Figure 5.1 and the test equipment already available the test bench was laid out according to the block diagram shown in Figure 5.2 as shown in Figure 5.3. This system as laid out is capable of conducting all four categories of test measurements without significant modification using a common calibration process. This configuration is unique for a two tone capable test bench as it uses a single vector signal generator (VSG) and driver amplifier for both tones while conventional test benches have separate input chains for each tones [41]. Normally this is done either because the VSG is incapable of generating two tones without introducing large amounts of noise or because the driver amplifiers provide significant IMD3 products of their own. In this configuration the SMJ100A vector signal generator (VSG) is used to generate a two tone signal using the process defined in Section 5.3 which is then amplified by
a ZHL-16W-43+ driver amplifier that was selected because it has low IMD3 products at the desired input power levels. At the output the FSQ26 vector signal analyzer (VSA) is used to measure the output power at each fundamental tone and intermodulation product. Power to the DUT is provided by the N6705A power supply which is capable of measuring the dc component of both voltages and currents for each of its supplies. When dynamic measurement of the drain voltage and current waveforms is desired a Tektronix DPO2024 oscilloscope with a voltage probe connected to channel 1 and a TCP0030 clamp current probe connected to channel 2 will be used. In Sections 5.2.3-5.2.9 the selection criteria and usage of each instrument will be discussed in more detail. The two-tone signal generated by the SMJ100A is discussed in Section 5.3, the calibration process for this bench is discussed in Section 5.4, and the MATLAB scripts can be found in Appendix B.

![Test bench block diagram as implemented. All test equipment (except the Oscilloscope) is connected in series via GPIB connectors to allow commands and measurements to be implemented through MATLAB.](image)

5.2.3 Vector Signal Generator

In the Radio Frequency Power and Analog Laboratory (RFPAL) I had access to a Rohde & Schwarz SMJ100A vector signal generator (VSG) capable of generating complex RF waveforms based on IQ signals as
well as some real complex communications signals suitable for ACPR testing. This instrument is capable of generating signals with up to 100 MHz instantaneous bandwidth based on an uploaded IQ waveform defined in a ".wav" file that can be generated in any number of software packages [42]. Given that this instrument is capable of generating a CW, two-tone, or complex modulation signal signal that it is linear at the output and is capable of operating within the frequency range of interest it was selected as the single-source VSG for the test bench. A detailed explanation of how to set the SMJ100A to generate a linear two-tone signal is given in Section 5.3. The instrument has built-in settings for complex modulation signals commonly found in communications [42].

5.2.4 Driver Amplifier

In order to prevent the VSG from distorting the output two-tones due to issues with the high output power needed at the DUT input plane a driver amplifier is used to increase the output power. The SMJ100A has highly linear output frequency response for RF output power under 0 dBm, so at all frequencies of interest
a good Driver amplifier should have greater than 40dB of gain with IMD products that are ideally lower than the noise floor of the test system. For this bench the ZHL-16W-43+ amplifier was selected for its preexisting presence in the laboratory, high dynamic range, high output power range (up to fifteen watts in linear operation), and high gain (40 dB typical) [43]. Given that this amplifier works within the frequency band of interest it was selected as the common bench driver amplifier. It has previously been packaged in an enclosure that uses a wall power plug for operation which removed the potential need for a potential third and/or fourth power supplies to be present in the test setup.

5.2.5 Vector Signal Analyzer

A Rohde & Schwarz FSQ26 vector signal analyzer (VSA) was selected as the output power sensor for spectrum analysis. This particular piece of equipment was selected due to its ease of use and preexisting presence in the RFPAL and ability to measure the ACPR of complex modulated signals [44].

5.2.6 Output Attenuator

The output attenuator is present to avoid saturating the FSQ26 due to the high output power of the DUT. The FSQ26 has a maximum input power rating of 30dBm [44] which means that given the 41dBm expected output power of the DUT a minimum of 10dB of attenuation is required. In order to ensure the safety of the FSQ26 a total attenuation of around 40 dB was selected to ensure no more than one milliwatt of power is incident on the FSQ26 input. The exact value of this attenuation does not need to be precisely controlled as it will be calibrated out as described in Section 5.4. A Pasternack PE7393-20 20dB attenuator and two Pasternack PE7016-10 10dB attenuators were used in this test configuration.

5.2.7 DUT Power Supply

In order to sweep $V_{DD}$ and $V_{GG}$ of the DUT the bench needs two command-able power supplies. For this test bench the N6705A dc power supply was chosen for its GPIB controllability, preexisting presence in the RFPAL, and integrated four supply output. All connections between the DUT and the N6705A were made with twisted-pair connections to minimize RF interference from outside sources that could perturb the
5.2.8 **Power Meter and Power Sensor**

A Hewlett Packard E4419B power meter and associated Hewlett Packard E9300A power sensor were selected as the power sensor calibration reference for the test bench. These pieces of test equipment were selected because they were already present in the RFPAL and have a dynamic range of -60 to +20 dBm (well within the range of potential powers).

5.2.9 **Oscilloscope**

A Tektronix DPO2024 oscilloscope was selected as the drain waveform measurement tool due to its presence in the lab, proven track record measuring the drain waveforms of other PAs, and its high bandwidth and sampling rate (500MHz and 1GS/s). Unfortunately this instrument is not GPIB command-able and as such measurement of the drain voltage and current waveforms had to be conducted manually separate from the main two tone measurement sweep.

5.3 **Complex IQ Signal Generation with R&S SMJ100A VSG**

Conventional two-tone tests are conducted with two signal sources that are separately generated and amplified before being summed at the input plane of the DUT [14]. In order to simplify the test configuration I choose instead to implement the two-tone generation with a single vector signal generator. The distortion products generated by the driver amplifier are calibrated out using the procedure described in Section 5.4.2. The SMJ100A vector signal generator used in this bench is capable of generating arbitrary waveforms based on a given set of I-Q signal pairs generated externally. In this section we describe the process by which the I-Q pairs are generated for the SMJ100A.

First we define the spectral windowing of the SMJ100A that we desire. The goal of our system is to generate two equal amplitude tones spaced $F_{\text{diff}}$ apart. We thus define the two tones at the RF output as in the below equations 5.1 and 5.2.
\[ F_1 = F_o - \frac{F_{diff}}{2} \quad (5.1) \]
\[ F_2 = F_o + \frac{F_{diff}}{2} \quad (5.2) \]

In order to ensure the tones are implemented without distortion at the RF output we need to offset the tones in baseband such that all waveform values are real. To accomplish this we redefine \( F_1 \) and \( F_2 \) as in the below equations 5.3 and 5.4. This new definition will allow us to implement the correct tones at the RF output without distortion due to the arbitrary wave generator.

\[ F_1 = 1 \text{MHz} \quad (5.3) \]
\[ F_2 = F_1 + F_{diff} \quad (5.4) \]

With the tones redefined for baseband we need to set the clock rate for the arbitrary wave generator. We determine the clock rate \( F_{sample} \) by multiplying the highest frequency tone \( F_2 \) by an oversampling factor as in the below equation 5.5.

\[ F_{sample} = F_2 \times OS \quad (5.5) \]

In order to correctly configure the arbitrary waveform generator for the two-tone signal in baseband we now need to determine the discrete sampling values that can be used to generate the I-Q pairs. The total number of samples is given by equation 5.6.

\[ N_{samples} = \frac{F_{sample}}{F_1} \quad (5.6) \]

With the total number of samples determined it is now possible to map the sample matrix (\( k \) from 1 to \( N_{samples} \)) to the time domain as a function of \( F_{sample} \) as in the below equation 5.7.

\[ T = (\bar{k} - 1) \frac{1}{F_{sample}} \quad (5.7) \]
With a time domain form of the samples in baseband it is now possible to calculate the unnormalized I and Q waveforms in the time domain that map to the two tones at $F_1$ and $F_2$ as in the below equations 5.8 and 5.9.

\begin{align*}
    I &= \cos(2\pi F_1 r) + \cos(2\pi F_2 r) \\
    Q &= \sin(2\pi F_1 r) + \sin(2\pi F_2 r)
\end{align*}

Finally, the calculated I and Q waveforms are amplitude normalized as in equations 5.11 and 5.12.

\begin{align*}
    E_{\text{max}} &= \max \sqrt{I^2 + Q^2} \\
    I_{\text{norm}} &= \frac{I}{E_{\text{max}} \sqrt{2}} \\
    Q_{\text{norm}} &= \frac{Q}{E_{\text{max}} \sqrt{2}}
\end{align*}

The resulting I and Q waveforms can then be uploaded to the SMJ100A via GPIB with a SMJ100A center operating frequency of $F_o - (F_1 + \frac{F_{\text{diff}}}{2})$ to compensate for the baseband offsets present in the IQ signal waveform.

With the process for computing the two tone waveform IQ signals needed to use the SMJ100A it is now critical that for the tone spacings’ under consideration the waveform spectral content is equivalent. The minimum oversampling rate needed to produce clean two tone excitations was determined experimentally to be 5X. Given the 100MHz video bandwidth of the SMJ100A this means the widest two tone spacing the SMJ100A is capable of generating is 20 MHz. For the purposes of the testing conducted tone spacings of 5 MHz, 10 MHz, and 20 MHz were considered.

A 5 MHz two tone separation was computed on the assumption of an oversampling rate of 5X (to have consistent oversampling with the 20 MHz case) using the procedure outlined above. This results in the signal parameters outlined in Table 5.1. The resulting IQ waveforms and output spectrum are visualized in Figure 5.4.
### Table 5.1: Signal parameters for 5 MHz separated two tone signal.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock Rate</td>
<td>24 MHz</td>
</tr>
<tr>
<td>Signal Duration</td>
<td>$10^{-6}$ sec</td>
</tr>
<tr>
<td>Samples</td>
<td>24</td>
</tr>
<tr>
<td>Peak Level</td>
<td>1</td>
</tr>
<tr>
<td>Peak Envelope Level</td>
<td>0.70711</td>
</tr>
<tr>
<td>Peak to average power ratio</td>
<td>3.0103</td>
</tr>
</tbody>
</table>

Figure 5.4: 5 MHz two tone IQ waveform amplitude in time (top), output spectrum (bottom left), and in the IQ plane (bottom right).

A 10 MHz two tone separation was computed on the assumption of an oversampling rate of 5X (to have consistent oversampling with the 20 MHz case) using the procedure outlined above. This results in the signal parameters outlined in Table 5.2. The resulting IQ waveforms and output spectrum are visualized in Figure 5.5.
A 20 MHz two tone separation was computed on the assumption of an oversampling rate of 5X (the maximum possible given the SMJ100A’s video bandwidth of 100 MHz) using the procedure outlined above. This results in the signal parameters outlined in Table 5.3. The resulting IQ waveforms and output spectrum are visualized in Figure 5.6.

![Figure 5.5: 10 MHz two tone IQ waveform amplitude in time (top), output spectrum (bottom left), and in the IQ plane (bottom right).](image)

**Table 5.2: Signal parameters for 10 MHz separated two tone signal.**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock Rate</td>
<td>44 MHz</td>
</tr>
<tr>
<td>Signal Duration</td>
<td>$10^{-6}$ sec</td>
</tr>
<tr>
<td>Samples</td>
<td>44</td>
</tr>
<tr>
<td>Peak Level</td>
<td>1</td>
</tr>
<tr>
<td>Peak Envelope Level</td>
<td>0.70711</td>
</tr>
<tr>
<td>Peak to average power ratio</td>
<td>3.0103</td>
</tr>
</tbody>
</table>
Table 5.3: Signal parameters for 20 MHz separated two tone signal.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock Rate</td>
<td>84 MHz</td>
</tr>
<tr>
<td>Signal Duration</td>
<td>$10^{-6}$ sec</td>
</tr>
<tr>
<td>Samples</td>
<td>84</td>
</tr>
<tr>
<td>Peak Level</td>
<td>1</td>
</tr>
<tr>
<td>Peak Envelope Level</td>
<td>0.70711</td>
</tr>
<tr>
<td>Peak to average power ratio</td>
<td>3.0103</td>
</tr>
</tbody>
</table>

Figure 5.6: 20 MHz two tone IQ waveform amplitude in time (top), output spectrum (bottom left), and in the IQ plane (bottom right). The two-tone IQ waveform becomes double valued due to the low oversampling rate at this frequency. The 20 MHz separated tones can provide stability issues in the full network, but the waveform through the driver amplifier is stable.

5.4 Calibration Procedure

In order to calibrate this test setup so that a known input power can be applied to the DUT and an accurate output power can be measured the loss of cables, connections, attenuation values, and driver gain must be determined. To accomplish this task the input attenuation and cable losses will be determined using the
SMJ100A and FSQ26 instruments. With the passive components characterized we calibrate the SMJ100A and associated driver amplifier to provide the desired $P_{in}$ at the input plane of the DUT. For the proposed test bench this will involve determining the losses of the output cable and attenuators and then calibrating out the input power applied to the DUT.

In Section 5.4.1 the process for determining the dB offsets of the output cable, output attenuators, and VSA will be discussed. In Section 5.4.2 these offset values will be used to calibrate the $P_{in}$ to the DUT.

5.4.1 Determination of Attenuator and FSQ26 Offsets

In this setup I start by connecting the output attenuator directly to the E9300A power sensor as in Figure ???. This measurement results in a dB offset for attenuator given a known input power of the VSG. This allows the computation of an offset that can be sued to reference the FSQ26 result back to the power meter measurement plane to ensure bench traceability to a single known-good measurement instrument. This calibration will be conducted for the total system of the output cable and output attenuator chains. This calibration measurement will be conducted under CW excitation at each frequency where the tone power will be measured.

![Diagram](image)

Figure 5.7: E4419B power meter calibration bench setup. The output attenuator should be connected to the VSG cable with a female-female SMA barrel.

We now calibrate the attenuators with the FSQ26 by measuring the attenuation of the FSQ26 cable and output attenuators with the FSQ26. This measurement is conducted by connecting the SMJ100A, FSQ26,
output attenuators, and FSQ26 cable as shown in Figure 5.8. In this configuration a CW tone at a desired frequency with a known power is applied to the output attenuator/FSQ26 cable system and the power of that tone is measured by the FSQ26 to determine the loss of those elements.

![Block diagram of calibration setup](image)

Figure 5.8: Output attenuator calibration block diagram. The attenuator interface cable to the DUT is connected directly to the SMJ100A such that the power incident on the attenuators is that of the SMJ100A.

The procedure described above was followed to find the actual attenuation of the three attenuator network. The resulting attenuation values including the FSQ26 power meter correction factor are shown in Figure 5.9. At most the attenuator network attenuates by 41 dB and at the least by 40.7 dB. These values are more than sufficient to ensure that the FSQ26 maximum input power limit of 30 dBm is not reached for the anticipated 41 dBm output power.

### 5.4.2 Input Power Plane Calibration

In order to run the sweeps as defined by the testing specifications discussed earlier in this chapter the applied power must be known at the DUT input plane such that we sweep input power per tone from 0 to 35 dBm. In order to do this we must introduce a driver amplifier to the test setup as previously described to meet the input power requirements and to avoid distortion that occurs in high power operation of the SMJ100A. In order to calibrate the overall system to provide the desired $P_{in}$ we connect the bench as shown in Figure 5.10. Based off the calibration steps conducted in Section 5.4.1 all elements beyond the Driver amplifier output are known as a function of frequency and power. With all of these attenuation values known the input power
can be determined. The output power of the SMJ100A is then iterated until the maximum power incident on
the DUT will be within 1 dBm of the 35 dBm target power.

The procedure described above was followed to find the actual power at the input plane of the DUT using
the attenuation values from Figure 5.9. The resulting power at the DUT input over SMJ100A excitation
power over the 2 GHz - 2.5 GHz frequency range in 100 MHz increments is shown in Figure 5.11. At most
the driver amplifier network applies 35.2 dBm and at least 34.4 dBm to the input of the DUT. These values
are more than sufficient to ensure that the DUT will be able to reach the anticipated 41 dBm output power.
Figure 5.10: Driver amplifier $P_{in}$ calibration bench setup. No additional connectors are necessary.
Figure 5.11: Driver amplifier measured output power incident at DUT input for a given SMJ100A output power under CW excitation.
Chapter 6

Discussion of Results

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6.1 **Overview of Networks and Analysis Process**

In Chapter 4 nine different biasing approaches embedded in five circuit layouts were developed with approximately equivalent first and second harmonic terminations. These networks were then fabricated on 20 mil thick Rogers 4350b substrate and subsequently tested. In this chapter the test results for Networks F through I will be discussed. In Section 6.7 the two-tone results for each network and associated self-modulation effects will be compared. The test procedure followed to generate the results provided here is described in Chapter 5. CW results for each of the networks presented can be found in Appendix C.

6.2 **Network A-E: Inductor Based Bias Design**

Due to issues of time Networks A through E could not be tested. The common network was fabricated as described in Section 4.7.1 and will be tested in future work.

6.3 **Network F: 50Ω, \(\lambda/4\) Line Results**

6.3.1 **Two-Tone Results**

The response of network F to a two-tone excitation was measured as a function of gate bias, center frequency, and tone spacings for gate biases between -3.5 V and -2.5 V, center frequencies between 2.1 GHz and 2.3 GHz, and tone spacings of 5 MHz, 10 MHz, and 20 MHz. For the sake of brevity only the results for a center frequency of 2.2 GHz (the designed center frequency) and gate bias of -3 V will be considered.

In Figure 6.1 the measured higher and lower fundamental and intermodulation products for a 5 MHz tone spacing is reported. From the reported results we can see that both higher and lower terms all follow a consistent pattern. The observed variance at low input power for the intermodulation terms is due to measurement error close to the analyzer noise floor.

In Figure 6.2 the measured higher and lower fundamental and intermodulation products for a 10 MHz tone spacing is reported. From the reported results we can see that both higher and lower terms all follow a
consistent pattern. The observed level IMD3 power at low input power for the intermodulation terms is due to measurement error close to the analyzer noise floor.

In Figure 6.3 the measured higher and lower fundamental and intermodulation products for a 20 MHz tone spacing is reported. From the reported results we can see that both higher and lower terms all follow a consistent pattern with the higher tone exhibiting a 2 dB to 3 dB increase in IMD3 power. The observed level IMD3 power at low input power for the intermodulation terms is due to measurement error close to the analyzer noise floor.
Figure 6.1: Network F: 5 MHz Tone spacing at -3V gate bias. Intermodulation terms are dashed lines.

Figure 6.2: Network F: 10 MHz Tone spacing at -3V gate bias. Intermodulation terms are dashed lines.

Figure 6.3: Network F: 20 MHz Tone spacing at -3V gate bias. Intermodulation terms are dashed lines.
### Table 6.1: Network F: measured ACPR Signal with 5 MHz bandwidth and 41 dBm PEP.

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<th>Mask Spacing</th>
<th>Lower Channel</th>
<th>Upper Channel</th>
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<tr>
<td>5 MHz</td>
<td>-27.80 dB</td>
<td>-25.70 dB</td>
</tr>
<tr>
<td>10 MHz</td>
<td>-44.87 dB</td>
<td>-44.92 dB</td>
</tr>
</tbody>
</table>

#### 6.3.2 Complex Modulated Waveform Results

In order to understand how this amplifier performs under a complex modulation scheme it was tested using a LTE EUTRA waveform with 5 MHz signal bandwidth. This signal was configured to have a 41 dBm peak envelope power (PEP) and 10 dB peak to average power ratio (PAPR). The resulting adjacent channel power ratio (ACPR) measurements for the two defined bands is shown in Table 6.1. The asymmetric response of the upper and lower 5 MHz mask are indicative of the baseband dependency observed at this bias point.

#### 6.4 Network G: 30Ω, λ/4 Line Results

##### 6.4.1 Two-Tone Results

The response of network G to a two-tone excitation was measured as a function of gate bias, center frequency, and tone spacing’s for gate biases between -3.5 V and -2.5 V, center frequencies between 2.1 GHz and 2.3 GHz, and tone spacing’s of 5 MHz, 10 MHz, and 20 MHz. For the sake of brevity only the results for a center frequency of 2.2 GHz (the designed center frequency) and gate bias of -3 V will be considered.

In Figure 6.4 the measured higher and lower fundamental and intermodulation products for a 5 MHz tone spacing is reported. From the reported results we can see that both higher and lower terms all follow a consistent pattern with an IMD3 "null" at 34 dBm input power and associated gain expansion of the fundamental tone powers. The observed variance at low input power for the intermodulation terms is due to measurement error close to the analyzer noise floor.

In Figure 6.5 the measured higher and lower fundamental and intermodulation products for a 10 MHz tone spacing is reported. From the reported results we can see that both higher and lower terms all follow
a consistent pattern with an IMD3 "null" at 34 dBm input power and associated gain expansion of the fundamental tone powers. The observed null is shallower than that for the 5 MHz tone spacing due to the higher baseband impedance presented at 10 MHz. The observed level IMD3 power at low input power for the intermodulation terms is due to measurement error close to the analyzer noise floor.

In Figure 6.6 the measured higher and lower fundamental and intermodulation products for a 20 MHz tone spacing is reported. From the reported results we can see that both higher and lower terms all follow a consistent pattern with the null in the IMD3 response almost completely removed. The gain expansion at 35 dBm of input tone power is still present. The observed level IMD3 power at low input power for the intermodulation terms is due to measurement error close to the analyzer noise floor.
Figure 6.4: Network G: 5 MHz Tone spacing at -3V gate bias. Intermodulation terms are dashed lines.

Figure 6.5: Network G: 10 MHz Tone spacing at -3V gate bias. Intermodulation terms are dashed lines.

Figure 6.6: Network G: 20 MHz Tone spacing at -3V gate bias. Intermodulation terms are dashed lines.
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<th>Upper Channel</th>
</tr>
</thead>
<tbody>
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<td>5 MHz</td>
<td>-27.48 dB</td>
<td>-25.70 dB</td>
</tr>
<tr>
<td>10 MHz</td>
<td>-43.80 dB</td>
<td>-44.92 dB</td>
</tr>
</tbody>
</table>

Table 6.2: Network G: measured ACPR Signal with 5 MHz bandwidth and 41 dBm PEP.

6.4.2 **Complex Modulated Waveform Results**

In order to understand how this amplifier performs under a complex modulation scheme it was tested using a LTE EUTRA waveform with 5 MHz signal bandwidth. This signal was configured to have a 41 dBm peak envelope power (PEP) and 10 dB peak to average power ratio (PAPR). The resulting adjacent channel power ratio (ACPR) measurements for the two defined bands is shown in Table 6.2. The asymmetric response of the upper and lower 5 MHz mask are indicative of the baseband dependency observed at this bias point.

6.5 **Network H: 50Ω Single Shorted Stub Match Results**

6.5.1 **Two-Tone Results**

The response of network H to a two-tone excitation was measured as a function of gate bias, center frequency, and tone spacing’s for gate biases between -3.5 V and -2.5 V, center frequencies between 2.1 GHz and 2.3 GHz, and tone spacing’s of 5 MHz, 10 MHz, and 20 MHz. For the sake of brevity only the results for a center frequency of 2.2 GHz (the designed center frequency) and gate bias of -3 V will be considered.

In Figure 6.7 the measured higher and lower fundamental and intermodulation products for a 5 MHz tone spacing is reported. From the reported results we can see that both higher and lower terms all follow a consistent pattern with an IMD3 "null" at 32 dBm input power and associated gain expansion of the fundamental tone powers. The observed variance at low input power for the intermodulation terms is due to measurement error close to the analyzer noise floor.

In Figure 6.8 the measured higher and lower fundamental and intermodulation products for a 10 MHz tone spacing is reported. From the reported results we can see that both higher and lower terms all follow a
consistent pattern. The drop in gain and IMD3 observed at 23 dBm is due to an intermittent stability problem excited at that tone power. After significant tuning I was unable to resolve this behavior. At 32 dBm there is an observed null that is shallower than that for the 5 MHz tone spacing. Unlike the network G case we cannot pin this shallower null on the baseband impedance due to the stability issues observed in this network.

In Figure 6.9 the measured higher and lower fundamental and intermodulation products for a 20 MHz tone spacing is reported. From the reported results we can see that both higher and lower terms all follow a consistent pattern with the null in the IMD3 response completely removed. In fact, the IMD3 "expands" in the transition region. The gain expansion at 35 dBm of input tone power is present. The observed level IMD3 power at low input power for the intermodulation terms is due to measurement error close to the analyzer noise floor.
Figure 6.7: Network H: 5 MHz Tone spacing at -3V gate bias. Intermodulation terms are dashed lines.

Figure 6.8: Network H: 10 MHz Tone spacing at -3V gate bias. Intermodulation terms are dashed lines.

Figure 6.9: Network H: 20 MHz Tone spacing at -3V gate bias. Intermodulation terms are dashed lines.
6.5.2 Complex Modulated Waveform Results

In order to understand how this amplifier performs under a complex modulation scheme it was tested using a LTE EUTRA waveform with 5 MHz signal bandwidth. This signal was configured to have a 41 dBm peak envelope power (PEP) and 10 dB peak to average power ratio (PAPR). The resulting adjacent channel power ratio (ACPR) measurements for the two defined bands is shown in Table 6.3. The asymmetric response of the upper and lower 5 MHz mask are indicative of the baseband dependency observed at this bias point.

6.6 Network I: 30Ω Single Shorted Stub Match Results

6.6.1 Two-Tone Results

The response of network I to a two-tone excitation was measured as a function of gate bias, center frequency, and tone spacing’s for gate biases between -3.5 V and -2.5 V, center frequencies between 2.1 GHz and 2.3 GHz, and tone spacing’s of 5 MHz, 10 MHz, and 20 MHz. For the sake of brevity only the results for a center frequency of 2.2 GHz (the designed center frequency) and gate bias of -3 V will be considered.

In Figure 6.10 the measured higher and lower fundamental and intermodulation products for a 5 MHz tone spacing is reported. From the reported results we can see that both higher and lower terms all follow a consistent pattern with an IMD3 "null" at 28 dBm input power without associated gain expansion of the fundamental tone powers. The IMD3 null fills a much wide input power bandwidth than any other observed null, but it transitions from the 3 dB/dB slope at low input powers to a 5 dB/dB slope above the null.

In Figure 6.11 the measured higher and lower fundamental and intermodulation products for a 10 MHz tone spacing is reported. From the reported results we can see that both higher and lower terms all follow a
consistent pattern at the fundamental with an IMD3 "null" at 34 dBm input power for the higher tone that is not present in the lower tone. The observed null in the lower tone is shallower than that for the 5 MHz tone spacing while the higher tone null is deeper. This relationship suggests a highly reactive baseband termination at 10 MHz that results in a highly asymmetric IMD3 response. The observed level IMD3 power at low input power for the intermodulation terms is due to measurement error close to the analyzer noise floor.

In Figure 6.12 the measured higher and lower fundamental and intermodulation products for a 20 MHz tone spacing is reported. From the reported results we can see that both higher and lower terms all follow a consistent pattern with the higher tone showing 1 dB to 2 dB more power at the IMD3 and 1 dB to 2 dB less at the fundamental.
Figure 6.10: Network I: 5 MHz Tone spacing at -3V gate bias. Intermodulation terms are dashed lines.

Figure 6.11: Network I: 10 MHz Tone spacing at -3V gate bias. Intermodulation terms are dashed lines.

Figure 6.12: Network I: 20 MHz Tone spacing at -3V gate bias. Intermodulation terms are dashed lines.
<table>
<thead>
<tr>
<th>Mask Spacing</th>
<th>Lower Channel</th>
<th>Upper Channel</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 MHz</td>
<td>-28.10 dB</td>
<td>-23.73 dB</td>
</tr>
<tr>
<td>10 MHz</td>
<td>-45.13 dB</td>
<td>-44.81 dB</td>
</tr>
</tbody>
</table>

Table 6.4: Network I: measured ACPR with 5 MHz bandwidth and 41 dBm PEP.

6.6.2 Complex Modulated Waveform Results

In order to understand how this amplifier performs under a complex modulation scheme it was tested using a LTE EUTRA waveform with 5 MHz signal bandwidth. This signal was configured to have a 41 dBm peak envelope power (PEP) and 10 dB peak to average power ratio (PAPR). The resulting adjacent channel power ratio (ACPR) measurements for the two defined bands is shown in Table 6.4. The asymmetric response of the upper and lower 5 MHz mask are indicative of the baseband dependency observed at this bias point.

6.7 Comparison of Network Performance

To better understand the tradeoffs between each of the networks we consider the ratio of carrier power to intermodulation tone power for the higher carrier and intermodulation powers measured. Figure 6.13 reports this analysis for the four networks. Based on these reported values we can see that Network H (50 Ω shorted stub) presents the lowest C/I ratio over the full range of input powers while Network I (50 Ω shorted stub) and Network F (50 Ω λ/4 line) both have similarly high C.I ratios. Network G (30 Ω λ/4 line) performs very similarly to Network F over the full input power range.

We now move to compare the self-modulation performance of each of these networks. Given the measured self-modulation similarities of networks F and H (both are 50 Ω line based) and networks G and I (both are 30 Ω line based) we will only discuss networks H and I here for brevity.

First, we want to verify the instantaneous voltage and current waveforms to ensure that they are responding as theory indicates they should. Figure 6.14 shows the measured instantaneous voltage and current waveforms for Network H under 68 mA of average current draw. As expected we can see the characteristic voltage modulation due to the inductance of the line. Even though network I has a smaller voltage modulation we see
almost half a volt of shift under very small current draw (given the amplifier can draw ten times the shown average current). In this graphic we can also see how the 28 V crossings of the voltage waveform lags the maximum current points, as expected from the voltage-limiting we observe.

Next, we consider the difference in the instantaneous current waveform due to the change in bias line inductance. Figure 6.15 reports the one cycle of measured instantaneous current waveforms for 10 MHz tone separation for networks H and I. We can clearly see that network I (30 Ω) shows some distortion, but in general follows the expected current waveform. Network H (50 Ω) on the other hand shows significant current waveform distortion due to the voltage-limiting behavior of the transistor. The distinct peaks and valleys of the waveform can be attributed to the relatively large voltage dependence present in $g_m$.

Finally, we consider the current waveform distortion effects due to increasing tone spacing. Figure 6.16 shows the instantaneous current draw in network I for 100 mA average current draw signals under 5 MHz and 10 MHz tone spacings. We can clearly see that the 5 MHz spacing waveform is very similar to the ideal waveform while the 10 MHz spacing waveform shows clear distortion in a bifurcated peak. The increased
Figure 6.14: Network I: Low current draw voltage and current instantaneous waveforms at 5 MHz spacing.

Figure 6.15: Comparison of Network H (50 Ω) and Network I (30 Ω) instantaneous current draw for 10 MHz tone spacing with 200 mA average current draw.
distortion in the 10 MHz spacing can be attributed to the increased number of peaks compared to a 5 MHz spacing waveform for a similar current change. The increased number of peaks for a similar current change means that the 10 MHz spacing waveform experiences a higher $\frac{\partial i(t)}{\partial t}$ which leads to higher self-modulation.

Figure 6.16: Network I: Increased waveform distortion with 100 mA average current draw showing increased peaking due to increased tone spacing.
Chapter 7

Conclusion

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7.1 Summary and Important Results

In this work several key aspects to the design and realization of effective RF power amplifier bias circuits were discussed. In Chapter 2 "weak" and "strong" nonlinear effects in power amplifiers were investigated and their interactions explained based on existing results from the literature. "Weak" nonlinear effects were investigated using the Volterra-Wiener nonlinear transfer function model to demonstrate the baseband dependency present in those nonlinear effects. "Strong" nonlinear effects were briefly discussed using a describing function model which showed that in saturation the IMD3 tones will be one third the power of the saturated main tones and 180 degrees out of phase. Using these results we saw how "weak" and "strong" nonlinear behavior act additively in the transition region where the PA is starting to compress.

In Chapter 3 self-modulation and RF loss associated with the bias and supply lines were considered. The observed gain hysteresis and degraded power added efficiency of a real power amplifier were explained in
terms of the self-modulation of the bias voltage and current waveforms. This self-modulation is understood as a loss in current when the device becomes voltage limited as a result of a voltage sag due to the inductive nature of typical bias circuits.

In Chapter 4 nine single-ended power amplifier designs based on the CGH27015F GaN 15 W transistor from Cree (now Wolfspeed) were designed to test the bias line effects explained in Chapters 2 and 3. These amplifiers operated around a center frequency of 2.2 GHz with a 1 dB power compression output power of 41 dBm.

In Chapter 5 the testing methodology used to characterize the performance of the amplifier designs proposed in Chapter 4 was discussed. The required test bench specifications to characterize the power amplifiers under test were derived for the four classes of measurement that needed to be performed: single tone (CW) measurements, two tone measurements, drain voltage and current waveform measurements, and complex modulation signal measurements. The calibration process and calibration results were reported.

In Chapter 6 the results of testing four of the amplifiers described in Chapter 4 using the test bench described in Chapter 5 were presented. Networks F, G, H, and I were tested under CW, two tone, and complex modulation conditions and the effects of self modulation and "soft" nonlinearity driven by baseband terminations were discussed as a function of the different bias designs.

Several key takeaways were found through the investigation described above. These takeaways are discussed in more detail in their relevant chapters. These takeaways have been centrally compiled here for reference.

**Key Takeaways:**

1. The optimal bias line implementation to minimize IMD3 is driven by the desired video bandwidth of the signal.

2. In general the baseband impedance should vary with the second harmonic impedance across the amplifier’s video bandwidth to minimize the IMD3 in the "soft" nonlinearity regime.

3. The baseband impedance should be selected with the second harmonic impedance across the amplifier’s video bandwidth to induce an appropriate "sweet spot" in IMD3 as the amplifier begins to compress.
(4) For systems where the narrow-band approximation does not hold, the baseband impedance can be used to minimize IMD3 with the second harmonic, entirely independently of the first harmonic.

(5) Self-modulation effects are more pronounced at higher video bandwidth due to an increased number of peaking transients.

(6) Self-modulation can be minimized through lower line inductance, but the use of wide transmission lines does not necessarily improve IMD3.

7.2 Future Work

Given the relatively small body of work currently available on bias line design and its associated concerns this research area presents a unique opportunity. The linearity-efficiency compromise has strangled the design of power amplifiers, but by improving the linearity of the system through control of the soft nonlinearities dependent on the baseband impedance this constraint can be eased allowing more efficient amplifier design. Moving forward with this approach there are three particularly interesting design problems as described below.

**Potential Future Work:**

1. Biasing Class-J amplifiers such that the baseband impedance follows the second harmonic impedance

2. "Baseband feedback" to lower IMD3 by making a "negative" baseband impedance

3. Active biasing circuits to minimize self-modulation

The biasing of Class-J amplifiers (or continuous mode classes in general) is interesting due to the variable second harmonic termination presented to the device. The application of variable fundamental and second harmonic terminations is used to improve the efficiency of the amplifier while maintaining RF output power [45]. The dependence of the soft nonlinearity cancellation on the difference between the second harmonic and baseband impedances means that for a conventionally biased Class-J PA we would expect to see a highly variable linearity response to different video bandwidths. This particular architecture is then
ripe for investigation as the second harmonic termination becomes a design parameter rather than a fixed value, which could allow co-design of a system that shows simultaneously improved linearity and efficiency compared to a conventionally Class-B device.

Another highly interesting approach involves the implementation of a feedback network across the baseband such that the impedance presented at baseband can be dynamically controlled. The easiest way to understand the value of baseband feedback is to consider the vector representation of IMD3 originally shown in Figure 2.8 that depicts the IMD3 as a vector sum of the vectors $K_C$, $K_D$, and $K_D^*$. In baseband feedback it is possible to realize $K_D$, and $K_D^*$ vectors with arbitrary imaginary and real parts such that they can cancel the $K_C$ vector and completely eliminate IMD3 power in the ideal case. The baseband feedback has been previously demonstrated to reduce IMD3 power by up to 20 dB in common gate silicon transistors which suggests this approach could be used in modern systems [46]. Figure 7.1 shows a two stage modelling approach that builds to the proposed feedback network. Effective nonlinear modelling of a simultaneous feedback and feed-forward system separated in frequency represents a very interesting design problem that is not well considered in the current literature. The application of a baseband feedback network would also allow the linearity effects and self-modulation induced by a bias element to be decoupled from each other.

![Figure 7.1: Proposed baseband feedback power amplifier design approach.](image)

While each of the above research topics focuses on linearity improvement through baseband impedance control it is also valuable to explore alternative methods to concurrently minimize self-modulation. A commonly used technique with older designs is to employ an active bias approach. An active bias usually
involves using a voltage follower circuit such that a desired voltage can be accurately maintained while applying the necessary current to the device. This approach minimizes the self-modulation effect but introduces tradeoffs in the realizable RF loss and IMD3.

Overall there are several interesting and highly valuable extensions to the work presented here. The future of RF power amplifier design is a bright one, and I am personally very excited to see where it leads me.
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Appendix A

Heatsink Mechanical Drawing
# Appendix B

## MATLAB Code for Power Amplifier Characterization Bench

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B.1 CW Testing Scripts
% Master's Thesis CW Measurement Main
% William Sear
% 03-November-2018

%% Setup MATLAB
addpath('C:\Users\Mee\Documents\WORK\RFPL\ThesisWork\College-MastersThesis\Testing\EquipmentTools')

%% Configure Calibration Range
%Fo = [2.1e9:10e6:2.3e9]; %Hz
%Pavs_Desired = [0:1:43]; %dBm

%% Bench Equipment Configuration and Setup
% General Settings
timestamp = datestr(now, 'yyyy.mm.dd_HH.MM');

% Equipment Setup
SMJ100A = SMJ100A_Setup() %Vector Signal Generator
FSQ26 = FSQ26_Setup(2.2e9), bandwidth, measureTime, mechAttenuation) %Vector Signal Analyzer
N6705A = N6705A_Setup() %DC Power Supply
Gate = 1;
Drain = 2;

%% Bias On DUT
N6705A_SetVal(N6705A, Gate, 'current', 0.5)
N6705A_SetVal(N6705A, Drain, 'current', 1.5)
N6705A_SetVal(N6705A, Gate, 'voltage', 5) %Bias DUT to Pinch Off
N6705A_OnOff(N6705A, Gate, 'on')
pause(1)
N6705A_SetVal(N6705A, Drain, 'voltage', 0) %Bias Drain low
N6705A_OnOff(N6705A, Drain, 'on')
N6705A_SetVal(N6705A, Drain, 'voltage', 28) %Bias up Drain
N6705A_SetVal(N6705A, Gate, 'voltage', 3) %Bias DUT to Operational

%% Calibrate Driver Amplifier Power Levels
Pset = -43.1:1:-8.1;
%Pmeas_Driver = CalDriver( SMJ100A, FSQ26, 2.2e9, Pset)
%save('Driver_CW.mat', 'Pmeas_Driver', 'Pset')
[Pmeas_Amp_NetH, Pdc, Id] = CalDriver( SMJ100A, FSQ26, [2.1e9 2.15e9 2.2e9 2.25e9 2.3e9], Pset, N6705A)
%save('Driver_2Tone.mat', 'Pset', 'P1H', 'P1L', 'P3H', 'P3L', 'Pcmp', 'ToneSpacing')
%save('NetH_CW.mat', 'Pdc', 'Pmeas_Amp_NetH', 'Pset')

%% Bias Off DUT
N6705A_SetVal(N6705A, Gate, 'voltage', 5) %Bias DUT to Pinch Off
pause(1)
N6705A_SetVal(N6705A, Drain, 'voltage', 0) %Bias Drain down
pause(1)
N6705A_OnOff(N6705A, Drain, 'off')
pause(1)
N6705A_OnOff(N6705A, Gate, 'off') %Comment out if DUT will remain connected

%% Disconnect Bench Equipment
SMJ100A_Close( SMJ100A ) %Vector Signal Generator
N6705A_Close( N6705A ) %DC Supply
FSQ26_Close( FSQ26 ) %Vector Signal Analyzer

%% Find Results
%Pavs = Pmeas_Driver(2:end) + RealAtten(11);
%Pin = 0.001*10.^(Pavs./10);
%PoutdBm = Pmeas_Amp_NetH+RealAtten(11);
%Pout = 0.001*10.^(PoutdBm./10)
%Gain = Pmeas_Amp-Pmeas_Driver;

%ax = gca;
%ax.GridAlphaMode = 'manual'
%ax.GridAlpha = 0.35
function [ Pout, Pdc, Id ] = CalDriver( SMJ100A, FSQ26, Fo, Pcal, N6705A), bandwidth, measureTime, mechAttenuation)

% CalCoupler Calibrates the Power In at the Input plane of the DUT
% Detailed explanation goes here

%% Setup
% SMJ100A = SMJ100A_Setup() % Vector Signal Generator
% FSQ26 = FSQ26_Setup(2.2e9), bandwidth, measureTime, mechAttenuation) % Vector Signal Analyzer

%% Thermal Steady State
SMJ100A_FreqSet(SMJ100A, Fo(1))
SMJ100A_PowerSet(SMJ100A, Pcal(1))
SMJ100A_OnOff(SMJ100A, 'on')
pause(20)

Vgg = -3.2:0.1:-2.5;

%% Run Calibration
Pout = zeros(length(Fo), length(Vgg), length(Pcal));
Vd = zeros(length(Fo), length(Vgg), length(Pcal));
Vg = zeros(length(Fo), length(Vgg), length(Pcal));
Id = zeros(length(Fo), length(Vgg), length(Pcal));
Ig = zeros(length(Fo), length(Vgg), length(Pcal));
Pdc = zeros(length(Fo), length(Vgg), length(Pcal));

h = waitbar(0, 'Driver Calibration Sweep in Progress...')
idx = 0;
for i = 1:length(Fo)
    SMJ100A_FreqSet(SMJ100A, Fo(i))
    FSQ26_Close( FSQ26 )
    FSQ26 = FSQ26_Setup(Fo(i)), bandwidth, measureTime, mechAttenuation)
    for k = 1:length(Vgg)
        N6705A_SetVal(N6705A, 1, 'voltage', abs(Vgg(k))
        for j = 1:length(Pcal)
            SMJ100A_PowerSet(SMJ100A, Pcal(j))
            pause(5) % Thermal Steady State
            Pout(i,k,j) = FSQ26_ReadTonePower(FSQ26, Fo(i));
            Vd(i,k,j) = N6705A_GetVal(N6705A, 2, 'voltage');
            Vg(i,k,j) = N6705A_GetVal(N6705A, 1, 'voltage');
            Id(i,k,j) = N6705A_GetVal(N6705A, 2, 'current');
            Ig(i,k,j) = N6705A_GetVal(N6705A, 1, 'current');
            Pdc(i,k,j) = Vd(i,k) * Id(i,k) + Vg(i,k) * Ig(i,k);
            waitbar(idx./((length(Fo)*length(Pcal)*length(Vgg))), 'CW Sweep in Progress...')
            idx = idx+1;
        end %Pcal
    end %Vgg
end %Fo
SMJ100A_OnOff(SMJ100A, 'off')
close(h) % close waitbar
end
B.2 Two Tone Testing Scripts
B.2.1 Two Tone Main Script

11/6/18 9:56 AM C:\Users\Mee\Documents...\TwoTone CalMain.m 1 of 2

% Master's Thesis Two Tone Test Main
% William Sear
% 03-November-2018

%% Setup MATLAB
addpath('C:\Users\Mee\Documents\_WORK\RFPL\ThesisWork\College\MastersThesis\Testing\EquipmentTools')

%% Configure Calibration Range
Pset = -43.1:1:-8.1;
Pcmp = 0;
Pset = Pset - Pcmp;
ToneSpacing = [5e6 10e6 20e6];

%% Bench Equipment Configuration
% General Settings
timestamp = datestr(now, 'yyyy.mm.dd_HH.MM');

% Equipment Setup
SMJ100A = SMJ100A_Setup() %Vector Signal Generator
FSQ26 = FSQ26_Setup(2.2e9), bandwidth, measureTime, mechAttenuation) %Vector Signal Analyzer
N6705A = N6705A_Setup() %DC Power Supply

Drain = 2;
Gate = 1;

%% Bias On DUT
N6705A_SetVal(N6705A, Gate, 'current', 0.5)
N6705A_SetVal(N6705A, Drain, 'current', 1.5)

N6705A_SetVal(N6705A, Gate, 'voltage', 5) %Bias DUT to Pinch Off
N6705A_OnOff(N6705A, Gate, 'on')
pause(1)
N6705A_SetVal(N6705A, Drain, 'voltage', 0) %Bias Drain low
N6705A_OnOff(N6705A, Drain, 'on')
N6705A_SetVal(N6705A, Drain, 'voltage', 28) %Bias up Drain

%% Calibrate Driver IMD3
[ P1L, P1H, P3L, P3H, Pdc, Id ] = TwoTone_CalDriver( SMJ100A, FSQ26, [2.2e9], Pset-
ToneSpacing, N6705A)

%% Bias Off DUT
N6705A_SetVal(N6705A, Gate, 'voltage', 5) %Bias DUT to Pinch Off
pause(1)
N6705A_SetVal(N6705A, Drain, 'voltage', 0) %Bias Drain down
pause(1)
N6705A_OnOff(N6705A, Drain, 'off')
pause(1)
N6705A_OnOff(N6705A, Gate, 'off') %Comment out if DUT will remain connected
%% Disconnect Bench Equipment
SMJ100A_Close( SMJ100A ) % Vector Signal Generator
N6705A_Close( N6705A ) % DC Supply
FSQ26_Close( FSQ26 ) % Vector Signal Analyzer
function [ Pout, Pdc, Id ] = CalDriver( SMJ100A, FSQ26, Fo, Pcal, N6705A, bandwidth, measureTime, mechAttenuation )
% CalCoupler Calibrates the Power In at the Input plane of the DUT
% Detailed explanation goes here

%% Setup
% SMJ100A = SMJ100A_Setup() %Vector Signal Generator
% FSQ26 = FSQ26_Setup(2.2e9), bandwidth, measureTime, mechAttenuation) %Vector Signal Analyzer

%% Thermal Steady State
SMJ100A_FreqSet(SMJ100A, Fo(1))
SMJ100A_PowerSet(SMJ100A, Pcal(1))
SMJ100A_OnOff(SMJ100A, 'on')
pause(20)
Vgg = -3.2:0.1:-2.5;

%% Run Calibration
Pout = zeros(length(Fo), length(Vgg), length(Pcal));
Vd = zeros(length(Fo), length(Vgg), length(Pcal));
Vg = zeros(length(Fo), length(Vgg), length(Pcal));
Id = zeros(length(Fo), length(Vgg), length(Pcal));
Ig = zeros(length(Fo), length(Vgg), length(Pcal));
Pdc = zeros(length(Fo), length(Vgg), length(Pcal));

h = waitbar(0, 'Driver Calibration Sweep in Progress...')
idx = 0;
for i = 1:length(Fo)
    SMJ100A_FreqSet(SMJ100A, Fo(i))
    FSQ26_Close(FSQ26)
end %Fo

for k = 1:length(Vgg)
    N6705A_SetVal(N6705A, 1, 'voltage', abs(Vgg(k)))
end %Vgg

for j = 1:length(Pcal)
    SMJ100A_PowerSet(SMJ100A, Pcal(j))
    pause(5) %Thermal Steady State
    Pout(i,j,k) = FSQ26_ReadTonePower(FSQ26, Fo(i));
    Vd(i,j,k) = N6705A_GetVal(N6705A, 2, 'voltage');
    Vg(i,j,k) = N6705A_GetVal(N6705A, 1, 'voltage');
    Id(i,j,k) = N6705A_GetVal(N6705A, 2, 'current');
    Ig(i,j,k) = N6705A_GetVal(N6705A, 1, 'current');
    Pdc(i,j,k) = Vd(i,j)*Id(i,j) + Vg(i,j)*Ig(i,j);
    waitbar(idx./(length(Fo)*length(Pcal)*length(Vgg)),h,'CW Sweep in Progress...')
    idx = idx+1;
end %Pcal
end %Vgg
end %Fo
SMJ100A_OnOff(SMJ100A, 'off')
close(h) %close waitbar
P3H(j,i,m,k) = FSQ26_ReadTonePower(FSQ26, IMD3ToneH);

Vd(j,i,m,k) = N6705A_GetVal(N6705A, 2, 'voltage');
Vg(j,i,m,k) = N6705A_GetVal(N6705A, 1, 'voltage');
Id(j,i,m,k) = N6705A_GetVal(N6705A, 2, 'current');
Ig(j,i,m,k) = N6705A_GetVal(N6705A, 1, 'current');
Pdc(j,i,m,k) = Vd(j,i,m,k)*Id(j,i,m,k) + Vg(j,i,m,k)*Ig(j,i,m,k);

waitbar(idx.\(\text{length(Fo)}\)*\(\text{length(ToneSpacing)}\)*\(\text{length(Pcal)}\)*\(\text{length(Vgg)}\)), 'Two Tone: Sweep in Progress...'
idx = idx+1;
end %Pcal
end %Spacing
    end % Vgg
end %Fo

SMJ100A_OnOff(SMJ100A, 'off')
close(h) %close waitbar
end %function
B.3 SMJ100A Supporting Functions
B.3.1 SMJ100A Setup

```matlab
function [ SMJ100A ] = SMJ100A_Setup(  )
%SMJ100A_Setup Configures the SMJ100A Signal Generator to be used in MatLab
% Detailed explanation goes here
SMJ100A = gpib('AGILENT', 7, 28);
fclose(SMJ100A)
KeepLocalFile    = 0;                       % waveform only temporarily saved
LocalFileName    = 'awgn.wv';               % The local and remote file name
InstrTargetPath = 'D:\';                   % MS Windows based, e.g. SMU, SMJ, SMATE
StartARB         = 1;                       % start in path A
end
```
function [ ] = SMJ100A_OnOff( SMJ100A, ChangeTo )

%SMJ100A_OnOff Turns the SMJ100A On and Off
%   Detailed explanation goes here

if strcmp(ChangeTo, 'On') | strcmp(ChangeTo, 'on')
    [status, Result] = rs_send_query( SMJ100A, 'OUTP:STAT ON; *OPC?');
    if( ~status ); clear;  return; end
elseif strcmp(ChangeTo, 'Off') | strcmp(ChangeTo, 'off')
    [status, Result] = rs_send_query( SMJ100A, 'OUTP:STAT OFF; *OPC?');
    if( ~status ); clear;  return; end
else
    disp('Unknown ChangeTo for SMJ100A_OnOff')
end
end

B.3.2 SMJ100A RF On/Off Commanding
B.3.3 SMJ100A RF Frequency Commanding

function [] = SMJ100A_FreqSet(SMJ100A, Fo)
%SMJ100A_FreqSet Sets the Frequency of the SMJ100A
% Detailed explanation goes here

message = sprintf('FREQ %.6f GHz; *OPC?', Fo/1e9);
[status, Result] = rs_send_query(SMJ100A, message);
if(~status); clear; return; end

end
function [  ] = SMJ100A_PowerSet( SMJ100A,  Power)
%SMJ100A_PowerSet Sets output power of SMJ100A in dBm
% N/A
message =  sprintf('POW %f dBm; *OPC?',Power);
[status, Result] = rs_send_query( SMJ100A, message );
    if( ~status ); clear;  return; end

end
function [ ] = SMJ100A_TwoToneGen( SMJ100A, Fo, DFreq1, DFreq2, OS )
%SMJ100A_TwoTone Generates a Two Tone Signal of frequencies DFreq1 and DFreq2

KeepLocalFile    = 0;                       % waveform only temporarily saved
LocalFileName    = 'awgn.wv';               % The local and remote file name
InstrTargetPath = 'D:\';                   % MS Windows based, e.g. SMU, SMJ, SMATE
StartARB         = 1;                       % start in path A

FMax = DFreq1;
if( DFreq2>FMax )
    FMax = DFreq2;
end

% calculate clock rate for ARB
Fsample = FMax * OS;
disp(['  Clock Rate      : ', num2str(Fsample/1e6,5), ' MHz']);
if( Fsample > 300e6)
    error('*** Error: Max. clock rate of 300 MHz exceeded !');
    return;
end

ggT of the two frequencies
a = int32(DFreq1);
b = int32(DFreq2);
if( a>0 && b>0 )
    while( a ~= b )
        if( a>b )
            a = a-b;
        else
            b = b-a;
        end
    end
iggt = a;
disp(['  ggT             : ', num2str(iggt), ' Hz' ]);;

% useful period width
Tggt = 1.0 ./ double(iggt);
disp(['  Signal Duration : ', num2str(Tggt,5), ' s']);

% calculate number of samples
Nsamples = Tggt * Fsample;
disp(['  Samples         : ', num2str(Nsamples,5)]);
% Make sure to use less than 16 Msamples
if( Nsamples > 16*1024*1024 )
    error('*** Error: Maximum number of samples exceeded !');
    return;
end
disp ([" "]);

% generate array of sample points
k = 1:1:Nsamples;
% and convert to time scale
Time = (k-1) * 1.0/Fsample;

% signal 1 and 2
Sig1 = cos( 2.0 * pi * DFreq1 * Time );
Sig2 = cos( 2.0 * pi * DFreq2 * Time );

Sig3 = sin( 2.0 * pi * DFreq1 * Time );
Sig4 = sin( 2.0 * pi * DFreq2 * Time );

% sum up all carriers along the time dimension in our
% result matrix
I_data = (Sig1 + Sig2);
Q_data = (Sig3 + Sig4);

% scale to 1.0 for the max envelope
MaxEnvelope = max( abs(complex(I_data,Q_data)) );
I_data = (I_data / MaxEnvelope) / sqrt(2);
Q_data = (Q_data / MaxEnvelope) / sqrt(2);

% *************************************************************************
% Setup Waveform Structure
% *************************************************************************
IQInfo.I_data         = I_data;         % I signal
IQInfo.Q_data         = Q_data;         % Q signal
IQInfo.comment        = 'Two Tone';     % optional comment
IQInfo.copyright      = 'Rohde&Schwarz';% optional copyright
IQInfo.clock          = Fsample;        % sample rate
IQInfo.no_scaling     = 0;              % scale automatically
IQInfo.path           = InstrTargetPath;% location on instrument
IQInfo.filename       = LocalFileName;  % local and remote file name

% *************************************************************************
% Plot Data
% *************************************************************************
rs_visualize( Fsample, IQInfo.I_data, IQInfo.Q_data );

% *************************************************************************
% Instrument Setup
% *************************************************************************
% check for R&S device, we also need the *IDN? result later...
disp( 'Checking instrument...' );
[status, InstrIDN] = rs_send_query( SMJ100A,'*IDN?' );
if(~status); clear; return; end
if( isempty( strfind( InstrIDN, 'Rohde&Schwarz' ) ) )
    disp('This is not a Rohde&Schwarz device.);
    clear; return;
end

% reset the instrument
[status, OPCResponse] = rs_send_query( SMJ100A, '*RST; *OPC?' );
if(~status); clear; return; end
[status] = rs_send_command( SMJ100A, '*CLS' );
if(~status); clear; return; end

% generate and send waveform
[status] = rs_generate_wave( SMJ100A, IQInfo, StartARB, KeepLocalFile );
if(~status); clear; return; end

% Apply RF settings if this is not a pure baseband source
if( isempty( strfind( InstrIDN, 'AFQ' ) ) && isempty( strfind( InstrIDN, 'AMU' ) ) )
    disp('Setting up RF...');
    % apply some RF settings
    message = sprintf('FREQ %.6f GHz; *OPC?', Fo/1e9)
    [status, Result] = rs_send_query( SMJ100A, message );
    if(~status); clear; return; end

    [status, Result] = rs_send_query( SMJ100A, 'POW -30.0 dBm; *OPC?' );
    if(~status); clear; return; end

    % switch output ON
    [status, Result] = rs_send_query( SMJ100A, 'OUTP:STAT ON; *OPC?' );
    if(~status); clear; return; end
end

% Read the instruments error queue
status = rs_check_instrument_errors( SMJ100A );
if(~status); clear; return; end
function [ ] = SMJ100A_Close( SMJ100A )
%SMJ100A_Close Disconnects from the SMJ100A Vector Signal Generator
% No detailed explanation
[status, Result] = rs_send_query( SMJ100A, 'OUTP:STAT OFF; *OPC?' );
if( ~status ); clear; return; end
fclose(SMJ100A);
delete(SMJ100A);
clear SMJ100A
end
B.4 FSQ26 SUPPORTING FUNCTIONS
function [ FSQ26 ] = FSQ26_Setup( centerFrequency), bandwidth, measureTime,...
%mechAttenuation )

%FSQ26_Setup Connects to the FSQ26 Vector Signal Generator and returns an
%object that can access the instrument.
% centerFrequency: Initial Center Frequency of Operation(Hz)
% bandwidth: Resolution bandwidth of signal(Hz)
% measureTime: Sets the integration time(sec)
% mechAttenuation: Mechanical attenuation Setting(dB)

% Bandwidth of the signal (Hz)
bandwidth = 500e6;
% Measurement time (s)
measureTime = 8e-3;
% Mechanical attenuation in the signal analyzer(dB)
mechAttenuation = 0;

FSQ26 = gpib('AGILENT', 7, 20);
FSQ26.InputBufferSize = 30e6;
FSQ26.Timeout = 20;
fopen(FSQ26)

% Set up signal analyzer mode to Basic/IQ mode
fprintf(FSQ26,'

% Set the center frequency
fprintf(FSQ26,['
% Set the resolution bandwidth
fprintf(FSQ26,

% Turn off averaging
fprintf(FSQ26,'
% set to take one single measurement once the trigger line goes high
fprintf(FSQ26,'
% Set the trigger to external source 1 with positive slope triggering
fprintf(FSQ26,
% Set the time for which measurement needs to be made
fprintf(FSQ26,
% Turn off electrical attenuation.
fprintf(FSQ26,
% Set mechanical attenuation level
fprintf(FSQ26,

% Turn IQ signal ranging to auto

136
fprintf(FSQ26,:SENSe:VOLTage:IQ:RANGE:AUTO ON);

% Set the endianness of returned data
fprintf(FSQ26,:FORMat:BORDer NORMal);

% Set the format of the returned data
fprintf(FSQ26,:FORMat:DATA REAL,32);

end
function [ Power ] = FSQ26_ReadTonePower( FSQ26, Freq )
% Summary of this function goes here
% Detailed explanation goes here

% Clear markers
% Trigger the instrument and initiate measurement
fprintf(FSQ26,'*TRG');
fprintf(FSQ26,':INITiate:WAVeform');

% Set Marker to Freq
fprintf(FSQ26,['CALC:MARK1:X ' num2str(Freq)]);
% Read Marker
Power = str2num(query(FSQ26, 'CALC:MARK1:Y?'));

end
function [ ] = FSQ26_Close( FSQ26 )
%FSQ26_Clear Disconnects from the FSQ26 Vector Signal Analyzer
%   No detailed explanation

fclose(FSQ26);
delete(FSQ26)
clear FSQ26
end
B.5 N6705A Supporting Functions
function [ N6705A ] = N6705A_Setup(  )
%N6705A_Setup Connects to the N6705A DC Power Supply and returns an
%object that can access the instrument.
N6705A = gpib('AGILENT', 7, 5);
fopen(N6705A)
end
function [ ] = N6705A_OnOff( N6705A, Channel, ChangeTo )
%N6705A_OnOff Allows N6705A supply channels to be turned off and on
%   N/A

if strcmp(ChangeTo, 'On') | strcmp(ChangeTo, 'on')
    message = sprintf('OUTP ON,(@%.0f)', Channel);
elseif strcmp(ChangeTo, 'Off') | strcmp(ChangeTo, 'off')
    message = sprintf('OUTP OFF,(@%.0f)', Channel);
else
    disp('Unknown ChangeTo for N6705A_GetVal')
end
fprintf(N6705A, message);
end
function [ ] = N6705A_SetVal( N6705A, Channel, ValueType, Value )

%N6705A_SetVal Sets the current or voltage to Value on the specified
%Channel
% N/A
if strcmp(ValueType, 'voltage') || strcmp(ValueType, 'Voltage')
    message = sprintf('VOLT %.2f, (@%.0f)', Value, Channel);
elseif strcmp(ValueType, 'current') || strcmp(ValueType, 'Current')
    message = sprintf('CURR %.2f, (@%.0f)', Value, Channel);
else
    disp('Unknown Value Type for N6705A_SetVal')
end
fprintf(N6705A, message)
end
function [ Value ] = N6705A_GetVal( N6705A, Channel, ValueType )
%N6705A_ReadVal Returns the current or voltage on the specified Channel
% N/A

if ValueType == 'voltage' | ValueType == 'Voltage'
    message = sprintf('MEAS:VOLT? (@%.0f)', Channel);
elseif ValueType == 'current' | ValueType == 'Current'
    message = sprintf('MEAS:CURR? (@%.0f)', Channel);
else
    disp('Unknown Value Type for N6705A_GetVal')
end
Value = str2num(query(N6705A, message));
end

B.5.4 N6705A Supply Power Return Value Commanding
function [ ] = N6705A_Close( N6705A )
%N6705A_Close Turns off and disconnects from N6705A Power Supply
% No detailed explanation.

fprintf(N6705A,'OUTP OFF,(01:4)');
fclose(N6705A)
delete(N6705A)
clear N6705A
end
B.6 E4419B SUPPORTING FUNCTIONS
B.6.1 E4419B Setup

function [ E4419B ] = E4419B_Setup( )
%FSQ26_Setup Connects to the E4419B Power Meter and returns an
%object that can access the instrument.

E4419B = gpib('AGILENT', 7, 14);
fopen(E4419B)
end
function [Power] = E4419B_ReadPower( E4419B, F )
%UNTITLED3 Summary of this function goes here
% Detailed explanation goes here
message = sprintf('SENS2:FREQ %.2fHz', F);
fprintf(E4419B, message);
%fprintf(E4419B, 'CONF2 DEF, DEF, (@2)');
fprintf(E4419B, 'INIT2');
Power = str2num(query(E4419B, 'FETC2?'));
end
function [ ] = E4419B_Close( E4419B )
% E4419B_Close Disconnects from E4419B Power Meter.
%   No detailed explanation
fclose(E4419B)
delete(E4419B)
clear E4419B
end
Appendix C

CW Results from Frequency Sweep

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C.1 Network F

The response of network F to a single tone excitation was measured as a function of gate bias and center frequency for gate biases between -3.5 V and -2.5 V and center frequencies between 2.1 GHz and 2.3 GHz. For the sake of brevity only the results for a center frequency of 2.2 GHz (the designed center frequency) will be considered.

In Figure C.1 the output power as a function of input power and gate bias is reported. There are three sweep values for which the results are inconsistent with the other reported curves (most notably the blue curve that rises to 20 dBm out at 24 dBm in at -2.5V) because at those gate biases the device becomes unstable. The results are still reported here as the instability is weak and a signal is still passed. In general we can see that while the device reaches the desired 41 dBm output power 1 dB compression point it follows a characteristic Class-C response. In general a higher bias voltage results in higher output power, as would
be expected.

In Figure C.2 the gain as a function of input power and gate bias is reported. There are three sweep values for which the results are inconsistent with the other reported curves (most notably the blue curve that rises to -10 dB of gain at 24 dBm in at -2.5V) because at those gate biases the device becomes unstable. The results are still reported here as the instability is weak and a signal is still passed. In general we can see that while the device reaches the desired 41 dBm output power 1 dB compression point it follows a characteristic Class-C response with gain only occurring when greater than 31 dBm of input power is present. This result is consistent with the results reported in Figure C.1 and with the bias point selected. In general a higher bias voltage results in higher gain, as would be expected.

In Figure C.3 the drain current draw as a function of input power and gate bias is reported. The three
unstable bias points show current draws that are consistent with the other curves. These results are consistent with the results reported in Chapter 4. As expected, when the gate bias is increased the current draw also increases.

In Figure C.4 the drain efficiency as a function of input power and gate bias is reported. There are three sweep values for which the results are inconsistent with the other reported curves because at those gate biases the device becomes unstable. The results are still reported here as the instability is weak and a signal is still passed. Given the output power reported in Figure C.1 and the drain current reported in Figure C.3 the drain efficiency follows the expected Class-C characteristic with generally low efficiency that rapidly increases to a maximum over 50%.

In Figure C.5 the power added efficiency as a function of input power and gate bias is reported. There
are three sweep values for which the results are inconsistent with the other reported curves because at those

gate biases the device becomes unstable. The results are still reported here as the instability is weak and a
signal is still passed. Given the output power reported in Figure C.1 and the drain current reported in Figure

C.3 the power added efficiency follows the expected Class-C characteristic with negative efficiency (due to
negative gain) that rapidly increases once the device presents gain.

C.2 Network G

The response of network G to a single tone excitation was measured as a function of gate bias and center
frequency for gate biases between -3.5 V and -2.5 V and center frequencies between 2.1 GHz and 2.3 GHz.
Figure C.4: Network F: drain efficiency as a function of input power at 2.2 GHz for gate bias between -3.5V and -2.5V.

For the sake of brevity only the results for a center frequency of 2.2 GHz (the designed center frequency) will be considered.

In Figure C.6 the output power as a function of input power and gate bias is reported. There are three sweep values for which the results are inconsistent with the other reported curves (most notably the blue curve that rises to 20 dBm out at 24 dBm in at -2.5V) because at those gate biases the device becomes unstable. The results are still reported here as the instability is weak and a signal is still passed. In general we can see that while the device does not reach the desired 41 dBm output power 1 dB compression point while following a Class-C response. In general a higher bias voltage results in higher output power, as would be expected.

In Figure C.7 the gain as a function of input power and gate bias is reported. There are three sweep values
for which the results are inconsistent with the other reported curves (most notably the blue curve that rises to -10 dB of gain at 24 dBm in at -2.5V) because at those gate biases the device becomes unstable. The results are still reported here as the instability is weak and a signal is still passed. In general we can see that the device does not reach the desired 41 dBm output power 1 dB compression point and follows a characteristic Class-C response with gain only occurring when greater than 31 dBm of input power is present. This result is consistent with the results reported in Figure C.6 and with the bias point selected. In general a higher bias voltage results in higher gain, as would be expected.

In Figure C.8 the drain current draw as a function of input power and gate bias is reported. The three unstable bias points show current draws that are consistent with the other curves. These results are consistent with the results reported in Chapter 4. As expected, when the gate bias is increased the current draw also
In Figure C.9 the drain efficiency as a function of input power and gate bias is reported. There are three sweep values for which the results are inconsistent with the other reported curves because at those gate biases the device becomes unstable. The results are still reported here as the instability is weak and a signal is still passed. Given the output power reported in Figure C.6 and the drain current reported in Figure C.8 the drain efficiency follows the expected Class-C characteristic with generally low efficiency that rapidly increases to a maximum (in this case 21%).

In Figure C.10 the power added efficiency as a function of input power and gate bias is reported. There are three sweep values for which the results are inconsistent with the other reported curves because at those gate biases the device becomes unstable. The results are still reported here as the instability is weak and a
signal is still passed. Given the output power reported in Figure C.6 and the drain current reported in Figure C.8 the power added efficiency follows the expected Class-C characteristic with negative efficiency (due to negative gain) that rapidly increases once the device presents gain.

**C.3 Network H**

The response of network H to a single tone excitation was measured as a function of gate bias and center frequency for gate biases between -3.5 V and -2.5 V and center frequencies between 2.1 GHz and 2.3 GHz. For the sake of brevity only the results for a center frequency of 2.2 GHz (the designed center frequency) will be considered.

In Figure C.11 the output power as a function of input power and gate bias is reported. There are five
sweep values for which the results are inconsistent with the other reported curves (the curves with higher bias points that drop out and then "pop up" at higher input powers) because at those gate biases the device becomes unstable. The results are still reported here as the instability is weak and a signal is still passed. In general we can see that while the device reaches the desired 41 dBm output power 1 dB compression point it follows a characteristic Class-C response. In general a higher bias voltage results in higher output power, as would be expected.

In Figure C.12 the gain as a function of input power and gate bias is reported. There are five sweep values for which the results are inconsistent with the other reported curves because at those gate biases the device becomes unstable. The results are still reported here as the instability is weak and a signal is still passed. In general we can see that while the device reaches the desired 41 dBm output power 1 dB compression point it
follows a characteristic Class-C response with gain only occurring when greater than 31 dBm of input power is present. This result is consistent with the results reported in Figure C.11 and with the bias point selected. In general a higher bias voltage results in higher gain, as would be expected.

In Figure C.13 the drain current draw as a function of input power and gate bias is reported. The five unstable bias points show current draws that are consistent with reported output power. These results are consistent with the results reported in Chapter 4. As expected, when the gate bias is increased the current draw also increases.

In Figure C.14 the drain efficiency as a function of input power and gate bias is reported. There are five sweep values for which the results are inconsistent with the other reported curves because at those gate biases the device becomes unstable. The results are still reported here as the instability is weak and a signal
Figure C.10: Network G: PAE as a function of input power at 2.2 GHz for gate bias between -3.5V and -2.5V.

is still passed. Given the output power reported in Figure C.1 and the drain current reported in Figure C.13 the drain efficiency follows the expected Class-C characteristic with generally low efficiency that rapidly increases to a maximum over 50%.

In Figure C.15 the power added efficiency as a function of input power and gate bias is reported. There are five sweep values for which the results are inconsistent with the other reported curves because at those gate biases the device becomes unstable. The results are still reported here as the instability is weak and a signal is still passed. Given the output power reported in Figure C.11 and the drain current reported in Figure C.13 the power added efficiency follows the expected Class-C characteristic with negative efficiency (due to negative gain) that rapidly increases once the device presents gain.
C.4 Network I

The response of network I to a single tone excitation was measured as a function of gate bias and center frequency for gate biases between -3.5 V and -2.5 V and center frequencies between 2.1 GHz and 2.3 GHz. For the sake of brevity only the results for a center frequency of 2.2 GHz (the designed center frequency) will be considered.

In Figure C.16 the output power as a function of input power and gate bias is reported. There are there sweep values for which the results are inconsistent with the other reported curves (the curves with higher bias points that drop out and then "pop up" at higher input powers) because at those gate biases the device becomes unstable. The results are still reported here as the instability is weak and a signal is still passed. In
general we can see that while the device reaches the desired 41 dBm output power 1 dB compression point it follows a characteristic Class-C response. In general a higher bias voltage results in higher output power, as would be expected.

In Figure C.17 the gain as a function of input power and gate bias is reported. There are three sweep values for which the results are inconsistent with the other reported curves because at those gate biases the device becomes unstable. The results are still reported here as the instability is weak and a signal is still passed. In general we can see that while the device reaches the desired 41 dBm output power 1 dB compression point it follows a characteristic Class-C response with gain only occurring when greater than 31 dBm of input power is present. This result is consistent with the results reported in Figure C.16 and with the bias point selected. In general a higher bias voltage results in higher gain, as would be expected.
In Figure C.18 the drain current draw as a function of input power and gate bias is reported. The three unstable bias points show current draws that are consistent with reported output power. These results are consistent with the results reported in Chapter 4. As expected, when the gate bias is increased the current draw also increases.

In Figure C.19 the drain efficiency as a function of input power and gate bias is reported. There are three sweep values for which the results are inconsistent with the other reported curves because at those gate biases the device becomes unstable. The results are still reported here as the instability is weak and a signal is still passed. Given the output power reported in Figure C.1 and the drain current reported in Figure C.18 the drain efficiency follows the expected Class-C characteristic with generally low efficiency that rapidly increases to a maximum over 50%.
In Figure C.20 the power added efficiency as a function of input power and gate bias is reported. There are three sweep values for which the results are inconsistent with the other reported curves because at those gate biases the device becomes unstable. The results are still reported here as the instability is weak and a signal is still passed. Given the output power reported in Figure C.16 and the drain current reported in Figure C.18 the power added efficiency follows the expected Class-C characteristic with negative efficiency (due to negative gain) that rapidly increases once the device presents gain.
Figure C.15: Network H: PAE as a function of input power at 2.2 GHz for gate bias between -3.5V and -2.5V. Intermodulation terms are dashed lines.
Figure C.16: Network I: output power as a function of input power at 2.2 GHz for gate bias between -3.5V and -2.5V.
Figure C.17: Network I: gain as a function of input power at 2.2 GHz for gate bias between -3.5V and -2.5V.
Figure C.18: Network I: drain current as a function of input power at 2.2 GHz for gate bias between -3.5V and -2.5V.
Figure C.19: Network I: drain efficiency as a function of input power at 2.2 GHz for gate bias between -3.5V and -2.5V.
Figure C.20: Network I: PAE as a function of input power at 2.2 GHz for gate bias between -3.5V and -2.5V.