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by

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1 Introduction

A 75% efficient amplifier can deliver twice the power that a 50% efficient amplifier can deliver, with the same devices and the same heat-sinking capability in both cases. The class-E switched-mode amplifier topology, shown in Figure 1, is investigated here. This class of amplifier was first proposed by Sokal and Sokal in 1975 [1]. The class-E amplifier is a tuned circuit in which the current and voltage time waveforms of the switch element are not simultaneously greater than zero, so that the dissipated power in the switching device is minimized. The active device, in this case a MESFET, acts as an ideal switch, and the surrounding circuitry needs to be properly designed to give class-E operation. At low RF frequencies, such circuits have shown to exhibit efficiencies as high as 96% [1]. Ideally, the efficiency is limited only by the drain-to-source saturation resistance of the transistor and the lossy properties of its parasitic elements. Device parasitic reactances are included in the tuned circuit design and do not degrade the circuit performance. For example, the capacitance C_1 in the circuit in Figure 1 is the output capacitance of the transistor itself. In this paper the switching element will be a MESFET, although high-frequency class-E circuits can be made using HBTs, PHEMTs, BJT's, or even vacuum tubes.

2 Simplified analysis of this class E circuit

There are several assumptions made in the simplified analysis of the class-E circuit presented here (see Figure 1). It is assumed that the switching element (in this case a MESFET) has zero on-resistance and infinite off-resistance. For a properly designed gate-drive circuit, the off resistance will be very large, but care must be taken to ensure that the on-resistance of a practical GaAs FET is much smaller than the impedance that it drives when it is turned on. The shunt capacitor C_1 for a maximum-frequency design consists solely of the output capacitance of the MESFET and is assumed to be linear in this analysis. In practice, the capacitance C_1 is nonlinear; its capacitance changes as a function of the voltage applied across it. The effects of this nonlinearity will be addressed in a future paper, although it has been found that an equivalent linear capacitance can approximate the nonlinear real capacitance in the circuit for a first-order design. L_b and C_b together act as an ideal bias tee. For dc biasing, the voltage V_g appears across the MESFET drain-source terminals, but not across the

$$\phi = -\arctan\frac{2}{\pi} \simeq -32.48°$$

$$a = \sqrt{1+\frac{\pi^2}{4}} \simeq 1.862$$

Note that these are constants for *any* high-Q class-E circuit with a capacitor in shunt with the switch (any microwave class-E circuit, for example).

$$v_{net} = \frac{I_g}{C_1}(t + \frac{aT_s}{2\pi}(\cos(\omega_s t + \phi) - \cos\phi))$$

$$i_{net} = I_g(a\sin(\omega_s t + \phi) - 1)$$

Now the voltage and current through the load network are known. Only the load impedance at f_s has to be found, since the load only responds to the fundamental frequency f_s. The fundamental component of load current, i_{net_1}, is known, but the fundamental component of load voltage, v_{net_1}, must be found using Fourier Series. The calculations are somewhat tedious, so only the results are given here.

$$v_{net_1} = a_2 I_g \sin(\omega_s t + \phi_2)$$

where

$$a_2 = \frac{1}{2\pi\omega_s C_1}\sqrt{(-4 + a\pi\cos\phi)^2 + (-2\pi + 4a\cos\phi + a\pi\sin\phi)^2}$$

$$\phi_2 = \frac{\pi}{2} + \arctan(\frac{-2\pi + 4a\cos\phi + a\pi\sin\phi}{-4 + a\pi\cos\phi})$$

The phasor impedance of the external load network can now be found:

$$Z_{net_1} = \frac{a_2}{a}\exp j(\phi_2 - \phi) \simeq \frac{0.28015}{\omega_s C_1}\exp j49.0524°$$

Notice that the required load angle for class-E operation is a constant, regardless of the rest of the topology. The magnitude is directly proportional to the impedance of the capacitor shunting the switch at the switching frequency. To ensure class-E operation, all that is needed is a fundamental impedance of Z_{net_1}, and open circuit conditions at all of the higher harmonic frequencies (a filter does this).

Now the specific external load network topology comes into the picture (Figure 3). All that is important for this step is the impedance of this particular topology at the switching frequency f_s (this network satisfies the condition of large input impedance at the higher harmonic frequencies).

$$Z_{net_1} = j\omega_s L_1 + \frac{R}{1 + j\omega_s C_2 R}$$

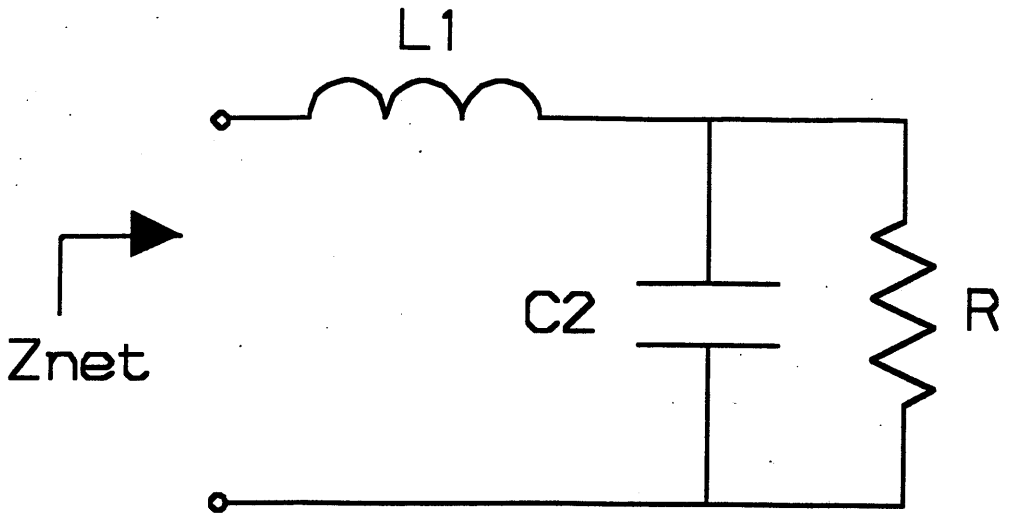

Figure 3: External load network seen by the switched capacitor at RF frequencies.

Equating the two expressions for Z_{net_1}, one complex equation in two unknowns (L_1 and C_2) is obtained. Equating real and imaginary parts of the equation, expressions for L_1 and C_2 are found:

$$C_2 = \sqrt{\frac{C_1}{\omega_s R k_1 \cos\theta_1}}$$

$$L_1 = \sqrt{\frac{C_1}{\omega_s R k_1 \cos\theta_1}} \frac{R^2}{1 + \frac{\omega_s C_1 R}{k_1 \cos\theta_1}} + \frac{k_1 \sin\theta_1}{\omega_s^2 C_1}$$

$$k_1 = \omega_s C_1 \frac{a_2}{a}$$

$$\theta_1 = \phi_2 - \phi$$

3 Relation between V_g and I_g

It is of interest to find the relationship between V_g and I_g, or in other words, how much current is drawn for a given supply voltage or vice-versa.

V_g is the dc component of $v_s(t)$, the voltage across the switch, capacitor and load network. From above,

$$v_s(t) = \frac{I_g}{C_1}(t + \frac{aT_s}{2\pi}(\cos(\omega_s t + \phi) - \cos\phi))$$

Take the time average of the switch voltage:

$$V_g = \frac{1}{T_s}\int_0^{\frac{T_s}{2}} v_s(t)dt = \frac{1}{\pi}\frac{I_g}{\omega_s C_1}$$

$$I_g = \pi\omega_s C_1 V_g$$

This rather simple result has important implications for a practical microwave class-E circuit, assuming that the minimum value of C_1 must necessarily be the parasitic capacitance of a microwave device, for example C_{ds} of a MESFET. For example, at a specified frequency, a device with some output capacitance C_1 must operate well above the knee voltage, say 3 volts. Since ω_s, C_1, and V_g are now specified, one hopes that the device can handle the required maximum current, which is $(1+a)I_g \simeq 2.86I_g$! If the device can not handle this current, then it is *impossible* to make a practical class-E circuit with the particular device at that frequency.

In fact, an approximate maximum frequency of class-E operation can be found for a given device. Assume that the device can't operate as a switch below $V_{min} = 1\,\mathrm{V}$ (otherwise it is too close to the knee voltage to obtain meaningful high-efficiency operation). Then take the device's maximum (peak) current, $I_{max} = (1+a)I_g \simeq 2.862I_g$. Then

$$f_{max} = \frac{I_g}{2\pi^2 C_1 V_g} = \frac{I_{max}}{C_1 V_{min}}\frac{1}{2\pi^2(1+a)} \simeq \frac{I_{max}}{56.5C_1}$$

Take, for example, the Fujitsu FLK052WG transistor. For this MESFET, take $I_{max} = I_{dss} \simeq 200\,\mathrm{mA}$ and $C_1 \simeq 1.2\,\mathrm{pF}$. For this transistor, $f_{max} \simeq 3\,\mathrm{GHz}$. Above this frequency, this device can not be used for a true class-E circuit.

The above discussion also implies that a given technology (MESFET, HEMT, HBT) using a given process will yield some maximum class-E output power as a function of frequency. This topic will be the subject of a future paper.

4 Microstrip Single-Stage Class E Amplifier

A single-stage microstrip class E amplifier was built and measured **to demonstrate the feasibility** of the class E transmission-line microwave amplifier approach. The circuit was fabricated on a Rogers Duroid substrate 60 mils thick with $\epsilon_r = 2.2$, using a low-power, non-optimal Fujitsu FLK052WG MESFET. The circuit was designed at 2.0 GHz for 59% drain efficiency, and 63% drain efficiency was measured at 2.0 GHz. A maximum of 68% drain efficiency was measured at 2.2 GHz. Hewlett Packard's MDS circuit simulator was used with nonlinear harmonic balance and a Curtice cubic model for the transistor. In this design, emphasis was placed on the output circuit. No input match was designed, to minimize frequency dependence due to the input circuit.

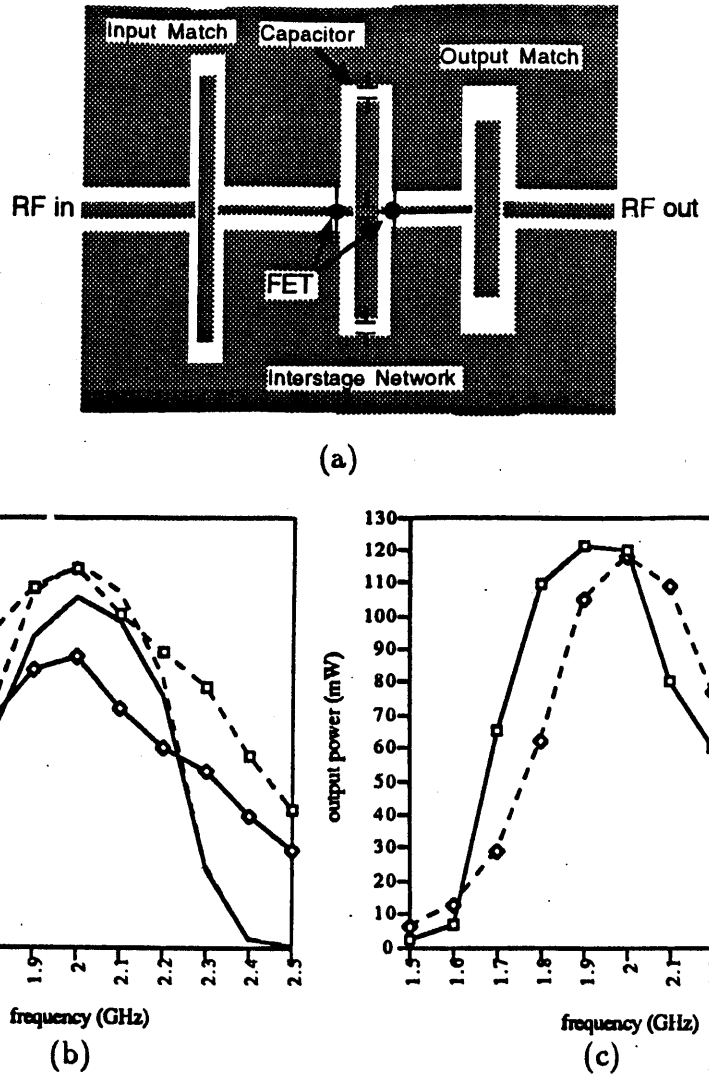

Figure 4: (a) Coplanar waveguide 2.0 GHz class E amplifier. (b) Power-added efficiency (solid line) and drain efficiency (dashed line). Measured results are represented with symbols. (c) Measured (solid line) and simulated (dashed line) output power vs. frequency.

5 Coplanar Two-Stage Low-Power Class E Amplifier

A two-stage coplanar waveguide (CPW) class E amplifier was designed and built using the same low-power MESFET as used above, as shown in Figure 4(a). CPW was chosen to eliminate reactance due to source vias and to facilitate heat sinking. A sinusoidal input matching stage was designed using a single open stub. The output power matching section was designed as in the previous case. A square wave voltage across the gate of the output-stage MESFET improves the drain efficiency of the amplifier. A shorted stub 66 electrical degrees long produced a nearly square waveform between the two FET's, while minimizing the power dissipated in the first FET. It was found that this section of shunt line mostly cancels out the parasitic capacitances of the two transistors at the odd harmonic frequencies, which are the Fourier components of a square wave.

The two-stage CPW class E amplifier was fabricated and measured, and a drain

efficiency of 61% and output power of 120 mW were measured at 2.0 GHz as predicted, indicating that the class E output power matching section worked. The simulated power-added efficiency was 59%, while a 47% power-added efficiency was measured. Simulated and measured results are shown in Figure 4(b) and (c). A more accurate nonlinear MESFET model may improve the design procedure for the first stage.

6 Coplanar Two-Stage High-Power Class E Amplifier

A new coplanar class E amplifier using high-power research chip MESFETs provided by the M/A-Com company was designed. This new amplifier was again simulated using a Curtice cubic model for the MESFETs and using the harmonic balance simulator on MDS. The metal layout is shown in Figure 5, below. The design is similar to the above lower-power CPW circuit, with some significant improvements in expected performance and some design tweaks.

Fabrication of this circuit is currently in progress, and the simulated power-added efficiency is 86%, while the simulated drain efficiency is 90%. CPW conductor losses are included in the circuit simulation, and these losses result in approximately 4% reduction in efficiency. Approximately 1 W of output power is expected from this new circuit at 2.0 GHz, at approximately 8 dBm input power. Saturated gain is therefore approximately 22 dB for this two-stage design.

Drain voltage and current waveforms for the output-stage MESFET are shown in Figure 6, while the nonsinusoidal (flattened-top) gate voltage waveform for the output-stage MESFET is shown in Figure 7. The output voltage waveform is shown in Figure 9. The second harmonic for the output signal is 59 dB below the carrier, while the third harmonic is 23 dB below the carrier.

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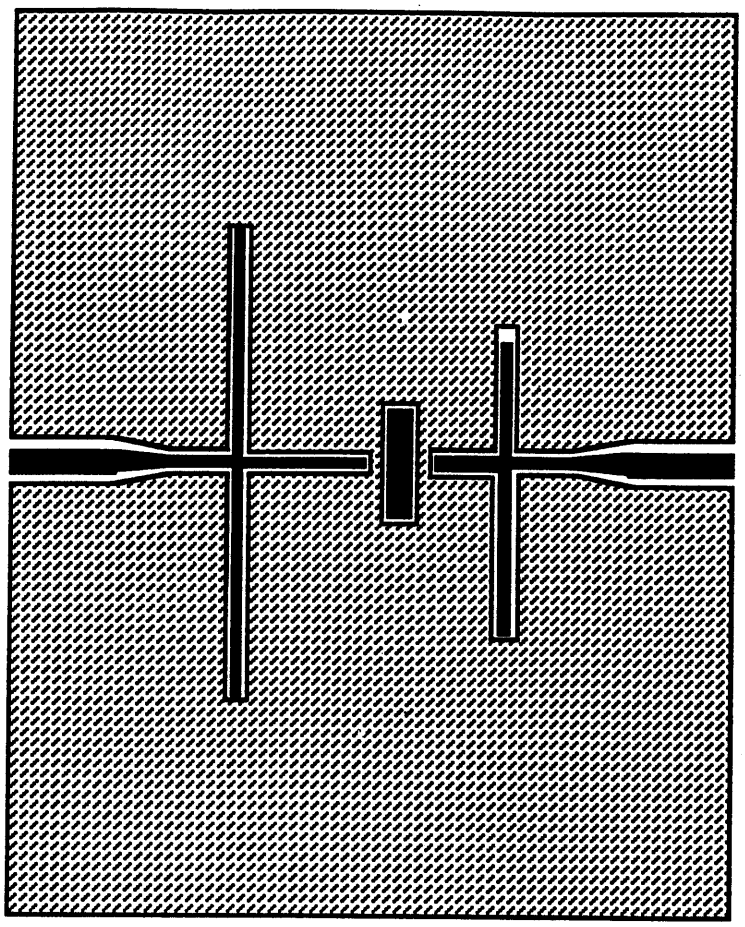

Figure 5: CPW metal geometry for new class E amplifier.

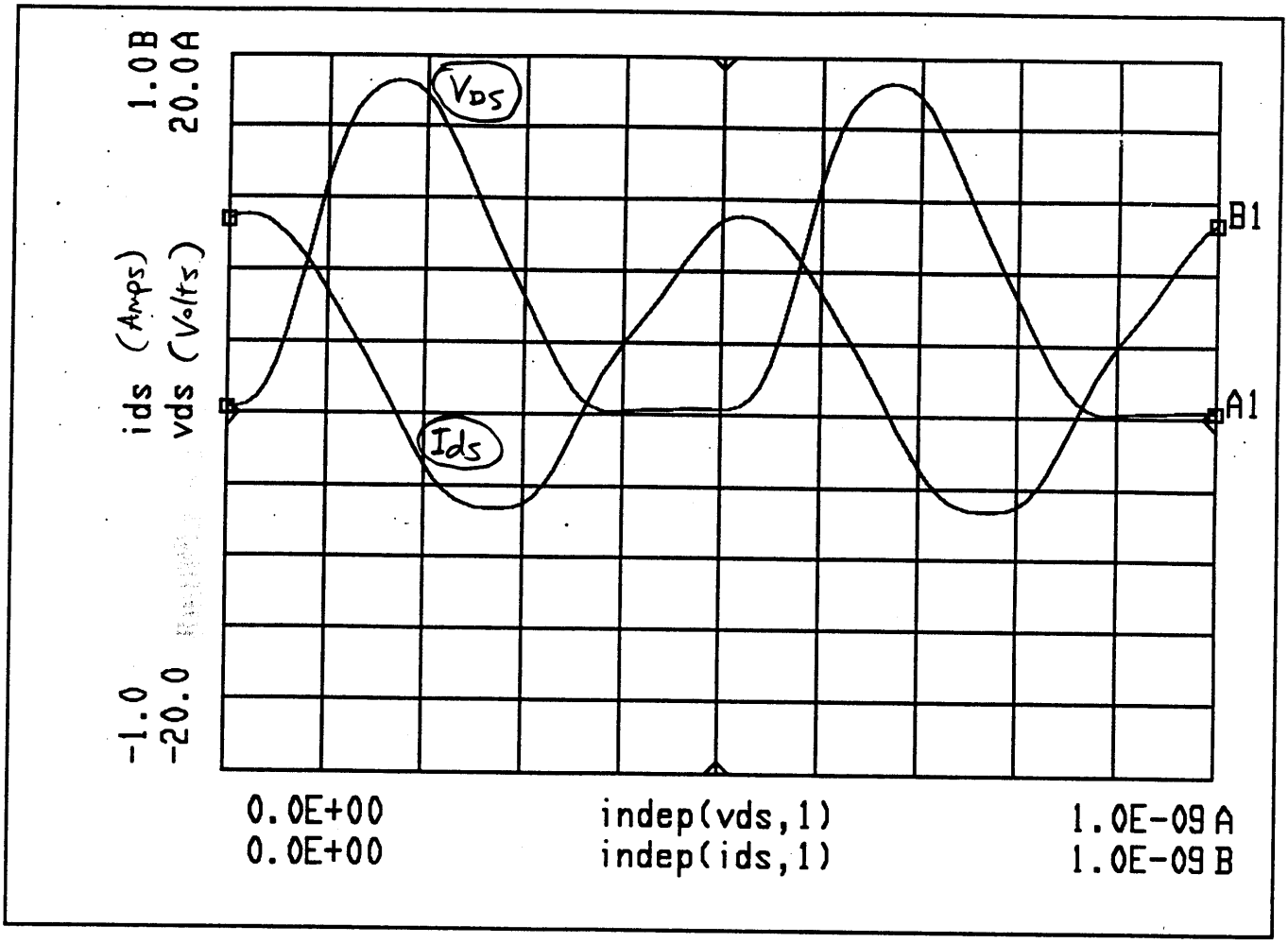

Figure 6: Drain voltage and current waveforms for the output-stage MESFET.

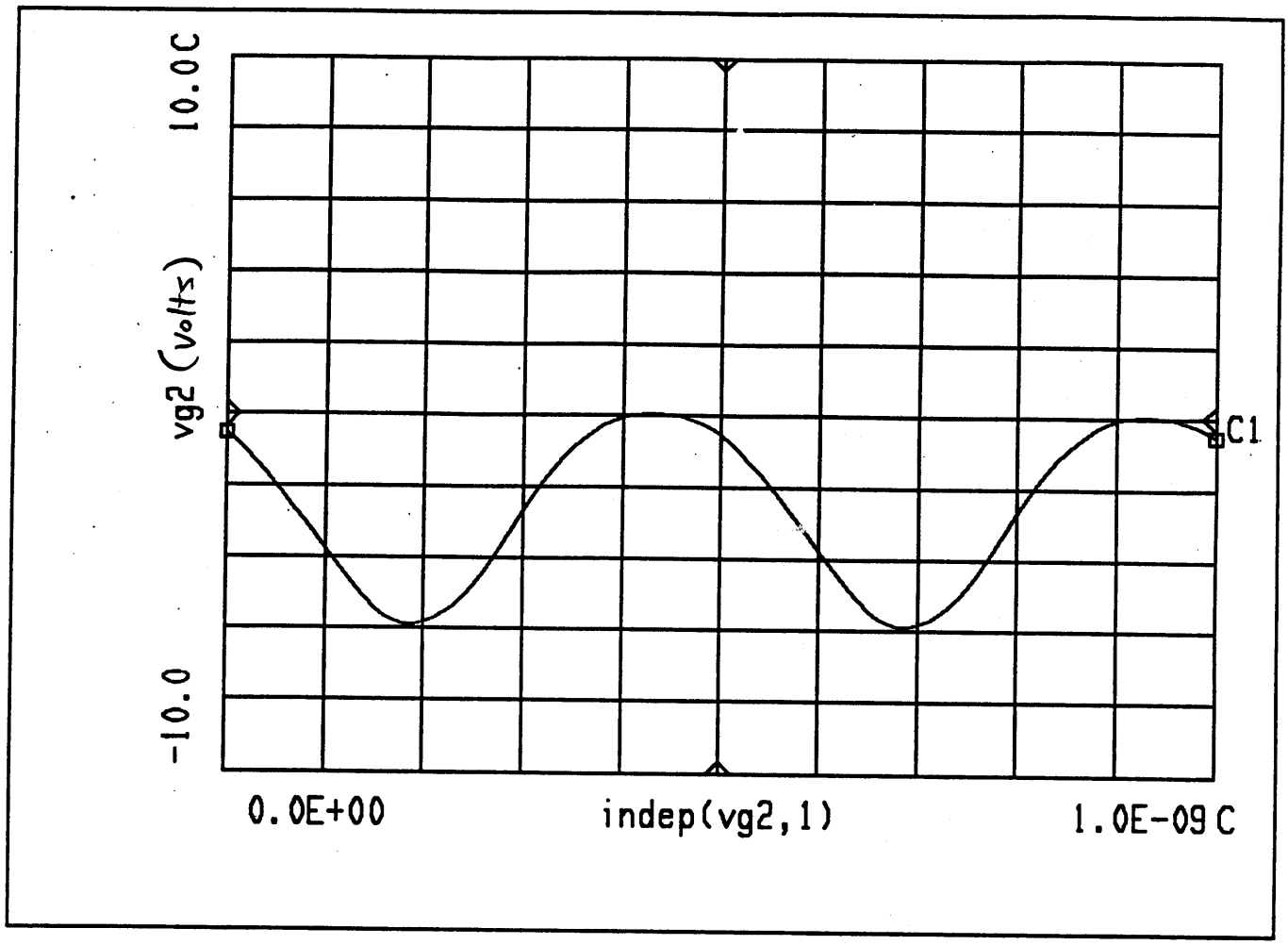

Figure 7: Gate voltage waveform for the output-stage MESFET. Notice the flattened top.

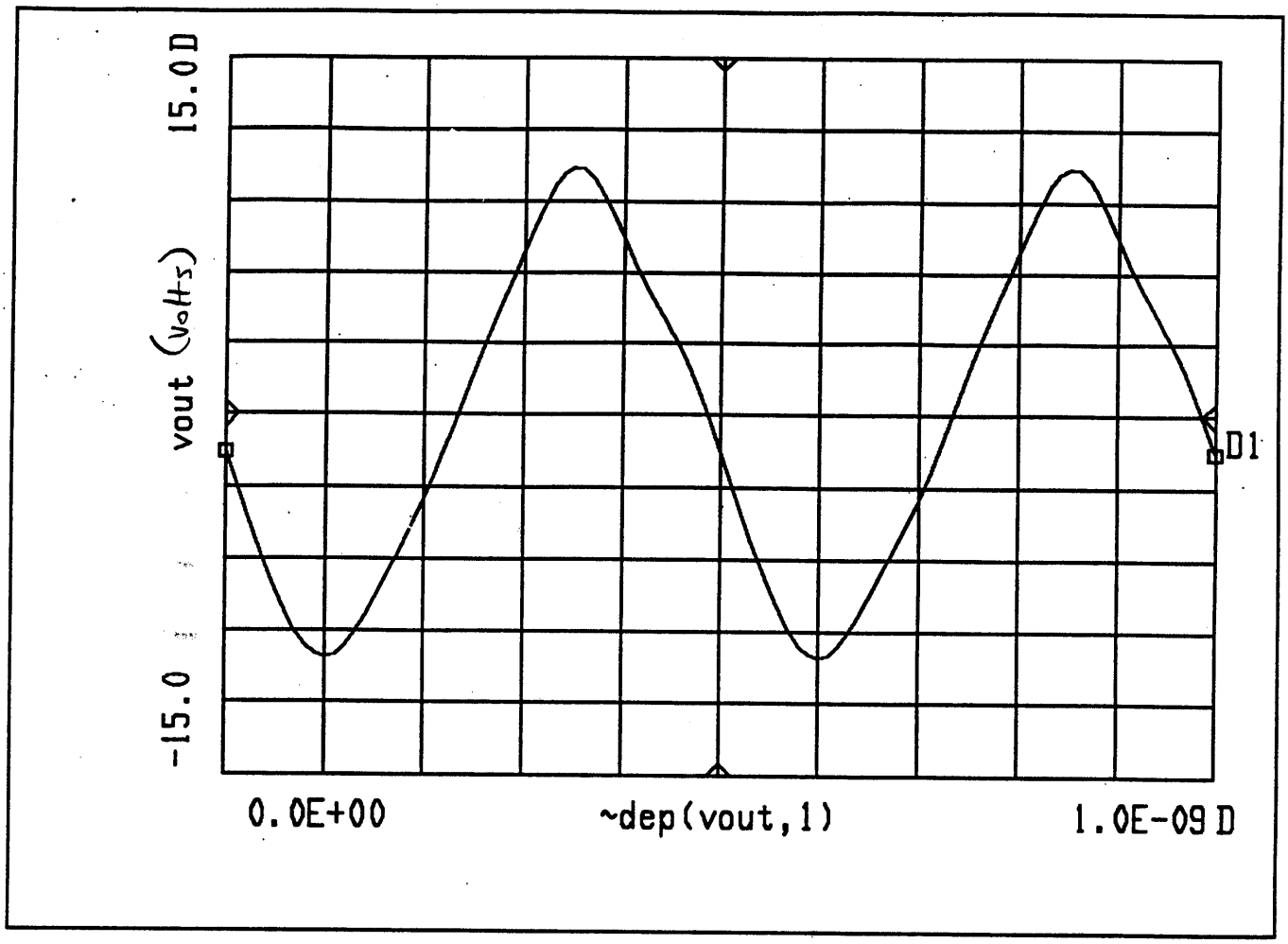

Figure 8: Output voltage waveform for the new CPW class E amplifier. The second harmonic is -59 dBc and the third harmonic is -23 dBc.

The Class E Amplifier–An Exact Solution

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1 Introduction

This is a short writeup documenting the exact solution of an ideal class E amplifier. The exact solution requires the solution of a fifth-order system of differential equations. Scott Bundy originally solved the system in Spring of 1992, and Mathematica was used to verify the results, as well as to plot curves of various voltages and currents throughout the circuit.

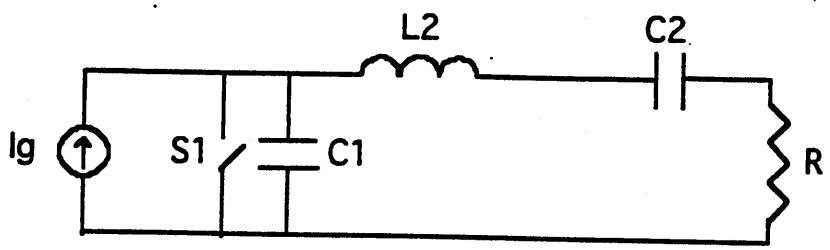

Figure 1: Class E high-efficiency amplifier circuit

2 Switched-Mode Analysis–Differential Equations

The class E circuit analyzed here is shown in Figure 1. The equations are originally written for the voltage across the capacitor C_2, and they are later converted to switch voltage and output voltage. Since the switch voltage is zero during half of the cycle, it cannot be used to describe the system for the entire cycle. Also, it is inconvenient to use output voltage to solve the system, since the output voltage is nearly sinusoidal in a correctly-designed class E circuit, and mathematically it is difficult to recover the switch voltage waveform from it. Specifically, an integration must be performed upon the output voltage in order to recover the switch voltage waveform. It is easier to differentiate the switch voltage to get the output voltage. The equations for the two half-cycles for V_{C_2} are given below:

$$(0 < t < T_s/2): \frac{d^3V_{C_2}}{dt^3} + \frac{R}{L_2}\frac{d^2V_{C_2}}{dt^2} + \frac{1}{L_2}\left(\frac{1}{C_1} + \frac{1}{C_2}\right)\frac{dV_{C_2}}{dt} = \frac{I_g}{C_1C_2L_2}$$

$$(T_s/2 < t < T_s): \frac{d^2V_{C_2}}{dt^2} + \frac{R}{L_2}\frac{dV_{C_2}}{dt} + \frac{V_{C_1}}{L_2C_2} = 0$$

And the boundary conditions on V_{S_1} (the switch voltage waveform) are:

$$V_{S_1}(0) = 0$$

$$V_{S_1}(\frac{T_s}{2}) = 0$$

$$\frac{dV_{S_1}}{dt}(\frac{T_s}{2}) = 0$$

3 General Solution of Equations

The general solution for this class E amplifier circuit is given below. Keep in mind that K_1, K_2 and K_3, as well as A_1 and A_2, are complicated functions of the circuit parameters (the circuit elements and the switching period):

$$(0 < t < T_s/2): V_{C_1}(t) = K_1 + \frac{I_g t}{C_1 + C_2} + K_2 \exp^{\frac{-tR}{2L_2}} \sin(t\sqrt{\frac{C_1 + C_2}{C_1C_2L_2} - (\frac{R}{2L_2})^2}) + K_3 \exp^{\frac{-tR}{2L_2}} \cos(t\sqrt{\frac{C_1 + C_2}{C_1C_2L_2} - (\frac{R}{2L_2})^2})$$

$$(T_s/2 < t < T_s): V_{C_1}(t) = A_1 \exp^{\frac{-tR}{2L_2}} \sin(t\sqrt{\frac{1}{C_2L_2} - (\frac{R}{2L_2})^2}) + A_2 \exp^{\frac{-tR}{2L_2}} \cos(t\sqrt{\frac{1}{C_2L_2} - (\frac{R}{2L_2})^2})$$

As was mentioned above, the parameters K_1, K_2, K_3, A_1 and A_2 are complicated functions of the circuit parameters. They are given here:

$$K_1 = \frac{I_g}{C_1 + C_2}\frac{K_{1n}}{K_{1d}}$$

$$K_{1n} = \frac{T_s}{2}\sqrt{\frac{C_1 + C_2}{C_1C_2L_2} - (\frac{R}{2L_2})^2}\cot(\frac{T_s}{2}\sqrt{\frac{C_1 + C_2}{C_1C_2L_2} - (\frac{R}{2L_2})^2}) - \frac{RT_s/2}{2L_2} - 1$$

$$K_{1d} = \sqrt{\frac{C_1 + C_2}{C_1C_2L_2} - (\frac{R}{2L_2})^2}\exp^{\frac{-RT_s}{4L_2}}(\sin(T_s/2\sqrt{\frac{C_1 + C_2}{C_1C_2L_2} - (\frac{R}{2L_2})^2}) +$$

$$\cos(T_s/2\sqrt{\frac{C_1+C_2}{C_1C_2L_2}-(\frac{R}{2L_2})^2})\cot(T_s/2\sqrt{\frac{C_1+C_2}{C_1C_2L_2}-(\frac{R}{2L_2})^2}))-$$
$$\sqrt{\frac{C_1+C_2}{C_1C_2L_2}-(\frac{R}{2L_2})^2}\cot(T_s/2\sqrt{\frac{C_1+C_2}{C_1C_2L_2}-(\frac{R}{2L_2})^2})+\frac{R}{2L_2}$$

$$K_2=K_1(\cot(T_s/2\sqrt{\frac{C_1+C_2}{C_1C_2L_2}-(\frac{R}{2L_2})^2})-\exp^{\frac{RT_s}{4L_2}}\csc(T_s/2\sqrt{\frac{C_1+C_2}{C_1C_2L_2}-(\frac{R}{2L_2})^2}))-$$
$$\frac{I_gT_s}{2}\frac{\exp^{\frac{RT_s}{4L_2}}}{\sin(T_s/2\sqrt{\frac{C_1+C_2}{C_1C_2L_2}-(\frac{R}{2L_2})^2})(C_1+C_2)}$$

$$K_3=-K_1$$

$$A_1=\frac{\frac{I_g}{C_2}(2L_2\sqrt{\frac{1}{C_2L_2}-(\frac{R}{2L_2})^2}\sin(\frac{T_s}{2}\sqrt{\frac{1}{C_2L_2}-(\frac{R}{2L_2})^2})\frac{1}{R}+\cos(\frac{T_s}{2}\sqrt{\frac{1}{C_2L_2}-(\frac{R}{2L_2})^2}))-B\exp^{\frac{RT_s}{4L_2}}}{(\frac{R}{2L_2}+2L_2(\frac{1}{C_2L_2}-(\frac{R}{2L_2})^2)\frac{1}{R})\sin(T_s/2\sqrt{\frac{1}{C_2L_2}-(\frac{R}{2L_2})^2})}$$

$$B=\frac{I_g}{C_2}-\frac{C_1}{C_2}(\frac{I_g}{C_1+C_2}+K_2\sqrt{\frac{C_1+C_2}{C_1C_2L_2}-(\frac{R}{2L_2})^2}-\frac{K_3R}{2L_2})$$

$$A_2=\frac{2L_2}{R}(A_1\sqrt{\frac{1}{C_2L_2}-(\frac{R}{2L_2})^2}-\frac{I_g}{C_2})$$