Graphene-Semiconductor Heterojunctions and Devices

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Graphene-semiconductor heterojunctions and devices

by

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Graphene-semiconductor heterojunctions and devices
written by Tzu-Min Ou
has been approved for the Department of Electrical, Computer, and Energy Engineering

Prof. Bart Van Zeghbroeck

Date

The final copy of this thesis has been examined by the signatories, and we find that both the content and the form meet acceptable presentation standards of scholarly work in the above mentioned discipline.
In this thesis we explore the potential of versatile graphene-semiconductor heterojunctions in photodetection and field-effect transistor (FET) applications.

The first part of the thesis studies near-infrared photodiode (NIR PD) based on a graphene-\textit{n}-Si heterojunction in which graphene is used as the absorbing medium. Graphene is chosen for its absorption in NIR wavelengths to which Si is not responsive. Most graphene detectors in the literature are photoconductors that have a high dark current. The graphene-Si heterojunction PD has a large Schottky barrier height that suppresses the dark current and enhances the current rectification and the photon detectivity.

The fabricated graphene-Si heterojunction PD under conventional telecommunication 1.3 (1.5)-\textmu m illumination exhibits a responsivity of 3 (0.2) mA/W, an internal quantum efficiency of 14 (0.6) %, a noise-equivalent power of 1.5 (30) pW/Hz$^{0.5}$, and a specific detectivity of $3 \times 10^9$ cm$^{-1}$Hz$^{0.5}$/W. An unexpected tunnel oxide is observed at the graphene-Si interface, further reducing the dark current. The performance in terms of sensitivity and noise is comparable to the commercially available discrete germanium NIR PDs due to its low dark current density on the order of 10 fA/\textmu m$^2$. The Si CMOS-compatible PD based on graphene-Si heterojunction provides a promising route to realize a critical component for monolithically integrated Si photonic interconnects.

The second part of the thesis focuses on a novel graphene junction FET (GJFET) gated by a graphene-semiconductor heterojunction. The majority of graphene transistors in the literature—including MOSFETs, barristors, and tunneling FETs—have a heavily-doped Si back gate separated from the graphene channel by a conventional or high-K dielectric layer. The threshold voltage of individual transistors cannot be tuned easily in such designs, and have an additional problem with shorted back gates. In GJFETs, a Schottky junction is formed as graphene is placed on a semi-
conductor, resulting in a depletion region inside the semiconductor that induces a complementary charge in the graphene. Changing the reverse bias across the graphene-semiconductor junction modulates the depletion region width and thereby changes the total charge in graphene. The charge density of the graphene is also modulated by the doping density of the semiconductor substrate. The GJFET structure provides a solution for Dirac voltage tuning and back gate isolation by location-specific doping on a single device wafer.

A detailed understanding of the device is obtained through the design, fabrication, and analysis of GJFETs with atmospheric pressure chemical-vapor deposited graphene on n-type Si and 4H-SiC substrates of various doping densities. A variable depletion width model is built to numerically simulate the performance. A representative n-Si \((4.5 \times 10^{15} \text{ cm}^{-3})\) GJFET exhibits an on-off ratio of 3.8, an intrinsic hole density of \(8 \times 10^{11} \text{ cm}^{-2}\), and a Dirac voltage of 14.1 V. Fitting the transfer characteristic of the Si GJFET with our device model yields an electron and hole mobility of 300 and 1300 \(\text{cm}^2/\text{V} \cdot \text{s}\) respectively. The tunability of the threshold voltage by varying the substrate doping density is also demonstrated. With an increasing substrate doping from \(8 \times 10^{14}\) to \(2 \times 10^{16} \text{ cm}^{-3}\), the threshold of the Si GJFET decreases from 24.9 V to 3.8 V. With even higher doping density \((5 \times 10^{18} \text{ cm}^{-3})\) in \(n^+\)-4H-SiC, the Dirac voltage of the GJFET is further reduced to 1.5 V. These results also demonstrate the feasibility of integrating GJFET with semiconductor substrates other than Si, widening their potential for use in high-frequency electronics.
Dedication

To my family for their unwavering support.
Many people have contributed to the completion of this thesis in direct and indirect ways. I owe each of them a great debt of gratitude. I would like to thank my advisor, Dr. Bart Van Zeghbroeck, for all the insightful discussions and for providing me the facility that makes this thesis possible. I would like to thank all the CNL/NCF staff, especially Jan Van Zeghbroeck and Tomoko Borsa, who helped maintain the functioning of the equipment and facilitates the research in this thesis. I would like to thank my colleagues and friends, Dr. Zefram Marks, Dr. Joshua ford, and Ian Haygood for their companionship. I also would like to thank all my past mentors who have guided me to this day. Finally, my special thanks go to Dr. Deborah Keyek-Franssen and her family for treating me like a member of their own.
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Chapter 1

Introduction

Semiconductor devices are the basic components that constitute the most intricate electronic systems with diverse functionalities. The advance of semiconductor devices has been the main driving force behind the electronic industry since the mid-20th century, making it the largest industry in the world today. In order to sustain this nonstop improvement and meet the growing demand for emerging applications, new materials are being discovered and novel semiconductor device structures are being invented. Graphene is one of those new materials and stands out among all known semiconductors due to its unique energy band structure and ease of preparation. Its extraordinary electronic properties, such as high carrier mobility and high carrier saturation velocity, have great potentialities for (opto-)electronics, especially in high-frequency applications. However, even though there is a lot of research being conducted on graphene itself, the graphene-semiconductor heterojunctions—and the devices based on this structure—are seldom studied. The motivation and scope of this Ph.D. thesis lies in the exploration of a novel structure—a graphene-semiconductor heterojunction for device applications. By incorporating graphene with conventional semiconductors, new device functionalities are expectable given the physics of the unique heterojunction.

Chapter 1 (this chapter) reviews the material properties of graphene as well as some other selected semiconductors. The important findings and devices from literature on the graphene-semiconductor heterojunctions are also introduced. Finally, the novel devices based on this heterojunction are described in detail. These include a graphene-silicon infrared photodiode (IR PD) and a three-terminal device that is devised in this thesis—a graphene junction field-effect transistor
The unprecedented functionality of the GJFET’s tunable Dirac voltage, as opposed to that of traditional graphene transistors, is also introduced.

Chapter 2 analyzes the GJFETs from theoretical point of view. The properties of graphene for calculation and the device models are described. The results predicting the performance of the GJFET are obtained by numerical simulation and discussed.

Chapter 3 provides the details of the device fabrication process. Analysis techniques for the material and the devices are also introduced.

Chapter 4 studies the foundation of a GJFET—the graphene-semiconductor heterojunction. The experimental results are obtained from graphene-silicon Schottky-like diodes. The performance of graphene-silicon heterojunction IR PD is also evaluated and analyzed.

Chapter 5 demonstrates the GJFETs. The experimental data for a graphene MOSFET on silicon and GJFETs on both silicon and silicon carbide are presented and compared. The tunable Dirac voltage predicted by simulation is also tested.

Chapter 6 summarizes the main findings from the experiment and the key points derived from the discussions.

Chapter 7 concludes this thesis.
1.1 Background of semiconductor materials

In this section, the material properties of selected semiconductors are introduced. These include graphene: the target material in this thesis, silicon: the mainstream semiconductor, and silicon carbide: interesting because of its superior band structure for GJFET applications and for epitaxial graphene growth.

1.1.1 Graphene

As a relatively young semiconductor (discovered in 2004), graphene is the first thermodynamically stable, atomically-thin material obtained in human history [1]. Its discovery and its extraordinary properties have proven to be of great interest to both scientific and industrial communities. Intensive research efforts on graphene arose worldwide, known as graphene gold rush, which also inspired the exploration of other two-dimensional (2D) electronic materials, such as phosphorene [2, 3], metal dichalcogenides [4–6], etc., providing great potential for research and various applications.

The extraordinary properties of graphene stem from its simple crystal structure shown in Fig. 1.1a. Graphene is composed exclusively of carbon atoms. Each carbon atom in graphene bonds covalently with another three atoms with 120° between adjacent σ-bonds on a 2D plane. The resultant crystal structure is a single atomic layer, creating a perfect hexagonal honeycomb lattice. The distance between nearest carbon atoms is 1.42 Å, and the distance between the second nearest ones is 2.46 Å, which is also the lattice constant of graphene. The compact lattice structure makes graphene completely impervious to all gases and liquid molecules. The remaining fourth electronic orbital of each carbon atom, which stands perpendicular to the plane, forms a π-bond with that from an adjacent carbon atom. It is these delocalized electrons in π-bonds that play the critical role in making graphene a semiconducting layer, along which the electrons and holes can move freely.
(a) Graphene—hexagonal

(b) Si—cubic

(c) 4H-SiC—Wurtzite

(d) 3C-SiC—Zinc blende
Due to the strong $\sigma$-bonds joining the adjacent carbon atoms, graphene has extreme mechanical properties. It has the highest known intrinsic tensile strength of 130 GPa and Young’s modulus of 1 TPa [7], making it the strongest material ever obtained in human history. When mixed with other substances, even at a very low weight fraction, graphene significantly increases the mechanical strength of the matrix material and suppresses cracking [8]. The enhancement from mixed graphene even outperforms its carbon nanotube (CNT) counterpart due to the much larger surface-to-volume ratio and its 2D nature. Those properties make graphene an interesting material for a wide range of applications, such as in nano and micro-electro-mechanical systems (N/MEMS).

Superlubricity is another property that has great potential for mechanical applications. The interaction between adjacent graphene sheets is dominated by van der Waal forces—as in graphite. Because of this weak adhesion, graphite has long been used as a solid lubricant. Moreover, research shows that the friction can be eliminated at the microscale in graphene-to-graphene interfaces [9]. When the lattices of adjacent graphene layers are in incommensurable contact, the friction
vanishes—an ideal property for N/MEMS applications.

In terms of thermal properties, graphene still gives the ultimate performance. The suspended single-layer graphene has a room-temperature thermal conductivity of \( \sim 50 \text{ W/cm-K} \) [10]—about 130 times that of copper, 5 times that of graphite and diamond’s (both \( \sim 10 \text{ W/cm-K} \)), and 1.4 times that of a CNT. The superior thermal conductivity comes from the isotropic ballistic thermal conductance within the plane, which is dominated by phonons. This extraordinary thermal conductivity is ideal for electronic applications.

1.1.1.2 Chemical properties

Graphene has high chemical reactivity due to its ultra-high surface-to-volume ratio. Every carbon atom in the graphene lattice is exposed for chemical reaction on both sides of the plane. Also, carbon atoms on the edge and at the lattice defects of graphene are more chemically reactive due to the unbonded electrons. When additional atoms or molecules adhere to graphene, graphene’s electronic structure is altered because either the lattice symmetry is broken or the \( \pi \)-electron is now used for bonding. The resultant charge transfer is referred to as chemical doping of graphene. Chemical doping alters the properties of graphene, e.g. the electrical conductivity or optical absorption, etc., and therefore graphene is a potential material for chemical sensing applications.

1.1.1.3 Electronic properties

As mentioned earlier, \( \pi \)-electrons play a critical role in determining the electronic properties of graphene. The periodic honeycomb lattice of graphene splits the energy levels of \( \pi \)-bond orbitals into two energy bands. The bonding \( \pi \)-electrons with lower energy constitute the valence band, and the anti-bonding \( \pi^* \)-electrons with higher energy form the conduction band. The cone-shaped conduction and valence bands contact each other at a single point; this point is referred to as the **Dirac point**, and the conduction and valence bands are called Dirac cones. A detailed calculation of the electronic band structure of graphene is provided in [11], and the band structure of graphene
is shown in Fig. 1.2. This unique electronic band structure makes graphene a zero bandgap semiconductor. Moreover, intriguing electronic and optical properties arise because of this perfectly symmetrical head-to-head cone-shaped energy bands.

The most interesting electronic property in terms of transistor applications is graphene’s low Density of States (DoS) close to the Dirac point. The DoS of graphene is directly proportional to the energy difference from the Dirac point as a result of the linear dispersion relation, yielding numbers on the order of $0–10^{14}$ cm$^{-2}$ within an electron volt from the Dirac point. This low DoS allows the carrier (electron or hole) density to be easily modulated by an external structure, such as a dielectric capacitor [1], or by chemical doping as mentioned in 1.1.1.2. As carrier density changes, so too does the position of graphene’s Fermi level relative to the Dirac point. The process that changes the carrier density is called doping, as in traditional semiconductors. This phenomenon is visualized in Fig. 1.3. This property differentiates graphene from a semi-metal, whose conduction and valence bands are in contact or partially overlapped, resulting in a much larger DoS and a fixed Fermi level.

Figure 1.2: Energy band structure of graphene in the first Brillouin zone. Dirac cones (conduction and valence bands) are in contact with each other at the Dirac points.
1.1.1.4 Doping density

There are many factors that can change the doping of graphene. Unintentional doping can come from chemical contamination from the growth/transfer process, the surface properties of the substrate such as dangling bonds, the external environment to which the graphene is exposed, etc. It has been shown that oxygen molecules in ambient air serve as a $p$-type dopant to graphene, and this $p$-doping is enhanced by water vapor in the air [12]. The doping from air is a reversible process where graphene can be de-doped by thermal annealing in vacuum. In addition to doping from air, graphene normally shows $p$-type doped behavior after being placed on SiO$_2$ surface.

Intentional doping can be implemented by chemical functionalization, adding material onto graphene, or by metal contacts, electric fields, etc. For example, $n$-doping of graphene can be achieved by annealing graphene sheets in gaseous NH$_3$ environment [13]. This chemical $n$-doping is also a reversible process that can be undone by vacuum annealing. The most widely used intentional doping method is electric field-effect doping. The electric field effect can alter graphene’s carrier density up to few $10^{13}$ cm$^{-2}$, as opposed to undoped graphene whose intrinsic carrier density is only about $8\times10^{10}$ cm$^{-2}$ for both holes and electrons at room temperature. This approximately two-orders-of-magnitude modulation of carrier density by the electric field, combined with the high carrier mobility introduced in the following section, is what makes graphene a potential candidate as a FET channel material.

![Energy band structure of graphene under different doping conditions.](image)

Figure 1.3: Energy band structure of graphene under different doping conditions.
1.1.1.5 Carrier mobility of graphene

The dispersion relation for typical semiconductors at the extreme points of the energy bands is approximately parabolic. Therefore the effective mass of the carriers \( m^* = \frac{\hbar^2}{(d^2 E/dk^2)} \), where \( d^2 E/dk^2 \) is the curvature of the dispersion curve, yields a non-zero value. The general trend is inversely proportional: the smaller the \( m^* \), the higher the carrier mobility. Because of graphene’s linear dispersion relation in the vicinity of the Dirac point, both the electrons and holes in graphene behave as massless Dirac fermions (\( m^* = 0 \)). Because of this behavior, the carriers in graphene have extraordinarily high mobility, making it an exceptional candidate material for electronic devices, especially with respect to high-speed applications.

Carrier mobility of graphene can be affected by many factors, such as temperature, cleanliness, grain size, carrier density, defect density, ripples in the sheets, number of layers, edges, the interaction with the substrate, etc; therefore, the maximum carrier mobility was obtained in exfoliated, suspended graphene with the lowest defect density and no perturbation from the substrate, and an electron and hole mobility well above \( 1 \times 10^6 \text{ cm}^2/\text{V-s} \) under low carrier densities (\( 1 \times 10^{10} \text{ cm}^{-2} \)) at 15 K was recorded [14]. At room temperature, the theoretical limit of graphene’s carrier mobility is about \( 2 \times 10^5 \text{ cm}^2/\text{V-s} \) at carrier densities on the order of a few \( 10^{12} \text{ cm}^{-2} \) [15, 16]. This predicted high mobility is experimentally obtained at room temperature; \( 2.5 \times 10^5 \text{ cm}^2/\text{V-s} \) was recorded by Hall measurement on exfoliated graphene sandwiched in hexagonal boron nitride (h-BN) sheets [17] under a low carrier density of about \( 10^{11} \text{ cm}^{-2} \). All of the maximal values mentioned previously have been obtained on exfoliated samples because the graphene cleaved from graphite has the least number of defects. However, from a practical point of view, exfoliation is not a viable technology for industry-scale production. The graphene produced by chemical vapor deposition (CVD) is therefore of greater interest.

For CVD graphene transferred onto \( \text{SiO}_2 \) and hexagonal boron nitride surfaces, the carrier mobility maxima obtained at room temperature are 1.6 and \( 3 \times 10^4 \text{ cm}^2/\text{V-s} \), respectively [18, 19]. However, the more commonly obtained hole mobility value for CVD graphene on \( \text{SiO}_2 \) is a single
order of magnitude smaller, while the electron mobility is even further decreased by an additional factor of 2 to 6. This lower value can be attributed to non-optimized growth and transfer processes. The mobility disparity between hole and electron is commonly observed in CVD graphene FETs and attributed to the $p$-$n$ junctions at the metal contacts, but the exact cause is still unknown.

The case for epitaxial graphene grown on hexagonal silicon carbide is different from that of transferred CVD-grown graphene. The surface polarity of the silicon carbide substrate, i.e. C- or Si-face, plays an important role in determining the electronic properties of epitaxial graphene. The maximum recorded carrier mobility for multilayer epitaxial graphene measured at 300 K is 5800 cm$^2$/V·s on the Si-face and $1.5 \times 10^5$ cm$^2$/V·s on the C-face [20].

Epitaxial graphene is attractive for high-speed electronics due to the advantage that its high carrier mobility is obtainable on a semi-insulating (SI) substrate. IBM has shown the great potential of epitaxial graphene FETs on the Si-face of a 2” 4H-SiC substrate: with a 240nm gate length and a 10nm thick atomic-layer deposition (ALD) HfO$_2$ dielectric gate, the graphene top-gated MOSFET demonstrated a unit current gain cut-off frequency ($f_T$) of 100 GHz [21], outperforming state-of-the-art Si MOSFETs of the same gate length ($f_T \sim 40$ GHz). Even higher $f_T$ and $f_{MAX}$ have been demonstrated with epitaxial graphene [22, 23], showing its potential for high-frequency electronics. The corresponding field-effect mobility is around 900–1400 cm$^2$/V·s after gate dielectric deposition by ALD (1000–1500 cm$^2$/V·s before ALD). The performance is expected to be further enhanced with optimized epitaxial graphene growth and improved gate dielectric material selection and deposition.

1.1.1.6 Optical properties

Graphene’s zero bandgap and the perfectly symmetrical energy band structure result in its extraordinary optical properties. In theory, a single layer of graphene absorbs $\pi \alpha \approx 2.3\%$ of light regardless of wavelength, where $\alpha$ is the fine-structure constant. This universal absorption has been experimentally demonstrated on suspended exfoliated graphene [24]: each graphene layer absorbs $\sim 2.3\%$ of normally incident light regardless of wavelength in the visible spectrum (400–750 nm).
The 2.3% absorption is quite significant considering that graphene is only one-atom thick, i.e. 0.34 Å in thickness.

\[ E = h\nu - \frac{E}{2} + \frac{E}{2} \]

Figure 1.4: Mechanism of graphene’s optical absorption. Left: undoped graphene. Middle: \( p \)-doped graphene. Right: \( n \)-doped graphene.

The optical absorption of graphene can be influenced by its doping condition. Fig. 1.4 shows the mechanism of graphene’s optical absorption under three different doping conditions. The conduction and valence bands are shown as Dirac cones with the red (white) regions indicating filled (empty) electronic states, and blue arrows represent photon absorption paths. In the first scenario where graphene is undoped (\( E_F \) stays at the Dirac point), its valence band is completely filled by electrons and the conduction band is empty. In this case, incident photons with any energy will be absorbed because of the availability of both electron in the valence band and empty states in the conduction band. The excited electron jumps vertically into an available state in the conduction band. The second scenario is when graphene is \( p \)-type doped. In this case, low-energy photons is transparent to graphene because no electron is available at the top end of the valence band, resulting in no optical absorption. And the last scenario is when graphene is \( n \)-type doped. The lack of empty states at the bottom of the conduction band prevents the absorption of low-energy photons (Pauli blocking). Based on this mechanism, the optical absorption/transmission of low-energy photons can be modulated by shifting the Fermi level of graphene, and active optical devices such as optical modulators in fiber communication wavelength are demonstrated [25].
1.1.1.7 Single-layer vs. multi-layer graphene

The term graphene conventionally refers to a single-layer graphene (SLG) as opposed to a multi-layer graphene (MLG). The number of graphene layers has profound influence on the electronic band structure. The extreme case of MLG is the bulk graphite. In graphite, the component graphene layers stack up in an interlocking order by weak van der Waal force, as shown in Fig. 1.1a. Graphite is considered metallic with excellent electrical conductivity along the plane of layers. When the number of graphene layers decreases to just a few, the electronic property becomes very different from graphite.

The properties of SLG are introduced in previous sections. The lack of an intrinsic bandgap prohibits the use of SLG in traditional MOSFET structure as a switch for digital circuits. Lots of efforts were devoted to create a bandgap in SLG, such as narrowing down the width of graphene sheets to form graphene nano-ribbons (GNRs) [26], by using special substrates [27,28], or by adding molecules in a spatially periodic order [29]. Nonetheless, those methods either require precise control of the width and the type of the edge of GNRs, or the fabrication is incompatible to conventional microfabrication process. As a result, a more viable way to induce a bandgap is by using bi-layer graphene (BLG). It has been shown theoretically that BLG has parabolic-shaped conduction and valence bands with zero bandgap under no external perturbation. When an electric field is applied to the plane of BLG vertically, an energy bandgap up to 250 meV can be induced depending on the strength of the electric field [30]. Despite of the bandgap, the challenges for BLG application from a practical point of view remains in the controlable production of large-area and uniform bilayers.

1.1.1.8 Graphene in-situ characterization—Raman spectroscopy

Raman spectroscopy has become the most widely used technique to examine the quality of graphene after production owing to its fast and nondestructive nature [31]. By detecting the energy shift of outcoming radiation with respect to the incident light, Raman spectroscopy probes the atomic structure as well as the electronic properties of the sample by electron-phonon interaction.
Each peak in Raman spectrum is related to a specific mode of lattice vibration. Its position, width, intensity, area, and dispersion—the position of the peak as a function of the incident photon energy—provide abundant information of graphene on the number of layers, doping level, edges, strain and stress, defects, chemical modifications, etc.

Typical Raman spectra is shown in Fig. 1.5 where a pristine, free-of-defect graphene shows only strong G and 2D peaks. The G peak comes from one-phonon process where the electron couples with the high-frequency phonon mode that two sublattices of graphene moves in opposite directions within the plane, as shown in Fig. 1.6. This one-phonon process involves no momentum change and can be suppressed by doping, leading to a higher G peak intensity for higher doping level in graphene [31]. The 2D peak corresponds to the case where electrons and holes are backscattered in opposite directions, subsequently generating two phonons with opposite wave vectors. This process does not need any defect to activate, and thus 2D peak always appears in Raman spectrum of graphene. 2D peak is sensitive to the number of graphene layers, the electronic band structure, and the orientation between layers.

On the other hand, the graphene with defects shows a series of defect-activated peaks in addition to the original peaks. With structural defects in graphene—such as holes, cracks and edges—the lattice-breathing modes (LBMs, shown in Fig. 1.6) are activated. LBMs correspond to the formation of a strong D peak. This D peak is strongly dispersive with excitation photon energy.

The graphene’s quality can thus be assessed by comparing the shapes, intensities, and the peak positions of the Raman spectra.
Figure 1.5: Example Raman spectra of pristine (black) and defected (red) graphene.

Figure 1.6: Left: The lattice vibrating mode corresponding to G peak formation. Middle: The Raman process of G peak. Right: Lattice-breathing modes corresponding to D and other defect-activated peaks.
1.1.2 Silicon (Si)

Silicon is the dominating semiconductor in electronic industry. It is also the most widely used substrate for graphene device fabrication. It has a cubic lattice (Fig. 1.1.2) where each Si atom bonds with another three in a tetrahedral order. Its properties are often compared as the baseline with other semiconductors.

Silicon has an indirect bandgap of 1.12 eV at 300 K with an electron affinity of 4.05 eV. Its relative dielectric constant is 11.9. The breakdown field in general is about $3 \times 10^5$ V/cm. The intrinsic carrier density of silicon is about $10^{12}$ cm$^{-3}$ with bulk electron mobility of $\sim 1450$ and hole mobility of $\sim 500$ cm$^2$/V·s. The biggest advantage that silicon provides is the capability of being oxidized to form a layer of high-quality amorphous silicon dioxide (SiO$_2$) with very low density of interfacial defects. This SiO$_2$ layer has a bandgap of 8.9 eV, a relative dielectric constant of 3.9, and a breakdown field of about 6 MV/cm. It has very good insulating property in terms of pinhole densities and it is easy to fabricate.

Silicon dioxide on silicon (SiO$_2$/Si) is the predominant substrate for graphene device fabrication. Graphene with different number of layers can be visualized under the optical microscope—which is the fastest and nondestructive method to directly observe graphene on a device substrate. It was found that the optical contrast of graphene sheets placed on SiO$_2$/Si substrate can be described by Fresnel law [32]. The thickness of SiO$_2$ can be optimized so that the opacity of graphene sheets becomes maximum. Using Fresnel equations, the optical contrast of graphene on both SiO$_2$ and Si$_3$N$_4$ on silicon substrate are calculated and the results are shown in Fig. 1.7.

The optical contrast of graphene is a function of the wavelength of light and the thickness of the dielectric layer. The highest optical contrast at the middle of visible spectrum (i.e. green $\sim 500$–550 nm) is obtained when SiO$_2$ thickness is 90 and 275 nm, which is why most of the graphene devices are made on Si wafers with $\sim 300$-nm-thick SiO$_2$. It is also worth mentioning that Si$_3$N$_4$ provides better contrast for graphene even though the optimum thickness is different from that on SiO$_2$ and the optimum band is slightly narrower. Also in Fig. 1.7 the Z-scale (the contrast) is
1.1.3 Silicon carbide (SiC)

Silicon carbide is potential for graphene device fabrication because it is a substrate for high-speed electronics and graphene can be grown on it directly. Silicon carbide has several polytypes (same compound with different crystal structures in only one direction), e.g. 4H-SiC, 6H-SiC, 15R-SiC, and 3C-SiC. All polytypes have different bandgaps, but the valence band edges are found to be at the same level [33]. Among the various polytypes, 4H-SiC and 3C-SiC are of interest to the graphene device applications explained as follows.

4H-SiC has a hexagonal lattice structure as shown in Fig 1.1c. It has a larger bandgap of 3.23 eV, an electron affinity of 3.2 eV, electron and hole mobility of about 900 and 120 cm$^2$/V·s respectively at 300 K, a thermal conductivity of about 3.7 W/cm-K, and a breakdown fields of about 3–5 MV/cm) [34]. For these reasons, 4H-SiC has outstanding current-carrying capability and heat dissipation. Another advantage 4H-SiC’s wide bandgap provides is that the semi-insulating
substrate can be used to fabricate high-speed devices.

A high quality SiO$_2$ layer can also be thermally grown by oxidizing 4H-SiC surfaces. Graphene can be visualized on 4H-SiC substrate with a specific SiO$_2$ thickness, facilitating the fabrication of graphene devices. The calculated optical contrast of graphene on different dielectric layers (SiO$_2$ and Si$_3$N$_4$) on 4H-SiC substrate are shown in Fig. 1.8. The optimum SiO$_2$ thickness for the highest graphene optical contrast is $\sim$70 nm under the green light (550 nm).

![Figure 1.8: Calculated optical contrast of graphene on different dielectric layer (SiO$_2$ and Si$_3$N$_4$) on a 4H-SiC substrate.](image)

3C-SiC has a cubic (zinc-blende) lattice structure as shown in Fig 1.1d, and it has been used as the raw material and substrate to grown graphene [35]. It has a bandgap of 2.36 eV at 300 K. The reduced interference from phonon—due to the higher symmetry of cubic lattice—yields a high electron mobility that is comparable to 4H-SiC and a much higher hole mobility (300 vs. 120 cm$^2$/V·s) [34]. Together with the fact that a native silicon oxide layer can be thermally grown, 3C-SiC has great potential for realizing CMOS architecture working at high temperature. Another advantage of 3C-SiC is its compatibility with silicon—3C-SiC can be epitaxially grown on silicon substrate [36]. This will greatly facilitate the integration of graphene with silicon-based systems on a single chip [37].
1.1.4 Other carbon-based semiconductors

In this section two related carbon-based semiconductors are introduced: diamond and the carbon nanotubes.

1.1.4.1 Diamond

Diamond is formed exclusively by carbon atoms in a tetrahedral order, forming a cubic lattice resembling silicon (Fig. 1.1.2). The covalent bond between carbon atoms is extremely strong and thus gives diamond its supreme physical, chemical, and mechanical properties. Without doping, diamond at 300 K has a bandgap of 5.5 eV, a breakdown field of up to 10 MV/cm, and a thermal conductivity of 10–20 W/cm-K [38]—making diamond a great electrical insulator and one of the best thermal conductors. Natural diamond was first found behaving as p-type semiconductor in 1952 with boron acting as deep acceptor (with an ionization energy of 0.37 eV) [39]. This activation energy can be reduced by increasing acceptor concentration beyond $3 \times 10^{19}$ cm$^{-3}$. At very high boron concentration ($> 10^{21}$ cm$^{-3}$) the activation energy approaches zero and diamond becomes metallic. On the other hand, the shallowest donor found in diamond so far is phosphorous with an ionization energy of 0.52 eV [40], making p-type semiconducting diamond difficult to obtain.

Diamond was once considered the most difficult substance to synthesize, but considerable progress has been made toward realizing diamond electronic devices. Small area, single crystal diamond thin film is grown homoepitaxially (i.e. on diamond substrate) by microwave-assisted chemical vapor deposition (CVD) on a high-pressure high-temperature synthetic diamond substrate [41]. The measured electron and hole mobilities are 4500 and 3800 cm$^2$/V-s respectively at room temperature. Large-area, wafer-sized diamond thin films can be grown heteroepitaxially by microwave plasma-enhanced CVD on various substrates [42]. The qualities of diamond produced this way are inferior to the homoepitaxial one. Albeit the remaining challenges, such as the lack of an n-type shallow dopant and an improved method to synthesize high quality thin films, diamond is still a prominent candidate of electronic material in high-temperature and high-power applications.
Carbon nanotube (CNT)

A carbon nanotube (CNT) is a seamless roll of a graphene sheet with a cylindrical shape and a diameter in nanometer scale as shown in Fig. 1.1e. CNTs can achieve an extremely high aspect ratio of several millions. For this reason CNTs are often considered as a one-dimensional material.

CNTs can be categorized as single-wall nanotubes (SWNTs) and multi-wall nanotubes (MWNTs) based on the number of coaxial nanotubes. MWNTs are a combination of coaxial SWNTs with different radii and lengths. The attractive interaction among SWNTs is van der Waal force as in graphite. Based on the chiral angle at which the graphene sheet rolls up, every SWNT can be characterized specifically by a set of indices \((n,m)\) [43]. The integers \(n\) and \(m\) refer to the number of unit vectors of the graphene honeycomb lattice. When \(n = m\), the SWNT is called armchair; when \(m\) or \(n = 0\), the SWNT is called zigzag; otherwise the SWNT is called chiral. The diameter of a SWNT can then be calculated based on its indices. The electronic properties of a SWNT depend significantly on the indices as well as the diameter. For example, armchair nanotubes are metallic. When \(n - m = \pm 3k\) (\(k\) is an integer), the SWNT is a small bandgap semiconductor; otherwise, the tube is a moderate semiconductor. The bandgap of a SWNT can vary from 0 to above 2 eV based on the diameter, and this behavior is described by Kataura plot as shown in Fig. 1.9. CNT can be mass-produced by several techniques—arc discharge, laser ablation, thermal plasma method, and CVD. Among which CVD is the most promising way for industrial-scale production because of its low production cost and controllable growth on specific substrates.

Just like graphene that has strong \(\sigma\)-bonds joining carbon atoms together and \(\pi\)-bonds contributing to the electrical and optical properties, CNTs also have desirable mechanical, thermal, and electrical properties due to its lattice structure. For example, CNTs are known to be one of the strongest and stiffest materials in its axial direction among any existing material, with a measured tensile strength of 11–68 GPa and Young’s modulus of 270–950 GPa [44], while being soft in the radial direction. The thermal conductivity of CNTs along the axis at room temperature is about 35 W/cm·K, about 9 times of copper [45], while being a good heat insulator in the radial direction (similar to that of soil) [46]. For electrical and electronic applications, metallic CNT can carry
Figure 1.9: Kataura plot describing the bandgap of metallic and semiconducting CNTs as a function of tube diameter.

A current density up to $4 \times 10^9$ A/cm$^2$ in theory, more than a thousand times than copper's current carrying capability while avoiding electromigration issues of metal [47]. This property makes metallic CNTs an ideal material for interconnects.

1.1.5 Comparison and table of properties of selected semiconductors

Table 1.1 concludes the properties of the semiconductors introduced in Chapter 1.
Table 1.1: List of material parameters and properties of the semiconductors introduced in Chapter 1.

<table>
<thead>
<tr>
<th></th>
<th>Graphene</th>
<th>Si</th>
<th>4H-SiC</th>
<th>3C-SiC</th>
<th>Diamond</th>
<th>CNT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Lattice system</strong></td>
<td>Hexagonal</td>
<td>Cubic</td>
<td>Hexagonal</td>
<td>Cubic</td>
<td>Cubic</td>
<td>Hexagonal</td>
</tr>
<tr>
<td><strong>Dielectric constant</strong></td>
<td>( \frac{\varepsilon_s}{\varepsilon_0} )</td>
<td>( \varepsilon_\perp = \sim 3^a ) [48]</td>
<td>11.9</td>
<td>( \varepsilon_\perp = 9.7 )</td>
<td>9.7</td>
<td>5.7</td>
</tr>
<tr>
<td></td>
<td>( \varepsilon_\parallel = \sim 1.8^a ) [48]</td>
<td>( \varepsilon_\parallel = 10 )</td>
<td>11.9</td>
<td>( \varepsilon_\parallel = 10 )</td>
<td>5.7</td>
<td>0 to &gt;2</td>
</tr>
<tr>
<td><strong>Bandgap (eV)</strong></td>
<td></td>
<td>0</td>
<td>1.12</td>
<td>3.23</td>
<td>2.36</td>
<td>5.5</td>
</tr>
<tr>
<td><strong>Bandgap type</strong></td>
<td>Direct</td>
<td>Indirect</td>
<td>Indirect</td>
<td>Indirect</td>
<td>Indirect</td>
<td>Direct</td>
</tr>
<tr>
<td><strong>Electron affinity (eV)</strong></td>
<td>4.57 [49]</td>
<td>4.05</td>
<td>3.2–3.4 [50–53]</td>
<td>3.8–4.0 [51–53]</td>
<td>varies(^b)</td>
<td>varies(^c)</td>
</tr>
<tr>
<td><strong>Electron mobility(^d) (cm(^2)/V·s)</strong></td>
<td>(2 \times 10^5) (^e)</td>
<td>1450</td>
<td>900</td>
<td>800</td>
<td>4500</td>
<td>&gt; 1 \times 10^5 [54]</td>
</tr>
<tr>
<td><strong>Hole mobility(^d) (cm(^2)/V·s)</strong></td>
<td>(2 \times 10^5) (^e)</td>
<td>500</td>
<td>120</td>
<td>320</td>
<td>3800</td>
<td>&gt; 1 \times 10^5 [54]</td>
</tr>
<tr>
<td><strong>Carrier saturation velocity (10(^7) cm/s)</strong></td>
<td>5.5 [55]</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>2 [56]</td>
</tr>
<tr>
<td><strong>Breakdown field (10(^5) V/cm)</strong></td>
<td>N/A</td>
<td>2.5–8</td>
<td>30–50</td>
<td>(\sim 10)</td>
<td>10–100</td>
<td>N/A</td>
</tr>
<tr>
<td><strong>Thermal conductivity (W/cm·K)</strong></td>
<td>50</td>
<td>1.3</td>
<td>3.6</td>
<td>3.7</td>
<td>10</td>
<td>35(^f)</td>
</tr>
<tr>
<td><strong>Young’s modulus (GPa)</strong></td>
<td>1000</td>
<td>130–170</td>
<td>448</td>
<td>748</td>
<td>1035</td>
<td>270–950</td>
</tr>
</tbody>
</table>

Note: All properties at 300 K.
\(^a\)Also depending on the substrate, see [57].
\(^b\)Depending the surface of diamond. Negative for hydrogen-terminated diamond, and positive for hydrogen-free surface. [58].
\(^c\)Depending on the chirality of CNT.
\(^d\)Bulk mobility at low doping density.
\(^e\)Theoretical limit.
\(^f\)Along the axis of CNT.
1.2 Graphene-semiconductor heterojunctions

The graphene described in this section refers to CVD-grown graphene which is subsequently transferred onto semiconductor substrates. The epitaxial graphene grown directly on semiconductor substrates such as silicon carbide is not included as the physics at the interface is more complicated and not yet fully understood.

From the theory of a metal-semiconductor junction, the energy band structures between two materials determines the rectifying characteristics of interface. Under thermal equilibrium, the Fermi levels of two materials align due to the charge transfer. The charge transfer results in a built-in electric field within the semiconductor, and thus causes its energy bands to bend. When the band bending forms an unsurmountable energy barrier to the carriers (either electron in the conduction band or hole in the valence band), the interface becomes rectifying and is called a Schottky junction as opposed to an ohmic junction. The carrier transport mechanism at Schottky junction is dominated by the probability of majority carriers to overcome the barrier height—defined as the energy difference from the Fermi level of metal to the conduction (valence) band edge of \( n(p) \)-type semiconductor for electron (hole). This is known as the thermionic-emission theory [59], and the current density flowing through the interface can be calculated by

\[
J(T, \phi_B, V) = A^* T^2 e^{-\frac{q \phi_B}{k T}} [e^{\frac{q V}{k T \eta}} - 1] \quad \text{in A/cm}^2,
\]

where \( A^* \) is the Richardson constant of semiconductor substrate, \( T \) is the temperature, \( q \) is electron charge, \( q \phi_B \) is the Schottky barrier height, \( k_B \) is Boltzmann’s constant, \( V \) is the applied voltage, and \( \eta \) is the ideality factor.

Graphene as a zero-bandgap semiconductor has many properties resembles a metal. The graphene-semiconductor heterojunctions also behave like a Schottky junction. The distinguishing feature of graphene is that its Fermi-level position varies with its carrier density. This property results in a tunable Schottky barrier height due to graphene’s movable Fermi level position—the mechanism allows the device concept of GJFET. This graphene-semiconductor heterojunction is the fundamental component studied in this thesis, and the physics of which will be discussed in detail in
Chapter 2. In the following section, the background of the graphene-semiconductor heterojunction related to the research in this thesis is introduced.

1.2.1 Graphene on silicon

The very first reported graphene-semiconductor heterojunction is formed by transferred CVD graphene on an $n$-silicon substrate [60]. The graphene was grown on Ni and then transferred onto the patterned $\text{SiO}_2/n\text{Si}$ substrate. The $n$-Si wafer (doped of $1.5-3\times10^{15} \text{ cm}^{-3}$) with 300nm $\text{SiO}_2$ was patterned and etched to form windows. After graphene transfer, the device is completed by sputtering the gold electrode surrounding the window on $\text{SiO}_2$ to form electrical contact to graphene. The flexible nature of graphene makes it well conform with the surface morphology, and covers the bare Si in the window to form a heterojunction. The structure of this device is shown in Fig. 1.10.

![Figure 1.10: The first device that utilize a graphene-silicon Schottky junction as the active area of a solar cell.](image)

The authors measured the current-voltage characteristic of this heterojunction and found the interface showed a noticeable rectifying behavior. They propose that the rectification is due to a graphene/$n$-Si Schottky junction based on its resemblance to a semiconducting CNT to $n$-Si heterojunction. The device was used as a solar cell with an efficiency of 1.7 %. Graphene in this device serves as the transparent electrode and the hole transport layer. The silicon serves as the light absorbing medium. The photogenerated electron-hole pairs are separated by the built-in
electric field within the silicon.

The graphene-silicon Schottky junction is later confirmed to be formed not only on $n$-Si but also on $p$-type of silicon substrate [61]. In this particular experiment, exfoliated graphene was placed on both $n$- and $p$-types of silicon substrates with a step structure similar to Fig. 1.10. From the forward-bias current-voltage characteristics, it is found that the Schottky junction is formed between BLG and both $n$- and $p$-types of silicon with Schottky barrier heights (SBHs) of 0.41 and 0.45 eV respectively at 300 K. The SBHs showed a strong temperature dependence, meaning the carrier transport mechanism is dominated by thermionic emission. The authors also showed that the SBH is changed by vacuum annealing, which suggests that the SBH can be varied by doping of graphene. Even though this work demonstrated the Schottky diodes formed by BLG instead of SLG, the same Schottky junction formation is in principle applicable to the SLG-silicon interface. The ideality factor of BLG/Si Schottky diode ranges around 4–7 and 25–28 on $n$- and $p$-silicon substrate, respectively. The ideality factors of graphene-silicon Schottky diodes showed no obvious dependence on the temperature or the number of graphene layers.

The ideality factor is a parameter measuring the degree of thermionic emission across the interface. It is affected by the fabrication process and thus the interfacial condition. In the ideal Schottky junction where the current is 100% dominated by thermionic emission, the ideality factor is 1. In the real world this parameter typically falls between 1–2 for metal-silicon Schottky diodes, and it can be significantly higher for Schottky diodes made with immature fabrication process. To address this problem, a specific CVD technique to reduce metallic impurities during graphene growth, combined with a dry transfer method was developed [62]. A nearly ideal graphene/$n$-Si interface with an ideality factor of 1.08 was obtained.

1.2.2 Graphene on GaAs, GaN, and 4H-SiC

Tongay et al. reported on rectifying junctions formed by CVD SLG transferred onto various $n$-type semiconductors—including Si, GaAs, GaN, and 4H-SiC [63]. The device structure used in his study is the same as the one shown in Fig. 1.10, except that the SiO$_2$ is deposited by plasma-
enhanced CVD instead of thermal oxidation, and the material of ohmic contact is different for each semiconductor substrate. The doping densities for Si, GaAs, GaN, and 4H-SiC used in this study are $2 \times 10^{15}$, $3 \times 10^{16}$, $1 \times 10^{16}$, and $1 \times 10^{17}$ cm$^{-3}$, respectively. Surface orientations are not specified.

The authors first confirmed that all the graphene sheets on SiO$_2$ showed a $p$-type doping about $5 \times 10^{12}$ cm$^{-2}$, i.e. the Fermi level of graphene is below the Dirac point from hall measurement. They attribute the $p$-type doping to the copper etchant used and the gold contact. This $p$-doping leads to high SBHs of 0.86, 0.79, and 0.73 eV for graphene-semiconductor Schottky diodes fabricated on Si, GaAS, and GaN, respectively. These SBH values are extracted by temperature-dependent current-voltage ($I$-$V$) characteristics in the forward bias region. However, for the graphene on 4H-SiC, the SBH extracted by the same method is 0.91 eV. Using an electron affinity of 3.4 eV for 4H-SiC, the graphene is expected to have a work function of 4.31 eV which is above the Dirac point—indicating an $n$-type graphene on 4H-SiC surface. They contribute this measured low SBH to the bond polarization at 4H-SiC surface.

It is also found in this paper that the SBHs for all four heterojunctions is a function of bias voltage—SBH decreases with reverse bias—rather than staying as a constant as in a conventional metal-semiconductor Schottky junction. This SBH reduction causes the reverse-leakage current to gradually increase with reverse-bias voltage. The reason for this SBH lowering is because under reverse bias, graphene is negatively charged and its Fermi level is shifted upward relative to the Dirac point.

The authors have also compared the SBHs extracted by capacitance-voltage ($C$-$V$) measurement to the values obtained by forward $I$-$V$ characteristics. A discrepancy in SBHs is found between both methods. A higher SBH values is obtained for the same junction by $C$-$V$ measurement. It is caused by the inhomogeneous doping in the graphene sheets, and thus the SBH inhomogeneity. $C$-$V$ measurement measures the average SBH across the diode area, while $I$-$V$ extracts the SBH from the point that contributes to the current most, i.e. the point having the lowest SBH. The transferred CVD graphene on 4H-SiC surface has many atomic scale ripples, nano-scale edges, and
deformation caused by the SiC surface steps, leading to the spatial fluctuation of the doping to graphene. This SBH inhomogeneity in graphene-4H-SiC system is further confirmed by others using scanning tunneling spectroscopy [64]. Therefore the SBH of graphene-4H-SiC heterojunction cannot be explained simply by traditional Schottky junction theory due to the inhomogeneity caused by silicon carbide surface steps. This leads to a larger leakage current than expected at reverse bias that may affect the performance of the devices based on graphene/4H-SiC interface.
1.3 Devices based on a graphene-semiconductor heterojunction

1.3.1 Photodetector

The first category of heterojunction-based device of our interest is the photodetector. Photodetectors are devices that can convert incident light into other measurable quantity, typically in the form of electric current. Traditional semiconductor has a absorption cutoff at the wavelength corresponding to its bandgap, \( \lambda = \frac{E_g}{hc} \), where \( E_g \), \( h \), and \( c \) are the bandgap, Planck constant, and speed of light respectively. Therefore, the semiconductor becomes transparent to light at long wavelength (small photon energy).

Because of graphene’s zero-bandgap nature, pristine graphene has an ultrawide absorption spectrum. This property makes it useful in many applications as a sole detector, unlike in many cases where multiple photodetectors with different spectral ranges are employed. The second advantage of graphene photoconductor is its fast operation speed, or a wide operation bandwidth. This is a result of graphene’s high carrier mobility that shortens the carrier transit time. In theory, the bandwidth of graphene photodetector can be > 500 GHz and is limited by the \( RC \) time constant from the parasitics rather than by the transit time [65]. Actual graphene photodetector operated in 40 GHz [65] and an optical data link with 10 Gb/s [66] has been reported.

Before introducing graphene photodetectors, the figures of merit (FOM) providing quantitative assessment on the performance are briefly described here. Detailed explanation of which will be given later in the chapter of experiment and analysis. The most widely used FOM is the responsivity, which represents the capability of a photodetector to convert incident optical power into photocurrent. Internal Quantum efficiency is similar to responsivity, measuring the photon-to-carrier conversion ratio. With those in mind the graphene photodetector will be introduced in subsequent sections.
1.3.1.1 Photoconductor—graphene FET

The first graphene-based photodetectors is demonstrated with a back-gated graphene MOS-FET structure [67]. The photodetector operated in the photoconductor scheme which is composed by a graphene sheet with two ohmic contact electrodes (the source and drain) on each side. Applying a small voltage between the source and drain electrodes results in a built-in electric field within the graphene. When incident photons are absorbed in graphene, electron-hole pairs are generated and then separated by the built-in field. Finally they are collected at different electrodes as the photocurrent. The backgate can modulate this photocurrent (or the built-in field) by applying a gate voltage.

However, due to graphene’s zero bandgap nature, this operation has large dark current—an undesirable property meaning low sensitivity and high noise. Fortunately it was also found that the current mostly generated at the regions adjacent to metal-graphene interface even at zero drain-source bias [67–69]. This is because graphene’s low density of states making it strongly doped by metal electrodes at the metal contacts [70]. At the regions where graphene is in contact with the metal, its Fermi-level is close to that of the metal due to charge transfer, while other regions are uninfluenced and can be controlled by the back gate voltage. Because of this Fermi-level difference between the metal contact region and the uninfluenced one, a built-in electric field is formed at the transition region inbetween [67–69]. This enables an unique high-speed operation, with zero bias and thus zero dark current. A responsivity of 0.5 mA/W (corresponding to a internal quantum efficiency 6–16%) was obtained under 1550nm illumination at a gate bias of 80 V [65]. By using different metals with different work functions and closely spaced source/drain electrodes, the built-in field is enhanced and results in an enhanced responsivity of 6.1 mA/W at the same wavelength at a gate bias of 15 V [66]. Multi-top gates [71] can also be used to enhance the built-in field instead of different source/drain materials.

However, drawbacks exist in the graphene-FET structure as a photodetector. The inherent optical absorption of graphene is too low for photonic applications. This low absorption limits the
responsivity of graphene-MOSFET-based photodetectors on the order of 1 mA/W [72,73]. The low absorption can be improved by integrating graphene with other field-enhanced nanostructures [74] or waveguide structures [75–77], but it still suffers from the small absorption area. Since the built-in field exists only in the transition regions, the electron-hole pairs are separated therein only. The actual absorption area of the photodetector is limited to these sub-micron wide areas [78]. This means a large portion of the device area is needed for closely spaced metal electrodes, while only a small portion of the area is used to generate photocurrent. This limits the responsivity (on the order of mA/W) and the speed of the graphene-MOSFET-based photodetectors.

1.3.1.2 Photodiode—graphene-semiconductor heterojunction

The other type of graphene-based photodetector is a true two-terminal device based on graphene-semiconductor heterojunction—a photodiode. The photodiode has a simple structure formed by a graphene-semiconductor heterojunction where graphene is open and exposed to incident light. The Fermi-level difference between graphene and semiconductor results in a depletion region with built-in electric field within the semiconductor that helps separate electron and hole pairs. The wavelength of incident light studied in most of the reports in this realm is in the visible spectrum [61, 79, 80]. In this particular device scheme, the graphene is in contact with a bare semiconductor surface, and the current is flowing perpendicular to the graphene plane across the interface. Like usual photodiodes, graphene-semiconductor heterojunction photodiode also operates at the reverse-bias condition. The photodiode operation mechanism is explained in Fig. 1.11.

In the dark condition, the majority carrier with highest energy in graphene is distributed around the Fermi level \( (E_{F,G}) \). Under forward bias, the majority carrier flows from the semiconductor into graphene, contributing to a large forward bias current. When the heterojunction is reversely biased, the majority carriers cannot surpass the Schottky barrier height. The resultant reverse-bias current, or dark current, is described in Eqn. 1.1. It decreases exponentially with the SBH at the interface, and therefore a semiconductor that can provide higher SBH is preferred in a graphene-semiconductor photodiode scheme. A heterojunction photodiode therefore has a high
Figure 1.11: Graphene/semiconductor photodiode without and with visible light illumination. (a) Left column: Graphene/n-semiconductor Schottky diode. In this case majority carrier is electron. (b) Right column: Graphene/p-semiconductor Schottky diode. In this case the majority carrier is hole.

rectification ratio in the dark due to the Schottky barrier height.

When visible light is illuminated on the heterojunction photodiode, there are two mechanisms that can contribute to the reverse-biased current, or photocurrent: the absorption in the graphene and the absorption in the semiconductor. Since graphene only absorbs $\sim 2\%$ of the light, the dominating mechanism of photocurrent is due to the absorption in semiconductor. The photons are mainly absorbed in the depletion region within the semiconductor adjacent to graphene, and the built-in field separates the electron-hole pairs. The majority carriers are swept by the built-in field and collected at the semiconductor terminal. While the minority carriers are propelled by the built-in field into the graphene, and collected in the graphene terminal. Therefore in those
reports [61, 79, 80], graphene’s contribution to photocurrent is neglected and was used solely as a transparent electrode and a carrier transport layer.

1.3.2 Heterojunction solar cells

Graphene by itself is not an ideal absorbing material for solar cell as mentioned previously. The intrinsic absorption is only 2.3% due to its atomically thin absorption length. However, graphene-semiconductor heterojunction can still play a critical role as the active region of a solar cell. The photocurrent mechanism is basically the same as the case of photodiode shown in Fig. 1.11. In comparison with a solar cell made of pure silicon $p$-$n$ junction, graphene acts as a transparent electrode, a carrier transport layer, and a complementary absorbing medium to collect photons with energy $< 1.12 \text{ eV (}\lambda > 1100 \text{ nm)}$, which is a significant portion of solar energy that can not be collected by silicon-based solar cells. Photoexcited electron-hole pairs are deep inside graphene’s valence and conduction bands, and therefore the excited majority carrier—under the assistance of the interfacial electric field—has high enough energy to overcome the Schottky barrier height and be swept and collected in the silicon side. However this absorption in graphene is often ignored in papers [60, 61, 79–81].

As mentioned earlier, the first paper found Schottky junction behavior of a graphene/$n$-Si interface used this structure as a solar cell [60]. The authors claim that graphene serves as a transparent electrode as well as a anti-reflection coating for the solar cell. This proof-of-concept graphene-silicon solar cell showed open circuit voltage of 0.42–0.48 V, depending on the intensity of incident light, and a short-circuit current density of 4–6.8 A/cm², corresponding to an efficiency of $\approx 1.7\%$. Even though the efficiency is not high, this device demonstrated the potential advantages, e.g. the ease to expand to large area, low cost, simple device structure and integrable fabrication process with silicon technology, etc. of this type of interface in electronic and photovoltaic applications. The efficiency is later improved to a record of 8.6% by chemical doping of graphene—making it more $p$-type to increase the built-in potential and decreasing the series resistance in graphene sheet [81].
1.3.3 Barristor

The main technological challenge for graphene FETs being useful in logic applications is to achieve an on-off ratio $> 10^3$. Because of the lack of a bandgap and the relatively low density of states, the carrier density of graphene at room temperature falls in the range of $10^{11}$–$10^{13}$ cm$^{-2}$ (as explained in 2.1). This means the channel conductivity—and thus the on/off ratio—can only be modulated by two orders of magnitude at most.

One solution to this problem is to invent a new device that operates in a fundamentally different way from a MOSFET, i.e. not to use the conductivity of graphene. One of the most successful devices is known as the graphene barristor [82–84]. Its device structure and operating mechanism is shown in Fig. 1.12a and 1.12b respectively. The "channel" is the Schottky-like heterojunction formed by graphene and a semiconductor with a bandgap. As explained in 1.2, when graphene and the semiconductor are in contact, a Schottky-like heterojunction with tunable Schottky barrier height (SBH) is formed. The reverse-bias current across the heterojunction decreases exponentially with the SBH.

The barristor structure uses a gate—formed by a dielectric layer and a metal electrode—to modulate graphene’s carrier density. This gate—a dielectric gate capacitor—can be placed either on top or beneath the graphene. Since graphene’s density of state is low close to the Dirac point, its Fermi level position (work function) depends on its carrier density. The change of work function by the gate bias voltage then in turn changes the SBH, and thus exponentially modulates the reverse-bias current through the interface. This switching mechanism of a graphene barristor is depicted in the band diagrams shown in Fig. 1.12b. Yang et al. demonstrates both $n$- and $p$- types of barristor on 150mm Si wafer, and showed an on/off ratio of $10^5$ [82]. They also demonstrated basic logic circuits: an inverter and a half-adder by combining complimentary graphene barristors.

There is another type of graphene FET that also uses a gate capacitor to modulate the Fermi level position of graphene to achieve high an on/off ratio—a vertical graphene tunneling FET [85]. However in this device, the tuning of Fermi level is to to modulate the carrier tunneling
Figure 1.12: (a) Schematics of top- and bottom-gated graphene barristor. (b) Operation mechanism shown in energy band diagrams. Here the exemplary majority carrier type is $n$-type (electron). The same operating principle applies to $p$-type barristor with opposite gate and drain bias polarity.

probability between two stacked graphene layers separated by an insulating layer, rather than tuning the Schottky barrier height. It can also achieve an on/off ratio of $10^5$ depending largely on the insulating layer used. Yet this tunneling FET is not as versatile as a graphene-semiconductor heterojunction and will not be discussed further in this thesis.
1.4 Novel graphene-semiconductor heterojunction devices

1.4.1 Infrared photodetector

The graphene-silicon heterojunction infrared (IR) photodiode (PD) is a true two-terminal device. It is rarely explored but potentially can solve the problems of small absorption area, low absorption, and low responsivity of a graphene-FET-based photodetector [86, 87]. First, the device area of graphene FET-based photodetector is limited by the narrow transition region surrounding the metal electrodes. However, in graphene-semiconductor heterojunction photodiode, the entire heterojunction area has a depletion region underneath the graphene. Thus the entire heterojunction area is the device active area. Second, the low optical absorption of graphene is due to its single atomic nature. However, if the absorption can be converted to a direction in parallel to the plane with a light guiding structure such as a silicon waveguide, the absorption length can be increased by orders of magnitude without sacrificing the dark current (maintaining the same device area). The absorption and thus the responsivity is expected to increase dramatically. Therefore, this graphene-silicon heterojunction photodiode is of our interest for silicon photonic applications.

A silicon photonic interconnect can enhance the bandwidth of data transfer with much higher efficiency than traditional electrical interconnect [88–90]. The typical wavelength falls in the IR region of 1260–1675 nm. However because silicon has a bandgap of 1.12 eV at room temperature, it is transparent to light of wavelength >1100 nm. Therefore silicon cannot be used as the detector in the wavelength of fiber-optic telecommunication. Germanium (Ge) and Indium Gallium Arsenide (InGaAs) are the choices of material. However, integrating these two materials with silicon is proven very challenging, especially for the InGaAs. The current technology for the receiver end in Si photonics uses Ge PIN PDs. The the main challenge of integrating Ge into Si by epitaxial growth is the large lattice mismatch 4.2%, which prohibits low defect, high quality Ge layers. Large thermal mismatch and the aggressive cleaning process needed for Ge also increase the difficulty of monolithically integrating Ge with Si [91, 92].

The broad absorption spectrum of graphene and the ease of integration with silicon provide
the advantage of a graphene-silicon heterojunction IR PD. It enables a monolithic silicon chip for
IR detection and Si photonics. As introduced in 1.3.1.2, the IR light is absorbed in graphene,
generating photo-excited electron-hole pairs. The mechanism is very different from that described
in 1.3.1.2 for visible spectrum. The semiconductor contribute to the most of the photocurrent
in visible wavelength, while in the IR regime the graphene is the only absorption medium. The
operation mechanism of the heterojunction IR PD is depicted in Fig. 1.13. The electron-hole pairs

![Figure 1.13: Current mechanism of a graphene-\(n\)Si infrared photodiode.](image)

are separated by the interfacial electric field, and the excited majority carrier with high energy in
the conduction band thus has a higher probability to overcome the Schottky barrier height. Once
the majority carrier surpass the SBH, it is swept out by the electric filed within the depletion region
and collected in the semiconductor end. The leftover minority carriers recombines with opposite
charge directly in graphene. This process completes the photocurrent loop.

Graphene-silicon heterojunction used as a novel IR photodetector will be explored by mod-
eling and numerical simulation in Chapter 2. Real devices will be fabricated in Chapter 3, and
characterized and analyzed in detail in Chapter 4.

1.4.2 Graphene junction field-effect transistor (GJFET)

The majority of the graphene transistors reported so far—whether they are based on the
transferred chemical-vapor deposition (CVD) or exfoliated graphene—use a heavily doped silicon
substrate with an oxide layer as the back gate (or bottom gate), forming a graphene MOSFET. This device structure is mainly adopted to visualize graphene during the fabrication as explained in 1.1.2. Also a heavily-doped substrate is typically used, because it is the gate electrode and should be as metallic as possible to reduce unwanted parasitics. This type of back-gated transistor requires a certain gate voltage, usually positive, to turn the channel to the off state due to the initial hole doping in graphene. The main sources of the initial hole doping likely come from the chemical doping during transfer process, the oxygen in atmosphere, or the charge transfer and/or induction from the substrate. Therefore, those graphene back-gate MOSFETs are normally-on device, or more officially called $p$-channel depletion-mode MOSFETs. The voltage required to turn off the channel—commonly referred to as the Dirac voltage ($V_{\text{Dirac}}$) or the threshold voltage ($V_{\text{th}}$)—is an indication of the initial hole doping density in graphene. The threshold voltage is an important parameter for circuit applications. Therefore threshold voltage tuning capability via fabrication process is a very desirable property for transistors to become applicable.

In some transistor designs, an top gate (a dielectric layer and a metal contact) is deposited onto the graphene channel in addition to the existing bottom gate, forming dual-gate graphene FETs shown in Fig. 1.14 [93–95]. This design enables the threshold voltage tuning with bottom gate and uses the top one as the control gate to modulate the current flowing in channel. However, depositing the top gate further interferes the lattice symmetry of graphene and thus degrades the carrier mobility. Moreover, another main drawback of this scheme is that all the back gates of the transistors built on the same wafer are shorted together through the heavily doped substrate. This brings two associated problems. First, since the graphene at different locations may have different doping levels, i.e. different threshold voltages, this common back-gate scheme is not in favor of the circuit design as the transistors cannot be turned on or off at the same time as desired. Second, this heavily doped back-gate scheme is unfavorable to the control of $V_{\text{th}}$ of individual transistor on the same substrate, and thus only one type, either $p$ or $n$, of MOSFET can exist on a substrate. This means to build a fundamental component of the circuit—an inverter, the only scheme that can be used is the enhancedment-load inverter and top gates must be used, as shown in Fig. 1.14.
To solve the problems, a back-gate structure using graphene/semiconductor Schottky junction is invented (Fig. 1.14). This graphene FET integrates both functionalities of $V_{th}$-tuning and current modulation into a single gate. We name it graphene junction field-effect transistors (GJFETs) for its similar gate structure to the traditional JFETs. The main difference between the two is the channel material; in our device it is the graphene that is used rather than another semiconductor layer. The usage of graphene channel utilizes its high carrier mobility and high carrier saturation velocity, making GJFET particularly suitable for high-speed applications. The threshold voltage
of GJFET also depends on the initial doping of the transferred graphene. However, the density of initial holes in GJFET can be modulated directly by the space charge (ionized dopant) density in the depletion region within the semiconductor substrate, which is controlled by the substrate doping density. With the GJFET structure and the mature technologies to selectively dope specific locations by ion implantation, each GJFET can be isolated and the threshold voltage tuning of each individual transistor on the same wafer becomes feasible and favorable to circuit applications. Both \( p \) and \( n \) types of GJFETs can coexist on the same substrate, and a complementary inverter can be made without the need of top gates (Fig. 1.14).

Since GJFET also employs graphene-semiconductor Schottky-like junction as the main part of the device, it can be easily confused with graphene barristor that has similar structure. However, a barrister has a fundamentally different device operation mechanism and characteristics from a GJFET. In terms of gate structure and mechanism, a barristor resembles a graphene MOSFET more than our GJFET. Both barrister and graphene MOSFET employ a dielectric gate capacitor to modulate the charge of graphene, and thus the current flowing in the channel. The distinguishing feature between a barrister and a graphene MOSFET is the channel—in a barrister the current flows vertically through the graphene-semiconductor heterojunction, while in a graphene MOSFET, as well as in our GJFET, the current flows laterally within the graphene sheet between the source and drain electrodes. Since the current flowing through the Schottky junction depends exponentially on the barrier height, a barrister can achieve a high current on/off ratio (\( >10^5 \)) by shifting the Fermi-level of graphene for a partial of an electron volt. On the other hand, the on/off current ratio of a graphene MOSFET is determined by graphene’s Fermi level position (and thus the carrier density) of the graphene channel, which is the same governing principle in our GJFET. Therefore the off current in theory cannot be blocked completely at room temperature as a result of graphene’s zero bandgap. And the on/off ratio can only reach as high as two orders of magnitude due to the band structure of graphene.

The novel device functionality enabled by a GJFET structure is the ease of \( V_{th} \) tuning. Since the space charge density is the product of depletion region width and the substrate doping density
(\(N_D\)), varying \(N_D\) enables threshold voltage tuning of GJFET devices without the need of an additional gate.

It should be noted that the \(V_{th}\) tunability is also achievable in a barrister and a graphene MOSFET. Both of them employ a dielectric capacitor as the gate. The \(V_{th}\) of such a MOS capacitor is affected by the gate capacitance and the work function difference between graphene and the gate material. The knobs to tune the \(V_{th}\) in a MOS back gate are the work function of the gate metal material (typically less than an electronvolt), the dielectric constant of the gate dielectric, and the dielectric thickness (assuming the Fermi-level position is the same for all graphene sheets on the same wafer, which is often not the case as local contaminants would cause different initial hole densities in graphene sheets at different locations even on the same wafer, diversing the \(V_{th}\)).

To control the \(V_{th}\) of a MOS gate—either top or back gate—requires depositing different gate dielectric materials and/or different thicknesses and/or different gate metal materials at different locations on a wafer. Therefore tuning \(V_{th}\) in such MOS gates requires a much more complicated process, especially when multi \(V_{th}\) is to be realized on the same wafer. This greatly complicates the fabrication process from the technology point of view. The GJFET structure is a viable solution to this problem. GJFET uses a completely different gate mechanism from a MOS gate—it uses a depletion-region capacitor within the graphene-semiconductor heterojunction. The capacitance can be controlled by the doping density of the substrate, which is the key for realizing \(V_{th}\) tunability with ease of fabrication.

A physical model of device operation will be provided in Chapter 2, where numerical simulations based on a self-constructed algorithm will also be demonstrated. The important feature of a GJFET: the tunability of \(V_{th}\) will also be simulated and experimentally demonstrated in Chapter 5, where the GJFETs fabricated on substrates with different doping densities will be characterized and analyzed.
Chapter 2

Device modeling and simulation

2.1 Band structure and electronic properties of graphene

The fascinating properties of graphene originate from its unique honeycomb lattice structure. The detailed electronic energy band structure of graphene was calculated way back to 1947 by Wallace in his theoretical paper: "The band theory of graphite" [11]. In the calculation he used tight-binding approximation on the sublattices of a single layer of graphite (known as graphene now) to derive the dispersion relation of electron. From his derivation Wallace found that the dispersion relation becomes linear in the vicinity of $K$ (or $K'$) vector:

$$E_{\pm}(q) \approx \pm \hbar v_F |q| + O(|q/K|^2), \quad (2.1)$$

where $q$ is the momentum with respect to $K$ and $|q| \ll |K|$, $\hbar$ is the reduced Planck constant, and $v_F \simeq 1.1 \times 10^8$ cm/s is the Fermi velocity. This linear dispersion relation is different from a normal particle’s quadratic dispersion relation $E = \frac{(\hbar k)^2}{2m^*}$, which yields an effective mass $m^*$ inversely proportional to the second derivative $\frac{d^2E}{dk^2}$. The calculated 3D energy band structure in momentum space of graphene is shown in Fig. 2.1. As could be found from the figure, the conduction band contacts with valence band at six corners of the first Brillouin zone (K and K' points), and the dispersion is linear and symmetric around $E_k = 0$ described by Eq. 2.1. The linear dispersion relation resembles the energy of ultrarelativistic particles—massless Dirac fermions in quantum mechanics, and therefore the energy bands are called Dirac cones and those points where energy bands contact are referred to as Dirac points.
Based on the dispersion relation (Eq. 2.1) and the 2D nature of graphene, the density of states (DoS, \( g(E) \)) per unit area and energy can be calculated:

\[
g(E) = \frac{1}{A} \frac{dN}{dE} = \frac{1}{A} \frac{dN}{dk} \frac{dk}{dE} = \frac{2k}{\pi \hbar v_F} = \frac{2E}{\pi(hv_F)^2}. \tag{2.2}
\]

The DoS of graphene is also a linear function of energy and momentum as shown in Fig. 2.2

The electron (\( n \)) and hole (\( p \)) densities of graphene can then be calculated based on the DoS and Fermi-Dirac distribution (\( f_{FD}(E) \)) at a given temperature \( T \):

\[
n(E_F, T) = \int_0^\infty g(E) \cdot f_{FD}(E) \, dE = \frac{2}{\pi(hv_F)^2} \int_0^\infty \frac{E}{1 + e^{(E - E_F)/k_B T}} \, dE \tag{2.3}
\]

and

\[
p(E_F, T) = \int_{-\infty}^0 g(E) \cdot [1 - f_{FD}(E)] \, dE = \frac{2}{\pi(hv_F)^2} \int_0^\infty \frac{E}{1 + e^{(E + E_F)/k_B T}} \, dE, \tag{2.4}
\]

where \( E = 0 \) is the Dirac point that serves as the top edge of the valence band and the bottom edge of the conduction band, \( E_F \) is the Fermi level that determines the carrier densities. At zero temperature \( T = 0 \), the Fermi-Dirac distribution can be simplified as a step function, and then the carrier densities can be simplified:

\[
n(E_F) = \frac{(E_F)^2}{\pi(hv_F)^2}. \tag{2.5}
\]
for electron density and

\[ p(-E_F) = \frac{(-E_F)^2}{\pi(hv_F)^2} \tag{2.6} \]

for hole density, where the negative sign means that Fermi level is below Dirac point, and vice versa. Equation 2.5 and 2.6 can be rearranged to show Fermi level as functions of the carrier densities:

\[ E_F(n) = hv_F\sqrt{n\pi} \tag{2.7} \]

for \( n \)-type graphene and

\[ -E_F(p) = hv_F\sqrt{p\pi} \tag{2.8} \]

for \( p \)-type graphene. Because of the simplicity of Eq. 2.5–2.8, these equations are often used by physicists. However it should be noted that they are only good approximations when \( |E_F| \gg 0 \) due to the nature of Fermi-Dirac distribution. As \( |E_F| \) is approaching the Dirac point \( (E_F = 0) \) the approximations on carrier densities yield increasing errors compared to the results obtained by Fermi integrals, i.e. Eq. 2.3 and 2.4.

The electron and hole densities of graphene at \( T = 0 \) and 300 K are shown in Fig. 2.3a, and the net charge density \( |n - p| \) is shown in Fig. 2.3b. Both figures are calculated based on Fermi integrals. From Fig. 2.3a one can find the intrinsic carrier density \( (i = n = p) \) of graphene is
about $8 \times 10^{10}$ cm$^{-2}$ at 300 K. This is very different from the approximations (Eq. 2.5–2.6) which predict zero carrier when $E_F$ locates at the Dirac point. On the other hand, the approximations yield satisfactory results as shown in Fig. 2.3b where the solid lines (the approximations) fit the dotted ones (the Fermi integrals) reasonably well.

![Graphene Conductivity](image)

(a) Carrier densities  
(b) Net charge density

Figure 2.3: Calculated (a) electron and hole densities and (b) net charge density of graphene with Fermi integrals at $T = 0$ and 300 K.

The resistivity of graphene sheet can be related to its carrier densities by considering the mobilities for each type of carriers. This resistivity is often referred to as sheet resistance $R_{sh}$ in the unit of $\Omega/\square$:

$$R_{sh}(E_F, T) = \frac{1}{q[n(E_F, T) \cdot \mu_n + p(E_F, T) \cdot \mu_p]},$$

(2.9)

where $q$ is the electronic charge, $\mu_n$ and $\mu_p$ are electron and hole mobility respectively. The conductivity $\sigma$ of graphene sheet is the inverse of the sheet resistance and therefore it can be expressed by

$$\sigma(E_F, T) = \frac{1}{R_{sh}(E_F, T)} = q[n(E_F, T) \cdot \mu_n + p(E_F, T) \cdot \mu_p].$$

(2.10)

The unit of $\sigma$ is $\Omega^{-1}$ or $S$. A plot of graphene conductivity as a function of $E_F$ and $T$ is shown in Fig. 2.4 for $T = 0$ and 300 K.
Figure 2.4: Calculated graphene conductivity as a function of Fermi level and temperature. Electron and hole mobilities are both 800 cm$^2$/V·s for simulation.

This conductivity modulation has been experimentally shown by an externally applied electric field in a MOS structure [1], and is often obtained as transfer characteristic of G-MOSFET. GJFET uses graphene as channel just like G-MOSFET, and therefore the transfer characteristic is expected to be the same based on the same switching mechanism as introduced in 1.4.2. This electric field effect can be explained by the modulation of graphene carrier densities (and the Fermi level, $E_F$). This field effect combined with the high carrier mobility of graphene makes it a candidate material for FET channels. However the intrinsic carrier density—as a result of thermal energy and zero bandgap—limits the modulation depth, or on-off ratio, of the graphene FETs. This can be observed from Fig. 2.3a where the carrier density can only be changed up to several hundred times higher than its intrinsic carrier density at 300 K by a typical MOS structure, implying a maximum on-off current ratio close to $10^3$ under high gate-bias condition. While this property limits the application of G-MOSFET and GJFET as switch in digital circuit, the high carrier mobility and its unique energy band structure still make graphene an interesting material in many other applications, such as transparent conducting layer, optical modulator, high-speed electronics, etc.
2.2 Graphene-semiconductor heterojunction

A graphene/semiconductor heterojunction resembles a metal/semiconductor junction in many aspects because of the electronic properties of graphene. The interfacial properties in both cases—whether rectifying or ohmic—are determined by the band alignment, or the relative work function position. If graphene or metal’s work function is larger than the work function of semiconductor, a depletion (accumulation) region is created within $n$- ($p$-) type semiconductor. This makes graphene or metal to $n$- ($p$-) semiconductor interface a Schottky (ohmic) junction. On the other hand if graphene’s work function is smaller than the work function of $n$- ($p$-) semiconductor, then the cases will be reversed, forming a Schottky junction with $p$-type semiconductor and an ohmic junction with $n$-type semiconductor. In all cases, the carrier type that is responsible for current transport is the majority carrier of the semiconductor.

For undoped single-layer graphene, the work function is found to be 4.57 eV, similar to that of graphite ($\sim$4.6 eV) [49]. Since in undoped graphene the Fermi level falls in the Dirac point where conduction and valence bands meet, the electron affinity is also 4.57 eV. This material parameter provides the information needed to draw the energy band diagram of a graphene-semiconductor interface. Since pristine graphene has a work function of 4.57 eV [49]—which is around the middle of silicon’s bandgap, and even the doped graphene typically has an work function within $0 \pm 0.2$ eV from this pristine value (see Fig. 2.3), the graphene/silicon interface most likely forms rectifying (Schottky) junction for both $n$- and $p$-type silicon with slight-to-moderately doping density. The same situation applies to 4H-SiC and 3C-SiC. Based on their electron affinity and bandgap values listed in Table 1.1, graphene/SiC interface forms Schottky junction for both $n$- and $p$-type 4H- and 3C-SiC. But now since the Schottky barrier height is much larger in 4H-SiC than that in graphene/silicon case, the Schottky behavior in graphene/4H-SiC can be sustained even in high doping concentrations.

The current density that flows vertically across the Schottky junction is described in Eqn.
1.1, which is shown here again for convenience:

\[
J(T, \phi_B, V) = A^* T^2 e^{(-\frac{q \phi_B}{k_B T})} \left[ e^{(\frac{q V}{k_B T})} - 1 \right] \ (A/cm^2),
\]

(2.11)

where \(A^*\) is the Richardson constant of semiconductor substrate, \(T\) is the temperature, \(q\) is electron charge, \(q \phi_B\) is the Schottky barrier height (SBH), \(k_B\) is Boltzmann’s constant, \(V\) is the applied voltage, \(\eta\) is the ideality factor.

The main distinctive difference between graphene/semiconductor and metal/semiconductor junctions is that the SBH is not a constant in graphene/semiconductor Schottky junction. The SBH \((q \phi_B)\), defined as the energy difference between the work function of graphene \((\Phi_G)\) and the electron affinity of the semiconductor \((\chi_s)\), is varying as a function of the applied bias, \(V\).

The reason behind this unique phenomenon is because the low density of state (DoS) of graphene compared with that of metal. As described in 1.2, the charge transfer (or induction) occurs when work functions are different in the materials on both sides of the Schottky junction. In metal, the DoS is so high that the induced charge can not shift metal’s Fermi level at all, resulting in a fixed work function in metal. So the SBH in Eqn. 2.11 is a constant for metal/semiconductor junction. While in graphene the story is totally different that the Fermi level (work function) is changed due to the induced charge. And since the amount of induced charge is related to the bias voltage, the SBH is obviously a function of bias voltage (and the type of semiconductor). The SBH \((q \phi_B)\) is thus dynamically changes as the bias voltage changes.

This phenomenon is qualitatively described in Fig 2.5. Here an \(n\)-type semiconductor is used as an example and therefore the space charge in depletion region is positive, which induces electrons in graphene. Before forming a Schottky junction, or when the junction is at the flat-band condition, there is no space charge formed inside the semiconductor, and thus graphene contains its original carrier density either \(p_0\) from transfer process or atmosphere as shown in Fig. 2.5a.

Once the junction is at equilibrium, a depletion region filled with space charge is formed inside the semiconductor. In order to hold charge neutrality, an equal amount of charge with opposite polarity is induced in graphene by the space charge inside semiconductor. The Fermi level of graphene is
Figure 2.5: Schottky barrier height of a graphene-semiconductor heterojunction as a function of bias voltage. Blue dotted line is the depletion region boundary, and blue cross is space charge.
therefore shifted due to those induced charges and this will in turn changes the width of depletion region and the amount of space charge. After reaching equilibrium as shown in Fig. 2.5b, a new Schottky barrier height smaller than the flab-band condition is formed in the heterojunction. The same space charge effect also influences the amount of charge in graphene when a bias voltage is applied across the junction, which modulates the space charge region (or depletion region) width and therefore the complimentary charge induced in graphene. The SBH is dynamically changing with the bias as shown in Fig. 2.5c and d as a result of Fermi level \((E_{F,G})\) shift of graphene.

The current flowing through graphene/semiconductor heterojunction depending on the SBH therefore should be expressed as:

\[
J(p_0, V) = A^* T^2 e \left( -\frac{q \phi_B(p_0, V)}{k_B T} \right) \left[ e^{\left( \frac{q V}{k_B T} \right)} - 1 \right], \tag{2.12}
\]

which is a function of graphene’s initial carrier density \((p_0)\) and bias voltage \(V\). At reverse bias where \(e^{\left( \frac{q V}{k_B T} \right)} \ll 1\), the reverse leakage current is increasing slowly with reverse bias instead of staying as a constant predicted by ideal Schottky theory (2.11). This behavior was also observed by others [62,79].

Here we begin the analysis by assuming an ideal Schottky junction in graphene/semiconductor interface, i.e. no interfacial layer and no surface states exist (no Fermi-level pinning). We only consider current due to thermionic emission. Also we assume that the interface is under quasi-equilibrium that the current flow does not affect the position of Fermi levels. The depletion region width \((x_d)\) within semiconductor can be expressed:

\[
x_d(V) = \sqrt{\frac{2 \varepsilon_s}{q N_d} \cdot \left( \psi_{bi} - V - \frac{k_B T}{q} \right)}, \tag{2.13}
\]

where \(\varepsilon_s\) and \(N_d\) are the dielectric constant and doping density of semiconductor, and \(\psi_{bi}\) is the built-in potential which can be expressed as

\[
\psi_{bi} = \frac{1}{q} [\Phi_G - \chi_s - k_B T \ln(\frac{N_c}{N_d})], \tag{2.14}
\]

where \(N_c\) is the effective density of state in the conduction band at 300 K. In the equation above,

\[
\Phi_G = 4.57 - E_{F,G} \tag{2.15}
\]
is a function of graphene’s Fermi level position with respect to the Dirac point \((E_{F,G})\), and therefore it is a function of the carrier density of graphene as shown in Fig. 2.3a. Assume this initial carrier density in graphene is \(p_0\). The space charge density

\[
Q_{sc} = qN_d x_d
\]  

is as a result a function of \(E_{F,G}\) after substituting 2.13, 2.14, and 2.15 into 2.16:

\[
Q_{sc}(E_{F,G}, V) = qN_d x_d = \sqrt{2q\varepsilon_s N_d \cdot (4.57 - E_{F,G} - \chi_s - k_BT \ln(\frac{N_c}{N_d}) - V - \frac{k_BT}{q})},
\]

which is a function of \(E_{F,G}\) and \(V\). This space charge density will induce an equal amount of charge in graphene, but with opposite sign. For example, if \(n\)-type semiconductor is used to form the Schottky junction with graphene, positive space charge is created inside the depletion region of semiconductor. In order to maintain the charge neutrality, the space charge will in turn induce an equal amount of negative charge (electron) inside graphene and shift \(E_{F,G}\) upwards. This \(E_{F,G}\) shift is shown by comparing Fig. 2.5a and b. This up-shifting \(E_{F,G}\) creates a smaller \(\psi_{bi}\) and thus a narrower \(x_d\) with less space charge. This tends to stop the up-shift of \(E_{F,G}\) and results in a converging or stable final \(E_{F,G}\) value.

The process is simulated numerically by assuming a dependable variable—carrier density as a function of bias voltage \((p_0'(V))\). \(p_0'(V)\) is obtained by \(p_0'(V) = p_0 - Q_{sc}(E_{F,G}, V)\). This \(p_0'(V)\) yields a new \(\Phi_G\) and therefore a new \(Q_{sc}\). By repeating the calculation, \(\Phi_G\) and \(Q_{sc}\) eventually converge to a consistent value. These parameters then are used to solve the only variable \(E_{F,G}\) as a self-consistent result. This final converging \(E_{F,G}\) is obtained at a certain bias voltage \(V\). Based on this equilibrium \(E_{F,G}\) value, SBH and current density can then be calculated.

Simulation results based on the physical model and the numerical calculation described above are provided for a graphene/\(n\)-Si heterojunction. The first thing of interest to us is how Fermi level of graphene shifts as a function of bias voltage. From previous description we know that the Fermi level shift results in an increasing SBH lowering with reverse-bias voltage. Also, from semiconductor physics, there is another additional effect called **image-force SBH lowering**. It explains the SBH
decrease with increasing reverse-bias voltage [59]. The image-force lowering can be expressed as

\[ q\Delta \phi_B = \sqrt{\frac{q^3 \varepsilon_m}{4\pi \varepsilon_s}}, \]  

(2.18)

where \( \varepsilon_m \) is the maximum electric field strength occurs at the interface and can be expressed as

\[ \varepsilon_m = \sqrt{\frac{2qN_d}{\varepsilon_s} \left(4.57 - E_{F,G} - \chi_s - \frac{k_BT}{q} \ln\left(\frac{N_c}{N_d}\right) - V - \frac{k_BT}{q}\right)}. \]  

(2.19)

The comparison between both SBH lowering mechanisms is shown in Fig. 2.6. Here we discuss two scenarios: the first is when graphene has a fixed \( p_0 \) on different substrate \( N_d \) (Fig. 2.6a), the second is when graphene has different \( p_0 \) while substrate \( N_d \) is hold constant (Fig. 2.6b).

From Fig. 2.6a we conclude that the the Fermi level shift in graphene due to its low DoS is the major effect that lowers SBH. The \( E_{F,G} \) increases more rapidly than any \( q\Delta \phi_B \) regardless of \( N_d \), with a trend that the higher \( N_d \) the steeper \( E_{F,G} \) shifting. This is understandable since \( E_{F,G} \) is induced by the space charge with the depletion region, therefore \( E_{F,G} \) and \( N_d \) show a positive correspondence. On the other hand, the image-force lowering (\( q\Delta \phi_B \)) increases slowly with the reverses-bias voltage and with \( N_d \) since the higher the \( N_d \) the larger the \( \varepsilon_m \) and thus the larger the \( q\Delta \phi_B \). However image-force lowering, \( q\Delta \phi_B \), is a relatively weak effect compared with the Fermi level shift with respect to Dirac point, \( E_{F,G} \), in graphene due to its low DoS. The same conclusions can be drawn from Fig. 2.6b that the major effect of SBH lowering is due to graphene’s Fermi level shift as a result of its low DoS close to Dirac point.

Considering both effects of Fermi level shift and image-force lowering, the total SBH is calculated and shown in 2.6c and d. From 2.6c the effect of increasing \( N_d \) on stronger SBH lowering is observed, while the SBH at zero bias does not change as a result of constant \( p_0 \). From phiBNdfixed, on the other hand, the zero-basis SBH increases significantly with \( p_0 \) as a result of the Graphene’s Fermi level shift, while the space-charge effect is similar for all three cases (the same \( N_d \)). The total SBH determines the current density flowing across the graphene/n-Si heterojunction as described by Eqn. 2.12. The corresponding calculated current density as a function of \( p_0 \) and \( V \) under fixed \( N_d \) and the current density as a function of \( N_d \) and \( V \) under fixed \( P_0 \) are shown in Fig. 2.6e and f respectively.
(a) $E_{F,G}$ and $q\Delta\phi_B$ ($p_0$ fixed to $1\times10^{12}$ cm$^{-2}$)

(b) $E_{F,G}$ and $q\Delta\phi_B$ ($N_d$ fixed to $4\times10^{15}$ cm$^{-3}$)

(c) Total $q\phi_B$ ($p_0$ fixed to $1\times10^{12}$ cm$^{-2}$)

(d) Total $q\phi_B$ ($N_d$ fixed to $4\times10^{15}$ cm$^{-3}$)
2.3 Infrared photodetector

The current mechanism described above is under quasi-equilibrium and does not include other effects such as carrier generation by light, etc. It is also the dark current of a graphene/semiconductor photodetector. When IR light is illuminated in the active region of a graphene/\( n\)-semiconductor heterojunction photodetector, an additional current resulting from photo-generated majority carrier contributes to the total current flowing across the Schottky junction. This component is shown in Fig. 2.7 as \( I_{\text{photo}} \), and it is the photo-generated majority carriers that overcomes the effective SBH \( (q\phi_B^{\text{eff}}) \).

Due to the symmetric band structure of graphene, the light is absorbed when the condition \( h\nu = 2 \cdot \Delta E_{F,G} \) is met, where \( h\nu \) is the photon energy and \( \Delta E_{F,G} \) is the energy of photo-generated hole (electron) with respect to the Dirac point. This condition is a result of momentum conservation and it can only be met when the graphene’s Fermi level position is above half of the photon energy \( (E_{F,G} < \frac{1}{2}h\nu) \). If the position of Fermi level is below \( \Delta E_{F,G} \) \( (E_{F,G} > \Delta E_{F,G}) \), there would be no...
available electron in the valence band to be excited. The commonly used 1300nm (for Si photonics) and 1550nm (optical fiber communications) IR light, the corresponding photon energy is 0.95 and 0.8 eV respectively. As shown in Fig. 2.6b, for graphene/n-Si system the $E_{F,G}$ easily satisfies the requirement $E_{F,G} < \frac{1}{2}h\nu$ provided $p_0$ is lower than $\sim 1 \times 10^{13}$ cm$^{-2}$.

The photo-generated electron has much higher energy than the electron in equilibrium (below Fermi level) and the SBH photo-generated electron sees is therefore significantly lower than the SBH discussed previously ($q\phi_{B}^{eff} \ll q\phi_B$, see Fig. 2.7). This yields a higher probability for photo-generated electrons to enter the conduction band of n-semiconductor and contribute to photocurrent. The equation describing this photo-current following thermionic emission theory can be

\[
I_{photo} = qV - I_{dark} = q\phi_B^{eff} - \Delta E_{F,G} - \Delta E_{F,G} - q\phi_B
\]

Figure 2.7: Top: the mechanism of photocurrent in graphene-n-semiconductor heterojunction IR photodetector. Bottom: zoom-in picture at the interface.
expressed as

\[ I_{\text{photo}} = \eta \frac{q P_{\text{opt}}}{h \nu} A A^* T^2 e^{\left( -\frac{q \phi_{\text{eff}}}{k_B T} \right)} \left[ e^{\left( \frac{q \nu}{\eta k_B T} \right)} - 1 \right] \]

\[ \propto \frac{P_{\text{opt}}}{\nu} e^{\left( -\frac{q \phi_{\text{eff}}}{k_B T} \right)} \left[ e^{\left( \frac{q \nu}{\eta k_B T} \right)} - 1 \right], \]

where \( P_{\text{opt}} \) is the incident optical power, \( \eta \) is the quantum efficiency. The total current with IR illumination is therefore

\[ I_{\text{total}} = I_{\text{photo}} + I_{\text{dark}} \]

\[ = [\eta \frac{q P_{\text{opt}}}{h \nu} e^{\left( -\frac{q \phi_{\text{eff}}}{k_B T} \right)} + e^{\left( -\frac{q \phi_{\text{B}}}{k_B T} \right)}] A A^* T^2 \left[ e^{\left( \frac{q \nu}{\eta k_B T} \right)} - 1 \right]. \]

The model here does not include the effect that the number of photo-generated carriers may be limited by the low DoS of graphene under strong illumination. Also the dark current component is likely reduced under illumination because the number of available electrons close to Fermi level is reduced by photo-generation process. Finally, the lifetime of photo-generated majority carrier is not considered, which may greatly influence the probability of overcoming the effective SBH. A more comprehensive physical model is still needed.
2.4 Graphene junction field-effect transistor

2.4.1 Linear model

GJFET is the a FET scheme devised in this thesis. It was briefly introduced in 1.4.2. A GJFET structure employs a graphene/semiconductor heterojunction as the gate and a graphene sheet as the channel. The conceptual device structure is shown in Fig. 2.8. The current flowing within graphene between source and drain is controlled by the voltage ($V_{gs}$) applied on the semiconductor (gate) with respect to the graphene (source).

As discussed earlier in 2.2, the Fermi level position ($E_{F,G}$) of graphene varies with the space charge density generated within the semiconductor. Therefore it is affected by the doping density of the semiconductor substrate ($N_d$), the bias voltage between the heterojunction ($V$), and the initial hole density of graphene ($p_0$), with the latter towards the list having greater influence on $E_{F,G}$. Initial holes existing in graphene after exposure to ambient air is also the reason why an $n$-type semiconductor is used as the substrate—it provides positive space charge to induce electrons in graphene to compensate the initial holes. $E_{F,G}$ then determines the end carrier density of graphene channel, and thus the current flowing within graphene. The on-off current ratio is therefore controlled by the voltage applied on the semiconductor (gate) with respect to the graphene (source), as well as by $N_d$ and $p_0$.

The basic GJFET model considered here is a linear model, which assumes uniform electric field within the graphene channel and the carrier mobility are constant, independent to drain or gate bias. Also the depletion region width under graphene channel is assume to be constant—i.e. the drain bias voltage is insignificantly small compared to the gate bias. The last assumption is the drain-source current ($I_{ds}$) is not affected by gate leakage current ($I_g$)—i.e. $I_g \ll I_{ds}$. To obtain numerical simulation of GJFET, we begin with revisiting graphene-semiconductor hetero junction. Equations 2.12–2.17 serve as the core equations to numerically obtain a self-consistent $E_{F,G}$ at every bias voltage $V_{gs}$. The analysis shown in Fig. 2.6 also applies to the GJFET to determine $E_{F,G}$ as well as to estimate the gate leakage current ($I_g$) including both effects of $E_{F,G}$ shift and
Figure 2.8: (a) Conceptual device structure of the GJFET. (b) Band alignment at flat-band condition. (c) Schematic transfer characteristic of the GJFET. (d)(e)(f) Band alignment describing the operation mechanism of the GJFET.
image-force SBH lowering. The self-consistent $E_{F,G}$ yields the conductivity of graphene, obtained with the assumption of constant hole and electron mobility through out channel, as expressed in Eqn. 2.22, which is iterated here:

$$\sigma(V_{gs}) = q[n(V_{gs}) \cdot \mu_n + p(V_{gs}) \cdot \mu_p].$$ \hspace{1cm} (2.22)

The current flows within graphene channel is then obtained by assuming an constant electric field distribution in graphene channel and ignoring any parasitic resistance:

$$I_{ds}(V_{gs}) = q[n(V_{gs}) \cdot \mu_n + p(V_{gs}) \cdot \mu_p] \frac{V_{ds}}{L} W,$$ \hspace{1cm} (2.23)

where $V_{ds}$ is the drain-source bias, $W$ is the channel width, and $L$ is the channel length.

The simulated $I_{ds}$ as a function of $V_{gs}$, $N_d$, and $p_0$ is shown in Fig. 2.9 for both graphene/n-Si and graphene/n-4H-SiC GJFETs. The simulation parameters are: $W/L = 5/3$ $\mu$m, $\mu_n/\mu_p = 1000/1000$ cm$^2$/V·s, and other parameters shown in the insets of Fig. 2.9. The material parameters are adopt from table 1.1. The $I_{ds}$ vs. $V_{gs}$ of a FET is called the transfer characteristic, from which the tranconductance $g_m$ can be found by

$$g_m = \frac{dI_{ds}}{dV_{gs}},$$ \hspace{1cm} (2.24)

which is the slope of the transfer characteristic curve.

From Fig. 2.9a and c, we found the higher the $N_d$, the smaller the $V_{gs}$ is needed to turn $I_{ds}$ to its minimum with a fixed $p_0$. This voltage is called Dirac voltage $V_{Dirac}$ or threshold voltage $V_{th}$. When $V_{gs} = V_{Dirac}$, $E_{F,G}$ is shifted to Dirac point, at which graphene has the minimum number of carriers. This behavior can be seen from Fig. 2.9b and d, which demonstrates $E_{F,G}$ shift corresponding to the transfer characteristics shown in Fig. 2.9a and c respectively. This $E_{F,G}$ shift is the main mechanism of GJFET operation. Another point worth mentioning is the higher the $N_d$, the higher the $g_m$ of GJFET (Fig. 2.9a and c), which is opposite to the trend in a Si MOSFET operated in saturation region [59]. $g_m$ modulation in a graphene MOSFET can only be obtained by changing the thickness of the gate oxide because $g_m \propto C_{ox}$, and thus the tunability is
(a) $I_{ds}(V_{gs}, N_d)$ with $p_0$ fixed

(b) $E_{F,G}(V_{gs}, N_d)$ with $p_0$ fixed

(c) $I_{ds}(V_{gs}, N_d)$ with $p_0$ fixed

(d) $E_{F,G}(V_{gs}, N_d)$ with $p_0$ fixed
Figure 2.9: Calculated transfer characteristic of the GJFET: $I_{ds}$ vs. $V_g$ & $N_d$ with (a) $p_0=1 \times 10^{12}$ and (c) $p_0=2 \times 10^{12}$ cm$^{-2}$. (e) $I_{ds}$ vs. $V_g$ & $p_0$ with fixed $N_d=2 \times 10^{16}$ cm$^{-3}$. (b)(d)(f) $E_{F,G}$ shift corresponding to (a)(c)(e) respectively. Solid (dotted) lines: the GJFET on n-Si (4H-SiC).

Limited (by minimum oxide thickness). The $g_m$ in GJFET on the other hand can be made high if a highly-doped substrate is used.

Comparing Fig. 2.9a and c we also found the higher the $p_0$ the larger the $V_{Dirac}$. This trend is calculated and shown as transfer characteristics in Fig. 2.9e for a fixed $N_d$. The trend of increasing $V_{Dirac}$ with $p_0$ is clear. Also the $g_m$ in GJFETs with three different $p_0$ is similar, especially at $V_{gs}$ away from $V_{Dirac}$. This result suggests that $N_d$ rather than $p_0$ is the main parameter determines the $g_m$ of GJFET. Although not shown here, another main factor affecting $g_m$ is the carrier mobility as in Si MOSFET. The higher the mobility, the higher the $g_m$.

The trend of lowering (increasing) $V_{Dirac}$ with increasing (lowering) $N_d$ and lowering (increasing) $p_0$ is concluded in Fig. 2.10. This figure can also serve as a reference chart to find out $p_0$ of graphene on either n-Si or n-4H-SiC surface with a simple GJFET structure and electrical measurement setup.

The use of a highly doped substrate can be problematic because of the high $I_g$. GJFET can only be functional when the gate leakage is low compared to signal current ($I_{ds}$). If $I_g$ is too
high, the channel current is washed out by $I_g$, and the GJFET becomes two Schottky diodes in parallel and no longer functions as a FET. High gate leakage current is also the critical reason for a GJFET to breakdown. In the extreme case when $I_g$ is so high that the graphene/semiconductor junction and/or metal contact is damaged by heat generated. The device is dead. This is the reason why in Fig. 2.9 graphene/$n$-Si GJFET is also simulated. Graphene/$n$-4H-SiC is expected to have much higher SBH—thus much lower reverse-bias leakage current—compared to graphene/$n$-Si heterojunction due to the much smaller electron affinity of 4H-SiC. Simulation results show that graphene/$n$-4H-SiC GJFET has similar behavior as graphene/$n$-Si one in terms of transfer characteristic. But the gate leakage current is orders of magnitude lower for the same device active area ($A = L \times W$).

Figure 2.11 shows the $I_g$ simulated for both graphene on $n$-Si and $n$-4H-SiC GJFETs. The parameters are the same as those used in Fig. transfer-char. Solid (dash) lines are for graphene/$n$-Si ($n$-4H-SiC) GJFET and they correspond to left (right) axes in both Figure 2.11a and b. The benefit of using 4H-SiC over Si as GJFET gate is obvious from Fig. 2.11a: The gate leakage current is $10^{14}$ smaller. The channel-to-gate-leakage current ratio ($I_{ds}/I_g$) is also calculated, which determines the operational margin of GJFET. Let’s say a minimum $I_{ds}/I_g$ ratio of $10^2$ is needed.
Figure 2.11: (a) Calculated gate leakage current of the GJFET. $I_g$ vs. $N_d$ with $p_0 = 1 \times 10^{12}$ cm$^{-2}$. (b) Calculated $I_{ds}/I_g$ ratio with $p_0$ fixed. Solid lines correspond to left axes: GJFET on $n$-Si. Dash lines correspond to right axes: GJFET on n-4H-SiC.

for a certain application and we need to choose from one of the GJFETs shown in Fig. 2.11. Then there is only one GJFET on $n$-Si can meet the requirement and can be used—the GJFET made on $n$-Si with $N_d = 2 \times 10^{16}$ cm$^{-3}$. Because it has a $V_{Dirac} \approx 3$ V from Fig. 2.9a and it can be biased up to $V_{gs} \approx 5$ V before the leakage runs over the limit. Therefore a trade-off between small $V_{Dirac}$ and high $I_{ds}/I_g$ ratio should be considered carefully when designing GJFET for a specific application.

It should be noted that the $V_{Dirac}$, i.e. the gate voltage corresponding to the minimum channel conductivity, is not always the gate voltage that makes graphene’s Fermi level at the Dirac point. The argument is only true when the hole and the electron have the same mobility. Since the channel conductivity is determined by the combination of electron and hole (Eqn. 2.22), the mobility disparity does affect $I_{ds}$ and thus the $V_{Dirac}$. The $V_{Dirac}$ is shifted toward to a larger value when $\mu_p \mu_n$ (toward the electron-dominating side in the transfer curve), and vice versa. This is often the case as transferred CVD graphene usually has higher hole mobility than electron. The shift in $V_{Dirac}$ can be few volts depending on the degree of disparity and the $N_d$. The $V_{Dirac}$ obtained from the numerical simulation uses the gate voltage at the minimum $I_{ds}$, the same definition as the
$V_{\text{Dirac}}$ obtained in the measurement.

### 2.4.2 Variable depletion width model (VDW)

Now we consider an advanced model of GJFET where the depletion region width ($X_d$) is allowed to vary along the direction of channel length. This situation happens when a higher drain-to-source bias voltage ($V_{ds}$) is applied or when the gate-to-source bias ($V_{gs}$) is low. In this case the effective gate-to-source bias $V_{gs}^{\text{eff}}$ becomes different at each point underneath the graphene channel along the longitudinal direction. At the source end of the channel, since source is always ground, the $V_{gs}^{\text{eff}}$ is still $V_{gs}$. On the drain end the graphene/n-semiconductor heterojunction is maximally reverse biased because GJFET is a p-channel normally-on FET. Therefore $V_{gs}^{\text{eff}}$ at this end becomes $V_{gs} + V_{ds}$. The schematic picture of the gradually varying depletion region width in GJFET is shown in Fig. 2.12. Since space charge density ($Q_{sc}$) is proportional to $X_d$, thus more hole is compensate towards the drain end. The graphene close to drain end would be less p-doped than it is on the source side. Therefore a gradually changing conductivity along channel length exists.

In VDM the channel is analyzed piece-wisely using linear model in each component section. In each section $n(V_{gs}^{\text{eff}})$ and $p(V_{gs}^{\text{eff}})$ is the carrier density, which is a function of local depletion region width, and thus a function of $V_{gs}^{\text{eff}}$. The channel current ($I_{ds}$) now should be modified based on Eqn. 2.23, assuming constant carrier mobility for electron and hole:

$$I_{ds}(V_{gs}^{\text{eff}}) = q\int_0^{V_{ds}} [n(V_{gs}^{\text{eff}}) \cdot \mu_n + p(V_{gs}^{\text{eff}}) \cdot \mu_p] \frac{dV_{ds}}{dL} \cdot W.$$  \hfill (2.25)

Integrate both sides,

$$\int_0^L I_{ds}(V_{gs}^{\text{eff}}) dL = qW \int_0^{V_{ds}} [n(V_{gs}^{\text{eff}}) \cdot \mu_n + p(V_{gs}^{\text{eff}}) \cdot \mu_p] dV_{ds}. \hfill (2.26)$$

Since current should be continuous along the channel, the equation above becomes

$$I_{ds}(V_{gs}) = \frac{qW}{L} \int_0^{V_{ds}} [n(V_{gs}^{\text{eff}}) \cdot \mu_n + p(V_{gs}^{\text{eff}}) \cdot \mu_p] dV_{ds}. \hfill (2.27)$$
Figure 2.12: A GJFET model (VDW) with variable depletion region width ($X_d$).
This is the final result used to simulate the channel current of a GJFET under different $V_{gs}$ and $V_{ds}$.

Simulation results are shown in Fig. 2.13, where output ($I_{ds}$ vs $V_{ds}$ at various $V_{gs}$) and transfer characteristics ($I_{ds}$ vs $V_{gs}$ at various $V_{ds}$) are shown. The $N_d$ and $p_0$ used here are $4.5 \times 10^{15}$ cm$^{-3}$ and $8 \times 10^{11}$ cm$^{-2}$ respectively. The other material parameters and device geometry used for simulation are the same as those used previously. From Fig. 2.13a we can find the output current ($I_{ds}$) is not linear with $V_{ds}$ as assumed in the linear model. Instead, $I_{ds}$ increases with $V_{ds}$ with some slope change at a fixed $V_{gs}$. Under different $V_{gs}$ the change in slope also varies, making some output curves sublinear and some superlinear. The resultant output characteristics have crosses between curves occasionally. We also found the output curve with the lowest slope is close to linear ($V_{gs} = 8$ V). For $V_{gs} < 8$ V the curves are sublinear, while for $V_{gs} > 8$ V the curves are superlinear. This can be explained by the energy band offset within graphene channel. The increase in $V_{gs}$ basically shift the $E_{F,G}$ of the entire graphene channel up towards the Dirac point as a whole. When $V_{ds}$ and $V_{gs}$ are both low, the channel is like the upper part of Fig. 2.13c that the entire channel is $p$-type (with the source end heavily $p$-type and the drain end lightly $p$-type). Therefore the total channel resistance $R_{channel}$ is low and the transfer curve has large slope. When $V_{ds}$ increases but $V_{gs}$ still low, the neutral region of graphene begins to appear in the drain end and moves toward the source side. The total channel resistance is dominated by the high resistance section (neutral region). This makes the $R_{channel}$ start to increase and the slope of transfer curve as a result to decrease. The entire transfer curve becomes sublinear, as described in the second part of Fig. 2.13c. When $V_{gs} = 8$ V, the neutral region appears at the drain end and moves toward the source end for $V_{gs} = 0$–$5$ V and therefore $R_{channel}$ stays nearly unchanged. Therefore the transfer curve at $V_{gs} = 8$ V is close to linear. At higher $V_{gs}$ (> $8$ V) but low $V_{ds}$, the neutral region of graphene appears in the channel already and thus $R_{channel}$ is high, resulting in a smaller slope in transfer curve. This is depicted in the third part of Fig. 2.13c. As $V_{ds}$ increases at high $V_{gs}$, the entire channel becomes $n$-type, just like the opposite case of low $V_{ds}$ and $V_{gs}$. The drain (source) side is heavily (lightly) $n$-doped and the entire channel has a low $R_{channel}$. The slope becomes large again, making the
entire transfer curve superlinear. This is depicted in the bottom of Fig. 2.13c.

The transfer characteristics are also influenced by the effect of energy band offset within graphene channel, making Dirac voltage $V_{\text{Dirac}}$ shift with different $V_{ds}$ bias. This phenomenon is shown in Fig. VDWtransfer. The higher the $V_{ds}$, the lower the $V_{\text{Dirac}}$. This is because higher $V_{ds}$ will more likely make the drain end graphene become neutral as explained previously, and thus $V_{\text{Dirac}}$ appears earlier at higher $V_{ds}$. Also the larger the $V_{ds}$, the larger the $g_m$, but the increase in $g_m$ is not obvious when $V_{ds} \geq 3$ V.

Finally the comparison between linear and variable depletion region width models is also provided at low $V_{ds}$ (0.1 V). These two models yield exactly the same results, suggesting the validity of both models. However it should be noted that linear model only works for low $V_{ds}$ where the energy band offset within graphene channel is not significant. At large $V_{ds}$ or when energy band offset within graphene channel starts to appear, the VDW model should be used to generate a more precise result of simulation.
Figure 2.13: Simulation results of graphene-nSi GJFET using VDW model. (a) Output characteristic. (b) Transfer characteristic. (c) Energy band offset within graphene channel under different $V_{ds}$. Red (blue) represents $p$- ($n$-) type region of graphene. Black: neutral. Glowing means heavily doped region. (d) Comparison between linear and VDW models.
Chapter 3

Fabrication process

The overview of fabrication process used in this thesis is shown in Fig. 3.1. The detail of each step is described in the following sections.

3.1 Graphene fabrication method

There are numerous physical and chemical techniques to produce graphene monolayers and multilayers [96], such as reduced graphene oxide flakes, laser ablation, liquid phase exfoliation of graphite, molecular assembly, and few methods introduced below. However not all of them are cost effective and can produce electronic-device grade graphene that is compatible to current microelectronic fabrication technology, i.e. a uniform number of layers in wafer scale with macroscopically large grain size and low density of defects. As a result in the following paragraphs, three major methods adopted by electronics industry and the academic by now are introduced—mechanical exfoliation, chemical vapor deposition (CVD), and epitaxial growth.

3.1.1 Exfoliation by Scotch tape

The first graphene monolayer was fabricated by repetitive cleaving bulk graphite with an adhesive tape [1]. Graphite—an allotropic of carbon—is composed of numerous graphene layers stacking up into a bulk. Graphene sheets are weakly bounded with each other because the dominating attraction between layers is van der Waal force. In exfoliation process initially the Scotch tape peels multilayers of graphene from the surface of graphite and serves as a support to transfer
as-grown CVD graphene
PMMA coating & graphene separation
device substrate
oxidation, window opening, & back contact
graphene transfer, PMMA removal, anneal, & graphene patterning
top contact

Figure 3.1: The overview of device fabrication process used in this thesis.
the graphene onto other substrate. After transfer onto desired substrate, graphene flakes—pieces of random number of layers—are bounded to the substrate surface by van der Waal force and there is a chance that multilayers of graphene are left at random locations on the substrate after the tape is pulled off. After repeating the same stick-and-pull-off steps, eventually a single layer of graphene can be produced on the substrate surface. This technique is known as Scotch tape method or drawing method for the repeated movement. The graphene produced by mechanical exfoliation demonstrates the best quality as of 2014—lowest number of defects and highest electron mobility—among all fabrication methods. However even this method is still preferred by scientific community for research, it is not feasible from the industrial perspective because the yield of single-layer graphene is very low, the positioning of the graphene flakes is difficult to control, and the size of flakes—few millimeters maximum—is far smaller than wafer scale which is required by industrial manufacture.

3.1.2 Chemical vapor deposition (CVD)

Pure 2D material cannot be formed without the support of a 3D structure—either a sandwich as graphite or a bottom support as a substrate [97]. Exfoliation takes advantage of the former and the CVD (and the method introduced next—epitaxial growth) makes use of the latter. CVD is a preferred fabrication method for large scale manufacture because it produces graphene sheets of large areas—as large as the substrates used—and provides more degrees of freedom to manipulate the synthesis process and the resulting quality of the product.

Synthesizing graphene with CVD involves the use of the following substances: a transition metal substrate as catalyst for the pyrolysis of the reactant gas, inert gas as the carrier, methane as the source of carbon, hydrogen to balance the chemical reactions, and a reactor that operates normally at 1000–1200 °C. Depending on the pressure of synthesis, graphene CVD can be categorized as atmospheric pressure CVD (APCVD), low pressure CVD (LPCVD) which operates below 1 atm, and ultrahigh vacuum CVD (UHVCVD) that is carried out below $10^{-9}$ torr. In general lower pressure yields a better uniformity of numbers of graphene layers—normally fewer layers—
and higher quality. But it also comes with the cost of longer synthesizing time, smaller area of graphene sheets, and higher synthesizing difficulty as the substrate surface is under evaporation simultaneously at low pressure (the vapor pressure of copper and nickel at 1050 °C is approximately $8 \times 10^{-5}$ and $8 \times 10^{-7}$ torr respectively.)

CVD synthesis contains two major steps. The first is the pyrolysis of methane. This is achieved by the catalytic reaction of the transition metal substrate and the carbon containing gas. Without the catalytic substrate, the pyrolysis needs a much higher temperature. Therefore it prevents the carbon cluster from forming in the gas phase and ensures the pyrolysis is only carried out at the substrate surface. The second step is the ordering of the disassociated carbon atoms to form graphene layers. This is achieved by the assist of the lattice of the metal substrate—(111) surface of face-centered cubic crystal—and the properties of the metal used. The most commonly used metal substrates are nickel and copper, both serve the catalytic function but have very different carbon solubility. Nickel is used earlier to demonstrate CVD graphene, but a problem associated with this substrate is that the carbon solubility in nickel is too high at the temperature of the first step. Therefore in order to form graphene, a lowered temperature is needed to precipitate the dissolved carbon atoms to the surface of nickel. This increases the difficulty as it requires stringent control of the temperature and the cooling rate to form few-layer graphene. (The same nature makes nickel a preferred candidate for few-layer graphene production.) Also it is observed that the carbon atoms tend to aggregate in the grain boundaries of nickel, and as temperature drops multi-layer graphene (MLG) are generated at the grain boundaries of nickel substrate. This worsens the overall uniformity of the number of graphene layers produced, and therefore copper becomes a popular choice of substrate for single-layer graphene (SLG) production. Copper on the other hand has very low carbon solubility at the temperature for methane pyrolysis. Only a little amount of carbon can dissolve into copper, and most of the dissociated carbon atoms are forced to stay at the surface to form graphene. Once graphene is formed on the copper surface even at the grain boundaries, the lattice structure of graphene makes it impervious to methane and the pyrolysis stops. This surface-limiting mechanism results in a uniform, single layer graphene growth
on the surface of copper substrate. Despite of the large area and the predominant control of number of layers, there are still few challenges remaining for CVD graphene to be accepted by industrial manufacture. Those challenges include optimizing the grain size, the crystallographic orientation of different grains, ripples, doping levels, and the most important of all, the optimized transfer process that causes the least damages after CVD growth.

An inherent problem of CVD graphene for device fabrication is the separation from the metal substrate where it grows, combined with the following transfer of graphene onto another device substrate. Graphene is considered a potential candidate beyond silicon CMOS scaling technology for its superior electronic properties. Therefore a method to place graphene into a substrate—whether with pre-existing patterns or not—for further fabrication process is a necessity. CVD graphene are tightly bounded to the metal substrate where it is grown and it is difficult to separate them mechanically. To date the interaction between CVD graphene and its substrates are still not fully understood. The most widely used method that can be applied to large scale manufacture is to chemically etch away the metal substrate to release CVD graphene. This is usually achieved by using an additional supporting layer that helps maintain the 2D structure of the released graphene. However the problem associates with the wet etching is that the liquid chemical etchants introduce additional defects and doping to the CVD graphene. A removal step of supporting layer after graphene transfer onto device substrates sometimes introduces more damages to CVD graphene. Despite of the considerable efforts to develop better transfer techniques, an optimized one is still needed and under research for reliable and consistent CVD graphene device fabrication.

Direct growth of graphene on dielectric or semiconductor substrates using modified CVD process such as plasma-enhanced CVD [98] and other physical vapor deposition such as molecular beam epitaxy [99–101] are under research. Those methods are studied in order to eliminate the transfer step required by traditional graphene CVD on transition metal substrate. However they are still in an early stage of development and the quality of graphene produced is not as competitive as the major methods introduced above as of 2014.

In this thesis the graphene sheets used to fabricate all the devices are grown by APCVD
on commercially available copper foil with 10 ppm CH$_4$ in Ar (2400 sccm) and H$_2$ (40 sccm) at 1080 °C for one hour. The resultant graphene flakes are typically 1050 m in diameter as observed with an scanning electron microscope (SEM). Figure 3.2a and b demonstrates the SEM images of as-grown graphene on copper substrate. Graphene grows across the boundary of different grains of copper (indicated by different grey areas in SEM image) achieving large area and has some dendritic boundaries (openings) itself. Nano-particles are a commonly seen by-product that locate randomly on the surface after CVD growth. The landing of those nanoparticles causes the discontinuity (holes) of graphene sheets. The formation of them are not fully understood yet. Raman spectroscopy was employed to ensure the quality of the graphene after CVD growth. Example Raman spectra of different batches of as-grown CVD graphene are shown in Fig. 3.2c after subtracting the signal from copper substrate. The spectra show only distinct G and 2D peaks without other defect-activated peaks.

3.1.3 Epitaxial growth—controlled silicon sublimation of SiC

Graphene can be produced on hexagonal-latticed silicon carbide substrate by silicon sublimation at high temperature, typically beyond 1050 °C at ultra high vacuum and 1500 °C at atmospheric pressure in argon. The sublimation is sometimes carried out in a confined graphite enclosure so that the growth of graphene is close to thermal dynamic equilibrium. Because of the hexagonal lattice in both (0001) Si-face and (0001) C-face and the carbon-containing composition, silicon carbide (as shown in Fig. 1.1c) serves as an ideal template to produce wafer-scale graphene known as epitaxial graphene. During the sublimation of silicon atoms the remaining carbon atoms rearrange themselves based on the hexagonal lattice plane underneath to form graphite like carbon layers—despite of the large lattice mismatch that is prone to induce defects. Since this sublimation is not a self-limiting process, the growth of a uniform SLG or MLG depends on several factors: the surface polarity of SiC substrate used—either C-face or Si-face, the surface morphology of the substrate, and the growth environment including the growth time, surrounding gases, temperature, and pressure.
Figure 3.2: (a),(b) SEM images of as-grown APCVD graphene on copper substrate, and (c) Raman spectra of different batches of as-grown APCVD graphene (the background signal of copper has been subtracted.)
In a general sense C-face of silicon carbide substrate has a higher graphitization rate as a result of its carbon-rich nature. However the poor surface morphology—typically tens of microns laterally and several hundreds of nanometer vertically—of the C-face at high temperature inevitably generates graphene sheets with small grain sizes and poor uniformity of number of layers. Si-face on the other hand has slower graphitization rate, but the suppressed molecular dynamics favors the larger surface steps and thus enhances the uniformity of number of graphene layers [102].

The adhesion between epitaxial graphene and silicon carbide is strong, making it difficult to mechanically separate epitaxial graphene from substrate. Also the lack of efficient etchant to selectively etch silicon carbide substrate makes it impossible to release epitaxial graphene via etching. For this reason most electronic devices based on epitaxial graphene are made with standard microfabrication process directly on top of the silicon carbide substrate. Also the interface between graphene and silicon carbide is charged, regardless of surface polarity, resulting in an n-type first layer of graphene (negatively charged on the order of $5 \times 10^{12} - 1 \times 10^{13}$ cm$^{-2}$) [103].

The interaction between epitaxial graphene and silicon carbide substrate is different for Si and C terminated faces and has profound influence on carrier mobility. The interaction on Si-face is strong because about 30% of the carbon atoms in graphene are covalently bonded to underlying silicon atoms [104]. The electronic properties of such epitaxial graphene are inferior due to reduced number of $\pi$-electrons. The problem can be addressed by hydrogen intercalation, forming quasi-free-standing graphene [104]. On the other hand the interaction of epitaxial graphene and C-face is much weaker. Also the highly random orientations of each domain make adjacent graphene decouple with each other, causing multilayer epitaxial graphene on C-face to behave like isolated single-layer graphene [105]. This effect is also reflected in the higher carrier mobility of epitaxial graphene on C-face than on Si-face.
3.2 Graphene transfer process

As CVD becomes the mainstream method to produce large-area, high uniformity, and high quality graphene, the methods to transfer graphene reliably onto any device substrate are developed [106]. The most widely adopted transfer method is polymer supported etching and transfer method, which contains four steps: coating of supporting polymer, separation of graphene, transfer, and removal of the polymer.

As the name suggests, a thin layer of polymer is coated on graphene to mechanically hold and support graphene through the following steps. The most widely used polymer is Poly(methyl methacrylate), PMMA, because of its good adhesion with graphene, ease of coating, and the good resultant graphene with less cracks [107].

The separation step is usually done by etching away the growth substrate of transition metal. However, the etchant of substrate would cause chemical contamination of unwanted doping to graphene. Therefore another bubbling method is developed [108]. The method is basically electrolysis of water with PMMA/graphene/metal composite as one of the electrode. The electrolysis of water generates gaseous hydrogen and oxygen at the metal surface that separate PMMA/graphene and metal. Therefore, it is more like a mechanical peeling-off separation which causes less chemical contamination but more mechanical defects. The advantage of it is that metal growth substrate is not damaged and reusable, which is important if precious metal is used. Reused metal substrate also has larger grain size after going through high-temperature thermal cycle of graphene growth, which can be potential for growing higher quality graphene sheet. The graphene sheets used to make devices in this thesis were peeled off from copper foil with a PMMA supporting layer by electrolysis in a diluted KOH solution (<0.1 M).

The transfer process is typically done in DI water, in which PMMA/graphene composite is rinsed thoroughly to remove the contamination from previous step as much as possible. The device substrate is then placed underneath PMMA/graphene and pulled out of DI water slowly so that PMMA/graphene stays on the surface of device substrate. This scoop-up step completes the
transfer process. The final step is to remove the supporting layer—the PMMA layer—by dipping the PMMA/ graphene/device substrate composite in organic solvent such as acetone.
3.3 Graphene anneal

PMMA as a supporting layer for transfer process is difficult to be completely removed by solvent only. As a result an additional thermal annealing step is often needed to thermally decompose PMMA molecules. The graphene annealing process used in fabricating devices in this thesis is carried out in atmospheric pressure of Ar and H\textsubscript{2} (both 40 sccm) at 300 °C for one hour. However even after thermal annealing, it is found that PMMA is not removed entirely, and it reacts with graphene and produces some local rehybridization of carbon atoms that affects graphene’s band structure [109]. Overall by considering the aforementioned drawbacks, the state-of-the-art transfer process is still not optimized and will need more research effort to improve the quality of transferred graphene.

3.4 Oxidation of semiconductor substrate

Device substrates (\textit{n}-type Si and 4H-SiC) are oxidized to form an amorphous SiO\textsubscript{2} layer with specific thickness. The SiO\textsubscript{2} serves as an insulating layer among devices on the same substrate. It also separates the top contacts from each other and from the substrate. The thickness of SiO\textsubscript{2} is chosen to optimize the optical contrast of SLG for optical microscope observation, as described in Chapter 1. For graphene/SiO\textsubscript{2}/\textit{n}-Si, the thickness of SiO\textsubscript{2} is ∼90 nm; for graphene/SiO\textsubscript{2}/\textit{n}-4H-SiC, the thickness of SiO\textsubscript{2} is ∼80 nm.

The oxidation is done inside a quartz tube furnace. Before oxidation, device substrates are thoroughly cleaned by sonication in acetone, isopropyl alcohol, and DI water to remove particles and grease. The substrates are then dipped in heated Nanostrip for 20 minutes to remove metal ions and organic contaminants. The final step of cleaning is a quick dip in fresh buffered oxide etchant to remove any native oxide. The oxidation condition for \textit{n}-Si is 1150 °C for 33 minutes in dry oxygen. For \textit{n}-4H-SiC the oxidation temperature is 1200°C and the time is 1 hour for C-face and 4.5 hour for Si-face in dry oxygen. A chart of experimental dry oxidation thickness for 4H-SiC is shown in Fig. 3.3. Our experiment shows that Si-face has a slower oxidation rate than C-face,
with a SiO₂ thickness ratio about 1:6 for the same oxidation time at the same temperature.

Figure 3.3: Experimental dry oxidation thickness for 4H-SiC.
3.5 Metalization

The back contact metal to $n$-type Si and 4H-SiC is Al and Ni (both 100 nm) respectively. The same cleaning process as described in 3.4 is performed before back contact is deposited by thermal evaporation at a base pressure of $<5 \times 10^{-6}$ torr. As-deposited Ni/$n$-4H-SiC contact exhibits rectifying (Schottky) behavior and requires a thermal anneal at 1000 °C in forming gas to become nonrectifying (ohmic).

The top contacts to graphene used in this thesis is Cr/Au (5/100 nm) deposited by the same thermal evaporation method used for back contact. Because of the lack of bandgap, graphene naturally forms ohmic contact with any any metal deposited on top of it. However an important issue is of the metal contact the adhesion with graphene. Ideally graphene has very low surface energy and a nonpolar surface without dangling bonds. The adhesion would be poor by only physical adsorption—if dominated by van der Waal force only. Ni was used in our early experiment, but we found that Ni electrode on graphene is very easily peeled off by the lift-off process used to define the electrodes (Fig. 3.4). Even large Ni pads were unable to survive through the electrical test on probe station. Therefore we switched to Cr/Au which has good adhesion on graphene as well as low contact ressistance.

![SEM image](image.png)

Figure 3.4: A SEM image showing the poor adhesion of Ni electrode on graphene after lift-off.
To assess the contact resistance of the metal-to-graphene contact in our device, a transfer length method (TLM) structure is used. The structure is composed of patterned graphene stripe with metal electrodes on its two ends as shown in Fig. 3.5. The geometry of graphene stripe was defined by photolithography and oxygen plasma dry etch. The metal electrode was then defined by thermal evaporation and lift-off. The length and width of the stripe is varied, and the total electrical resistance between two electrodes can be described by

$$R_{total} = 2R_c + R_{sh} \frac{L}{W},$$

where $R_c$ is the contact resistance in $\Omega$, $R_{sh}$ is the sheet resistance of graphene stripe in $\Omega/\square$, $L$ is the length of graphene stripe between two electrode, and $W$ is the width of graphene stripe. Equation 3.1 can be rearranged in the following form to include various $L$ and $W$ of graphene

![Diagram](image-url)

Figure 3.5: Top: Schematic structure of a Transfer length method (TLM) structure. Bottom: a plot of metal-to-graphene TLM results.
In this equation, the parameter $R_c \cdot W$ is extracted at $L = 0$ as width-normalized contact resistance. This $R_c \cdot W$—with an unit of $\Omega$-cm—is commonly seen in the literature of graphene related studies. It is because the contact resistance to graphene is dominated by contact edge width as a result of graphene’s 2D nature [110] as opposed to conventional 3D semiconductors to which the contact resistance is dominated by contact area. However standard analysis of metal-to-semiconductor contact still applies to metal-to-graphene contacts [111]. Other normalized parameters such as contact resistivity $\rho_c$ (or referred to as specific contact resistance) with an unit of $\Omega$-cm$^2$ and transfer length $\lambda = \sqrt{\frac{\rho_c}{R_{sh}}}$ which is the current penetration depth from the edge into the bottom of the metal contact can be obtained.

An ideal plot of $R_{total} \cdot W$ vs. $L$ should look like the black line at the bottom of Fig. 3.5. As $L$ and $W$ varies, the ideal $R_{total} \cdot W$ values fall into a straight line whose slope is $R_{sh}$. At $L = 0$, assuming sufficient contact length ($L_c > 1.5\lambda$), we obtain twice the width-normalized contact resistance

$$2R_c \cdot W = 2\sqrt{\rho_c R_{sh} \coth(\frac{L_c}{\lambda})}$$

$$\approx 2\sqrt{\rho_c R_{sh}}.$$  

And with the value of $R_{sh}$ the contact resistivity $\rho_c$ and transfer length $\lambda$ can be extracted using the equation above.

Nonetheless in reality the graphene stripes are not always free of defect. A great chance is that microscopic cracks (as can be seen from the SEM images in Fig. 3.2) would exist in the graphene stripes of TLM structure, which lowers the effective width of the stripes. (Transfered CVD graphene with PMMA also introduce additional unwanted cracks and ripples.) Cracks are even more likely to exist in long TLM structures. Those cracks increase the total resistance as well as the slope $R_{sh}$ of TLM data. However the y-intercept ($2R_c \cdot W$) should not change much due to cracks as long as the metal contact length and width are much larger than the crack size. The
effect of microscopic cracks on TLM result is shown as the red line in Fig. 3.5. Therefore from the
statistic point of view only those data points that yield a good linear fit with lowest slope should
be considered valid. The resulting straight fitting line with lowest slope then gives us the contact
parameters close to ideal values without cracks.
3.6 Device structures (mask layout)

The mask layout used to fabricate devices studied in this thesis is shown in Fig. 3.6. The graphene/$n$-semiconductor Schottky diodes (SDs) and bottom-gated G-JFETs require only three masks to make. The first is the window-opening mask (green filled regions) that uncovers bare semiconductor surface from the thermally grown oxide. After windows are opened, CVD graphene is transferred onto the device substrate to form graphene/$n$-semiconductor heterojunction. Then the PMMA is removed and graphene is annealed. The second mask (red hatch-lined regions) is then used to pattern active graphene regions where only active graphene/$n$-semiconductor heterojunction and the areas to form metal ohmic contact are left. Then the third mask (blue hatch-lined regions) is to define the metal ohmic contact to graphene and pads for electrical test.

The zoom-in layout and the corresponding cross-sectional device structure for discrete graphene/$n$-semiconductor SDs and G-JFETs are shown in Fig. 3.7. Device SD A is a conventional Schottky diode formed by metal-to-$n$-semiconductor. It serves as a control device to provide a performance baseline to be compared. Device SD B is formed by graphene/$n$-semiconductor heterojunction with the metal contact directly covering the active region. Device SD C is formed by graphene/$n$-semiconductor heterojunction with a remote metal contact separate by thermal oxide. Some large-area Schottky diodes (350×350 µm$^2$) with structures of SD A, B, and C are also made as shown in Fig. 3.8.

For three terminal devices, G-MOSFET is fabricated with graphene sheets sitting on thermal oxide. It serves as a control device and can also be used as TLM sturcture to extract metal-to-graphene contact information. G-JFET A has a contact geometry the same as device SD C with a remote metal contact separate by thermal oxide. G-JFET B has a contact geometry the same as device SD B with with the metal contacts directly sitting on top of graphene. G-JFET C is the improved version that combines the advantages and excludes the drawbacks (leakage paths) from both G-JFET A and B.
Figure 3.6: Overview of mask layout for devices and test structures.

Figure 3.7: Mask layout for discrete devices and their cross-sectional structures.
Figure 3.8: Mask layout for alignment marks and large-area diodes.
Chapter 4

Characterization and analysis of graphene-semiconductor heterojunction

In this chapter, the properties of fabricated graphene-semiconductor heterojunctions will be characterized and analyzed with electrical measurement. The basic mechanism will be examined and the properties will be explored as functional devices.

A Schottky-like heterojunction forms when graphene and semiconductor are put in direct contact due to their work function difference [60, 61, 63], and it is conventionally referred to as a Schottky diode (SD). Graphene-semiconductor SD is of our interest as it is the critical component of a GJFET—the gate that determines the switching mechanism. The graphene-semiconductor SD itself is also of interest as a two-terminal device due to graphene’s peculiar optical and electronic properties. The heterojunction has good rectifying behavior, meaning a low dark current under reverse bias, making it suitable for light detection application. For this reason, the infrared photodiode (IR PD) based on a graphene-Si heterojunction will be explored later in this chapter. The characterization and analysis begin with the basic electrical characterization of the graphene-$n$-Si Schottky diode.

4.1 Graphene/$n$-silicon Schottky diode

Three types of SDs are fabricated for comparison. The details of fabrication process are described in the previous chapter. The first one, Schottky diode A (SD A) is a traditional metal-to-semiconductor Schottky diode formed by Cr/Au on $n$Si. The second one, Schottky diode B (SD B) has a structure the same as SD A except for an additional graphene layer inserted between the
Figure 4.1: Schematic device structures of graphene/n-semiconductor Schottky diodes

Cr/Au and the nSi, forming a Cr/Au-graphene-nSi structure. The last one, Schottky diode C (SD C), is formed by graphene on nSi directly and has its Cr/Au contact sitting on top of the oxide layer. The schematic device structures for all three types of SDs are shown in Fig. 4.1.

The n-Si substrate used for device fabrication is phosphorous doped, 2-inch prime grade wafer finished with (100) surface. The doping density \( N_d \) is determined by four-point probe (FPP) and C-V measurement with large-area Cr/Au pads. The results are shown in Fig. 4.2: both methods yield an \( N_d \) of around \( 4.5 \times 10^{15} \text{ cm}^{-3} \).

4.1.1 Current-voltage (I-V) characteristics of graphene-nSi Schottky diodes

The collective \( J-V \) curves for each type of SD respectively are shown in Fig. 4.3a–c, and a comparison among three is shown in Fig. SDcomparison. For analysis the current is normalized to the device area, and therefore \( J \) is shown instead of \( I \). The variation of the \( J-V \) curves of SD B and C can be contributed to nonuniform graphene coverage. The graphene sheet grown by APCVD is not 100% continuous, and the coverage is even worsen by the cracks/holes introduced in the transfer process. For this reason, the SBH of SD B thus has nonuniformity as some device area is Cr/Au-nSi instead of Cr/Au-graphene-nSi. Moreover the effective device area of SD C becomes smaller than expected, resulting in an overestimated \( J \) of SD C with ideal device area. An unusual
kink appears in the $J-V$ curves of SD C, which will be examined by optical response measurement and discussed later.

### 4.1.1.1 Analysis

As discussed in 2.2, the current flowing through a Schottky junction is dominated by thermionic emission, which can be expressed as the equation:

$$I = A A^* T^2 e^{-\frac{q \phi_B}{k_B T}} \cdot (e^{\frac{q V}{\eta k_B T}} - 1)$$

where $A$ is the junction area, $A^*$ is the Richardson constant of semiconductor substrate, $T$ is the temperature, $q$ is electron charge, $q \phi_B$ is the Schottky barrier height (SBH), $k_B$ is Boltzmann’s constant, $V$ is the applied voltage, and $\eta$ is the ideality factor. In the equation, there are two parameters of interest. The first is the ideality factor $\eta$ that determines the degree of thermionic emission at the interface. Ideally when the current is 100% dominated by thermionic emission, then $\eta = 1$. However this ideal case does not exist in most of Schottky junctions in reality. Other carrier transport mechanism occurs and contributes to the current as well, such as the majority carrier tunneling through the Schottky barrier. Therefore the $\eta$ increases as the tunneling part increases,
Figure 4.3: \(J-V\) characteristics of (a) SD A, (b) SD B, (c) SD C, and (d) the comparison of representative diodes of each type. The data was obtained in the dark at room temperature resulting in an \(\eta\) typically around 2 for metal-to-Si Schottky diodes [59]. The \(\eta\) can be extracted from the slope of the straight line of an \(I-V\) curve in semi-logarithmic scale. This straight line region typically only exists under small forward bias (\(V > 0\)) region. Under large forward bias, the series resistance begins to limit the current and thus the \(I-V\) curve turns into linear. From low forward bias region, the \(\eta\) can be extracted from the equation

\[
\eta = \frac{q}{k_B T} \left( \frac{1}{\text{slope}} \right). \tag{4.2}
\]
Depending on the series resistance, this straight region can be very narrow, limiting the accuracy of the "slope" method discussed above. An analytical method is reported by Cheung [112], which uses the series-resistance-dominating region to extract the parameters of a Schottky junction, such as $\eta$ by linear fitting of the $\frac{dV}{d\ln(V)}$ vs. $J$ plot.

With this method, the average $\eta$ for SD A (4 diodes), B (22 diodes), and C (22 diodes) are extracted as $2.8 \pm 0.12$, $3 \pm 0.8$, and $2.9 \pm 0.8$, respectively. The similarity of $\eta \sim 3$ indicates that the current transport mechanism is dominated by a significant tunneling portion in all three SDs. Since the substrate doping is not high, the tunneling may appear as a result of an interfacial layer, which will be further examined by light illumination later. The rectification current ratio—a figure of merit that evaluates the diode performance—for SD A (4 diodes), B (22 diodes), and C (22 diodes) at $\pm 3$ V are $10^3$, $10^4$–$10^5$, and $10^5$–$10^6$ respectively. Device SD C here has the best rectifying performance as the retification is two to threes of magnitude higher than a traditional metal-semiconductor Schottky junction. This high rectification is an indication of higher SBH. The same conclusion can be drawn from the comparison, 4.3d, where the lowest current density of SD C implies the highest Schottky Barrier Height (SBH).

### 4.1.2 Temperature dependence of graphene-$n$Si Schottky diodes

Although the $J$-$V$ characteristics provide qualitative information about the SBHs of a trend of $q\phi_{B,SD\ C} > q\phi_{B,SD\ B} > q\phi_{B,SD\ A}$, additional temperature-dependent $I$-$V$ measurement is performed to extract SBH of each type of Schottky diode quantitatively. The results are shown in Fig. 4.4.

#### 4.1.2.1 Analysis

Based on Eqn. 4.1, when the diode is under large reverse bias ($-V \gg 3kT$), the magnitude of the current is simplified as:

$$I = AA^* T^2 e^{-\frac{\phi_B}{k_BT}}. \quad (4.3)$$
Figure 4.4: Temperature-dependent $I$-$V$ characteristics of (a) SD A, (b) SD B, and (c) SD C; the insets are Richardson plots with linear fittings for each diode at various reverse biases. (d) The extracted SBHs as a function of reverse-bias voltage.

If we plot $\ln\left(\frac{I}{T^2}\right)$ vs. $\frac{1}{T}$, the result should be a straight line with a slope of $-\frac{q\phi_B}{k_B}$, from which the SBH can be extracted. This plot is referred to as Richardson plot. The results of temperature-dependent $I$-$V$ measurement for each type of SDs with such analyzing technique are shown in Fig. 4.4. The reverse-bias current of all diodes increases smoothly with temperature as expected (Fig. 4.4a–c). The Richardson plots for each diode at different reverse-bias voltages exhibited nice linear behavior shown in the insets. Finally the extracted SBHs of all diodes as a function of reverse-bias voltage.
voltage are shown in Fig.4.4d for comparison. Device SD C has a distinctly larger SBH than those of SD B and C, and between the two, SD B has a larger SBH than that of SD A. The results showed a highest SBH formed between the graphene and the semiconductor, while the SBH between the metal and the semiconductor is the lowest. With a graphene sheet inserted between the metal and the semiconductor, the SBH is enhanced by about 20%. It is also observed that SD A and B have similar slope of decreasing SBH with reverse-bias voltage, while SD C has a slope more than twice as high. Further analysis showed that the SBHs of SD A and B both decreases by \( \sim 0.02 \text{ eV} \) from -1 to -3 V, corresponding well to 0.028 eV predicted by image-force lowering [59]. However, the SBH of SD C decreases by \( \sim 0.06 \text{ eV} \).

The results obtained here are reasonable due to graphene’s low density of state compared with metal. When graphene and metal are in contact, graphene is doped by the charge transfer [70] and thus graphene’s Fermi level is pulled close to that of metal. Since device SD B has a structure of metal on graphene on semiconductor, the graphene in this case is expected to behave similar to the metal on its top. This explains why SD A and SD B have similar SBHs and why both SBHs decreases alike as a function of reverse-bias voltage. Device SD C, however, is composed by graphene-semiconductor junction only, without the metal on top of graphene. The contact is remote from the junction and thus the doping from the metal does not affect the junction area. This makes the SBH in device SD C is determined solely by the energy difference between graphene’s Fermi level and the conduction band edge of the semiconductor. The conduction band edge of semiconductor in a Schottky barrier is bent by image charge, responsible for image-force lowering. Therefore the additional SBH decrease must come from graphene’s Fermi level shift due to its low density of state. As reverse bias increases, the expanding depletion region in semiconductor contains increasing positive space charge, thus inducing more electrons inside graphene. This results in a upward-shifting Fermi level, and thus decreases the measured SBH. Also, it is worth mentioning that this is the desired property for a graphene junction field-effect transistor. The Fermi level shift by the reverse bias is exactly the gate mechanism that switches graphene’s conductivity.
4.2 Photodiode—Graphene-$n$Si heterojunction diode

As discussed in 1.1.1.6, graphene’s unique band structure yields a 2.3% optical absorption of normally incident light across the entire visible spectrum, up to mid infrared region. The sensor of light—graphene photodetector—is developed based on this property. Most graphene photodetectors use a back-gated MOS structure, operating in photoconductor scheme, and thus have a large dark current due to graphene’s zero bandgap. On the contrary, the photodiode (PD) operates in the reverse-bias region of the graphene-semiconductor heterojunction, thus exhibiting low dark current due to the blocking Schottky barrier. In this section, the graphene-$n$Si heterojunctions will explored as a photodiode (PD). The device structures are the same as those characterized in the previous section (Fig. 4.1), i.e. PD A (Cr/Au-$n$Si), PD B (Cr/Au-graphene-$n$Si), and PD C (graphene-$n$Si).

4.2.1 Response to visible white light

The photo responses of PDs to different intensities of white light are shown in Fig. 4.5. The light source is the incandescent bulb on the probe station. The results here are expected to provide qualitative information about the SDs and the interfaces.

The $I-V$ characteristics of all three PDs exhibited a kink at around -1.8 V. This kink indicates the existence of a thin interfacial layer, which was studied and used in metal-insulator-semiconductor (MIS) tunnel diodes for current multiplication and photovoltaics [113, 114]. We suspect the formation of this thin tunnel oxide in our devices was due to the graphene transfer process in DI water. We confirmed an 1–2nm thick oxide layer formed by dipping a freshly exposed Si surface in DI water for 20 minutes. This tunnel oxide does consume a very small voltage drop and add an additional probability term to the current equation (Eqn. 4.1), making the current smaller and increasing the ideality factor $\eta$. Yet overall, the basic operation mechanism of the PDs still works, such as the formation of depletion region in $n$Si and graphene’s Fermi level shift by reverse-bias voltage, etc.

In device PD A, the absorbing area only exists on the edges of metal electrode, and thus
the optical response is very weak due to the small active area of about $1 \times 10 \, \mu \text{m}^2$. The large dark current of PD A also clouds the optical response as a result of its lowest SBH. **Device PD B** has similar active area ($\sim 1 \times 10 \, \mu \text{m}^2$) that also only exists close to the edges of metal electrode. But
due to its larger SBH as well as the existence of graphene sheet, the dark current is much lower and the absorption is higher than those of SD A. This can be observed as the clearer photocurrent vs.
the dark current in PD B. **Device PD C** has the strongest and the most distinct optical response, while having about the same active area ($\sim 3 \times 5 \, \mu m^2$) as PD B. This is contributed to its highest SBH and thus the lowest dark current.

The PD operation mechanism is shown in Fig. 4.5d. When the PD is in the dark, the blocking SBH prevents the majority carrier from passing through the interface, resulting in a low dark current provided a large SBH. When PDs are under illumination of white light, the photons are absorbed in two regions: the graphene and the depletion region in semiconductor (for short wavelength), both creating excited electron-hole pairs that are separated by the electric field at the interface (or inside the depletion region if absorption occurs in semiconductor). After separation, electrons and holes are driven by the electric field and flow toward $n$Si and the graphene respectively, where they become the majority carriers and are collected by the metal electrodes (photocurrent). On the same substrate, a larger SBH has higher interfacial electric field, and thus favors the electron-hole pair separation and collection. This corresponds well to the conclusion from previous section that $q\phi_{B,SDC} > q\phi_{B,SDB}$, and explains why PD C has the larger photocurrent than PD B.

### 4.2.2 Response to 1.3 $\mu$m light

What really interests us is the application of graphene-semiconductor heterojunction photodiode in the regime of wavelength that is transparent to the semiconductor. The graphene-Si heterojunction PD has great potential for monolithically integrated Si photonics that can enhance the bandwidth of data transfer with much higher efficiency than traditional electrical interconnect [88–90]. The current technology for the receiver end in Si photonics uses Ge p-i-n PDs. However the the main challenge of integrating Ge into Si by epitaxial growth is the large lattice mismatch 4.2%, which prohibits low defect, high quality Ge layers. Two major bands used in fiber-optic telecommunication are O band (1260–1360 nm) and C band (1530–1565 nm) because the former has the lowest dispersion and the latter has the lowest attenuation in commercial silica
optical fiber. For this reason, we test our PDs with 1.3 and 1.55\(\mu m\) infrared (IR) illumination.

In this section, PD C (Fig. 4.1) with an active area of 3 × 5 \(\mu m^2\) will be tested as the device of interest because it has the highest SBH, providing the lowest dark current and the most efficient carrier separation and collection based on the results from the previous section. The optical response of PD C under calibrated 1.3\(\mu m\) illumination with different intensities is shown in Fig. 4.6a. The device PD C is operated under reverse bias, exhibiting a good linear photocurrent increase with 1.3\(\mu m\) IR illumination intensity. To characterize its performance as an IR detector, some figures of merit (FOM) are calculated and shown in Fig. 4.6b–d. The first is the responsivity (\(\mathcal{R}\)) measuring the capability of the device to convert incident optical power to photocurrent, which is defined as

\[
\mathcal{R} = \frac{I_{\text{photo}} - I_{\text{dark}}}{P_{\text{opt}}} \text{ in A/W.} 
\]  

Another similar FOM is the internal quantum efficiency (IQE), measuring the efficiency of the device to convert absorbed photons into collectable carriers.

\[
\text{IQE} = \frac{(I_{\text{photo}} - I_{\text{dark}})/q}{(P_{\text{opt}} \times 2.3\%)/h\nu} \text{ in \%.} 
\]  

The third is the noise-equivalent power (NEP), measuring the sensitivity of the PD. It is defined as the minimum detectable optical power to generate a photocurrent that equals the root-mean-square noise current in one-hertz output bandwidth.

\[
\text{NEP} = \frac{\sqrt{2q \cdot I_{\text{dark}}}}{\mathcal{R}} \text{ in pW/Hz}^{0.5}. 
\]  

The last one is the specific detectivity (\(D^*\)), measuring the performance of the device similar to NEP, but it is normalized to the device area as well as the bandwidth of measurement, and thus yielding a material-genic FOM independent of device size, measurement condition, etc.

\[
D^* = \frac{\sqrt{Af}}{\text{NEP}} \text{ in cm-Hz}^{0.5}/\text{W,} 
\]  

where \(A\) is the device active area and \(f\) is the measurement bandwidth (\(f = \frac{1}{2\Delta t}, \Delta t = \text{integration time}\)).
From Fig. 4.6, it is found that graphene-$n$Si heterojunction PD has a $\mathcal{R}$ of about 3.3 mA/W, corresponding to an $IQE$ of $\sim 14\%$. This $\mathcal{R}$ matches most reported values of graphene photodetectors under normal illumination [65,66,72,79], which is about an order of magnitude lower than commercial Ge PDs that typically have a $\mathcal{R}$ on the order of $10^{-1}$ A/W. This low $\mathcal{R}$ is due to the low optical absorption (only 2.3%) of a single layer of graphene. On the other hand, the graphene-$n$Si heterojunction PD has very low $NEP$ and high $D^*$—on the order of pW/Hz$^{0.5}$ and $10^9$ cm-Hz$^{0.5}$/W.
respectively—as good as those commercially available discrete Ge photodiodes (e.g. FDG-series Ge photodiode for NIR wavelength from Thorlabs Inc.).

4.2.3 Response to 1.55 \( \mu \text{m} \) light

The optical response of the graphene-\( n \)Si heterojunction PD under different 1.55\( \mu \text{m} \) illumination intensity is shown in Fig. 4.7a and the corresponding FOM are calculated and shown in Fig. 4.7b–d.

Overall, the performance is about an order of magnitude inferior than that under 1.3\( \mu \text{m} \) illumination. This is understandable from the band structure of the PD, as shown in Fig 4.8.

Since graphene has an electron affinity of \( \sim 4.6 \text{ eV} \) [49], the position of the Dirac point sits at the middle of the bandgap of Si. After graphene absorbs a photon with energy of \( h\nu \), electron and hole are excited in the conduction and valence band with energy of \( +\frac{h\nu}{2} \) and \( -\frac{h\nu}{2} \) relative to the Dirac point, respectively. From 4.1.2, we found the PD has a SBH of about 0.65 eV under reverse bias. Therefore when IR light is shone on the device, excited electron sees an effective SBH of 0.175 eV under 1.3\( \mu \text{m} \) and an effective SBH of 0.25 eV under 1.55\( \mu \text{m} \) illumination, respectively. The effective barrier width is also thinner in the case of 1.3\( \mu \text{m} \) illumination as the excited electron is closer to the apex of the Schottky barrier. The combined effects of lower effective SBH and width thus result in better FOM in the case of 1.3\( \mu \text{m} \) illumination.

4.2.4 Competing mechanisms that affect the internal quantum efficiency

The responsivity (and thus the internal quantum efficiency) for our graphene-\( n \)Si IR PD under 1.3\( \mu \text{m} \) illumination is comparable to what the literature obtains (typically \( \mathcal{R} \sim \text{mA/W} \) and \( IQE \sim 6–16\% \)) using vertically incident light and the graphene as the absorbing medium [65,66]. In the planar structure such as a graphene photoconductor, the low \( IQE \) is a result of the short photocarrier lifetime, on the time scale of 100 fs [115–117]. The photogenerated carriers must be separated by the electric field inside the graphene plane and collected in the electrodes within this period of time in order to become the photocurrent. This collection efficiency—\( IQE \)—is determined
Figure 4.7: (a) Optical response of PD C under calibrated 1.55 μm illumination with different intensities. (b) Responsivity and internal quantum efficiency. (c) Noise equivalent power, and (d) Specific Detectivity.
by the velocity of carriers and the length of the graphene across which they have to travel. For a graphene channel of 1 \( \mu \text{m} \) in length, with a carrier saturation velocity of \( 5.5 \times 10^7 \text{ cm/s} \), the time of traveling is about 1.8 ps which is about an order larger than the the photocarrier lifetime. This explains the low \( IQE \sim 10\% \) in the planar graphene photodetectors, because most of the hot electrons cannot make it to the electrode and lose their energy to optical phonons.

The same mechanism applies to our graphene-nSi IR PD, but the photogenerated hot electrons in this case travel in the direction perpendicular to the graphene plane into the conduction band of the semiconductor to become photocurrent. This carrier transport process is hampered by an effective SBH, but it is also with the assistance of the interfacial electric field pointing from semiconductor to the graphene. In addition, the distance that hot electrons needs to travel (the width of the effective barrier width) is much shorter than the lateral dimension of a graphene channel. All these competing mechanisms result in a comparable \( R \) and \( IQE \) in the graphene-nSi heterojunction IR PD.
4.3 Summary

In this chapter, the graphene-$n$Si heterojunction demonstrates promising properties as photodetector, especially in the wavelength for fiber-optic communication. By placing graphene on top of Si surface, the heterojunction exhibits great rectifying behavior and fair optical responsiveness. In Si photonic circuits, the signal is carried by IR light and guided by Si waveguides and ring resonators. Since Si is transparent to the IR light, Ge with smaller bandgap is used as the choice of PD material. However, integrating Ge PDs or epitaxially grow Ge PD on Si wafer is challenging due to the large lattice and thermal mismatch, and the aggressive cleaning process for Ge.

On the contrary, the graphene-Si heterojunction PD can be made by simply placing graphene on Si waveguides. The simpleness of the device structure and the ease of integration with Si CMOS technology make graphene-Si heterojunction PD a viable solution for monolithically integrated Si photonics. More important, the inherent low optical absorption of graphene can be hugely increases by the waveguide structure. Since IR light travels laterally along the graphene plane rather than vertically, the absorption length can be easily boost from the order of angstrom to micrometer while keeping the device active area the same. Doing so maintains the dark current while greatly increases the responsivity and other FOM. The literature has shown a two-orders-of-magnitude increase in the $\Re$ (to the order of 0.1 A/W) by using the waveguide structure [75–77, 87]. Such graphene-Si heterojunction PD on the Si waveguide is potential for realizing a critical component of integrated Si photonic interconnect.
Chapter 5

Characterization and analysis of graphene junction field-effect transistor (GJFET)

Graphene is considered as a potential channel material for high-speed electronics due to its high carrier mobility and transconductance. In this chapter we will explore a novel graphene transistor based on a graphene-semiconductor heterojunction—graphene junction field-effect transistor (GJFET).

5.1 Graphene metal-oxide-semiconductor field-effect transistor (G-MOSFET)

A graphene metal-oxide-semiconductor field-effect transistor (G-MOSFET) was fabricated with APCVD-grown graphene on a $p^+\text{-Si } (N_D=10^{19} \text{ cm}^{-3})$ with 90nm thermal oxide layer. It was tested as a control device and to provide a baseline for later comparison. The schematic structure and the optical images of fabricated G-MOSFETs are shown in Fig. 5.1. The gate oxide is 90nm thick to maximize the visibility of graphene. The field oxide is thinned from gate oxide layer to visualize the channel region.

5.1.1 Analysis

The measured transfer characteristic of the G-MOSFET is shown in Fig. 5.2a. The device is an initially-on (depletion mode) FET as expected, and thus it requires a positive gate bias $V_{GS}$ to turn the channel off. The G-MOSFET showed an on/off ratio of 5.8, despite the need of a huge $V_{GS}$ swing of $\sim100$ V. The Dirac voltage $V_{Dirac}$ appeared at $V_{GS} = +49$ V, corresponding to an
Figure 5.1: (a) Device structure of fabricated G-MOSFET. (b),(c) Optical images of fabricated devices. (d) High-contrast optical image to show graphene flakes on the gate oxide.
initial hole density $p_0$ of $1.2 \times 10^{13}$ cm$^{-2}$ at zero gate bias. This $p_0$ is at the higher end of reported values for CVD-grown graphene transferred onto SiO$_2$ surface, likely due to the transfer process.

The transconductance $g_m$ is extracted as the slope of the transfer curve and shown in Fig. 5.2b. For better comparison with the literature, the $g_m$ is normalized to the device geometry such as the channel length and width $L/W$, and the drain-to-source voltage $V_{DS}$ [118–121]. The $g_m$, $\frac{g_m L}{W |V_{DS}|}$, and $\frac{g_m L}{W |V_{DS}|}$ have peak values of 10.5 S/m, 105 $\mu$S/V, and 29.4 $\mu$S/V, respectively, which are on the average of CVD-grown graphene transferred onto SiO$_2$ back gate. The field-effect carrier mobility is calculated based on the quadratic model of MOSFET:

$$\mu_{FE} = \frac{L \cdot g_m}{W \cdot C_{ox} \cdot V_{DS}}.$$  (5.1)

The peak value of $\mu_{FE}$ is about 767 cm$^2$/V-s, again a fair value for CVD-grown graphene. The corresponding cutoff frequency of this G-MOSFET is given by

$$f_T = \frac{g_m}{2\pi C_{ox} L W} = 1.6 \text{ GHz.}$$  (5.2)

Finally, we extract the data from TLM measurement of the graphene stripes with various $L/W$ ratios on SiO$_2$. The total resistance between two Cr/Au contacts normalized to the contact
The width ($R_{\text{tot}} \cdot W$) is plotted as a function of the length of graphene stripe ($L$). The collective result is shown in Fig. 5.3a, where the box plot is also shown next to each group of data points for statistical analysis. The box indicates the median quartile of experimental data (25–75%); the middle bar is the mean value and the square is the median value. Since the graphene tends to be shattered after transfer, the $R_{\text{tot}}$ of TLM measurement is expected to be superlinear (bent upwards) as $L$ increases. This trend is observed in Fig. 5.3a. Therefore in order to extract graphene’s innate sheet resistance without being affected by the structural defects, the minimum values for small $L$ groups should be used. The linear fitting of such minimum values are shown in Fig. 5.3b, from which a $R_{\text{sh}}$ of 3.02 kΩ/□, a contact resistivity $\rho_c$ of $1.5 \times 10^{-6}$ Ω-cm², a width-normalized contact resistance $R_c \cdot W$ of 673.2 Ω-µm, and a penetration depth $\lambda$ of 0.22 µm.
5.2 GJFETs on silicon

In this section we will explore a graphene-semiconductor heterojunction as a transistor—a GJFET. Graphene is used as the channel in which current flows laterally to utilize graphene’s high carrier mobility, whereas semiconductor is the gate within which the depletion region contains space charge that modulates graphene’s conductivity.

5.2.1 Analysis

Based on the experimental results of the graphene-nSi Schottky diodes, the optimized contact geometry (SD C in Fig. 4.1) is used in our GJFETs, which has the Cr/Au-to-graphene contacts on top of the oxide. The high SBH should provide the lowest gate leakage $I_G$, since the main source of $I_G$ is the reverse-bias current of the Schottky heterojunction. The GJFETs are fabricated on a nSi substrate of $N_D=4.5\times10^{15}$ cm$^{-3}$ with device a structure shown in Fig. 5.4a–c. The fabricated GJFETs have an oxide layer that helps visualize graphene during fabrication and separate the metal pads from the nSi substrate. The fabrication process of G-JFETs is the same as that of the graphene/nSi Schottky diodes. The GJFETs have a parasitic resistance in series with the graphene channel due to the minimum alignment distance ($a$ in Fig. 5.4a) between the metal contact and the graphene/nSi interface. This parasitic resistance ($R_s$) was assumed to be constant and was included in the analysis using the circuit shown in Fig. 5.4d. We ignore the effect of the thin tunnel oxide since it only slightly increases the $V_{Dirac}$ and as a result leads to a slightly overestimated initial hole density $p_0$ in the graphene. Also, we operated the GJFETs as a $p$-channel depletion-mode FET by applying a negative drain voltage relative to the source. The transfer characteristics were measured under a small drain-to-source bias to ensure that the devices are operated in their linear regime and to mitigate the influence of parasitic resistances.

Fig. 5.5 shows the experimental transfer characteristic and the $I_G$ of a representative GJFET. Under zero gate bias, the device was in its on state because of the initial hole doping in graphene, making it a $p$-channel depletion-mode FET. As the gate bias voltage increases, the graphene-Si
Figure 5.4: (a) Device structure of fabricated GJFET. (b), (c) Optical images of fabricated devices. (d) Circuit model for analyzing the GJFET.
heterojunction is under higher reverse bias. The expanding depletion region induces more electrons in graphene, hence neutralizing the holes therein. Due to the decreasing hole density and the low density of states around the Dirac point, graphene’s Fermi level is being shifted upwards from its valence band toward the Dirac point. This process can be observed from the decreasing amount of drain current ($I_D$), as the Fermi level closer to the Dirac point, the lower the conductivity of graphene. When the gate bias is large enough ($V_{GS} = V_{Dirac}$), the Fermi level reaches the Dirac point and there exists the minimum conductivity. The non-zero conductivity at this point arises from graphene’s zero bandgap, which is a result of room-temperature Fermi-Dirac distribution that demands an equal amount of electron and hole in the conduction and valence band, respectively. As the gate voltage keeps increasing, the Fermi level is moving upwards into the conduction band and the graphene becomes increasingly $n$-doped. The $|I_D|$ increases again.

The transistor showed a $V_{Dirac}$ of 14.1 V and an on-off current ratio of 3.8. This $V_{Dirac}$ corresponds to an initial hole density $p_0$ of $8 \times 10^{11}$ cm$^{-2}$ in graphene under flatband conditions. This hole density is less than 1/20 of that in our fabricated G-MOSFET with the same batch of graphene and the same transfer and fabrication process. The SBH at zero gate bias corresponding
to this $p_0$ value is calculated to be 0.62 eV, about 10% lower than the previous diode measurement obtained from a different device SD C. This is likely a result of graphene’s local doping variation caused by the graphene transfer process. Using the circuit model with a constant $R_s$, we obtained a simulated curve that fits the experimental data well, as shown in Fig. 5.5a. The fitting parameters, electron ($\mu_n$) and hole mobility ($\mu_p$), are 300 and 1300 cm$^2$/V·s respectively. With the carrier mobility, the transit frequency of the GJFET is calculated by

$$f_{tr} = \frac{1}{\tau_{tr}} = \frac{\mu_p V_{DS}}{L^2} = 1.44 \text{ GHz.} \quad (5.3)$$

Another fitting parameter is $R_s$, which has a sheet resistance of 16 kΩ/sq, about 2.5 times as large as that of the GJFET channel. This value is also more than 5 times the sheet resistance of graphene on oxide in previous section. This high sheet resistance is reasonable due to the coverage of graphene over the oxide step height. Our device model predicts an ideal on-off ratio as high as 12 when the $R_s$ is removed, as shown in Fig. 5.5b. Also, the GJFET showed a transconductance $g_m$ of 0.36 $\mu$S in p-channel region. When it is normalized, the $\frac{g_m}{W}$, $\frac{g_m}{|V_{DS}|}$, and $\frac{g_mL}{W|V_{DS}|}$ have values of 0.07 S/m, 3.6 $\mu$S/V, and 2.2 $\mu$S/V, respectively, lower than those of G-MOSFET. If $R_s$ is removed, the $g_m$ can be enhanced to 7.25 $\mu$S, about 20 times higher than the case being influenced by $R_s$. And the normalized $g_m$ would become comparable to the G-MOSFET. Finally, the gate leakage $I_G$ was measured to be only 1.6 (6.8)% of $I_D$ when $V_{GS}$ is biased at $V_{Dirac}$ (20 V), as shown in Fig. 5.5a. This low gate leakage means the successful operation of our GJFET.

To examine the $V_{Dirac}$ tunability, we also fabricated GJFETs on $n$-Si with various substrate doping densities using the same batch of graphene and the same fabrication process. With a lightly-doped $n$-Si of $7.4 \times 10^{14}$ cm$^{-3}$, the lowest $V_{Dirac}$ obtained was 22.1 V. Whereas with a heavily-doped $n$-Si substrate of $2 \times 10^{16}$ cm$^{-3}$, $V_{Dirac}$ was reduced to 3.8 V while concurrently keeping the largest $I_G$ less than 10% of the $I_D$. For even higher substrate doping density ($N_D > 10^{18}$ cm$^{-3}$), the graphene-$n^+$Si heterojunction becomes too leaky, losing the rectifying behavior, and thus can not maintain the normal operation of GJFET.
5.3 GJFETs on silicon carbide

To further lower the $V_{\text{Dirac}}$ by increasing substrate doping density while not being limited by the increasing gate leakage current, $n^+-4$H-SiC substrate was used for making GJFETs. 4H-SiC is chosen as the gate material because it has a smaller electron affinity and thus in principle provides a larger Schottky Barrier Height (SBH) to suppress $I_G$. The same APCVD graphene, same fabrication process, same device structure, and the same circuit model as shown in Fig. 5.4 were used to fabricate GJFETs on both Si- (0001) and C- (000\textbar 1) face of the 4H-SiC.

5.3.1 Analysis

Fig. 5.6 shows the leakage current suppression in the graphene-to-$n^+$4H-SiC Schottky diode. The Cr/Au metal contact does not form good Schottky juctions with $n^+$-4H-SiC as the substrate is heavily doped of $5.0\times10^{18}$ cm$^{-3}$. This can be observed in Fig. 5.6a where the Cr/Au-to-$n^+$-4H-SiC diodes showed low rectification ratio at ±3 V, close to that of Cr/Au-$n$Si Schottky diode on an $n$Si of $4.5\times10^{15}$ cm$^{-3}$. However the graphene-$n^+$-4H-SiC SDs showed outstanding retification, with a reverse leakage current about an order of magnitude smaller that that on $n$Si at the same

![Graph showing J-V characteristics of Schottky diodes](image1)  
(a) SD A and C on both faces of $n^+$-4H-SiC

![Graph showing Exp. data of 12 diodes](image2)  
(b) Collection of SD C on $n$-Si

Figure 5.6: $J$-$V$ characteristics of Schottky diodes (a) on both faces of $n^+$-4H-SiC and (b) on $n$-Si (repeated from Fig. 4.3c for comparison).
reverse-bias voltage, despite a substrate doping density more than three orders of magnitude higher.

![Graphs showing transfer characteristics of GJFETs on Si-face and C-face](image)

Figure 5.7: Measured transfer characteristics and $I_G$ of GJFETs on (a) Si-face and (b) C-face of 4H-SiC. Both graphs are on the same scale for comparison. The corresponding output curves on (c) Si-face and (d) C-face.

The measured transfer characteristics and $I_G$ of the GJFETs on both faces of an $n^+$-4H-SiC wafer doped of $5.0 \times 10^{18}$ cm$^{-3}$ are shown in Fig. 5.7a and b, and the corresponding output curves are shown in Fig. 5.7c and d, respectively. The $V_{Dirac}$ of the GJFET on Si-face is further reduced to as low as 1.5 V while maintaining an $I_G$ less than 0.1% of the $I_D$ at all times. This $I_G$ is on the same order of magnitude as the the GJFETs on $n$Si doped of $4.5 \times 10^{15}$ cm$^{-3}$, even the substrate
doping is more than three orders of magnitude higher. The transconductance $g_m$ of 1.41 $\mu$S is obtained, with corresponding normalized $\frac{g_m}{W}$ = 0.14 S/m, $\frac{g_m}{|V_{DS}|}$ = 14.1 $\mu$S/V, and $\frac{g_m \cdot L}{W \cdot |V_{DS}|}$ = 4.23 $\mu$S/V.

For the GJFET on C-face, the $I_D$ is smaller while $I_G$ a bit larger due to a longer channel length and a larger device area. The peak $g_m$ on C-face is 0.64 $\mu$S, corresponding to a normalized $\frac{g_m \cdot L}{W \cdot |V_{DS}|}$ of 6.4 $\mu$S/V, similar to that of the GJFET on Si-face but lower than a G-MOSFET, likely due to the parasitic series resistance.

Overall the $I_G$ reduction worked as expected due to the higher SBH on 4H-SiC, and distinct current modulation was found for GJFETs on both faces. The output curves of GJFETs on both faces of 4H-SiC showed saturation (sub-linear) behavior at zero gate bias. For the one on Si-face, the $I_D$ began to increase super-linearly at high $V_{GS}$ due to the charge inversion from $p$ to $n$-type in graphene channel.

5.4 Summary

![Figure 5.8: Marks: Experimentally obtained $V_{Dirac}$ of the GJFETs on wafers of various $N_D$. Solid (dash) line: simulated $V_{Dirac}$ of GJFET on $n$-Si (4H-SiC) as a function of $N_D$ with different $p_0$.](image)

Finally, the measured $V_{Dirac}$ values for all fabricated GJFETs are summarized in Fig. 5.8, together with the simulated $V_{Dirac}$ as a function of substrate doping density $N_D$ for various initial
hole densities \( p_0 \) in graphene. In Fig. 5.8, the solid (dash) lines represent the calculated \( V_{\text{Dirac}} \) for GJFETs on \( n \)-Si (\( n \)-4H-SiC). We found a narrow \( p_0 \) distribution in the range of \( 0.5-1 \times 10^{12} \, \text{cm}^{-2} \) of graphene devices fabricated on Si, where the difference likely comes from the process variation occurred during the graphene transfer. On the other hand, the graphene on 4H-SiC showed a magnitude higher \( p_0 \) of \( 1.2-1.4 \times 10^{13} \, \text{cm}^{-2} \), which is likely a result of process variation combined with surface polarization [63,64]. The trend of decreasing \( V_{\text{Dirac}} \) with increasing \( N_D \) well matches our prediction. Our experimental data shown in Fig. 4 confirms the \( V_{\text{Dirac}} \) tunability of GJFETs by varying \( N_D \). Our results also suggest the use of a gate material that forms high SBH with graphene, such as the 4H-SiC demonstrated, when high substrate doping is employed to reduce \( V_{\text{Dirac}} \). If graphene is clean enough with low initial hole density, the channel can even become \( n \)-type at zero gate bias. In this way, both \( p \) and \( n \)-type graphene FETs can be isolated and coexist on the same substrate by doping specific regions underneath the graphene channel during device fabrication.

In summary, the reduction of \( V_{\text{Dirac}} \) with high \( N_D \) is contributed to two factors. First, \( p_0 \) in the graphene channel is partially neutralized by the complementary charge induced by the space charge within the semiconductor at zero gate bias. This eliminates a significant portion of \( p_0 \), leaving only a part of it to be turned off by applying a gate bias, thus reducing \( V_{\text{Dirac}} \). This effect is unique to GJFET and very different from a G-MOSFET. Second, higher \( N_D \) causes a faster increase of space charge density with the gate bias, and hence the GJFET reaches \( V_{\text{Dirac}} \) at a smaller gate voltage. The unique gate mechanism of the GJFET provides an additional degree of freedom to tune the \( V_{\text{Dirac}} \) as well as the conductivity of graphene at zero gate bias by varying \( N_D \).
Chapter 6

Summary

This thesis explores the extraordinary properties of graphene for photonic and electronic applications. This thesis presents two exploratory devices based on a graphene-semiconductor heterojunction, namely a graphene-silicon infrared photodiode and a graphene junction field-effect transistor.

Graphene-silicon infrared photodiode (PD) utilizes graphenes wide optical absorption spectrum including the infrared region to which silicon is transparent. The heterojunction PD of interest, as opposed to the widely studied graphene photoconductor scheme, has a large Schottky barrier height and thus results in a low dark current. Under 1.3 and 1.55m illumination, the fabricated heterojunction PD exhibits high sensitivity comparable to commercial discrete germanium PDs for fiber-optic communications. Such heterojunction PD provides a low-cost, CMOS-compatible solution to realize high-bandwidth Si photonic interconnect.

Graphene junction field-effect transistor (GJFET) is a switching device gated by a graphene-semiconductor heterojunction. Graphene is used as the channel in which current flows laterally to utilize its high carrier mobility. Semiconductor is used as the gate within which the depletion region contains space charge that modulates graphenes conductivity. Since the space charge directly links to the doping density of semiconductor, varying gate doping controls the Dirac voltage of a GJFET. Such tunability of Dirac voltage is desirable for circuit implementation. We demonstrate the tunability by fabricating GJFETs on both Si and 4H-SiC substrates with various doping densities. This FET architecture is applicable to other 2D materials and substrates, and thus has potential
applications in high-speed electronics.

The extension beyond the scope of this thesis includes, but not limited to, a silicon waveguide-integrated graphene-Si heterojunction PD operated in a Si photonic circuit and a complementary inverter based on both $p$- and $n$- types of epitaxial GJFETs on the same SiC substrate. These applications are unattainable with state-of-the-art technology and would have an immediate impact in the related fields, such as Si photonics and high-speed graphene-based circuits.
Chapter 7

Conclusion

In this thesis, we combine graphene with conventional semiconductor to form functional devices. The optimized contact geometry was determined to yield a good rectifying heterojunction with high Schottky barrier height (SBH).

A photodiode is formed by laying graphene on $n$-type silicon surface. The low dark current as a result of the high SBH ($\sim0.7$ eV) makes the photodiode exhibit low dark current (on the order of 10 pA), low noise (NEP on the order of pW/Hz$^{0.5}$), and decent detectivity ($D^*$ on the order of $10^9$ cm-Hz$^{0.5}$/W) at 1.3$\mu$m telecommunication wavelength at room temperature.

Graphene-semiconductor heterojunction can also be used as a gate to control graphene’s conductivity. We successfully demonstrate graphene junction field-effect transistors (GJFETs) on $n$Si and $n^+$-4H-SiC. Even with large parasitic resistance, the GJFETs still exhibit a distinct current modulation in transfer characteristic. Hole and electron mobility on Si surface are found to be 1300 and 300 cm$^2$/V-s, respectively, by curve fitting. In addition, the GJFET structure can be used to identify the initial hole density $p_0$ of graphene on a bare semiconductor surface with simple electrical measurement. A tight distribution of $p_0$ of $0.5-1\times10^{12}$ cm$^{-2}$ is found on Si, and a $p_0$ of about $1\times10^{13}$ cm$^{-2}$ is found on both faces of 4H-SiC. Lastly, the tunability of the $V_{Dirac}$ of individual graphene transistor enabled by varying the doping density of the semiconductor in the heterojunction back gate is confirmed. The $V_{Dirac}$ as low as 3.8 and 1.5 V are obtained on $n$Si and $n^+$-4H-SiC doped of $2\times10^{16}$ and $5\times10^{18}$ cm$^{-3}$, respectively.
Bibliography


