

EFFICIENCY OPTIMIZATION IN DIGITALLY
CONTROLLED FLYBACK DC-DC CONVERTERS OVER
WIDE RANGES OF OPERATING CONDITIONS

by

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Efficiency Optimization in Digitally Controlled Flyback DC-DC Converters Over Wide Ranges of Operating Conditions

Thesis directed by Prof. Dragan Maksimović

Because of increasingly demanding energy programs and initiatives, it is required to maintain high efficiency in various DC-DC converter applications over wide ranges of operating conditions. To achieve these efficiency goals, this thesis introduces an efficiency optimization approach, which can be applied to given power stages. In the proposed optimization approach, power stage design parameters and controller parameters are concurrently optimized over a range of operating conditions based on power loss models and multi-variable non-linear constrained optimization. A digital controller facilitates on-line efficiency optimization by storing the optimum controller parameters in a look-up table. A flyback DC-DC converter, commonly used in low output power applications, is adopted for experimental verifications of the proposed optimization approach. A valley switching technique is employed to significantly decrease MOSFET turn-on switching loss in discontinuous conduction mode (DCM), and solutions to a problem related to undesirable frequency hopping, commonly observed in other valley switching schemes, are proposed and discussed. A gain-scheduled compensator and a new control scheme, named k -control, are implemented for consistent transient responses over different operating conditions. Finally, simplified sensing and analog-to-digital (A/D) conversion techniques are proposed, targeting a low-cost, small-size and low-pin-count (≤ 8) digital controller IC chip implementation.

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Chapter 1

Introduction

Modern DC-DC or AC-DC power converter applications are required to operate over wide ranges of operating conditions. For example, electronic devices such as personal computers, monitors and printers stay in the “sleep-mode” when the devices are not in use for a while. In the sleep-mode, power supplies operate at light loads. On the other hand, the supplies operate at full loads when the appliances are ordinarily in use.

Due to increasing environmental and energy saving concerns, energy programs and initiatives have established related energy standards which demand the converters to maintain high efficiency over wide ranges of operating conditions (e.g. input voltage and load current) [1] – [4]. Table 1.1 shows energy standards provided by 80 plus for 115V internal power supplies (desktop, workstation and non-redundant server applications) and 230V internal power supplies (redundant, data center applications), presenting efficiency requirements over different load conditions. The energy standards require efficiency that is more than 80% over all load conditions and more than 90%, especially for Platinum and Titanium levels.

To meet these efficiency goals in the area of DC-DC converters, “green-mode” analog controllers featuring multi-mode operation have been introduced [5] – [7]. However, such approaches are often tied to specific power converter topologies or assume certain power stage parameters. In the area of digital DC-DC control, approaches have been proposed to achieve on-

Table 1.1. 80 plus energy standards for 115V and 230V internal power supplies

	115V internal supply			230V internal supply		
Load (%)	20	50	100	20	50	100
Bronze	82%	85%	82%	81%	85%	81%
Silver	85%	88%	85%	85%	89%	85%
Gold	87%	90%	87%	88%	92%	88%
Platinum	90%	92%	89%	90%	94%	91%
Titanium	–	–	–	94%	96%	91%

line efficiency optimization, e.g. by adjusting dead-times [8] – [10], by multi-mode operation [9, 11], by adjusting the supply voltage for compensation of the propagation delay variations due to the variations of intrinsic parameter and operating condition [12], or by real-time prediction of the load current [13]. Such on-line optimization techniques are attractive but require more complex controllers, and may not perform well in the presence of dynamically changing operating conditions.

This thesis proposes and discusses a new approach to achieving efficiency optimization over wide ranges of operating conditions, which can be relatively simply applied to any given power stage. This approach maximizes efficiency of a given power stage over wide ranges of operating conditions by optimization of power stage design parameters – for example, inductors, MOSFETs and transformers – and by controller adaptations such as (1) switching timing such as near ZVS turn-on in discontinuous conduction mode (DCM) and optimum dead times in bridge or synchronous rectifier converters, (2) switching frequency for best conduction loss versus switching loss tradeoff, and (3) operating modes – continuous conduction mode (CCM), DCM or burst mode.

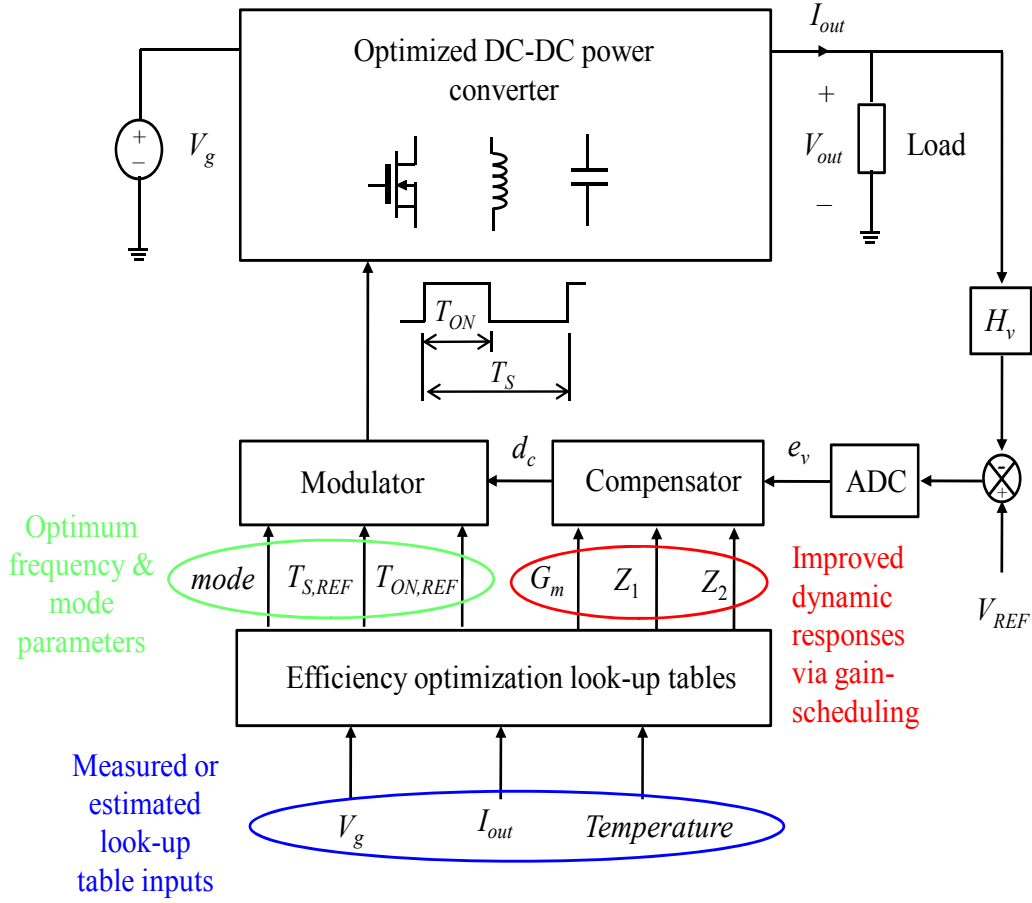


Fig. 1.1. Efficiency optimization approach by addressing simultaneously power-stage-design and controller parameters, and by using a look-up table based digital controller.

Fig. 1.1 presents a block diagram of the proposed efficiency optimization approach. A number of switch-mode power supply design optimization approaches have been described in the literature [14] – [19]. Similar to [16], the approach adopted in the thesis is based on three main ideas: (1) a relatively simple, but sufficiently detailed loss model capable of representing the main loss mechanisms over wide ranges of operating points; (2) an objective function that allows minimization of the power loss weighted over ranges of operating points (multi-variable non-

linear constrained optimization), under a cost constraint, and (3) combined design time optimization (power stage) and controller optimization, taking advantages of a digital controller capability to set the controller adaptations for any given operating point.

The optimum controller parameters are programmed in a look-up table of the digital controller based on the optimization results, as shown in Fig. 1.1, which presents a simpler and more general approach compared to other on-line efficiency optimization approaches. The digital controller senses the operating points such that the look-up table updates the optimum controller parameters to a modulator to achieve on-line efficiency optimization. Furthermore, the look-up table stores compensator parameters (e.g., compensator gain G_m , zeros Z_1 and Z_2) to employ gain scheduling for the purpose of achieving the target crossover frequency (f_c) with adequate phase margin (φ_m) over wide ranges of operating conditions.

Chapter 2 introduces a conventional flyback DC-DC converter which is adopted and tested to experimentally verify advantages of the proposed on-line efficiency optimization approach.

Chapter 3 describes the power loss models used for concurrent power stage and controller optimizations in conventional flyback DC-DC converters.

Chapter 4 presents details of the procedures to optimize power stage design parameters and controller parameters, using the power loss models and objective function that allows minimization of the overall power losses.

Chapter 5 addresses relatively simple look-up table based digital controller implementation to accomplish on-line efficiency optimization over wide ranges of operating conditions, together with several issues usually observed in multi-mode operations and control approaches to improving large-signal dynamic operation.

Chapter 6 proposes simplified sensing and analog-to-digital (A/D) conversion techniques to implement a low-cost, small-size and low-pin-count (≤ 8) digital controller IC chip.

Conclusions are presented in Chapter 7, which includes a summary of the contributions and a discussion of opportunities for future work.

Chapter 2

Flyback DC-DC Converters

This chapter introduces a conventional flyback DC-DC converter, which is adopted as an example to experimentally verify advantages of the proposed efficiency optimization approach. The flyback DC-DC converter is commonly used for low output power applications, typically from few watts to 100W because of its simplicity, low cost and isolation between the input and the output. For example, the flyback DC-DC converter can be employed as a second stage in AC-DC rectifier systems, as shown in Fig. 2.1. A modern AC-DC rectifier is usually designed based on a CCM boost converter to achieve high power factor (PF), very close to one, such that AC current harmonics are low and AC distribution losses can be minimized. However, the boost PFC rectifier produces a high DC voltage, greater than the peak ac line voltage. So the flyback DC-DC converter converts down the rectified DC voltage and performs point-of-load regulation to supply low DC voltage, as needed.

This chapter is organized as follows. Sections 2.1 and 2.2 present how the flyback converter operates in CCM and DCM, which are determined by continuity of magnetizing current flow over a switching period, respectively. In Section 2.3 resonance characteristics of the converter are described, resulting in significant contributions to overall power losses. This chapter is summarized and concluded in Section 2.4.

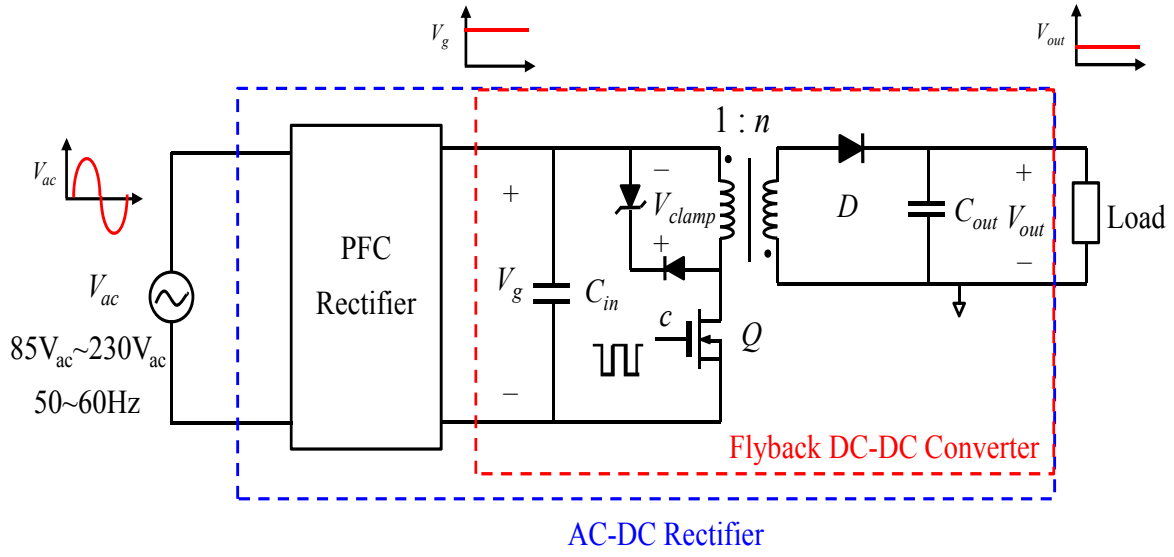


Fig. 2.1. Flyback DC-DC converter in an AC-DC rectifier system.

2.1 Continuous Conduction Mode (CCM)

Fig. 2.2 shows a flyback DC-DC converter with a transformer equivalent circuit in which the magnetizing inductance (L_M) is connected in parallel with the primary winding. Signal c shown in Fig. 2.2 is the control signal for switching operation of the power MOSFET Q . The switch Q conducts when the control signal is high ($0 < t < dT_s$, subinterval 1), while the output diode D is open. The converter circuit model during the subinterval 1 is presented as Fig. 2.3 (a). Then, with the assumption that the converter operates with small inductor current ripple and small capacitor voltage ripple, the output voltage and inductor current are approximated by their DC components, and then the inductor voltage v_L and capacitor current i_C are given by

$$v_L = V_g \quad (2.1)$$

$$i_C = -\frac{V_{out}}{R} \quad (2.2)$$

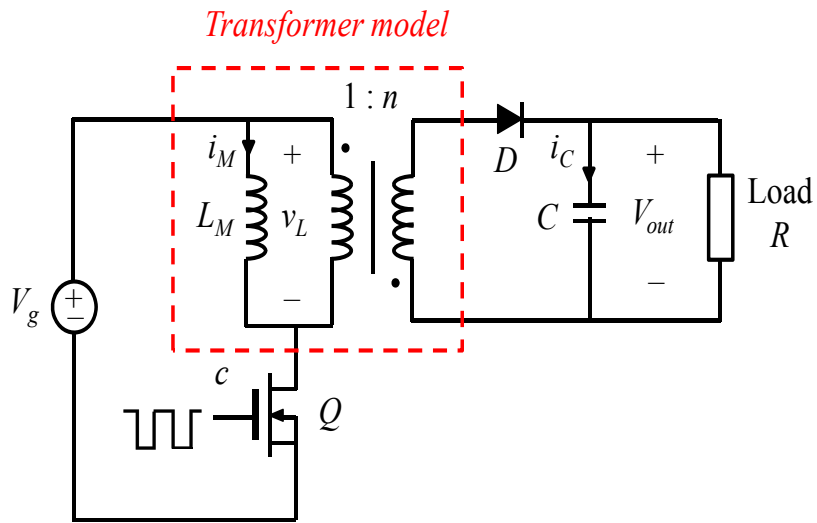
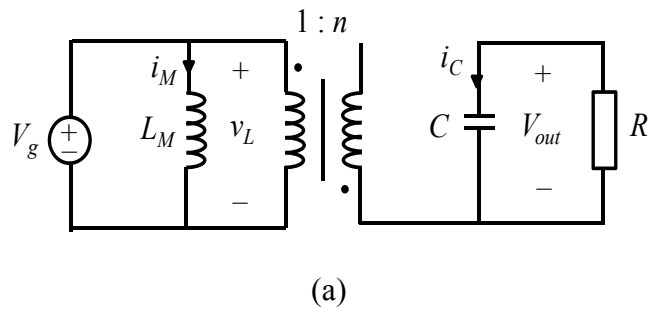
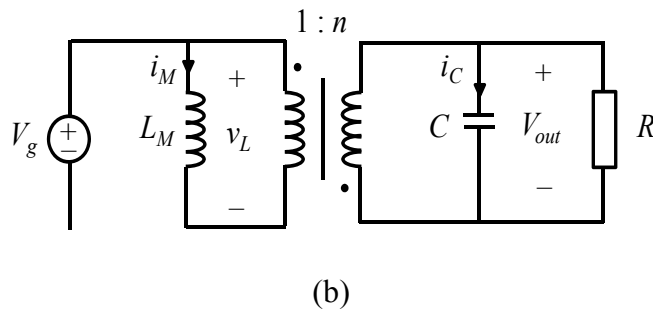


Fig. 2.2. Flyback DC-DC converter with transformer equivalent circuit.



(a)



(b)

Fig. 2.3. Flyback converter circuit: (a) during subinterval 1 and (b) during subinterval 2.

During subinterval 2 ($dT_S < t < (1-d)T_S$), the control signal is low such that the switch Q is off, and the diode D conducts. The circuit model in this interval is shown in Fig. 2.3 (b). Under the same assumptions as in the first subinterval, the inductor voltage and capacitor current are:

$$v_L = -\frac{V_{out}}{n} \quad (2.3)$$

$$i_C = \frac{I_M}{n} - \frac{V_{out}}{R} \quad (2.4)$$

The principles of volt-second balance and charge balance are applied to the magnetizing inductance and the output capacitor, respectively [20],

$$\langle v_L \rangle = \frac{1}{T_S} \int_0^{T_S} v_L(t) dt = d(V_g) + (1-d) \left(-\frac{V_{out}}{n} \right) = 0 \quad (2.5)$$

$$\langle i_C \rangle = \frac{1}{T_S} \int_0^{T_S} i_C(t) dt = d \left(-\frac{V_{out}}{R} \right) + (1-d) \left(\frac{I_M}{n} - \frac{V_{out}}{R} \right) = 0 \quad (2.6)$$

From (2.5) the conversion ratio M , i.e. the ratio of output voltage and input voltage, is obtained as

$$M(d) = \frac{V_{out}}{V_g} = n \frac{d}{1-d} \quad (2.7)$$

Equation (2.6) yields the DC component of the magnetizing current (I_M) as a function of duty cycle d and turns ratio n ,

$$I_M = \frac{nV_{out}}{(1-d)R} \quad (2.8)$$

The magnetizing current i_M , MOSFET current i_Q , and control signal c waveforms in CCM are shown in Fig. 2.4. The magnetizing current flows through the MOSFET Q and linearly increases during the first subinterval (Q on, D off) with the slope of V_g/L_M . On the other hand,

the magnetizing current decreases with the slope of $-V_{out}/(nL_M)$ during the second subinterval (Q off, D on) and falls to the same starting point when the switching period (T_S) ends.

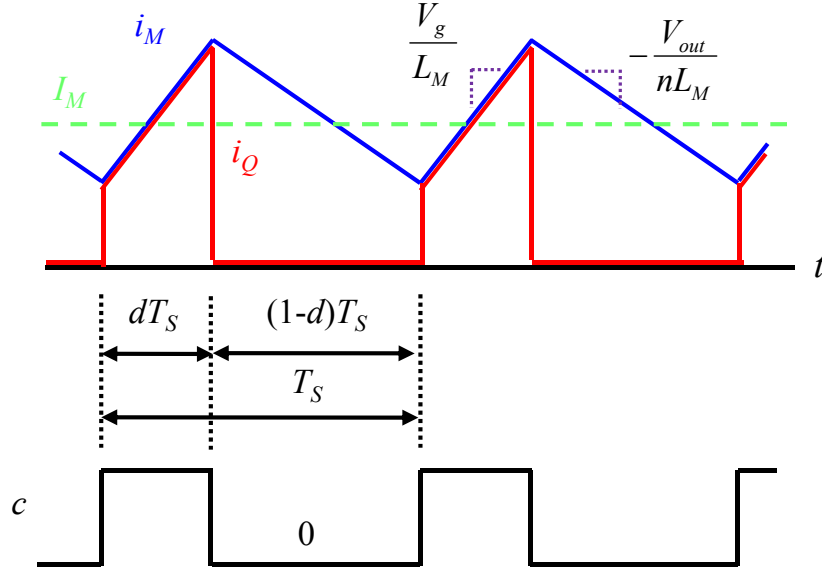


Fig. 2.4. Waveforms of magnetizing current i_M , MOSFET current i_Q and control signal c in CCM.

2.2 Discontinuous Conduction Mode (DCM)

In DCM, which occurs at lower loads, the magnetizing current falls down to zero before the next switching cycle starts, as shown in Fig. 2.5. This discontinuity of the magnetizing current results in significantly different operating characteristics, including a load-dependent conversion ratio M , and a different expression for the DC component of the magnetizing current I_M , as well as different large-signal and small-signal dynamic models.

The converter circuits during the first and second subintervals are the same as those in CCM and the magnetizing current reaches to zero at the end of the second subinterval. Fig. 2.6

shows the converter circuit during the third subinterval (d_3T_S) – the MOSFET Q and the output diode D are both off, and magnetizing current is zero.

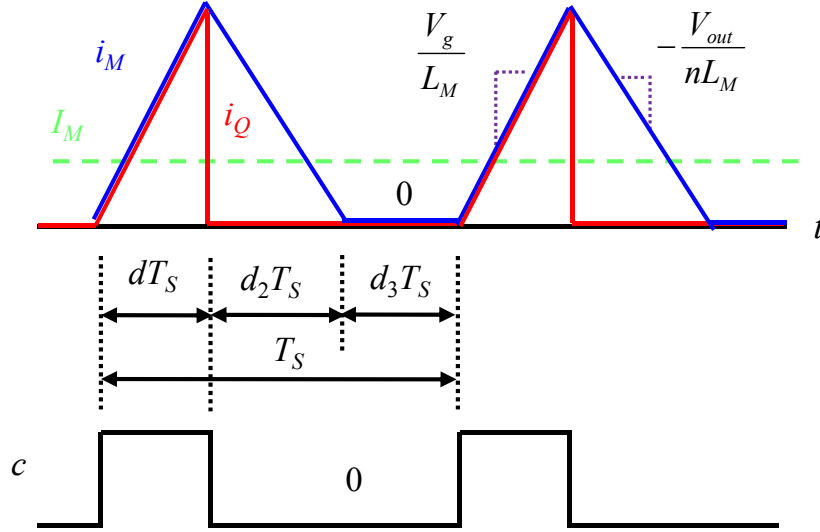


Fig. 2.5. Waveforms of magnetizing current i_M , MOSFET current i_Q and control signal c in DCM.

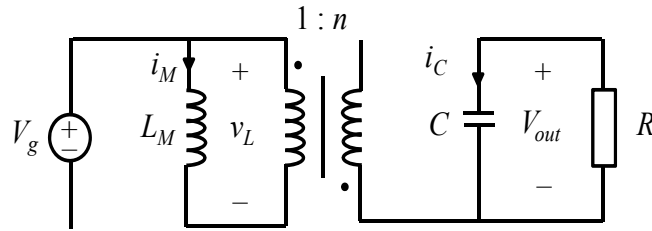


Fig. 2.6. Flyback circuit during subinterval 3 in DCM.

The procedure to calculate the input-to-output conversion ratio M and duty cycle D in DCM is more complicated. With an assumption that the flyback power stage is lossless, the averaged switch model of the DCM switch network is usually used to obtain the conversion ratio

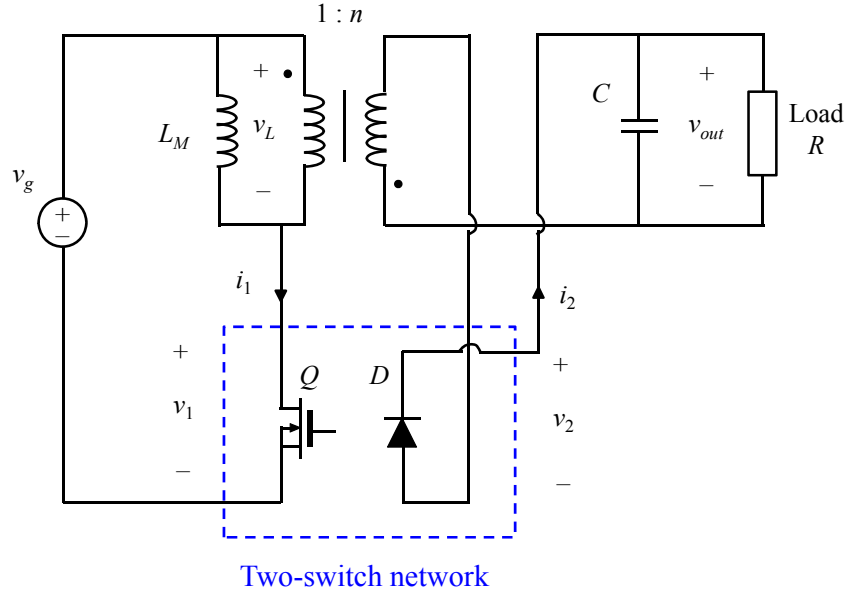


Fig. 2.7. Averaged switch network of flyback converter with switch network terminals identified.

and duty cycle, as presented in [20]. Fig. 2.7 shows the flyback converter with switch network terminals identified.

A DCM averaged switch network can be found by analysis of the waveforms presented in Fig. 2.8. By averaging the v_1 waveform, the average switch network input voltage $\langle v_1 \rangle_{T_s}$ is given by

$$\langle v_1 \rangle_{T_s} = d_2 \left(\langle v_g \rangle_{T_s} + \frac{\langle v_{out} \rangle_{T_s}}{n} \right) + d_3 \langle v_g \rangle_{T_s} \quad (2.9)$$

By inserting $d_3 = 1 - d - d_2$ to (2.9), $\langle v_1 \rangle_{T_s}$ is expressed as

$$\langle v_1 \rangle_{T_s} = (1 - d) \langle v_g \rangle_{T_s} + d_2 \frac{\langle v_{out} \rangle_{T_s}}{n} \quad (2.10)$$

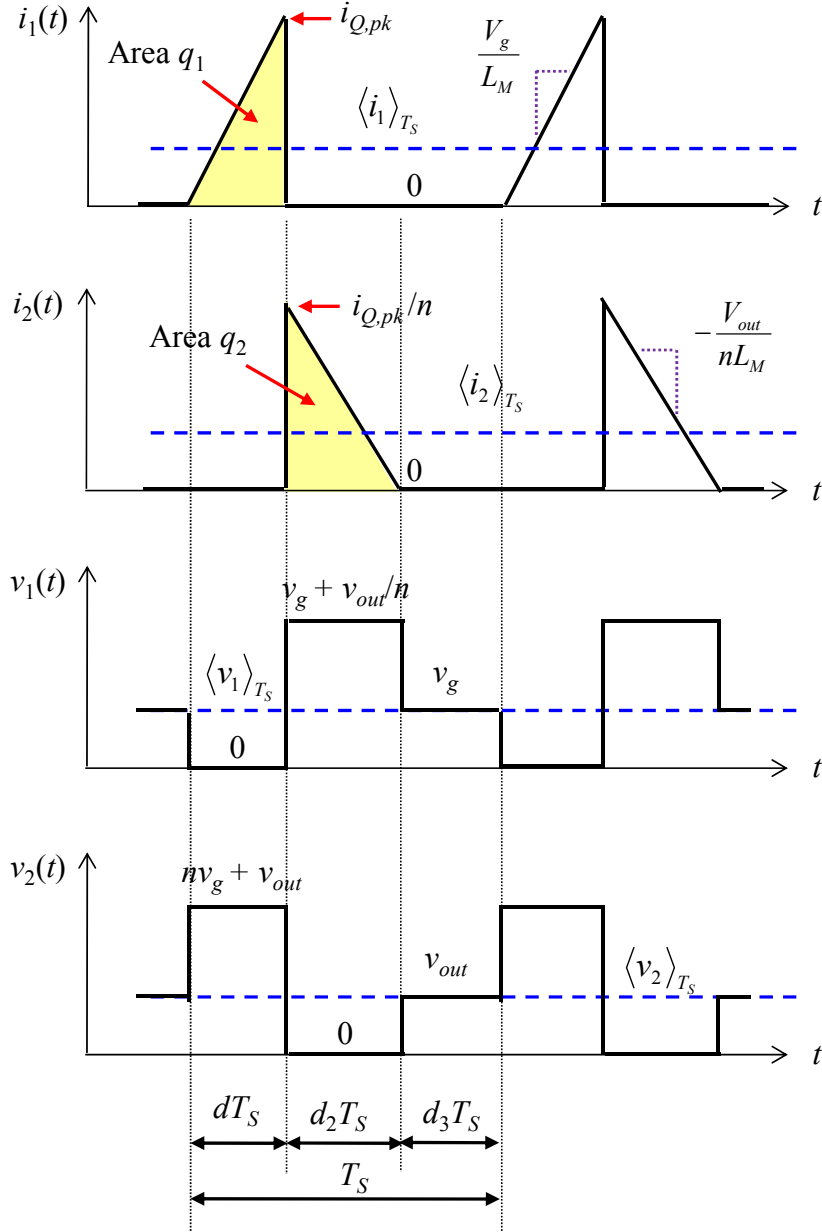


Fig. 2.8. Switch network voltage and current waveforms in DCM.

Similar analysis yields the following expression for the average switch network output voltage (average diode voltage).

$$\langle v_2 \rangle_{T_s} = nd \langle v_g \rangle_{T_s} + (1 - d_2) \langle v_{out} \rangle_{T_s} \quad (2.11)$$

The average MOSFET current $\langle i_1 \rangle_{T_s}$ is obtained by the i_1 waveform in Fig. 2.8.

$$\langle i_1 \rangle_{T_s} = \frac{1}{T_s} \int_0^{T_s} i_1(t) dt = \frac{q_1}{T_s} \quad (2.12)$$

The integral q_1 is the area under the i_1 waveform during the first subinterval, which can be expressed as

$$q_1 = \int_0^{T_s} i_1(t) dt = \frac{1}{2} (dT_s) (i_{Q,pk}) \quad (2.13)$$

where $i_{Q,pk}$ is the peak MOSFET current. From Fig. 2.8,

$$i_{Q,pk} = \frac{v_g}{L_M} dT_s \quad (2.14)$$

By substituting (2.14) and (2.13) into (2.12),

$$\langle i_1 \rangle_{T_s} = \frac{d^2 T_s}{2L_M} \langle v_g \rangle_{T_s} \quad (2.15)$$

Similar analysis corresponding to the average diode current $\langle i_2 \rangle_{T_s}$ and the integral q_2 results in

$$\langle i_2 \rangle_{T_s} = \frac{dd_2 T_s}{2nL_M} \langle v_g \rangle_{T_s} \quad (2.16)$$

To express the average switch terminal quantities as a function of d , d_2 can be eliminated by using the fact that the average inductor voltage computed over one switching period is zero. Therefore,

$$\langle v_{L_M} \rangle_{T_s} = d \langle v_g \rangle_{T_s} - d_2 \frac{\langle v_{out} \rangle_{T_s}}{n} + d_3 \cdot 0 = 0 \quad (2.17)$$

$$d_2 = nd \frac{\langle v_g \rangle_{T_s}}{\langle v_{out} \rangle_{T_s}} \quad (2.18)$$

Simple expressions for the averaged switch network quantities in the discontinuous conduction mode can be found by substituting (2.18) into (2.10), (2.11), (2.15) and (2.16).

$$\langle v_1 \rangle_{T_s} = \langle v_g \rangle_{T_s} \quad (2.19)$$

$$\langle v_2 \rangle_{T_s} = \langle v_{out} \rangle_{T_s} \quad (2.20)$$

$$\langle i_1 \rangle_{T_s} = \frac{d^2 T_s}{2L_M} \langle v_1 \rangle_{T_s} \quad (2.21)$$

$$\langle i_2 \rangle_{T_s} = \frac{d^2 T_s}{2L_M} \frac{\langle v_1 \rangle_{T_s}^2}{\langle v_2 \rangle_{T_s}} \quad (2.22)$$

From (2.21), it can be observed that the average input current $\langle i_1 \rangle_{T_s}$ is proportional to the applied input voltage $\langle v_1 \rangle_{T_s}$, which means that the low-frequency components of the input port obey Ohm's law. Therefore, by defining the effective resistance R_e as

$$R_e(d) = \frac{2L_M}{d^2 T_s} \quad (2.23)$$

the switch network input port is modeled as

$$\langle i_1 \rangle_{T_s} = \frac{\langle v_1 \rangle_{T_s}}{R_e(d)} \quad (2.24)$$

Then, the switch network output port is constructed from (2.22) and (2.23) as

$$\langle i_2 \rangle_{T_s} \langle v_2 \rangle_{T_s} = \frac{d^2 T_s}{2L_M} \langle v_1 \rangle_{T_s}^2 = \frac{\langle v_1 \rangle_{T_s}^2}{R_e(d)} = \langle p \rangle_{T_s} \quad (2.25)$$

Equations (2.24) and (2.25) show that the switch network input port behaves as the effective resistance R_e , and the power consumed by R_e is transferred to the switch network output port which acts as a source of power that can be represented by the dependent power source symbol.

Therefore, the corresponding averaged switch model of the flyback DC-DC converter in discontinuous conduction mode is modeled as in Fig. 2.9.

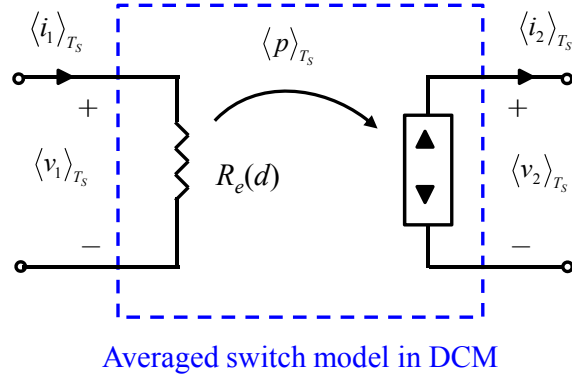


Fig. 2.9. Averaged switch model of flyback converter in DCM.

In consequence, the switch network of the DCM flyback converter can be replaced by the averaged switch model (Fig. 2.9), and the equivalent flyback converter circuit is shown in Fig. 2.10.

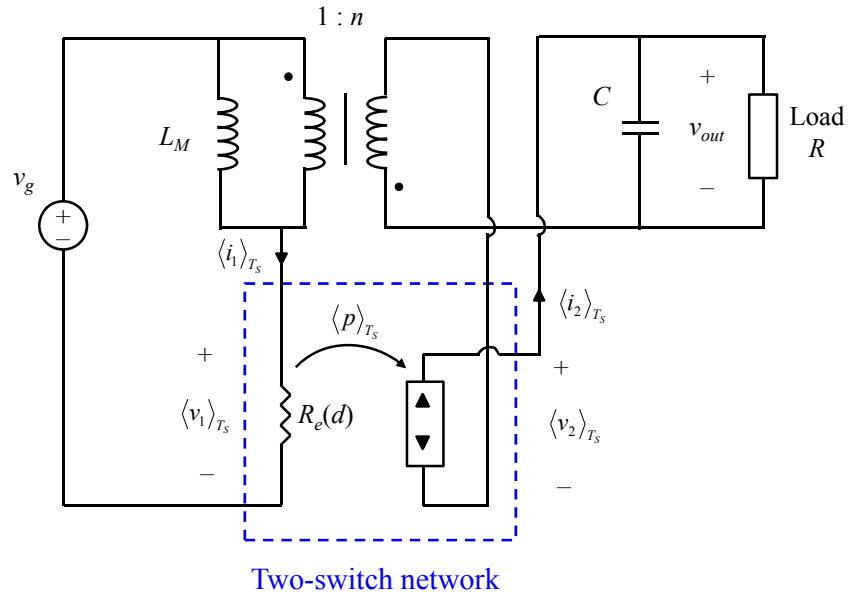


Fig. 2.10. Replacement of switch network in DCM flyback converter with the loss-free resistor model.

The equivalent circuit of the DCM flyback converter (Fig. 2.10) is usually used to obtain the conversion ratio M and duty cycle D by analyzing the DC network of the circuit. When the converter operates in steady state, the DC model of the equivalent circuit can be obtained (Fig. 2.11) by letting the inductor and the capacitor become a short-circuit and an open-circuit, respectively. Under the assumption that the flyback converter system is lossless, the input power is transferred to the output load without a loss, resulting in

$$P = \frac{V_g^2}{R_e} = \frac{V_{out}^2}{R} \quad (2.26)$$

From (2.23) and (2.26), the conversion ratio M and the duty cycle D are

$$M = \frac{V_{out}}{V_g} = \sqrt{\frac{R}{R_e}} = \sqrt{\frac{RD^2 T_S}{2L_M}} \quad (2.27)$$

$$D = \frac{\sqrt{2V_{out} I_{out} L_M F_S}}{V_g} \quad (2.28)$$

where F_S is the switching frequency ($F_S = 1/T_S$).

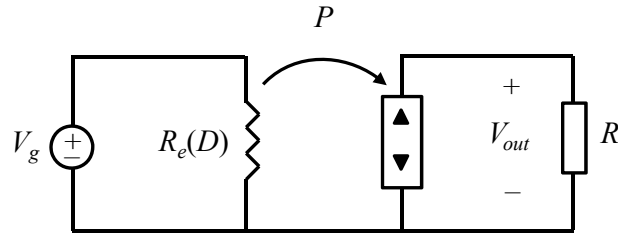


Fig. 2.11. DC model of the DCM flyback converter with loss free resistor

2.3 Resonances in the Flyback DC-DC Converter

In flyback DC-DC converters there are two kinds of resonances, which may result in significant switching losses: (1) a resonance between the magnetizing inductance L_M and the switching-node capacitance C_{sw} during the third subinterval in DCM, and (2) a resonance between the leakage inductance L_{lk} and the switching-node capacitance C_{sw} during the output diode conduction interval. Fig. 2.12 shows the flyback converter including the switching-node capacitance and a more general transformer model, including leakage inductance L_{lk} . Because the leakage inductance cannot be removed in practical constructions of the flyback transformer, the inductance is added in series with the primary winding in the transformer model. The switching-node capacitance is the total capacitances connected in parallel between the switching node and

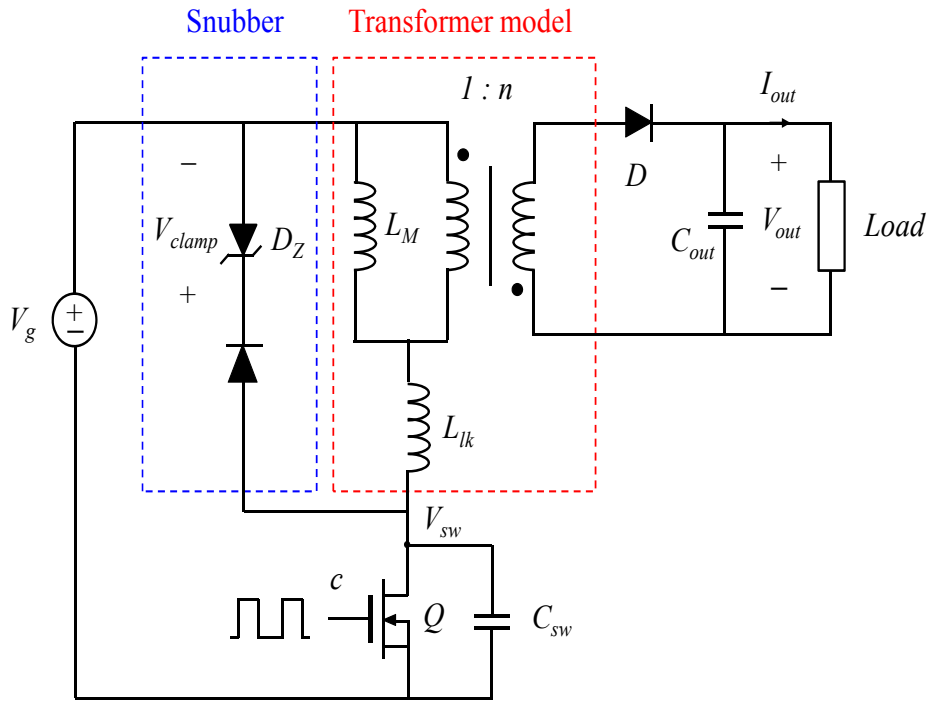


Fig. 2.12. Flyback converter including switching-node capacitance C_{sw} , leakage inductance L_{lk} , and voltage-clamp snubber diodes.

ground, which is a combination of drain-to-source capacitance of the MOSFET, transformer winding capacitance, and output capacitance of the snubber diodes.

When the converter operates in DCM, ringing due to the resonance between the magnetizing inductance L_M and the switching-node capacitance C_{sw} is observed during the subinterval 3 (Q off, D off) as shown in Fig. 2.13. A quasi-resonant (QR) control with valley switching is widely adopted in flyback DC-DC converters to decrease the switching loss due to the switching-node capacitance by taking an advantage of near zero-voltage switching [21] – [24]. The valley switching technique forces the switch to turn on at the minimum switching-node voltage V_{sw} . An example of valley switching is shown in Fig. 2.13. The switching loss mechanism with the assumption that the valley switching is employed when the flyback converter operates in DCM is described in Chapter 3.

When the switch Q is off and the output diode D starts to conduct, the leakage inductance L_{lk} and switching-node capacitance C_{sw} make resonance at the switching-node (Fig. 2.13) since energy stored in the leakage inductance is transferred to the switching-node capacitance. It results in undesirable voltage oscillation at the switching node, producing large voltage spikes which would make the MOSFET fail unless the voltage rating of the MOSFET is sufficiently large. To overcome this issue, a Zener diode snubber is usually employed to clamp the resonant voltage, but the snubber may consume a significant power, which implies a tradeoff between the power consumed by the snubber and the MOSFET voltage rating. The details of this loss mechanism and techniques to decrease the loss are presented in Chapters 3 and 4, respectively.

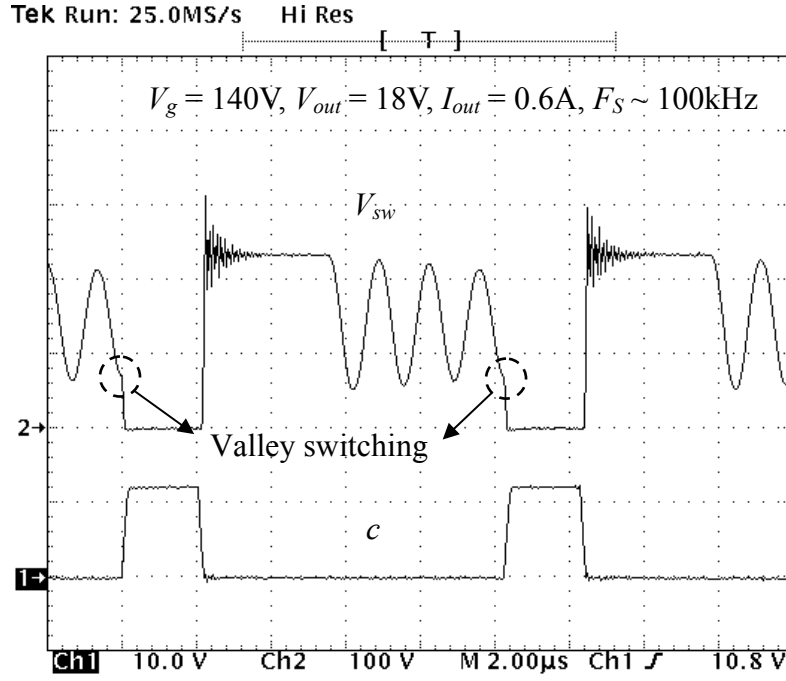


Fig. 2.13. Example of quasi-resonant (QR) control with valley switching in DCM.

2.4. Conclusions

A flyback DC-DC converter, which is employed as a test case for the proposed on-line efficiency optimization approach, is introduced in this chapter. Continuity of the magnetizing inductor current results in two operating modes, continuous conduction mode (CCM) and discontinuous conduction mode (DCM). Steady-state conversion ratios and duty cycles are derived in both CCM and DCM using the principles of inductor volt-second balance and capacitor charge balance [20]. Resonance mechanisms, which can significantly affect switching losses, are briefly described. Chapters 3 and 4 address approaches to reducing the switching losses due to the resonances.

Chapter 3

Power Loss Modeling for Efficiency Optimization

Sufficiently detailed loss models are necessary in order to perform efficiency optimization over design and controller parameters. This chapter describes power loss modeling in conventional flyback converters and presents model verification by comparisons with experimental results.

3.1 Power Loss Modeling

The approaches to loss modeling adopted in the thesis, which are based on well known or published results, are briefly summarized in this section. A constant operating temperature (60°C) is assumed in all models.

3.1.1 Conduction Losses

Conduction losses are modeled based on approximate converter waveforms from an ideal-switch converter model. The transistor Q on-resistance R_{on} , as well as the diode D , forward voltage drop V_F , series resistance R_D , as well as effective series resistances (ESRs) of input and output capacitors are taken from the component data sheets. The DC resistances of primary and secondary sides in a flyback transformer are calculated from the winding structures by using

$$R_{dc,trans} = \rho \frac{l}{A_w} \quad (3.1)$$

where ρ is the wire resistivity, l is the length of the wire used for the flyback transformer windings in primary or secondary sides, and A_w is the cross-sectional area of the wire used for the corresponding windings.

3.1.2 Switching Loss Due To Switching-Node Capacitance

At the end of each switching period, the energy stored in the non-linear switching-node capacitance is dissipated when the switch is turned on. Assuming the controller employs valley switching in DCM to have an advantage of decreased switching loss, the valley switching voltage (V_{sw}) is estimated as follows in DCM:

$$V_{sw} = V_g - \frac{V_{out} + V_F}{n} e^{-\alpha N_{cycle} T_{OSC}} \quad (3.2)$$

$$\alpha = \frac{R_r}{2L_M} \quad (3.3)$$

$$N_{cycle} = \text{round}\left(\frac{D_3 T_s}{T_{OSC}}\right) + 0.5 \quad (3.4)$$

where T_{OSC} is an oscillation period and R_r is a damping resistance. In CCM,

$$V_{sw} = V_g + \frac{V_{out} + V_F}{n} \quad (3.5)$$

The switching-node capacitance consists of a non-linear drain-to-source capacitance of the MOSFET, and a winding capacitance of the transformer. The loss is modeled as

$$P_{sw} = \frac{1}{2} C_w V_{sw}^2 F_s + E(V_{sw}) F_s \quad (3.6)$$

where C_w is the winding capacitance and $E(V_{sw})$ is the energy stored in the MOSFET drain-to-source capacitance as a function of the switching-node voltage, which is usually available from the MOSFET data sheet. The winding capacitance is calculated by measuring the ringing period.

3.1.3 Switching Loss Due To Leakage Inductance

The leakage inductance is analytically modeled from the transformer winding structure as described in [25]. The waveforms associated with the dissipative snubber in Fig. 2.12 are shown in Fig. 3.1.

When the switch Q turns off at $t = dT_s$, the output diode D conducts and the current starts to flow through the diode (i_D). At the same time, the energy stored in the leakage inductance begins to be discharged – the snubber diode conducts (D_s) and the leakage inductance current (i_{lk}) flows through the snubber until the diode current builds up as shown in Fig. 3.1. The switching loss due to the leakage inductance (P_{clamp}) is expressed as

$$P_{clamp} = \frac{1}{2} \cdot V_{clamp} \cdot i_{Q,pk} \cdot T_C \cdot F_s \quad (3.7)$$

From the analysis of the leakage inductance current waveform, the time for the diode current to build up (T_C) is found as

$$T_C = \frac{i_{Q,pk} L_{lk}}{V_{clamp} - V_{out} / n} = \frac{L_{lk}}{L_M + L_{lk}} \frac{nV_g}{nV_{clamp} - V_{out}} dT_s \quad (3.8)$$

By inserting (3.8) into (3.7), the switching loss due to the leakage inductance can be expressed as

$$P_{clamp} = \frac{1}{2} L_{lk} i_{Q,pk}^2 \frac{nV_{clamp}}{nV_{clamp} - V_{out}} F_s \quad (3.9)$$

where V_{clamp} is the snubber Zener voltage, and $I_{max,Q}$ is the peak MOSFET current.

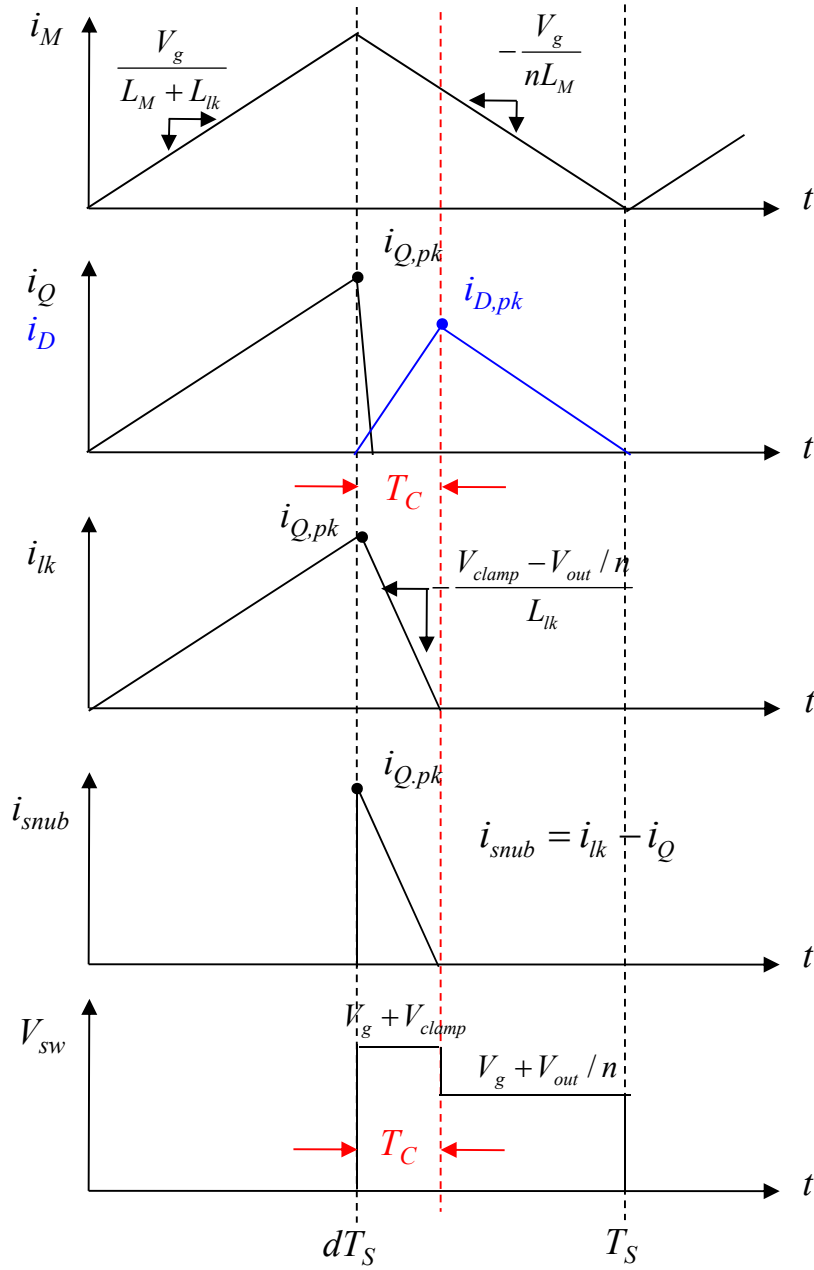


Fig. 3.1. Waveforms associated with the dissipative snubber: i_M (magnetizing current), i_Q (MOSFET current), i_D (output diode current), i_{lk} (leakage inductance current), i_{snub} (current through snubber Zener diode), and V_{sw} (switching-node voltage).

3.1.4. Transformer Proximity Loss and Core Loss

The 1-D model of the proximity loss is constructed using the approach presented in [26]. Fig. 3.2 shows examples of winding structures in non-interleaved and interleaved transformers for the loss modeling – 2 layers on the primary side and 1 layer on the secondary side, together with magnetomotive force (MMF) distributions in DCM. The MMF distribution in each transformer winding layer is found in time domain and decomposed into sinusoidal harmonics by Fourier series analysis. The power loss density is then computed for each harmonic and power loss densities over all harmonics are summed to find the proximity loss in each layer. The corresponding loss model in each layer ($P_{prox,layer}$) is as follows [26]:

$$P_{prox,layer} = \frac{R_{layer}}{2N_l^2} \sum_i \varphi_i \left[\left(|F_i(h)|^2 + |F_i(0)|^2 \right) G_1(\varphi_i) - 4|F_i(h)||F_i(0)|\cos(\Delta\theta_i)G_2(\varphi_i) \right] \quad (3.10)$$

$$G_1(\varphi_i) = \frac{\sinh(2\varphi_i) + \sin(2\varphi_i)}{\cosh(2\varphi_i) - \cos(2\varphi_i)} \quad (3.11)$$

$$G_2(\varphi_i) = \frac{\sinh(2\varphi_i)\cos(2\varphi_i) + \cosh(2\varphi_i)\sin(2\varphi_i)}{\cosh(2\varphi_i) - \cos(2\varphi_i)} \quad (3.12)$$

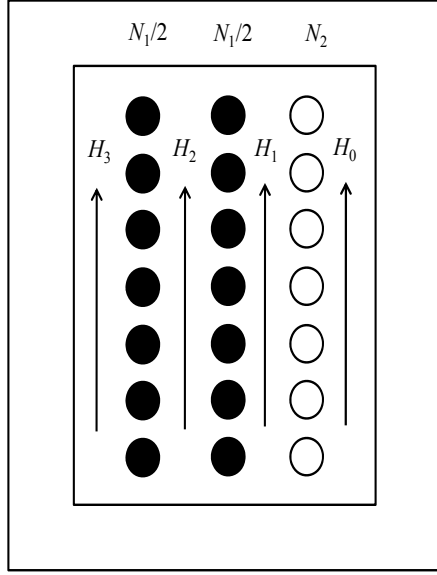
$$\Delta\theta_i = \theta_i(0) - \theta_i(h) \quad (3.13)$$

$$\varphi_i = \left(\frac{\pi}{4} \right)^{0.75} \sqrt{\frac{N_l}{l_w}} \left(\frac{d^{1.5}}{\delta_i} \right) \quad (3.14)$$

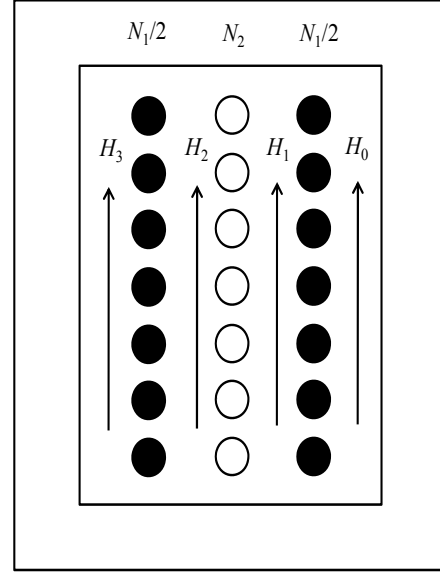
$$\delta_i = \sqrt{\frac{\rho}{\pi\mu_o F_s}} \quad (3.15)$$

where R_{layer} is the DC resistance of a layer, N_l is the number of turns in a layer, l_w is the layer width or winding width, d is a diameter of the wire used in a layer, and μ_o is the permeability of free space equal to $4\pi \cdot 10^{-7}$ H/m.

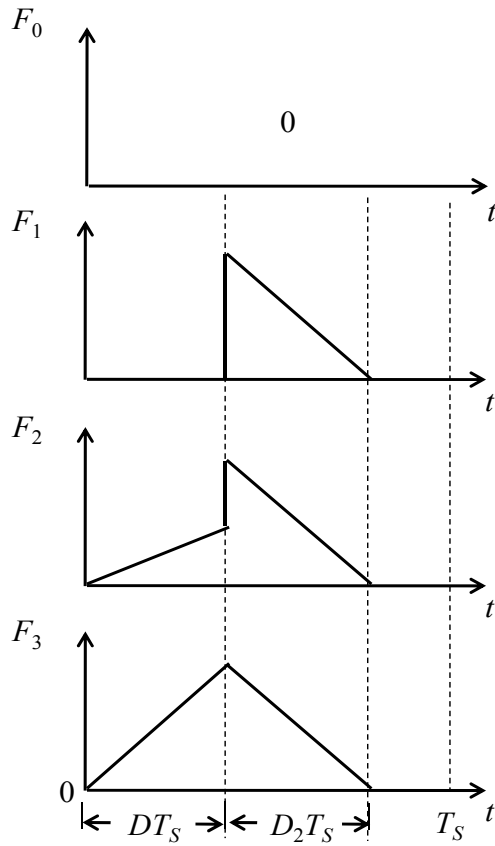
The air-gap of the transformer may have a significant influence on the AC winding resistance due to the fringing effects [27], [28]. However, these effects have not been included



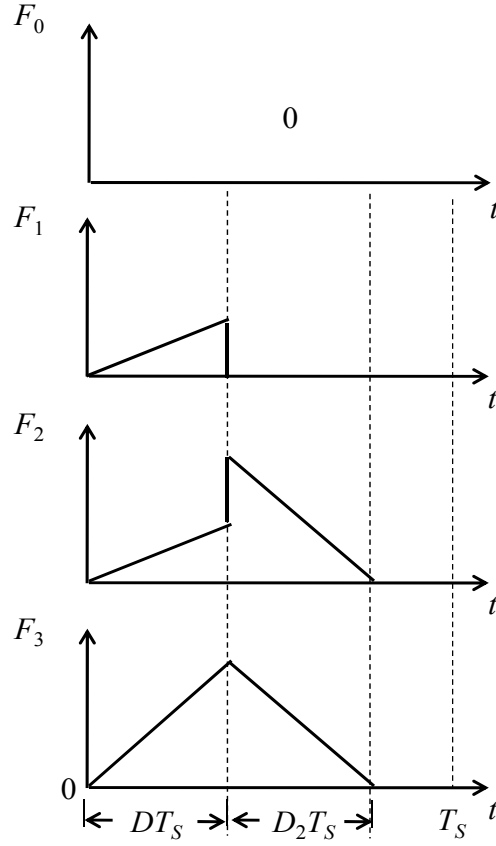
(a) non-interleaved transformer



(b) interleaved transformer



(c) MMF of non-interleaved transformer



(d) MMF of interleaved transformer

Fig. 3.2. Examples of transformer winding structures and MMF distributions for proximity loss modeling.

because of difficulties in incorporating necessary 2-D or 3-D finite element analysis in the optimization process.

The Steinmetz equation is generally used for core loss modeling when the magnetic flux density B is sinusoidal,

$$P_{core} = k \cdot f^{\alpha} \cdot B_{max}^{\beta} \quad (3.16)$$

where f is the frequency of sinusoidal ac excitation of magnetic flux density, B_{max} is the peak ac flux density amplitude, and k , α , and β are Steinmetz parameters. The manufacturers of magnetic core materials provide the data of core loss as a function of flux density with different temperatures and frequencies, as shown in Fig. 3.3, which is based only on sinusoidal excitation of magnetic flux density. So the Steinmetz parameters (k , α , and β) can be found from the data of core loss and curve fitting of the loss data to (3.16).

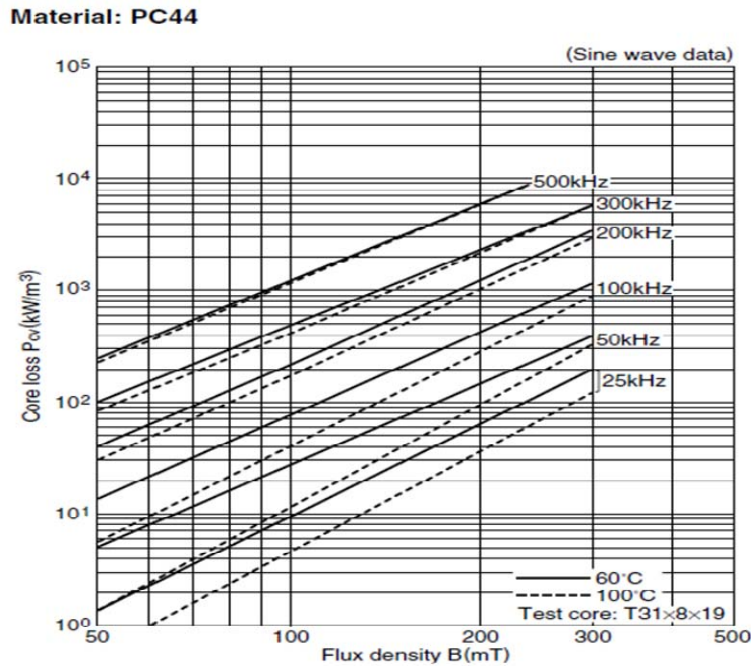


Fig. 3.3. Core loss as a function of flux density (PC44 power ferrite of TDK).

However, the magnetic flux density is not sinusoidal and the Steinmetz equation cannot be applied to core loss calculation of standard switch-mode power supplies such as the flyback converter. The improved Generalized Steinmetz Equation (iGSE) has been introduced in [29] to calculate the core loss, which allows for arbitrary (non-sinusoidal) waveforms. The magnetic flux density trajectory is split into major and minor loops to calculate the modified expression for time-average core loss (3.17) in which the same Steinmetz parameters (k , α , and β) are used.

$$P_{core} = \frac{1}{T_s} \int_0^{T_s} k_i \cdot \left| \frac{dB}{dt} \right|^\alpha \cdot (\Delta B)^{\beta-\alpha} dt \quad (3.17)$$

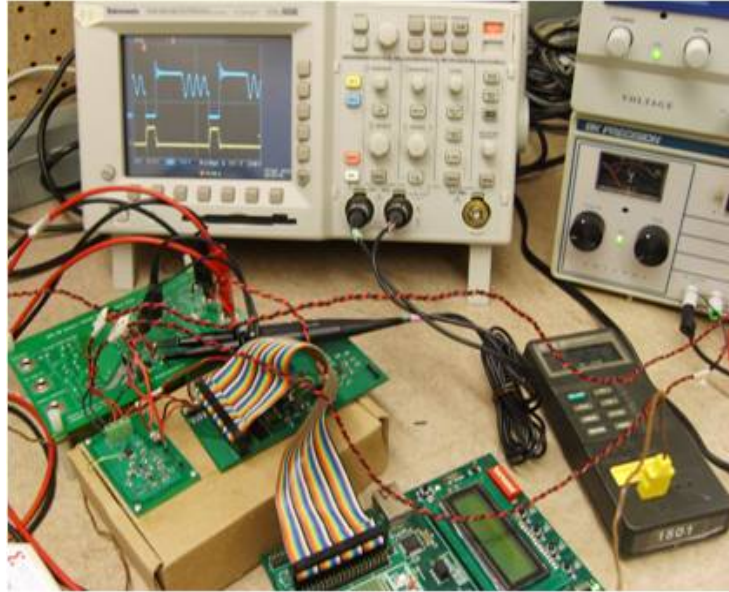
where

$$k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos \theta|^\alpha 2^{\beta-\alpha} d\theta} \quad (3.18)$$

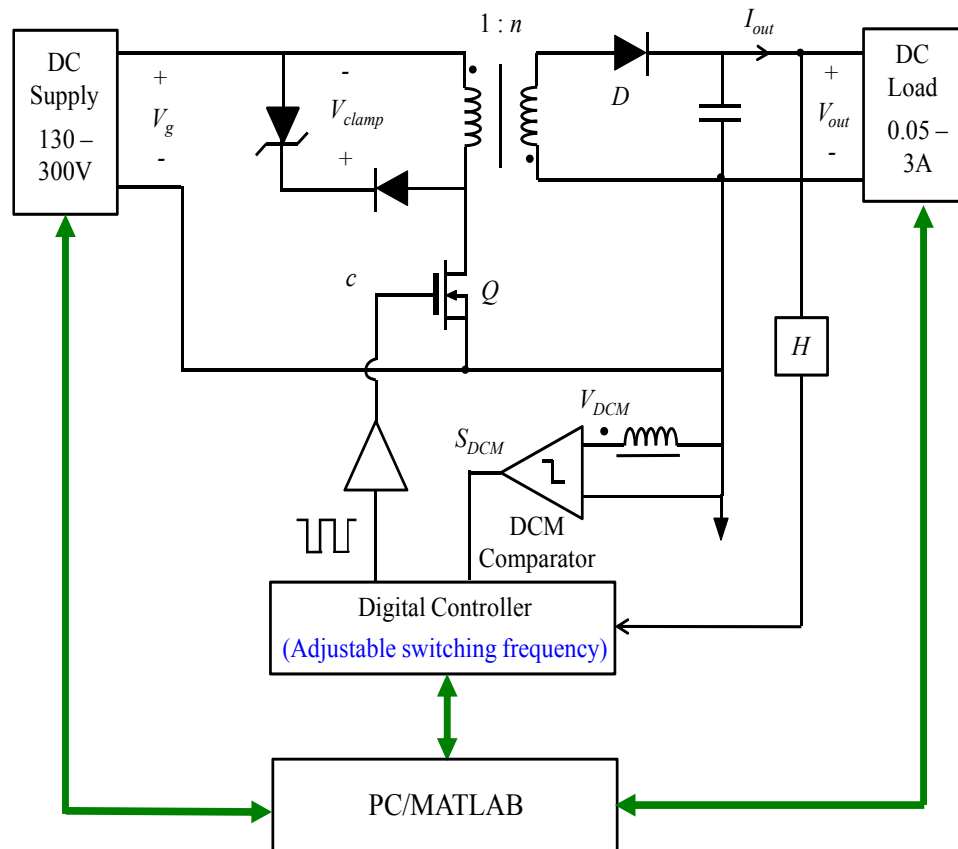
3.2 Comparisons with Experimental Efficiency Characterization Results

The experimental setup – shown in Fig. 3.4 – consists of a 65-W flyback DC-DC converter power stage [30] interfaced to a Virtex IV FPGA development board used as a digital controller, a programmable DC power supply, an electronic DC load, and efficiency characterization routines implemented in MATLAB on a PC.

The parameters of the power stage prototype in [30], which is used as a baseline design in this chapter, are: $V_g = 130V \sim 300V$, $V_{out} = 18V$, $I_{out} = 50mA \sim 3A$, $n = 0.22$, $L_M = 270\mu H$, $L_{lk} = 5.2\mu H$, $V_{clamp} = 150V$, $H = 0.07$. For the transformer a PQ 26/25 core of PC44 power ferrite (TDK) is used and the primary side is wound with $N_1 = 32$ turns of 0.5 mm TEX-E wire, while the secondary side has $N_2 = 7$ turns of 3 parallel AWG24 wires.



(a)



(b)

Fig. 3.4. Experimental setup for efficiency characterization.

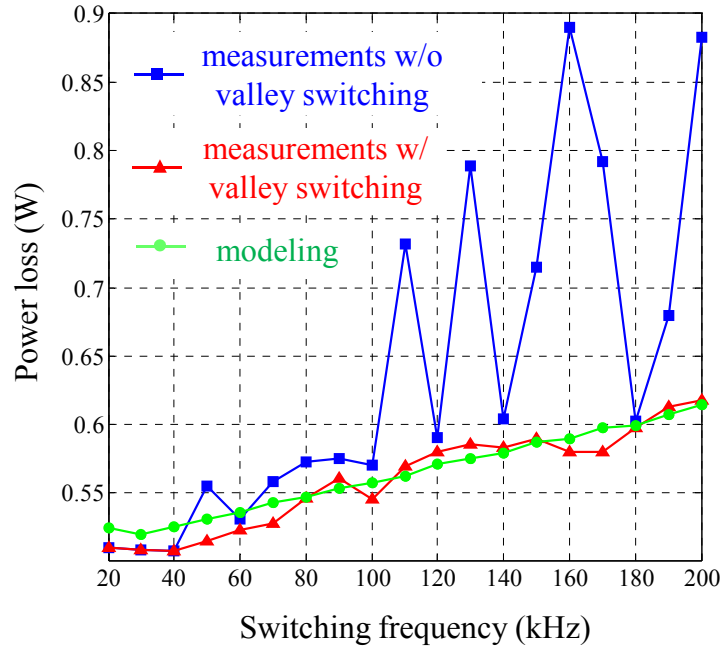
During efficiency characterization, the MATLAB/PC controls the DC power supply and the DC load as well as the switching frequency of the converter, and measures the input and output power. The digital controller regulates the output voltage via switch on-time, and communicates with MATLAB to receive the switching period command and commands to turn on or off the valley switching, and to send regulation status, on-time and DCM/CCM status. Valley switching is implemented using a state-machine in the digital controller, similar to [31]. If valley switching is enabled, the digital controller detects DCM comparator signal (S_{DCM}) to measure and store the oscillation period of the ringing (T_{OSC}). After the switching period set from MATLAB expires, the state machine waits for S_{DCM} transition and extends the switch off-time by $T_{OSC}/4$ such that the switch turns on at the minimum switching-node voltage in DCM.

In order to collect the efficiency data, the switching frequency was swept from 20kHz to 200kHz with a 10kHz step, with or without valley switching at various load currents (50mA ~ 3A) and input voltages (130V ~ 300V).

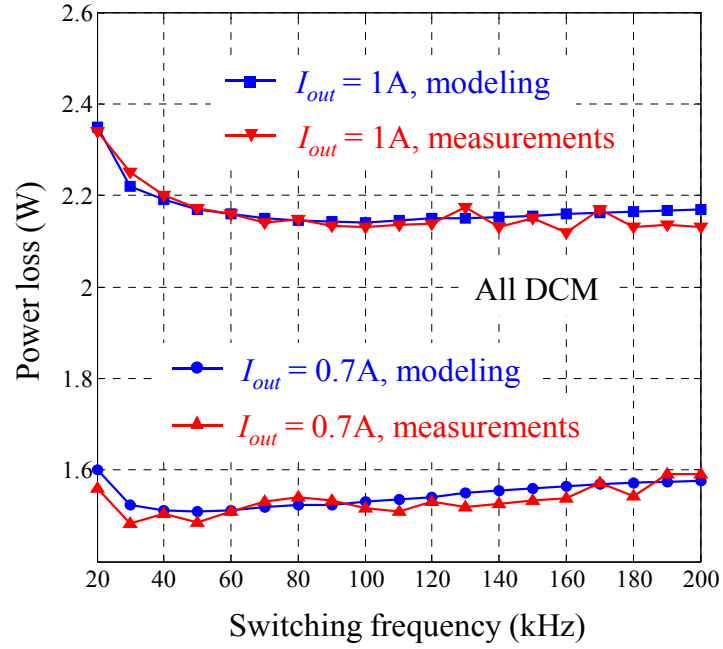
To validate the loss modeling, Fig. 3.5 shows a comparison of the power losses predicted by the model with the results obtained from the experimental characterization described in Section 3.2. The loss modeling predicts the total power dissipation within 5% of the measurement results. It should be noted how the valley switching results in significantly decreased power losses as shown in Fig. 3.5 (a), which is desirable for improved efficiency in DCM operation. At intermediate loads the power loss curves are relatively flat over the entire switching frequency range because the output diode conduction loss and the loss due to the leakage inductance are dominant.

3.3 Conclusions

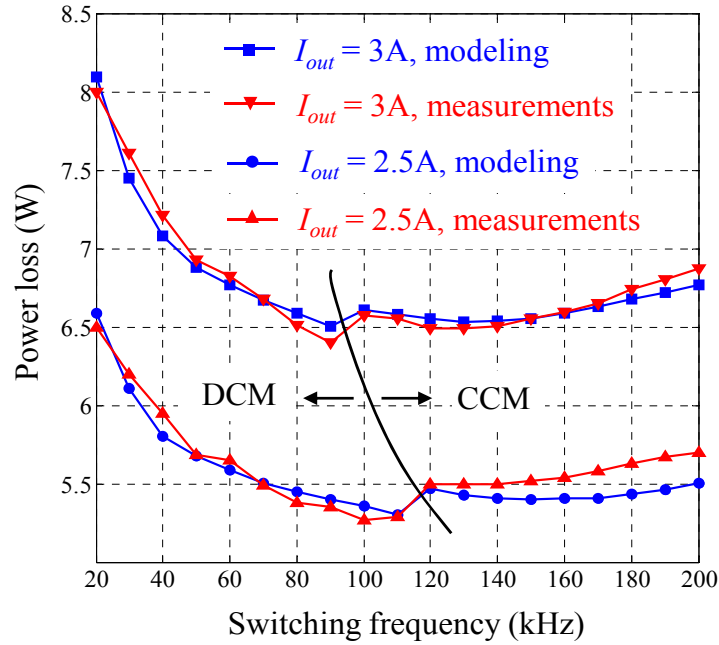
Power losses in a conventional flyback DC-DC converter are analyzed and modeled. The loss models are relatively simple but sufficiently detailed accurate for efficiency characterization and optimization over wide ranges of operating conditions. The detailed power loss modeling predicts the power dissipation within 5 % of experimental results. The experimental and power loss modeling results show that efficiency can be improved using valley switching in DCM. The best efficiency is obtained close to DCM/CCM boundary at heavy loads, and at a minimum frequency (20 kHz) at light loads. At intermediate loads, power loss curves are relatively flat over a range of switching frequencies due to the switching loss caused by the leakage inductance, and the conduction loss associated with the output diode.



(a) Power loss as a function of frequency at $V_g = 130\text{V}$ and $I_{out} = 0.25\text{A}$



(b) Power loss as a function of frequency at $V_g = 200V$ and $I_{out} = 0.7A$ and $I_{out} = 1A$



(c) Power loss as a function of frequency at $V_g = 200V$ and $I_{out} = 2.5A$ and $I_{out} = 3A$

Fig. 3.5. Power loss characterization at light, intermediate and heavy loads: comparison of results based on loss modeling and based on experiments.

Chapter 4

Efficiency Optimization in Flyback DC-DC Converters

Compared to a conventional flyback topology described in Chapters 2 and 3, various more advanced topologies have been proposed to improve efficiency. For example, the active-clamp flyback converter features soft switching and recycling of the energy stored in the leakage inductance (L_{lk}) [32] – [35]. Another approach is to replace the output diode with a synchronous rectifier, thus reducing the dominant conduction loss in relatively low output voltage applications [36] – [38]. However, these modifications come at increased cost. A number of switch-mode power supply design optimization approaches have been described in the literature [14] – [19]. In this chapter the optimization procedure, similar to [16], is proposed to optimize power stage design parameters (i.e. turns ratio n , number of turns in primary side N_1 , MOSFET Q , and snubber diode Zener voltage V_{clamp}) and controller parameters (switching frequency F_S and operating modes) based on detailed power loss models described in Chapter 3 and multi-variable non-linear optimization over wide ranges of operating conditions, while keeping low cost of the converter power stage. A valley switching technique is applied to reduce MOSFET turn-on switching loss in discontinuous conduction mode (DCM). An optimization procedure is formulated to minimize power loss weighted over a range of operating points, under a cost constraint. Experimental results with a 65 W flyback prototype demonstrate that combined

design-time optimization and controller optimization can lead to significant efficiency improvements.

4.1 Efficiency Optimization Procedure

A flyback converter design requires many trade-offs and iterations with a large number of design variables. The first step of the optimization procedure is to determine the external specifications of the converter (e.g. range of operating conditions, $V_{g,i}$ and $I_{out,j}$) and component limits used as constraints in the optimization. The core size, core material and the output diode are defined as the constraints in this optimization, and are kept the same as in the original baseline design [30], so that the power-stage cost remains essentially the same. Other constraints are defined for the selection of wires in the transformer, magnetizing inductance and the clamp voltage V_{clamp} in the snubber. Round wires are used for transformer windings and a window area is filled such that copper losses due to the DC resistances are minimized as described in [20]. The magnetizing inductance is determined for the core not to be saturated using

$$L_M I_{\max,Q} < N_1 B_{\max} A_C \quad (4.1)$$

where N_1 is the number of turns on the primary side, $B_{\max}$ is the maximum flux density and A_C is the cross-sectional area of the given core. The maximum possible clamp voltage V_{clamp} is selected based on the voltage rating of the selected MOSFET to minimize the leakage inductance loss given by (3.9). The interleaved transformer is employed in the optimization process because the leakage inductance can be significantly reduced compared to the non-interleaved transformer [27]. Furthermore, it was assumed that the controller employs valley switching at all DCM operating points.

Fig. 4.1 shows a flowchart of the optimization procedure, which is divided into two optimization processes. The most inner loop is the switching frequency optimization (i.e. the controller optimization) for a given set of design parameters and for a given set of operating points of interest. In the outer loop (i.e. the design optimization), the variable design parameters include the turns-ratio (n), the number of turns on the primary side (N_1) and the MOSFET (Q).

The objective function f is defined as a weighted sum of the converter losses over the set of operating points,

$$f = \sum_{i,j} \alpha_{i,j} \frac{P_{loss}(i,j)}{P_{out}(i,j)} \quad (4.2)$$

$$\sum_{i,j} \alpha_{i,j} = 1 \quad (4.3)$$

Note that the loss $P_{loss}(i,j)$ at an operating point (i,j) is normalized by the output power at the same operating point and weighted by a factor $\alpha_{i,j}$. The weight factors ($\alpha_{i,j}$) determine the importance of efficiency at each operating point. The process employs MATLAB function (*fmincon*) for multi-variable non-linear constrained optimization. The end results of the optimization procedure are the design parameters of the power stage and the optimum switching frequency to be implemented in the controller. This is particularly well suited for digital controller realization, where the optimum switching frequency can be easily programmed as a function of the operating point.

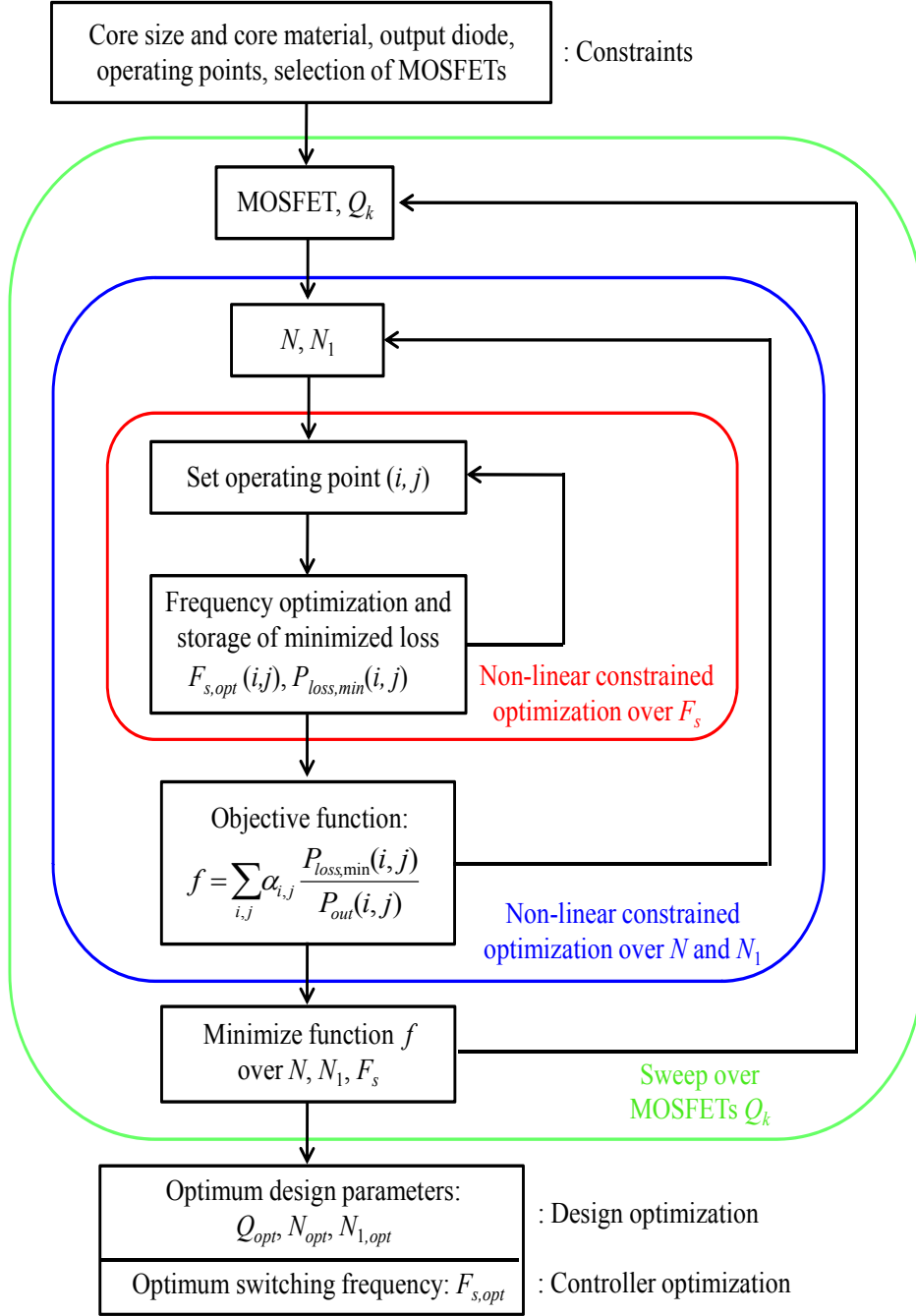


Fig. 4.1. Block diagram of efficiency optimization procedure. The optimum design parameters (n, N_1 and MOSFET) and optimum switching frequency (F_s) as functions of operating point (V_g, I_{out}) can be found simultaneously based on experimentally verified power loss models and multi-variable non-linear constrained optimization process.

4.2 Optimization Results

Fig. 4.2 shows nine operating points considered, and summarizes three cases taken as examples of the optimization procedure. The first case is that nine operating points – combinations of minimum, intermediate, and maximum input voltage, and minimum, intermediate, and maximum load current – are selected and equally weighted ($\alpha_{i,j} = 1/9$). This choice of the weights corresponds to a design where efficiency at each operating point is considered equally important. Equivalently, in this case the total power loss is minimized under the assumption that the time the converter spends at an operating point is inversely proportional to the output power. In the other two optimization examples, only one operating point is considered, $\alpha_{1,1} = 1$, or $\alpha_{3,2} = 1$, respectively.

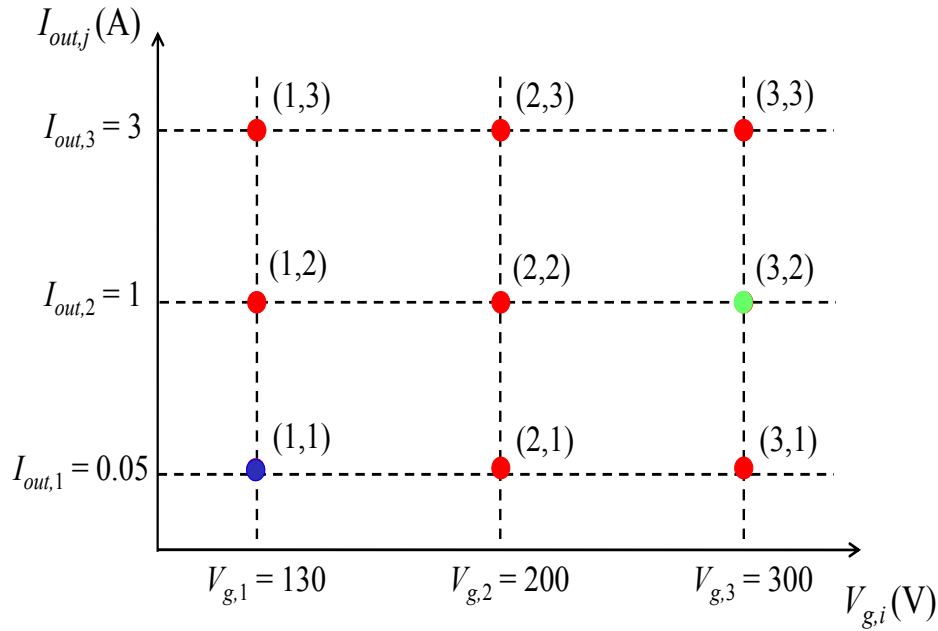


Fig. 4.2. Three optimization examples: case 1 ($\alpha_{i,j} = 1/9$), case 2 ($\alpha_{1,1} = 1$) and case 3 ($\alpha_{3,2} = 1$).

The ranges of design parameters and switching frequency are shown in Table 4.1. Two types of Infineon 600V MOSFETs and two types of 800V MOSFETs were considered. The voltage and current ratings of the considered MOSFETs, together with unit costs (1,000 pricing, Mouser Electronics), are shown in Table 4.1. Minimum and maximum boundaries of the turns-ratio are 0.15 and 0.50, respectively. The number of turns on the primary side is between 20 and 50. The switching frequency range covers DCM and CCM operations at most of the considered operating points.

Table 4.1. Ranges of design parameters

Parameters	Ranges for optimization
MOSFET	600V, 06A (SPP06N60C3, \$ 0.767) 600V, 11A (SPP11N60C3, \$ 1.160) 800V, 06A (SPP06N80C3, \$ 1.070) 800V, 11A (SPP11N80C3, \$ 1.690)
n	0.15 ~ 0.50
N_1	20 ~ 50
F_S	20kHz ~ 400kHz

Table 4.2 shows the optimization results for the 3 examples, in comparison with the original baseline design [30]. Note that the optimized design and the controller parameters are different in the 3 cases because of the different weight factors. In all cases, the 800V, 6A MOSFET was selected, the cost of which is slightly lower compared to the 600V, 11A MOSFET in the original baseline design. The MOSFET having a higher voltage rating results in reduced switching loss because it allows a higher clamp voltage, which reduces the loss (3.9) associated with the leakage inductance. Furthermore, the MOSFET with a higher on-resistance and a smaller output capacitance results in lower losses in these examples. The largest loss reduction

Table 4.2. Results of design optimization

	Case 1 ($\alpha_{i,j} = 1/9$)	Case 2 ($\alpha_{1,1} = 1$)	Case 3 ($\alpha_{3,2} = 1$)	Original design [30]
MOSFET	800V, 6A (SPP06N80C3)	800V, 6A (SPP06N80C3)	800V, 6A (SPP06N80C3)	600V, 11A (SPP11N60C3)
n	0.20	0.16	0.25	0.22
N_1	34	32	36	32
L_M	360 μ H	320 μ H	405 μ H	270 μ H
L_{lk}	2.6 μ H	2.4 μ H	2.7 μ H	5.2 μ H
V_{clamp}	400V	400V	400V	150V
Transformer	Interleaved	Interleaved	Interleaved	Non-interleaved
Wire in primary side	AWG#23	AWG#22	AWG#23	TEX-E (0.5mm)
Wire in secondary side	AWG#15	AWG#14	AWG#16	3 $\times$ AWG#24
# of layers in primary side	2	2	2	2
# of layers in secondary side	1	1	1	1

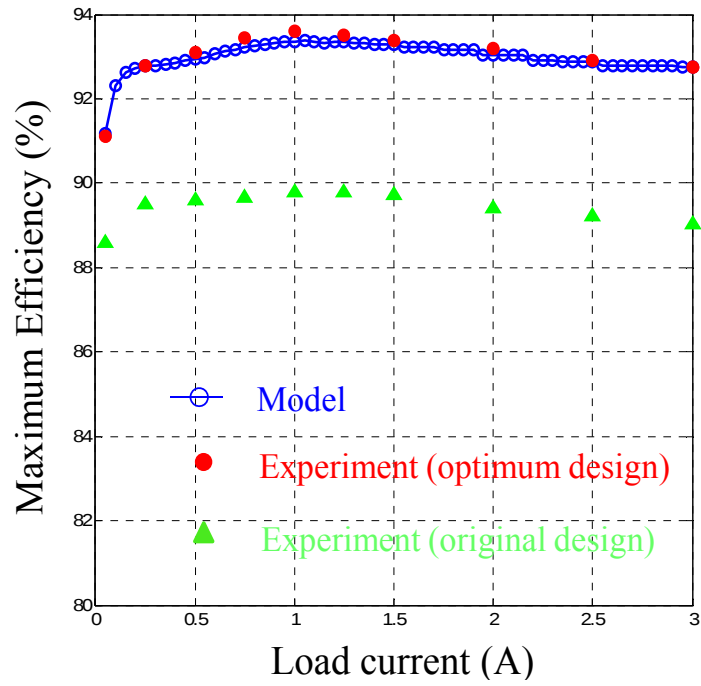
effect can be attributed to the reduction in the leakage inductance value by about one half due to the interleaved transformer windings.

Table 4.3 presents maximum efficiencies obtained from the optimization processes in the 3 cases compared to the baseline design, together with a comparison of the optimum switching frequencies. Compared to the original design, efficiency is improved by more than 3% in all 3 cases. Note that cases 2 and 3 result in the best efficiencies at the particular operating points (1, 1) and (3, 2), respectively.

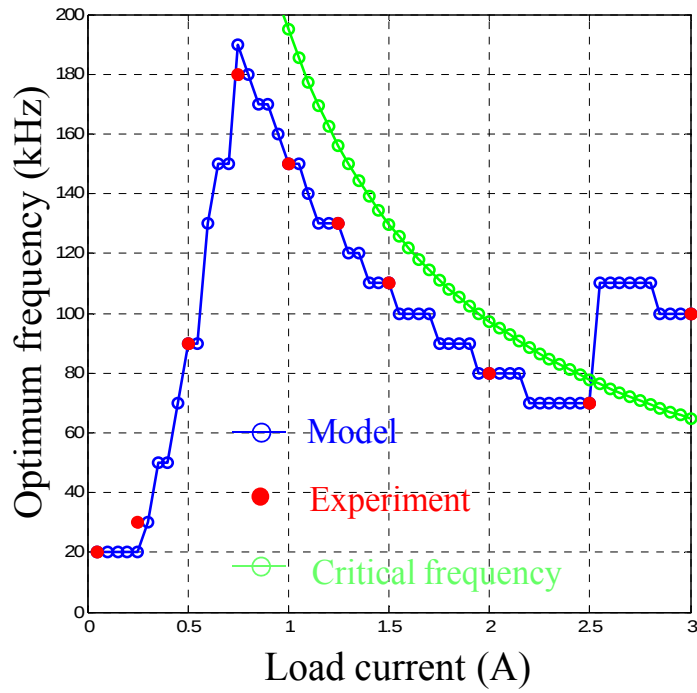
Table 4.3. Maximum efficiencies and optimum switching frequencies
in 3 cases at 9 different operating conditions

	Case 1 ($\alpha_{i,j} = 1/9$)		Case 2 ($\alpha_{1,1} = 1$)		Case 3 ($\alpha_{3,2} = 1$)		Original design [30]	
	η_{max} (%)	$F_{s,opt}$ (kHz)	η_{max} (%)	$F_{s,opt}$ (kHz)	η_{max} (%)	$F_{s,opt}$ (kHz)	η_{max} (%)	$F_{s,opt}$ (kHz)
130V, 50mA (1,1)	91.2	20	91.2	20	91.1	20	88.6	20
130V, 1A (1,2)	93.4	150	93.4	210	93.3	100	89.8	180
130V, 3A (1,3)	92.8	100	92.6	140	92.7	70	89.0	120
200V, 50mA (2,1)	88.6	20	88.7	20	88.4	20	85.1	20
200V, 1A (2,2)	92.6	140	92.7	180	92.7	110	89.6	190
200V, 3A (2,3)	92.7	70	92.5	110	92.6	80	89.6	90
300V, 50mA (3,1)	83.5	20	83.7	20	83.1	20	80.1	20
300V, 1A (3,2)	92.0	30	91.7	40	92.1	30	89.3	70
300V, 3A (3,3)	92.6	90	92.5	140	92.6	60	89.7	110

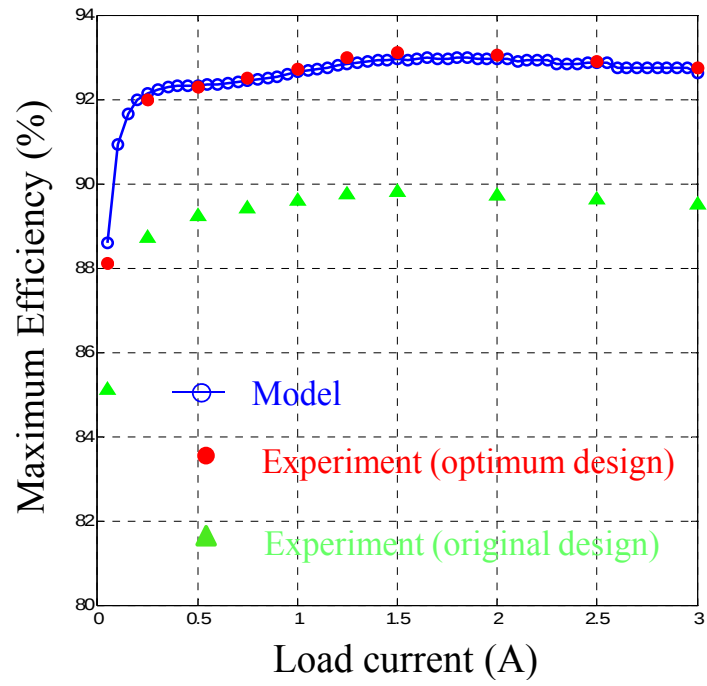
Fig. 4.3 shows efficiency characterizations for the optimization case 1 (equal weights for all 9 considered operating points): comparisons between the optimization and experimental results ((a), (c) and (e)), and optimum switching frequency as a function of load current with different input voltages ((b), (d) and (f)). The optimization results predict the efficiency within 0.3% and the switching frequency within 10 kHz under various operating conditions. Efficiencies greater than 92% are achieved under most operating conditions except at very light loads, with improvements of more than 3% compared to the original baseline design.



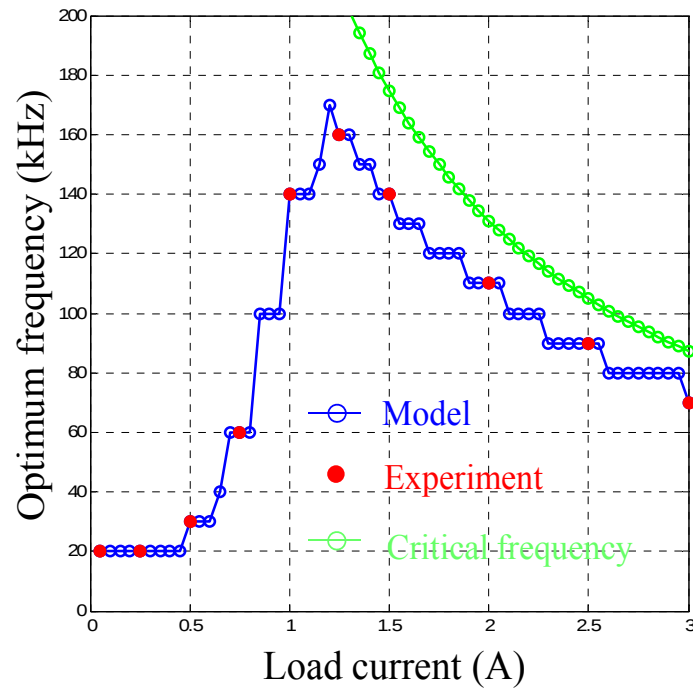
(a) Optimum efficiency as a function of load current at 130V



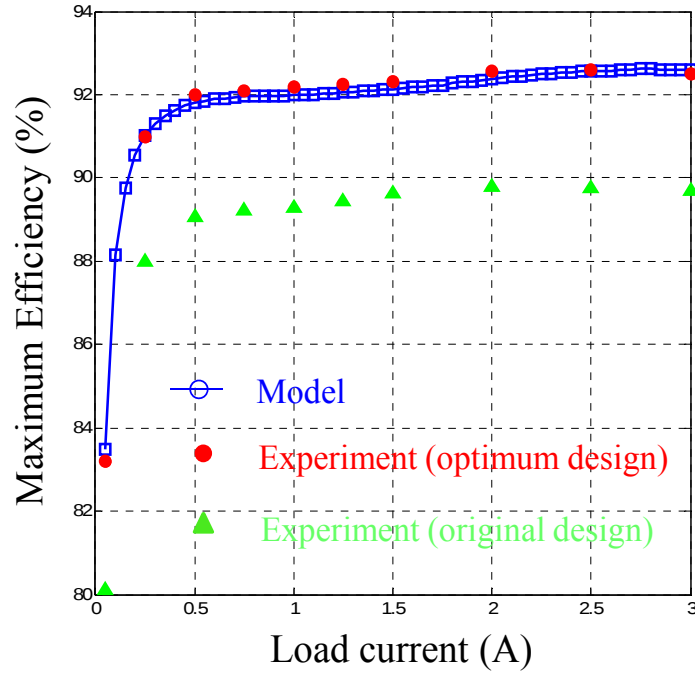
(b) Optimum switching frequency as a function of load current at 130V



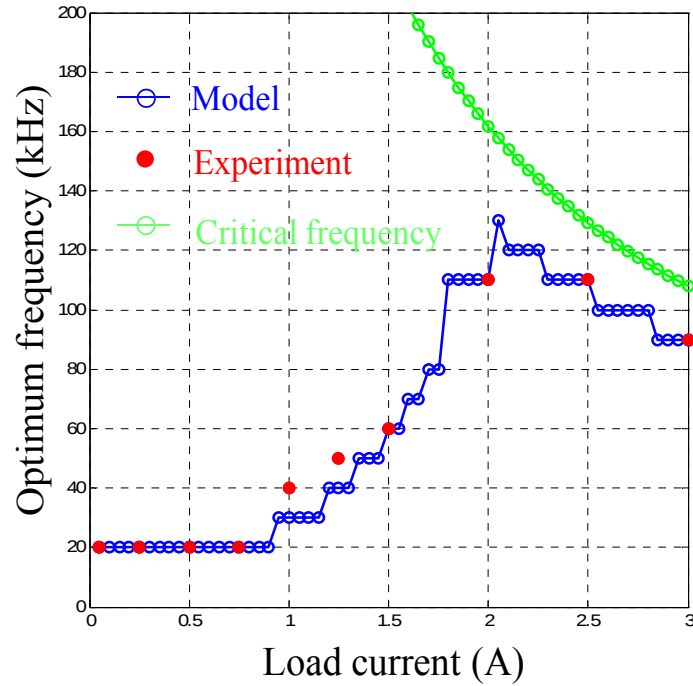
(c) Optimum efficiency as a function of load current at 200V



(d) Optimum switching frequency as a function of load current at 200V



(e) Optimum efficiency as a function of load current at 300V



(f) Optimum switching frequency as a function of load current at 300V

Fig. 4.3. Optimum efficiency ((a), (c) and (e)) and optimum switching frequency ((b), (d) and (f)) as functions of load current for case 1 optimum design, and the original design shown in Table 4.2 with 3 different input voltages (130V, 200V, and 300V).

Several interesting features of the optimum switching frequencies and operating mode can be deduced from the optimization and efficiency characterization results. The optimum switching frequency at light loads is in the vicinity of the lowest allowed switching frequency (20 kHz) because of dominant switching losses due to the switching-node capacitance. The optimum frequency at heavy and intermediate loads is close to the DCM/CCM boundary (i.e. close to the critical frequency) because the valley switching does not occur in CCM and the switching loss due to the switching-node capacitance increases abruptly as the converter moves from the DCM/CCM boundary to CCM. The optimum frequency drops below the DCM/CCM boundary frequency as the load drops below a value that depends on the input voltage. Another interesting point is that the best efficiency can be achieved in CCM at low input voltages and at heavy loads, as shown in Fig. 4.3 (b), when conduction losses are more dominant.

In conclusion, the best operating mode and the optimum switching frequency can be found from the optimization procedure and programmed in a digital controller as functions of the measured or estimated operating conditions. Fig. 4.4 shows a summary of the best operating modes. The controller employs valley switching under all DCM operating conditions and selects the appropriate operating modes in different regions – a minimum fixed switching frequency at light loads (20kHz), a switching frequency stored in a look-up table at loads where the optimum frequency is below the DCM/CCM boundary frequency, operation close to critical conduction mode (DCM/CCM boundary) at intermediate and heavy loads, and operation in CCM at low voltages and at heavy loads. Experimental waveforms for the representative operating points A – D in Fig. 4.4 are shown in Fig. 4.5.

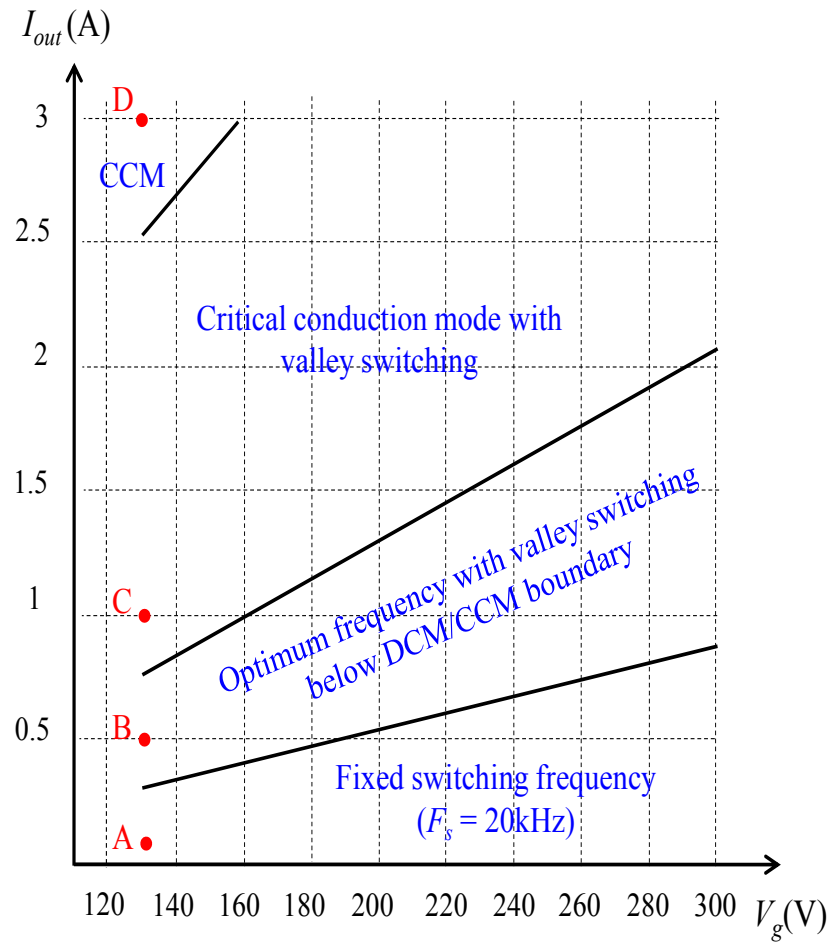
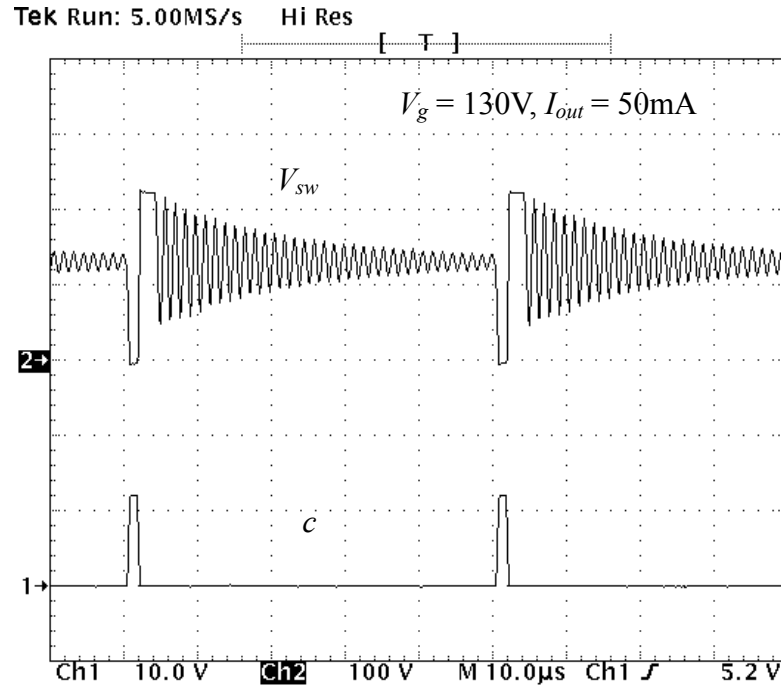
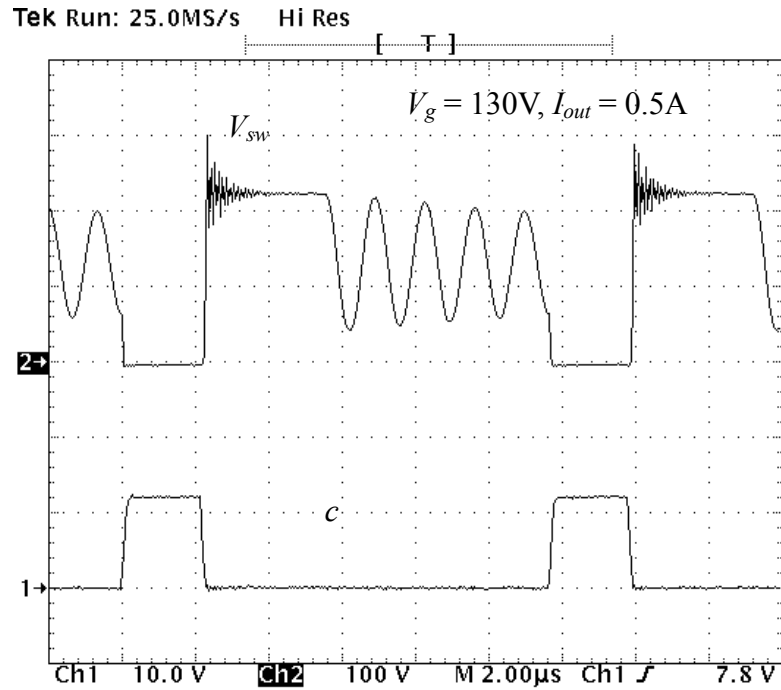


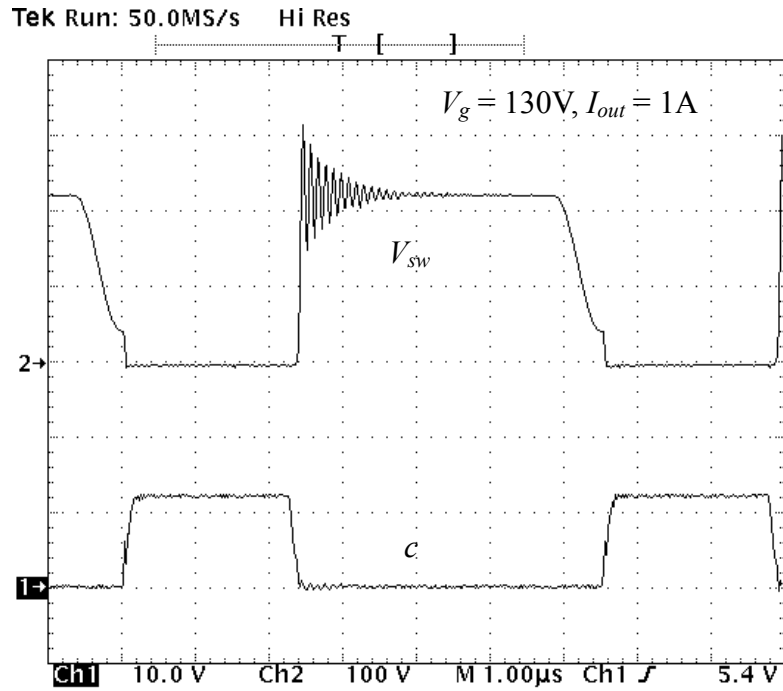
Fig. 4.4. Operating modes based on operating conditions.



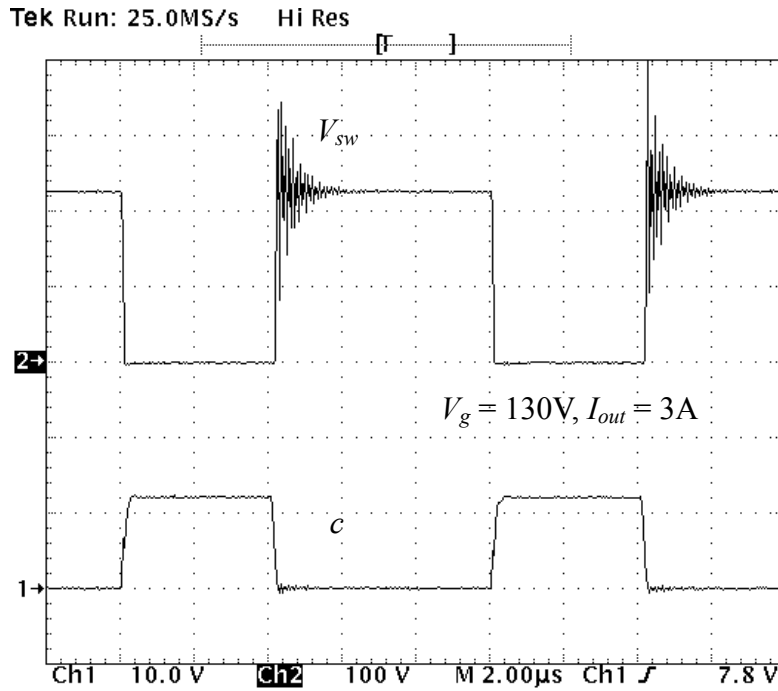
(a) Waveforms at point A (fixed minimum switching frequency, $F_s = 20$ kHz)



(b) Waveforms at point B (switching frequency below DCM/CCM boundary, $F_s = 90$ kHz)



(c) Waveforms at point C (critical conduction mode, $F_s = 150\text{ kHz}$)



(d) Waveforms at point D (CCM, $F_s = 100\text{ kHz}$)

Fig.4.5. Waveforms of switching-node voltage (V_{sw}) and control signal (c) at different operating modes: point A (a), point B (b), point C (c) and point D (d).

4.3 Conclusions

Efficiency of a DC-DC flyback converter is characterized and optimized over wide ranges of operating conditions based on detailed power loss models and multi-variable non-linear constrained optimization. The proposed optimization approach can be separated into two optimization processes – the design parameter optimization and the controller parameter optimization – enabling the power stage design and the controller design simultaneously while keeping low cost and resulting in significant efficiency improvements. Furthermore, this approach is very suitable for a digital control implementation because the optimum controller parameters can be simply stored in a look-up table. The optimization results for 3 design examples are shown, one of which is experimentally verified. The optimization and experimental results for a 65-W flyback converter show that efficiency can be significantly improved over wide ranges of operating conditions.

Chapter 5

Digital Controller Design for On-Line Efficiency Optimization

This chapter presents a relatively simple look-up table based digital control approach for on-line efficiency optimization over wide ranges of operating conditions. The proposed digital controller allows programmable modes of operation in the look-up table based on efficiency characterization and optimization. The proposed approach is simpler and more general compared to other on-line efficiency optimization techniques. Programmability of the optimum controller parameters is discussed in Section 5.1. A particular problem has been observed related to undesirable frequency hopping in mode 2 (look-up table based frequency operation), or over different operating modes, where the controller tends to jump between different switching frequencies corresponding to different numbers of DCM oscillation periods. This behavior, commonly observed in other valley-switching control schemes, is undesirable because of increased output voltage ripple and possible audible noise. Section 5.2 presents solutions to this problem and experimental results, together with analysis of efficiency improvements due to the optimization processes. Section 5.3 addresses dynamic operation of the controller. To improve large-signal transient responses, a gain-scheduled compensator is employed, and a new control scheme, named the k -control, is proposed such that the valley switching points dynamically change during transients. Small-signal ac models are derived and analyzed both in DCM and in

CCM to determine the compensator and k -control parameters over different operating modes. This chapter is concluded in Section 5.4.

5.1 Optimum Controller Parameters Based On Efficiency Optimization

Fig. 5.1 shows a block diagram of the proposed digital controller, around a conventional flyback DC-DC converter. As described in Chapter 4 and [39], the proposed efficiency optimization approach results in the optimum power stage parameters under a cost constraint, and optimum controller parameters: operating modes and switching frequencies F_s over various

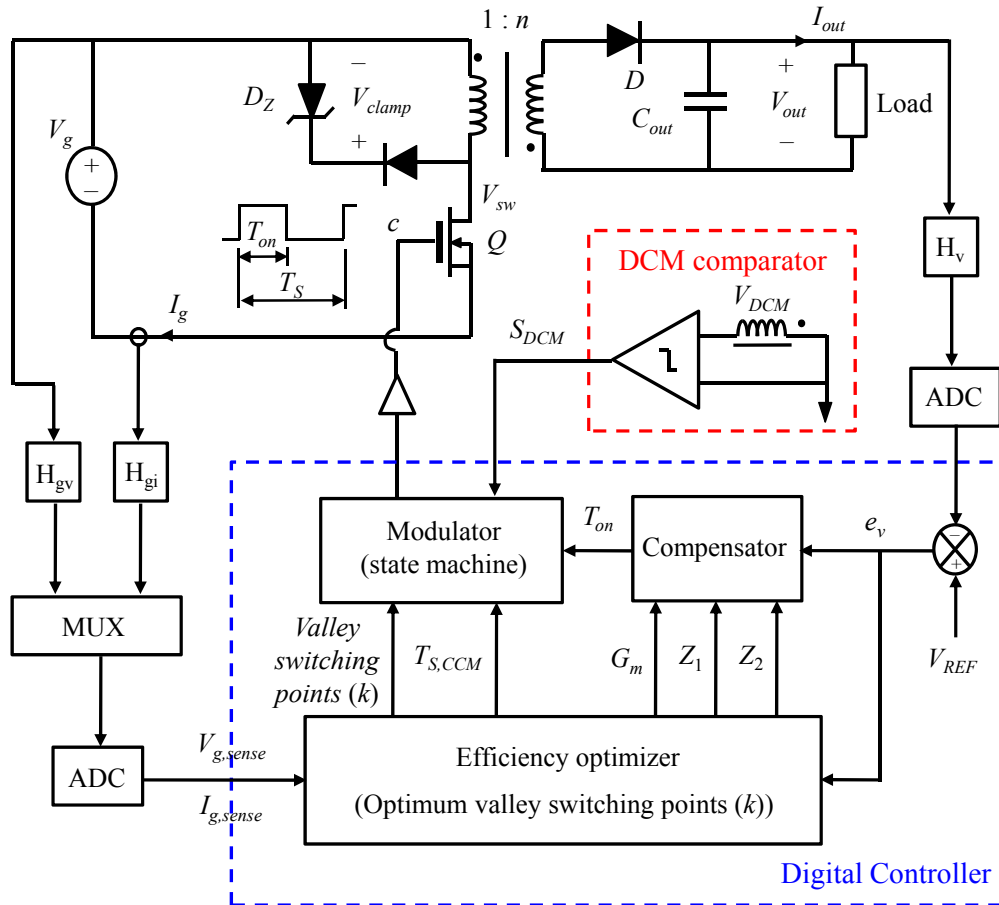


Fig. 5.1. Block diagram of a digital controller with look-up table based on-line efficiency optimization for a conventional flyback DC-DC converter.

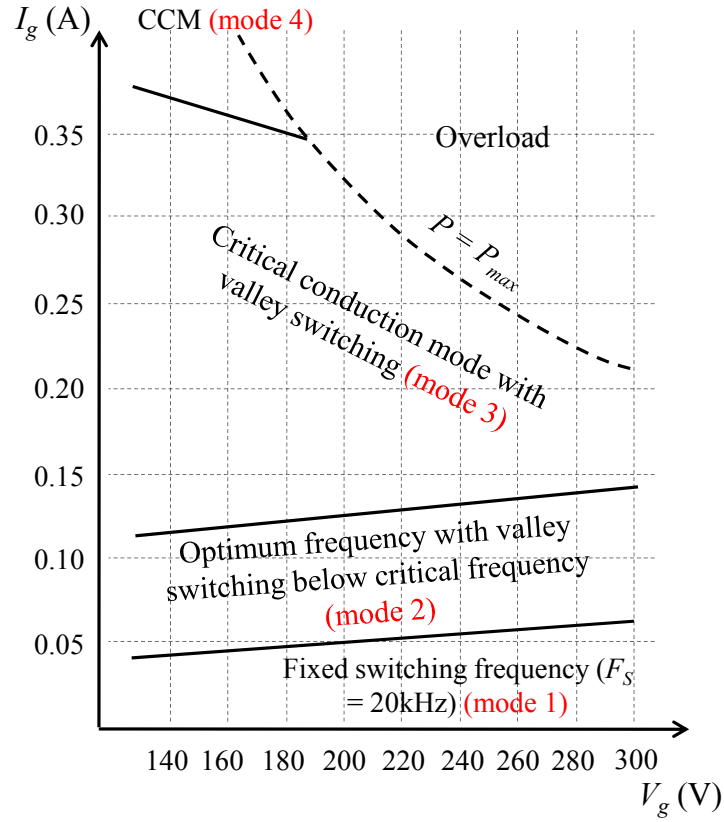
operating conditions. The optimum controller parameters can be programmed in the digital controller, which presents simpler and more general approach compared to other on-line efficiency optimization approaches.

The digital controller is designed for the optimization case 1, where all operating points are equally weighted ($\alpha_{i,j} = 1/9$) as presented in Chapter 4. The constrained and optimized parameters of the 65-W power stage prototype are summarized in Table 5.1.

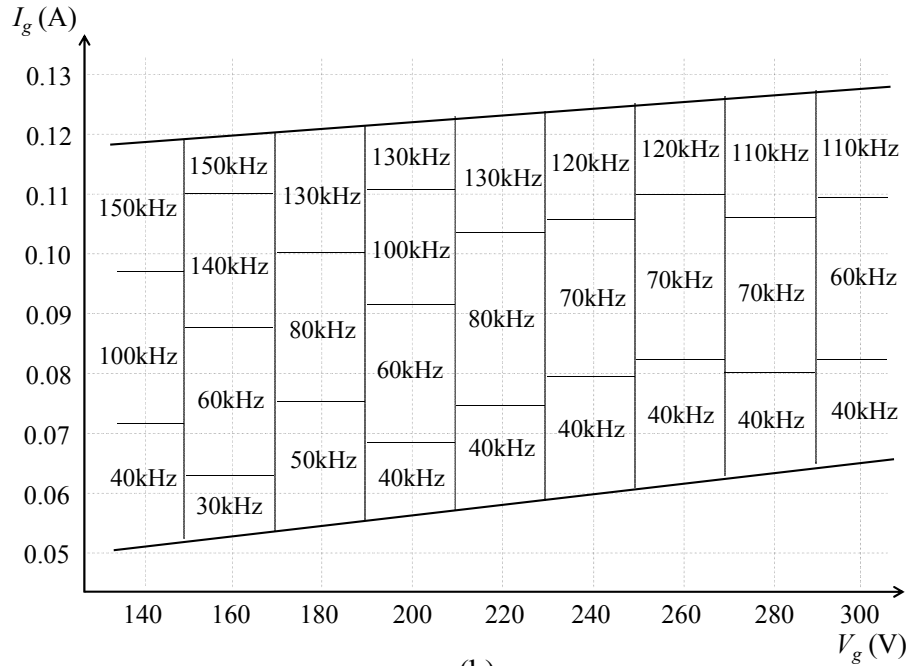
Table 5.1. Flyback power stage parameters

Parameters	Values
Input voltage, V_g	130 – 300V
Output voltage, V_{out}	18V
Load current, I_{out}	0.05 – 3A
Switching frequency, F_s	20 – 200kHz
Turns ratio, n	0.20
Magnetizing inductance, L_M	360 μ H
Leakage inductance, L_{lk}	2.6 μ H
Transformer type	Interleaved
MOSFET, Q	800V, 6A (SPP06N80C3)
Output capacitance, C_{out}	4,500 μ F
Clamp voltage, V_{clamp}	400V

The four different operating modes and optimum switching frequencies obtained from the efficiency optimization approach are shown as functions of the operating conditions (input voltage V_g and input current I_g) in Fig. 5.2 (a) and (b). Note that the optimum controller parameters are characterized over a range of input current instead of output current because the input current is sensed to detect the operating conditions. The near-linear mode boundaries



(a)



(b)

Fig. 5.2. (a) Optimum operating modes 1 – 4 as functions of operating conditions (input voltage V_g and input current I_g) and (b) optimum switching frequency $F_{s,OPT}$ stored in the look-up table for mode 2.

simplify the look-up table in the controller. The modes include operation at a minimum fixed switching frequency (20kHz) (mode 1), a switching frequency with valley switching (below a critical switching frequency) stored in a look-up table (mode 2), operation close to the critical conduction mode with valley switching (mode 3), and operation in continuous conduction mode (CCM) at optimum switching frequencies stored in a look-up table (mode 4). The switching frequency look-up table in mode 2 is designed such that the optimum switching frequency is assigned at the center of the corresponding slots. Efficiency at the boundaries related to input current deviates around 0.1% from the optimum efficiency. As shown in Fig. 5.2(b), the look-up table size is relatively small, having 29 entries. Fig. 5.3 presents efficiency deviation as a function of the number of look-up table entries, which illustrates how granularity of the look-up table is a trade-off between the table size and the efficiency loss due to operation away from the optimum switching frequency.

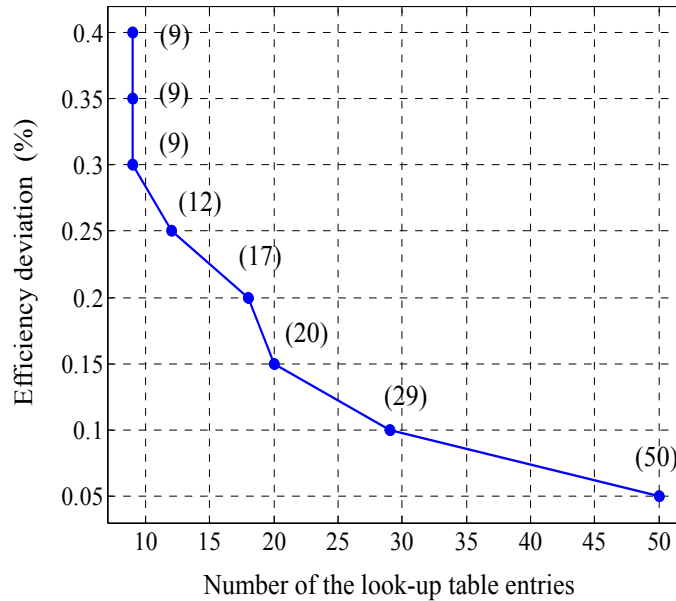


Fig. 5.3. Efficiency deviation as a function of the number of look-up table entries.

5.2 Static Operation of the Proposed Digital Controller

As commonly observed in other approaches based on valley switching, undesirable frequency hopping can occur in mode 2, where the target switching frequency is set in the look-up table as a function of input voltage and input current, or over different operating modes. The controller tends to jump between different switching frequencies corresponding to different numbers of DCM oscillation periods. This behavior is undesirable because of increased output voltage ripple and possible audible noise. In this section it is shown how the frequency hopping problem is caused by two different mechanisms, and solutions are proposed, together with digital controller implementation and corresponding experimental results

5.2.1 Frequency Hopping Mechanism #1

Valley switching is implemented using a state-machine in the digital controller, similar to [31]. The state-machine is programmed such that the switch turns on at the first valley switching point after the optimum switching period $T_{S,OPT}$ stored in the look-up table. However, the valley switching point does not pass the boundary of the optimum switching period consistently at certain operating conditions, resulting in the frequency hopping by one DCM oscillation period in mode 2 (Fig. 5. 4).

An approach to addressing this frequency hopping mechanism in an analog control scheme has been proposed in [40], using an adaptive blanking time control. In [40] two blanking times (T_{limit1} and T_{limit2}) and a window detection time (T_C) are properly determined and the blanking times are adaptively changed under certain load conditions.

The digital controller allows a relatively simple approach to eliminating the frequency hopping mechanism #1, by storing the optimum valley switching points k_{opt} in the look-up table

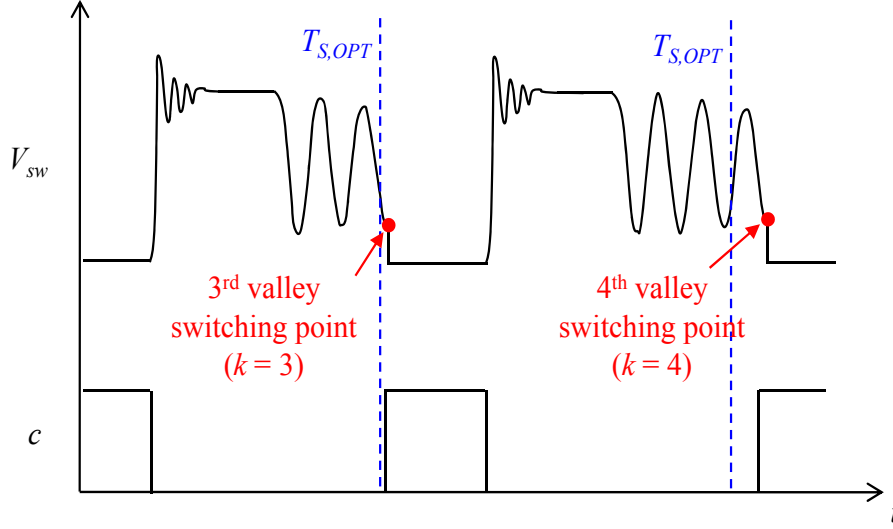
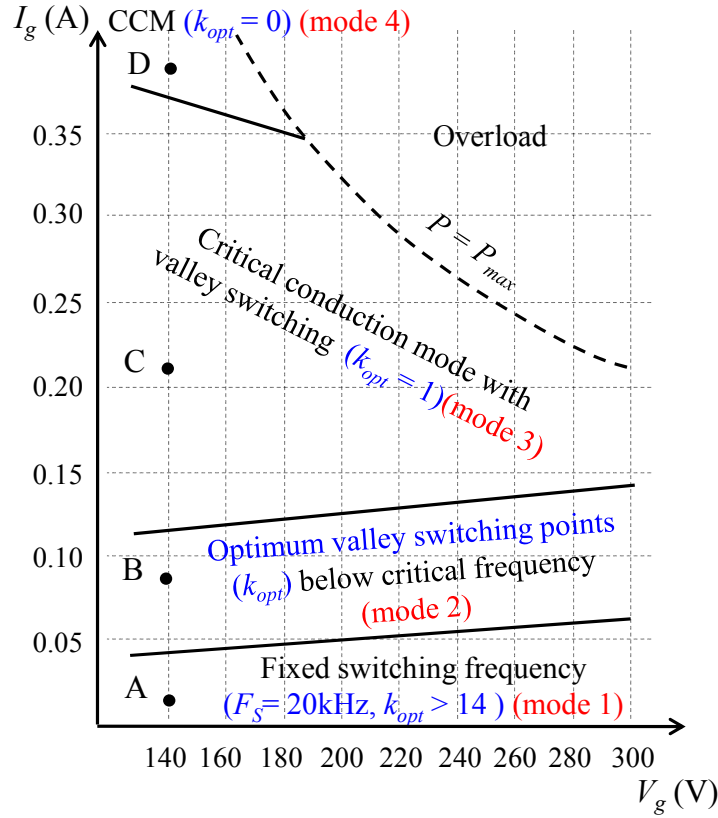
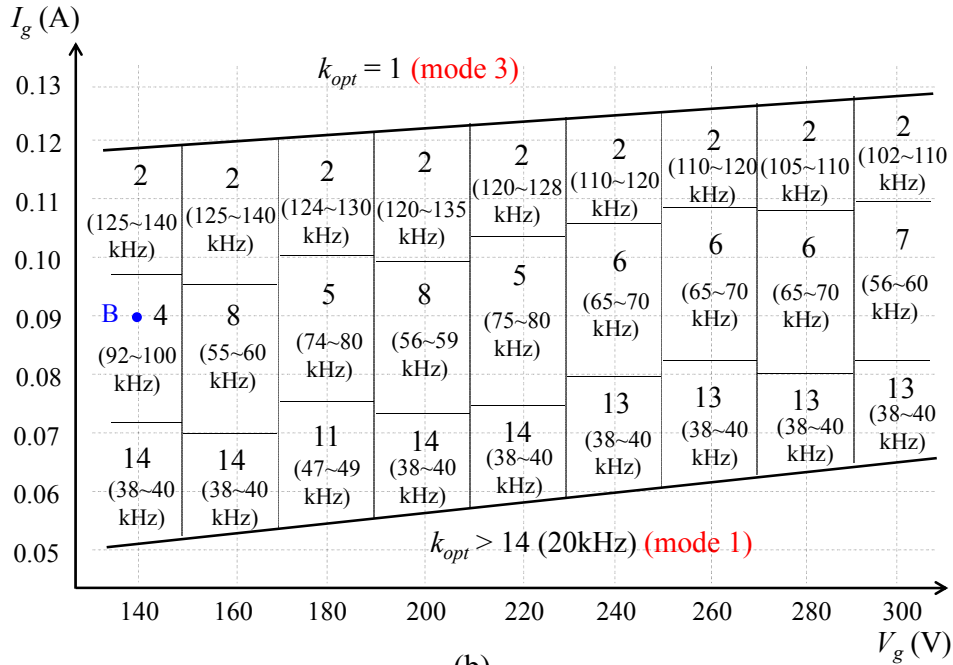


Fig. 5.4. Example of frequency hopping mechanism#1 (switching-node voltage (V_{sw}) and control signal (c)) – jumping from 3rd valley switching point ($k = 3$) to 4th valley switching point ($k = 4$).

instead of the optimum switching periods or frequencies. The state-machine can be easily modified such that the valley switching points are counted. The switch turns on at the valley switching point k_{opt} stored in the look-up table. The optimum valley switching points are obtained from the power loss model used for the controller optimization described in Chapter 4. Another advantage of this approach is that a smaller look-up table can be obtained compared to the look-up table storing the optimum switching period (Fig. 5.2 (b)). Fig. 5.5 shows the optimum operating modes and the modified look-up table for mode 2 in terms of the optimum valley switching points k_{opt} with measured switching frequencies in each slot. The measured switching frequencies corresponding to the optimum valley switching points are comparable to the optimum switching frequencies obtained from the controller optimization. Valley switching is not employed in mode 1 because at long switching periods the oscillation decays so valley switching benefits are lost. Instead, in mode 1, the converter operates at a pre-set minimum switching frequency (20 kHz).



(a)



(b)

Fig. 5.5. (a) Optimum operating modes 1 – 4 as functions of operating conditions (input voltage V_g and input current I_g) and (b) optimum valley switching points (k_{opt}) stored in the look-up table for mode 2.

5.2.2 Frequency Hopping Mechanism #2

As implied by the look-up table shown in Fig. 5.5, the valley switching points are abruptly changed at specific values of the input current or the input voltage. Smooth changes of optimum valley switching points depend on the size of each slot in the look-up table. The smaller the size of the slots, the smoother the changes are across the slots. When the input current or the input voltage is at a slot boundary, switching frequency hopping is observed due to jumps in the selected values of k_{opt} .

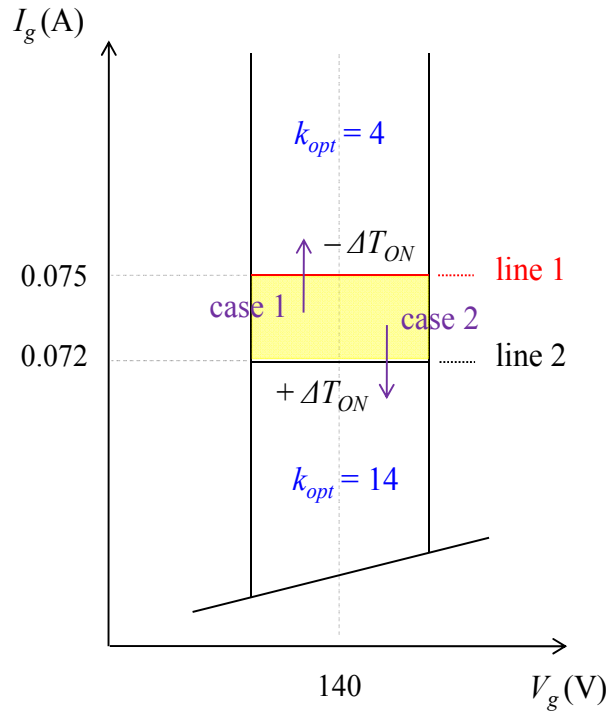


Fig. 5.6. Example of a hysteresis band added to a boundary in mode 2.

To address this frequency hopping mechanism, hysteresis bands are used at the look-up table slot boundaries. Fig. 5.6 shows an example of how the hysteresis is applied to one of the boundaries. Line 2 is an existing boundary and line 1 is a boundary of the added hysteresis band.

The value of k_{opt} is decided according to operating conditions. For example, if the input current I_g smoothly increases and passes line 1 (case 1), the valley switching point k_{opt} changes to 4. At the same time, ΔT_{ON} is subtracted from the switch on-time T_{ON} to minimize the disturbance caused by the change in k_{opt} . Upon this transition, the boundary changes to line 2. If the input current smoothly decreases and passes across line 2 (case 2), the hysteresis function is performed in the direction opposite to case 1.

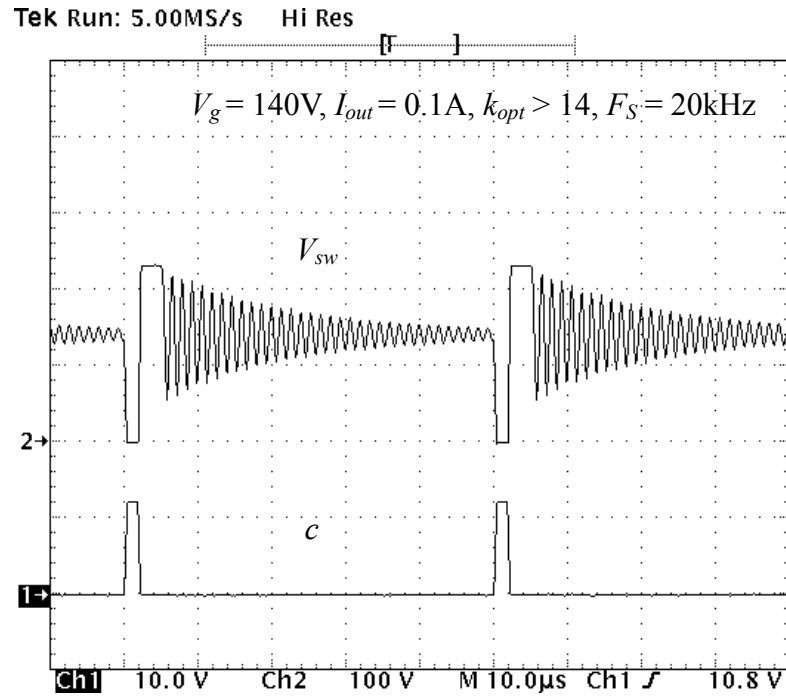
5.2.3 Digital Controller Implementation

As shown in Fig. 5.1, the feedback control loop consists of sensing and A/D conversion of the output voltage, a compensator which computes the switch on-time T_{ON} once per switching cycle, and a variable-frequency modulator implemented as a state machine. Detailed modulator implementation in the controller is presented in Appendix A. The input current, along with the input voltage, are sensed once per switching period, using a relatively slow, low-resolution A/D converter. The sensed values are low-pass filtered using an analog RC filter to obtain averaged values indicative of the operating point. The bandwidth of the RC filter is determined as a compromise between speed of efficiency optimization actions, and sensitivity of the controller. The efficiency optimizer block includes a look-up table which outputs the optimum valley switching points k_{opt} for modes 1 – 3, and the optimum switching periods $T_{S,CCM}$ for mode 4. In order to achieve smooth mode transitions and consistent dynamic responses, the compensator parameters (gain G_m , zeros Z_1 , Z_2) are also updated by the efficiency optimizer block. The compensator parameters are selected from small-signal modeling analysis over various operating conditions, as discussed further in Section 5.3.

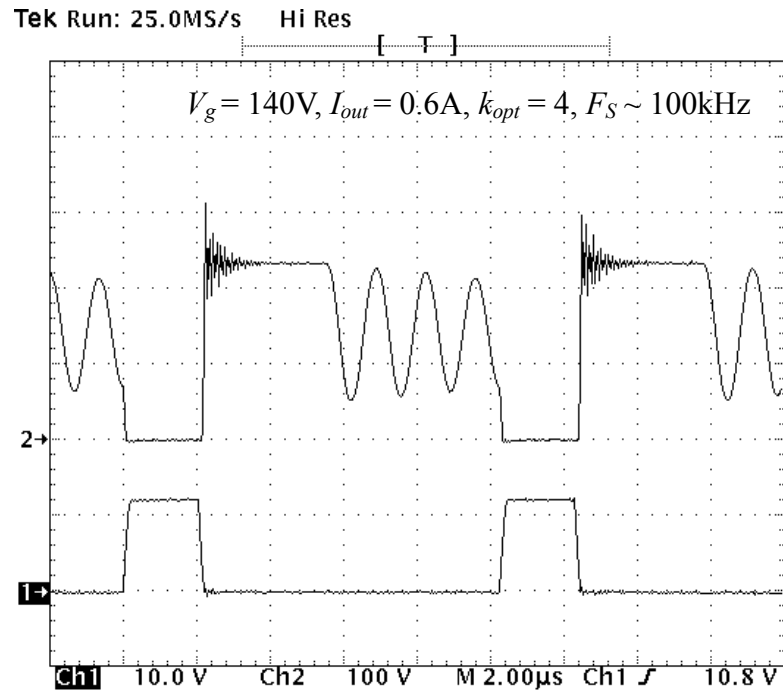
5.2.4 Experimental Results

Fig. 5.7 presents measured steady-state waveforms of the switching-node voltage V_{sw} and control signal c at the representative operating points A – D in Fig. 5.5 (a) and (b), showing how the controller properly selects the modes and the valley switching points k_{opt} .

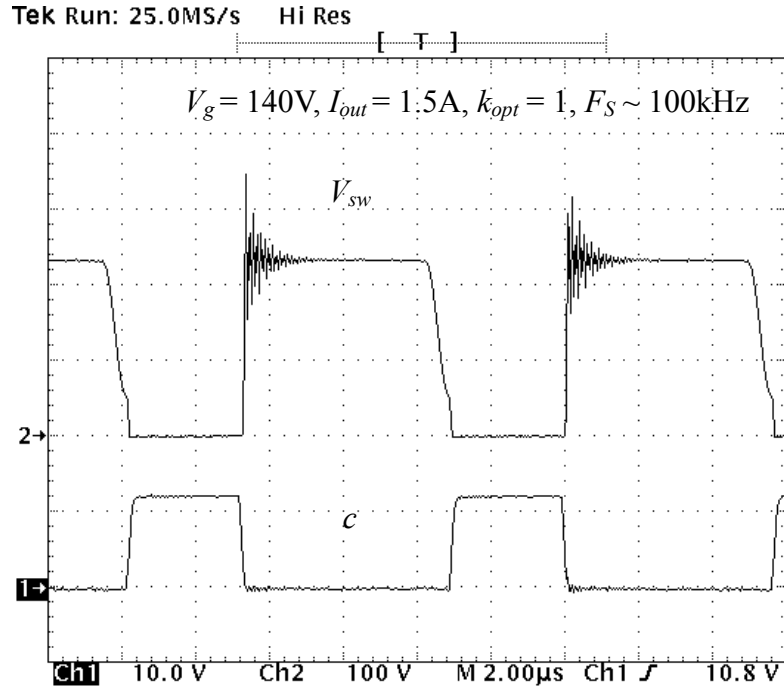
Fig. 5.8 presents comparisons of efficiencies as functions of the load current with 3 different input voltages (140V, 220V and 300V), for 3 cases: (case 1) efficiency based on the results of efficiency optimization using power loss modeling and multi-variable non-linear constrained optimization, (case 2) experimentally measured efficiency with the same 65-W flyback prototype using the proposed digital controller with on-line efficiency optimization, and (case 3) experimentally measured efficiency of the 65-W flyback prototype [30] with the analog green-mode controller [5] used as a baseline in this comparison. An assumption is made that a custom digital controller chip implementing the proposed techniques would have the same or lower power consumption as the baseline analog controller. As shown in Fig. 5.8, model based optimization and actual experimental results are consistent at all operating points (within 0.3%), except at very light loads due to a loss in the resistive voltage divider used for input voltage sensing, which was not included in the loss model. Efficiency of the optimized flyback prototype with the digital controller (case 2) exceeds 92% at all operating points over approximately 3:1 range of input voltages and 10:1 range of loads, with significant improvements of more than 3% at intermediate and heavy loads to about 8% at very light loads and low voltages compared to the baseline design (case 3).



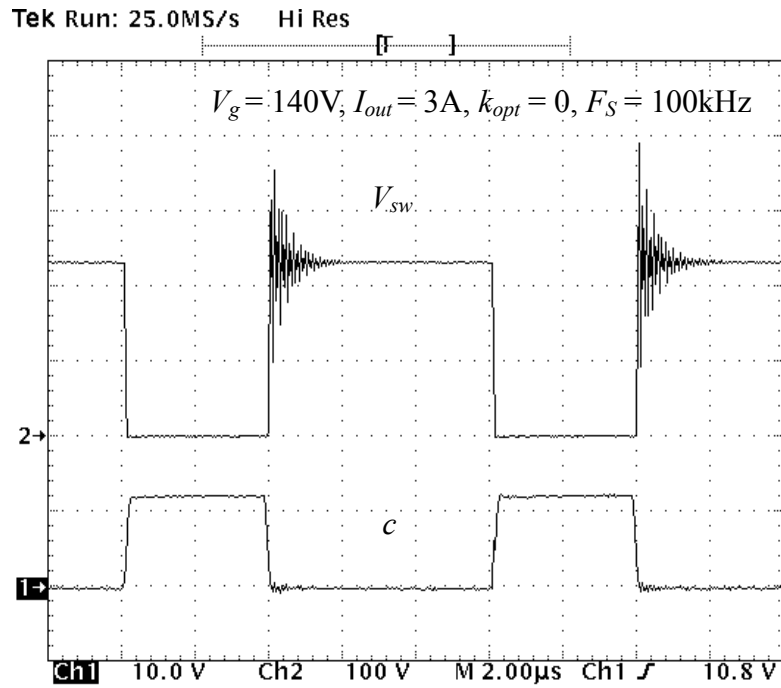
(a) Waveforms at point A (mode 1)



(b) Waveforms at point B (mode 2)

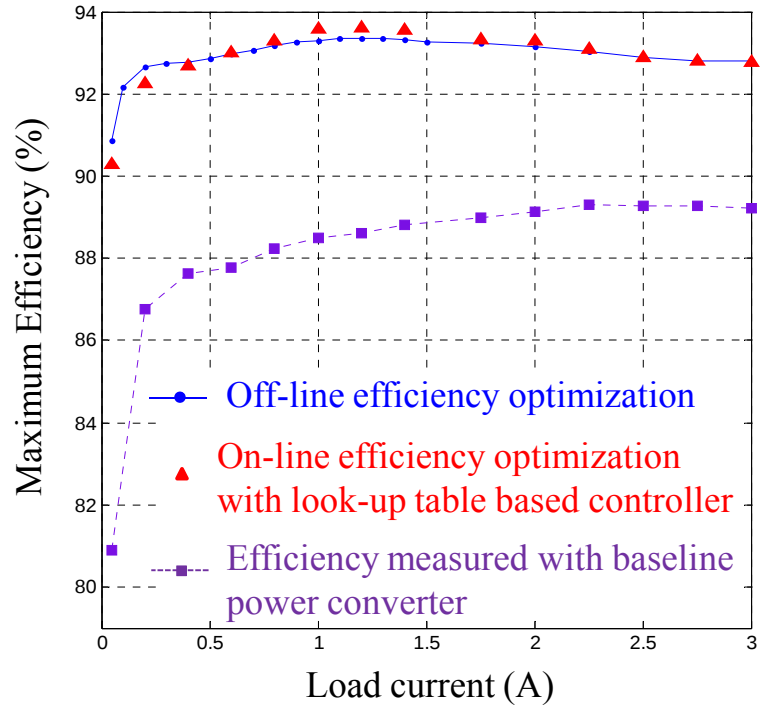


(c) Waveforms at point C (mode 3)

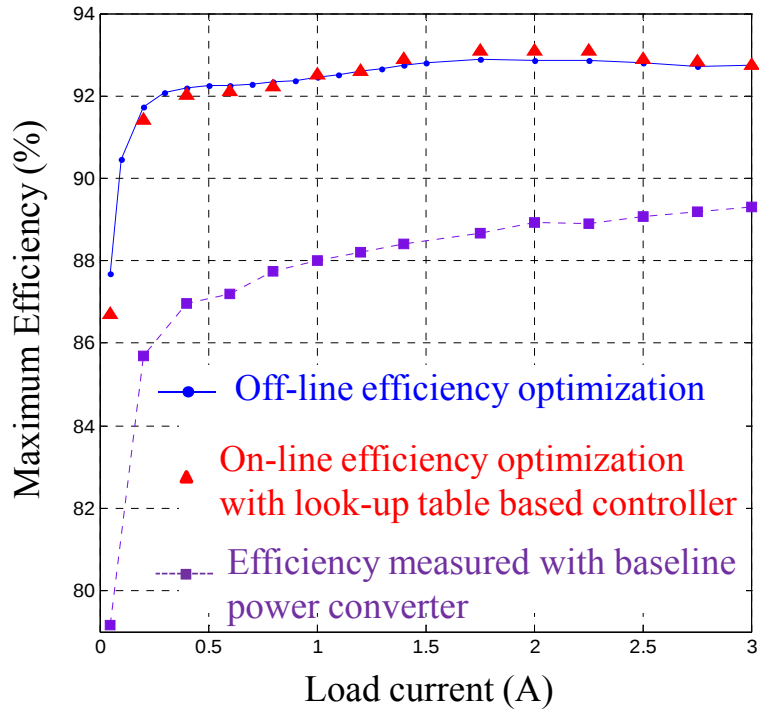


(d) Waveforms at point D (mode 4)

Fig. 5.7. Steady-state waveforms (switching-node voltage (V_{sw}) and control signal (c)) measured at points A – D in Fig. 5.5.



(a) $V_g = 140V$



(b) $V_g = 220V$

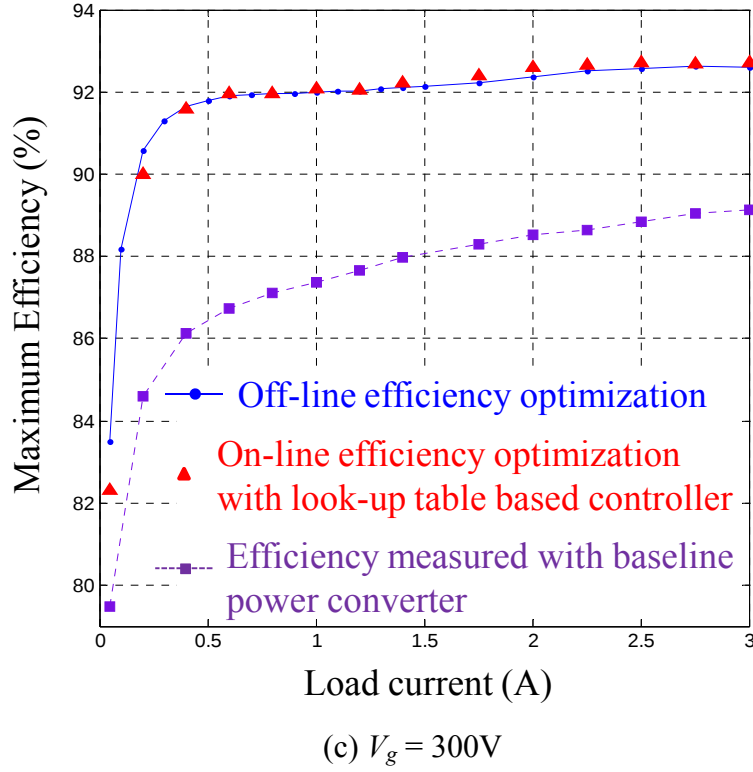


Fig. 5.8. Comparison of efficiency results at 3 different input voltages (140V, 220V and 300V).

5.2.5 Efficiency Improvements Analysis

So far, it is verified that the proposed on-line efficiency optimization approach based on the cost-constrained concurrent power stage/controller optimization and the look-up table based digital controller improves efficiency over wide ranges of operating conditions. In this section, the efficiency improvements are discussed with respect to contributions by the power stage and controller modifications, respectively.

For experimental verifications of efficiency improvements due to the power stage optimization, power stage design parameters of the baseline flyback prototype [30] are replaced by optimum design parameters (case 1 in Table 4.2), while the analog green-mode controller [5]

and other components are kept the same. Fig. 5.9 shows switching frequencies and operating modes measured with the modified flyback prototype over a range of load current (0.1A – 3A) at 3 different input voltages (130V, 200V and 300V). The green-mode controller enables different operating modes over a range of operating conditions. At light loads ($\leq 1W$), the converter operates in a burst mode where switching frequencies are pretty low and hysteretic bursts of pulses are generated during the switching periods to maintain a desirable output voltage level. In areas of analog green-mode controllers, the burst mode is usually adopted at light loads to decrease switching losses by forcing converters to operate at very low switching frequencies [41] – [44]. As the output power increases, the critical conduction mode (valley switching in DCM/CCM boundary) and quasi-resonant (QR) control (valley switching) below DCM/CCM boundary are employed at heavy loads and intermediate loads, respectively, which is very similar to the proposed look-up table based digital controller.

Fig. 5.10 presents comparisons between efficiency measured with the baseline and modified flyback prototypes. The power stage optimization results in significant efficiency improvements of more than 3% at intermediate and heavy loads and 6% at very light loads for all 3 input voltages.

Fig. 5.11 shows comparisons of each power loss in the baseline and modified flyback prototypes at 3 different loads with a constant input voltage (130V). The power loss models constructed for the efficiency characterization and optimization are used for the comparison. The five power losses are presented for the baseline design (blue) and the optimum power stage design (green): (1) conduction losses P_{cond} due to the transistor on-resistance, the output diode forward voltage drop, series resistance of the output diode, effective series resistances (ESRs) of input and output capacitors, and DC resistances of primary and secondary sides in the

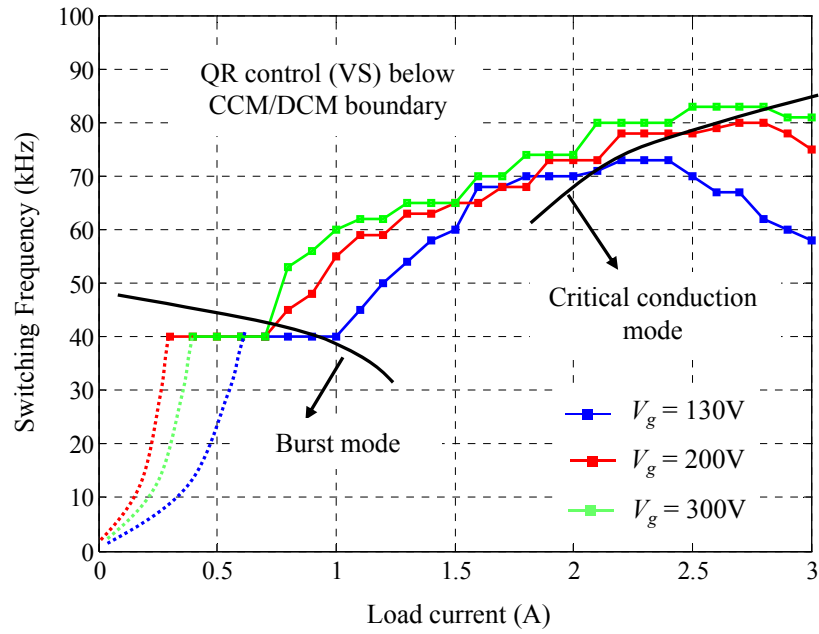


Fig. 5.9. Switching frequencies and operating modes of flyback prototype with optimum design parameters and analog green-mode controller [5] ($V_g = 130\text{V}$).

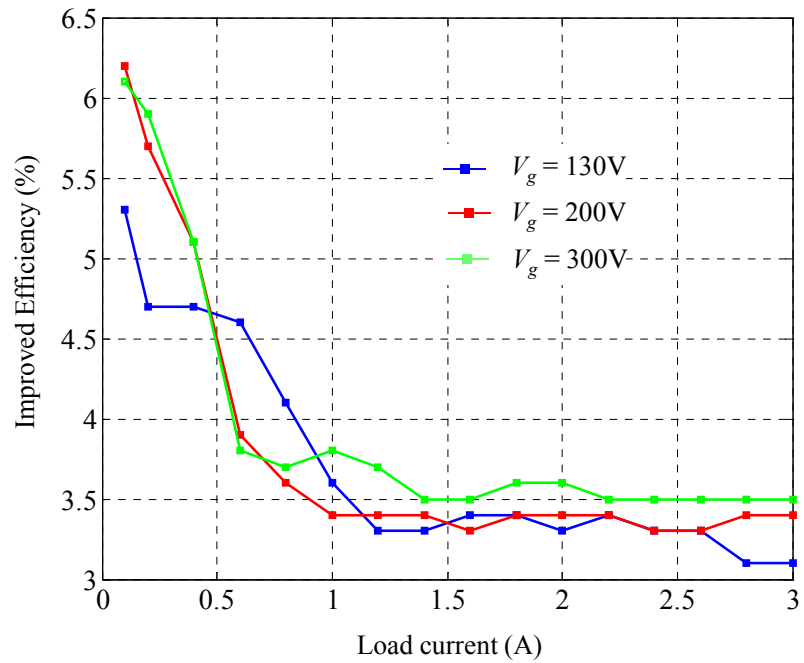
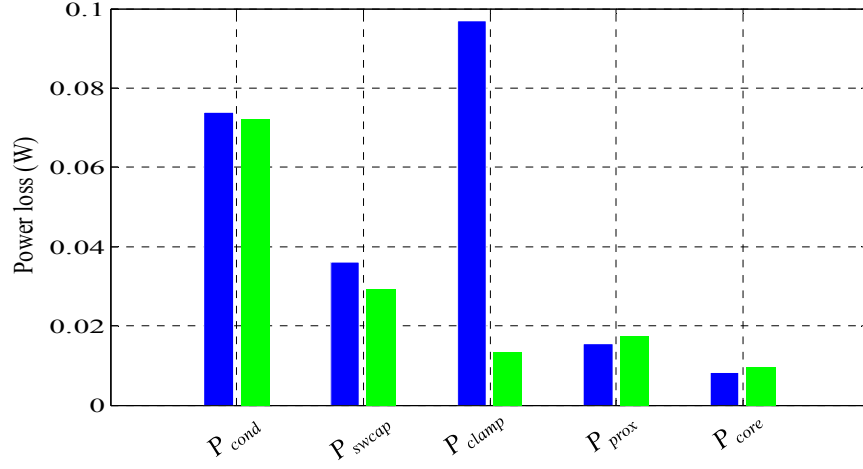
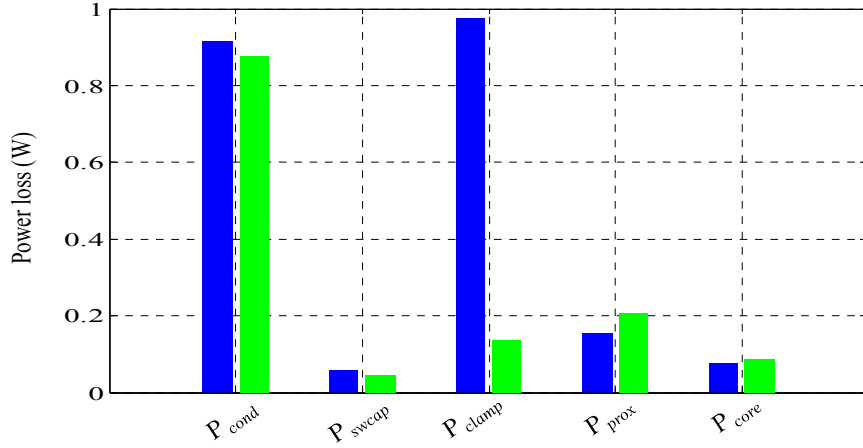


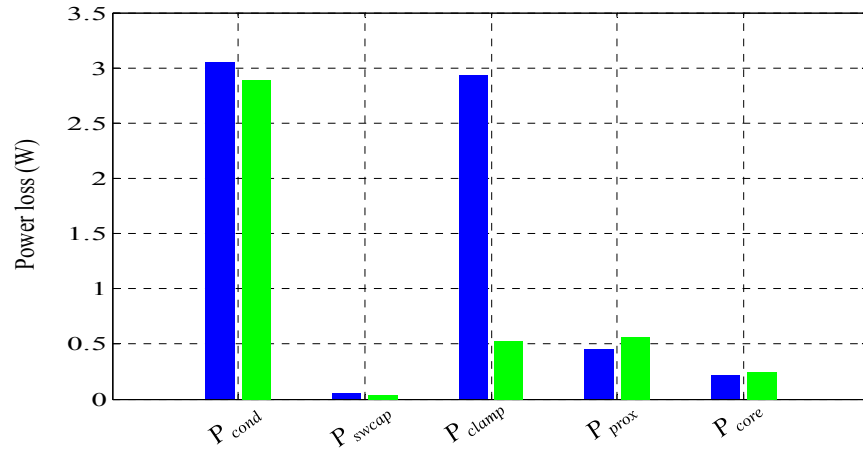
Fig. 5.10. Efficiency improved due to power stage optimization.



(a) Light load ($I_{out} = 0.1$ A)



(b) Intermediate load ($I_{out} = 1$ A)



(c) Heavy load ($I_{out} = 3$ A)

Fig. 5.11. Power losses comparisons at 130V over different loads (blue: baseline design, green: optimum power stage design).

transformer, (2) switching loss due to the switching-node capacitance P_{swcap} , (3) switching loss due to the leakage inductance P_{clamp} , (4) transformer proximity loss P_{prox} , and (5) transformer core loss P_{core} . It should be noted that power loss models for the burst-mode operation are not modeled, so the constant minimum switching frequency (20kHz) is assumed at light load ($I_{out} = 0.1A$).

As shown in Fig. 5.11, the switching loss due to the leakage inductance P_{clamp} is most significantly decreased over all different loads. The interleaved transformer reduces the leakage inductance by around half, and larger MOSFET voltage rating ($\sim 800V$) and clamped voltage V_{clamp} ($\sim 400V$) allow that the snubber does not affect the switching loss due to the leakage inductance ($V_{clamp} \rightarrow \infty$ in (3.9)):

$$P_{clamp} = \frac{1}{2} L_{lk} i_{Q,pk}^2 F_S \quad (5.1)$$

where L_{lk} is the leakage inductance and $i_{Q,pk}$ is the peak MOSFET drain current. Since the valley switching is adopted in DCM, the switching loss due to the switching-node capacitance P_{swcap} is relatively small compared to other losses, especially at intermediate and heavy loads, and is slightly reduced by lower switching-node capacitance. The conduction losses and core losses are kept almost the same, and the larger proximity losses are caused mainly by increased DC resistances in the transformer due to more windings in primary and secondary sides.

To examine contributions of the controller optimization to efficiency improvements, efficiency is experimentally measured for two cases and compared in Fig. 5.12: (case 1) the flyback prototype with the same analog green-mode controller and optimum power stage, and (case 2) the flyback prototype with the optimum power stage and proposed digital controller implemented for on-line efficiency optimization. In this comparison, it is assumed that a custom

digital controller chip implementing the proposed on-line efficiency optimization techniques would have the same or lower power consumption as the baseline analog green-mode controller.

Fig. 5.12 shows that efficiency can be improved over most of operating conditions, especially at 130V. Compared to the power stage parameter optimization, however, the proposed digital controller results in slight efficiency improvements because the switching frequencies and operating modes are very similar in both cases. At a certain operating point, efficiency is reduced because the valley switching points stored in the look-up table abruptly changes at boundaries where efficiency loss from the optimum is significant.

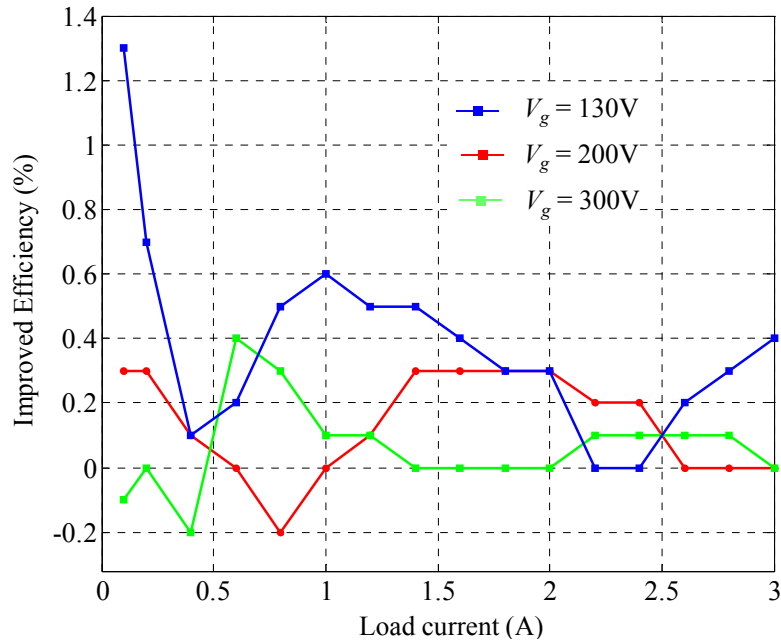
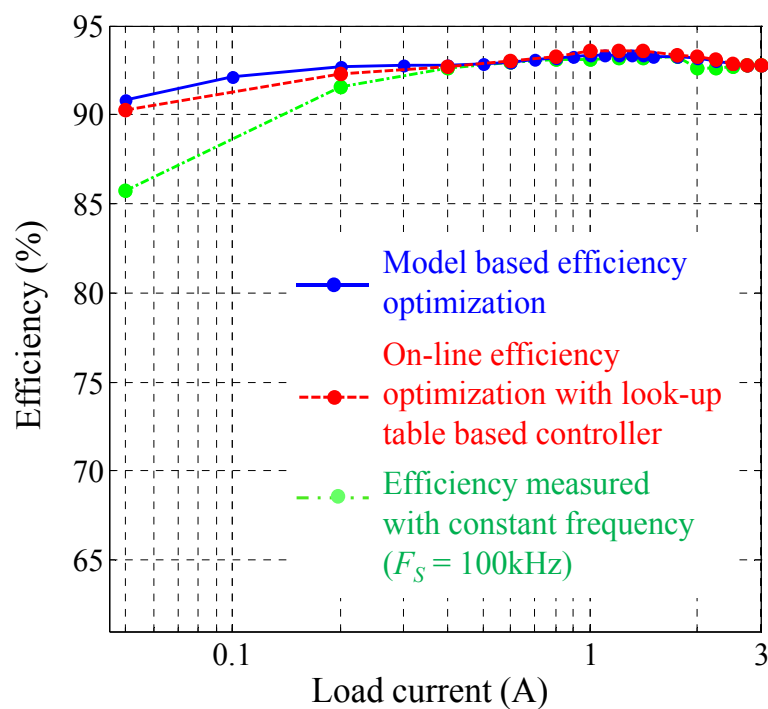


Fig. 5.12. Efficiency improved due to the look-up table based digital controller.

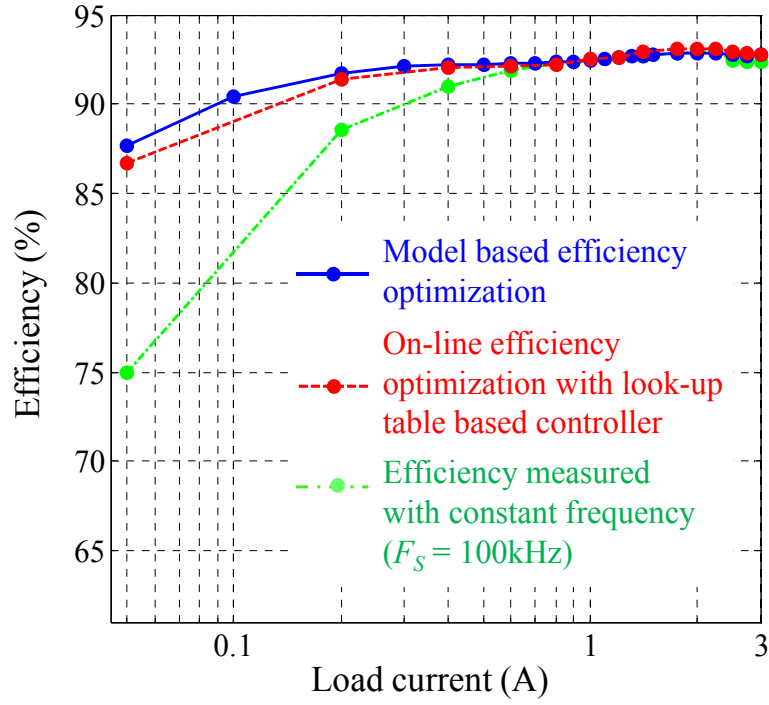
Efficiency measured with a constant switching frequency ($F_S = 100kHz$) and optimum power stage is presented in Fig. 5.13, together with results of cases 1 and 2 (model based optimization and on-line efficiency optimization with the look-up table based controller) shown

in Fig. 5.8. Comparisons of each efficiency result indicate how the proposed digital controller performs with the converter to achieve on-line efficiency optimization. Compared to the efficiency measured with the optimized prototype having fixed-frequency operation, the look-up table based controller improves efficiencies over all operating conditions, especially at very light loads.

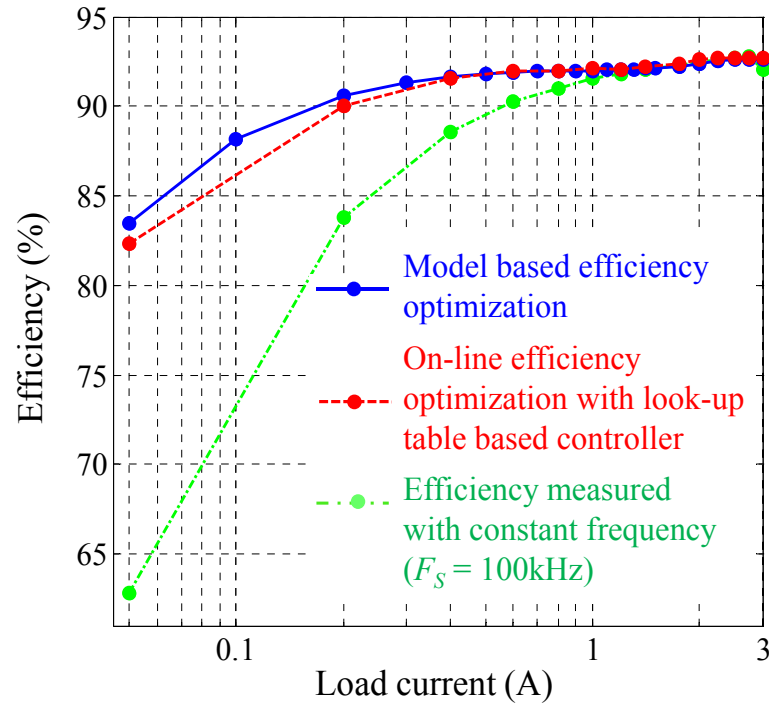
In conclusion, a significant portion of the loss reduction can be attributed to modifications in power stage based on the cost constrained optimization. The proposed look-up table based digital controller simply facilitates implementation of the concurrent power-stage/controller optimization approach.



(a) $V_g = 140\text{V}$



(b) $V_g = 220V$



(c) $V_g = 300V$

Fig. 5.13. Comparison of efficiency results at 3 different input voltages (140V, 220V and 300V).

5.3 Dynamic Operation of the Proposed Digital Controller

With a discrete-time compensator having fixed parameters (gain G_m , zeros Z_1 and Z_2), it is not possible to achieve the target cross-over frequency with adequate phase margin in the loop gain analysis. Instead, gain scheduling is applied, with compensator coefficient loaded from the look-up table depending on the operating conditions. An extension, named “ k -control”, is introduced to improve large-signal transient responses over mode boundaries, and to limit the peak current stress during transients. Small-signal modeling and analysis are presented to determine the gain-scheduled compensator and k -control parameters.

5.3.1 k -control scheme

As described in Section 5.2, the optimum valley switching points k_{opt} stored in the look-up table change abruptly with variations in the sensed input voltage and input current, which may affect large-signal transient responses. When a large step-up load transient is applied to the converter operating at light load and low switching frequency (in mode 1), the compensator increases T_{ON} significantly above the steady-state value, which may result in excessive transistor peak currents.

To improve large-signal transient responses, a simple extension, named the “ k -control”, is applied. The k -control allows for dynamic changes of the valley switching points during transients. Fig. 5.14 shows how the k -control scheme is implemented in the optimizer block. The k -control loop can be easily added to the main output voltage control loop with the same gain-scheduled compensator. An increment Δk in the number of the valley switching points k is introduced based on the scaled output voltage error ($e_v = V_{REF} - V_{out}$). $\Delta k = \alpha \cdot e_v$, where $\alpha < 0$. For example, consider again the case when a large step-up load transient is applied to the converter

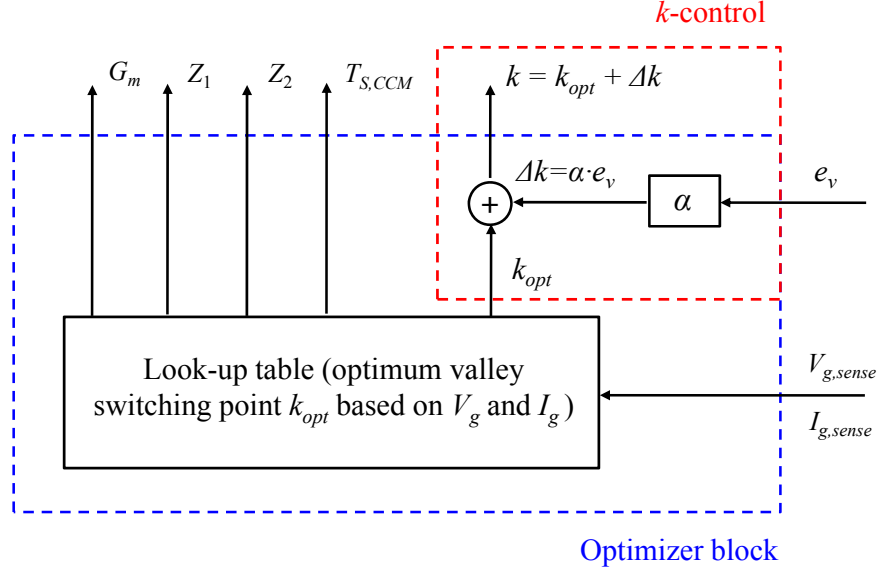


Fig. 5.14. k -control implementation in optimizer block.

operating at light load (in mode 1). As the output voltage drops and e_v increases, $\Delta k < 0$ is added to k_{opt} from the look-up table. As a result, k is reduced and the switching frequency increases, so that the compensator brings the voltage back to regulation faster and reduces T_{ON} and peak current overshoots. In steady state, when the error e_v is 0, $\Delta k = 0$, and $k = k_{opt}$ to achieve on-line efficiency optimization.

5.3.2 Small-Signal Modeling in DCM (Modes 1 – 3)

The averaged switch network derived in Chapter 2 is used for small-signal modeling and analysis in DCM. Since the output voltage is regulated through the switch on-time T_{ON} (instead of the duty cycle d) and the switching frequency is variable over different operating points, the effective resistor $R_e(d)$ should be modified as a function of the switch on-time T_{ON} and switching period T_S . By inserting $d = T_{ON}/T_S$ to (2.23), the effective resistor R_e is

$$R_e(T_{ON}, T_S) = \frac{2L_M T_S}{T_{ON}^2} \quad (5.2)$$

To include impacts of the k -control on the output voltage regulation in the small-signal model, the switching period T_S is described as a function of the switch on-time T_{ON} and the valley switching point k because the switching period depends on the valley switching points which varies in the presence of the output voltage error ($k = k_{opt} + \Delta k$ and $\Delta k = \alpha \cdot e_v$). Fig. 5.15 shows the magnetizing inductor current i_M over one switching period, with each valley switching point indicated.

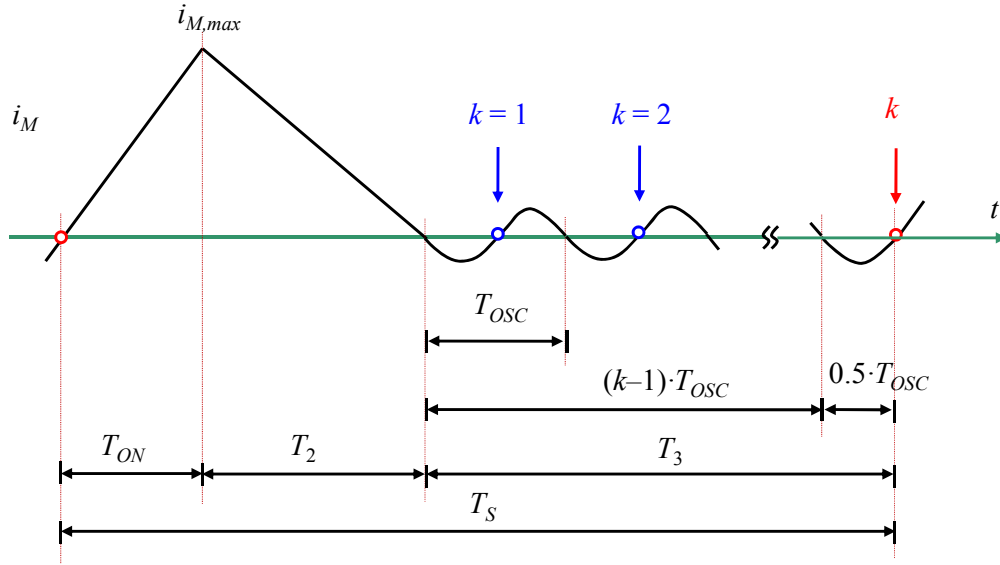


Fig. 5.15. Magnetizing current i_M with valley switching points to obtain switching period T_S as a function of switch on-time T_{ON} and valley switching point k .

From comparisons of the peak MOSFET and output diode currents, the diode conduction time interval T_2 is

$$T_2 = \frac{nv_g}{v_{out}} T_{ON} \quad (5.3)$$

As shown in Fig. 5.15, the switch Q turns on at the k^{th} valley switching point and the time interval T_3 (Q and D both off) is deduced as

$$T_3 = (k - 0.5) \cdot T_{OSC} \quad (5.4)$$

where T_{OSC} is the oscillation period. Therefore, the switching period T_S is

$$T_S = T_{ON} + T_2 + T_3 \quad (5.5)$$

$$T_S(T_{ON}, k) = T_{ON} \left(1 + \frac{nv_g}{v_{out}} \right) + (k - 0.5)T_{OSC} \quad (5.6)$$

From (5.2) and (5.6), the effective resistor R_e is modeled as

$$R_e(T_{ON}, k) = \frac{2L_M}{T_{ON}^2} \left\{ T_{ON} \left(1 + \frac{nv_g}{v_{out}} \right) + (k - 0.5) \cdot T_{OSC} \right\} \quad (5.7)$$

showing that the averaged switch network is controlled by the switch on-time T_{ON} and the valley switching point k (Fig. 5.16).

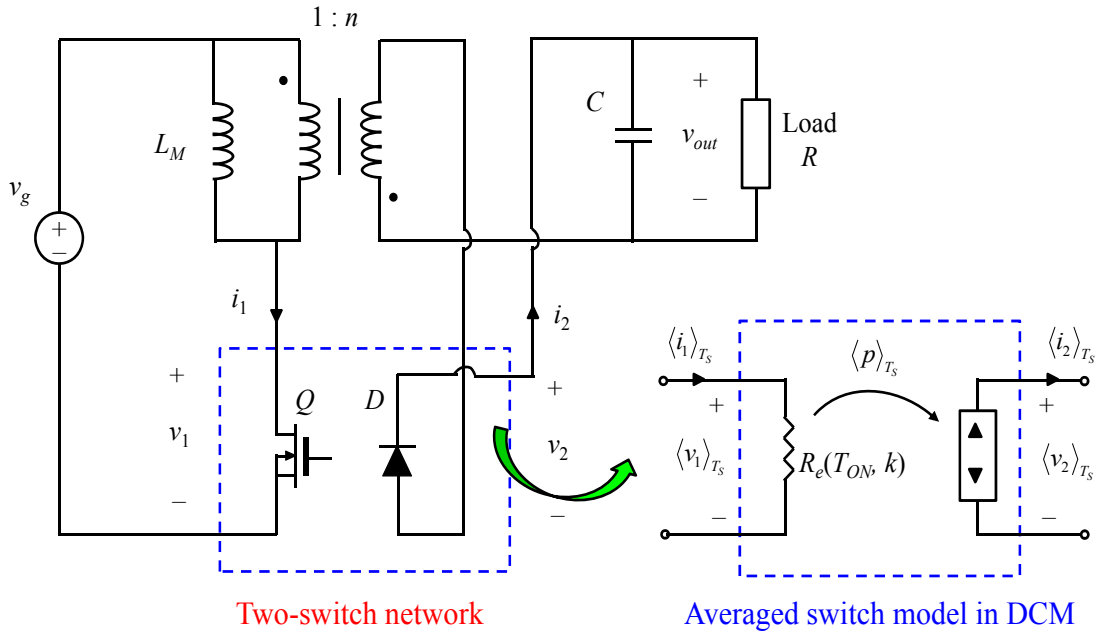


Fig. 5.16. Averaged switch network with modified effective resistor R_e as a function of the switch on-time T_{ON} and valley switching point k .

Overall block diagram of the control loops around the flyback converter with on-line efficiency optimization is presented in Fig. 5.17. These control loops can be divided into linear loops (output voltage regulation loop and k -control loop) and non-linear loops (loops to sense operating conditions). Under the assumption that the optimum valley switching point k_{opt} stored in the look-up table is constant like the reference voltage V_{REF} , the k -control loop can be considered as a linear loop because the output voltage error is multiplied by the k -control gain α .

Fig. 5.17. Overall block diagram of control loops in the flyback converter.

$$\langle i_1 \rangle_{T_s} = \frac{\langle v_1 \rangle_{T_s}}{R_o(T_{ON}, k)} = f_1(\langle v_1 \rangle_{T_s}, \langle v_2 \rangle_{T_s}, T_{ON}, k) \quad (5.8)$$

$$\langle i_2 \rangle_{T_s} = \frac{\langle v_1 \rangle_{T_s}^2}{R_e(T_{ON}, k) \langle v_2 \rangle_{T_s}} = f_2(\langle v_1 \rangle_{T_s}, \langle v_2 \rangle_{T_s}, T_{ON}, k) \quad (5.9)$$

As presented in [20], the input and output currents are perturbed around a quiescent operating point.

$$T_{ON} = T_{on} + \hat{t}_{on} \quad (5.10)$$

$$k = K + \hat{k} \quad (5.11)$$

$$\langle i_1 \rangle_{T_s} = I_1 + \hat{i}_1 \quad (5.12)$$

$$\langle i_2 \rangle_{T_s} = I_2 + \hat{i}_2 \quad (5.13)$$

$$\langle v_1 \rangle_{T_s} = V_1 + \hat{v}_1 \quad (5.14)$$

$$\langle v_2 \rangle_{T_s} = V_2 + \hat{v}_2 \quad (5.15)$$

where T_{on} is the quiescent value of the switch on-time, K is the quiescent value of the valley switching point k , etc. Small ac variations of each quantity are expressed as $\hat{t}_{on}$, $\hat{k}$, $\hat{i}_1$, $\hat{i}_2$, $\hat{v}_1$, and $\hat{v}_2$. Then, (5.8) and (5.9) are linearized to obtain small-signal ac model [20], resulting in

$$\hat{i}_1 = \hat{v}_1 \cdot \frac{1}{r_1} + \hat{v}_2 \cdot g_1 + \hat{t}_{on} \cdot j_1 + \hat{k} \cdot k_1 \quad (5.16)$$

$$\hat{i}_2 = \hat{v}_2 \cdot \left(-\frac{1}{r_2} \right) + \hat{v}_1 \cdot g_2 + \hat{t}_{on} \cdot j_2 + \hat{k} \cdot k_2 \quad (5.17)$$

where the higher-order nonlinear terms are discarded. The small-signal switch model parameters of the DCM flyback converter (r_1 , g_1 , j_1 etc.) are found by Taylor expansion, and shown in Table 5.2.

Table 5.2. Small-signal flyback DCM switch model parameters
(conversion ratio $M = V_{out}/V_g$)

Switch network input port		Switch network output port	
r_1	$R_e(T_{ON}, K) \frac{T_{ON}(1+n/M) + (K-0.5)T_{OSC}}{T_{ON} + (K-0.5)T_{OSC}}$	r_2	$M^2 R_e(T_{ON}, K) \frac{T_{ON}(1+n/M) + (K-0.5)T_{OSC}}{T_{ON} + (K-0.5)T_{OSC}}$
g_1	$\frac{1}{M^2 R_e(T_{ON}, K)} \frac{nT_{ON}}{T_{ON}(1+n/M) + (K-0.5)T_{OSC}}$	g_2	$\frac{2}{MR_e(T_{ON}, K)} \frac{T_{ON} + (K-0.5)T_{OSC} + nT_{ON}/2M}{T_{ON} + (K-0.5)T_{OSC} + nT_{ON}/M}$
j_1	$\frac{V_G}{T_{ON} R_e(T_{ON}, K)} \left\{ 1 + \frac{(K-0.5)T_{OSC}}{T_{ON}(1+n/M) + (K-0.5)T_{OSC}} \right\}$	j_2	$\frac{V_G}{T_{ON} M R_e(T_{ON}, K)} \left\{ 1 + \frac{(K-0.5)T_{OSC}}{T_{ON}(1+n/M) + (K-0.5)T_{OSC}} \right\}$
k_1	$-\frac{V_G}{R_e(T_{ON}, K)} \frac{T_{OSC}}{T_{ON}(1+n/M) + (K-0.5)T_{OSC}}$	k_2	$-\frac{V_G}{M R_e(T_{ON}, K)} \frac{T_{OSC}}{T_{ON}(1+n/M) + (K-0.5)T_{OSC}}$

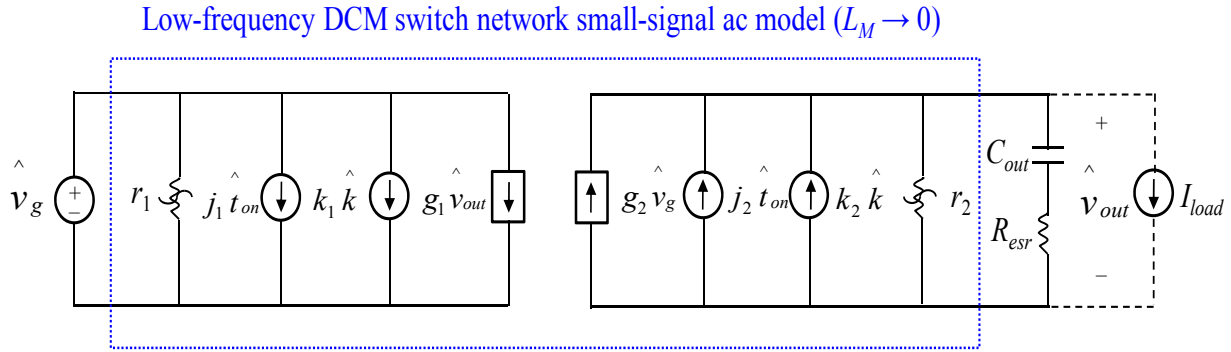


Fig. 5.18. Low-frequency small-signal ac model of the DCM flyback converter with the magnetizing inductance L_M shorted.

With the assumption that the high frequency dynamics due to the magnetizing inductance can be neglected ($L_M = 0$), the low-frequency small-signal ac model of the DCM flyback converter is obtained as Fig. 5.18. It should be noted that the output current I_{out} is

modeled as an ideal DC current source and not included in the model since the DC electronic load is set as a constant current mode in the experiments (Section 3.2).

Based on the small-signal model in Fig. 5.18, the continuous-time switch on-time to output voltage transfer function $G_{vton}(s)$ can be derived by letting $\hat{v}_g = 0$ and $\hat{k} = 0$:

$$G_{vton}(s) = j_2 \left\{ r_2 \parallel \left(\frac{1}{sC_{out}} + R_{esr} \right) \right\} \quad (5.18)$$

$$G_{vton}(s) = G_{o,vton} \frac{\left(1 + \frac{s}{2\pi f_{Z,vton}} \right)}{\left(1 + \frac{s}{2\pi f_{P,vton}} \right)} \quad (5.19)$$

with

$$G_{o,vton} = j_2 r_2 \quad (5.20)$$

$$f_{Z,vton} = \frac{1}{2\pi C_{out} R_{esr}} \quad (5.21)$$

$$f_{P,vton} = \frac{1}{2\pi C_{out} (r_2 + R_{esr})} \quad (5.22)$$

where R_{esr} is the equivalent series resistance (ESR) of the output capacitor.

In a similar way, $\hat{v}_g$ and $\hat{t}_{on}$ are set to zero and continuous-time valley switching point to output voltage transfer function $G_{vk}(s)$ is derived as

$$G_{vk}(s) = k_2 \left\{ r_2 \parallel \left(\frac{1}{sC_{out}} + R_{esr} \right) \right\} \quad (5.23)$$

$$G_{vk}(s) = G_{o,vk} \frac{\left(1 + \frac{s}{2\pi f_{Z,vk}} \right)}{\left(1 + \frac{s}{2\pi f_{P,vk}} \right)} \quad (5.24)$$

where

$$G_{o,kv} = k_2 r_2 \quad (5.25)$$

$$f_{Z,kv} = \frac{1}{2\pi C_{out} R_{esr}} \quad (5.26)$$

$$f_{P,vton} = \frac{1}{2\pi C_{out} (r_2 + R_{esr})} \quad (5.27)$$

A loop gain $T_v(s)$, which is the product of the gains around the forward and feedback paths of the control loop, is usually used to examine whether the control loop guarantees consistent transient responses over various operating conditions. Fig. 5.19 shows a complete block diagram of the small-signal model in output voltage regulation system with the assumption that the non-linear loops to sense operating conditions V_g and I_g can be neglected. From the model in Fig. 5.19, the loop gain $T_v(s)$ is obtained as

$$T_v(s) = H_v(s) \cdot \{G_c(s) \cdot G_{vton}(s) + \alpha(s) \cdot G_{vk}(s)\} \quad (5.28)$$

where $H_v(s)$ is scale-factor used for output voltage sensing, $G_c(s)$ is the gain-scheduled

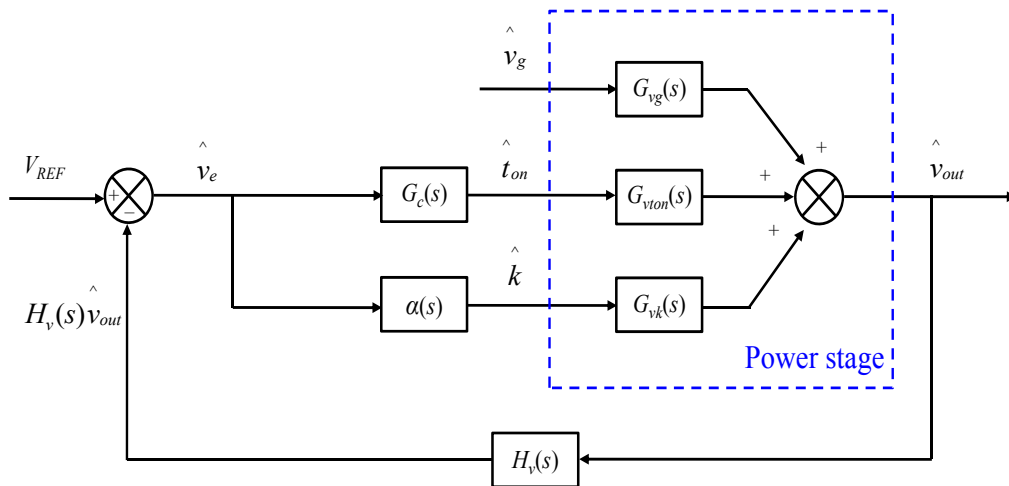


Fig. 5.19. Block diagram of the small-signal model of the DCM flyback converter with output voltage regulation.

compensator network and $\alpha(s)$ is the k -control gain. Note that the switch on-time regulation and k -control actions are added in the loop gain, resulting in the increased crossover frequency. Therefore, the k -control scheme is capable of improving dynamic responses.

5.3.3 Small-Signal Modeling in CCM (Mode 4)

In this section the small-signal equivalent circuit in CCM is modeled, including conduction losses due to the MOSFET on-resistance R_{on} and output diode forward voltage drop V_F . The same two-switch network shown in Fig. 2.7 is utilized. The switch network voltage and current waveforms are presented in Fig. 5.20, and features voltage drops due to the MOSFET on-resistance and output diode forward voltage drop in the switch network input and output voltages $\langle v_1 \rangle_{T_s}$ and $\langle v_2 \rangle_{T_s}$.

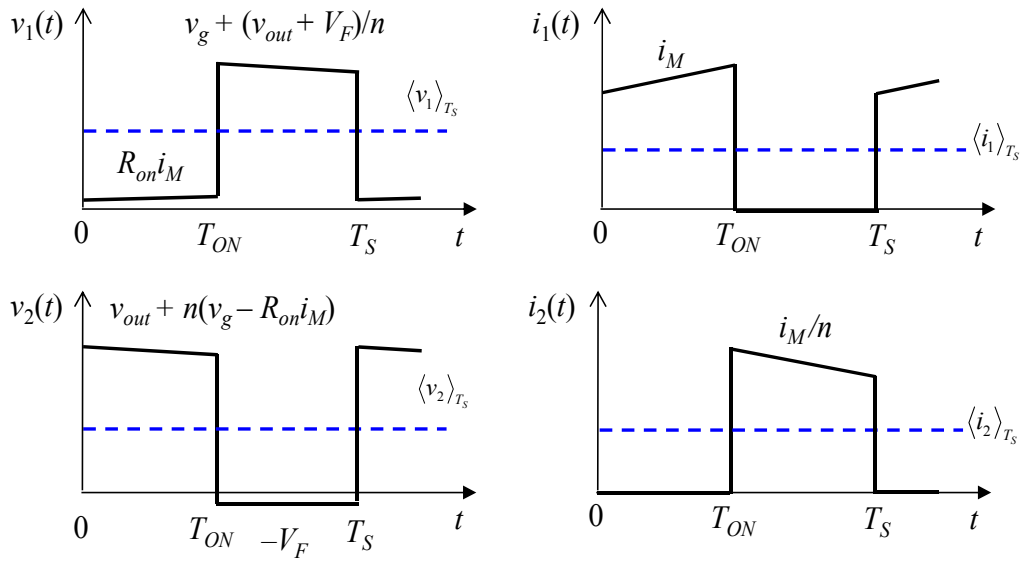


Fig. 5.20. Switch network voltage and current waveforms in CCM.

From analysis of the switch network waveforms,

$$\langle v_1 \rangle_{T_s} = \langle v_g \rangle_{T_s} - \langle v_L \rangle_{T_s} \quad (5.29)$$

$$\langle v_1 \rangle_{T_s} = \frac{T_{ON}}{T_s} R_{on} \langle i_M \rangle_{T_s} + \left(1 - \frac{T_{ON}}{T_s}\right) \cdot \left(\langle v_g \rangle_{T_s} + \frac{\langle v_{out} \rangle_{T_s} + V_F}{n} \right) \quad (5.30)$$

$$\langle v_2 \rangle_{T_s} = \frac{T_{ON}}{T_s} \left(\langle v_{out} \rangle_{T_s} + n \cdot \left(\langle v_g \rangle_{T_s} - R_{on} \langle i_M \rangle_{T_s} \right) \right) + \left(1 - \frac{T_{ON}}{T_s}\right) \cdot (-V_F) \quad (5.31)$$

$$\langle i_1 \rangle_{T_s} = \frac{T_{ON}}{T_s} \langle i_M \rangle_{T_s} \quad (5.32)$$

$$\langle i_2 \rangle_{T_s} = \left(1 - \frac{T_{ON}}{T_s}\right) \cdot \frac{\langle i_M \rangle_{T_s}}{n} \quad (5.33)$$

where v_L is the magnetizing inductance voltage and i_M is the magnetizing current. (5.30) and (5.31) yields a relationship that is

$$\langle v_g \rangle_{T_s} + \frac{\langle v_{out} \rangle_{T_s}}{n} = \langle v_1 \rangle_{T_s} + \frac{\langle v_2 \rangle_{T_s}}{n} \quad (5.34)$$

By substituting (5.34) and (5.32) into (5.30), the averaged switch network input voltage is derived as

$$\langle v_1 \rangle_{T_s} = \frac{T_s}{T_{ON}} R_{on} \langle i_1 \rangle_{T_s} + \left(\frac{T_s - T_{ON}}{n T_{ON}} \right) \cdot \left(\langle v_2 \rangle_{T_s} + V_F \right) \quad (5.35)$$

which contains conduction losses due to the MOSFET on-resistance in the input terminal and the output diode forward voltage drop in the output terminal. A relationship between the switch network input and output currents can be deduced from (5.32) and (5.33):

$$\langle i_2 \rangle_{T_s} = \left(\frac{T_s - T_{ON}}{n T_{ON}} \right) \cdot \langle i_1 \rangle_{T_s} \quad (5.36)$$

Fig. 5.21 shows the large-signal averaged switch-network of the flyback converter operating in CCM, which is modeled based on (5.35) and (5.36).

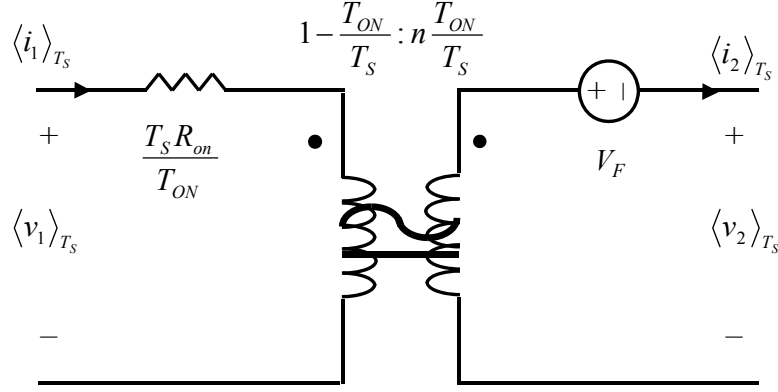


Fig. 5.21. Large-signal averaged switch network in CCM, including conduction losses due to the MOSFET on-resistance R_{on} and output diode forward voltage drop V_F .

For construction of a small-signal ac model, the large-signal model is perturbed and linearized in a similar manner to a DCM case, and the small signal ac descriptions corresponding to the magnetizing current are obtained as

$$L_M \frac{d\hat{i}_M}{dt} = \frac{T_{on}}{T_s} \hat{v}_g - \left(1 - \frac{T_{on}}{T_s}\right) \cdot \frac{\hat{v}_{out}}{n} + \left(V_G + \frac{V_{OUT} + V_F}{n} - I_M R_{on}\right) \cdot \frac{1}{T_s} \hat{t}_{on} - \frac{T_{ON}}{T_s} R_{on} \hat{i}_M \quad (5.37)$$

$$\hat{i}_2 = \left(1 - \frac{T_{on}}{T_s}\right) \cdot \frac{\hat{i}_M}{n} - \frac{I_M}{n T_s} \hat{t}_{on} \quad (5.38)$$

where I_M is the DC component of the magnetizing current.

The voltages around a loop in the switch-network input port and the currents around a loop in the switch-network output port are described in (5.37) and (5.38), respectively. Based on (5.37) and (5.38), the small-signal ac equivalent circuit of the CCM flyback converter is shown

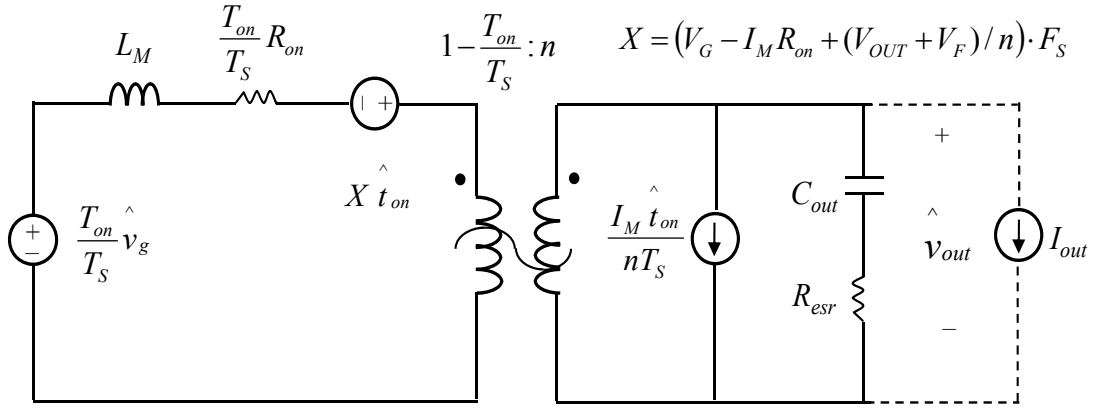


Fig. 5.22. Small-signal ac equivalent circuit of the CCM flyback converter, including conduction losses due to the MOSFET on-resistance R_{on} and output diode forward voltage drop V_F .

in Fig. 5.22. As in the DCM model, the load is modeled as an ideal DC current source and neglected in small-signal analysis.

By letting $\hat{v}_g = 0$ and using the principle of superposition related to $\hat{t}_{on}$, the continuous switch on-time to output voltage transfer function $G_{vton}(s)$ can be found:

$$G_{vton}(s) = G_{o,vton} \frac{\left(1 + \frac{s}{2\pi f_{LZ}}\right) \cdot \left(1 - \frac{s}{2\pi f_{RZ}}\right)}{1 + \frac{s}{Q \cdot (2\pi f_o)} + \left(\frac{s}{2\pi f_o}\right)^2} \quad (5.39)$$

with

$$G_{o,vton} = \frac{nV_G - (n + T_{on}/T_S)I_M R_{on} + V_{OUT} + V_F}{T_S - T_{on}} \quad (5.40)$$

$$f_{LZ} = \frac{1}{2\pi C_{out} R_{esr}} \quad (5.41)$$

$$f_{RZ} = \left(1 - \frac{T_{on}}{T_S}\right) \cdot \frac{nV_G - (n + T_{on}/T_S)I_M R_{on} + V_{OUT} + V_F}{2\pi n L_M I_M} \quad (5.42)$$

$$f_o = \frac{T_{on}}{2\pi n \sqrt{L_M C_{out}} \cdot T_S} \quad (5.43)$$

$$Q = \frac{nT_S}{T_{on}(R_{esr} + nR_{on} \cdot T_{on}/(T_S - T_{on}))} \sqrt{\frac{L_M}{C_{out}}} \quad (5.44)$$

For derivation of the loop gain $T_v(s)$, the k -control gain $\alpha(s)$ in Fig. 5.19 is set to zero because valley switching is not employed in CCM.

$$T_v(s) = H_v(s) \cdot G_c(s) \cdot G_{vton}(s) \quad (5.45)$$

5.3.4 Gain-Scheduled Compensator and k -Control Parameters Based On Small-Signal

Modeling and Analysis

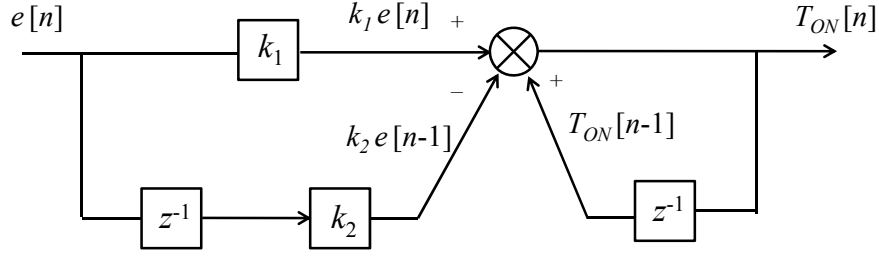
The look-up table based controller allows the converter to operate in DCM or in CCM. The gain-scheduled compensator and k -control parameters are selected based on small-signal modeling of the converter in both modes.

In the power stage, the output filter capacitance C_{out} is relatively large (same as in [30]), so that the target crossover frequency (f_c) is relatively low, around 1 kHz. Hence, high frequency dynamics in DCM are neglected. By using bilinear transformation and considering a delay due to the modulator and A/D converter, the continuous-time on-time to output voltage transfer function ($G(s)$) is transformed into discrete-time on-time to output voltage transfer function ($G(z)$). It should be noted that the sampling rate, which in the experimental prototype equals the switching frequency, varies across operating conditions. This is taken into account in the analysis of the loop gain magnitude and phase responses.

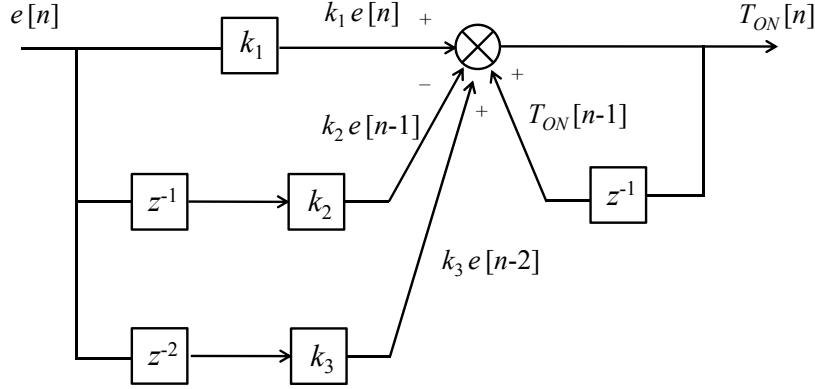
Table 5.3 summarizes the gain-scheduled compensator coefficients with compensator types over different operating modes. In DCM the PI compensator is employed with different parameters depending on operating conditions because the DCM flyback power stage is relatively simply modeled with a single pole at very low frequency due to the large output capacitance. On the other hand, complex poles and a right half-plane zero leads to significant phase lags in CCM, so the PID compensator is implemented for the CCM flyback converter to achieve adequate phase margin at the target crossover frequency. Fig. 5.23 shows block diagrams of the PI and PID compensators implemented in the digital controller.

Table 5.3. Gain-scheduled compensator parameters

Modes	Compensator types and parameters
$k_{opt} > 14$ (mode 1, DCM)	PI compensator $G_m \left(\frac{z - Z_1}{z - 1} \right)$ $G_m = 20.12 \times 10^{-5}, Z_1 = 0.994$
$1 \leq k_{opt} \leq 14$ (modes 2 and 3, DCM)	PI compensator $G_m \left(\frac{z - Z_1}{z - 1} \right)$ $G_m = 10.03 \times 10^{-5}, Z_1 = 0.9968$
$k_{opt} = 0$	PID compensator $G_m \frac{(z - Z_1)(z - Z_2)}{z(z - 1)}$ $G_m = 36.2 \times 10^{-5}, Z_1 = 0.9614, Z_2 = 0.9753$



(a) PI compensator block for DCM ($k_1 = G_m$, $k_2 = Z_1 \cdot G_m$)



(b) PID compensator block for CCM ($k_1 = G_m$, $k_2 = Z_1 + Z_2$, $k_3 = Z_1 \cdot Z_2$)

Fig. 5.23. Gain-scheduled compensator block diagrams.

In k -control scheme, the fixed k -control gain α is set as -1000 , which was found to result in well-behaved transient responses. When the converter operates at intermediate or heavy loads and the same gain-scheduled compensator (Table 5.3) is employed without k -control, it is difficult to achieve the target cross-over frequency due to very low loop-gain magnitude in high frequency ranges, as shown in Fig. 5.24. The k -control enables to increase magnitude of the loop gain, such that the cross-over frequency can be settled around 1 kHz, together with adequate phase margin ($\sim 70^\circ$).

Fig. 5.25 shows the loop gain magnitude and phase plots for 3 operating points. Over all operating point corners, the gain-scheduling and k -control approaches result in relatively consistent small-signal dynamic responses – the crossover frequency around 1 kHz and the phase margin more than 70° .

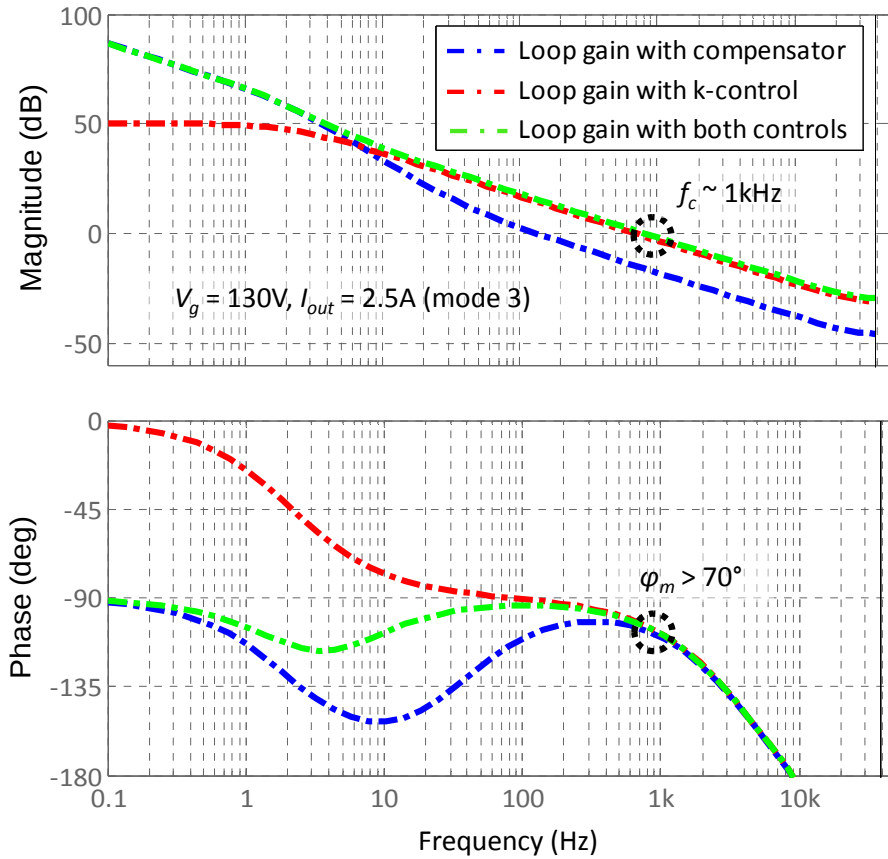


Fig. 5.24. Loop gain magnitude and phase responses in mode 3 ($V_g = 130\text{V}$ and $I_{out} = 2.5\text{A}$) for 3 cases: (case 1) the gain-scheduled compensator shown in Table 5.3 is employed without k -control, (case 2) k -control ($\alpha = -1000$) is employed without the compensator, and (case 3) both the compensator and k -control are employed.

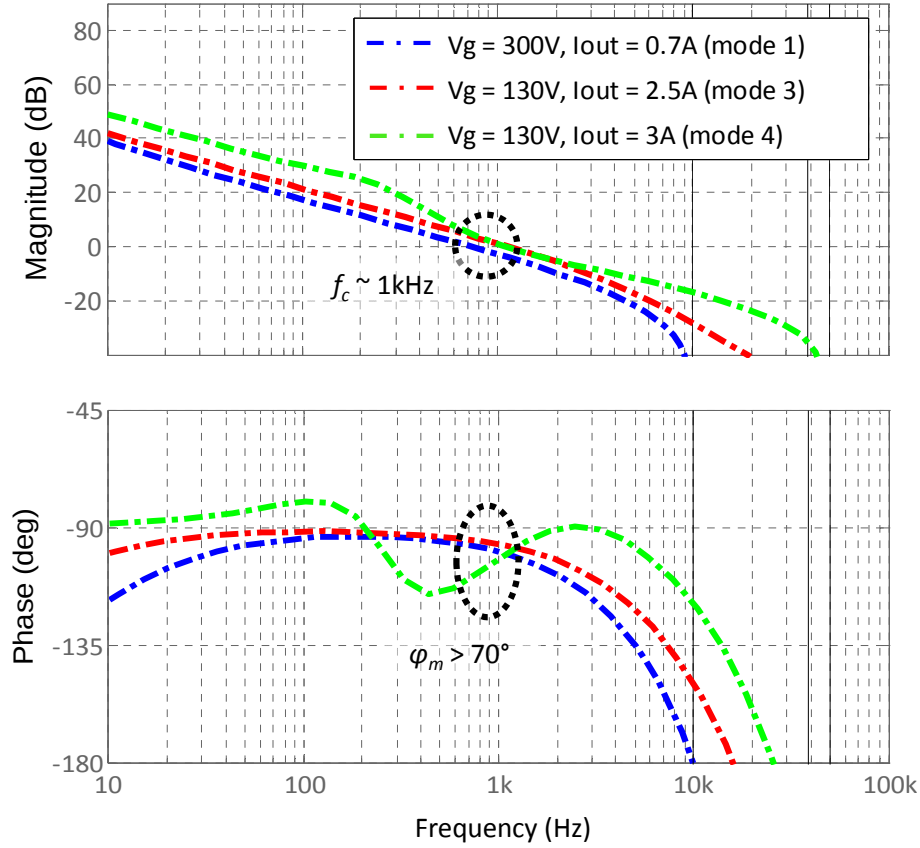


Fig. 5.25. Example of loop gain magnitude and phase responses at three operating conditions corresponding to different compensator parameters presented in Table 5.3 and fixed k -control gain ($\alpha = -1000$).

5.3.5 Simulation and Experimental Results

The k -control scheme ($\alpha = -1000$) and gain-scheduled compensator with parameters selected based on loop gain analysis are programmed in the digital controller. The A/D resolution of the output voltage error e_v is 2mV. The k -control increment Δk is set to zero if the output voltage error e_v is between $-4mV$ and $4mV$.

Simulation results of large-signal transient responses over different modes are presented in Fig. 5.26 (0.1A-to-2.5A step load transient) and Fig. 5.27 (2.5A-to-0.1A step load transient),

verifying that the valley switching points k change dynamically during the transients because the k -control increment Δk is not zero in presence of the output voltage error e_v ($\Delta k = \alpha \cdot e_v$ and $\alpha = -1000$) and added to the optimum valley switching points k_{opt} stored in the look-up table ($k = k_{opt} + \Delta k$). Note that the valley switching points k start equal to the optimum valley switching points k_{opt} and returns to k_{opt} after the transient, enabling on-line efficiency optimization. As shown in the simulation results, the k -control does not degrade operation of the main output voltage control loop to regulate on-time T_{ON} .

Experimental results (output voltage V_{out} and MOSFET drain current I_Q) are shown in Fig. 5.28, well matched with the simulation results – output voltage deviations during the transients are around 400mV, and times to return to steady states are around 4ms and 30ms in 0.1A-to-2.5A and 2.5A-to-0.1A step load transients, respectively.

Fig. 5.29 presents 0.1A-to-2.5A step load transient responses in a case when the converter only employs the gain-scheduled compensator shown in Table V without k -control ($\alpha = 0$). Comparisons between Fig. 5.28 and Fig. 5.29 show that the k -control results in lower output voltage undershoot and faster dynamic responses, together with decreased peak switch current overshoot.

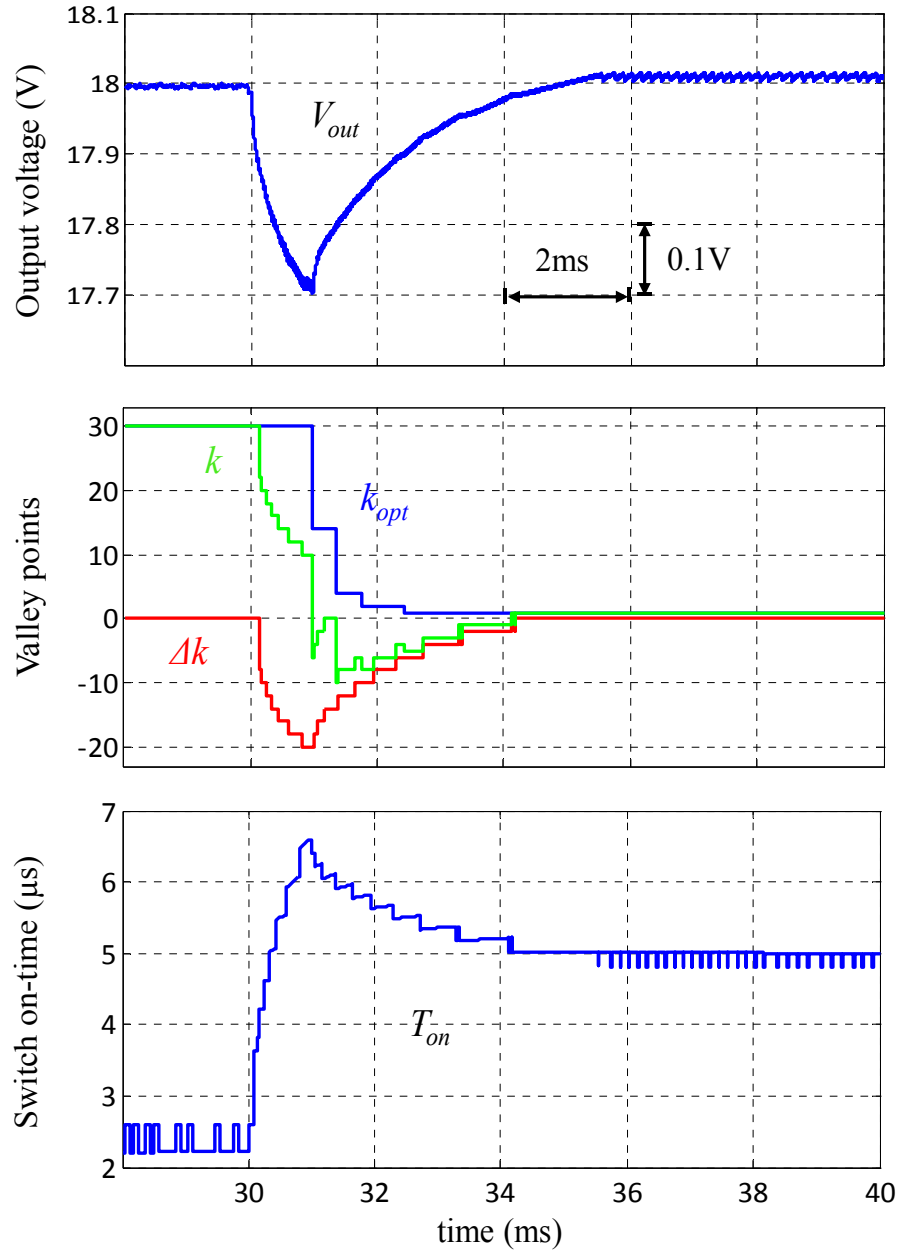


Fig. 5.26. Simulation results for a 0.1A to 2.5A step load transient at 130V (output voltage V_{out} , optimum valley switching points k_{opt} , k -control increment Δk , valley switching points k , and switch on-time T_{ON}).

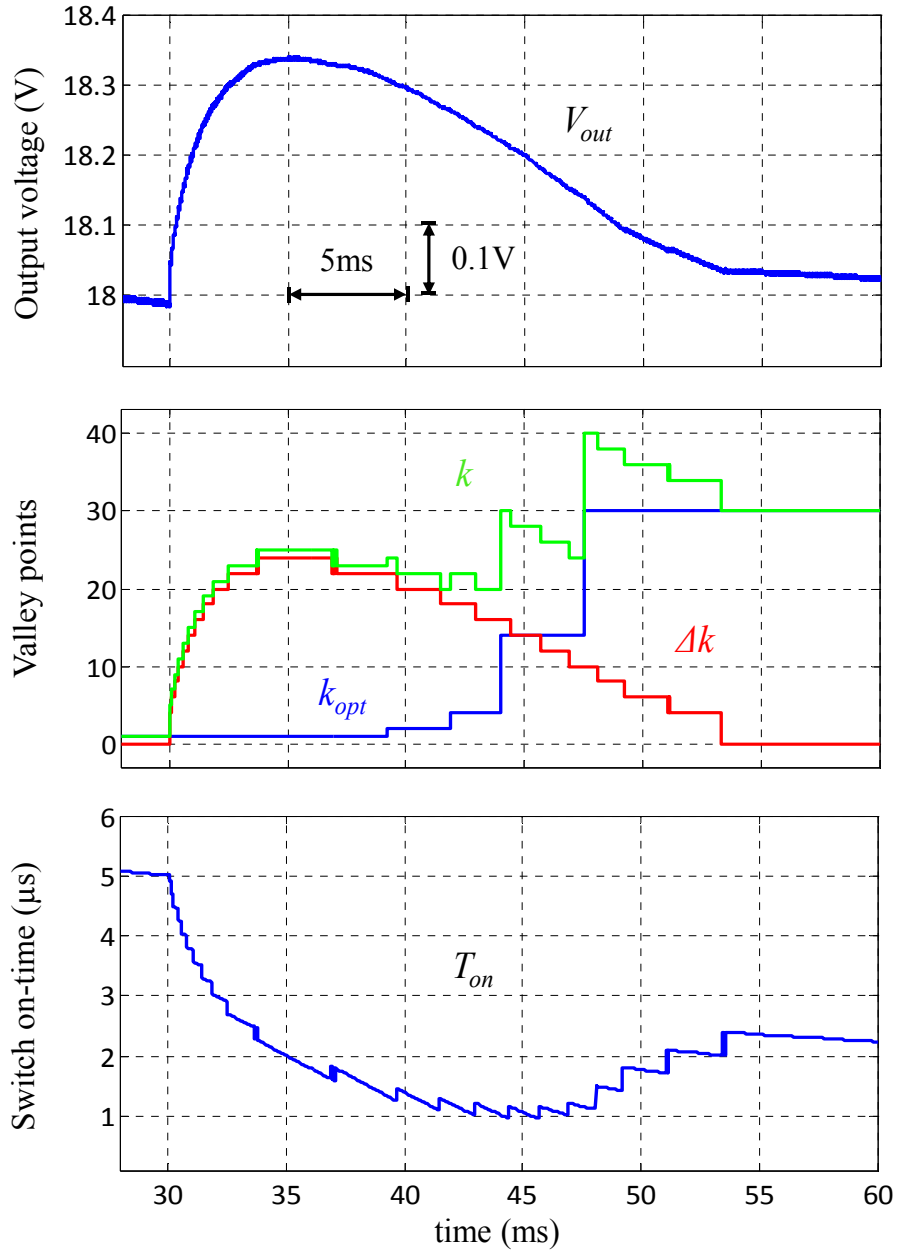
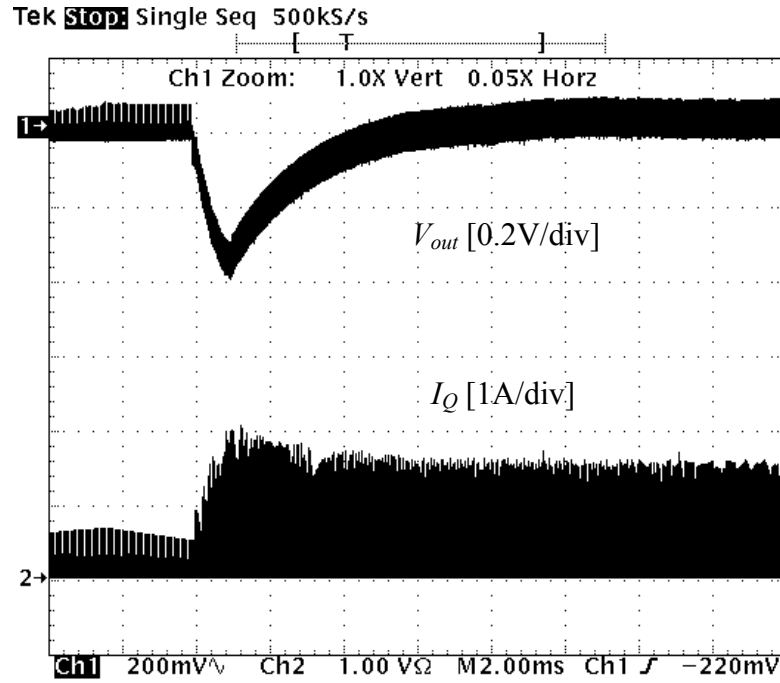
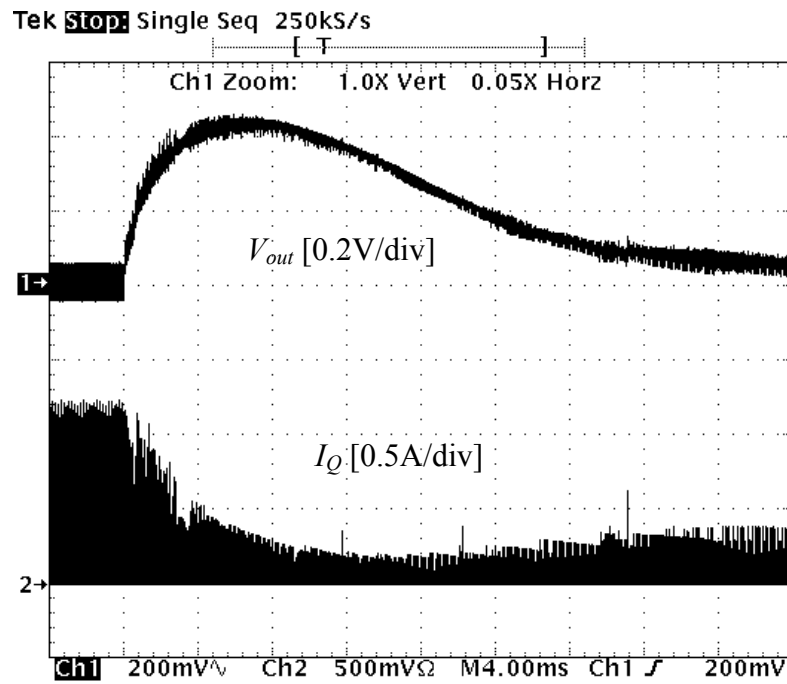


Fig. 5.27. Simulation results for a 2.5A to 0.1A step load transient at 130V (output voltage V_{out} , optimum valley switching points k_{opt} , k -control increment Δk , valley switching points k , and switch on-time T_{ON}).

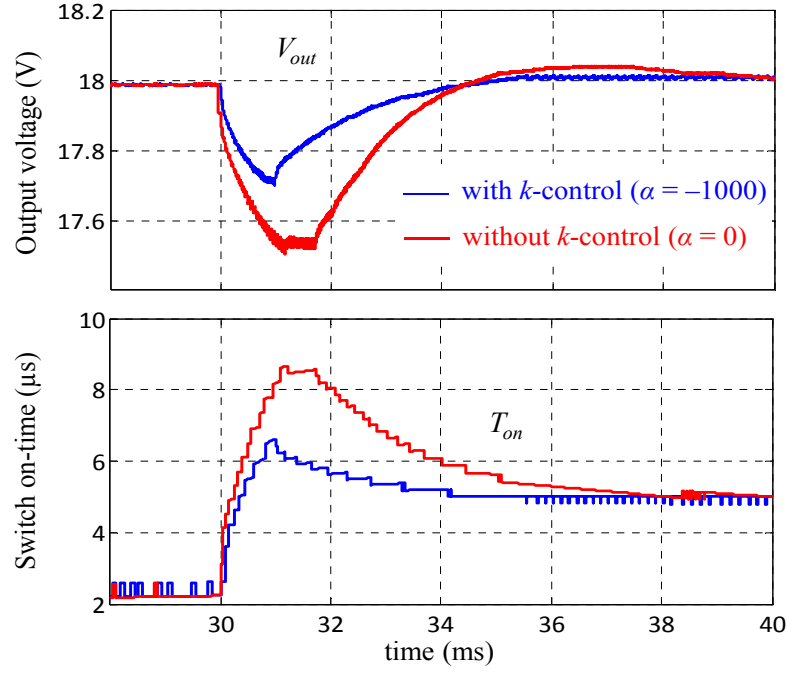


(a) 0.1A to 2.5A step load transient

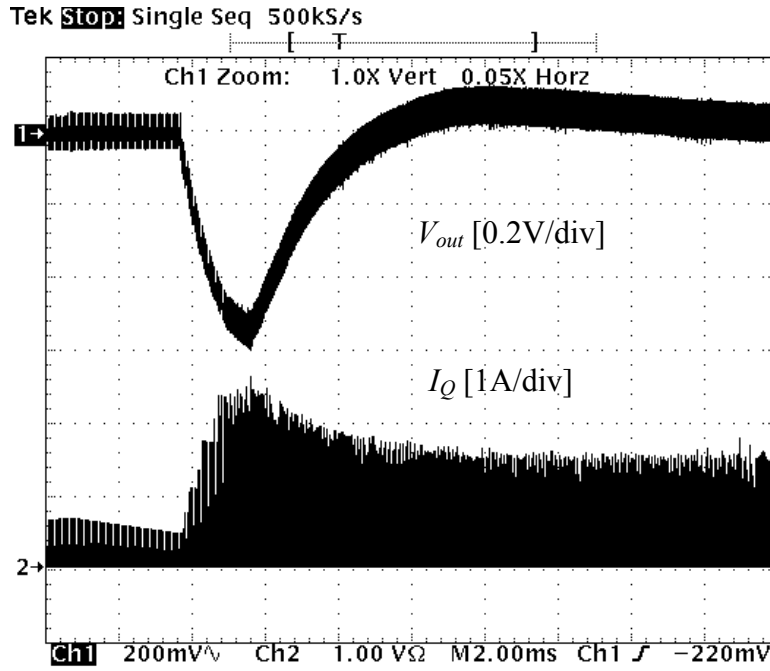


(b) 2.5A to 0.1A step load transient

Fig. 5.28. Experimental results for large step load transients at 130V (output voltage V_{out} and MOSFET drain current I_Q).



(a) Simulation results (V_{out} , T_{on}) with different k -control gains ($\alpha = 0$ (red) and $\alpha = -1000$ (blue))



(b) Experimental results (V_{out} and I_Q) without k -control ($\alpha = 0$)

Fig. 5.29. Simulation and experimental results for a 0.1A-to-2.5A step load transient at 130V in a case when the gain-scheduled compensator is employed without k -control ($\alpha = 0$).

5.4 Conclusions

This chapter describes a simple look-up table based digital controller to achieve on-line efficiency optimization over very wide ranges of operating conditions. Compared to other on-line optimization techniques, the approach is simpler and less susceptible to disturbances during converter operation including transients. Programmability of the look-up table implies that the same controller could be applied to different power stages. Undesirable frequency hopping mechanisms, commonly observed in valley switching control schemes, are resolved by storing optimum valley switching points in the look-up table and by using hysteresis bands in the look-up table boundaries. A gain-scheduled compensator is implemented based on small-signal modeling and analysis. A simple extension, named k -control, is proposed to improve large-signal transient responses and reduce peak MOSFET drain current during transients. Experimental results show that the controller achieves smooth mode transitions and consistent transient responses over different operating modes, and that efficiency exceeds 92% at all operating points over approximately 3:1 range of input voltages and 10:1 range of loads, with 3 – 8% efficiency improvements compared to a baseline reference design. Analysis of efficiency improvements implies that most of efficiency improvements are contributed by power stage optimization, and that the proposed digital controller enables simple implementation of the efficiency optimization.

Chapter 6

Simplified Sensing and A/D Conversion for Digitally Controlled Flyback DC-DC Converters with On-Line Efficiency Optimization

In Chapter 5, a digital control approach has been proposed to achieve on-line efficiency optimization in flyback DC-DC converters, by using a relatively simple look-up table which stores optimum controller parameters over different operating conditions. The approach is experimentally verified with a conventional 65W flyback DC-DC prototype (Chapter 5 and [45]). However, in this digital control scheme, sensing and analog-to-digital (A/D) conversion of input voltage V_g and input current I_g are required to detect operating conditions. In addition, the output voltage V_{out} is sensed and regulated conventionally, requiring additional secondary-side circuitry and an opto-coupler or other forms of isolation in the feedback path.

In flyback DC-DC applications, an auxiliary winding voltage V_{aux} and MOSFET drain current I_Q are usually sensed to employ valley switching and to protect the converter from overload conditions, respectively. By re-using V_{aux} and I_Q , this chapter proposes techniques to eliminate complicated A/D converters and the need for isolation in the feedback path. The work presented in this chapter builds upon similar simplified A/D conversion approaches [46] – [50],

and voltage regulation approaches based on primary-side sensing [51] – [60], and is targeting a low-cost, small-size, low-pin-count (≤ 8) digital controller IC chip implementation.

Section 6.1 describes feasible architecture of the digital controller IC chip based on the controller proposed for on-line efficiency optimization in Chapter 5 and additional circuitry to protect the converter from undesirable cases such as overload or overvoltage in the output stage. Section 6.2 addresses simplified sensing and A/D conversion techniques to regulate the output voltage and estimate input current and input voltage, by sensing the auxiliary winding voltage V_{aux} and MOSFET drain current I_Q . Section 6.3 presents details of how output voltage regulation is implemented on the primary side, together with input voltage and current estimations, while Section 6.4 shows experimental results. This chapter is concluded in Section 6.5.

6.1 Digital Controller IC Chip Architecture Based On Control Approach Proposed For On-Line Efficiency Optimization

Fig. 6.1 shows a practically feasible architecture of the digital controller IC chip based on the controller implementation described in Chapter 5. Two A/D converters are used in the controller – one is for output voltage regulation through directly sensed output voltage (pin 7, FB), and the other is to detect operating points input voltage V_g and input current I_g , which are sensed through pin 3 (OPPT_VG) and pin 4 (OPPT_IG), respectively, and are fed to the A/D converter through a digital multiplexer controlled by a clock signal produced in a clock generator. The specifications of each A/D converter are presented in Table 6.1.

The operating points detector, named OPPT detector in Fig. 6.1, updates the operating points V_g and I_g to the efficiency optimizer such that the look-up table provides optimum controller parameters (optimum switching period $T_{s,CCM}$ in CCM and valley switching point k)

and compensator parameters (G_m , Z_1 , and Z_2) to the modulator and the compensator, respectively, over different operating conditions. The switching-node voltage is sensed through the auxiliary winding (pin 8, QR_DETECT), so the modulator forces valley switching through the DCM comparator output signal (S_{DCM}) when the converter operates in DCM. The current and voltage monitor (CV monitor) enables actions to protect the converter from (1) overshoot of the MOSFET drain current and (2) overload responses by using the sensed MOSFET drain current I_Q (pin 2, CS), and (3) overvoltage in the output stage through the sensed auxiliary winding voltage V_{aux} (pin 8, QR_DETECT). The eight input and output (I/O) pins are assigned, and functions of the pins are summarized in Table 6.2.

Table 6.1. Specifications of A/D converters used for implementation of digital controller IC chip with on-line efficiency optimization

A/D converter for V_{out} regulation	A/D converter for V_g and I_g detection
• Voltage deviation = $\pm 0.4V$ • Output voltage resolution: 30mV • $0.8V/30mV = 27$ slots needed • A/D converter bits $n_{FB} = 5$ • Sampling rate equals switching frequency ($F_{s,max} \sim 140$ kHz)	• V_g slots in the look-up table = 9 (300V-130V)/20V • I_g slots in the look-up table = 15 0.45A/30mA • A/D converter bits $n_{oppt} = 4$ • Sampling rate equals switching frequency ($F_{s,max} \sim 140$ kHz)

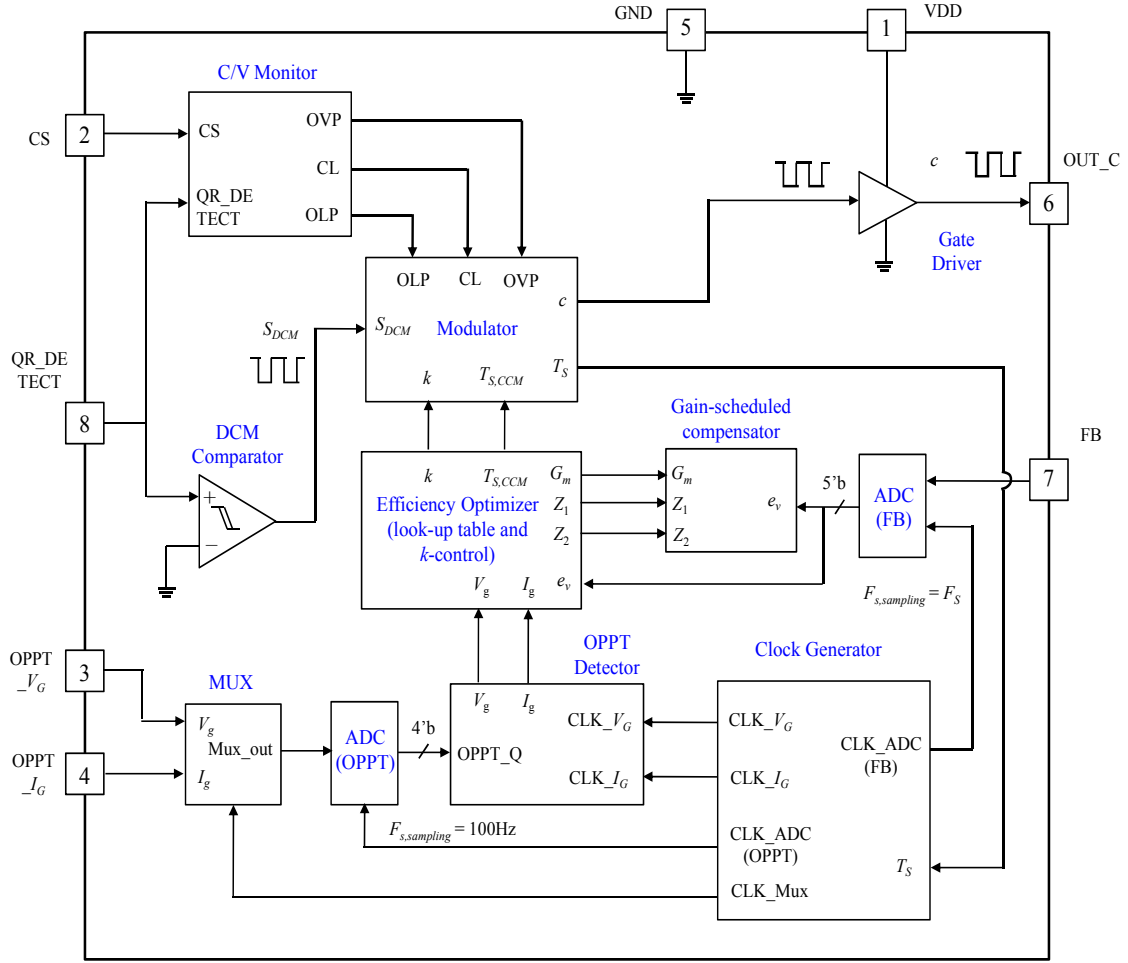


Fig. 6.1. Architecture of the digital controller IC chip for on-line efficiency optimization.

Table 6.2. I/O pins assignment and description (digital controller with direct sensing and A/D conversion)

Name	No.	I/O	Description
VDD	1	I	Provides power to the controller
CS	2	I	1. Senses MOSFET drain current I_Q 2. Limits the peak MOSFET drain current $i_{Q,peak}$ 3. Protects the converter from overload responses
OPPT_VG	3	I	Senses input voltage V_g
OPPT_IG	4	I	Senses input current I_g
GND	5	–	Ground for the controller
OUT_C	6	O	Gate driving signal c
FB	7	I	Senses feedback voltage for on-time regulation and k -control
QR_DECTECT	8	I	1. Senses auxiliary winding voltage V_{aux} 2. Detects valley switching points k 3. Protects the converter from overvoltage on the load

The flyback DC-DC converter with the digital controller IC chip is shown in Fig. 6.2. The controller chip is powered from voltage generated by the auxiliary winding voltage and additional circuitry (H_{vdd}). Because the output voltage is directly sensed and regulated in a conventional flyback DC-DC converter, an opto-coupler and additional secondary-side circuitry are usually employed for isolation between the input and output stages, which increases cost, size and number of I/O pins.

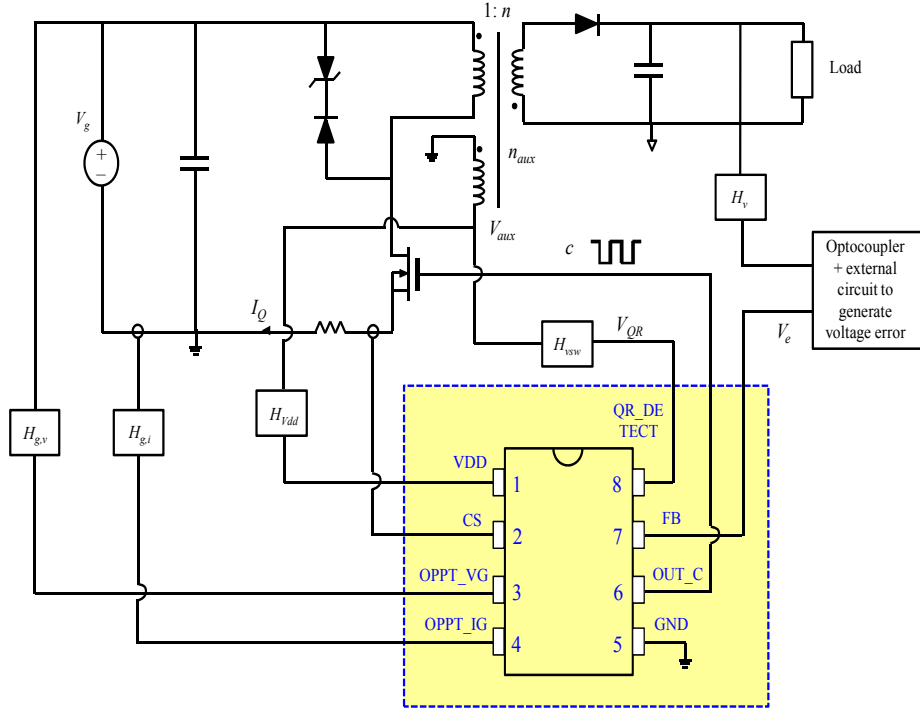


Fig. 6.2. Flyback DC-DC converter with the digital controller IC chip shown in Fig. 6.1 and additional circuitry for isolation in the feedback path.

6.2 Simplified Sensing and A/D Conversion Techniques

In flyback DC-DC converters, an auxiliary winding voltage V_{aux} and MOSFET drain current I_Q are usually sensed to employ valley switching and to protect the converters from overload conditions, respectively, as shown in Fig. 6.2. This section proposes approaches to eliminate complicated A/D converters and the need for isolation in the feedback path, by re-using the auxiliary winding voltage and MOSFET drain current. The work presented in this section is targeting a low-cost, small-size, low-pin-count (≤ 8) digital controller IC chip implementation. Fig. 6.3 shows a block diagram of the digital controller with proposed sensing and A/D conversion techniques around a conventional flyback DC-DC converter. The optimum

controller parameters obtained from an efficiency optimization approach for conventional flyback DC-DC converters and compensator gains are stored in the look-up table (efficiency optimizer block) over different operating points V_g and I_g which are estimated by sensing V_{aux} and I_Q , respectively. The switch on-time T_{ON} is adjusted to regulate V_{out} based on the sensed auxiliary winding voltage. With an assumption that the controller is implemented in a single IC chip, 5 input and output pins can be assigned, as shown in Fig. 6.3.

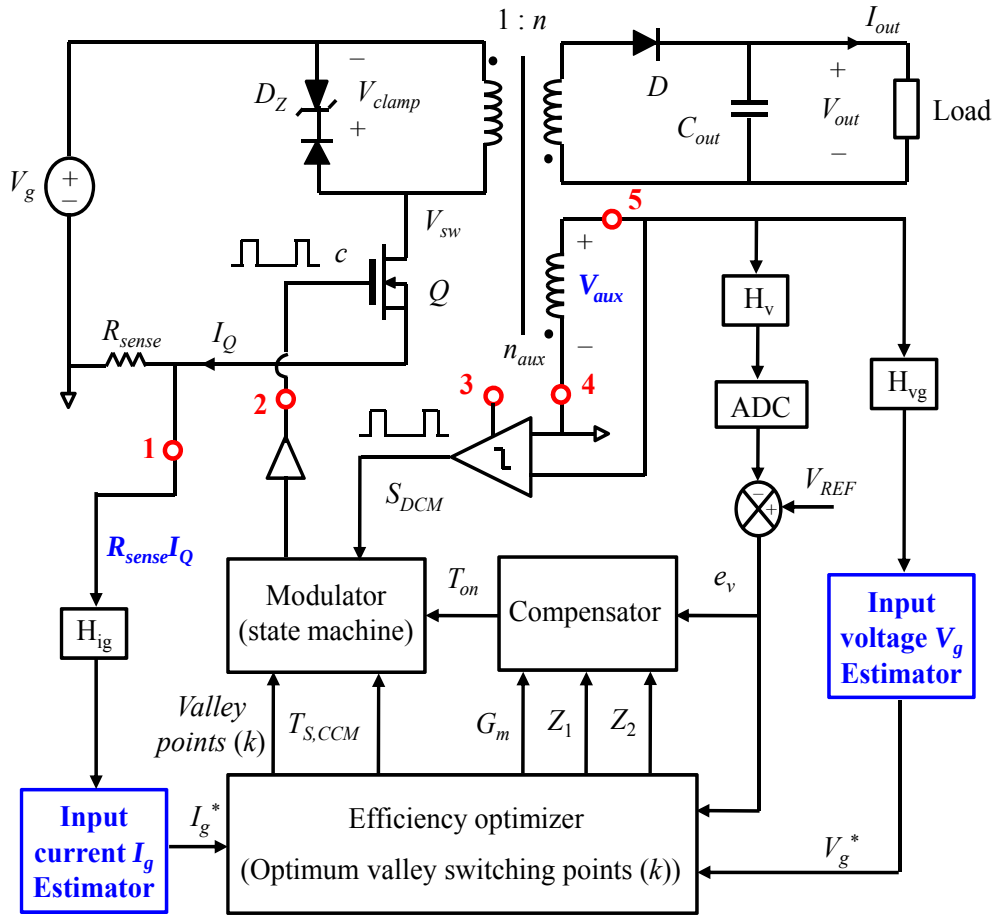


Fig. 6.3. A conventional flyback DC-DC converter with a block diagram of the digital controller with simplified sensing and A/D conversion. Detection of operating points and output voltage regulation are achieved by sensing auxiliary winding voltage V_{aux} and MOSFET current I_Q .

6.2.1 Output Voltage Regulation and Input Voltage Estimation V_g^* with Sensed Auxiliary

Winding Voltage V_{aux}

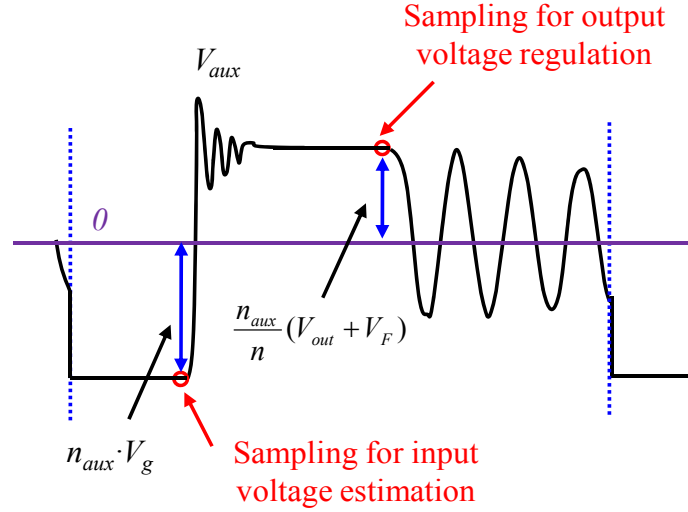


Fig. 6.4. Auxiliary winding voltage (V_{aux}) waveform with sampling points for output voltage regulation and input voltage estimation.

As shown in Fig. 6.4, the auxiliary winding voltage includes information about the output voltage at the second subinterval (Q off, D on) – the output voltage and output diode forward voltage are scaled by n_{aux}/n :

$$V_{aux} = \frac{n_{aux}}{n} (V_{out} + V_F) \quad (6.1)$$

where V_F is the output diode forward voltage drop, and n and n_{aux} are turns ratios between the primary and secondary winding, and between the primary and auxiliary winding, respectively, as shown in Fig. 6.3.

The primary side can be used to regulate the output voltage by sensing the auxiliary winding voltage. The scaled-down auxiliary winding voltage is sampled at the end of the diode conduction interval (where the diode forward voltage drop is close to zero), and the sensed

voltage is subtracted from the reference voltage V_{REF} , resulting in the output voltage error scaled by n_{aux}/n (e_v , Fig. 6.3). The compensator adjusts the switch on-time T_{ON} through the voltage error e_v for output voltage regulation.

Approaches have been proposed to avoid using complicated A/D converters in sensing voltages or currents [46] – [50]. In this section, a simple A/D conversion approach is presented for the input voltage estimation, using a single comparator A/D converter shown in Fig. 6.5. The level-shifted, scaled-down auxiliary winding voltage (the comparator positive input voltage, $V_{com}^+ = V_{offset} + K_{scale}V_{aux}$) is compared with the output of a digital-to-analog (D/A) converter. The comparator output is latched by a D flip-flop at the sampling point (S_g) shown in Fig. 6.4 where the output diode starts to conduct and the auxiliary winding voltage contains the input voltage information ($-n_{aux}V_g$). The integrator adds a scaled increment $+K_i$ or $-K_i$ to the previous estimated voltage ($V_{offset} - n_{aux}K_{scale}V_g^*$), according to signs of the latched signal, such that the

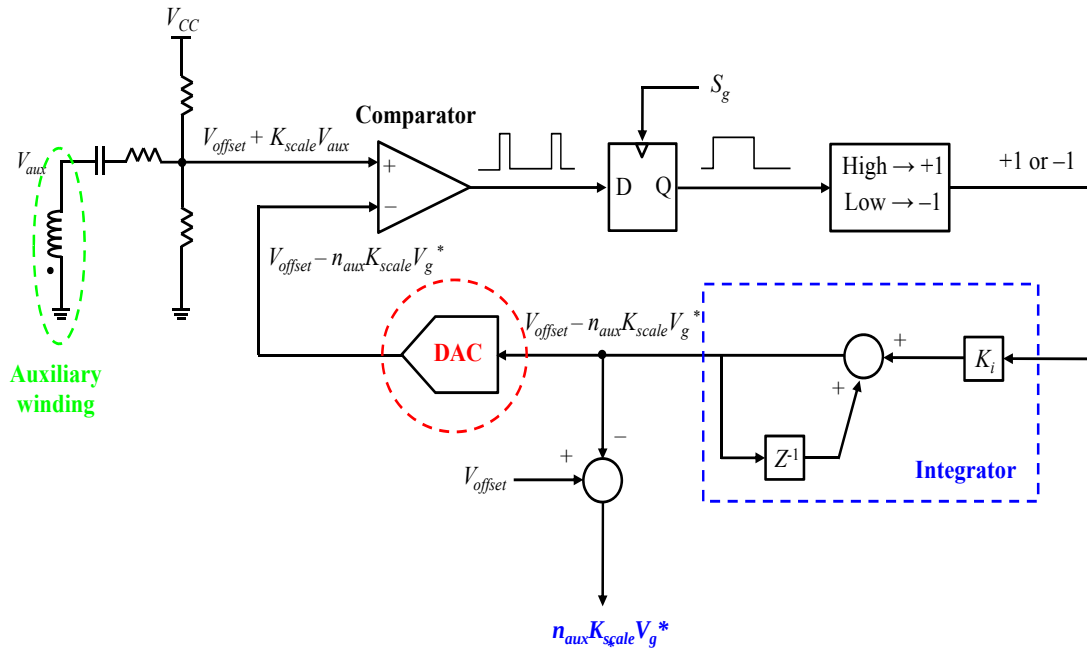


Fig. 6.5. Input voltage estimation V_g^* with a single comparator A/D converter.

estimated voltage follows V_{com}^+ at the sampling point, which is $V_{offset} - n_{aux}K_{scale}V_g$. These compensated and estimated values are in digital form, so the D/A converter converts them to an analog signal for comparison with the sensed voltage. Finally, the estimated voltage is subtracted from the offset voltage V_{offset} , resulting in the scaled-down estimated input voltage ($n_{aux}K_{scale}V_g^*$). This estimated input voltage is fed to the efficiency optimizer block in the digital controller to update optimum controller parameters (optimum valley switching points k and optimum switching periods $T_{S,CCM}$ in CCM) to the modulator over different operating conditions.

6.2.2 Input Current Estimation I_g^* with Sensed MOSFET Drain Current I_Q

The input current I_g is estimated through analysis of relationship between the input current and peak MOSFET drain current $I_{Q,peak}$, described as

$$I_g = \frac{1}{T_S} \int_0^{T_S} I_Q dt = \frac{T_{ON}}{2T_S} I_{Q,peak} \quad (6.2)$$

The switching frequency F_S varies over different operating conditions based on valley switching points programmed in the look-up table to achieve on-line efficiency optimization, so the switching period T_S should be stored in the modulator to determine an instant for compensation actions. The switch on-time T_{ON} is available from the compensator. Re-use of the switching period T_S and switch on-time T_{ON} from the modulator and compensator, respectively, allow that the input current can be estimated in using a single comparator A/D converter, similar to the input voltage estimation. As shown in Fig. 6.6, the MOSFET drain current scaled by a sensing resistor ($R_{sense}I_Q$) is compared with output of the D/A converter. Then, the comparator output is latched by a D flip-flop at the end of the first subinterval (S_g), producing +1 or -1 in order to add $+K_i$ or $-K_i$ to the previous estimated current divided by the switching period

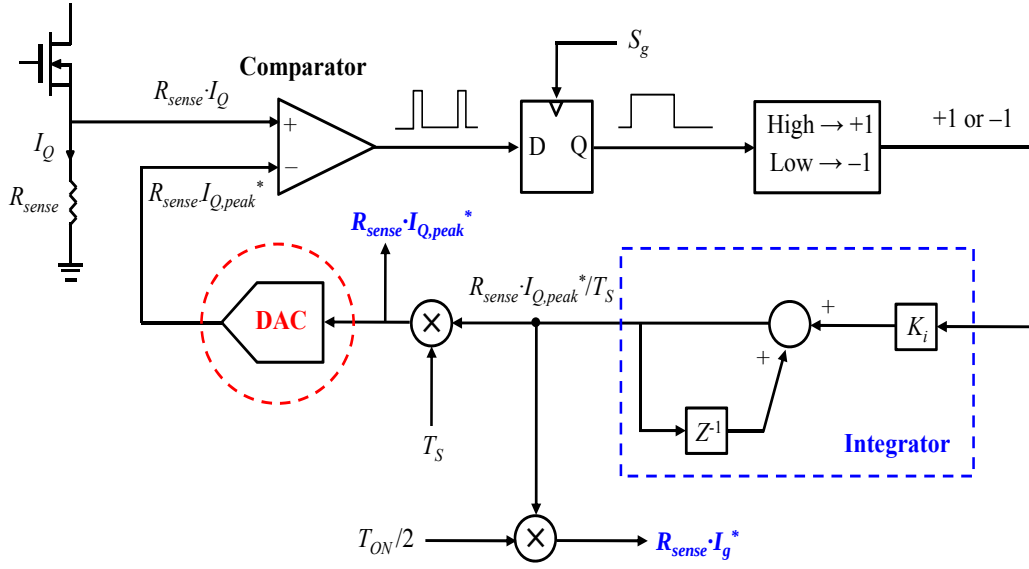


Fig. 6.6. Input current estimation I_g^* with a single comparator A/D converter.

$(R_{sense}I_{Q,peak}^*/T_s)$. This estimated value is multiplied by the switching period $R_{sense}I_{Q,peak}^*$. The D/A converter converts the estimate to an analog signal for comparison with the sensed current. Therefore, the estimation loop forces the output of the D/A converter to keep track of the sensed peak MOSFET drain current ($R_{sense}I_{Q,peak}$). To estimate the input current, the integrator output ($R_{sense}I_{Q,peak}^*/T_s$) is multiplied by one half of the switch on-time, resulting in the estimated input current scaled by the sensing resistor ($R_{sense}I_g^*$).

6.2.3 Low-Cost, Small-Size, Low-Pin-Count (≤ 8) Digital Controller IC Chip

Simplified sensing and A/D conversion approaches proposed in Sections 6.2.1 and 6.2.2 allow for implementing a low-cost, small-size, low-pin-count (≤ 8) digital controller for flyback DC-DC converters with on-line efficiency optimization. Fig. 6.7 shows a feasible 5-pin digital controller IC chip with the proposed sensing and A/D conversion techniques around a conventional flyback DC-DC converter. The primary-side control does not need an opto-coupler

and additional secondary circuitry for isolation, or other forms of isolation. Compared to use of the digital controller IC chip shown in Fig. 6.2, a pin to sense the feedback voltage (pin 7 (FB) in Fig. 6.1) can be eliminated. Pins 3 (OPPT_VG) and 4 (OPPT_IG) are not required by re-using the auxiliary winding voltage and MOSFET drain current, which are normally sensed for valley switching and protections of the converter. The input voltage and input current are estimated with single-comparator A/D converters, so the need for use of more complicated A/D converters can be removed. Table 6.3 describes functions of input and output pins assigned in the digital controller IC chip with the proposed sensing and A/D conversion techniques.

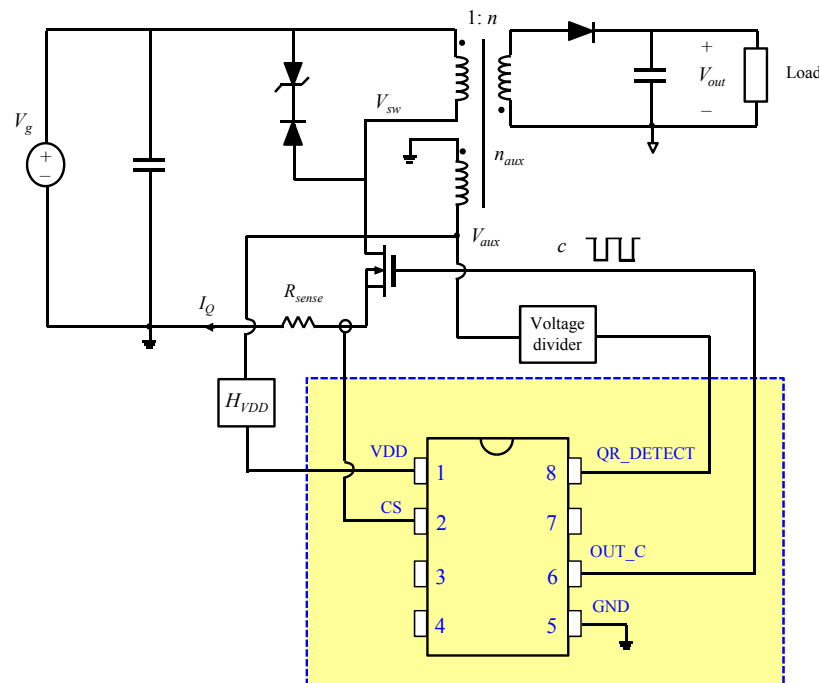


Fig. 6.7. 5-pin digital controller IC chip with the simplified sensing and A/D conversion techniques around a conventional flyback DC-DC converter.

Table 6.3. I/O pins assignment and description (digital controller with simplified sensing and A/D conversion)

Name	No.	I/O	Description
VDD	1	I	Provides power to the controller
CS	2	I	1. Senses MOSFET drain current I_Q 2. Estimates input current I_g^* 3. Limits the peak MOSFET drain current $I_{Q,peak}$ 4. Protects the converter from overload responses
GND	5	–	Ground for the controller
OUT_C	6	O	Gate driving signal c
QR_DECTECT	8	I	1. Senses auxiliary winding voltage V_{aux} 2. Regulates output voltage 3. Detects valley switching points k 4. Estimates input voltage V_g^* 5. Protects the converter from overvoltage on the load

6.3 Implementation of Primary-Side Control and Single Comparator Analog-to-Digital (A/D) Converters

To regulate the output voltage with the primary side control, it is important to keep the sampling instant over different operating conditions consistent, such that the sensed auxiliary winding voltage is not corrupted [51] – [60].

For output voltage error sensing, a pipeline A/D converter is employed and an example of the timing diagram of the pipeline A/D converter is shown in Fig. 6.8. A sampled analog signal S_1 is delayed by several clock cycles (T_{delay}). If, as with other types of A/D converters, the pipeline A/D converter senses the output voltage error once per switching period at the sampling point shown in Fig. 6.4, the delay may compromise output voltage regulation. Instead, the output voltage error is latched at a fixed point once a switching period, and the A/D converter clock is set such that the delayed voltage error is obtained at the latching point, as shown in Fig. 6.9.

Fig. 6.9 presents the output voltage error sampling mechanism. To reduce switch turn-on loss in discontinuous conduction mode (DCM), valley switching is usually employed in flyback DC-DC applications, as discussed in Chapters 2-5. In the proposed digital controller, the valley switching is implemented using a state machine in the modulator based on DCM comparator output S_{DCM} and oscillation period of the ringing in DCM (T_{OSC}) as described in Appendix A. From this state machine, a clock to latch the scaled output voltage error e_v is generated as shown in Fig. 6.9. The voltage error is latched at the time Q_{OFF} state transitions into S_0 state. The time delay due to the pipeline A/D converter operation (T_{delay}) is equal to one fourth of the oscillation period ($T_{delay} \sim 0.25 \cdot T_{OSC}$).

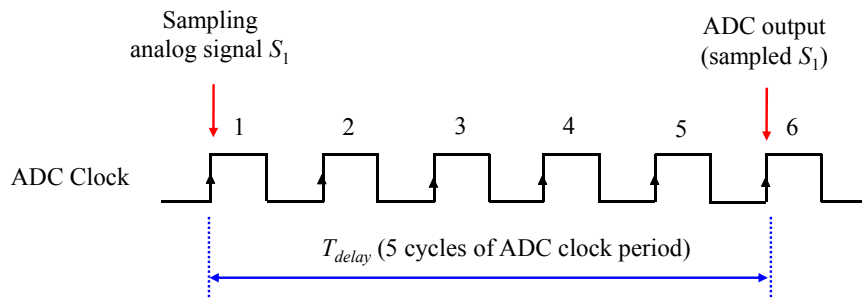


Fig. 6.8. Pipeline A/D converter clock timing diagram in a case when sampled signal comes at the converter output after 5cycles of the A/D converter clock period.

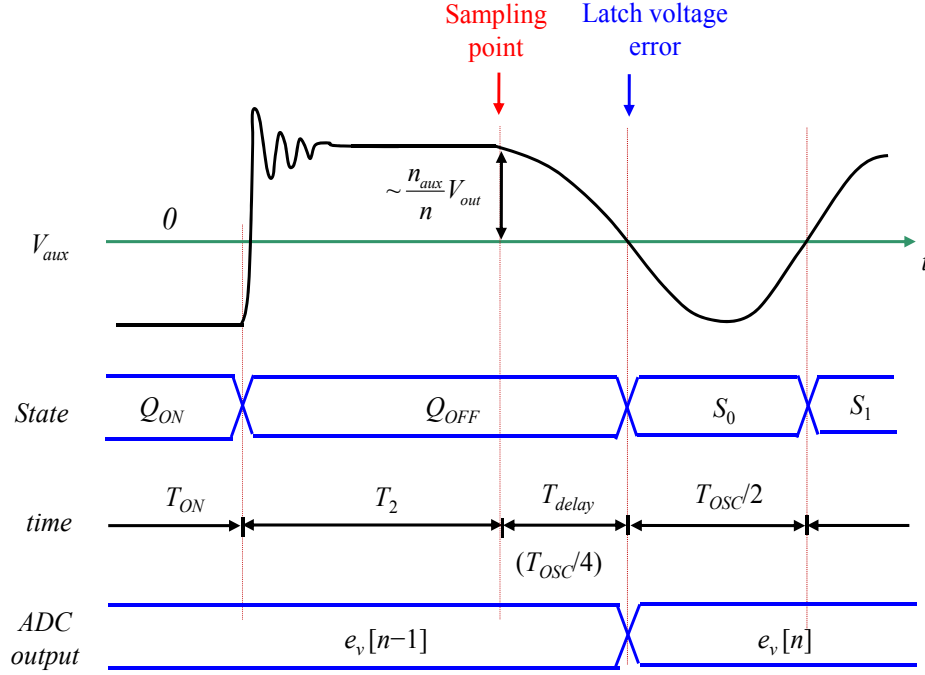


Fig. 6.9. Output voltage error sensing mechanism with pipeline A/D converter to achieve primary-side output voltage sensing and control.

If other types of A/D converters are used for voltage regulation, the scaled output voltage error e_v can be sensed once per switching period, as follows. As shown in Appendix A, time intervals of each state and the oscillation period T_{OSC} are measured and stored for valley switching in the modulator. Because Q_{OFF} state involves with the output diode conduction T_2 and one fourth of the oscillation (Fig. 6.9), the sampling point can be set at an instant right after the counter passes the diode conduction interval T_2 :

$$T_2 = T_{Q,OFF} - \frac{1}{4} T_{OSC} \quad (6.3)$$

where $T_{Q,OFF}$ is a Q_{OFF} state interval stored in the modulator.

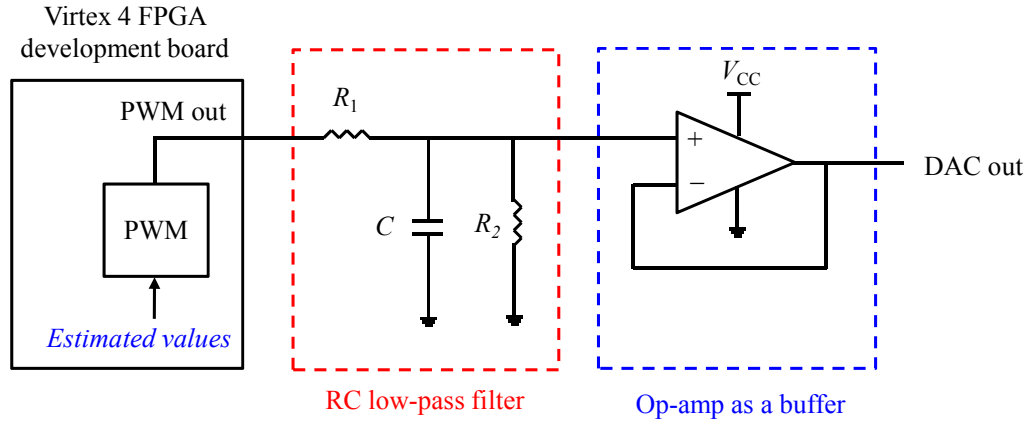


Fig. 6.10. 1-bit pulse-width modulator D/A converter used in the single-comparator A/D converter for input voltage and input current estimation.

For relatively simple implementation of the D/A converter in the single-comparator A/D converter approach used to estimate the input voltage or input current, and since the speed in the estimation loops is not critical, a 1-bit pulse-width modulation (PWM) D/A converter is employed. The estimated values through the detection loops ($V_{offset} - n_{aux}K_{scale}V_g^*$ and $R_{sense}I_{Q,peak}^*$) are modulated by pulse width modulators implemented in the digital controller. The modulated signals are averaged by RC low-pass filters followed by buffers, as shown in Fig. 6.10. The estimated values involve ripples caused by the PWM, but effects of these ripples on the estimation can be neglected by properly selecting filter components. The single-comparator A/D converter is fully digital except for the comparator and the low-pass filter.

6.4 Experimental Results

The experimental setup consists of 65 W flyback DC-DC converter which is the same as the optimized power stage presented in Table 5.1 and interfaced to a prototype digital controller using an FPGA, and an auxiliary board for implementation of primary-side control and

Table 6.4 Flyback power stage parameters

Parameters	Values
Input voltage, V_g	130 – 300V
Output voltage, V_{out}	18V
Load current, I_{out}	0.05 – 3A
Switching frequency, F_S	20 – 200kHz
Turns ratio between primary and secondary sides, n	0.20
Turns ratio between primary and auxiliary sides, n_{aux}	0.20
Magnetizing inductance, L_M	360 μ H
Leakage inductance, L_{lk}	2.6 μ H
Output capacitance, C_{out}	4,500 μ F
Clamp voltage, V_{clamp}	400V
MOSFET drain current sensing resistor, R_{sense}	0.2 Ω

estimation of input voltage and input current. The flyback power stage parameters are summarized in Table 6.4.

As described in Section 6.3, the pipeline A/D converter (THS1230, Texas Instrument) is used for output voltage error sensing, with a sampled signal delayed by 5 A/D converter clock cycles. The oscillation period T_{OSC} is around 1.2 μ s, so the A/D converter clock frequency is set to around 10MHz.

The same gain-scheduled compensator and k -control scheme, described in Chapter 5, are employed for improved dynamic responses and reduced peak MOSFET drain current (Table 5.3 and k -control gain $\alpha = -1000$).

Table 6.5. Experimental results of output voltage regulation and input voltage and input current estimations over different operating modes

Operating modes	1 ($F_S = 20\text{kHz}$)	2 ($1 < k_{opt} \leq 14$)	3 ($k_{opt} = 1$)	4 (CCM)
Output voltage V_{out}	17.91V	17.93V	17.88V	18.02V
Input voltage V_g	130V	150V	200V	130V
Estimated input voltage V_g^*	128.7V	148.2V	197.3V	128.7V
Input current I_g	7.2mA	67mA	0.184A	0.423A
Estimated input current I_g^*	6.9mA	63mA	0.177A	0.405A
Load current I_{out}	50mA	0.5A	2A	3A
Switching Frequency F_S	20kHz	~40kHz	~100kHz	110kHz
Valley switching points k	—	14	1	0

Table 6.5 presents experimental results of output voltage regulation through the sensed auxiliary winding voltage, demonstrating that the output voltage is precisely regulated around 18V over different operating modes.

For input voltage and current estimations, the PWM D/A converter is constructed as follows. The switching frequency of the PWM is synchronized with the switching frequency of the converter, and the cutoff frequency of the RC low-pass filter is around 1 kHz ($R_1 = R_2 = 10\text{k}\Omega$, $C = 10\text{nF}$). The integrator gain K_i for the input voltage is selected as 0.05, while K_i for input current estimation as 40, so that estimation actions are fast enough to achieve well-behaved

transient responses. The estimated input voltage or input current are updated once per switching period.

Figs. 6.11 and 6.12 show waveforms measured at the positive and the negative input of the comparators used in loops to estimate operating conditions V_g and I_g , respectively. The estimated values ($V_{offset} - n_{aux}K_{scale}V_g^*$ and $R_{sense}I_{Q,peak}^*$) properly track the level-shifted auxiliary winding voltage (Fig. 6.11) and the scaled peak MOSFET drain current (Fig. 12) at the sampling points where the switch on-time interval ends. The estimated input voltages V_g^* and input currents I_g^* are presented in Table 6.5, verifying that the estimation results are well matched with measured input voltages and input currents within errors of 2% and 5%, respectively.

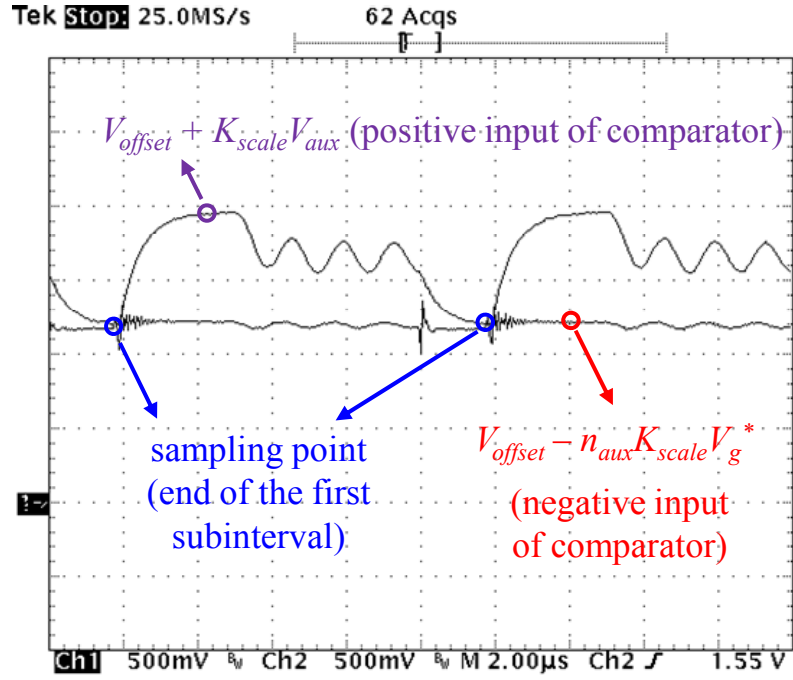
Fig. 6.13 shows comparisons of efficiencies as functions of the load current at 3 different input voltages (140V, 220V and 300V), for 3 cases: (case 1) experimentally measured efficiency with the 65 W flyback prototype using the proposed sensing and A/D conversion techniques, (case 2) experimentally measured efficiency of the 65W flyback prototype with direct sensing and detection of the operating conditions [45], and (case 3) experimentally measured efficiency of the same 65 W flyback prototype operated at a constant switching frequency (100kHz). From comparisons between cases 1 and 2, it should be noted that the proposed estimate input voltage and input current estimation techniques do not affect on-line efficiency optimization over wide ranges of operating conditions. Significant efficiency improvements are obtained compared to the efficiency measured with the prototype operating at fixed frequency (case 3).

Dynamic responses of the input current estimation loop during a 0.1A-to-2.5A step load transient are presented in Fig. 6.14, while experimental results for large signal transient responses (0.1A-to-2.5A and 2.5A-to-0.1A step load transients) are indicated in Fig. 6.15. The input current estimation settles in about 8 ms, which is sufficiently fast. Step-load transient

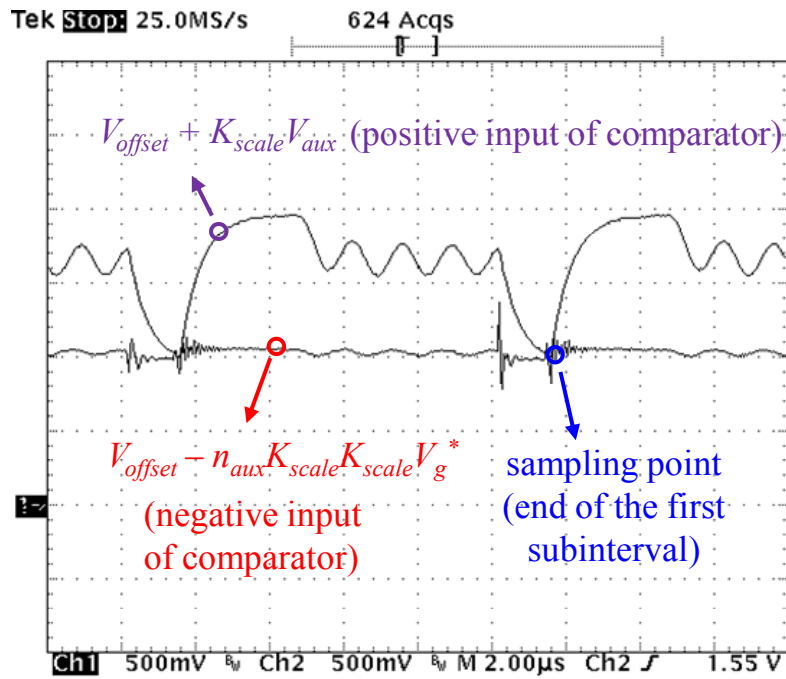
responses are essentially the same as in the prototype based on direct A/D sensing of the output voltage on the secondary side, together with A/D sensing of the input voltage and input current (Chapter 5 and [45]). The proposed sensing and A/D conversion approaches do not degrade dynamic responses or efficiency performance of the digitally controlled flyback converter.

6.5 Conclusions

This chapter describes simplified sensing and A/D conversion techniques for conventional flyback DC-DC converters with on-line efficiency optimization, targeting a low-cost, small-size, low-pin-count (≤ 8) digital controller chip implementation. Primary-side-only sensing and control are presented in combination with single-comparator A/D techniques to estimate input voltage and input current. The proposed sensing and A/D conversion techniques eliminate the need for complicated A/D converters to detect operating conditions as well as additional circuitry with isolation in the feedback path between secondary and primary. Experimental results on a 65W flyback prototype show that the operating points are estimated within 5% of the directly measured values. The output voltage is precisely regulated over various operating conditions. The proposed sensing and A/D conversion approaches enable on-line efficiency optimization and consistent transient responses over different operating modes.

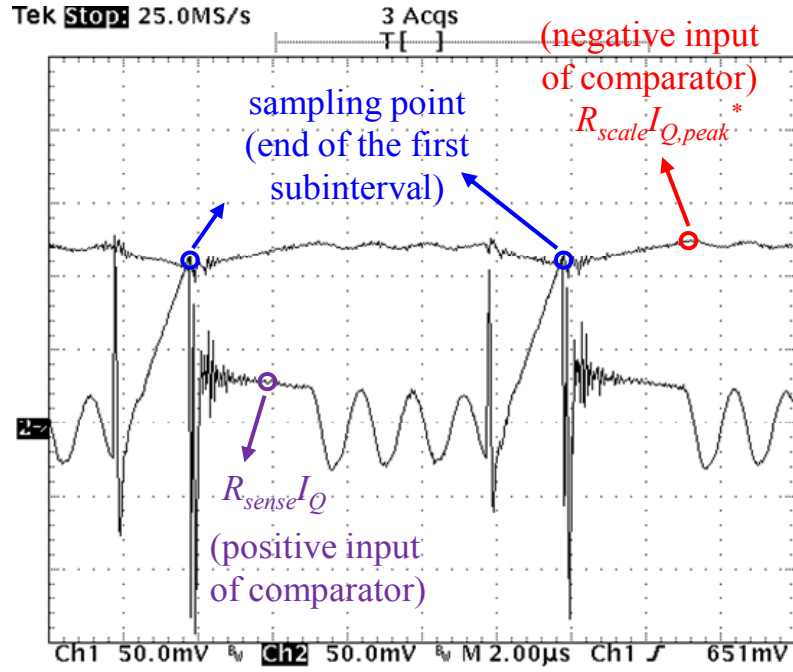


(a) $V_g = 130V$

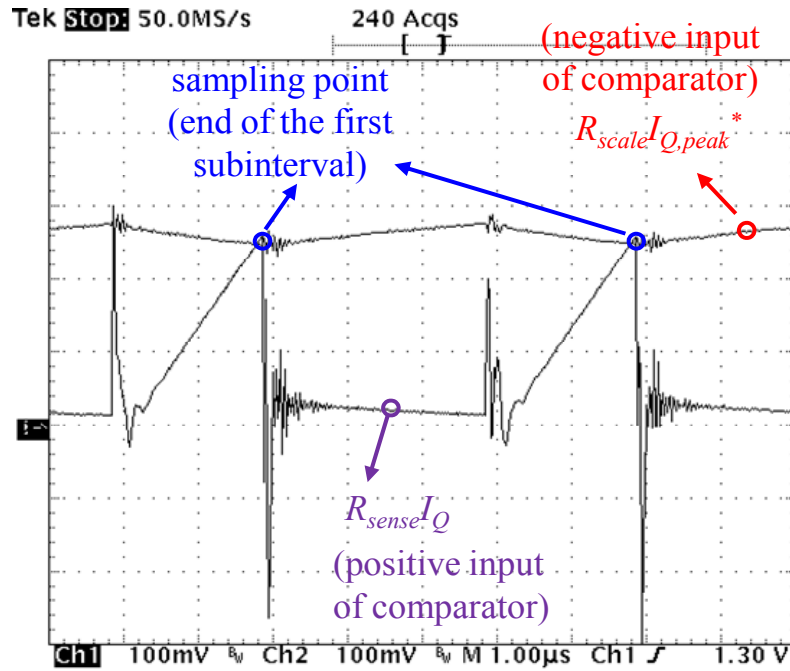


(b) $V_g = 200V$

Fig. 6.11. Waveforms measured for input voltage estimation V_g^* .

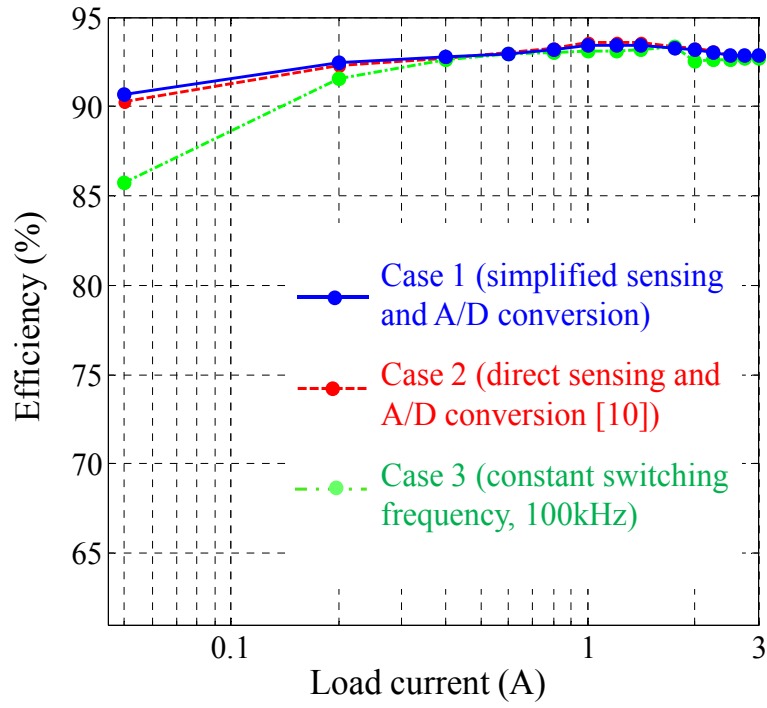


(a) $I_g = 75\text{mA}$

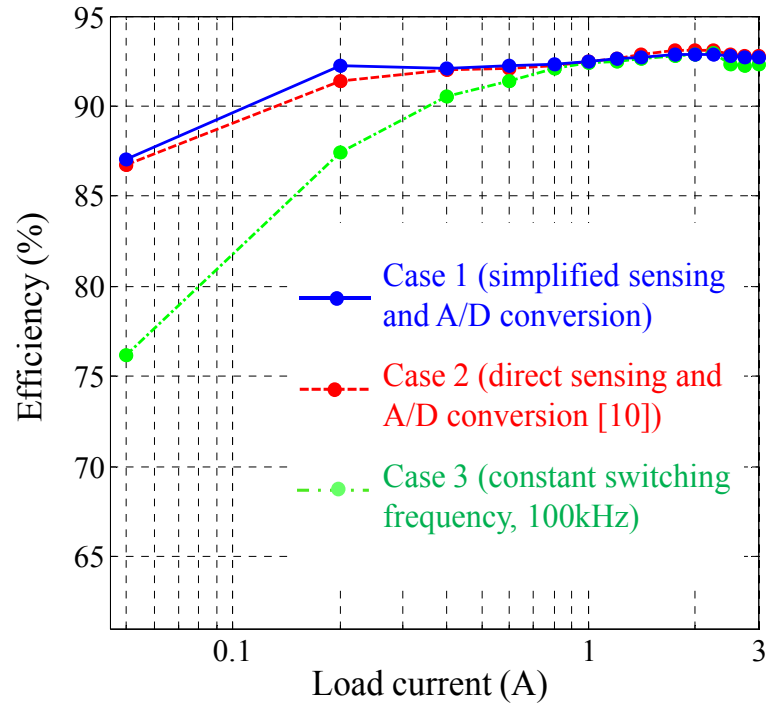


(b) $I_g = 0.4\text{A}$

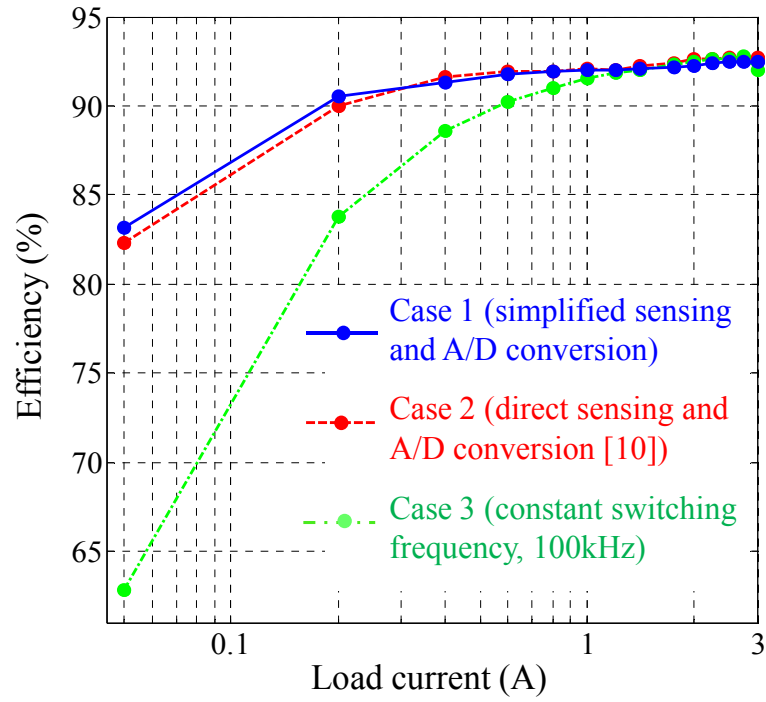
Fig. 6.12. Waveforms measured for input current estimation I_g^* .



(a) $V_g = 140V$



(b) $V_g = 220V$



(a) $V_g = 300V$

Fig. 6.13. Comparison of efficiency results at 3 different input voltages (140V, 220V and 300V).

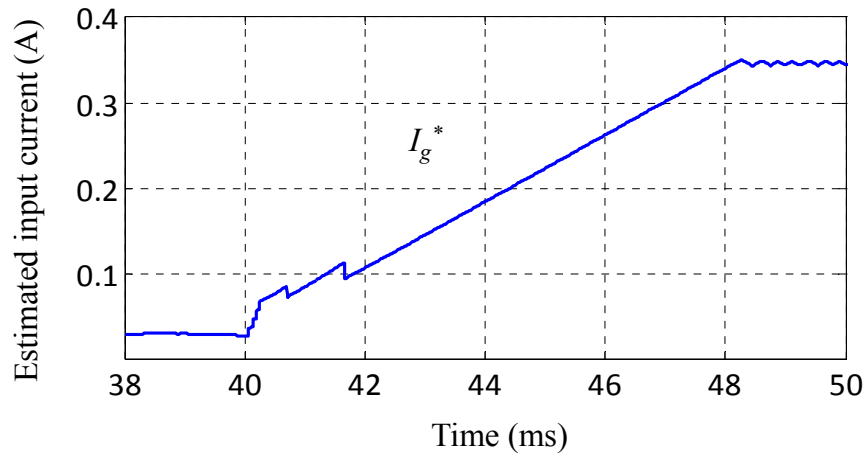
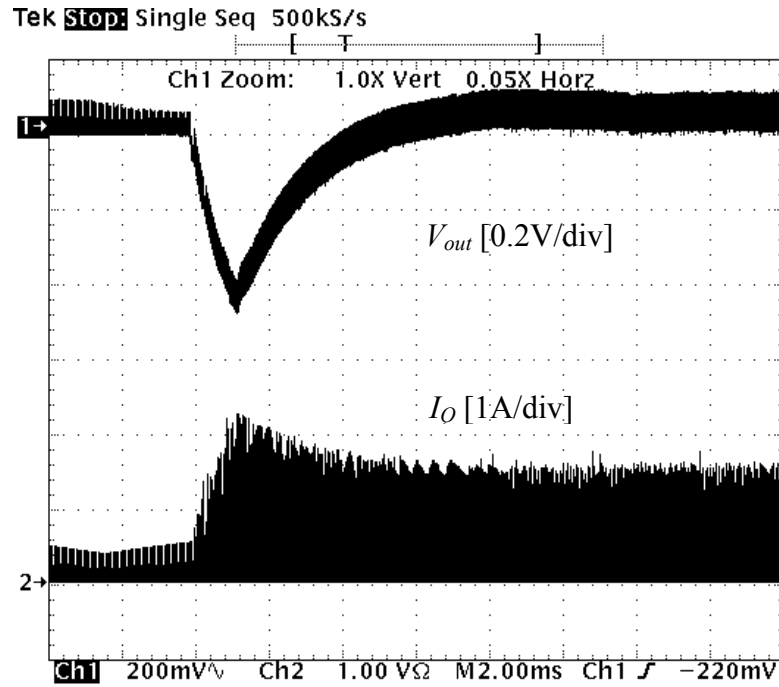
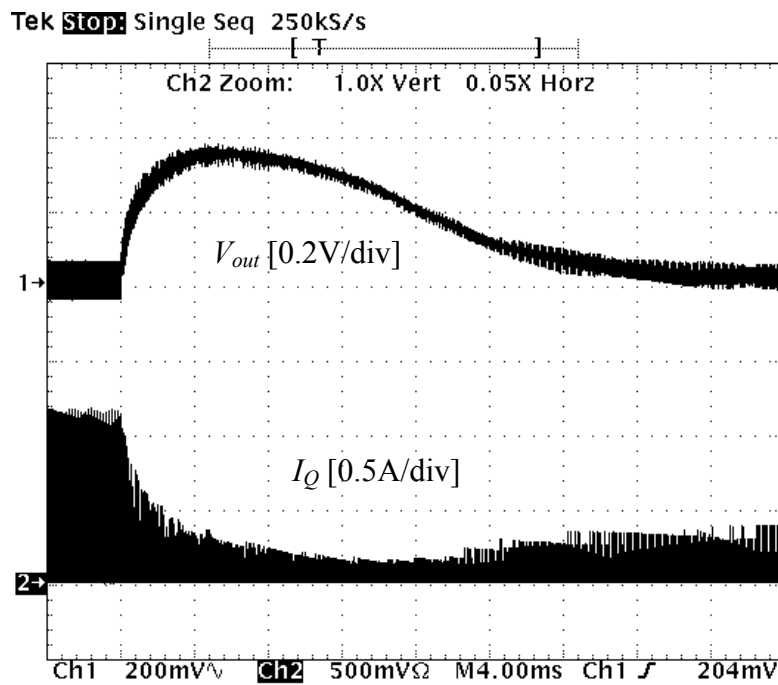


Fig. 6.14. Dynamic responses of input current estimation loop during 0.1A-to-2.5A step load transient.



(a) 0.1A-to-2.5A step load transient



(b) 2.5A-to-0.1A step load transient

Fig. 6.15. Experimental results (output voltage V_{out} and MOSFET drain current I_O) for step load transients at 130V.

Chapter 7

Conclusions

A relatively simple approach to achieve efficiency optimization in digitally controlled DC-DC converters is proposed and discussed in the thesis. The approach includes optimization of power stage design and controller parameters based on detailed power loss models and multi-variable non-linear constrained optimization, together with design of digital controller using a look-up table that stores the optimum controller parameters over different operating conditions. A flyback DC-DC converter configuration, introduced in Chapter 2, is examined for experimental verifications of the proposed efficiency optimization approach.

In Chapter 3, power loss models of a conventional flyback DC-DC converter are derived to perform efficiency optimization over power stage design and controller parameters. Experimental results demonstrate that the loss models are valid over wide ranges of operating conditions, by predicting the total power dissipation within 5% of the experimental results.

In Chapter 4, a procedure to optimize the power stage design and controller parameters is presented and experimentally verified, based on the power loss models derived in Chapter 3 and multi-variable non-linear constrained optimization over wide ranges of operating conditions. A valley switching technique is applied to decrease switch turn-on loss in discontinuous conduction mode. The optimization procedure is formulated to minimize power losses weighted over a range

of operating points, under a cost constraint. Significant efficiency improvements are achieved by the proposed efficiency optimization approach.

In Chapter 5, a look-up table based digital control approach is presented to accomplish on-line efficiency optimization. The controller parameters (optimum switching frequency and optimum operating modes) are programmed in the look-up table. Undesirable frequency hopping mechanisms, commonly observed in other valley switching schemes, are discussed and resolved by storing valley switching points and adding hysteresis bands to boundaries in the look-up table. A gain-scheduled compensator and a new control scheme, named k -control, are employed to improve large-signal transient responses. Experimental results show that efficiency can be significantly improved over wide ranges of operating conditions, and smooth mode transitions and consistent transient responses can be achieved over different operating modes. Contributions of power stage and controller optimization on efficiency improvements are analyzed, which show that a large portion of power loss reduction is achieved by power stage optimization, and that the look-up table based digital controller enables relatively simple implementation of the proposed on-line efficiency optimization approach.

In Chapter 6, simplified sensing and analog-to-digital (A/D) conversion techniques are proposed, targeting a low-cost, small-size, low-pin count (≤ 8) digital controller IC chip implementation for control of flyback DC-DC converters with on-line efficiency optimization. A primary-side control is employed to regulate output voltage, resulting in elimination of an opto-coupler and additional secondary side circuitry, or other forms of isolation in the feedback path. Single-comparator A/D converters are constructed to remove the need for complicated A/D converters for input voltage and input current detections. Experimental results demonstrate that

the proposed sensing and A/D conversion approaches allow for on-line efficiency optimization and consistent transient responses over various operating conditions.

7.1 Future Work

Control and optimization techniques presented in thesis can be used in other power electronics applications. In grid-tied photovoltaic (PV) systems, a centralized DC-AC inverter is usually employed and has been a main stream in industry. The centralized inverter converts DC power from multiple PV modules into AC power delivered to the AC grid. However, demands for alternative architecture based on microinverters have been growing recently due to potential advantages [61]. As opposed to central-inverter systems, a microinverter is connected to an individual PV module and microinverter outputs are tied to the AC grid in parallel, such that AC power from each microinverter is combined and fed into the grid. The approach reduces installation costs because currently simple, standard wiring techniques can be applied to microinverter-based PV systems. Another advantage is that the microinverter performs maximum power point tracking (MPPT) for each PV module instead of entire PV arrays in central inverter systems, thus improving energy capture in the presence of undesirable conditions such as partial shading or mismatches in PV modules.

As shown in Fig. 7.1, a DCM flyback converter can be adopted as an intermediate stage in the microinverter to convert DC power from the PV module into AC power, implying that the efficiency optimization and the digital control techniques proposed in the thesis can be extended to microinverter systems. The switch on-time or duty cycle changes over a line period to produce the AC power, and the flyback converter output voltage and current i_D are averaged by an EMI filter, resulting in folded line voltage v_g and line current i_g .

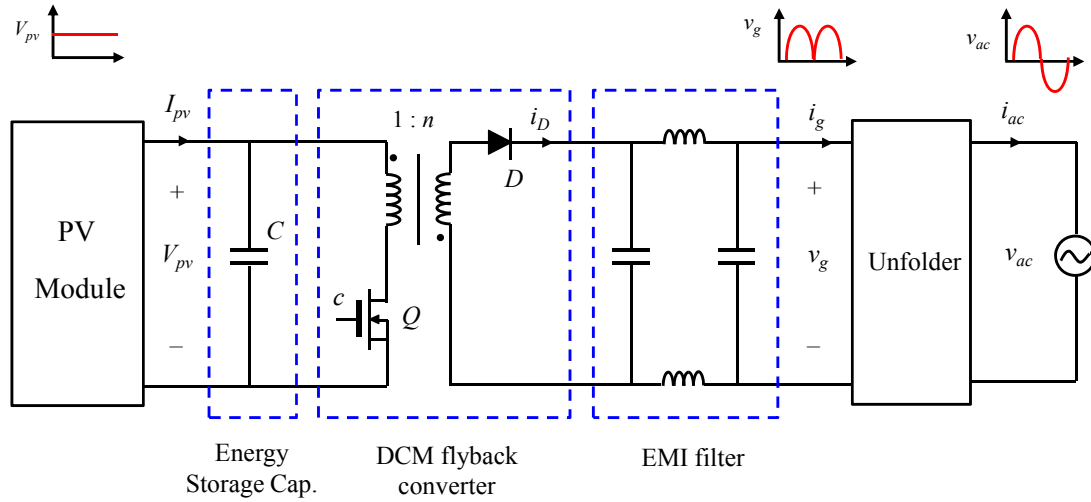


Fig. 7.1. PV microinverter using a DCM flyback converter.

It is very important to efficiently deliver captured energy to the AC grid. In most of power converter applications in PV microinverter systems, fixed switching frequency is used with valley switching over a line period. As presented in the thesis, however, the optimum controller parameters (switching frequency and operating modes) in flyback DC-DC converters are variable over different operating conditions. Under the assumption that the flyback power stage is appropriately designed, therefore, the controller optimization approach proposed in the thesis could be applied for improved efficiency compared to fixed-frequency operation over a range of operating conditions (e.g. folded ac line voltage v_g and power levels).

Appendix A

Valley Switching and State Machine (Modulator)

Implemented for Optimum Operating Modes

Detailed implementations of the valley switching scheme and state machine employed in the proposed digital controller are presented in this Appendix. Fig. A.1 shows waveforms and states related to the switch-turn-on at the 4th valley switching point. The auxiliary winding produces the auxiliary winding voltage V_{aux} , and the DCM comparator outputs the signal S_{DCM} by comparing the auxiliary winding voltage and zero. Therefore, the signal S_{DCM} has information of the ringing due to the magnetizing inductance and switching-node voltage during the 3rd subinterval, as shown in Fig. A.1. There are four important states defined corresponding to conductions of the MOSFET Q and output diode D , and the S_{DCM} . The first state is Q_{ON} state where the switch Q turns on during the 1st subinterval. The second state is Q_{OFF} state where the output diode D conducts. However, this state is not exactly the same as the diode conduction interval, because it includes one fourth of oscillation right after the diode turned off. S_0 and S_1 states are defined when the signal S_{DCM} is low and high during the 3rd subinterval, respectively. As shown in Fig. A.1, the valley switching points exist in the S_0 states. The states are summarized in Table A.1.

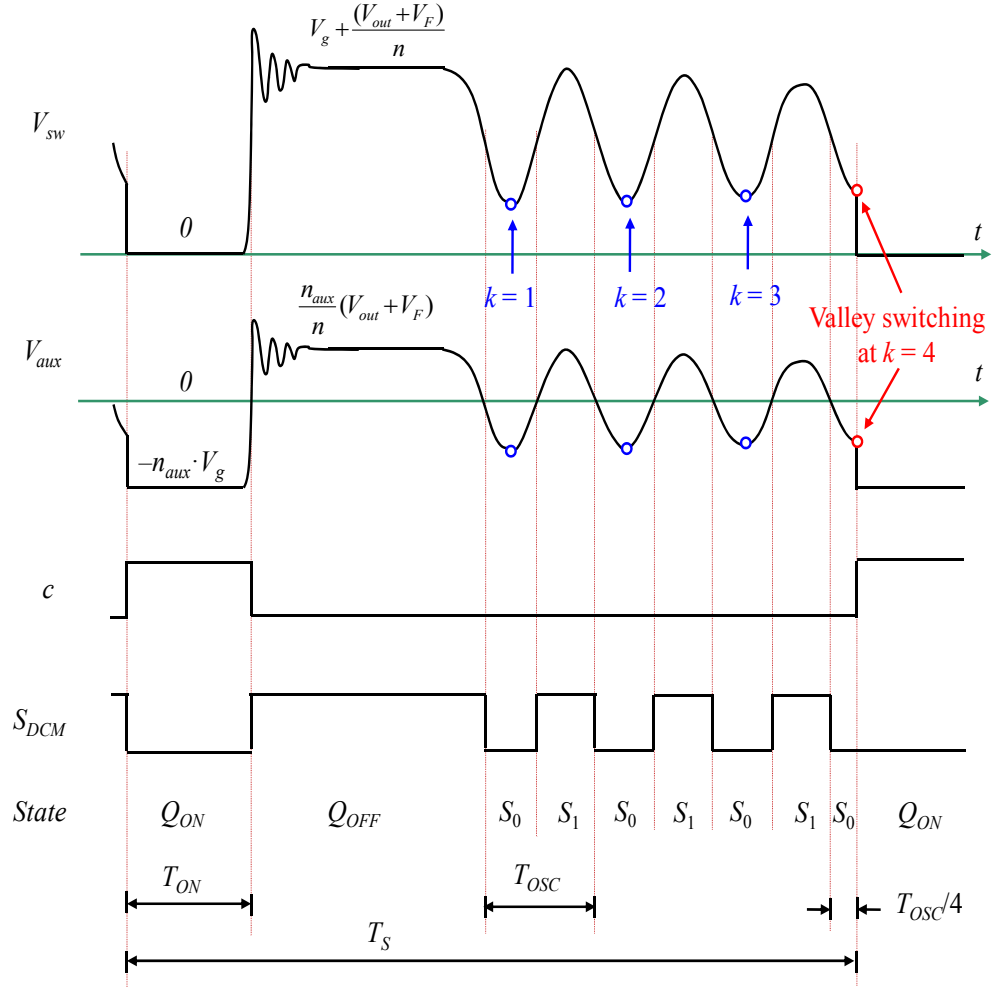


Fig. A.1. Waveforms and states related to example of valley switching – switch-turn-on at the 4th valley switching point (V_{sw} : switching-node voltage, V_{aux} : auxiliary winding voltage, c : control signal, and S_{DCM} : DCM comparator output).

Table A.1. Summary of each state programmed for valley switching

States	Description
$INIT$	Initial state. If undesirable situations occur, the states are initialized into this state.
Q_{ON}	The switch Q turns on during this state.
Q_{OFF}	The output diode D conducts and the 3 rd subinterval starts after the output diode conduction interval
S_0	The S_{DCM} is low during the 3 rd subinterval, where the valley switching points are located
S_1	The S_{DCM} is high during the 3 rd subinterval

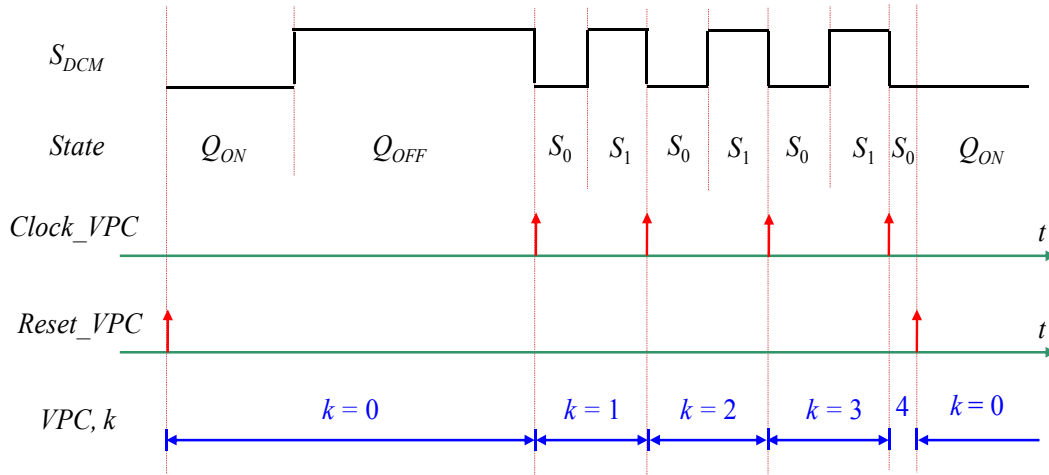


Fig. A.2. Example of counting valley switching points for switch-turn-on at the valley switching point updated from the look-up table ($k = 4$).

It is required to count valley switching points such that the modulator (state machine) turns on the switch at the valley switching point updated from the look-up table. Fig. A.2 shows clocks used to count valley switching points with the same example as Fig. A.1 ($k = 4$). The

clock, named $Clock_VPC$ in Fig. A.2, is generated in two cases: (1) the Q_{OFF} state changes into the S_0 state and (2) the S_1 state changes into the S_0 state. A counter in the modulator counts the clock $Clock_VPC$ to compare with the valley switching point k updated from the efficiency optimizer in Fig. 5.1.

For implementation of state machines in the modulator, 3 counters are employed: the two counters measure overall switching period T_S and time intervals of each state, named as counter and counter_state in Fig. A.3, respectively, and the other counter counts valley switching points. If the switching period measured by the counter is larger than the maximum switching period, the reset signal is triggered such that the states are initialized into the INIT state.

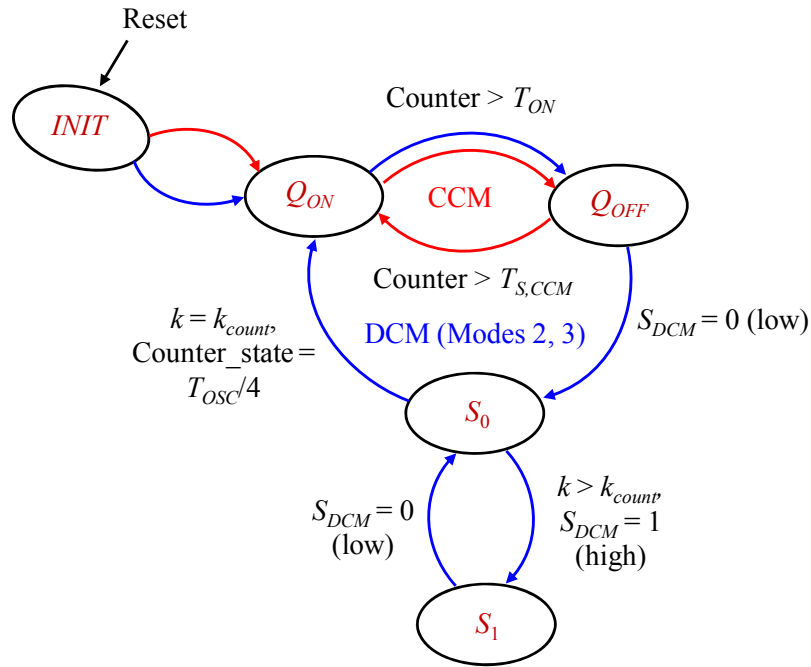


Fig. A.3. State machines implemented in modulator for optimum operating modes 2 – 4.

Fig. A.3 shows the state machine used to achieve optimum operating modes 2 – 4. When the converter operates in mode 4 (CCM), the switch Q is turned on if the measured switching period by the counter is the same as the optimum switching period $T_{S,CCM}$ stored in the look-up table. In mode 2 ($1 < k_{opt} \leq 14$), the S_0 and S_1 states are flipped until the counted valley switching points k_{count} reaches to the optimum valley switching points k . The state machine, then, forces the switch Q to turn on after one-fourth of oscillation period ($T_{OSC}/4$) which is measured by the counter_state. In mode 3 ($k_{opt} = 1$), the switch Q turns on during the S_0 state right after the Q_{OFF} state, since the valley switching point k is 1 to employ critical conduction mode.

As presented in Chapter 5, the oscillation decays at long switching periods and advantages of valley switching are lost, so the valley switching is not employed in mode 1 ($k > 14$). Therefore, the state machine is programmed in mode 1 so that the switch turns on again if the measured switching period crosses over the pre-set minimum switching period, $T_{S,MIN} = 50\mu s$.

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