Advanced Load Modulated Power Amplifier Architectures

by

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Advanced Load Modulated Power Amplifier Architectures

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Power amplifier (PA) applications increasingly require wideband linear operation, such as in carrier aggregation, high-data rate communications as well as several other RF systems including radar, RFID, RF sensing, imaging etc. Additionally, the high peak to average power ratio (PAPR) signals of modern communications systems require operation over a wide dynamic range. Both bandwidth and linearity requirements are at odds with efficiency in conventional amplifier design. As a result, PA design with a simultaneous wideband operation, linearity, and energy efficiency has been a longstanding challenge.

This thesis presents several advanced Load Modulated Balanced Amplifier (LMBA) architectures with a common goal of operating an LMBA from a single RF-input. From previous LMBA demonstrations, an externally generated control signal is injected into the isolation port of a balanced amplifier, thus controlling the load impedance seen by the two main devices of the balanced amplifier. This study focuses on both eliminating the externally needed control signal and making LMBA architectures compatible with high PAPR modulated signals while maintaining wideband operation.

The thesis proposes three novel architectures of LMBA, the RF-input LMBA, Octaveband LMBA, and Doherty-like LMBA (D-LMBA). The proposed architectures are demonstrated through five different PAs. A narrowband version of the RF-input LMBA operating at 800 MHz uses a saturated control PA to track the optimum load as the power backs-off while maintaining the efficiency in the back-off region (6.5dB output power back-off). The octaveband version, built on the same concept of RF-input operation, utilizes the passband phase response of a filter allowing it to operate over 1.8 GHz to 3.8 GHz. The D-LMBA demonstrated at 800 MHz and at 2.4 GHz utilizes a class C biased control PA, analogous to the auxiliary PA in a Doherty architecture, further increasing the back-off range to 8.5 dB. The D-LMBA concept is further extended to an X-band MMIC implementation for which octaveband PAs operating over 6-12 GHz are designed on Qorvo's GaN 0.15um process and are under test.

Dedication

To my beloved family.

Acknowledgments

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Chapter 1

Introduction

1.1 Motivation

The power amplifier (PA) is one of the most critical element of any wireless transmitter. The primary function of the PA is to amplify the signal to be transmitted to its required power level. The amplification is performed by converting direct current (DC)-input power into radio frequency (RF)-output power. As the number of power limited mobile transmitting platforms (e.g. cell phones, wearable electronics) increases it is highly desirable to increase the efficiency of the PA, most often measured as the ratio of RF-output power to dc-input power (drain efficiency).

Generally, the PA consumes more than 50% of the total power required by the entire transmitter [1–3]. Therefore, to have an efficient transmitter the PA needs to be highly efficient. In transmitters, the PA efficiency trades off with other system specifications such as linearity, bandwidth, and gain. The challenge of efficient PA design lies in managing these trade-offs while meeting system requirements. In general, the trade-offs are made based on the PA application and/or type of modulated input signal. Some of the key trade-offs in PA design are listed below.

Efficiency-linearity trade-off: In modern communication standards where the data rate and data volume are very high, the PA linearity plays an important role in the communication link. The PA linearity can

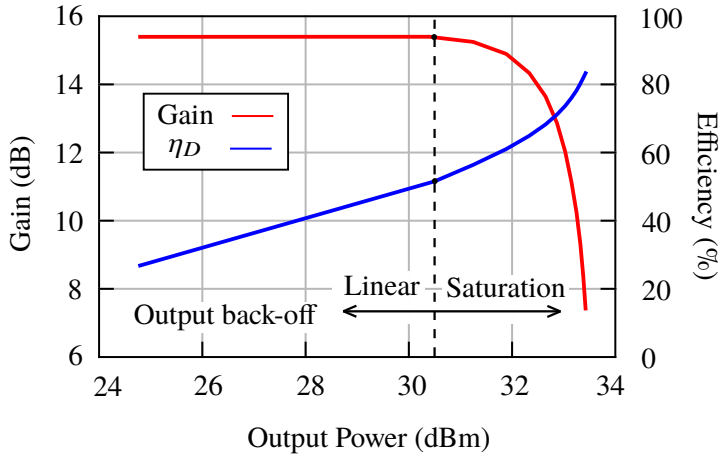
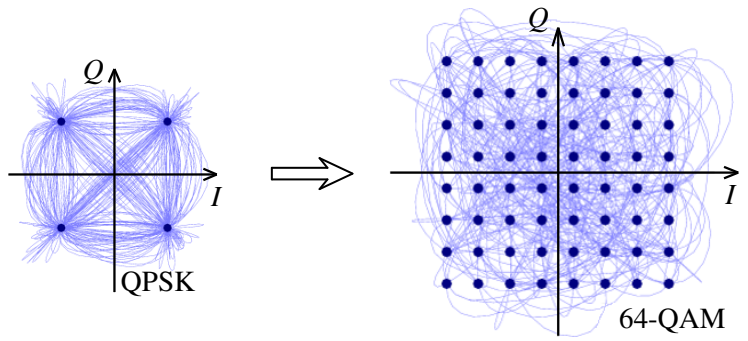


Figure 1.1: Representative plots of gain and drain efficiency (η_D) showing typical behavior of a single-ended PA. In the saturation region, the optimum efficiency of the PA is achieved. However, the gain compresses producing distortion.

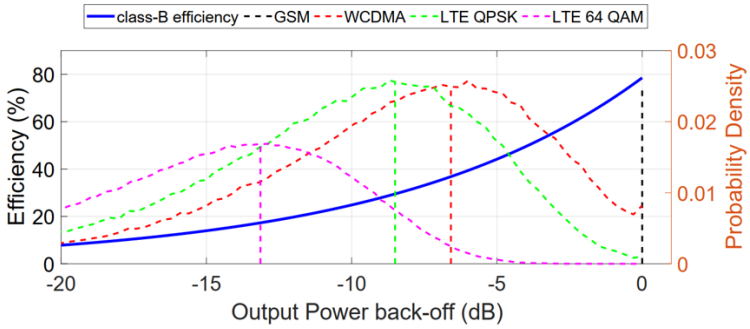
be improved by externally applying analog/digital pre-distortion techniques [4]; however such techniques increase system complexity and require additional baseband computations that eventually reduce the overall transmitter efficiency. Alternately, operating the PA in the power back-off region also improves the PA linearity, however this comes at a cost of lower efficiency. For example, as the power backs off, the efficiency of a typical class B PA reduces as the square root of the power. On the other hand efficient operation can be achieved when the PA is operated in the saturation region (near peak power), but a saturated PA compresses the signal amplitude and introduces phase distortion that in turn degrades the PA linearity. This trade-off is illustrated in Fig. 1.1 by plotting the typical behavior of a single-ended PA.

Efficiency-bandwidth trade-off: As wireless standards have evolved for improved spectrum sharing, more and more frequency bands have been allocated to cellular communication. A cost-effective way of supporting these communication links is to utilize a wideband transmitter which can cover different frequency bands. However, the bandwidth requirement adds an additional challenge for the PA designers. Wideband matching networks used in such transmitters are typically lossy, reducing the efficiency of the PA [5]. On the other, efficiency enhancement techniques improve the efficiency of the PA but are inherently narrow-band or require additional complexity to achieve wideband performance.

Efficiency-Modulation complexity trade-off: Another challenge imposed by the ever-evolving wireless standards is the modulation complexity of the signal. To support high data rate transmission, signal



(a)

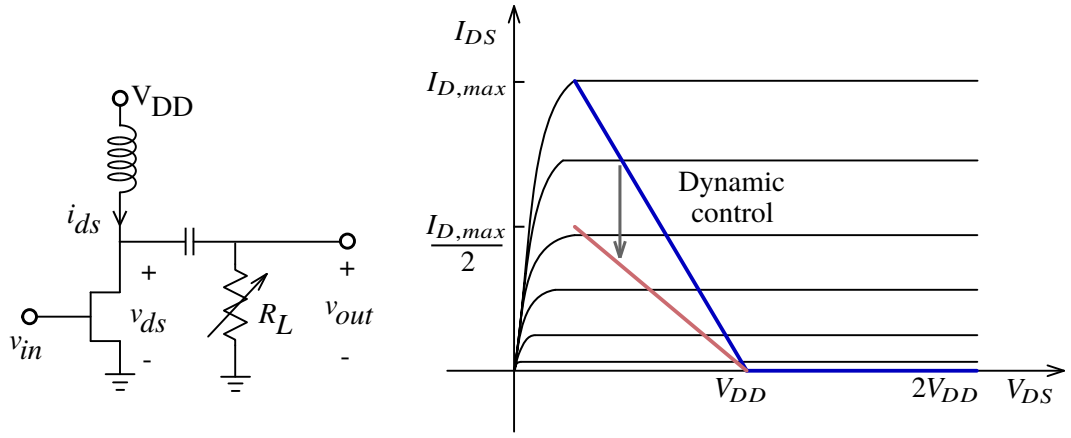


(b)

Figure 1.2: Efficiency vs modulation complexity (a) – Signal constellation density as the modulation complexity increases, (b) – Efficiency of a classic class-B PA and various signal probability density function (PDF).

constellations are made denser so that more bits can be associated with a single symbol. Multi-carrier signals such as OFDM consists of N adjacent and orthogonal sub-carriers spaced by the frequency distance f on the frequency axis. Such signals are capable of maintaining a high data rate however they require high peak-to-average-power ratio (PAPR) [6]. A high PAPR signal will spend more time at lower power levels where the instantaneous efficiency is low. This concept is illustrated in Fig. 1.2. An efficiency-output power profile of a conventional class-B is plotted on the left Y-axis and the probability density function (PDF) for various cellular signals is plotted on the right-Y axis. As the modulation complexity of the signal increases, the PAPR increases and the average efficiency of the PA decreases.

The motivation behind this research work is to manage the efficiency-bandwidth-modulation complexity trade-off by proposing novel PA architectures which can be simultaneously wideband, linear, energy efficient and can support complex modulation signal such as 4G and beyond. This research achieves this goal through novel advanced load modulated PA architectures.



(a) (b)

Figure 1.3: The concept of load modulation on a single-ended PA (a) – General schematic of a PA with varying load, (b) – Effect of load modulation on the I-V curve of the transistor.

1.2 Load Modulation

Load modulation techniques are implemented to enhance the overall transmitter efficiency, particularly in mobile and wireless transmitters where complex signal modulation schemes are widely utilized. Such transmitters are designed for signals that have PAPR in the range of 10-12 dB; load modulation improves average efficiency in these transmitters. The load modulation technique allows high efficiency to be maintained over wide power back-off range by dynamically varying the load corresponding to the input drive level.

The basic principle of efficiency enhancement through load modulation is to maintain maximum voltage swing across the output of the device (V_{ds}) while scaling the drain current (I_{ds}) with respect to the input voltage. This behavior can be achieved by dynamically varying the load impedance of the transistor. Fig. 1.3(a) shows a simplified transistor amplifier circuit operating under dynamic load modulation. Considering the transistor is biased in Class-B, the load-lines for peak power and 6-dB back-off power which would produce maximum voltage across the output of the device are shown in Fig. 1.3(b). From the loadline, it is apparent that as the output current scales in proportion with the output power, the load impedance must scale inversely with the output power to maintain the constant voltage swing.

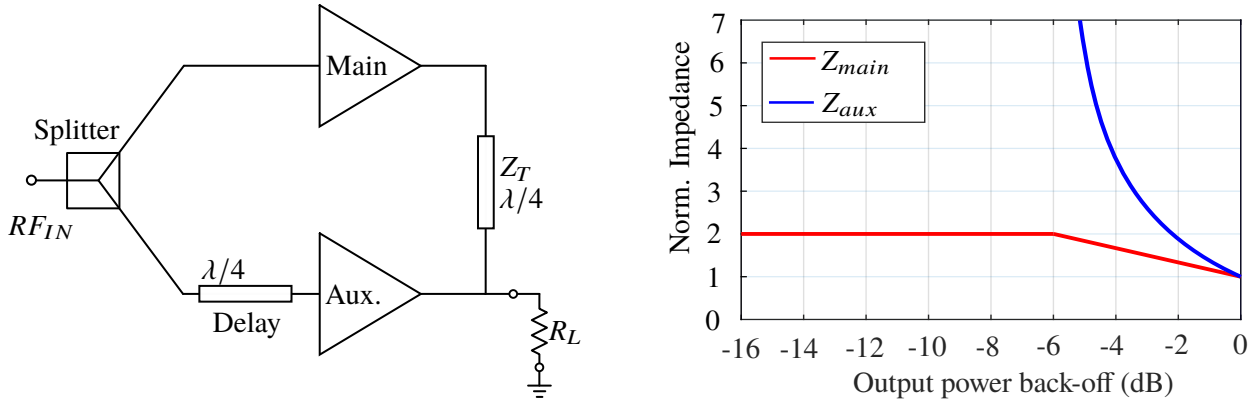
1.3 Efficiency Enhancement in PAs

An ideal class B PA yields the drain efficiency of $pi/4$ or 78.5%. Various techniques are implemented to achieve greater than 78.5% efficiency. The most common approaches which rely on constant dc supply and fixed load include overdriven PAs [7], harmonically tuned PAs such as class F [8] and inverse class F [9], switch-mode PAs such as class-D [10], class E [11–13] and inverse class E [14] and harmonically engineered PAs [15, 16] etc. The techniques which involve supply modulation include Envelope Elimination and Restoration (EER) [17, 18] and Envelope tracking [19, 20]. The next family of efficiency enhancement approach is based on the dynamic load modulation. The most prevalent example of this approach is the Doherty PA [21–23], with alternative techniques including outphasing [24–26] and direct load modulation [27–29]. These techniques, particularly the popular Doherty architecture, typically rely on narrowband matching structures that limit the achievable bandwidth.

Wideband Doherty PAs have also been demonstrated with, octave bandwidth by modifying the conventional quarter-wavelength transmission lines [30–32]. Similarly, wideband variations on outphasing power amplifiers have been explored [33], with up to 33% fractional bandwidth by absorbing the combining network structure into the matching network of the PA [34]. By employing more complicated digital signal separation, a continuum between Doherty and outphasing architectures can be exploited to further extend operating frequency beyond one octave, with 1-3 GHz operation demonstrated in [35]. Some of the commonly used efficiency enhancement techniques based on dynamic load modulation are summarized below. A detailed description of each of these technique can be found elsewhere.

1.3.1 Doherty PA

The Doherty PA (DPA) is one of the most commonly employed efficiency enhancement technique in modern base-station and broadcast transmitters. The DPA technique was first published in 1936 [21] for high-power tube amplifiers but is equally applicable in present-day wireless transmitters. The basic working principle of DPA exploits the concept of active load modulation in which two transistors interact with each other to improve the overall back-off efficiency. A second transistor usually termed as auxiliary or peaking transistor



(a) (b)

Figure 1.4: The Doherty PA (a) – Conceptual block diagram (b) – Load modulation of main transistor, auxiliary transistor.

is utilized to generate a signal which then modulates the load seen by the main (or carrier) transistor. The output combiner is designed such that the auxiliary transistor also undergoes load modulation based on the interaction with the main PA signal. The conceptual block diagram of the DPA is illustrated in Fig. 1.4 (a).

In the low power region, only the main transistor is active and the auxiliary is kept off until the input drive reaches a predefined level. This is typically realized by biasing the control PA in class-C. In this region, no load modulation takes place, and the main transistor biased in class-AB conducts linearly with input drive. In the high-power region, the auxiliary PA starts to conduct, modulating the load seen by the main transistor. This ensures that maximum voltage swing is maintained at the main transistor throughout the high power region, maintaining optimum efficiency for the main transistor. As the input drive increases, the auxiliary transistor also experiences load modulation through the current generated by the main transistor. The output combining network, a quarter wave transformer, ensures that both the transistor see optimum load impedance at the peak power. Fig. 1.4 (b) shows the load modulation experienced by the main and auxiliary PA in DPA.

1.3.2 Outphasing

Another prominent efficiency enhancement technique is the outphasing. The idea of outphasing was first introduced by Henri Chireix in 1935 [24] and a related technique was reinvented by D.C. Cox in 1974 [25]

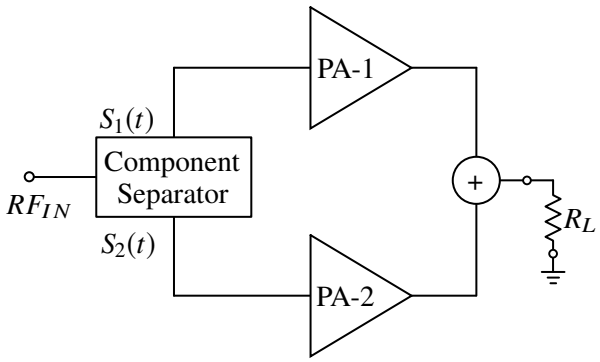


Figure 1.5: Conceptual block diagram of the Outphasing PA.

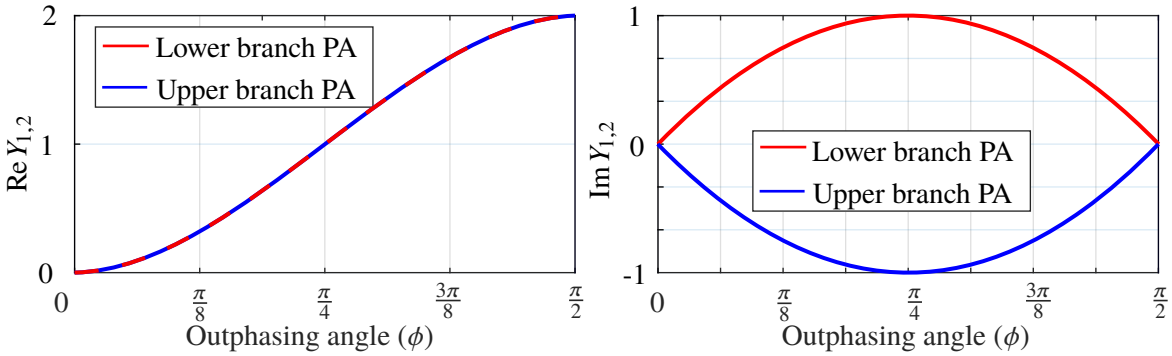


Figure 1.6: Load modulation in the outphasing PA as a function of outphasing angle (ϕ) (a) – real part of admittance, (a) – imaginary part of admittance.

under the title of Linear Amplification with Nonlinear Components (LINC). Outphasing PAs employ two constant envelope, phase-modulated signals which are then fed to the branch PAs, whose outputs are combined through a non-isolating combiner. Since the technique uses constant-envelope signals, in contrast to the DPA, highly efficient saturated PAs can be employed in the system.

A simple block diagram of the outphasing concept is shown in Fig. 1.5. Load modulation of the PAs occurs through the non-isolating combining network. The network is designed in such a way that the amplitude information encoded in the phase modulation is converted back into the amplitude, producing an amplified version of the original signal. The load seen by each of branch PAs and hence the generated output power can be controlled by the relative phase of the signal also known as the outphasing angle (ϕ). The reactive loading experienced by the branch PA can be compensated by adding opposite reactances in the respective branches, as proposed in the original paper [24]. Fig. 1.5 shows the admittance seen by the two

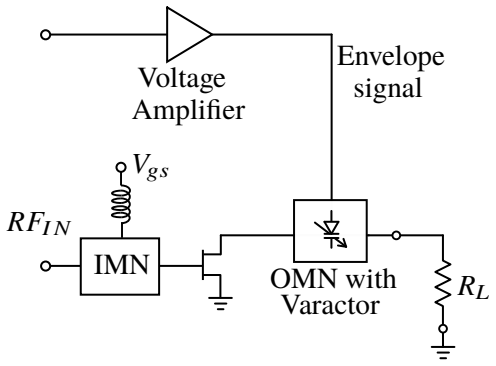


Figure 1.7: Conceptual block diagram of Varactor-based Load Modulation.

branch PAs in the outphasing PA.

A limitation in conventional outphasing systems, however, is that the two PAs see different loading trajectories leading to performance mismatch in the two paths. This suboptimal loading has been improved by using four PA paths instead of the conventional two [36, 37] but at the expense of complexity.

1.3.3 Varactor-based Load Modulation

Dynamic load modulation (DLM), as it was coined by Raab in his original paper is 2003 [27], is a technique of modulating the load using a voltage-sensitive reactive element. In his original demonstration, Raab used multiple MOSFETs as a tunable capacitive element (varactor) in the output matching network (OMN) to control the load seen by the class-E PA.

Varactor-based DLM operation is illustrated in Fig. 1.7. In general, the reactance of the varactor is tuned by the voltage across it. The voltage is controlled by a highly efficient voltage amplifier which operates at the envelope frequency of the signal. Such voltage amplifiers generate less power compared to the total output power fo the DLM and hence have minimal effect on the total efficiency of the system. By accurately tuning the varactor based on the envelope of the signal, significant improvement in the efficiency can be obtained. However, breakdown voltage of the varactor limits the use of this technique in high power applications.

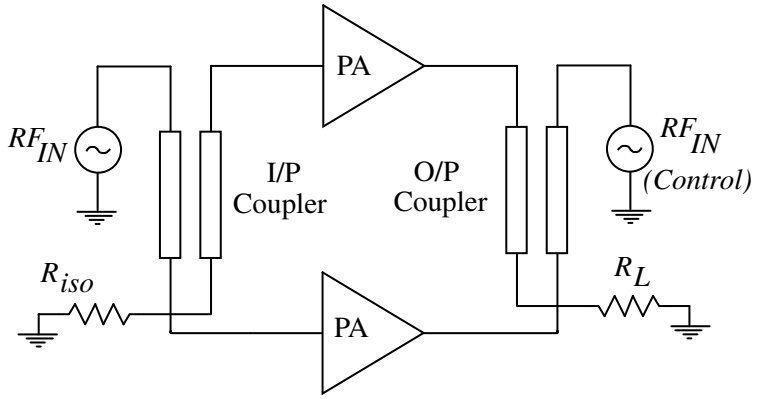


Figure 1.8: Simplified block diagram of the LMBA architecture [38].

1.4 Load Modulated Balanced Amplifier

The Load Modulated Balanced Amplifier, commonly referred to as LMBA, is a recent addition to the existing load modulation architectures. The LMBA was first proposed by Cripps in 2016 [38] as an efficiency enhancement technique that provides active load modulation over a wide OBO range and wide bandwidth.

As the name suggests, the LMBA is based on a conventional balanced amplifier architecture [39], with two transistors combined through quadrature hybrid couplers at the input and output. Fig. 1.8 shows the basic block diagram of the LMBA architecture. The LMBA differs from a balanced amplifier in that, instead of terminating the isolated port of the output coupler, a control signal is injected into it. The injected control signal is used to produce an active match for the two transistors, replacing a conventional passive output matching network. Because of the horizontal and vertical symmetry of the quadrature coupler, the injected signal is divided in half and appears at the drain of the PA in each branch. This signal then interacts with the output generated by the PA to present a load impedance to the drain. As proposed in the original paper [38], the control signal is generated externally from a second coherent RF source. Although it appears counter-intuitive, the injected control power gets fully recovered at the load of the system.

The advantages of the LMBA over other techniques such as DPA and outphasing PAs are as follows:

- Both the transistors are modulated with the same load impedance. This can be explained by noting that the two signals at the drain of the transistors are equal in magnitude and quadrature in phase, while

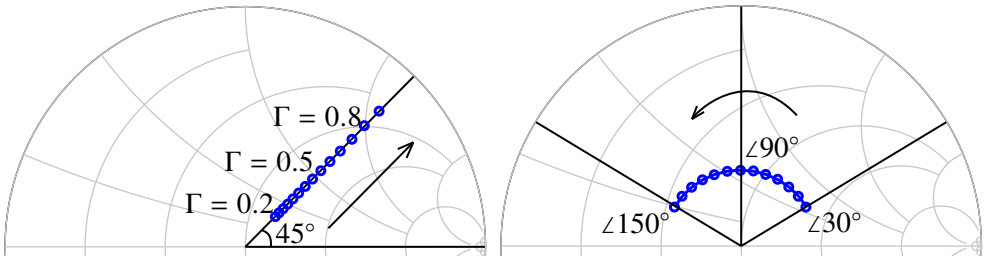


Figure 1.9: Effect of control signal on the load impedance seen by the two main transistors: (a) – as the magnitude of the control power increases, (b) – as the phase of the control power increases.

the control signal (after division into equal halves) also has a quadrature phase difference. Therefore, at the drain of each PA, the output signal interacts with the appropriately "phased" control signal to produce the same impedance at the drain of both the PAs.

- The output combiner of the LMBA can be wideband. The conventional DPA and outphasing PA use a narrowband output combiner which is the band-limiting component in both of these architectures. The LMBA uses a coupler as the output combiner which can be wideband depending upon the implementation. For example, a Lange coupler can easily provide over an octave bandwidth.

- By properly controlling the amplitude and phase of the control signal, both the transistors can be matched to any arbitrary impedance on the Smith chart.

1.4.1 Load control in LMBA

A qualitative relationship between the magnitude and phase of the control signal and the effective loading on the two transistors can be explained with help of the reflection coefficient (Γ). In general, for an N-port RF network, the Γ at port i can be defined in terms of the normalized voltage waves, a_i and b_i as follows [40]:

$$\Gamma = \frac{b_i}{a_i} \tag{1.1}$$

where $a_i = \frac{V_i^+}{\sqrt{Z_{0i}}}$ and $b_i = \frac{V_i^-}{\sqrt{Z_{0i}}}$. Here a_i is the forward propagating (transmitted) wave amplitude and b_i is the backward propagating (reflected) wave amplitude. Typically, a_i's and b_i's are complex numbers. $V_i^{\pm}$ are RMS voltages, and Z_{0i} is a real normalizing impedance.

From the perspective of the main transistor, the injected control signal appears as a reflected signal, and the signal generated by the transistor is the transmitted signal. In this way, by controlling the magnitude and phase of the control signal with respect to the main transistor signal the Γ or load seen by the main transistor can be controlled.

Fig. 1.9 illustrates the effect of the control signal on the load control. For ease of understanding, the load control mechanism is broken into two parts– magnitude control and phase control. In the rest of the thesis, the same style of explanation is presented for various proposed load control/modulation strategies.

The magnitude aspect of load control is shown in Fig. 1.9(a). Here, the relative phase of the control signal is held fixed. As the magnitude of the control power ($|P_{\text{ctrl}}|$) with respect to the power generated by the main transistor ($|P_{\text{main}}|$) increases, the $|\Gamma|$ presented to the main transistor increases.

In Fig. 1.9(b) the phase aspect of the load control is shown. In this case, the relative magnitude of the control power is held fixed. As the phase of the control power ($\angle P_{\text{ctrl}}$) with respect to the phase of main transistor power ($\angle P_{\text{main}}$) increases, the $\angle\Gamma$ presented to the main transistor rotates counter-clockwise in the Smith Chart.

1.5 Thesis Objective

As with some of the efficiency enhancement techniques (e.g., conventional outphasing and EER [17]), the LMBA as described in [38, 41] does not operate directly on a modulated RF input. Instead, an external control signal is required to provide the efficiency enhancement. This property makes the architecture less attractive compared to a wideband DPA approach with its ability to operate directly on a single modulated input. The objective of this thesis work is to eliminate the externally generated control signal such that the PA can be easily integrated with the rest of the transmitter without requiring any additional signal computation. In addition to developing an RF-input LMBA, another objective of this work is to utilize the control signal to achieve high back-off efficiency over a wide dynamic range while maintaining wideband performance.

1.6 Thesis Organization

Chapter 2 explains the first prototype of the RF-input LMBA. A new amplitude control strategy is proposed which eliminates the second RF source, while at the same time enhancing the system efficiency at the desired back-off level. The chapter presents measurement results of the proof-of-concept 800 MHz prototype.

Chapter 3 explains the octaveband LMBA. This work extends the control signal generation approach to include the automatic generation of the correct frequency-dependent phase, enabling greater than octave-bandwidth operation. The chapter also discusses the simulation and measurement results of the prototype PA which operates from 1.8-3.8 GHz.

Chapter 4 presents a new variant on the RF-input LMBA architecture, the Doherty-like load modulated balanced amplifier (D-LMBA). This architecture uses a class-C biased control PA that functions analogously to the auxiliary amplifier of a Doherty Power Amplifier (DPA), and a balanced amplifier that functions analogously to the main amplifier of a DPA. The chapter compares the measurement results of 800 MHz prototype of D-LMBA with that of RF-input LMBA presented in Chapter 2.

Chapter 5 extends the empirical approach presented in Chapter 4. This chapter primarily focuses on the theoretical aspects of Doherty-Like Load Modulated Balanced Amplifier. It derives the design equations for the system-level parameters of D-LMBA, i.e., the input power-splitting ratio, transistor scaling ratio, supply voltages, and so on. The design equations are derived in terms of transistor parameters and dynamic range of efficiency enhancement, simplifying the D-LMBA PA design procedure.

Chapter 6 presents the thesis conclusions, potential improvements, and future work to extend the research.

1.7 Thesis contributions

The research work has proposed three different PA architectures which has resulted in a filing of US Patent [42], three IEEE transactions journals [43–45], two conference proceedings [46,47] and a nomination for the best student paper award at IEEE International Microwave Symposium (IMS) [46].

Chapter 2

RF-input Load Modulated Balanced Amplifier

The previous chapter has given a detailed discussion of the Load Modulated balanced Amplifier (LMBA) using an externally generated control signal. In most communication systems however, the PA must be operated from a single RF input so that no baseband signal computation is required for the modulated signal. This chapter presents the first prototype of the novel RF-input LMBA architecture. The theory presented in the previous chapter is extended by proposing a new amplitude control strategy which enhances the system efficiency at the desired back-off level. The chapter first discusses the mechanism of generating the control signal from a single RF source, followed by a discussion on hardware implementation and lastly presents measurement results.

2.1 Control Signal Generation from modulated RF input

Automatic control signal generation from the RF input is separated into two components, amplitude modulation and phase control. The architecture is drafted such that the designs of these components can be treated independently. In this section, first the amplitude control is presented and then a constant phase control is discussed.

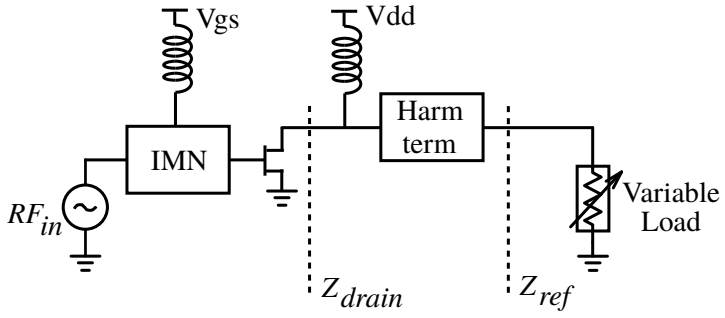


Figure 2.1: Schematic of the main PA subjected to load-pull simulations, showing Z_{drain} and Z_{ref} planes.

2.1.1 Amplitude control for load modulation

From the theory presented in Section 1.2, for back-off efficiency improvement the load presented to the main PAs in the balanced amplifier need to be modulated such that the maximum voltage swing across the output of device (V_{ds}) is maintained throughout the power back-off. One way of determining the optimum impedance at each power level is to use the load-line theory [48]. This theory calculates the optimum impedance at the current generator plane of the transistor. However, in the case of a discrete packaged transistor, the impedance seen at the intrinsic (current generator) plane is different from the impedance seen at the extrinsic (package) plane. Therefore, instead of relying on the load-line theory, load-pull data is used to determine the optimum load impedances. In this work, the load-pull data is acquired from simulations performed in the Advanced Design System (ADS). A packaged transistor device model provided by the manufacturer is utilized in the simulations.

Fig. 2.1 shows the simplified circuit of the main PA for load-pull simulations. The target load impedances are found at the Z_{ref} plane, shown with a dashed line. In the simulations, a 10-watt GaN device from Wolfspeed is chosen as the main PA transistor and is biased in class B. The transistor is conjugately matched on the input side while on the output side a bias network and a harmonic termination network is added. The harmonic termination network short circuits higher harmonics, producing class B waveforms at the Z_{drain} plane. The simulation results are plotted in Fig. 2.2. To emulate a power back-off scenario, the PAE contours are plotted at various output power back-off levels by reducing the RF-input drive level. The plot shows the trend of movement of target load impedances as the power is backed off.

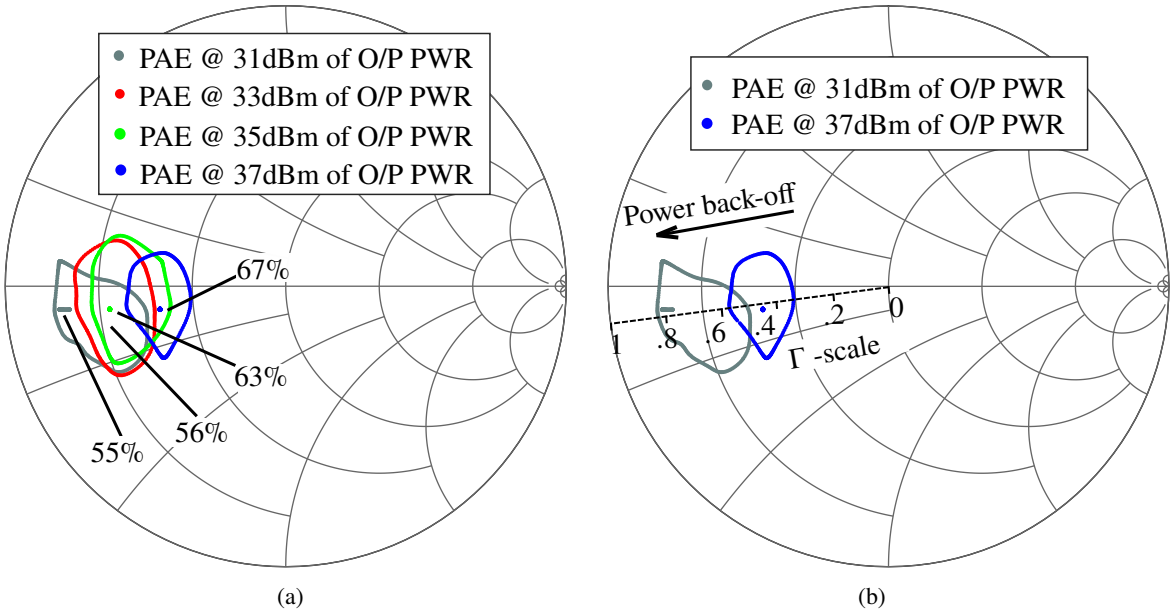


Figure 2.2: RF-input LMBA simulation results : (a) – PAE Contours at corresponding output backoff power, and (b) – PAE Contours highlighting inverse relationship between Γ_L and output power.

Fig. 2.2 (b) further extends the load trajectory analysis. PAE contours corresponding to peak power of 37 dBm (blue) and 6dB back-off power of 31 dBm (gray) are plotted with reference to reflection coefficient (Γ) scale. The plot suggests that for the main PA, the peak target load occurs at a lower magnitude of Γ, whereas the back-off target load occurs at a higher magnitude of Γ.

The results from load-pull suggest that to maintain high efficiency throughout the back-off range, as the input drive increases, the Γ seen by the main transistor should decrease. In other words, the control signal amplitude relative to the main signal amplitude should be reduced as the main path power increases. This is in compliance with the magnitude control theory of LMBA, which states that a lower magnitude of Γ can be obtained at the main transistor by reducing the control signal amplitude ($|P_{\text{ctrl}}|$) relative to the main signal [Section 1.4.1].

This inverse relationship is difficult to implement using RF circuit techniques. It is important to note, however, that it is the *relative* amplitude of the control signal power that must decrease compared to the total output power. That is, the control signal power does not need to decrease in an absolute sense. To implement this relationship, we exploit the compression characteristic of a PA to create an input power

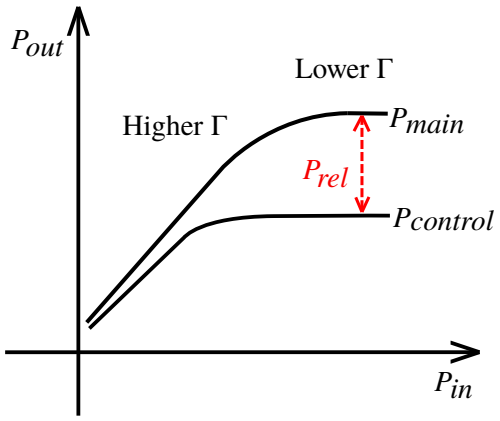


Figure 2.3: Proposed output power profiles for the control PA and the main PA to achieve efficiency enhancement in output power back-off.

dependent control power profile. This approach is illustrated in Fig. 2.3. The control path is inserted with a so called 'control PA', which saturates at a lower power level so that the relative power P_{rel} decreases with input drive, as desired. The term P_{rel} is defined as the ratio of the main PA output power to the control power, $P_{rel} = P_{main}/P_{ctrl}$, and determined by the input power level, the relative sizing of the main and control PAs, and the weighting of the input splitter. The different saturation characteristics in the two branches are implemented by using differently-sized packaged transistors. To achieve this characteristic, the control power should be saturated before the main power.

2.1.2 Phase Control

The relative phase of the control signal with respect to the output of the main PAs is critical to ensure that the impedance trajectory overlaps with the target load impedances for the main PAs. In the proof-of-concept design presented in this chapter, the control path phase is set using the transmission line length at the input to the control PA in the simulation. If desired, a phase tuner can be inserted before the input to the control PA and used to rotate the load trajectory seen by the main PAs. This phase adjustment is more practical than offset line adjustment in a conventional outphasing architecture, as it can be performed on the low-power input signal.

Although in this work the phase control strategy is narrowband it is noted that the wide bandwidth offered

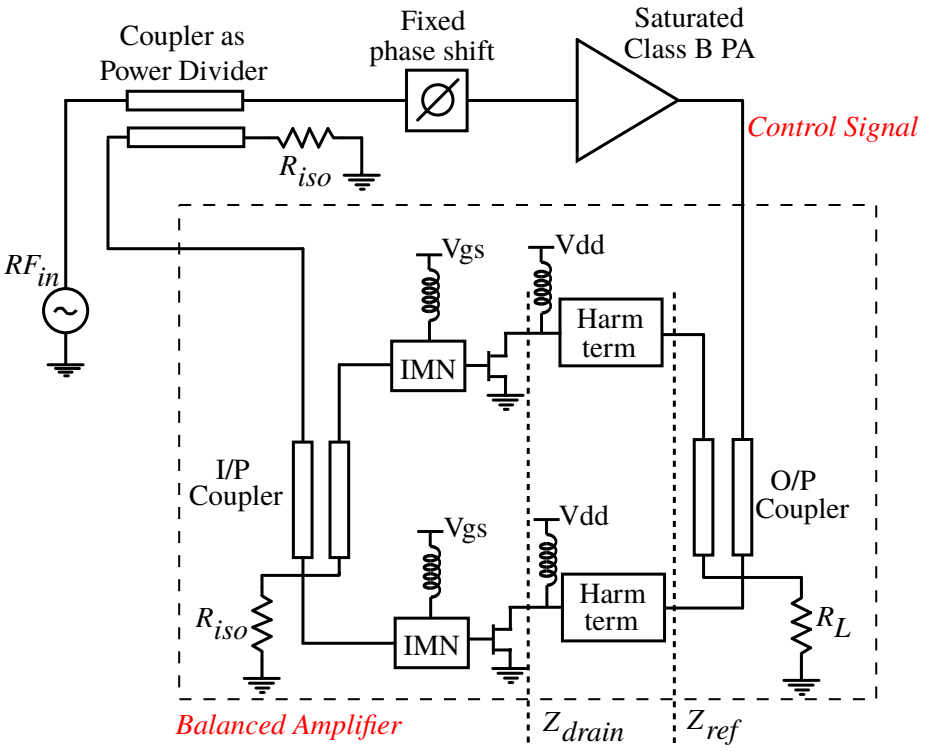


Figure 2.4: A complete block diagram of the proposed RF-input LMBA.

by the original approach in [38] can be achievable in RF-input form by controlling the phase response over the frequency. This frequency-dependent phase control aspect is explored and successfully implemented in Chapter 3 to achieve greater than octave bandwidth.

2.2 RF-input LMBA Architecture

The complete block diagram of the RF-input LMBA is shown in Fig. 2.4. The input RF signal is divided into two equal halves by a 3-dB hybrid coupler. One half of the signal part forms the input to the control PA whereas the other half forms the input to the balanced amplifier. Next, the control signal is phase shifted, using a passive element to provide a relative phase shift between the control and main paths. The phase shifted control signal is then amplified by the control PA. The control PA is biased in saturated class B to provide the required amplitude profile. We note that the dynamic range of load modulation of RF-input LMBA is decided by the power level at which the control PA starts to saturate (as described in Section 2.1.1).

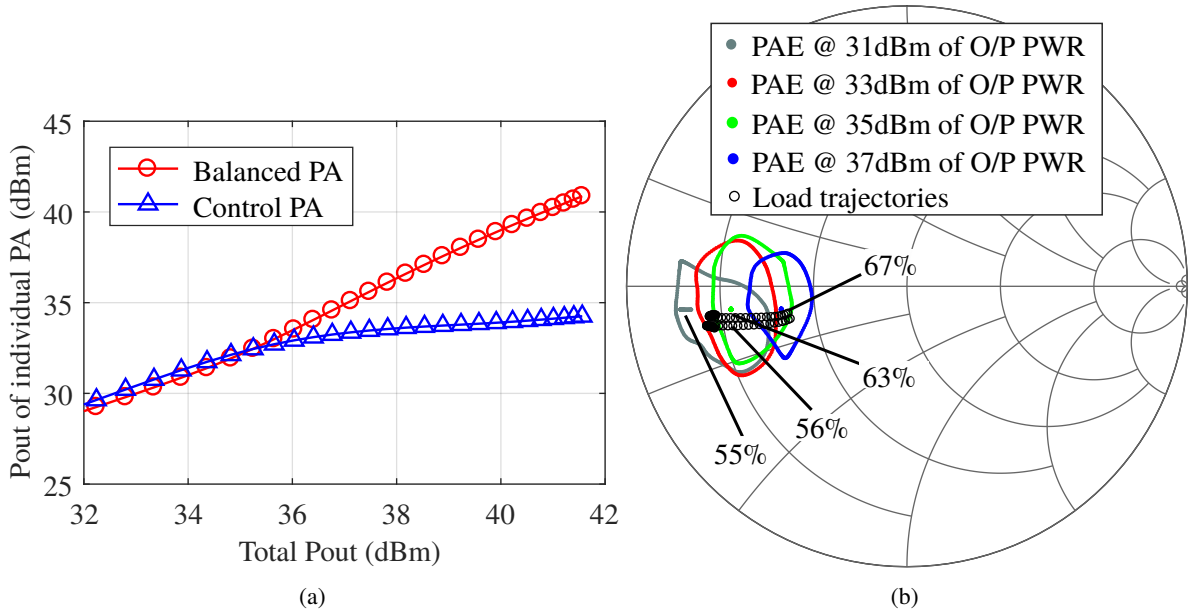


Figure 2.5: Load-pull simulation results of RF-input LMBA : (a) – output power profiles for the control PA and the main PA , and (b) – Load trajectories following desired optimum impedances as the output power backs off.

Further, we note that the extent of saturation of the control PA depends on the relative size of the transistor as well as the drain supply voltage (V_{DD}). In this prototype, in order to achieve a 6-dB of dynamic range, the relative size of the control transistor and the optimum value of V_{DD} is found empirically.

The balanced amplifier is shown in the dashed box in Fig. 2.4. It consists of two identical couplers and two identical main PAs. The main PAs are conjugately matched on the input, whereas a dynamic output match is obtained by the control signal injected through the output coupler. Both the main transistors are biased in class B. In addition to the bias network at the drain, harmonic terminations are added to ensure class B type waveforms.

Fig. 2.5 shows the load-pull simulation results of the RF-input LMBA. The left hand side plot shows output power profiles for the control PA and the main PA. The control PA starts to compress at around 6-dB back-off power, suggesting that the load modulation starts at 6 dB back-off. The right hand side plot shows load trajectories (hollow circle markers) following the desired optimum impedances as the output power backs off.

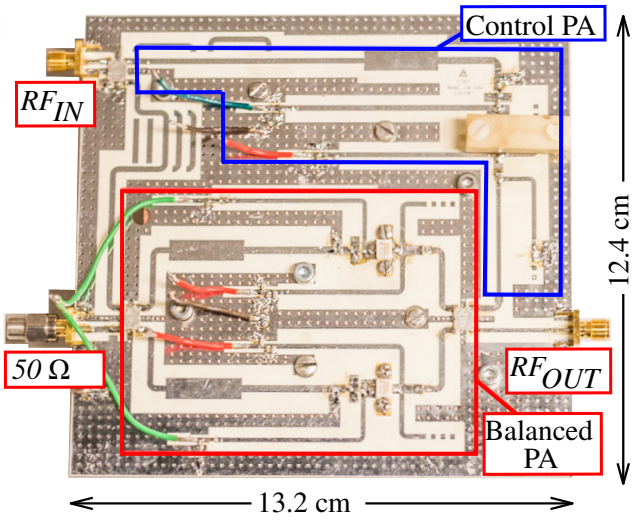


Figure 2.6: Photograph of the proof-of-concept RF-input LMBA.

2.3 RF-input LMBA Prototype Design

The proof-of-concept prototype is designed to operate over 700-850 MHz. A Wolfspeed CGH40010 (10 W) packaged GaN device is chosen for the main PAs whereas Wolfspeed CGH40006 (6 W) packaged device is chosen for the control PA. The 90° hybrid couplers are implemented using part no. X3C07P1-03S from Anaren. The same hybrid coupler is used as the power divider at the input. The phase shift between the control and main paths is implemented by a simple transmission line. The isolation port of the input coupler is made accessible by terminating it with an SMA connector. The port can be used to monitor the power reflections arising from input mismatch of the main PAs. For normal operation, the port is terminated with 50 Ω. The entire RF-input LMBA architecture was implemented on a 30-mil thick Rogers R04530 substrate, measuring approximately 13.2 cm by 12.4 cm. A photograph of the RF-input LMBA is shown in Fig. 2.6. The control PA is shown in the blue box on the top and the balanced amplifier is shown in the red box on the bottom left part.

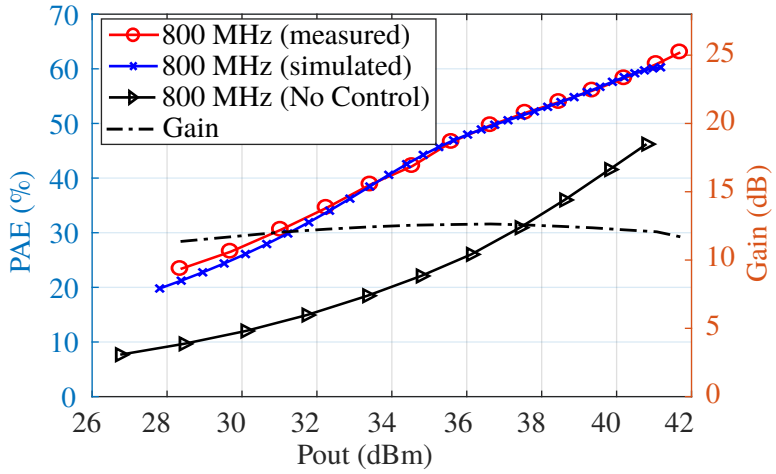


Figure 2.7: Measured (circle marker) and simulated (x marker) performance of the RF-input LMBA at 800 MHz. The lower line (triangle marker) shows the measured performance when the control PA is turned off.

2.4 Measurements

The CW PAE of the entire RF-input LMBA, measured at 800 MHz is shown in Fig. 2.7. For direct comparison, the simulated PAE is also plotted on the graph. Note that the PAE accounts for the power dissipated in both main and control paths i.e. it is the total PAE of the entire RF-input LMBA.

In order to analyze the effect of the control signal on the system performance, the system PAE is measured while the control signal is turned off, included in Fig. 2.7 (triangle markers). The comparison shows the advantage of this technique compared to a conventional class B balanced PA, in which the PAE drops off in proportion to the magnitude of the output voltage. We note that while the control is turned off, the balanced PA is poorly matched and hence the PAE is lower than for a matched design. Nonetheless the purpose of this experiment is to compare the shapes of the efficiency vs. output power plots to highlight the advantages of control signal injection.

At 800 MHz, the prototype shows the peak PAE of 63% at peak CW power of 41.7 dBm and PAE of 47% at 6 dB back-off. The gain of the system is measured to be 12 dB and is shown with the dashed line in Fig. 2.7. Fig. 2.8 shows the RF-input LMBA performance over 650-850 MHz frequency at different back-off levels. The prototype shows $\geq$ 30% PAE at 6 dB back-off over 700-850 MHz, giving a fractional bandwidth

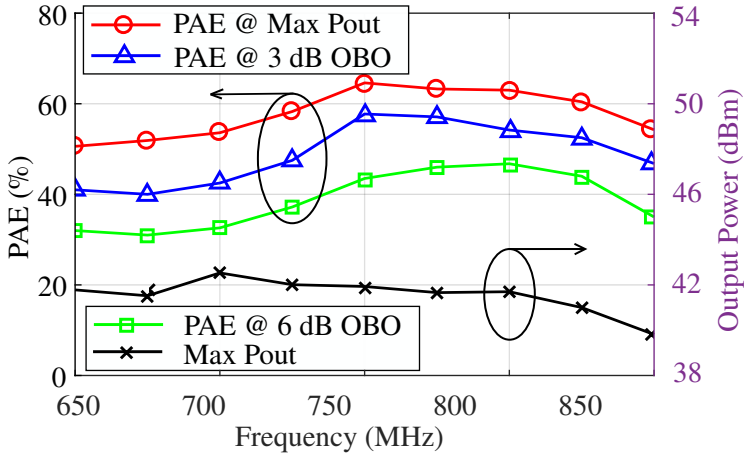


Figure 2.8: Measured LMBA performance across a 650-850 MHz frequency range.

of 19%.

The modulated signal performance of the prototype was tested using a W-CDMA signal with 3.84 MHz bandwidth and 10 dB (measured) PAPR centered at 800 MHz. The output spectrum is given in Fig. 2.9. The average efficiency for the 32.8 dBm output power signal was 32.57%, with worst case ACLR of 26.8 dB. No pre-distortion is applied for this measurement. In principle, however, this topology could be used directly in a conventional DPD system due to its single RF input.

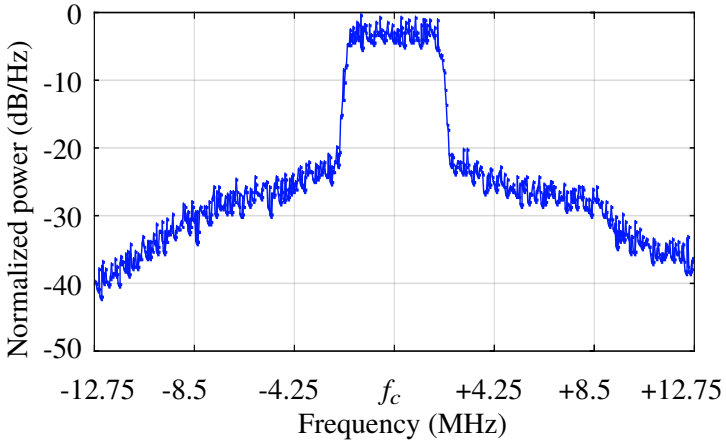


Figure 2.9: Modulated performance using a 3.84 MHz W-CDMA signal centered at 800 MHz with a PAPR of 10 dB. The average efficiency for the 32.8 dBm output power signal was 32.57%, with worst case ACLR of 26.8 dB.

2.5 Conclusion

A novel control signal generation methodology proposed in this work improves the back-off efficiency of a balanced amplifier by dynamically modulating the main PA load impedances. Moreover, it offers a variation of the LMBA approach that can operate directly on a modulated RF signal without requiring external control signal generation. The approach eliminates the baseband signal computation that would be required for modulated signals in the previously reported LMBA implementation [38].

In addition to the relative simplicity of the approach, one potential benefit is that it avoids nonlinear baseband signal computation and any associated bandwidth expansion. Compared to the original LMBA described in [38], the simplicity of the RF-input approach trades off with the wide-range load impedance control offered by an externally generated control signal. The proof-of-concept prototype demonstrates the basic feasibility of our approach.

Chapter 3

Octaveband Load Modulated Balanced Amplifier

In the last few decades, mobile wireless standards have undergone tremendous reforms to support ever-increasing demands of high data rate, low latency and an increasing number of customers. As the standards have evolved from 1G to 5G, the design challenges of wireless transmitters have become more difficult. The stringent specifications of next-gen modulation signals require the transmitter to be linear, high power and energy efficient. Additionally, wireless transmitters are required to operate over a wide range of frequencies in order to support multiple bands. All these demands require the PA to be linear, energy efficient and wide-band.

The RF-input LMBA presented in the previous chapter was designed to operate over a narrow band. The dynamic load modulation implemented in the previous prototype considered only a amplitude modulation of the control signal whereas the phase of the control signal was set to a fixed value. One of the significant advantages of the original LMBA [38], i.e. wideband operation, was not explored in the RF-input LMBA. This work extends the control signal generation approach to include the automatic generation of the correct frequency-dependent phase, enabling greater than octave-bandwidth operation.

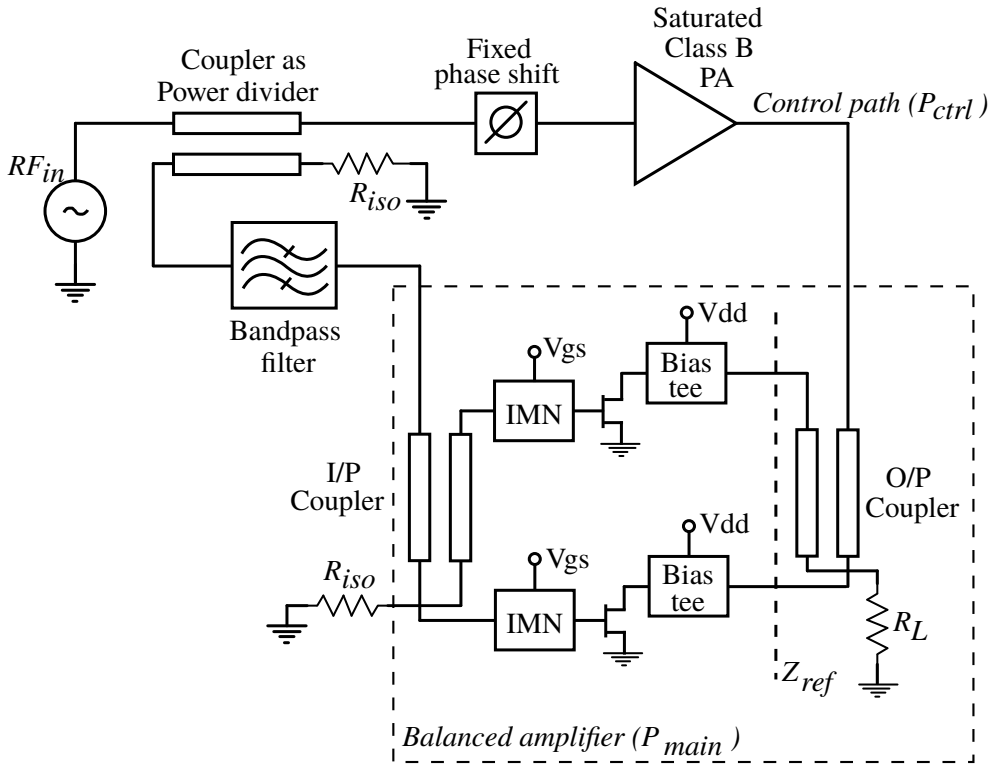


Figure 3.1: Simplified diagram of the wideband RF-input LMBA. The relative amplitude and phase of the control signal injected into the balanced amplifier isolation port are controlled by the relative PA compression characteristics of the control path and the relative phase introduced by the band-pass filter, respectively.

The chapter is organized as follows. First, a novel phase control approach for wideband operation is described. Next, the design of a new wideband RF-input LMBA prototype is described in detail. Finally, the chapter concludes with the measured performance of the octave-bandwidth prototype including with modulated signals and conclusion.

3.1 Control Signal Generation from modulated RF input

Similar to the RF-input LMBA architecture, in the Octaveband LMBA the control signal is derived from the input RF signal. The operation can be separated into two components, amplitude control and phase control. The amplitude component of the control is devised to modulate with respect to the input power to provide an efficiency match over the back-off range, whereas the phase component is devised to modulate with the frequency to provide an efficiency match over a wide bandwidth. Although the amplitude and phase

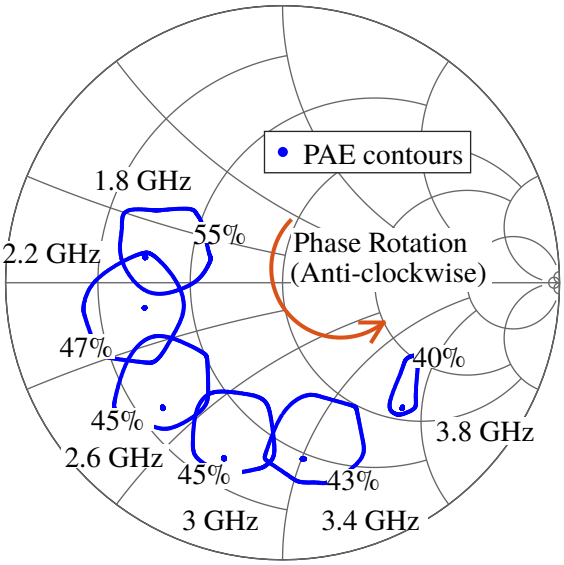


Figure 3.2: Frequency variation over 1.8–3.8 GHz of the optimal PAE contours for the main PA, which comprises a 10 W device, bias tee, and short interconnect length to reach the coupler. The counter-clockwise rotation makes matching with conventional passive components challenging.

components of the control signal are modulated independently, the overall effect of these components on the performance of the system is additive.

3.1.1 Amplitude control for back-off efficiency

The amplitude of the control signal is modulated using the same mechanism as that of RF-input LMBA. The input power dependent control profile as proposed in Fig. 2.3 is obtained by introducing a saturated PA in the control path. A detailed explanation of the amplitude control is discussed in Section 2.1.1.

3.1.2 Phase control for Wideband operation

The primary challenge in wideband PA design is that the load impedance corresponding to peak efficiency tracks counter-clockwise in the Smith Chart, while passive elements used for matching are dispersive (rotate clockwise). An example set of load pull simulations for the main PAs used in the experimental validation is shown in Fig. 3.2, illustrating the counter-clockwise rotation of the peak PAE and the PAE contours. PAE contours are used here as the target impedances because the focus of this work is on efficiency at back-off; in the experimental work [Section 3.3] it is shown that the peak output power is also maintained within

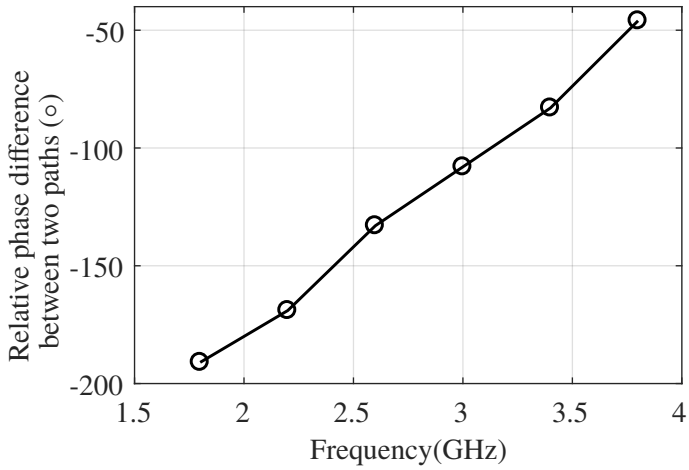
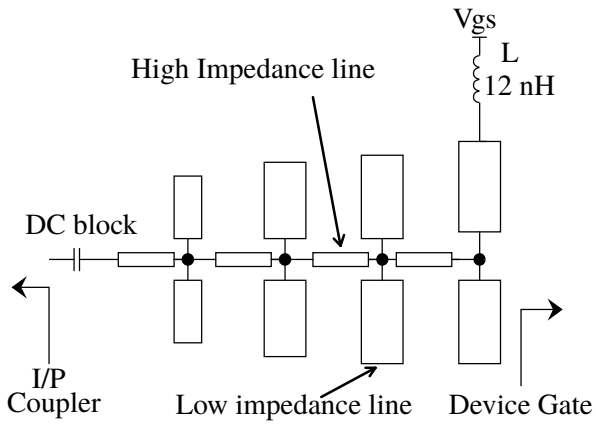


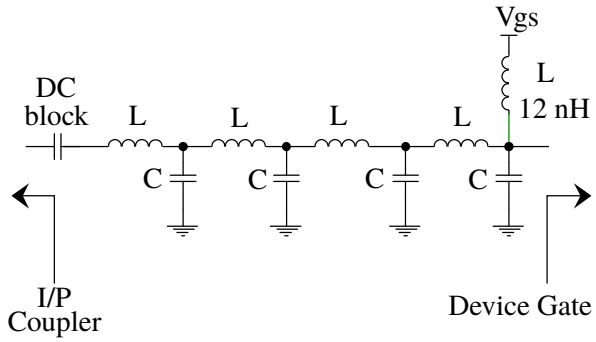
Figure 3.3: Frequency-dependent phase shift required for the control signal to match the counter-clockwide optimal load rotation shown in Fig. 3.2. This phase characteristic is implemented in our prototype using a bandpass filter.

approximately 1 dB across the band. The main PAs, in this case, comprise the Wolfspeed CGH40010F GaN device, a simple bias tee, and a microstrip interconnect (which contributes dispersion in addition to that of the device alone). The counter-clockwise rotation can be understood simplistically as resulting from the device output capacitance: the magnitude of this shunt reactance decreases with frequency, requiring the compensating inductive load to decrease. In practice, any additional frequency-dependent phase in the PA's output matching network will affect how rapidly this rotation occurs with frequency.

To track the optimal PAE point as it rotates counter-clockwise, the control signal phase must increase with frequency (see Fig. 1.8). As with the amplitude control approach described in Section 3.1.1, it is the *relative* phase of the two paths that must be controlled. Therefore, two possibilities are to use a non-Foster network in the control path, so that its phase increases with frequency, or to insert additional negative phase shift in the main PA paths such that the phase of these paths decreases more quickly with frequency. In each case, the relative phase of the control path will increase with frequency. The latter approach is analogous to that used in Chapter 2 for amplitude control, in which the relative power of the control signal is increased by shaping the control path's compression characteristics. We will focus on this method here, but note that the overall system may have increased dispersion due to the phase compensation, making it unsuitable for very wideband instantaneous signals.



(a) Low-pass prototype network topology.



(b) Equivalent distributed element network.

Figure 3.4: Input matching network of the balanced amplifier.

In order to generate the correct control signal phase response without affecting the amplitude control, a Butterworth bandpass filter is used. The filter's passband encompasses the frequency range of interest while the filter order and topology determines the frequency-dependent phase characteristic. As shown in Fig. 3.3, we can find the desired phase characteristic based on the load pull of the device. In practice, any existing dispersion in the other networks (control PA, interconnects, etc.) must also be considered and compensated for. The topology selection and design of the compensating filter for the experimental prototype is described in Section 3.2.

3.2 Wideband RF-input LMBA Design

3.2.1 Main path balanced PA

The balanced PA design includes design of the matching network at the input and the bias tee at the output. Both the PAs are identical and are biased at the same drain current to ensure they will be subjected to identical load modulation. Commercial off-the-shelf couplers (XMC0204F1-03 from Anaren) are used for the balanced amplifier as well as the input split.

3.2.1a Input match

A multi-stage low pass matching network based on transmission lines has been used in many broadband PAs [49], [50]. Design of such networks can be done based on low pass prototypes [51], [52]. A methodology suggested in [52] was followed for designing the input matching network to operate over the band of 1.8 GHz to 4 GHz. This work uses a four stage low pass filter topology to realize the input matching network, with each stage consisting of a series L and shunt C element. The element values of each stage are found from the tables given in [53]. Fig 3.4(a) shows the low-pass filter topology used in the input matching network. The matching network is implemented by converting the lumped element values into distributed ones in order to accurately realize the required element values. The series inductor is realized with a high impedance line, whereas the shunt C is realized by two parallel open circuited stubs as shown in Fig 3.4(b). The gate bias network is implemented with a dc blocking capacitor at the first stage of the network and an RF choke inductor at the fourth stage of the network. The final lengths and widths of the stubs are tuned in order to absorb the parasitics of the RF and dc block as well as the device packaging.

3.2.1b Output match and bias tee

In the octave-bandwidth RF-input LMBA architecture, any matching network at the main PA output must operate over the entire octave band and would add uneven phase dispersion in the main path. This uneven phase dispersion inhibits the phase tracking and is therefore undesirable. Therefore, in our design the transistor is not matched and only a bias tee is included at the output. If the control PA is turned off, both

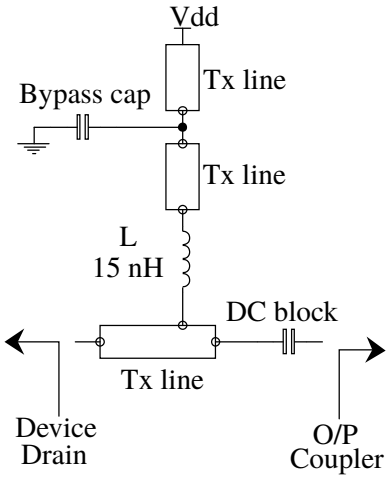


Figure 3.5: Schematic of output match of the balanced amplifier.

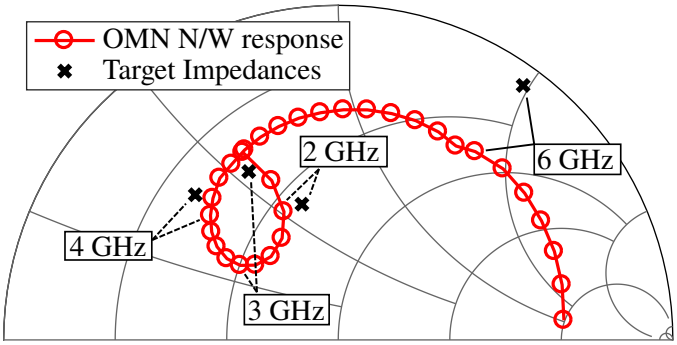


Figure 3.6: Output network response of the control PA (shown with 'o' marker) with corresponding target impedances (shown with 'x' marker).

of the main PAs simply see the bias tee followed by an unterminated coupler at the output. In other words, the main PAs will be poorly matched at the output in the absence of a control signal. The correct load will be presented to both the PAs only when the control signal is active. This approach is also used in previous LMBA implementations [38, 41, 46].

The schematic of the bias tee is at the output is shown in Fig 3.5. The 15 nH RF block is realized using a Coilcraft high self resonance frequency (SRF), low series resistance (ESR) inductor. The dc block is implemented with a 120 pF Murata capacitor. Based on the value of these lumped components, some phase is inevitably added in the main path; this phase must compensated for in the control path.

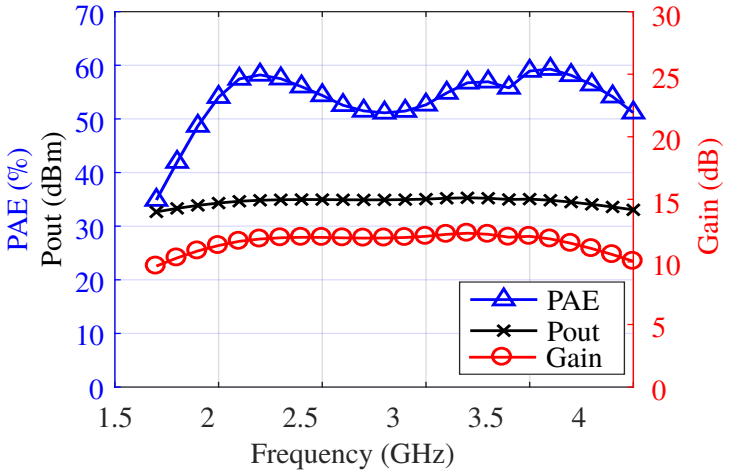


Figure 3.7: Simulated output power, gain and PAE of the wideband control PA with CW input of 20 dBm.

3.2.2 Control path PA

One challenge in the wideband LMBA architecture is that it requires a wideband PA for the control signal. In [41], the control path power is limited to 1 W (compared to the at least 39.5 dBm total output power), so that inefficiencies in the control signal generation will not significantly affect overall transmitter power. Here, we operate the control signal up 30 dBm, within 11–13 dB of the total output power.

To achieve wideband operation, simulated loadpull was performed on the 6 W Wolfspeed CGH40006P GaN transistor biased in class AB, operating with a quiescent drain current of 100 mA. Fundamental loadpull was performed at discrete frequencies in the 1.8–4 GHz band to determine optimum impedances for PAE. In addition, a second harmonic loadpull was simulated at $2f_0$, where f_0 is the center of the fundamental band (2.9 GHz), to further increase PAE over the operating frequency range. A nonuniform stepped impedance topology is used at the output of the device.

Due to the non-Foster behavior of the optimal output impedances, a perfect match over an octave bandwidth is difficult to achieve using passive components. A sensitivity analysis was therefore performed to determine the effect of less than optimal termination impedances. For this device, frequencies above 3 GHz are found to be more sensitive to load termination; therefore, more care is taken in matching in this range. A total of three sections of transmission line are used at the output to reduce complexity and enable optimization. Simulation of the output network as well as target impedances are shown in Fig. 3.6.

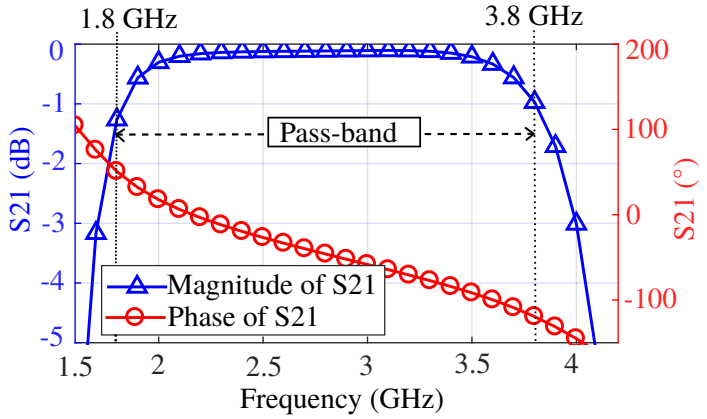


Figure 3.8: Simulated magnitude and phase response of the Butterworth bandpass filter.

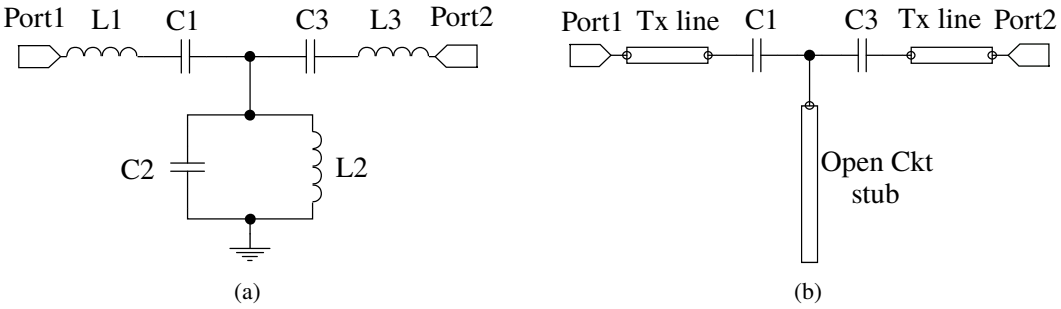


Figure 3.9: Butterworth filter implementation for phase compensation. (a) – Lumped componets; (b) – Transmission lines.

Source-pull of the device is performed with the output matching network attached over the bandwidth 1.8-4 GHz. The results are then used to synthesize a matching network at the input. It was observed that the matching ratio at the input is higher than that of the output. The gate bias network is absorbed into the input match to produce a hybrid wideband network at the input. The 6 watt transistor is operated at a 20 V supply, to keep it saturated (as mentioned in Section 3.1.1). This reduces the gain of the control PA, but keeps the control path efficiency high and generates right amount of control power for the dynamic load modulation to occur. Simulated output power, gain and power added efficiency of the control PA are shown in Fig. 3.7 for a CW input power of 30 dBm.

3.2.3 Frequency compensation filter

The key architectural difference between the RF-input LMBA [46] and the octave-bandwidth RF-input LMBA presented here is the bandpass filter. The filter response enables the broadband operation of the octave-band

LMBA by providing dispersion compensation. The phase response of the bandpass filter varies linearly over the frequency band, allowing the relative phase between the control and main path to vary dynamically as the frequency of operation is changed. The slope with which the phase of the filter varies (over frequency) can be controlled by three aspects of the filter: bandwidth, topology and order. For this prototype, a Butterworth topology was selected as it has flat response in the passband and minimal ripple. Ripple in the passband is avoided because it might interfere with the amplitude control.

The order of the filter is selected based on the required slope of the system. The dependence of the phase-slope on the filter order was utilized by the author previously in a demonstration of a dual-band Chireix combining network [54]. After setting the order of the filter, bandwidth of the filter can be selected to precisely tune the phase slope. The minimum limits on the bandwidth of the filter are set by the total bandwidth of the system. In order to fine tune the phase response, the only possibility is to increase the bandwidth of the filter. Here, the filter was designed to operate over a bandwidth of 1.8 to 3.8 GHz.

Fig. 3.8 shows the simulated overall filter performance. The passband attenuation is better than 0.2 dB. At the 1.8 GHz and 3.8 GHz (corner frequencies) of the filter the passband attenuation drops roughly by 1 dB. The phase response has a slope of negative 6.2 $^\circ$/100 MHz, which gives the required phase response to compensate for the frequency-dependent phase shift shown in Fig. 3.3 across the entire bandwidth. The right amount of phase slope tracks the load phase trajectory in the anti-clockwise direction to give broadband operation.

The wide bandwidth required makes the filter design a challenging task; as the bandwidth of the filter increases, the filter elements (whether lumped or distributed) become difficult to realize. In this prototype, a hybrid network of lumped and distributed components are utilized. Fig. 3.9 shows the implementation of the Butterworth filter used in our experimental prototype.

3.2.4 Simulated Wideband RF-input LMBA Performance

A photograph of the fabricated octave-bandwidth RF-input LMBA, measuring 6.7 cm $\times$ 8.3 cm is shown in Fig. 3.10. The PA's performance is simulated based on EM extraction and manufacturer-provided component models to validate the load trajectory control approach. In Fig. 3.11, the simulated load trajectories over

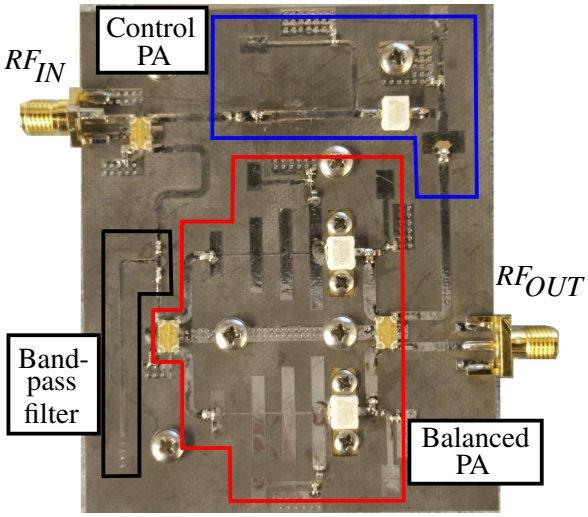


Figure 3.10: Photograph of the octave-bandwidth RF-input LMBA prototype, measuring 6.7×8.3 cm.

1.8–3.8 GHz are compared to the optimal PAE contours of the balanced amplifier device as frequency is swept. The load trajectories track the counter-clockwise rotation over the entire band. The extent of load modulation varies across the band due to variations in the control PA characteristics relative to those of the main balanced amplifier. As seen in Fig. 3.11, the design prioritizes load modulation at the high end of the band, where overall performance is expected to be lowest. The simulated performance in PAE, output power, and gain are shown in Figs. 3.12, 3.13, and 3.14. We note that in these simulations, as well as in the measured results in Section 3.3, the presented PAE includes consumption from all dc supplies. That is, the control PA power consumption is included in all of the presented numbers.

3.3 Experimental Results

The prototype of the octave-band RF-input LMBA was fabricated on Duroid-5880 having a dielectric constant of 2.2 and a thickness of 20 mils. Duroid-5880 was chosen to realize high impedance lines in the input matching network of the two main PAs as well as high impedance transfer ratios. The prototype was measured with CW and modulated input signals using the experimental setup shown in Fig. 3.15.

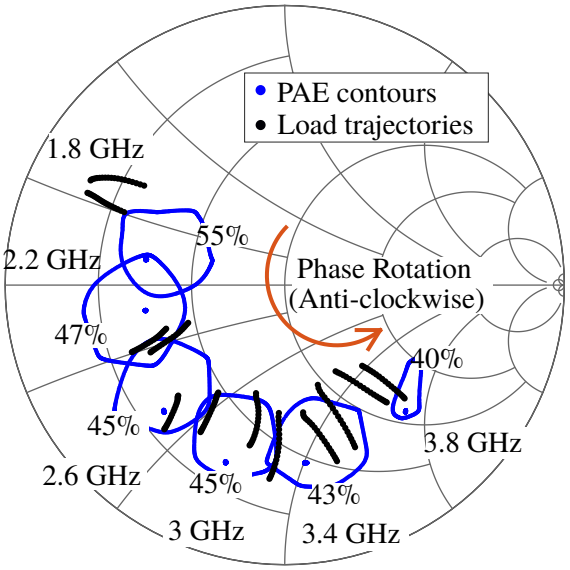


Figure 3.11: Frequency variation over 1.8-3.8 GHz of the optimal PAE contours for the device (blue contours), and the load trajectories of the balanced amplifier transistors (black trajectories) over the same frequency range. The load trajectories track the counter-clockwise rotation of the PAE targets over the octave band.

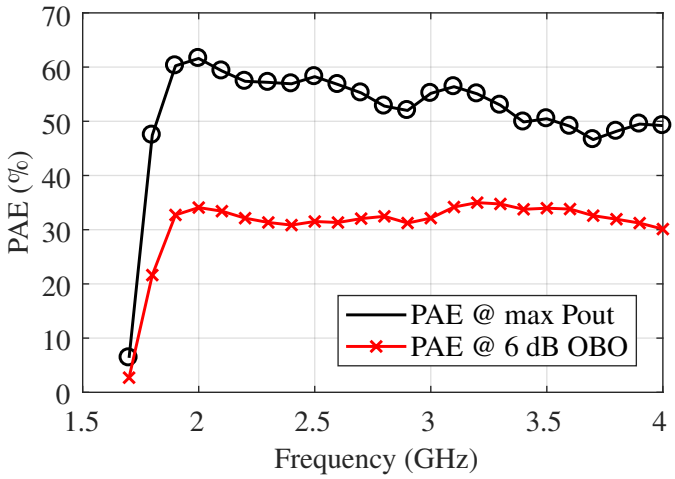


Figure 3.12: Simulated PAE for the octave-bandwidth RF-input LMBA at maximum output power and at 6 dB back-off. The power consumed by the control PA is included in all efficiency calculation in this work.

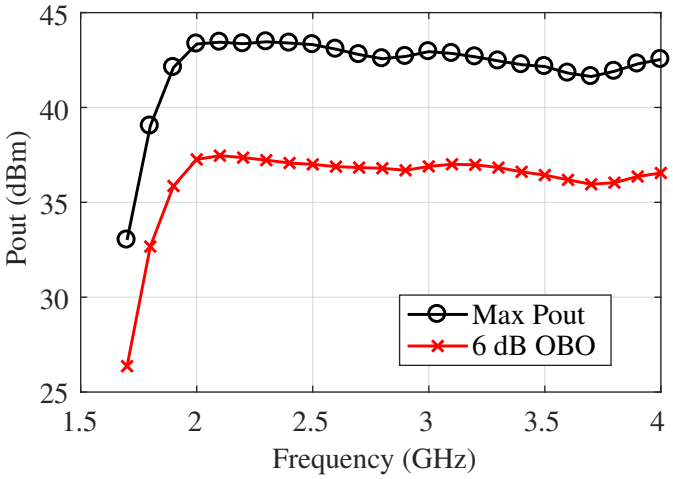


Figure 3.13: Simulated output power for the octave-bandwidth RF-input LMBA.

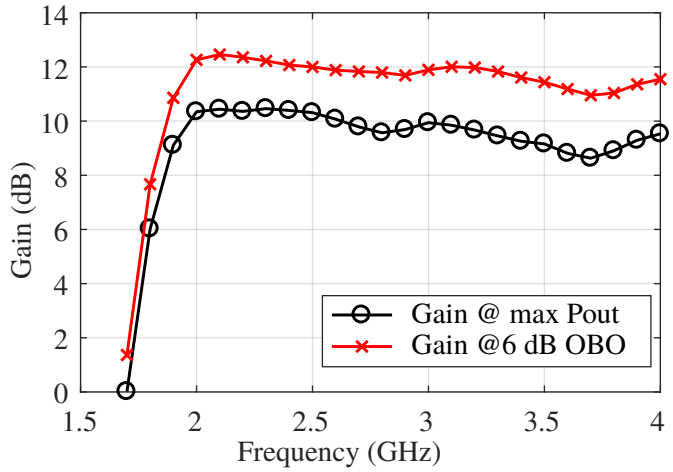


Figure 3.14: Simulated gain for the octave-bandwidth RF-input LMBA.

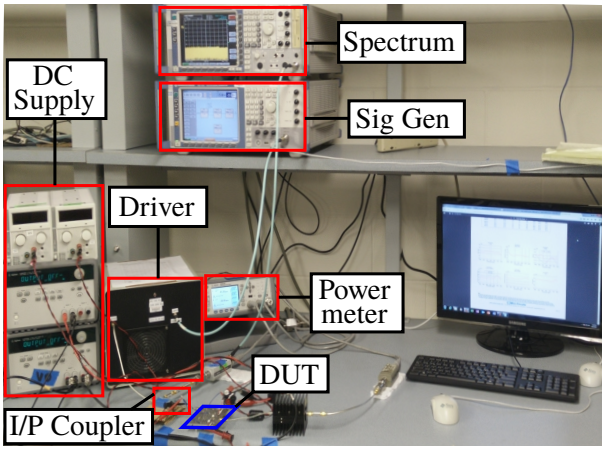


Figure 3.15: Photograph of the experimental test bench.

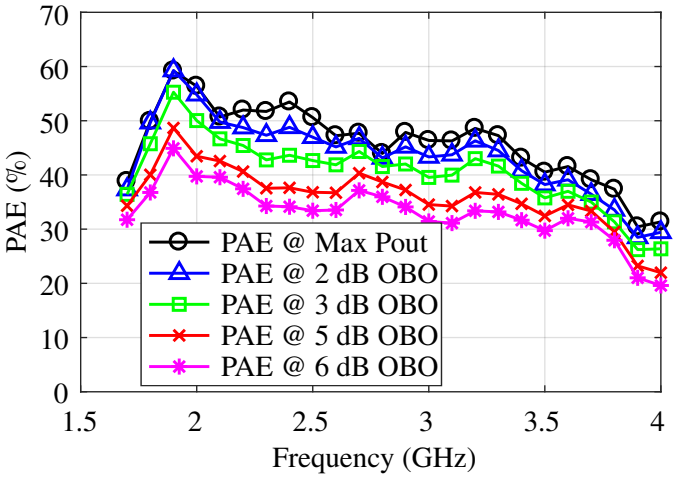


Figure 3.16: Measured PAE over 1.7 GHz to 4 GHz.

3.3.1 CW MEASUREMENTS

The total system PAE of the prototype including both main and control paths is measured from 1.7 GHz to 4 GHZ and is plotted in Fig. 3.16 at various output back-off levels. From Fig. 3.16, the total PAE of the system remains higher than 29% throughout the band of 1.8 GHz to 3.8 GHz at 6 dB OBO. The peak PAE of the system remains above 40% in the middle of the band and drops to 38% at the corner frequencies. Fig. 3.17 shows the output power plotted over 1.7 GHz to 4 GHZ. The maximum output power of 44 dBm occurs at 2.4 GHz and the output power remains above 42 dBm from 1.8 GHz to 3.8 GHz. From Fig. 3.17, the power drops linearly as the input power is lowered. The system gain is plotted in Fig. 3.18 and is found to be lower than the simulated performance. The reduction in the gain is due to input impedance mismatch at the main PAs. Any minimal mismatch at each transistor can cause non-trivial gain reduction in the balanced PA configuration. Drain efficiency is shown in Fig. 3.19 for direct comparison with other works.

The measurement results demonstrate that the prototype is performing amplitude control as the power backs off and phase control as the frequency of operation is changed, validating the approach. A comparison to other published works in the same frequency range, output power level, and technology is given in Table 3.1. Of the single-input architectures, our architecture demonstrates one of the widest fractional bandwidths, and outperforms PAs of similar bandwidths in back-off efficiency.

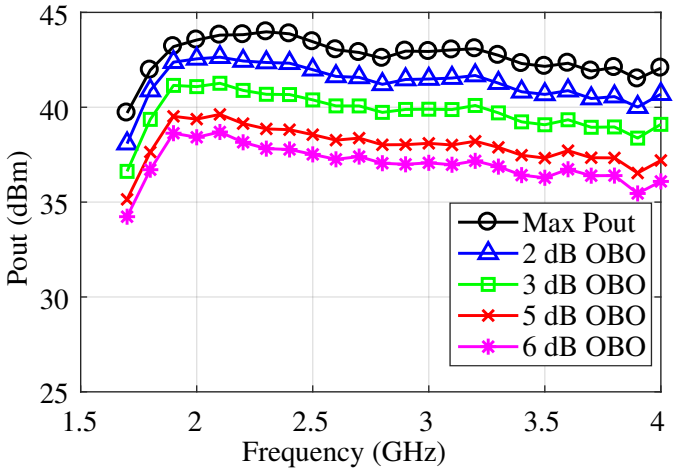


Figure 3.17: Measured output power over 1.7 GHz to 4 GHz.

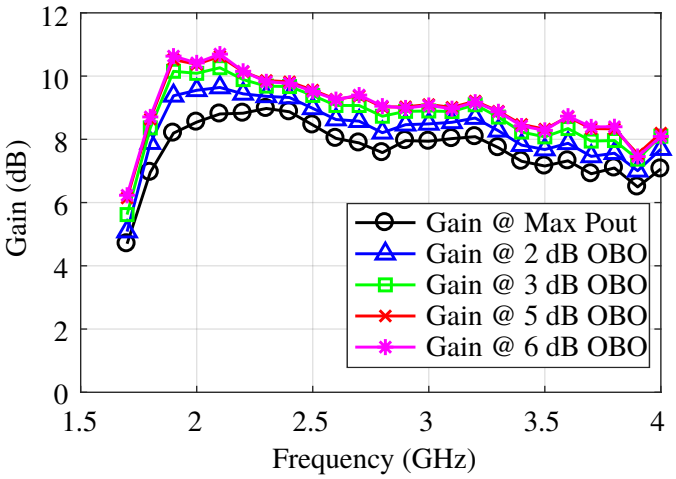


Figure 3.18: Measured gain over 1.7 GHz to 4 GHz.

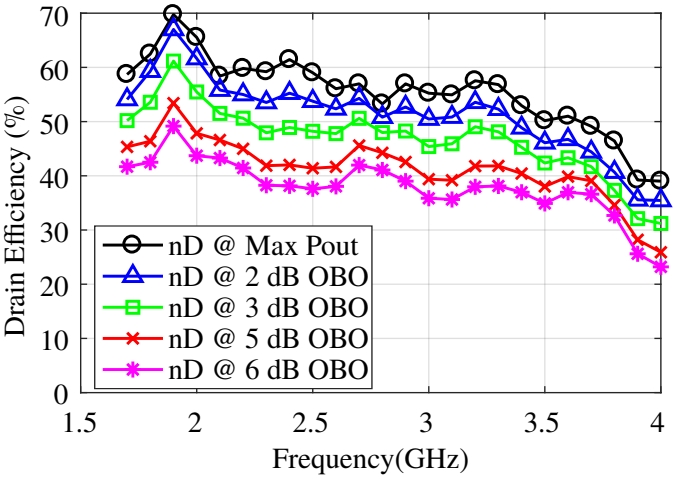


Figure 3.19: Measured drain efficiency over 1.7 GHz to 4 GHz.

Table 3.1: Performance comparison with state of the art GaN wideband PAs with similar frequency and output power range.

Ref.	Year	Architecture	RF inputs	Freq. (GHz)	BW (%)	P_{max} (dBm)	η @ P_{max} (%)	η @ 6 dB OBO (%)	PAE @ P_{max} (%)	PAE @ 6 dB OBO (%)
[55]	2009	class J	1	1.4-2.7	50	40	60-70 *	-	-	-
[56]	2010	Broadband match	1	1.9-4.3	77	42	57-72	20-25*	-	-
[35]	2013	Doherty-Outphasing continuum	2	1-3	100	44.9	45-68	48-68	42-64	45-65
[33]	2014	Outphasing	2	1.2-2.5	70	43	-	-	50-70 *	25-30 *
[32]	2014	Doherty	1	1.05 - 2.55	83	41	45-83	35-58	-	-
[31]	2016	Doherty	1	1.72-2.27	28	42.5	58-72	48-55	-	-
[30]	2017	Doherty	1	0.55-1.1	67	42	60-70	40-50	-	-
[34]	2017	Outphasing	2	0.75-1.05	33	44	71-82 *	60-80 *	-	-
[38]	2016	LMBA	2	0.8-2	86	42	65-85 *	50-65 *	-	-
[41]	2017	LMBA	2	4.5-7.5	50	39	47-77 *	28-60 *	-	-
[46]	2017	RF-input LMBA	1	0.7-0.85	19	42	57-70	34-48	52-63	31-47
This work	2017	RF-input LMBA	1	1.8 - 3.8	71	44	46-70	33-49	37-59	29-45

* - values read from graph

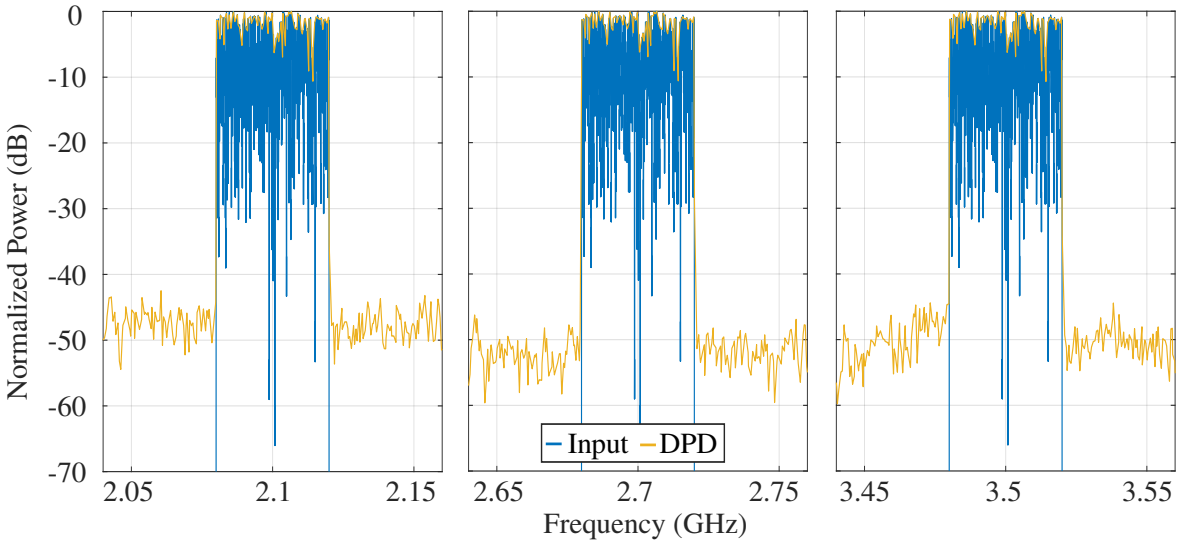


Figure 3.20: Measured output spectra of the octaveband LMBA at 2.1, 2.7 and 3.5 GHz for a 40-MHz, 10 dB PAPR signal with an output PAPR of 10 dB. The plot also shows predistorted input spectra.

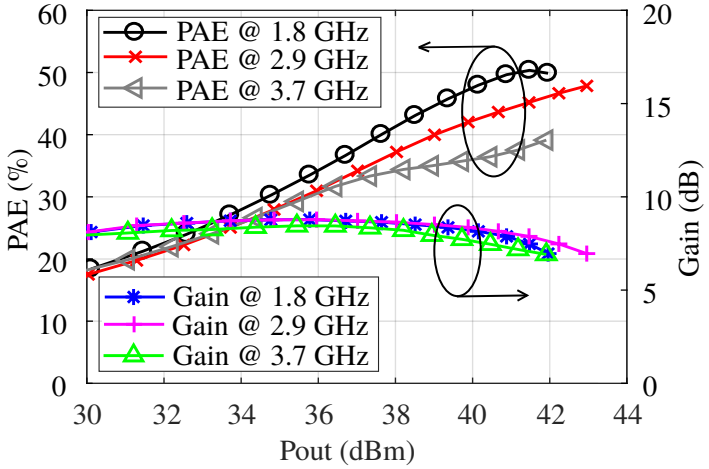


Figure 3.21: Total measured PAE and gain at three frequencies across the operating band.

3.3.2 Modulated measurements

Because of the single RF input used in this design, the same setup shown in Fig. 3.15 can easily be used to perform measurements with modulated signals. A wideband code division multiple access (W-CDMA) signal with 3.84 MHz bandwidth and 9 dB PAPR was used to carry out modulated signal tests. Fig. 3.20 shows output spectrum plots at 1.8 GHz, 2.7 GHz and 3.8 GHz. The worst case adjacent channel leakage ratio (ACLR) was observed to be -26 dB at 1.8 GHz, and improves as the frequency is increased. The best ACLR was observed to be -30 dB at 3.8 GHz. All measurements reported are presented without any predistortion; however, based on the almost linear AM-AM plot [Fig. 3.21] it is expected that the ACLR will improve if linearization is applied.

3.4 Conclusions

The frequency compensation approach presented in this chapter exploits the dispersion of a bandpass filter in order to operate the RF-input LMBA over greater than an octave bandwidth. This approach, related to our amplitude-control approach for load modulation, centers on controlling the relative phase of the control path and main path of an LMBA PA. This novel architecture eliminates the need for external signal generation of the control signal required for prior wideband LMBA system implementations. Advantages of the approach include reduced system complexity and the ability to work directly with many existing calibration and linearization techniques.

The proof-of-concept prototype is implemented using packaged GaN transistors, and demonstrates the technique over a 1.8-3.8 GHz operating range. The system achieves peak drain efficiency of 70%, and a drain efficiency above 46% at peak output power across the band. Back-off efficiency, maintained through load modulation, is above 33% over the entire band. Furthermore, due to the RF-input nature of this architecture, the prototype is easily measured with modulated signals. The PA demonstrates ACLRs ranging from -26 dB to -30 dB across the band without linearization for a 9 dB PAPR, 3.85 MHz W-CDMA signal.

The RF-input LMBA architecture proposed in this chapter is not specific to this particular band or bandwidth. Rather, the frequency range of the prototype was selected based on available commercial off-

the-shelf couplers and packaged devices. Wider bandwidths could be achieved through alternative couplers; in that case, the primary challenge will be in designing the wideband filter with the appropriate passband and phase response. To some extent, this challenge can be mitigated by using bare die or integrated devices, and by minimizing the size of the coupler and interconnects to reduce the frequency variation of the optimal load impedance contours over the operating range. Similarly, higher operating frequencies could be attained with attention to minimizing dispersion, making a MMIC implementation appealing. An interesting further study of this topology would be to understand the limitations in operating frequency range for greater than octave implementations.

Chapter 4

Doherty-Like Load Modulated Balanced Amplifier: An Empirical Approach

In this chapter, we present a new variant on the LMBA architecture, the Doherty-like load modulated balanced amplifier (D-LMBA). As with the related RF-input LMBA architecture [46], [57] (Chapters 2 and 3), the D-LMBA approach employs asymmetry between the main balanced amplifier and the control signal path to produce dynamic load modulation based on the modulated RF input. The D-LMBA differs from the RF-input LMBA in how the control and main PA power profiles are implemented. This architecture uses a class C biased control PA that functions analogously to the auxiliary amplifier of a Doherty Power Amplifier (DPA), and a balanced amplifier that functions analogously to the main amplifier of a DPA. The control PA turns on only in the high-power regime, whereas the balanced PA conducts current linearly with increasing input drive, hence the name Doherty-like LMBA.

This chapter is structured as follows: first, the load modulation mechanism is explained by breaking it down into low and high power regions. Next, a discussion is presented on the D-LMBA architecture with comparison to the DPA. Then an 800 MHz D-LMBA prototype is described followed by a discussion on the measurements and a conclusion.

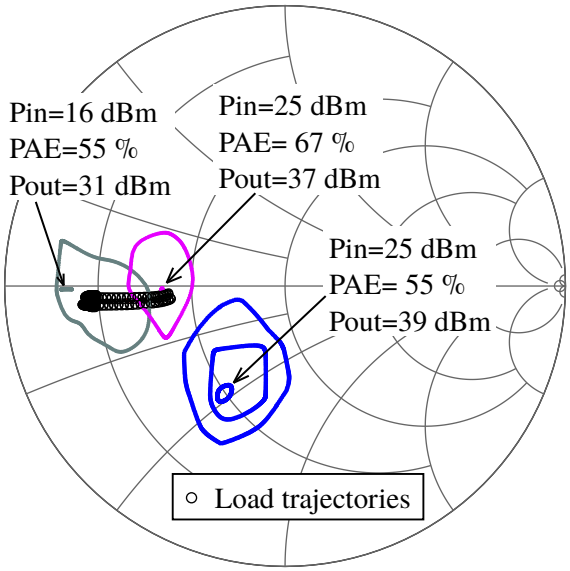


Figure 4.1: Smith chart depicting the simulated load modulation trajectory for the main PAs of RF-input LMBA (chapter 2) and the ideal load modulation trajectory for improved back-off range as well as efficiency.

4.1 Limitations of the RF-input LMBA

In Chapters 2 and 3, a control scheme is used in which the amplitude of the control signal decreases as the input power drive increases. This control scheme works well for small PAPR (~6 dB) signals as demonstrated in [46], [57]; however, for higher PAPR signals the observed efficiency improvement is insufficient. A further analysis of RF-input LMBA has shown two main limitations of the control scheme.

The first limitation of this strategy is that it is difficult to achieve load modulation over a high dynamic range, as a control PA working in ≥6 dB compression is required to achieve the required loading for the main PAs. The ≥6 dB compression of the control PA can be achieved by selecting a relatively small periphery device and operating on lower drain voltage; however this will limit the power capability of the large device and will generate high magnitudes of harmonic power. The second limitation lies in the operation of LMBA itself. When subjected to only amplitude control, the load modulation occurs in radial direction with reference to the center of the Smith chart ($\Gamma = 0$). This means the optimum PAE load as well as optimum power load should occur on the same radial line that extends out from $\Gamma = 0$. In contrast, it is observed that for transistors driven into compression the peak power and back-off PAE loads can occur at very different

values and may not necessarily fall on a radial line. This limits the ability of the RF-input LMBA to achieve the peak power and back-off PAE loads in the same configuration.

Fig. 4.1 illustrates the limitations of the RF-input LMBA approach. The load-pull contours are plotted for the main PA device used in the RF-input LMBA prototype in Chapter 2. The load modulation trajectory achieved by two main PAs is shown in black circles. Also shown is the ideal load modulation trajectory for 8 dB OBO in dashed line. It is clear from the load-pull simulations that with the LMBA technique in the absence of phase modulation, the load can only move in the radial direction on the Smith chart and peak power and back-off PAE load does not occur on a single radial line. Furthermore, it can be seen that the load is modulated in the range of R_{opt} to $\sim 2R_{opt}$ which is equivalent to only 6 dB of dynamic range. In spite of these limitations, it is noted that the RF-input LMBA demonstrated 8-10 percentage points of efficiency enhancement at 6 dB OBO compared to a class B PA.

4.2 Load Modulation

A new scheme for the control path is presented which increases the back-off range and improves the back-off efficiency while maintaining the RF-input nature of the architecture. Compared to the RF-input LMBA [46], the scheme proposed in this work extends the load trajectory to the center of the Smith chart, a direct consequence of the control power being zero at the output power back-off. Therefore, the D-LMBA PA is able to produce a wider range of load modulation. The matching network at the output of the main devices presents the optimum PAE load to these devices in the back-off region. As the input power increases, the control PA turns on and starts to generate the the control signal. This control signal gradually moves the load from the optimum PAE load to the optimum power load. The load modulation phenomenon in D-LMBA can be better understood by considering the following operating conditions:

- Low power region where the control PA is off and only main PAs are active. In this region, since the control power is absent, no load modulation of the main PAs occurs.
- High power region where the control PA and main PAs are active. The control power increases in proportion to the input signal, modulating the main PA load towards the optimum peak power load.

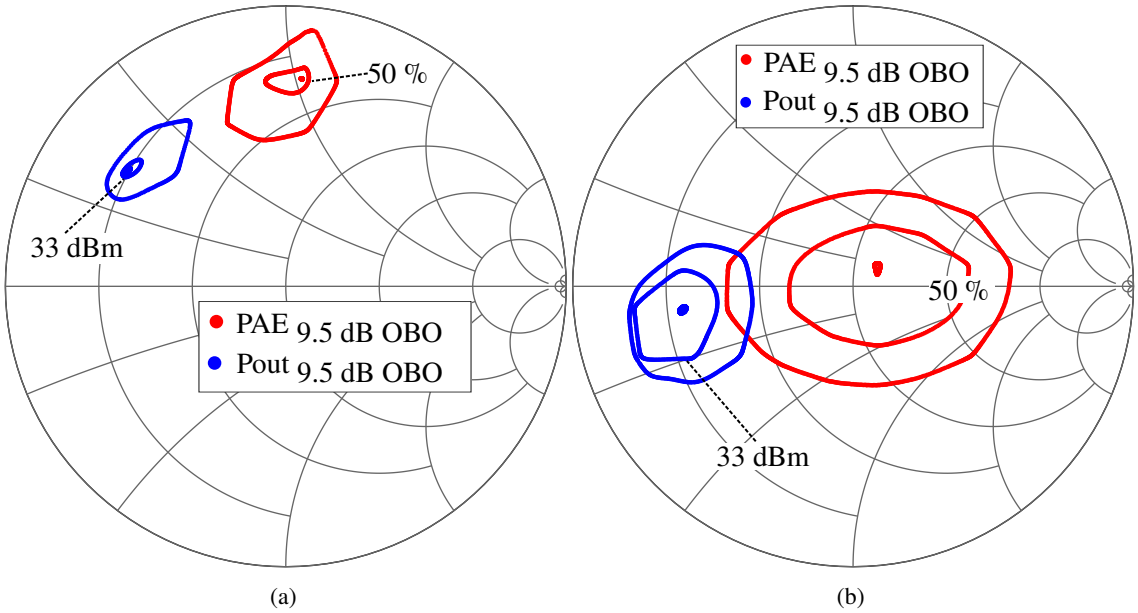


Figure 4.2: The output matching network (OMN) added to the main PA transforms the system impedance to the optimum PAE load at the back-off. The figure shows load-pull contours : (a)– before adding an OMN, (b)– after adding an OMN.

4.2.1 Low power region

The low power region is identified as the region where the control PA remains off. In this region, the main PAs are operated in linear class B. As the input power increases the power delivered by the main PAs increases linearly. The main PAs are conjugately matched at the input and a matching network (OMN) is added at the output that transforms the system impedance (also the characteristics impedance of the coupler) to the back-off PAE load. In the absence of control power, the OMN obtains an optimum back-off PAE load at the drain of the main transistors. This in turns improves the efficiency of the system at the required back-off level. The back-off PAE load of the main PA is determined beforehand from the load-pull analysis, similar to the design of the RF-input LMBA. The load-pull contours of the main PAs before adding the OMN and after adding the OMN are shown in Fig. 4.2(a) and 4.2(b) respectively. The OMN transforms the optimum back-off PAE load in the close proximity of the center of the Smith chart. This suggests that in the absence of the control power, both the main transistors remain PAE matched.

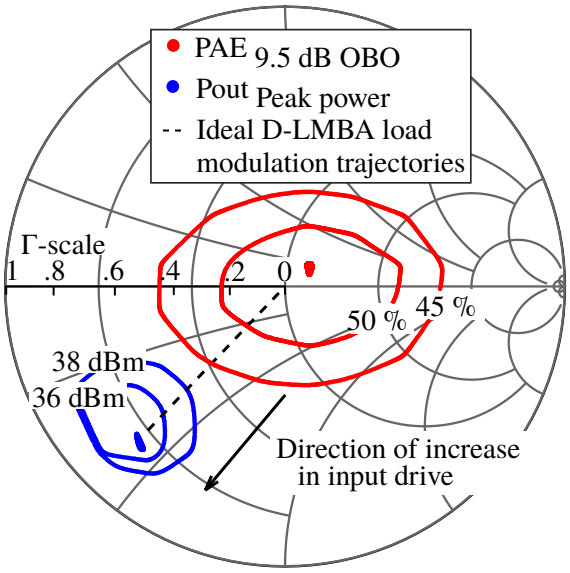


Figure 4.3: Load modulation in high power region in the D-LMBA. As the input drive increases, the load seen by the main PAs moves from the optimum back-off PAE load to the peak power load.

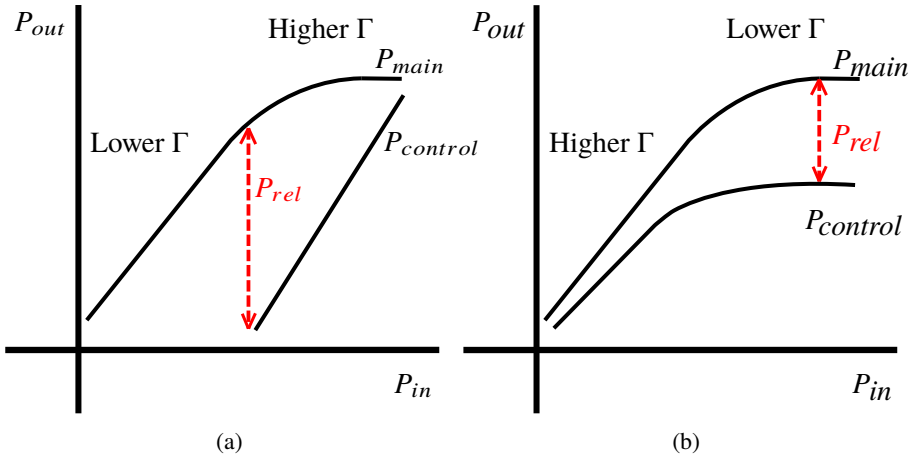


Figure 4.4: Representative plots of main and control output power as a function of input power (a) – for D-LMBA; (b) – for RF-input LMBA.

4.2.2 High power region

Similar to the conventional DPA, the boundary between the low power region and the high power region can be defined as the power level at which the control PA starts to conduct current. In the high power region, the already 'ON' class B main PAs are subjected to load modulation through injected power from the control PA. The class C biased control PA generates the control power in proportion to the input drive. As the input drive increases, the injected control power into the main PAs increases. This dynamically changes the load seen by the two main transistors. At the boundary, when the control power is just turned on, the main PAs are still matched to the back-off PAE load (i.e. $\Gamma \approx 0$). As the input drive further increases, the effective load moves radially towards a higher $|\Gamma|$, away from the center of the Smith chart. This load modulation is depicted in Fig. 4.3, with the ideal load modulation trajectory desired for the main PAs represented by the black dashed line. This radial trajectory can be confirmed from the magnitude control theory of the LMBA presented in Chapter 1 which states that 'the higher magnitude of reflection coefficient (Γ) can be obtained at the main transistor by increasing the control signal amplitude ($|P_{\text{ctrl}}|$) relative to the main signal'. The power profiles of the control and the main PA are illustrated in Fig. 4.4(a). For direct comparison, the control and main PA power profiles of the RF-input LMBA are also shown in Fig. 4.4(b).

The phase of the reflection coefficient trajectory is set by the relative phase of the control signal. By adding an appropriate phase shift between the control and the main path and by carefully scaling the devices, a load modulation trajectory can be obtained which will present the optimum power load at the peak power to the main transistors.

4.3 D-LMBA Architecture

A block diagram of the D-LMBA architecture is shown in Fig. 4.5. As with the related RF-input LMBA architecture [46], [57], the D-LMBA approach employs control signal generation (directly derived from the input RF signal) for dynamic load modulation. In contrast to the RF-input LMBA an output matching network (OMN) is added in the main PAs to transform the 50 Ω system impedance to a PAE match at OBO. This OMN ensures that in the reference plane after the OMN (Z_{ref} in Fig. 4.5), the target impedance is in

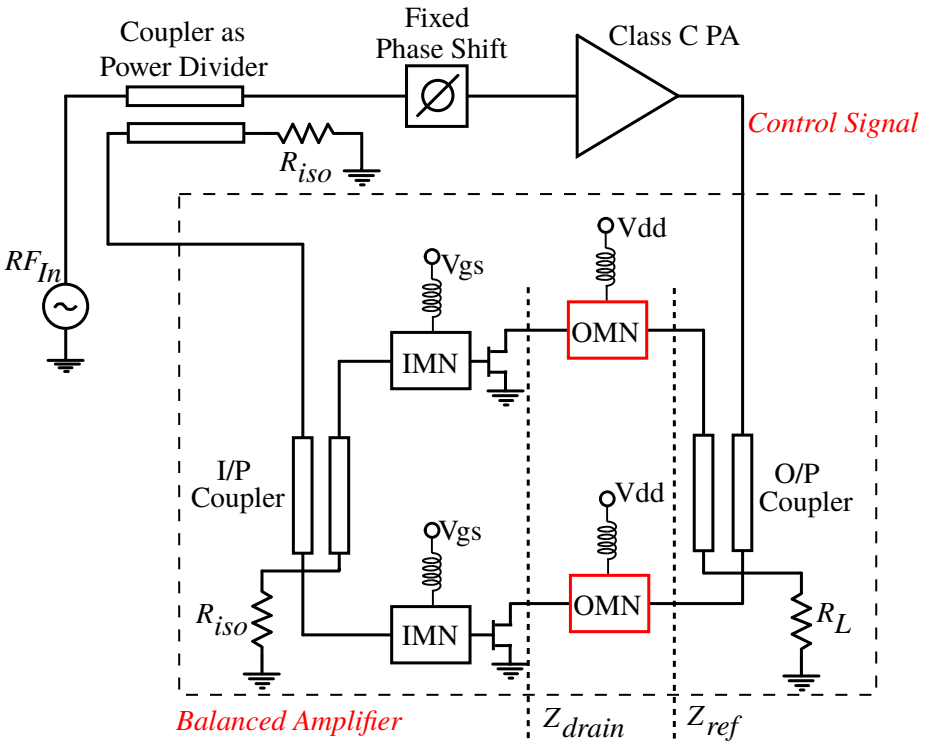


Figure 4.5: Block diagram of the D-LMBA. A class C control PA injects a signal to the output of the balanced amplifier, producing load modulation in the high-power operating mode.

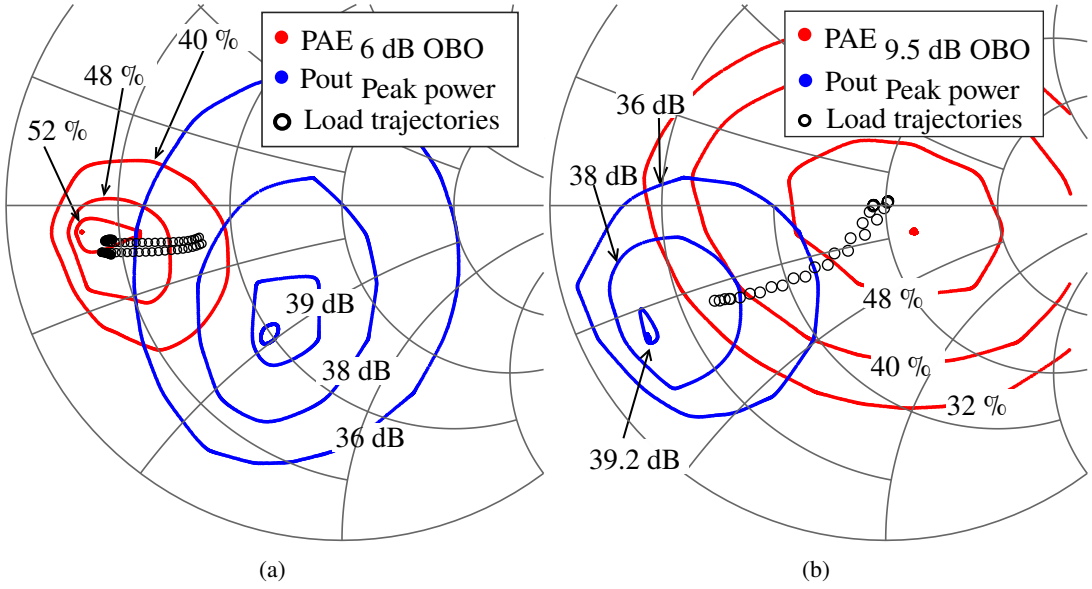


Figure 4.6: Load-pull simulations of the main PA (including output networks) at power back-off and max power out, with the loading trajectory for the two main PAs. Both plots are referenced to the inputs of the hybrid coupler. (a) – for RF-input LMBA; (b) – for D-LMBA.

the center of the Smith chart at back-off and moves radially away from the center towards a power match, as the power increases.

Simulated load-pull contours and load trajectories for the main PAs of the RF-input LMBA and D-LMBA are shown in Fig. 4.6. Both sets of load pull contours are referenced to the input ports of the output coupler in the respective designs (Z_{ref}), after the OMN of the main PAs. In each plot, output power contours are shown in blue, while the PAE contours (simulated at the target output back-off power level) are shown in red. PAE contours are used because of the focus of this work on improving efficiency at a target back-off level. The different contours reflect the different design approaches between this work and [46]; in [46] only a minimal bias network and a harmonic termination network is used whereas here an OMN provides a match at low power levels. The D-LMBA trajectory in Fig. 4.6(b) shows the expected increase in load modulation range due to the greater variation in P_{rel}, corresponding to enhanced efficiency over a larger back-off range compared to [46].

4.3.1 Comparison to Doherty PA

It is natural to compare the D-LMBA to the well-established DPA technique, as both approaches use load modulation for efficiency enhancement. Compared to a 2-way DPA (i.e., the balanced PA corresponds to the main PA and the control PA corresponds to the aux PA), the D-LMBA uses a relatively low-power aux PA to achieve a large load modulation range. For example, in [58] an efficiency peak at 6-dB back-off is achieved using a 10-W main PA and 25-W aux PA, in contrast to the 20-W main and 6-W aux used here. Similarly, in a 3-way DPA it is typical to use one main PA and two aux PAs [59]. In either case, the D-LMBA has better utilization of the devices in the back-off mode. Alternatively, it could be argued that the D-LMBA should be compared to a 3-way DPA due to the number of devices used. The D-LMBA prototype does not provide the same level of OBO efficiency as, e.g., [59], but has the advantage of a relatively simple design methodology. Although it is not exploited in this first proof of concept demonstration, a further advantage of the D-LMBA is that its combining network is inherently wideband, as utilized in [41].

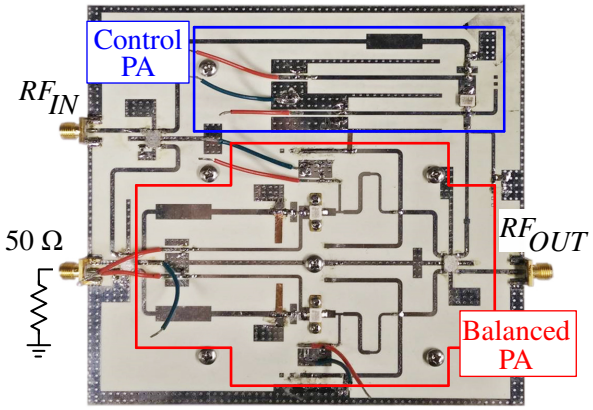


Figure 4.7: Photograph of the D-LMBA prototype, measuring 15.5×14.7 cm.

4.4 D-LMBA Prototype Design

To enable a direct comparison between the RF-input LMBA [46] and D-LMBA architectures, a proof-of-concept D-LMBA is designed at 800 MHz. The D-LMBA architecture is implemented on a 30-mil thick Rogers RO4350 substrate, measuring approximately 15.5 cm by 14.7 cm. The photograph of the prototype is shown in Fig. 4.7. The balanced PA is shown in the red box. It consists of two identical main PAs and two Anaren X3C07P1-03S 90° hybrid couplers. The main PAs are designed using CGH40010F packaged GaN devices from Wolfspeed. The devices are conjugately matched at the input. At the output, the OMN transforms the system impedance to the optimum PAE load at the back-off, found from the load-pull simulation and is implemented with the stepped microstrip lines. The second and third harmonic terminations are also part of the matching network and are implemented with shunt stubs. The stub lengths are adjusted in tuning by taking into consideration the package parasitic of the transistors.

The control path PA uses the Wolfspeed CGH40006P packaged GaN device, biased in deep class C. At the input the control PA is conjugately matched, whereas the output is matched to the peak PAE load. The control PA is shown in the blue box on the top of Fig. 4.7.

The power splitter at the input is realized using a 3 dB coupler. It is noted that for efficient implementation of this technique, an unequal power division would be optimum, however for cost-effectiveness of the system, the same coupler X3C07P1-03S is used as the power splitter. An analytical solution of the split ratio is

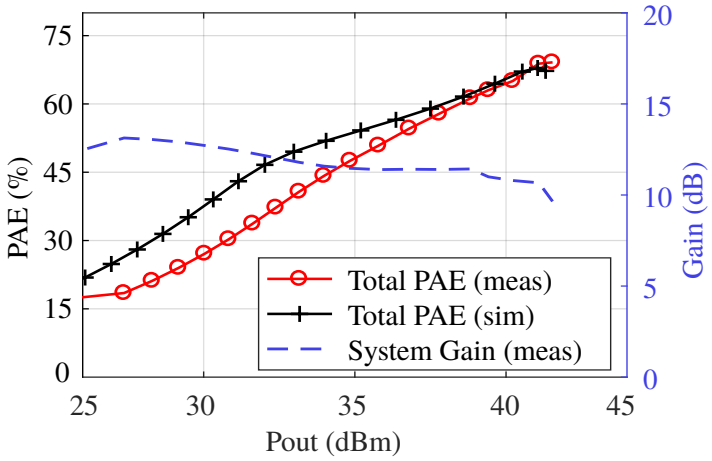


Figure 4.8: Measured PAE, simulated PAE and the measured gain at 800 MHz. The PAE calculation includes the power dissipated in the control PA.

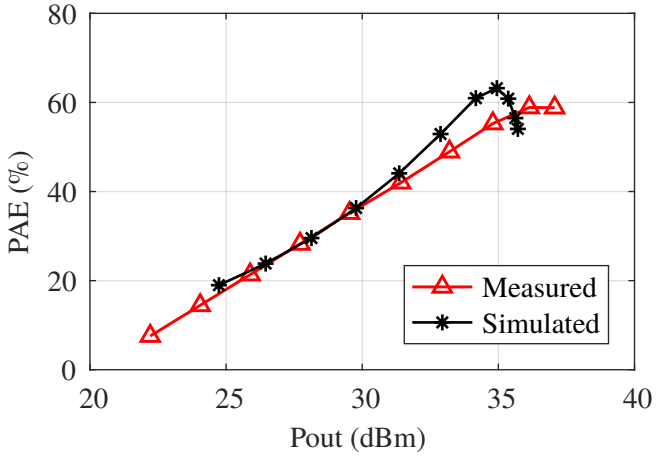


Figure 4.9: Measured and simulated PAE of balanced PA, obtained by modifying the PCB traces and completely bypassing the control path.

presented in the next chapter, where the split ratio is derived based on the required dynamic range and the scaling ratio between the control and main PA.

Similar to the RF-input LMBA architecture, a transmission line is used at the input of the control PA to achieve the required phase difference between the control and the main signal. The proof-of-concept PA is designed to work over a narrow bandwidth. However, a wide-band dynamic match can be achieved by utilizing the frequency-dependent phase compensation approach as implemented in the Octaveband RF-input LMBA (Chapter 3).

Table 4.1: Performance summary and comparison to related state-of-the-art PAs.

Ref.	Year	Architecture	RF inputs	Freq. (GHz)	BW (%)	P_{max} (dBm)	η @ P_{max} (%)	η @ 6 dB OBO (%)	η (%) @ P_{avg}(dBm)/ PAPR(dB)
[59]	2015	3-way Doherty	1	0.7-0.95	30.3	44.7	60-78.3	51.6-67.5	46-57 (32.8-35.1/9.5 dB) WCDMA
[58]	2014	Doherty	1	0.7-0.95	30.3	43	53-67 *	48-56 *	42 ** (33.5 /9.4 dB) 15-MHz LTE
[38]	2016	LMBA	2	0.8-2	86	42	65-85 *	50-65 *	-
[46]	2017	RF-input LMBA	1	0.7-0.85	19	41.7	57-70	34-48	34.1 (32.8/10 dB) 3.84-WCDMA
This work	2017	D-LMBA	1	0.77-0.86	11	41.7	54-75.5	45.7-51	47 (31.3/12.1 dB) 5-MHz LTE

* - values read from graph, ** - values for concurrent dualband signal

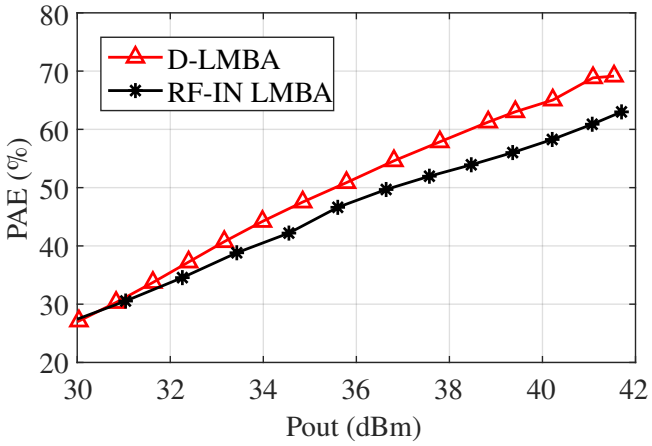


Figure 4.10: Efficiency comparison between the D-LMBA and RF-input LMBA. The D-LMBA approach improves the 6-dB OBO PAE by 5-7 percentage points.

4.5 Experimental Results

Fig. 4.8 compares the simulated and measured CW performance of D-LMBA at 800 MHz. The simulated performance exhibits enhanced efficiency over a 33.2-41.7 dBm range, or 8.5 dB. The measured results, however, have a discrepancy of approximately 8-9 percentage points in the back-off region.

To understand this discrepancy, the balanced PA is measured alone by modifying the PCB. The control PA traces at the input and output couplers are cut, and the appropriate ports are terminated on the PCB using SMD resistors. The isolation port of the input coupler is made accessible by connecting it to the SMA connector. The same port is then used to drive the balanced amplifier. In this way, the input power divider and control PA are completely bypassed. The balanced amplifier measured and simulated PAE is shown in Fig. 4.9. The measured PAE matches simulation at the back-off (where the PA is matched for, in the absence of the control signal), while there is a discrepancy at higher power where the balanced amplifier is overdriven.

The agreement in simulation and measurement for the balanced amplifier at OBO implies that the efficiency degradation in the total D-LMBA is related to the control amplifier operation. Therefore, we conclude that the discrepancy between simulation and measurement is dominated by impedance mismatch at the input to the control PA, especially when the control PA is off (not a well-modeled state) which would

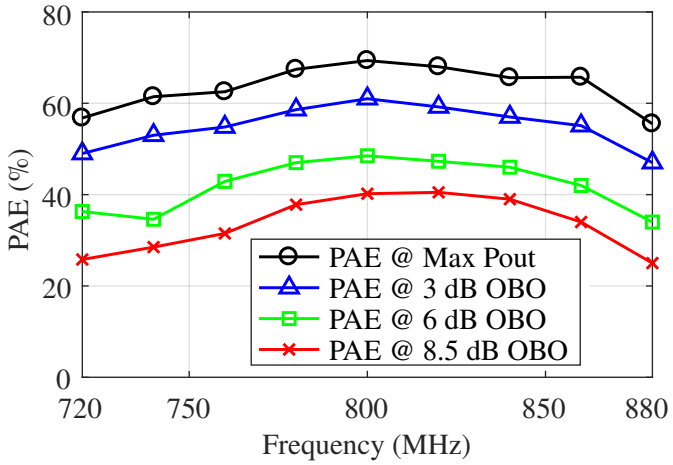


Figure 4.11: Measured PAE over 720 MHz to 880 MHz when the output power is varied from peak power to 8.5 dB output back-off (OBO).

interfere with the input split. In support of this theory is the 12 dB measured gain (linear), which is 1.4 dB lower than simulation implying inaccurate modeling in the input matching network. Despite the reduction in PAE from the simulation value, the D-LMBA shows a drain efficiency improvement of approximately 6-10 percentage points compared to [46] over a 6 dB range (Fig. 4.10), although with a degradation in bandwidth due to the addition of the OMN.

Fig. 4.11 shows the total system PAE including both main and control paths from 720 MHz to 880 MHz for 3, 6 and 8.5-dB output power back-off. The total PAE of the system remains higher than 35% over the range of 770 MHz to 860 MHz for 8.5 dB back-off. The bias points for all three devices were kept constant throughout frequencies and power levels.

A 5-MHz LTE signal with measured output PAPR of 12.1-dB is used to characterize the system linearity. The output spectrum of the signal centered at 800 MHz with and without memoryless digital predistortion (DPD) is shown in Fig. 4.12. With DPD, the PA has ACLR of -44.3 dBc with an average output power of 31.3 dBm and PAE of 45%. A summary of the D-LMBA performance and that of related works at similar frequencies, power levels, and technology is given in Table 4.1.

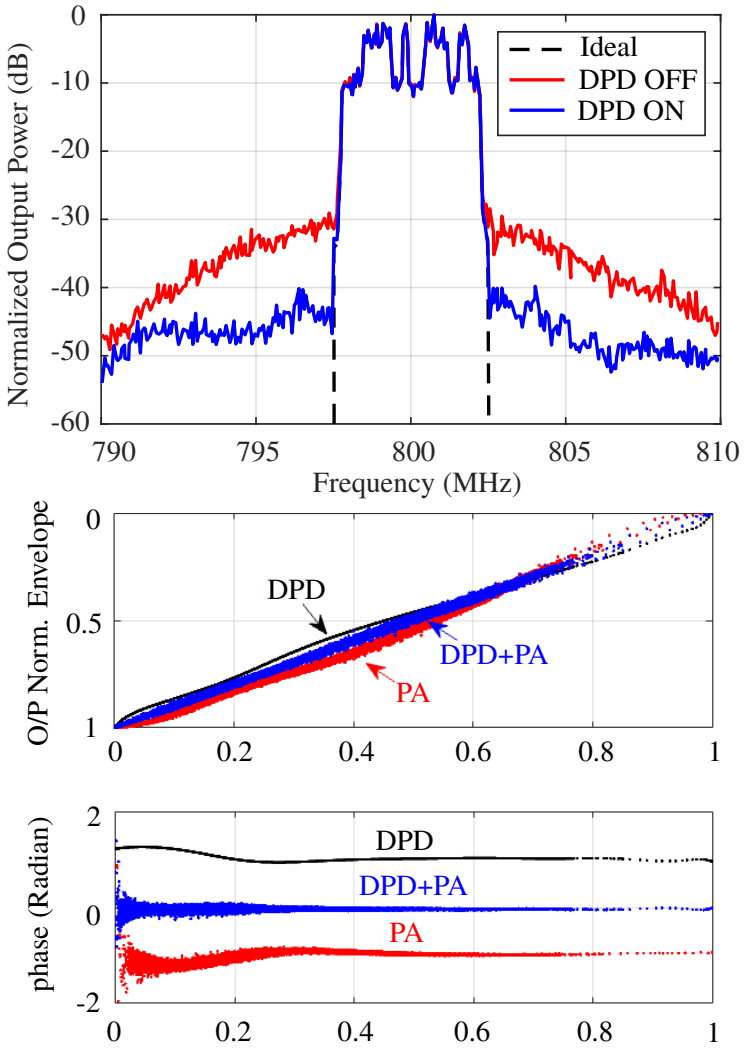


Figure 4.12: Measured 5-MHz LTE signal centered at 800 MHz with DPD. The result shows ACLR of -44.3 dBc at P_{avg} of 31.3 dBm and PAE = 45%.

4.6 Conclusions

The D-LMBA presented in this chapter demonstrates a new approach to an RF-input LMBA architecture, using a control scheme based on turning on the control PA at the upper end of the output power range. Compared to the RF-input LMBA [46], the D-LMBA prototype demonstrates a greater range of dynamic load modulation, and therefore improved back-off efficiency, but degradation in bandwidth. Both of these effects are due to the inclusion of a matching network in the main PAs. It is observed that the D-LMBA approach increased the 6-dB OBO PAE by 5-7 percentage points however the fractional bandwidth reduced

from 19% to 11% compared to RF-input LMBA. It is also proposed that by implementing the broadband matching network approach presented in [57], the bandwidth reduction can be compensated for, making this PA architecture an effective choice for efficient, linear operation.

The design methodology presented in this chapter is based on the empirical approach. It requires further development in terms of system parameters, particularly in the modeling of the input split, the dynamic range of efficiency enhancement, relative sizing of the multiple devices, relative drain supply voltages, system gain compression etc. A detailed analysis of these system parameters is presented in the next chapter.

Chapter 5

Doherty-Like Load Modulated Balanced Amplifier: An Analytical Approach

This chapter focuses on the theoretical aspects of Doherty-Like Load Modulated Balanced Amplifier, in contrast to the empirical approach presented in Chapter 4. It derives the design equations for the system-level parameters of the D-LMBA, i.e., the input power-splitting ratio, transistor scaling ratio, supply voltages, and so on. The design equations are derived in terms of transistor parameters and dynamic range of efficiency enhancement, simplifying the D-LMBA PA design procedure.

The presented derivation is based on the "black-box" method that has been previously applied to DPA [60, 61] and outphasing [34] PAs. The proposed theoretical analysis enables us to compare the D-LMBA to related load modulation techniques in terms of key parameters including the OBO range for efficiency enhancement, relative sizing of the multiple devices, relative drain supply voltages, relative power generated by the devices, system gain compression, and input power division among the devices.

The chapter is structured as follows: first, the circuit-parameters (currents, voltages, and impedances) for the individual PAs are derived by treating the transistors as ideal current sources. Next, the system-level parameters of the architecture are derived. Further, the analysis is extended by comparing the design parameters of the D-LMBA with that of other load modulation techniques. Next, a design methodology is

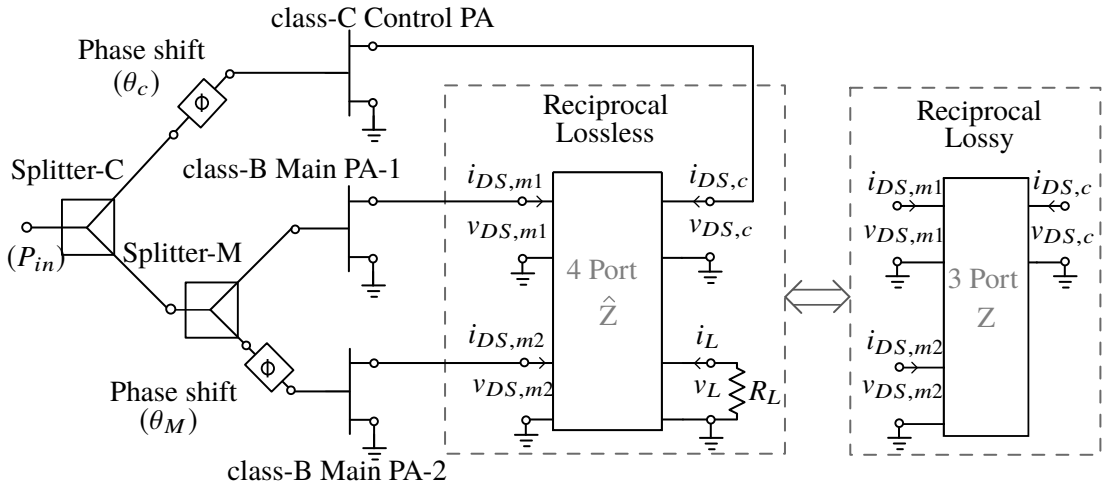


Figure 5.1: The generalized RF-input LMBA architecture with the output combiner illustrated as a four-port black-box network. The reciprocal and lossless four-port network $\hat{Z}$ with the fourth port terminated with a resistive load has an equivalent reciprocal and lossy three-port network Z. Analyzing the LMBA in terms of the three-port simplifies the analysis significantly.

proposed followed by a description of 2.4-GHz, 25-W design example. Lastly, a discussion on measurement results and conclusion is presented.

5.1 D-LMBA Analysis

A simplified schematic of the black-box analysis method for the D-LMBA architecture is depicted in Fig. 5.1. Based on the empirical approach presented in Chapter 4, the control PA is operated in class C while both the main PAs are operated in class B. The output combining network is treated as a "black-box" network to correlate the boundary conditions with the fundamental currents and voltages of the transistors.

In this section, the transistor modeling based on the class of operation is first described, and then, boundary conditions for high efficiency are identified. Finally, all circuit parameters and relationships are derived in terms of transistor parameters and a predetermined dynamic range of efficiency enhancement, i.e., the output power range where the efficiency is maximized.

5.1.1 Transistor Modeling

In the following analysis, the transistors are modeled as ideal current sources using a piecewise linear model [48]. The ideal current source does not capture the complete intricate behavior of a real transistor, in particular the nonlinear behavior. Nonetheless, the simplified model allows for an understanding of the basic operation and makes it possible to qualitatively compare different architectures.

The two main transistors comprising the balanced amplifier are sized identically, while at this point, it is assumed that the control PA device can be of an arbitrary size. Selection of this sizing ratio will be discussed in Section 5.1.4. The time-domain drain current of the class B biased main transistor 1 can be expressed as

$$i_{DS,m1}(\beta) = \begin{cases} \beta I_{\mathrm{MAX},m} \sin(\omega_0 t) & \text{for } 0 \le \omega_0 t \le \pi \\ 0 & \text{otherwise} \end{cases} \tag{5.1}$$

where β is the normalized input drive level ($0 \le \beta \le 1$), $I_{\mathrm{MAX},m}$ is the maximum current of each main transistor and ω_0 is the fundamental angular frequency. The two main transistors provide the same magnitude of current, but the drain current of main transistor 2 is delayed by a phase θ_m relative to the current of main transistor 1.

The control transistor is biased in class C, i.e., the gate bias $V_{GS,c}$ is selected below the threshold voltage V_{TH}. The time-domain drain current can be expressed as

$$i_{DS,c}(\beta, \beta_{bo}) = \begin{cases} \frac{I_{\mathrm{MAX},c}}{1-\beta_{bo}} (\beta \sin(\omega_0 t - \theta_c) - \beta_{bo}) & \text{for } \phi_x \le \omega_0 t - \theta_c \le \pi - \phi_x \\ 0 & \text{otherwise} \end{cases} \tag{5.2}$$

where ϕ_x is the angle at which the time domain gate-source voltage $v_{GS,c}$ reaches V_{TH}, θ_c is the relative phase compared to main transistor 1, and β_{bo} is the drive level where $v_{GS,c}$ first reaches V_{TH}. β_{bo} corresponds to the drive level where the class C biased transistor starts to conduct and can be expressed as

$$\beta_{bo} = \frac{V_{TH} - V_{GS,c}}{V_{gs,\max,c}} \tag{5.3}$$

where $V_{gs,\max,c}$ is the maximum fundamental gate voltage. The maximum dc current $I_{\mathrm{MAX},c}$ is related to

$I_{\mathrm{MAX},m}$ through a relative transistor size factor S_c

$$I_{\mathrm{MAX},c} = S_c I_{\mathrm{MAX},m}. \tag{5.4}$$

A detailed discussion of β_{bo}, including its relationship to the dynamic range of efficiency enhancement, γ, and of S_c can be found later in this section.

A Fourier series expansion of the time domain drain currents gives the following fundamental components for main transistor 1 (class B) and for the control transistor (class C)

$$I_{ds,m1} = -j\beta \frac{I_{\mathrm{MAX},m}}{2} \tag{5.5}$$

$$I_{ds,c} = \begin{cases} -j\frac{S_c I_{\mathrm{MAX},m}}{\pi(\beta_{bo}-1)} \times \left(\beta_{bo}\sqrt{1-\left(\frac{\beta_{bo}}{\beta}\right)^2} - \beta\cos^{-1}\left(\frac{\beta_{bo}}{\beta}\right)\right)\angle -\theta_c & \text{for } \beta \geq \beta_{bo} \\ 0 & \text{for } \beta < \beta_{bo} \end{cases} \tag{5.6}$$

At the maximum drive level, i.e., for $\beta = 1$, the maximum fundamental drain current of the control transistor can be related to the maximum fundamental drain current of main transistor 1 with a current factor α_M. At the backed-off drive level, i.e., for $\beta = \beta_{bo}$, the drain currents of the two main transistors are scaled linearly with β_{bo} and the drain current of the control transistor is zero. In summary:

$$\begin{aligned} I_{m1M} &= I_{ds,m1}\big|_{\beta=1} = I_{\mathrm{MAX},m}/2 \\ I_{m2M} &= I_{ds,m2}\big|_{\beta=1} = I_{m1M}\angle -\theta_m \\ I_{cM} &= I_{ds,c}\big|_{\beta=1} = \alpha_M I_{m1M}\angle -\theta_c \end{aligned} \tag{5.7}$$

$$\begin{aligned} I_{m1B} &= I_{ds,m1}\big|_{\beta=\beta_{bo}} = \beta_{bo} I_{m1M} \\ I_{m2B} &= I_{ds,m2}\big|_{\beta=\beta_{bo}} = \beta_{bo} I_{m2M} \\ I_{cB} &= I_{ds,c}\big|_{\beta=\beta_{bo}} = 0 \end{aligned} \tag{5.8}$$

Note that the fundamental currents at the maximum drive level are denoted with subscript M and at back-off level with subscript B. In (5.7) and (5.8), $I_{m1} = I_{ds,m1}$ is considered to be the reference current (zero phase), such that all other currents can be expressed in terms of I_{m1}. The fundamental drain currents are plotted in Fig. 5.2 for an example value of $\beta_{bo} = 0.33$.

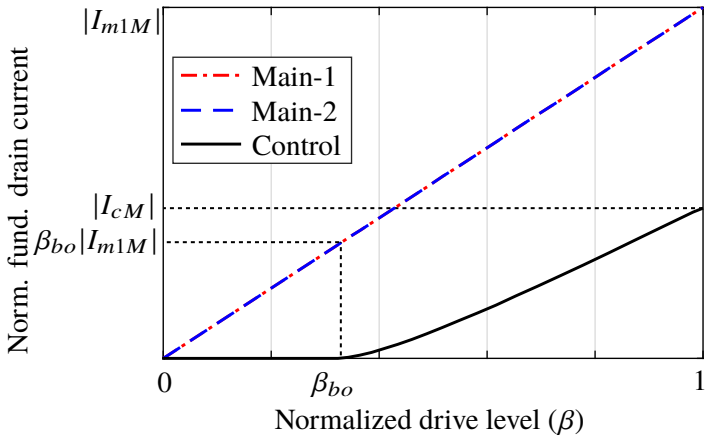


Figure 5.2: Fundamental drain currents of the two main transistors and the control transistor versus normalized input drive level β. The currents are plotted for an example value of $\beta_{bo} = 0.33$ and for an arbitrary combining network.

So far, the unknowns are the current ratio α_M, the control transistor gate bias $V_{GS,c}$, the relative size of the control transistor S_c, and the phase delays θ_c and θ_m. These unknowns will be solved in terms of the main transistor parameters and the backed-off drive level β_{bo} later in this section. It will also be shown that β_{bo} has a direct relation to the dynamic range of output power over which efficiency is enhanced.

5.1.2 Boundary Conditions and Output Combiner

The second step in the D-LMBA analysis is to derive the output combiner parameters from selected boundary conditions. Here, the boundary conditions are defined as achieving maximum efficiency at peak power and at a predetermined back-off level. This imposes the following conditions:

(1) at the maximum drive level ($\beta = 1$), optimal loads for high efficiency are presented to the two main transistor and to the control transistor; and

(2) at the back-off drive level ($\beta = \beta_{bo}$), optimal loads for high efficiency are presented to the two main transistors (here the control transistor is off).

The next step is to formalize these boundary conditions in terms of equations.

The four-port output combiner in Fig. 5.1 is reciprocal and lossless. By absorbing the load resistor into the network, the original four-port network can be converted to a three-port network. This simplifies the

following analysis significantly. This resulting three-port network will be reciprocal and lossy because of the inclusion of the resistor. A similar procedure is employed in [60, 61] to convert a lossless three-port network into lossy two-port network. The conversion from a lossless four-port network with the fourth port terminated with a resistive load to a lossy three-port network imposes the following three conditions that are derived in the Appendix and reproduced as (5.9).

$$\begin{aligned} \mathrm{Re}(Z_{12})^2 &= \mathrm{Re}(Z_{11})\,\mathrm{Re}(Z_{22}) \\ \mathrm{Re}(Z_{13})^2 &= \mathrm{Re}(Z_{11})\,\mathrm{Re}(Z_{33}) \\ \mathrm{Re}(Z_{23})^2 &= \mathrm{Re}(Z_{22})\,\mathrm{Re}(Z_{33}) \end{aligned} \tag{5.9}$$

The definition of the reciprocal three-port parameters is

$$\begin{aligned} V_{m1} &= Z_{11}I_{m1} + Z_{12}I_{m2} + Z_{13}I_c \\ V_{m2} &= Z_{12}I_{m1} + Z_{22}I_{m2} + Z_{23}I_c \\ V_c &= Z_{13}I_{m1} + Z_{23}I_{m2} + Z_{33}I_c \end{aligned} \tag{5.10}$$

Normalizing (5.10) with I_{m1}, I_{m2} and I_c respectively gives

$$\begin{aligned} Z_{Lm1} &= Z_{11} + Z_{12}\alpha_3\angle{-\theta_m} + Z_{13}\alpha_1\angle{-\theta_c} \\ Z_{Lm2} &= Z_{22} + Z_{12}/\alpha_3\angle\theta_m + Z_{23}\alpha_2\angle(\theta_m - \theta_c) \\ Z_{Lc} &= Z_{33} + Z_{13}/\alpha_1\angle\theta_c + Z_{23}/\alpha_2\angle{-(\theta_m - \theta_c)} \end{aligned} \tag{5.11}$$

where $\alpha_1 = I_c/I_{m1}$, $\alpha_2 = I_c/I_{m2}$ and $\alpha_3 = I_{m2}/I_{m1}$. Here Z_L denotes the load presented to the each PA.

Now, the boundary conditions discussed above can be formalized. For ideal transistors, as defined in Section 5.1.1, the following two sets of equations are obtained:

At the maximum drive level ($\beta = 1$)

$$\begin{aligned} R_{\mathrm{opt}} &= Z_{11} + Z_{12}\angle{-\theta_m} + Z_{13}\alpha_M\angle{-\theta_c} \\ R_{\mathrm{opt}} &= Z_{22} + Z_{12}\angle\theta_m + Z_{23}\alpha_M\angle(\theta_m - \theta_c) \\ Z_{LcM} &= Z_{33} + Z_{13}(1/\alpha_M)\angle\theta_c + Z_{23}(1/\alpha_M)\angle(-\theta_m + \theta_c) \end{aligned} \tag{5.12}$$

At the back-off level ($\beta = \beta_{bo}$)

$$\begin{aligned} R_{\mathrm{opt}}/\beta_{bo} &= Z_{11} + Z_{12}\angle{-\theta_m} \\ R_{\mathrm{opt}}/\beta_{bo} &= Z_{22} + Z_{12}\angle\theta_m \end{aligned} \tag{5.13}$$

Here, R_{opt} is the optimal class B load termination [48] and Z_{LcM} is the load presented to the control transistor at maximum drive level. To simplify further analysis, the optimal impedance for the main transistors is denoted Z_{Lm1M} and Z_{Lm1B} for maximum drive level and the backed-off drive level, respectively.

The remainder of the D-LMBA analysis can be performed using two different approaches. In the first approach, the three port combining network is treated as an arbitrary "black box" network. The parameters of the network are then calculated from (5.12) and (5.13) in terms of optimal load impedances, the current factor α_M, and the phase delays θ_m and θ_c. Once the complete parameters are known, a network is synthesized using passive components. In that case, the phase delays are found from the constraints in (5.9). The current factor α_M remains as a design parameter. Synthesizing the three-port network based on the given parameter may need rigorous computation. The advantage of such an approach, however, is that the optimal impedances can be extracted directly from load pull data with the output combiner directly performing output matching. This approach is analogous to that used in [34, 60, 61] for Doherty and outphasing PAs.

An alternative approach is to assume a known component as the output combiner. Based on the Z-parameters of this component, (5.12) and (5.13) are solved to find the design equations. The second approach is used in this work, with the combiner assumed to be based on a 90° hybrid coupler, as proposed in the original LMBA theory [38, 41, 62].

Assuming that the coupler has a characteristic impedance of Z_0, the conventional four-port parameters $\hat{Z}$ are given as (5.14) below. From the appendix, the reduced three-port parameters Z of the coupler are given as (5.15).

$$\hat{Z} = Z_0 \begin{bmatrix} 0 & +j & -j\sqrt{2} & 0 \\ +j & 0 & 0 & -j\sqrt{2} \\ -j\sqrt{2} & 0 & 0 & +j \\ 0 & -j\sqrt{2} & +j & 0 \end{bmatrix} \tag{5.14}$$

$$Z = Z_0 \begin{bmatrix} 0 & +j & -j\sqrt{2} \\ +j & 2 & -\sqrt{2} \\ -j\sqrt{2} & -\sqrt{2} & 1 \end{bmatrix} \tag{5.15}$$

Inserting the above three-port parameters (Z) into (5.12) and (5.13) results in

$$Z_{Lm1M} = Z_{Lm2M} = Z_0(1 - \alpha_M\sqrt{2})$$
$$Z_{LcM} = Z_0 \tag{5.16}$$

$$Z_{Lm1B} = Z_{Lm2B} = Z_0 \tag{5.17}$$

In the above sets of equations, θ_m is set to 90° to account for the phase delay between the two branches of the coupler. This, in turn, determines the value of θ_c, as there only exists one solution of $\theta_c = 90°$ that produces a resistive load in (5.12) and (5.13).

$$\theta_m = \theta_c = 90° \tag{5.18}$$

Equation (5.17) indicates that the characteristic impedance Z_0 of coupler can be chosen to be equal to the optimum class B back-off load of main-PA. This eliminates the need for an output matching network in the main PAs. In [62], for example, a 25-Ω characteristic impedance coupler is used. Given the permittivity (ϵ_r) and thickness of the substrate, however, the Z_{Lm1B} (determined from the load-pull) may potentially be an unrealizable impedance. In this case, an output matching network is added, which effectively transforms the Z_{Lm1B} to a realizable value of Z_0. In either case, the following analysis applies.

The two impedances Z_{Lm1M} at peak and Z_{Lm1B} at back-off are related as:

$$Z_{Lm1B} = \frac{Z_{Lm1M}}{\beta_{bo}} \tag{5.19}$$

By substituting (5.16) and (5.17) into (5.19), we derive the relationship between the current factor α_M and drive level where the class C transistor conducts, β_{bo}, as follows:

$$\beta_{bo} = 1 - \alpha_M\sqrt{2} \qquad \text{or} \qquad \alpha_M = \frac{1 - \beta_{bo}}{\sqrt{2}} \tag{5.20}$$

Now, the optimal load termination for the control PA Z_{LcM} is discussed. For maximum efficiency of the control PA, the maximum fundamental drain voltage swing V_{cM} is equal to the drain dc supply voltage $V_{DS,c}$ (assuming zero knee voltage). This drain dc supply of the control PA can be related to the drain dc supply of main transistor 1 $V_{DS,m1}$ through a factor x. Thus, Z_{LcM} can be expanded to

$$Z_{LcM} = \frac{V_{cM}}{|I_{cM}|} = \frac{V_{DS,c}}{\alpha_M I_{m1M}} = \frac{xV_{DS,m1}}{\alpha_M I_{m1M}} = \frac{xZ_{Lm1M}}{\alpha_M} \tag{5.21}$$

With (5.16), the relationship between the two dc supply voltages therefore depends on β_{bo} as:

$$V_{DS,c} = V_{DS,m}\left(\frac{1-\beta_{bo}}{\sqrt{2}\beta_{bo}}\right) \tag{5.22}$$

We note that for very large back-off ranges the supply voltage scaling determined by (5.22) may become impractically large. In our design example [Section 5.5], the main transistors are biased at a supply of 24 V, slightly reduced from the devices' nominal 28 V supply, to allow for a 34 V supply for the control transistor.

5.1.3 Output dynamic range and input drive back-off ratio

The relationship between the dynamic range of efficiency enhancement γ and the input drive level back-off β_{bo} is found from the following power relationship: the total power at peak is equal to the total power at back-off multiplied by γ, i.e.

$$P_{\text{out,total,M}} = \gamma P_{\text{out,total,B}} \tag{5.23}$$

This expression can be expanded to explicitly consider the contributions from the individual PAs as:

$$P_{\text{out,m1,M}} + P_{\text{out,m2,M}} + P_{\text{out,c,M}} = \gamma\left(P_{\text{out,m1,B}} + P_{\text{out,m2,B}}\right) \tag{5.24}$$

This can be simplified to relate the dynamic range of efficiency enhancement to input drive back-off as:

$$\gamma = \left(\frac{1+\beta_{bo}}{2\beta_{bo}}\right)^2 \qquad \text{or} \qquad \beta_{bo} = \frac{1}{2\sqrt{\gamma}-1} \tag{5.25}$$

5.1.4 Relative Transistor Size

The next step in the D-LMBA design is to determine the relative size of the main transistors compared to the control transistor, S_c, in terms of β_{bo}. From the definition of α_M:

$$|I_{cM}| = \alpha_M |I_{m1M}| \tag{5.26}$$

Substituting the maximum fundamental current magnitude from (5.5)-(5.6) and α_M from equation (5.20) gives:

$$\frac{S_c I_{\text{MAX},m}}{\pi(\beta_{bo}-1)}(\beta_{bo}\sqrt{1-\beta_{bo}^2} - \cos^{-1}\beta_{bo}) = \frac{1-\beta_{bo}}{\sqrt{2}}\frac{I_{\text{MAX},m}}{2} \tag{5.27}$$

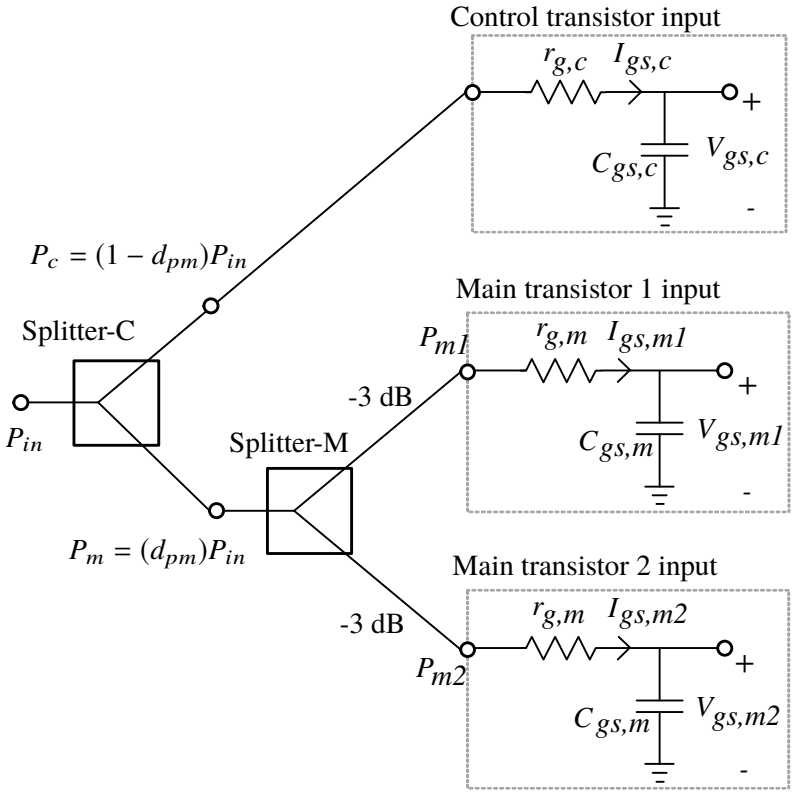


Figure 5.3: Generalized schematic of the D-LMBA input network. The transistor inputs are modeled with series resistance r_g and shunt capacitance C_{gs}.

Re-arranging the above equation:

$$S_c = \frac{\pi}{2\sqrt{2}} \frac{(1 - \beta_{bo})^2}{\cos^{-1}(\beta_{bo}) - \beta_{bo}\sqrt{1 - \beta_{bo}^2}} \tag{5.28}$$

Equation (5.28) highlights that the size of the control transistors scales with the input backed-off drivel level, or in other words, the relative sizing is determined by the dynamic range of efficiency enhancement.

5.2 Input power split ratios

In the RF-input LMBA architecture, the signal driving the control PA is directly derived from the modulated RF input signal. In previous related implementations [46, 57], two stages of 3-dB couplers were used at the input to generate the input signals to the control PA and the two main PAs. This design choice was based on the convenience of using identical, commercial off-the-shelf couplers. Here, we instead consider an arbitrary power ratio to the main and control PAs for optimal efficiency performance.

Fig. 5.3 shows the block diagram of the RF-input LMBA input power-splitting strategy. Let the total input power of the system be P_{in}. The power divider closest to the input, splitter-C, has a division ratio of $P_m : P_c$, where P_c represents the total input power to the control transistor and P_m represents the total input power to the balanced PA. Consider the power division factor of splitter-C, d_{pm}, defined as:

$$P_m = d_{pm} P_{in} \tag{5.29}$$

$$P_c = (1 - d_{pm}) P_{in} \tag{5.30}$$

Splitter-C is followed by a second power divider, splitter-M, in the balanced PA path (shown in Fig. 5.3). Following the conventional balanced amplifier design, splitter-M is a 90° hybrid coupler and constitutes the input part of the balanced amplifier. It evenly divides the signal, thus providing equal power to both the main transistors:

$$P_{m1} = P_{m2} = P_m/2 \tag{5.31}$$

The transistor inputs are modeled with gate parasitic elements in order to analyze the effect of relative transistor scaling on d_{pm} and to calculate the gain of the system. The gate parasitics are represented as a series gate resistor (r_g) and shunt gate to-source capacitor (C_{gs}). This approach was proposed in [63] to analyze the power splitting strategy between auxiliary and carrier amplifier transistors in a DPA system. Here, the same strategy is extended to analyze the power splitting among three transistors. Although this simplified model does not take into account the input impedance dependencies on power level, bias conditions, load termination, and package parasitics, it allows for a qualitative comparison with other architectures. In practice, the transistor nonlinearities not captured in this analysis will affect overall performance. For example, nonlinear output capacitance will cause "bending" of the loading trajectories as shown in simulation in Section 5.5. The input split model can be made more accurate by including nonlinear behavior of C_{gs} due to gain compression through the Miller effect [64, 65]. However, this will increase the mathematical complexity of the model and is outside the scope of this thesis.

Assuming the gate parasitics scale linearly with the transistor size, the resistance and capacitance scale as:

$$r_{g,c} = r_{g,m}/S_c \tag{5.32}$$

$$C_{gs,c} = C_{gs,m} S_c \tag{5.33}$$

Note that the gate parasitics of control transistors are denoted with suffix c and that of main transistors with suffix m.

It is assumed that all three transistors are conjugately matched at the input for maximum gain. In that scenario, the maximum power at the input of main transistor 1 and the control transistor are given as:

$$P_{m1} = 0.5 \times |V_{gs,\max,m1}|^2 (\omega_0 C_{gs,m})^2 r_{g,m} \tag{5.34}$$

$$P_c = 0.5 \times |V_{gs,\max,c}|^2 (\omega_0 C_{gs,c})^2 r_{g,c} \tag{5.35}$$

where $V_{gs,\max}$ is the maximum fundamental gate-source voltage. With (5.32) and (5.33), the maximum gate-source voltages can be expressed as:

$$|V_{gs,\max,m1}|^2 = \frac{2 \times P_{m1}}{(\omega_0 C_{gs,m})^2 r_{g,m}} = \frac{d_{pm} P_{in}}{(\omega_0 C_{gs,m})^2 r_{g,m}} \tag{5.36}$$

$$|V_{gs,\max,c}|^2 = \frac{2 \times (1 - d_{pm}) P_{in}}{(\omega_0 C_{gs,m})^2 r_{g,m} S_c} \tag{5.37}$$

The ratio of (5.36) and (5.37) gives an input voltage ratio V_R:

$$V_R^2 = \frac{V_{gs,\max,c}^2}{V_{gs,\max,m}^2} = \frac{1 - d_{pm}}{0.5 d_{pm} S_c} \tag{5.38}$$

Re-arranging the equation gives:

$$d_{pm} = \frac{1}{1 + 0.5 V_R^2 S_c} \tag{5.39}$$

The voltage ratio V_R can also be expressed in terms of transistor voltage bias conditions as

$$V_R = \frac{V_{gs,\max,c}}{V_{gs,\max,m}} = \frac{V_{SAT} - V_{GS,c}}{V_{SAT} - V_{GS,m}} \tag{5.40}$$

where V_{SAT} is the saturation voltage. The main PAs are biased in class B, therefore $V_{GS,m} = V_{TH}$. At the predetermined drive level β_{bo}, the control transistor does not conduct. In other words, the time domain gate-source voltage $v_{GS,c}$ reaches the threshold voltage V_{TH}. Using (5.3), which can be re-written as

$$V_{GS,c} = \frac{V_{TH} - \beta_{bo} V_{SAT}}{1 - \beta_{bo}}, \tag{5.41}$$

and combining (5.41) in (5.40), yields

$$V_R = \frac{1}{1-\beta_{bo}} \tag{5.42}$$

Substituting S_c from (5.28) and V_R from (5.42) into (5.39) gives the power split ratio in terms of β_{bo}

$$d_{pm} = \left[1 + \frac{\pi}{4\sqrt{2}\left(\cos^{-1}(\beta_{bo}) - \beta_{bo}\sqrt{1-\beta_{bo}^2}\right)}\right]^{-1} \tag{5.43}$$

Equation (5.43) highlights that the desired power division between the control and the balanced PA is decided alone by the dynamic range of efficiency enhancement γ. Note that d_{pm} could alternatively be implemented as a single, four-port power splitting network instead of as a corporate structure.

5.3 Comparison to Other Load Modulation PAs

In this section, the ideal single-frequency performance of the D-LMBA is evaluated and compared to the ideal performance of the conventional DPA, the outphasing PA with non-isolating power combining, and a PA with dynamic load modulation (DLM), i.e. direct modulation on a single transistor. The analysis of the ideal DPA performance [63] is similar to the analysis in Section 5.1. For the outphasing PA, two equally sized transistors are assumed. For DLM, a single class B transistor with direct resistive modulation is assumed. For an equitable comparison, β_{bo} is generalized and can be seen as a measure of output power back-off of a single branch in the main PA (or just the single branch in DLM). Assuming the fundamental drain voltage has maximum swing at peak power and the back-off point, we have

$$\frac{P_{del,\textit{main branch,back-off}}}{P_{del,\textit{main branch,peak-power}}} = \frac{0.5 \times I_{ds,bo} V_{ds}}{0.5 \times I_{ds,peak} V_{ds}} = \beta_{bo} \tag{5.44}$$

Design parameters of the four approaches are compared in Table 5.1. This table summarizes the following design parameters versus the generalized β_{bo}: the dynamic range of efficiency enhancement γ; the relative size factor S_c, which relates the control PA to the main PA-1 for the RF-input LMBA, the auxiliary PA to the carrier PA for the DPA, and the two branches in the outphasing PA; the gain compression; the input power split factors, which is between the control PA and the balanced PA for the RF-input LMBA, the auxiliary

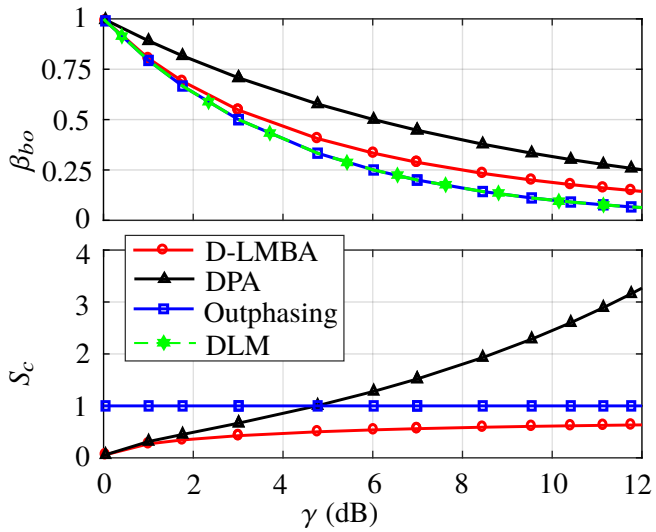


Figure 5.4: The generalized β_{bo} [see (5.44)] and the relative size of the control transistor S_c versus the dynamic range of efficiency enhancement γ.

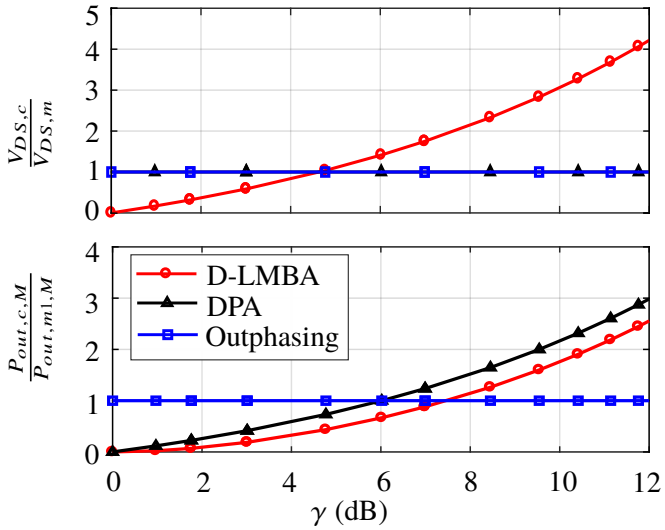


Figure 5.5: Drain supply voltage ratio and maximum output power ratio of branch PAs of load modulation architectures plotted versus the dynamic range of efficiency enhancement γ.

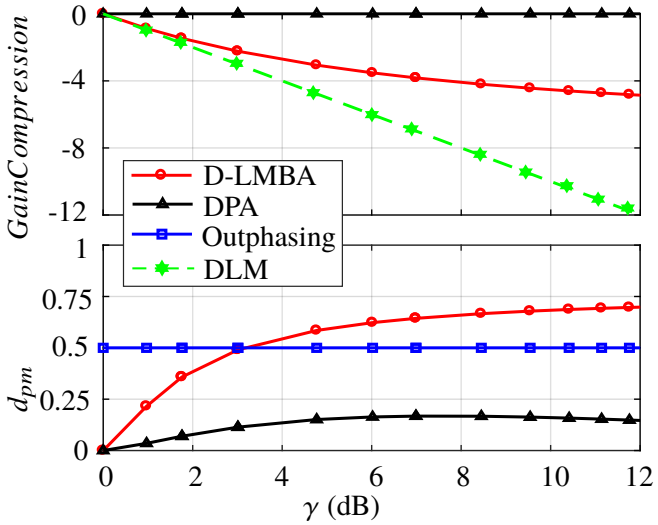


Figure 5.6: Gain compression and power division factor d_{pm} of load modulation architectures plotted versus the dynamic range of efficiency enhancement γ.

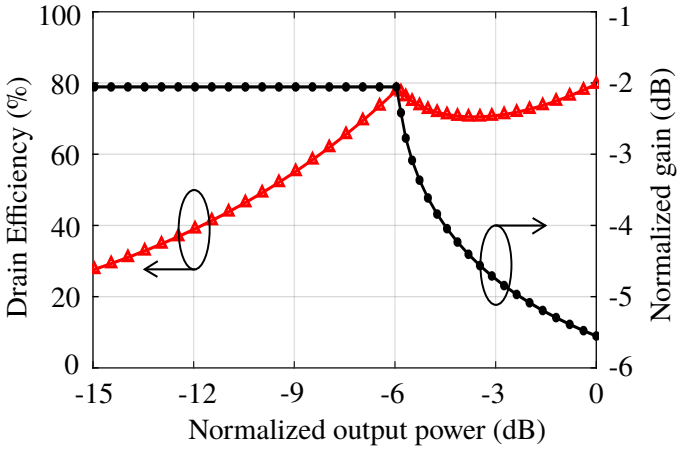


Figure 5.7: Ideal drain efficiency and normalized gain of the RF-input LMBA versus normalized output power. The gain is normalized to conventional class B PA gain. Under ideal conditions, the small signal gain of the RF-input LMBA is 2.05 dB lower than the conventional class B.

Table 5.1: Design parameters for different load modulation architectures

Parameter	RF-input LMBA	Doherty PA	Outphasing	DLM
Dynamic range of efficiency enhancement γ	$\left(\frac{1+\beta_{bo}}{2\beta_{bo}}\right)^2$	$\frac{1}{\beta_{bo}^2}$	$\frac{1}{\beta_{bo}}$	$\frac{1}{\beta_{bo}}$
Relative size of the control transistor S_c	$\frac{\pi}{2\sqrt{2}}\frac{(1-\beta_{bo})^2}{\cos^{-1}(\beta_{bo})-\beta_{bo}\sqrt{1-\beta_{bo}^2}}$	$\frac{\pi}{2}\frac{(1-\beta_{bo})^2}{\beta_{bo}\left(\cos^{-1}(\beta_{bo})-\beta_{bo}\sqrt{1-\beta_{bo}^2}\right)}$	1	–
Gain compression	$\left(\frac{1+\beta_{bo}}{2}\right)^2$	1	–	β_{bo}
Power division factor of splitter-C d_{pm}	$\frac{1}{1+\frac{\pi}{4\sqrt{2}\left(\cos^{-1}(\beta_{bo})-\beta_{bo}\sqrt{1-\beta_{bo}^2}\right)}}$	$\frac{1}{1+\frac{\pi}{2\beta_{bo}\left(\cos^{-1}(\beta_{bo})-\beta_{bo}\sqrt{1-\beta_{bo}^2}\right)}}$	$\frac{1}{2}$	–
$\frac{V_{DS,c}}{V_{DS,m}}$	$\frac{1-\beta_{bo}}{\sqrt{2}\beta_{bo}}$	1	1	–
$\frac{P_{\text{out,c,M}}}{P_{\text{out,m1,M}}}$	$\frac{(1-\beta_{bo})^2}{2\beta_{bo}}$	$\frac{1}{\beta_{bo}}-1$	1	–

PA and the carrier PA for the DPA, and between the two branches in the outphasing PA; the relative dc drain supply voltage; and the maximum output power ratio, which relates the control PA power to the main PA-1 power for the LMBA, and the auxiliary PA power to the carrier PA power for the DPA.

In Fig. 5.4, the relative size factor S_c and the generalized β_{bo} are plotted versus the dynamic range of efficiency enhancement γ. For a given γ, the main transistor has to be backed off the least for the DPA, somewhat more for the RF-input LMBA, and the most for the outphasing PA and DLM PAs. A real transistor has a limited dynamic range over which high efficiency can be maintained through load modulation [66]. Thus, the higher the β_{bo} for a large value of γ, the higher the efficiency a real transistor would present. For large values of γ, the size factor becomes large for the DPA, whereas it remains low for the RF-input LMBA. This is explained by the β_{bo} dependence of the dc bias voltage $V_{DS,c}$. A more fair comparison is, therefore, the power ratio of the control/auxiliary PA versus single main/carrier PA. This power ratio and

the drain dc voltage ratio are plotted versus γ in Fig. 5.5. The power ratio remains lower for the D-LMBA compared to the DPA for all values of γ. However, the control PA drain dc supply becomes very large relative to the main PAs for large values of γ for the D-LMBA. The main PA dc supply voltage could be selected such that the transistor is underutilized in order to counteract this asymmetry in bias voltages. In practice however, the asymmetry in drain supplies limits the ranges of possible values of γ for the D-LMBA. An interesting extension to this analysis, although outside the scope of this work, would be to analyze the efficiency compromise that results from placing a practical limitation on the drain supply levels when designing to higher PAPR specifications.

In Fig. 5.6, the gain compression and the input split factor d_{pm} are plotted versus γ. Since the class C biased control/auxiliary PA is off at back-off, all power going to that branch is wasted at low power levels. Thus, the split factor d_{pm} corresponds to the small signal gain loss compared with a conventional class B PA for the LMBA and DPA. The DPA ideally has a flat gain over the output power range, while the D-LMBA presents some gain compression, but DLM presents more. An ideal class B PA has a gain proportional to the resistive load. In practice, of course, real transistors will not exactly follow the simplistic modeling of the transistor input parasitics in this comparison. Thus, d_{pm} and the gain compression here represent a relative (rather than absolute) comparison between the different architectures. As an example, the efficiency and the gain (normalized to conventional class B PA gain) for an RF-input LMBA with γ = 6 dB are shown in Fig. 5.7. Similar results for LMBA with γ = 6 dB were reported in [62].

This single-frequency comparison of ideal performance shows that the RF-input LMBA presents some advantages compared to other load modulation architectures. In particular, the LMBA requires a small control PA resulting in a low small signal gain loss (when the control PA is off). Due to the asymmetry in drain biases, however, the practical values of the dynamic range of high efficiency γ is limited.

5.4 Design Methodology

This section describes a concrete design methodology for the D-LMBA. The methodology utilizes closed-form equations for various design parameters derived in the previous section. The detailed design procedure

is as follows:

Step 1: Select the total output power $P_{\text{out,total,M}}$ and the dynamic range of efficiency enhancement γ for the RF-input LMBA. The required $P_{\text{out,total,M}}$ dictates device technology and approximate combined periphery for the three transistors. Next, select γ based on the peak to average power ratio (PAPR) of the modulating signal. According to the theory in Section 5.1, the γ ratio corresponds to the power level of the second efficiency peak. In theory, this second peak gives the ideal class B efficiency. Hence, it is logical to use the expected signal PAPR as the design choice for γ.

Step 2: Calculate the design parameters. First, calculate the back-off drive level β_{bo} from (5.25) and then calculate the current ratio α_M and relative size factor S_{c} from (5.20) and (5.28), respectively. Note that the back-off level γ alone determines the value of all the above design parameters.

Step 3: Based on $P_{\text{out,total,M}}$ and the relative size factor S_{c}, select appropriate transistors for the main and control PAs.

Step 4: Select the gate and drain bias voltages for the transistors. The drain supply for the main transistors can be selected from the data sheet, and the drain supply for the control transistor is calculated from (5.22). It is also possible to underutilize the main transistor slightly by selecting a lower drain dc supply than what is specified in the data sheet, in order to incorporate a larger value of the control PA, which is required for large values of γ. Furthermore, the gate bias of the main transistors is set to V_{TH}, and the gate bias of the control PA is found in (5.41).

Step 5: Design the passive system components: splitter-C and the input and output couplers. Determine the d_{pm} from (5.43) and design splitter-C with the input port characteristics impedance of 50 Ω (source impedance). Design equations for an uneven Wilkinson splitter can be found in [67].

The input and output couplers along with the main PAs form part of the balanced amplifier. To maintain symmetry in the balanced amplifier, both the couplers need to be designed identically. Hence, the characteristic impedance of the couplers Z_0 can be chosen in two different ways. Z_0 can be chosen equal to the optimal back-off impedance for the main PAs Z_{Lm1B}, as explained in Section 5.1.2, or equal to that of the *P2* port of the power divider (see Fig. 5.8). In either case, an extra impedance transformation will be eliminated. The theory and design equations for the hybrid branch-line couplers can be found in [68].

Step 6: Design the PA sub-circuits, i.e., the two main PAs and the control PA. The output match of the main PAs can be designed in two ways depending on the selection of Z_0 of output coupler. If the coupler is designed in accordance with (5.17), then no impedance transformation is needed. On the other hand, in cases where the characteristic impedance of Z_{Lm1B} is difficult to realize on the given substrate, then a matching network can be added to transform the class B impedance Z_{Lm1B} to some suitable value of Z_0 (such as 50 Ω). The inputs of both main PAs are conjugately matched to the chosen Z_0 of the input coupler.

The class C biased control PA is conjugately matched to the port impedance from the uneven splitter at the input. At the transistor's output, a matching network is added to transform the load found from the loadpull simulation to the chosen Z_0 of the output coupler.

5.5 D-LMBA Design Example

The methodology presented in Section 5.4 is demonstrated with a 25-W PA design example. The proof-of-concept prototype is designed to operate with $\gamma = 6$ dB and a center frequency of 2.4 GHz. The corresponding design parameters, i.e., β_{bo}, S_c and α_M, are summarized in Table 5.2 and a detailed schematic is given in Fig. 5.8. The D-LMBA prototype is not designed with wideband operation in mind, because the goal is to validate the presented theory. We note, however, that the technique presented in [57] for wideband RF-input LMBA operation could be applied to this topology.

For the main PAs, two 10-W GaN packaged transistors from Wolfspeed (CGH40010F) are selected. Based on the value of S_c, the required control transistor required roughly half of the maximum dc current compared to one main transistor. This approximately corresponds to the 6-W GaN packaged transistor from Wolfspeed (CGH40006P), which was therefore chosen as the control transistor. The drain supply voltage for the main transistor is chosen as 24 V. The drain supply for the of control transistor is calculated as 34 V, according to (5.22). We note that the high supply voltage needed for the control PA required the main PA supply voltage to be reduced from its nominal 28-V value.

The d_{pm} of splitter-C determines the power division between the control and balanced PAs. The *P1* port of the power divider is connected to the control PA, whereas the *P2* port is connected to the input coupler

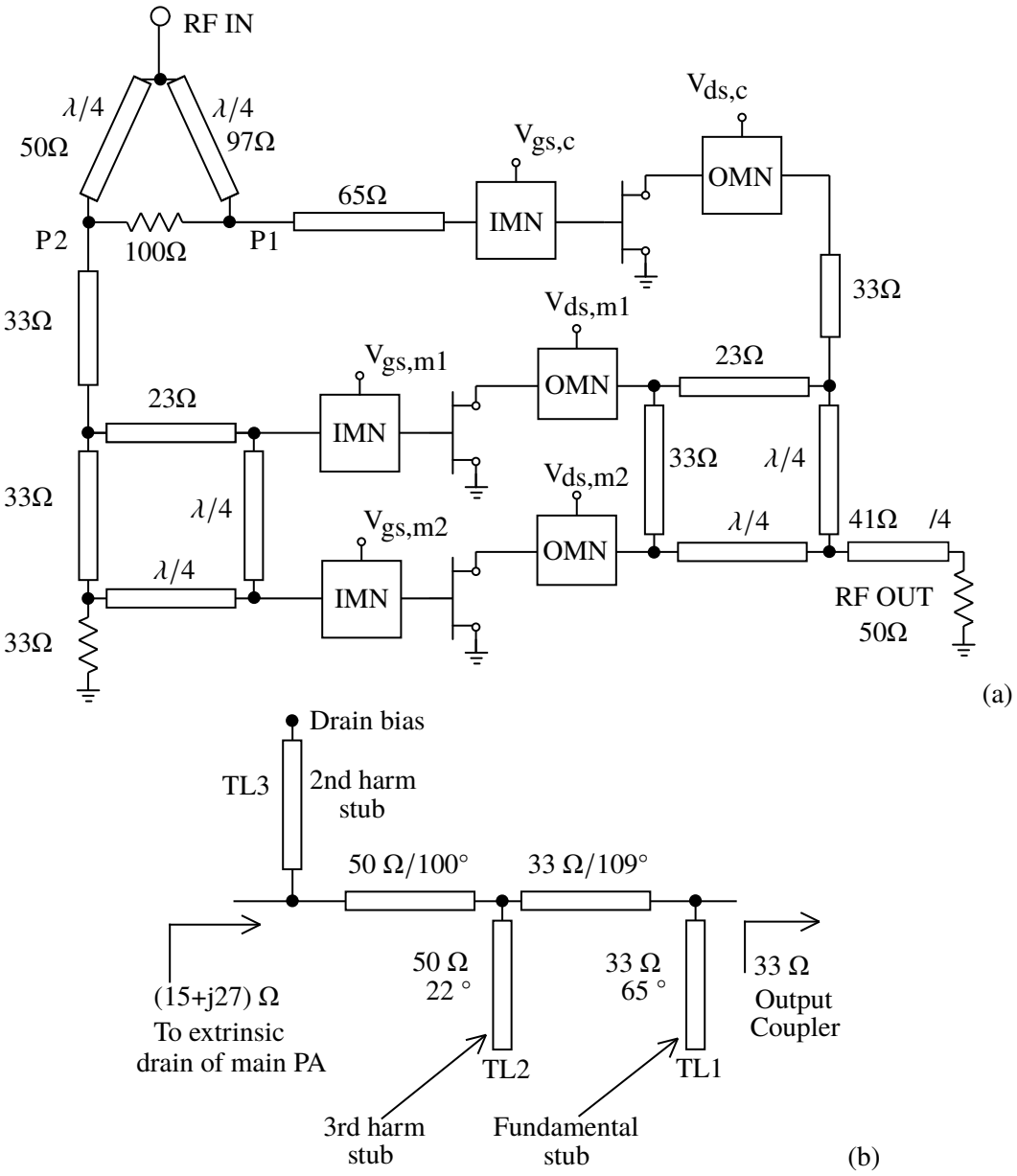


Figure 5.8: Schematic of (a) the RF-input LMBA architecture showing the design values for each system component, (b) details of the main PA OMN.

Table 5.2: Design summary for the prototype RF-input LMBA

γ	β_{bo}	α_M	S_c	d_{pm}	$V_{DS,m}$	$V_{DS,c}$	Z_{Lm1B}	Z_{LcM}
6 dB	0.3334	0.471	0.539	0.623	24 V	34 V	$15 + j27\Omega$	$28 + j88\Omega$

(See Fig. 5.8(a)).

For the input and output couplers, a branch-line topology is selected. The input coupler is designed to have a characteristic impedance equal to that of the *P2* port of the power divider (33-Ω). This reduces the necessary impedance transformation between the splitter and coupler.

The main PAs are connected between the input and output coupler. The input match network conjugately matches the input impedance of the main PA to 33 Ω. The series stability network is a part of input match and consists of the parallel combination of a 15-Ω resistor and 10-pF capacitor.

Fig. 5.8(b) shows the output matching network of the main PAs. It consists of an impedance match, harmonic termination and bias network. The network transforms the 33-Ω impedance of the coupler to the optimal back-off impedance of the main transistor, i.e. $Z_{Lm1B} = (15 + j27)$ Ω, which is found from loadpull. The network is designed using two open-circuited stubs so it can be tuned easily after fabrication. The fundamental impedance is adjusted using the TL1 stub whereas the third harmonic is controlled using the TL2 stub. For an improved PAE match, the effect of the third harmonic termination is evaluated in the simulations by sweeping the reflection coefficient phase. It was found that the third harmonic is less sensitive to the phase variation from $-15°$ to $190°$ and hence terminated accordingly. The second harmonic is terminated in a short circuit at the intrinsic drain using a quarter-wave stub (TL3) which also acts as the drain bias line.

The control PA IMN is designed to transform the conjugate input impedance of the 6-W packaged transistor to 65 Ω, whereas the output matching network transforms Z_{LcM} found from the loadpull simulations to 33 Ω. The θ_c phase shift is implemented with a microstrip line and is placed before the input matching network of the control PA.

Finally, at the output port a quarter-wave line is used to transform the 33-Ω coupler impedance to the 50-Ω load.

Fig. 5.9 shows the simulated load modulation trajectories at the extrinsic drain of the transistors as the total input power of the system (P_{in}) is swept from 27 dBm to 35.4 dBm. For comparison purposes, load-pull contours at the same impedance plane are also shown for the two device types. The load trajectories of the main PAs suggest that at the back-off power in the absence of the control signal, the OMN of the main PAs

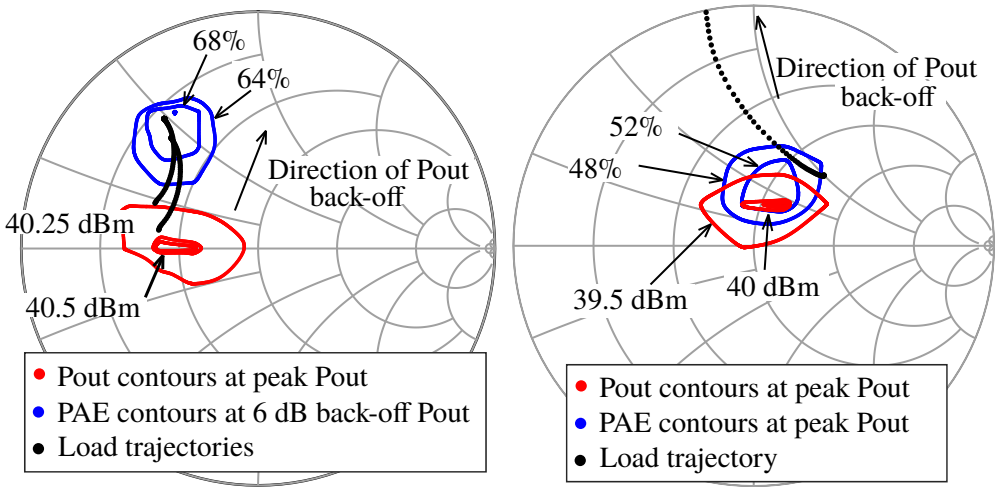


Figure 5.9: Simulated load impedance trajectories when the input power is swept from 27 dBm to 35.4 dBm at the extrinsic drain (package plane) of (a) balanced PA devices, and (b) the control PA. Simulated load pull contours at the same reference plane and corresponding to the peak input power level are shown for comparison.

presents the optimum PAE match. As the control PA starts to conduct, the main PAs are load modulated and are matched near the 40.25-dBm P_{out} contour. The difference in the load trajectories of the main PAs in the peak power region is attributed to the imbalance in the output coupler. In the back-off region, the control PA impedance is seen to be at $|\Gamma| = 1$ and at the peak power, the control load is modulated to match the impedance near the 52% PAE contour.

Fig. 5.10 shows the intrinsic fundamental drain currents of all three transistors for the EM-simulated circuit and for the ideal equations. The ideal currents are plotted versus the normalized input drive level β for a design value of $\beta_{bo} = 0.33$. Because the EM-simulated circuit is driven into compression, β exceeds 1; ideal currents are plotted to $\beta = 1$ since the theory does not address the compression characteristics of the transistor. Here, the input drive level is normalized with a value that corresponds to $P_{in} = 34$ dBm and $P_{\text{out,total}} = 45.06$ dBm. It is observed that the overall main PA current behavior closely follows the theoretical case. The asymmetry between the two main PA currents for high powers is attributed to the different load modulations. This is also evident from the load trajectories in Fig. 5.9. The maximum value of control PA in the simulated design is observed to be higher than the ideal case which is consistent with the fact that the control transistor size utilized in the design is bigger than the theoretical calculations.

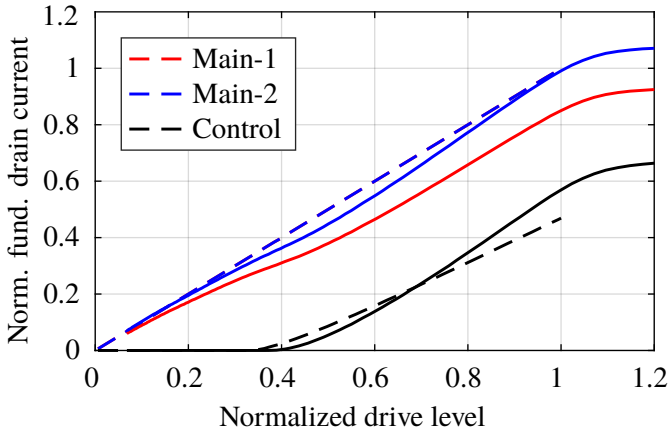


Figure 5.10: Ideal and EM simulated fundamental drain currents of the two main transistors and the control transistor versus normalized input drive level β.

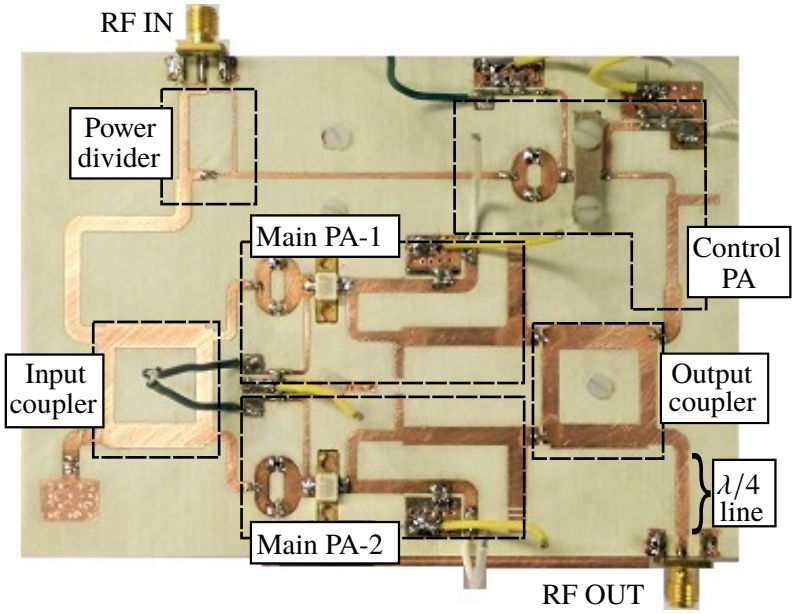


Figure 5.11: Photograph of the fabricated D-LMBA prototype, measuring 14 × 10 cm.

5.6 Experimental Results

Fig. 5.11 shows the photograph of the D-LMBA prototype. The PA is fabricated on Rogers RO4350 substrate with a dielectric constant of 3.48 and a thickness of 30 mil.

CW measurements are performed with a single-tone 2.4-GHz signal. Fig. 5.12 shows the simulated and measured total system PAE. The measured PAE remains above 50% throughout the 6-dB OBO range and is measured to be 60% at the peak power of 45.6 dBm. Moreover, the plot clearly depicts a back-off

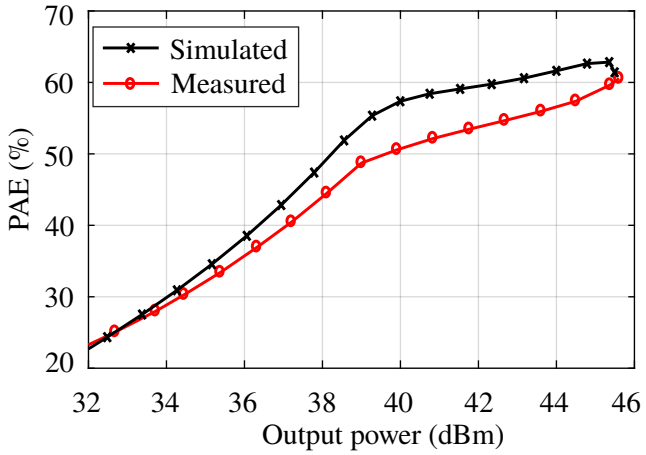


Figure 5.12: Total system PAE comparison between measurement and simulation results. Both plots demonstrate efficiency enhancement over 6-dB OBO.

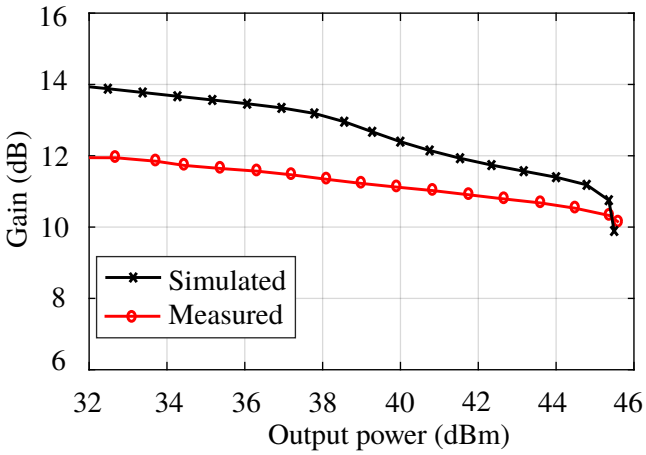


Figure 5.13: Measured and simulated system gain vs. output power.

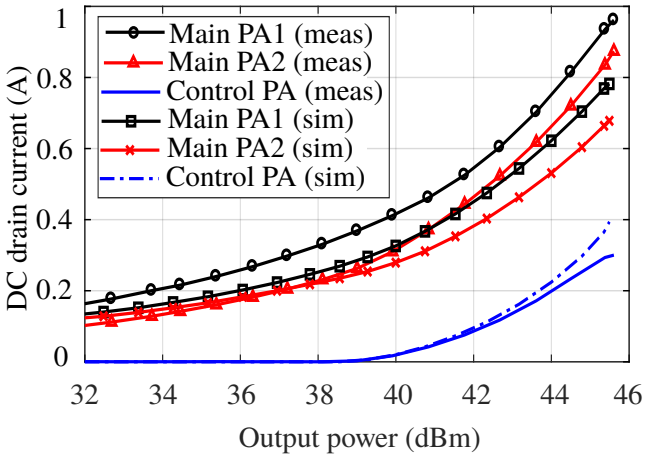


Figure 5.14: Measured and simulated drain dc current from all three transistors.

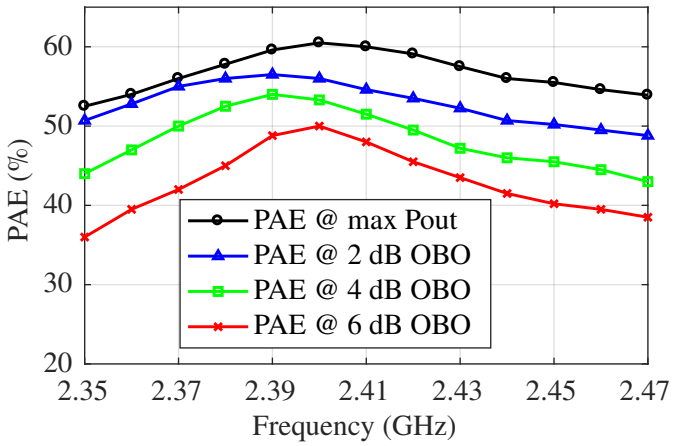


Figure 5.15: Measured total system PAE over 2.35 GHz to 2.47 GHz at 0, 2, 4 and 6-dB of OBO. The total system PAE at 6-dB back-off is measured to be more than 40% over 2.362 to 2.45 GHz.

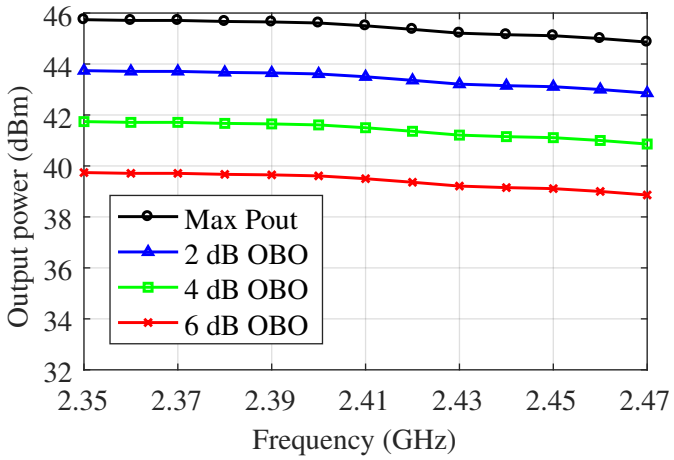


Figure 5.16: Measured output power over 2.35 GHz to 2.47 GHz at 0, 2, 4 and 6-dB of OBO. Over the frequency range the output power remains within ±0.6 dB for all back-off levels.

efficiency characteristic closely related to that of a DPA. The simulated PAE plot matches closely with the measured PAE. However, a discrepancy of 5-8 points is observed, attributed to losses in the connectors, lumped components, PCB etc. Note that the above efficiency plots take into account the dc power consumed by all three transistors.

Fig. 5.13 shows the simulated and measured system gain plotted versus the output power. The system gain is measured to be 12-dB in linear region and is 2-dB lower than the simulated gain. The discrepancy in the gain in the lower power region is attributed to potential model inaccuracies of the off-state of the class C biased control PA. We believe that an inaccurately modeled off-state impedance has lowered the system

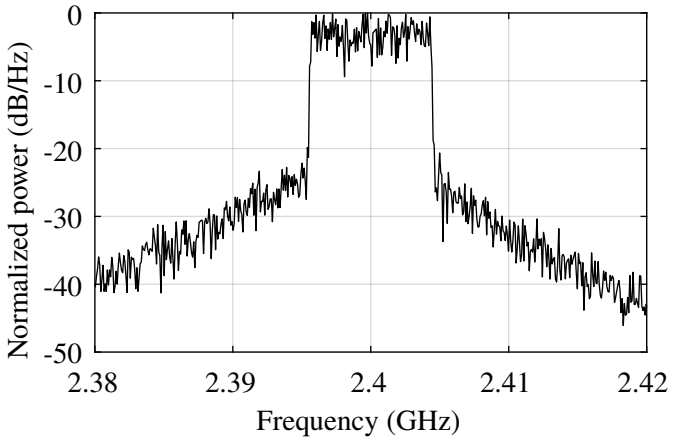


Figure 5.17: Output power spectrum of a 10-MHz LTE signal with a measured PAPR of 7.5 dB showing the unlinearized ACLR of -27 dBc.

gain at the back-off power levels, thus causing the measured gain compression characteristic to differ from the simulated one. Similar observations were also reported in previous DPA work [61, 69].

Fig. 5.14 compares the simulated and measured dc drain supply current of all three transistors plotted against output power. For the prototype characterization, the drain voltages of the three transistors are set as per the theory presented above. The gate voltages of the three transistors are slightly tuned to account for the device variability and tolerances. The final bias voltages are selected as a compromise between the system gain and the back-off PAE. The measured current of both main transistors is higher than in simulation by 50-200 mA in the high power region. This corresponds to the 5-8 points loss in measured PAE. The control transistor drain current starts to conduct at around 39 dBm following the expected class C behavior. However, it is noted that the control transistor consumes less current than in simulation, whereas the main transistors consume more current than expected. It is suspected that this discrepancy is due to nonidealities in the power division of splitter-C and inaccuracies in the load impedances presented to the PAs in the high-power region, which can be traced to PCB tolerances and parasitics of lumped components.

The frequency performance of the prototype is measured from 2.35 to 2.47 GHz. Fig. 5.15 shows the total system PAE plotted at various back-off power levels over the frequency band. The peak PAE remains over 58%, and the PAE at 6-dB OBO remains over 40% from 2.362 to 2.45 GHz. The output power is plotted in Fig 5.16. The output power variation remains within ±0.6 dB over 2.35-2.47 GHz for all back-off levels.

Table 5.3: Performance summary and comparison to related state-of-the-art PAs.

Ref./ Year	Architecture	RF inputs	Freq. (GHz)	P_{max} (dBm)	η @ P_{max} (%)	η @ 6 dB OBO (%)	η (%) @ P_{avg}(dBm)/ PAPR(dB)	ACLR (dBc)
[32] 2014	Doherty	1	1.05-2.55	40-41.9*	45-83	35-58	35-50** (35/5.4 dB) 5-MHz 3GPP	-28 ‡
[70] 2015	Doherty	1	2-2.7	41	58-70	36-65	50† (-/8.2 dB) 10-MHz LTE	-49.2 ◇
[71] 2016	Doherty	1	1.6-2.2	46.2-47	60-71	57-63*	50 (36/9.1 dB) 20-MHz LTE	-48 ♯
[72] 2016	Doherty	1	1.94	51.5*	64 *	55*	57 (45.4/6.5 dB) 10-MHz LTE	-48.3 ♯
[38] 2016	LMBA	2	0.8-2	42	65-85 *	50-65 *	-	-
[41] 2017	LMBA	2	4.5-7.5	39	47-77 *	28-60 *	-	-
[46] 2017	RF-input LMBA	1	0.75-0.85	42	57-70	34-48	34.1 (32.8/10 dB) 3.84-MHz WCDMA	-26.8 ‡
[73] 2017	Doherty	1	2.14	43*	62.5*†	57.8†	57(36.9/6.5 dB) 10-MHz LTE	-25 ‡
[57] 2017	RF-input LMBA	1	1.8-3.8	44	46-70	33-49	28(31.8/9 dB) 3.84-MHz WCDMA	-26.6 ‡
[62] 2018	LMBA	2	1.7-2.5	48-48.9	48-58†	43-53†	40†(39/9 dB) 20-MHz LTE	-49 ♯
[74] 2018	ET+Doherty	1	2.4	42	63	49	48* (34.1/8.6 dB) 10-MHz LTE	-30 ‡
[75] 2018	Doherty	1	1.5-3.8	42.3-43.4	42-63	33-55	33*** (34/9 dB) 7-MHz WiMAX	-48 ♯
This work	D-LMBA	1	2.4	45.6	67	54	47 (38/7.5 dB) 10-MHz LTE	-27 ‡

* - values read from graph, † - PAE value, ** - measured at 1.2, 1.8 and 2.5 GHz, *** - measured at 2.6 GHz ‡ - No DPD, ◇ - memoryless DPD, ♯ - memory DPD

The system linearity is characterized with a long term evolution (LTE) signal centered at 2.4-GHz with a measured PAPR of 7.5 dB. The measured output spectrum of the signal is shown in Fig. 5.17. The measurements show the unlinearized ACLR of -27 dBc at an average output power of 38 dBm and drain efficiency of 47%. A performance comparison to previous LMBAs published to date and DPAs with similar frequency range, output power level, and technology is presented in Table 5.3.

5.7 Conclusion

In this chapter, a theoretical analysis of the RF-input LMBA is presented. The analysis derives the closed-form design equations for various system-level parameters, such as input power split ratio, device sizing, current scaling, and supply-level determination based on a specified back-off range for efficiency enhancement. On the basis of these system-level parameters, the D-LMBA architecture is compared to the commonly used efficiency enhancement techniques.

A design methodology for the RF-input LMBA based on a specified output power and back-off level is proposed. The design technique is experimentally validated through a 2.4-GHz, 45.6-dBm RF-input LMBA prototype demonstrating peak CW PAE of 60% and back-off PAE of 50% over a 6-dB back-off range. The resulting RF-input LMBA has performance on par with state-of-the-art DPAs, but it has a relatively favorable device scaling ratio between the main and control PA devices.

Chapter 6

Summary and Future Work

This last chapter summarizes the thesis and describes some directions for future work including an integrated version of the octaveband D-LMBA. In addition, a discussion on increasing the dynamic range of D-LMBA is presented and an active input match concept is proposed.

6.1 Summary

In our first demonstration of the RF-input LMBA, we introduced a "control path" that automatically generates a control signal based on a single modulated RF input. We observed that the load impedance seen by the balanced amplifier transistors can be dynamically modulated as the desired power level changes. Advantages of dynamic load modulation include improved efficiency at backed-off power levels (e.g, 6-8 dB below peak power). The approach eliminates the baseband signal computation that would be required for modulated signals in the previously reported LMBA [38, 41]. However, the RF-input approach trades off with the wide-range load impedance control offered by an externally generated control signal. Other advantages of this approach are reduced system complexity and the ability to operate with many existing calibration and linearization techniques. This first of its kind approach was verified through a narrow-band prototype.

The single RF-input concept was then further extended to achieve the efficiency benefit over more than an octave bandwidth. The octaveband RF-input LMBA not only controls the amplitude of the control signal

as in the previous prototype but also modulates the control signal phase in order to achieve the efficiency match over an octave bandwidth. The frequency compensation approach presented in Chapter 3 exploits the dispersion of a bandpass filter in order to modulate the phase of the control signal with respect to the frequency of operation.

Although the octave RF-input LMBA prototype achieved both goals: efficiency and bandwidth, another variant of RF-input LMBA was developed to push the boundaries of this research and achieve efficiency for more complex modulations schemes whith higher Peak-to-average-power (PAPR) ratios. Our next architecture is the Doherty-LMBA (D-LMBA). Here, we developed a new control scheme of turning on the control PA at the higher output power region and a new approach for pre-matching the balanced amplifiers. The D-LMBA prototype demonstrates a greater range of dynamic load modulation, and therefore improved back-off efficiency, but degradation in bandwidth compared to the RF-input LMBA.

The first prototype of D-LMBA was based on an empirical design approach and it successfully proved the concept. The second prototype was designed based on a theoretical analysis of the D-LMBA architecture. Closed-form design equations for various system-level parameters, such as input power split ratio, relative device sizing, current scaling, and relative drain supply voltages were derived based on a pre-determined back-off range for efficiency enhancement. With the help of the proposed analytical method, the D-LMBA architecture was compared to the commonly used efficiency enhancement techniques.

6.2 Future Work

The major focus of this research is to operate the LMBA on a single RF-input while improving back-off efficiency over a wide bandwidth. The research work presented in this thesis has provided a significant step forward in the development of highly efficient load modulated PA architectures for modern wireless communication systems. The current work opens up various different areas of research on the LMBA. This section discusses possible future directions based on the work undertaken in this thesis.

Integrated version of Octaveband D-LMBA:

The logical continuation of the single frequency D-LMBA prototype presented in Chapter 4 and 5 is

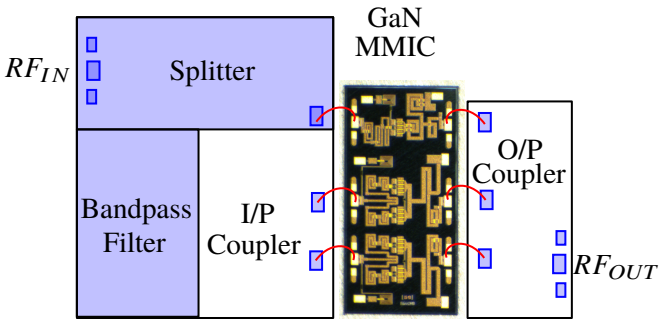


Figure 6.1: A proposed design plan (not to scale) of the integrated version of the octaveband D-LMBA.

to extend the operational bandwidth of the D-LMBA. As a part of continuing this research, an octaveband version of the D-LMBA is being designed to operate over 6-12 GHz. A proposed design plan of octaveband D-LMBA is shown in Fig. 6.2. The passive system components of D-LMBA including power splitter, bandpass filter, couplers will be designed on an Alumina substrate. The control PA, as well as the two main PAs of the balanced PA, have been designed and taped out on Qorvo's 0.15um GaN process. The MMIC PAs are currently under test.

Drain bias voltage scaling of the control PA in the D-LMBA:

The drain biasing of the class-C control PA and class-B main PAs in the D-LMBA is interesting due to the dependance of drain bias of control PA ($V_{ds,c}$) on the dynamic range of efficiency enhancement (γ) as well as drain bias of main PA ($V_{ds,m}$). This relation is derived and described in details in Chapter 5. It is observed that as γ increases, the required ($V_{ds,c}$) also increases. For signals with PAPR ($\geq 9dB$), the value of $V_{ds,c}$ can become very high and difficult to implement even with the high breakdown voltage technologies such as GaN. Hence this topic needs further investigation to make the architecture compatible with high PAPR signals.

RF-input LMBA for active-input match:

The LMBA reported in [38] is based on the idea of injecting the control signal at the output of the transistor to obtain an active match. The same concept can be extended to obtain an active match at the input. This active input match can be used to improve the gain and/or linearity of the PA. The active input match concept is illustrated in Fig. 6.2. The control profiler component can be designed based on the specific requirement of the system and is a subject of future research.

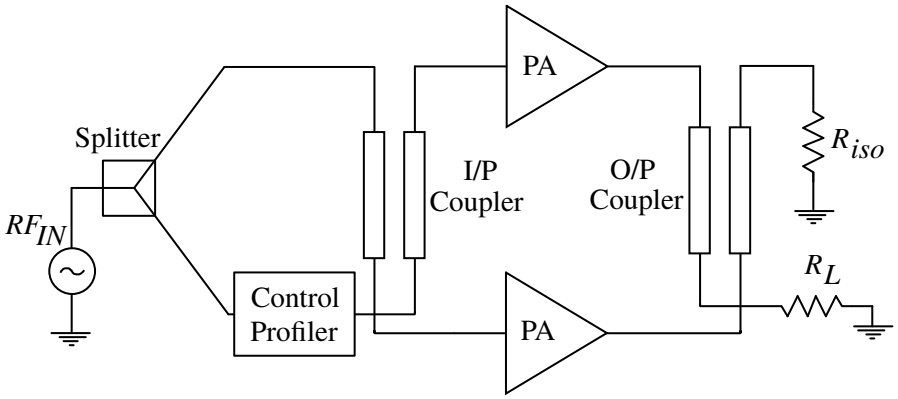


Figure 6.2: A conceptual block diagram of new variant on RF-input LMBA

Miscellaneous topics on RF-input/D- LMBA:

As a continuing research, it will be interesting to investigate the feasibility of the D-LMBA at mm-wave frequencies, specifically for 5G applications. Another interesting topic would be to explore the continuum between D-LMBA and the other load-modulation architectures. Finally, the operational bandwidth of the LMBA can potentially be further extended to achieve Decade bandwidth. For this, design challenges would primarily depend on the bandwidth limitations of the coupler and control PA. A complete study of the ability of the RF-input LMBA to extend to higher frequencies and bandwidths would be of great interest in order to fully understand the capabilities and limitations of this relatively new technique.

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Appendix A

Four-Port to Three-Port Conversion

In Section 5.1.2, the four-port lossless coupler is mathematically represented as a lossy three-port network. The following section derives the equality condition used in 5.9, based on the conversion of lossless four-port Z-parameters (denoted by $\hat{Z}_{ij}$) to lossy three-port Z-parameters (denoted by Z_{ij}).

In the proposed Doherty-like RF-input LMBA architecture, the output coupler is terminated by a resistive load R_L. By treating this R_L as an integral part of the coupler, the resulting network will reduce to lossy three-port as shown in Fig. A.1.

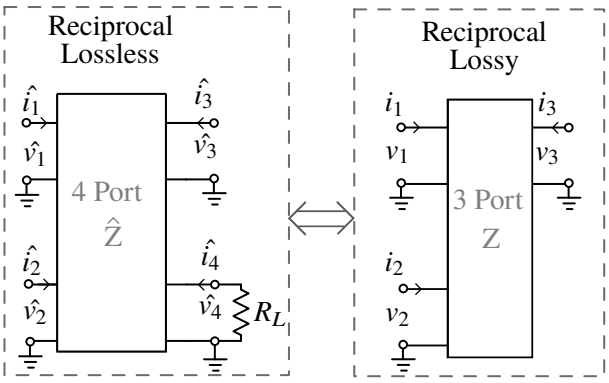

Figure A.1: The reciprocal and lossless four-port network $\hat{Z}$ with the fourth port terminated with a resistive load has an equivalent reciprocal and lossy three-port network Z.

The Z-parameters of this lossy three-port network can be represented in terms of the lossless four-port network as follows:

$$Z_{11} = \hat{Z}_{11} - \frac{\hat{Z}_{14}^2}{R_L - \hat{Z}_{44}} \tag{A.1}$$

$$Z_{22} = \hat{Z}_{22} - \frac{\hat{Z}_{24}^2}{R_L - \hat{Z}_{44}} \tag{A.2}$$

$$Z_{33} = \hat{Z}_{33} - \frac{\hat{Z}_{34}^2}{R_L - \hat{Z}_{44}} \tag{A.3}$$

with cross terms

$$Z_{12} = \hat{Z}_{12} - \frac{\hat{Z}_{14}\hat{Z}_{24}}{R_L - \hat{Z}_{44}} \tag{A.4}$$

$$Z_{13} = \hat{Z}_{13} - \frac{\hat{Z}_{14}\hat{Z}_{34}}{R_L - \hat{Z}_{44}} \tag{A.5}$$

$$Z_{23} = \hat{Z}_{23} - \frac{\hat{Z}_{24}\hat{Z}_{34}}{R_L - \hat{Z}_{44}} \tag{A.6}$$

Requiring the four-port network to be lossless results in the following conditions (similar to [60]):

$$\begin{aligned} \mathrm{Re}(Z_{12})^2 &= \mathrm{Re}(Z_{11})\,\mathrm{Re}(Z_{22}) \\ \mathrm{Re}(Z_{13})^2 &= \mathrm{Re}(Z_{11})\,\mathrm{Re}(Z_{33}) \\ \mathrm{Re}(Z_{23})^2 &= \mathrm{Re}(Z_{22})\,\mathrm{Re}(Z_{33}) \end{aligned} \tag{A.7}$$