

TECHNIQUES TO IMPROVE LED DRIVERS BY REDUCING
VOLTAGE STRESS AND ENERGY STORAGE

by

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Techniques to Improve LED Drivers by Reducing Voltage Stress and Energy Storage

Thesis directed by Associate Professor Regan Zane

High-brightness light-emitting diodes (HB LEDs) provide many advantages over other existing electric light sources, including high efficacy, long lifetime and small form factor. However, the overall lifetime of off-line LED applications is limited by the low-quality electrolytic capacitors utilized for energy storage. In order to use long-life capacitors while limiting cost increase, the required energy-storage capacitance should be reduced, which can be achieved with several techniques addressed in this thesis. The constant input current approach can achieve a power factor (PF) of 0.9, which meets ENERGY STAR requirements, while reducing required energy storage by one-third compared to unity-PF case. When ripple is allowed on the LED current, the trapezoidal LED current approach minimizes energy storage with small control effort. A second stage can significantly reduce required capacitance by allowing large voltage variation on the capacitor, while bidirectional structure helps limit additional power loss. The small form factor of LEDs offers flexibility for diverse and sophisticated design. In order to take this advantage, LED drivers should have a small size or thickness. Series-input structure provides a possibility to apply low-voltage components in high-voltage circuits, while the common duty cycle approach achieves automatic input voltage sharing and LED current copying, which can significantly simplify system design. With reduced rated voltage, integration of semiconductor devices becomes much easier and converters are able to operate at high switching frequencies with small components, both of which lead to high-level monolithic integration. All of the principles and control approaches are verified in experiments, with the results provided in this thesis.

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CHAPTER I

INTRODUCTION

Light-generating equipments play a very important role in human lives. From large outdoor display panels, to general lighting products like street lighting, back lighting for monitors, or even the small power-on indicators, lighting applications penetrate almost every corner of the modern world. The broad utilization of lighting products can be reflected by its electricity consumption as well. For instance, more than 20% of the total electricity usage in United States is consumed by lighting [1, 2]. Due to their extreme importance, lighting products are expected not only to generate high-quality luminance output but also to be power efficient and cost effective.

With continuous technological improvement and innovations, the efficiency of electrical lighting applications has improved significantly. The first major contributor to this efficiency improvement is the advancement of light sources, or light-emitting materials, and the second is the development of power electronic technologies that are necessary to utilize these light sources. The efficiency of light sources can be indexed by efficacy, which represents how much light is developed per unit power consumed by the devices, with the unit of Lumens/Watt. The common electric light sources can be divided into several categories, including incandescent, fluorescent, high intensity discharge (HID), and solid state, as shown in Fig. 1.1. Incandescent lamps, which have been in use for a long time, generate light through blackbody radiation. As a large portion



Figure 1.1: (a) Incandescent lamp, (b) fluorescent lamp, (c) HID lamp, and (d) HB LED devices.

of energy is transferred to heat, the efficacy of incandescent bulbs is only about 10-18 Lumens/Watt. Fluorescent lamps provide much higher efficacy, in the range of 70-90 Lumens/Watt, and have replaced incandescent lamps in many applications. Concerns with fluorescent lamps include their fragile tubes and their mercury-based materials, which are not environmentally friendly. The efficacy of HID lamps is even higher than fluorescent lamps. Similar to fluorescent lamps, some HID lamps lead to concerns about safe disposal. Both fluorescent lamps and HID lamps require ballasts to start and maintain their operation. Solid-state light (SSL) source normally refers to light-emitting diode (LED). For many years, LEDs were utilized majorly in applications requiring small light output, such as signal indicators. With recent advancement in materials and manufacturing process, high-brightness LEDs are attracting

more and more interest from both academia and industry, as they provide great potential for future lighting applications.

Compared to incandescent or discharge lamps, LEDs produce luminance output on a fundamentally different principle. They are semiconductors that convert electrical energy directly into luminous output. The “cold” generation of light by LEDs leads to high efficacy because most of the energy radiates in the visible spectrum. The present commercial high-efficiency LED lamps provide efficacy of 60~100 Lumens/Watt, while the technology is still under development. In addition to high efficacy, LED devices are safe for the environment, and their compact size provides more flexibility for applications. Another great advantage of LEDs is the very long lifetime (more than 50,000 hours expected), which can largely reduce the cost for maintenance.

Drive electronics are necessary to utilize LEDs. As LEDs are normally low-voltage dc devices, high-voltage ac power from the grid has to be converted to be suitable for LEDs. Meanwhile, drive electronics also provide power regulation and protection to the LED devices. In addition to these basic functionalities, special designs of drive electronics are necessary to make full use of the advantages of LEDs.

Compared to other electric light sources, LEDs offer much more flexibility in lighting system design, majorly due to their small form factor. Since the light output of a single LED is limited, normally a number of LEDs are included in a system in order to generate sufficient luminance. These small LEDs may be distributed in almost any form, which may lead to improvement of overall systems. For instance, although some present LED products are designed with the shape of bulb or tube in order to fit the existing retrofits, which are shown in Fig. 1.2, strip or plate configurations are more suitable for LED applications. The resulted small thickness

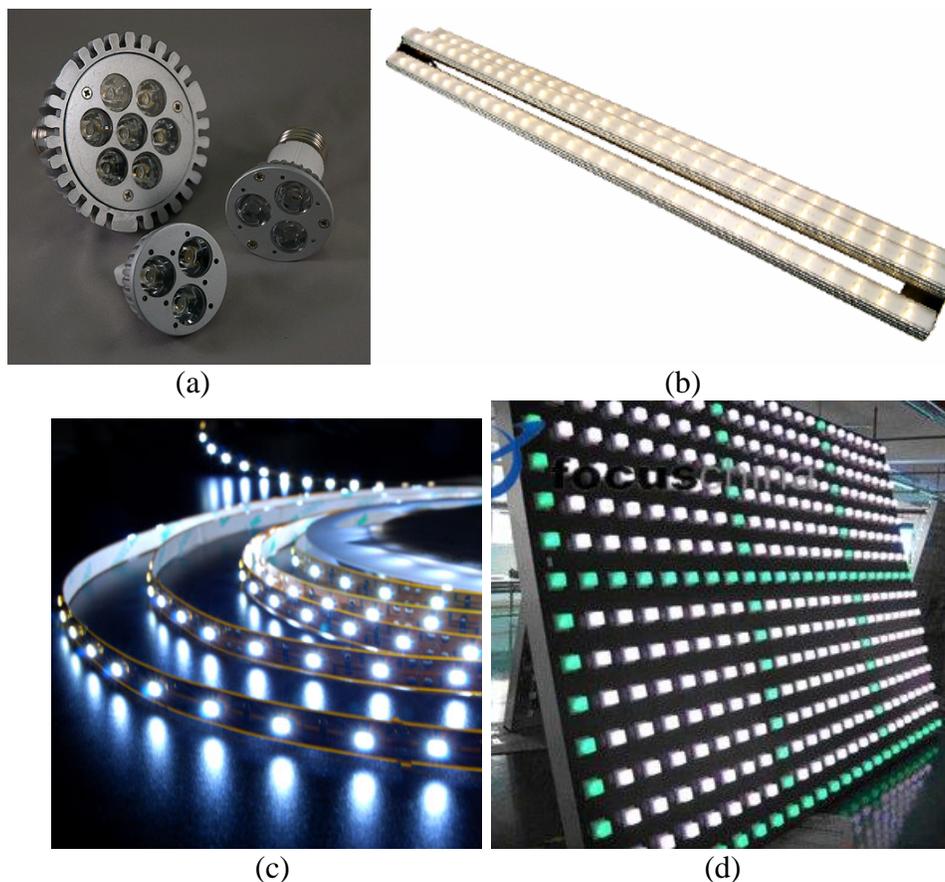


Figure 1.2: Typical configurations of LEDs: (a) incandescent lamp replacement, (b) fluorescent lamp replacement, (c) LED strip, and (d) LED plate.

offers more flexibility for usage, and can even be integrated to building fixtures. Meanwhile, the distributive configurations improve thermal dissipation, which is helpful to achieve high efficacy.

In order to take advantage of the small form factor of LED devices, the drive electronics should have small sizes or thickness as well. One approach is to reduce voltage stress on the devices in LED drivers. With lower rated voltage, the integration of semiconductor devices becomes much easier and lower in cost, and the drive circuits can operate at higher frequency and with low-profile components. All these benefits lead to high-level monolithic integration, which matches well with the small package of LED devices.

Another research focus is to make full use of the long lifetime of LED devices. Although LED devices can last a very long time, drive electronics often fail much earlier, primarily due to short-life electrolytic capacitors. For off-line applications, standards like ENERGY STAR program place requirements of high power factors [3], which lead to large double-line-frequency ripples on input power. In order to filter these power ripples, bulk electrolytic capacitors are normally utilized with the advantage of high power density at low cost. However, the lifetime of low-quality electrolytic capacitors is normally much shorter than LED lifetime, which can be even worse due to high operating temperature. The combination of low-quality capacitor, large power ripple and high temperature often leads to early failure of electrolytic capacitors, and thus the failure of LED lamps. As a result, energy storage approaches other than low-quality electrolytic capacitor should be developed in order to achieve long lifetime and competitive cost.

Cost reduction is another important target for LED system design. At present, one major obstacle for LED utilization is the high initial cost, which needs to be addressed to encourage the adoption of LED techniques. The projected cost for LED lighting is 2~3 dollars per kilo lumen (\$/klm) of light output by 2015, as planned by the Department of Energy [4]. With a share of about 20% of the total budget, the cost for drive electronics is expected to be approximately 0.1 dollar per Watt (\$/W) of power output, which places a significant challenge for driver design.

This thesis focuses on the techniques to improve the performance of LED drive electronics, including the lowering of voltage stress for high-level integration and the reduction of energy-storage capacitance to extend overall lifetime. A review of LED characteristics and existing drive electronics are provided in Chapter II, with the motivations for the research presented in this thesis. Chapter III introduces the series-input modular structure to reduce voltage stress on devices, and the common duty cycle approach to achieve automatic input

voltage distribution and output current copying. The techniques to reduce energy-storage capacitance are presented in Chapter IV, including the constant input current approach to achieve sufficient PF while reducing input power ripple, and a bidirectional second stage to reduce required capacitance with relatively small power loss. The approaches to combine series-input structure and reduction of energy-storage capacitance are presented in Chapter V. Chapter VI summarizes the contributions and concludes this thesis.

CHAPTER II

POWER ELECTRONICS IN LED LIGHTING

This chapter provides an overview of the concepts related to power electronics in LED lighting. The basic electric characteristics of light-emitting diodes (LEDs) are summarized in Section 2.1, followed by the introduction of switching power converters in Section 2.2. Section 2.3 summarizes some popular power electronics techniques applied in present LED lighting applications, with the emphasis on power factor correction (PFC). The motivations driving the research in this thesis are presented in Section 2.4, while Section 2.5 summarizes some related efforts reported recently.

2.1 LEDs

Light-emitting diodes (LEDs) are predicted to be the dominating electric light source in the future. Compared with other light sources, LEDs provide several advantages, which are still improving. One of the most important advantages is the high efficacy, which is very useful for energy savings. In addition, unlike fluorescent lamps or high intense discharge (HID) lamps, LEDs are environmentally safe. Another main advantage of LEDs is the very long lifetime. The commercial high-brightness white LEDs are expected to have a lifetime over 50,000 hours for the output to degrade to the 70% lumen maintenance level, which allows more than 10 years

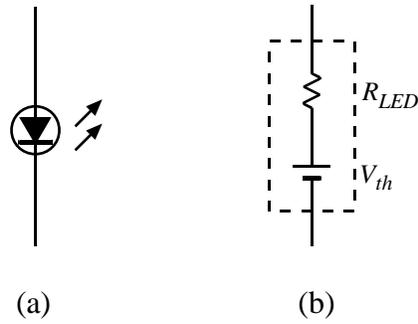


Figure 2.1: (a) Symbol and (b) electric model for an LED device.

operation, assuming 8 hours operation per day. Furthermore, LEDs provide flexibility for utilization compared with fluorescent and HID lamps, and their small form factor is very useful for applications with limited size.

Similar to ordinary diodes, LEDs are based on p-n junctions, which are built with “p” and “n” materials. When sufficient voltage is placed on a p-n junction, the holes in “p” material and the electrons in “n” material combine, releasing energy in the form of light. As the combination rate is proportional to current density, LEDs are considered “current-driven” devices, whose brightness depends largely on current. In order to operate an LED, a threshold voltage has to be reached. Around the nominal operation condition, the dynamic resistance of an LED is typically small. The common symbol and electric model for an LED are shown in Fig. 2.1, with the voltage source representing the threshold voltage V_{th} in series with the dynamic resistance R_{LED} of LED. As the variation on an LED current is much larger than that on voltage, drive circuits normally regulate LED current rather than voltage. When multiple LEDs are utilized, they are usually connected in a string so that their current can be regulated at the same time.

2.2 Switching converters

Switching converters have become the most popular drive electronics for LED applications, mainly due to their high power efficiency. With switching on and off of transistors and diodes, pulsated voltage and current signals are generated, and then filtered by inductors and capacitors to achieve specific outputs. As the transistors and diodes conduct with small voltage drops, the conduction loss in switching converters can be much smaller compared to linear regulators.

With different topologies, switching converters can provide various functionalities and features. For example, buck converters can generate low output voltage from high input voltage, while boost converters can only step up voltage. Buck-boost and Cuk converters, which are based on the cascaded connection of buck and boost converters, can theoretically provide any conversion ratio. When additional devices are added, such as transformers, many more types of converters are feasible for applications.

Take the non-inverting buck-boost converter as an example to demonstrate the operation of switching converters. The schematic of the converter is shown in Fig. 2.2, with two transistors S_h and S_l , and two diodes D_l and D_h . The converter is controlled by adjusting the conducting time of the high-side transistor S_h and low-side transistor S_l within one switching period, i.e., duty cycle D . When both S_h and S_l are conducting, input voltage source v_{in} charges inductor L . When S_h and S_l are off, the two diodes D_h and D_l conduct the inductor current, which charges the output capacitor. The total volt-seconds applied on the inductor over one switching period can be calculated as

$$\int_0^{T_s} v_L(t) dt = v_{in} D T_s + (-v_{out})(1-D) T_s, \quad (2.1)$$

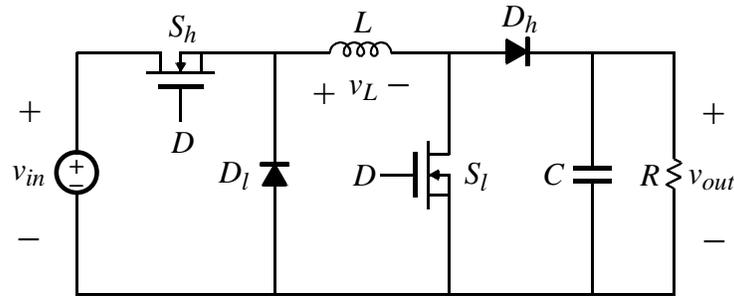


Figure 2.2: Non-inverting buck-boost converter.

where T_s is the switching period and D is the duty cycle. When the converter operates in a steady state, the total volt-seconds on the inductor over one switching period should be zero, yielding

$$v_{in}D - v_{out}(1-D) = 0, \quad (2.2)$$

or

$$v_{out} = \frac{D}{1-D} v_{in}. \quad (2.3)$$

The conversion ratio $M(D)$ is the ratio of output to input voltage of a converter. Eq. 2.3 demonstrates that the conversion ratio of non-inverting buck-boost converter is given by

$$M(D) = \frac{v_{out}}{v_{in}} = \frac{D}{1-D}. \quad (2.4)$$

Note that this conversion ratio depends on duty cycle only. Similarly, the conversion ratio for other converters can be derived with this approach [5]. The ratio of output to input current of a converter is just the inverse of voltage conversion ratio $M(D)$ when all power loss is neglected.

According to Eq. 2.4, the steady-state behavior of a converter is similar to a “dc” transformer, which converts a dc input voltage to a dc output voltage. The voltage conversion ratio of the transformer is $1:M(D)$, where $M(D)$ is the conversion ratio of the converter. The steady-state model of a switching converter is shown in Fig. 2.3.

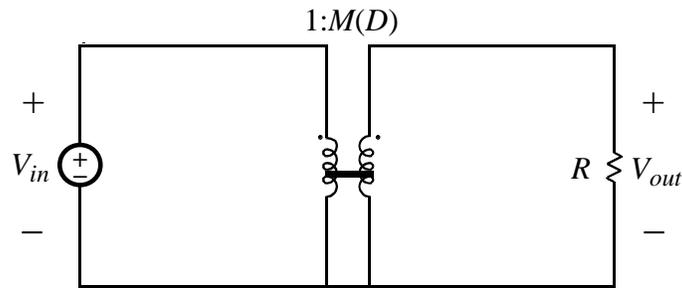


Figure 2.3: Steady-state model for a switching converter.

The above analysis is based on the assumption that the inductor current never reaches zero, i.e., continuous. In other words, either the two transistors or the two diodes are conducting throughout each switching period. If the inductor current reaches zero during the subinterval of diode conducting, the two diodes will go off, and the inductor is disconnected from both input and output ports with zero inductor current until the transistors are turned on again. Under this situation, the converter is said to enter the discontinuous conduction mode (DCM). In contrast to DCM is the continuous conduction mode (CCM), which means the inductor current is not pulsated. The inductor current waveforms in CCM and DCM are shown in Fig. 2.4. When one converter operates in DCM, the volt-second balance indicated by Eq. 2.2 is invalid. Thus the relation between output and input voltage, or conversion ratio of the converter does not only depend on duty cycle.

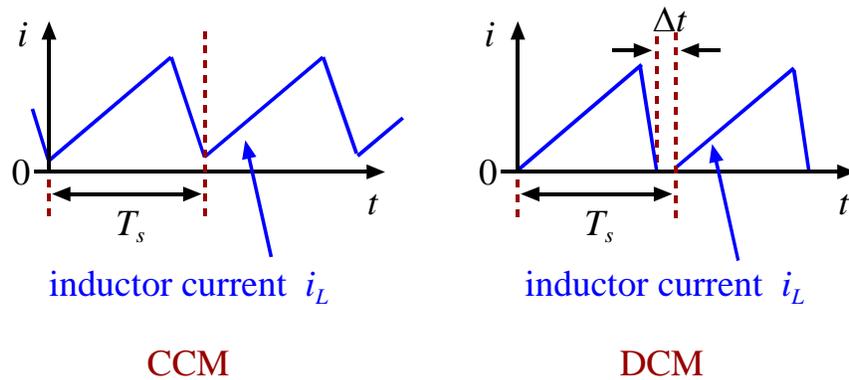


Figure 2.4: Inductor current waveforms of converters in CCM and DCM.

2.3 Power electronics in LED lighting

Power electronics are critical contributors to high-performance LED lighting applications. As the interface between power source and LED load, drive electronics should convert the input power, which is often ac and high-voltage, to dc and low-voltage for LEDs, while provide current regulation and other necessary protections at the same time. The typical structure for LED driver is shown in Fig. 2.5. For off-line applications, normally two stages are included in the circuit, with a power factor correction (PFC) stage followed by a dc-dc stage. The PFC stage is necessary as high power factors are required by standards like ENERGY STAR program, while the second stage provides regulation of LED current. The second stage may not be included in some applications where bulk capacitors are parallel with the LED load to limit LED current ripple. In applications where dc source is available, only the dc-dc stage is necessary to power LED load.

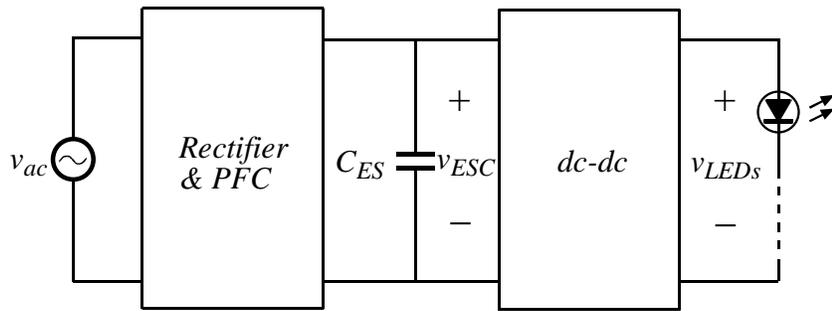


Figure 2.5: Typical structure for LED drivers. Rectifier and PFC stage are unnecessary when dc power source is available.

Power factor (PF) is a measurement indicating the quality of energy transmission on the grid. The higher PF achieved, the less power loss occurs on the grid. PF is defined as the ratio of the average input power delivered to an equipment divided by the magnitude of the complex power (or apparent power), as represented by Eq. 2.5. In general, PF improves when input current gets closer to the shape and phase of input voltage. For grid-powered applications, the maximum value of $PF = 1$ is achieved when input current is pure sinusoidal and in phase with line voltage.

$$\text{power factor} = \frac{\text{average power}}{(\text{rms voltage})(\text{rms current})} \quad (2.5)$$

For off-line LED lighting applications, high PF is required by standards. For instance, the PF for commercial solid-state lighting applications is required to be higher than 0.9 by the ENERGY STAR program, while the minimal PF requirement for residential products is 0.7 [3].

Many approaches are feasible to achieve high PF for off-line circuits. The basic idea is to shape input current so that it becomes sinusoidal and in phase with input voltage. One popular approach, which is called the average current control, utilizes a scaled input voltage waveform as the reference for average input current, as shown in Fig. 2.6. Two control loops are included in

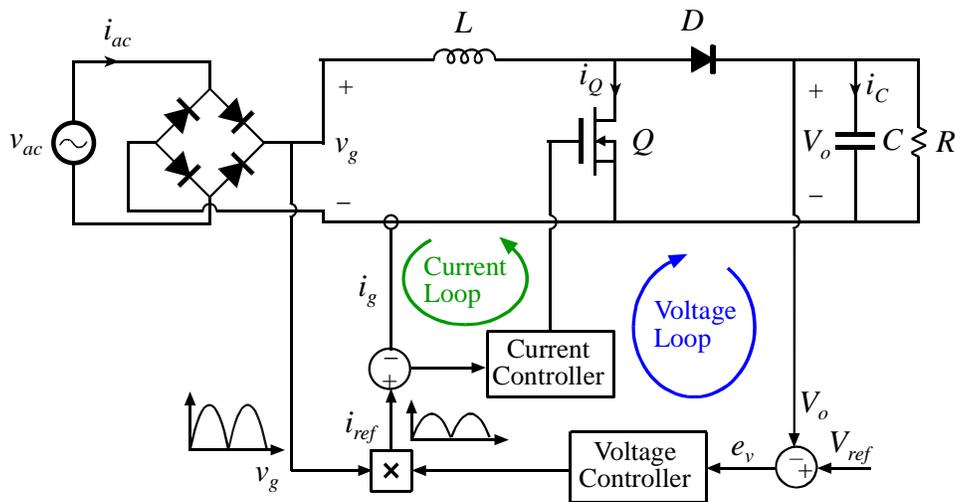


Figure 2.6: A PFC boost converter with average current control.

the circuit. A current control loop regulates the input current to a reference that is proportional to input voltage, while a voltage loop adjusts the scale between the input current reference and input voltage to stabilize the output voltage. If the voltage loop is slow enough, the current reference signal will be very close to sinusoidal and in phase with input voltage, and thus a good PF can be achieved.

Other control approaches are developed to achieve high PF without input voltage sensing [6-9]. For instance, the non-linear carrier control approach utilizes a special reference signal instead of scaled input voltage, i.e., non-linear carrier, as the reference for input current [8]. With a suitable carrier signal, a high PF can be achieved.

Some other approaches are feasible for specific topologies and conduction mode. For example, it is easy to achieve high PF with boost converters in critical conduction mode (CRM), which means the converter operates right at the boundary between CCM and DCM. With CRM, the low-side transistor of a boost converter is turned on right at zero crossing of inductor current, resulting in an input current waveform shown in Fig. 2.7. In this case, the average input current

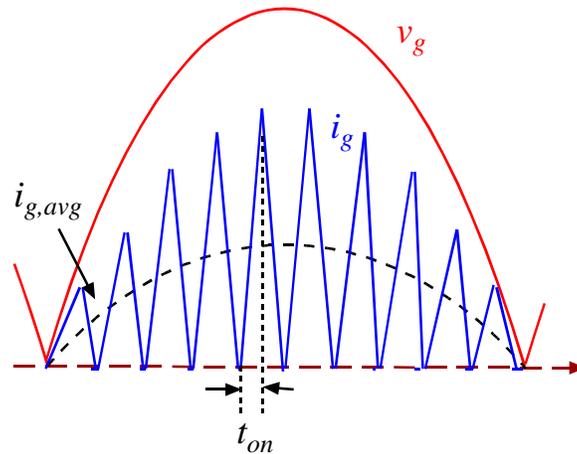


Figure 2.7: Input current waveform of a boost converter operating in CRM.

within each switching period is approximately half of peak inductor current, as indicated by Eq. 2.6. It can be seen that input current $i_{g,avg}$ is proportional to input voltage v_g under this condition. Thus, when the conduction time of low-side transistor t_{on} is constant within every half-line cycle, the input current waveform will be a scaled version of input voltage waveform, and a high PF can be achieved.

$$i_{g,avg} = \frac{1}{2} i_{L,peak} = \frac{1}{2} \frac{t_{on}}{L} v_g \quad (2.6)$$

With approaches mentioned above, a PF close to unity can be achieved. However, as the input voltage and input current are sinusoidal and in phase, the resulted input power contains a very large ripple, which can lead to large variations on LED current. As a result, significant filtering is required in order to limit the low-frequency LED current ripple. This is also one reason to include second stages in off-line LED drivers.

Regulation of LED current can be achieved with second stages in LED drivers. In off-line applications, buck converters are a common choice for the second stages, as normally the bus voltages are higher than LED string voltages. The major concern about the second stage is the

additional power loss. With the cascaded structure in Fig. 2.5, input energy has to be processed by both stages to reach the LED load. As a result, significant effort is required to achieve high power efficiency.

In order to avoid the cost and power loss associated with the second stage, the second stage is not included in some off-line applications. However, bulk capacitors have to be used to limit LED current ripple in these circuits.

2.4 Research Motivations

One major issue of many existing off-line LED drivers is the short lifetime, which is much less than the expected long lifetime of LED devices. As the drive circuits are often packaged together with the LED devices within lamps, failure of a drive circuit requires replacement of a whole lamp, which wastes the long lifetime of LEDs. Past studies show that the aluminum electrolytic capacitors in the drive circuits are the major reason for early failure. The wear-out of electrolytic capacitors is primarily due to evaporation and deterioration of electrolytes, which processes can be accelerated by elevated ambient or internal temperature. As an electrolytic capacitor degrades, its capacitance drops and its equivalent series resistance (ESR) increases, both of which cause increases in capacitor voltage ripple, which finally lead to the failure of the circuit [10].

In order to extend the lifetime of LED drivers, aluminum electrolytic capacitors have to be removed [11]. One option is to replace them with long-life capacitors, such as ceramic or film capacitors. However, these capacitors are much more expensive compared to electrolytic capacitors. Thus, in order to utilize ceramic or film capacitors while maintaining reasonable cost, the required energy-storage capacitance should be reduced.

Besides high efficacy and long lifetime, another advantage of LED devices is the miniature size, which offers flexibility for diverse and sophisticated design. For instance, LED applications with small size or thickness will be suitable for space-limited situations or integration with building fixtures. However, in high-voltage applications, the drive electronics normally operate at relatively low switching frequencies to limit power loss, which results in large components. Meanwhile, semiconductor devices with high rated voltage, which are required due to high voltage stress, are difficult to integrate. All of these disadvantages hinder the size shrinking of high-voltage LED applications.

A series-input structure provides a possible method to reduce the voltage stress on the devices in high-voltage applications. When several cells in a system are series-connected from the input port, the input voltage of the system is distributed among them. If the system is well designed and balanced, the input voltage of each cell is the input voltage divided by the number of cells. The more cells connected, the less voltage rating is required for each cell. The integration of the semiconductor devices becomes much easier with reduced rated voltage. Meanwhile, the circuits can operate at higher switching frequencies with low-profile inductors and capacitors. As a result, it is possible to achieve high-level integration with series-input structure [12].

2.5 Reported efforts to eliminate electrolytic capacitors in LED drivers

Recently, many approaches have been proposed to eliminate electrolytic capacitors in off-line LED applications. The purpose of electrolytic capacitors in off-line applications is for energy storage, so as to balance the energy between input power with large variations and the

constant output power. To reduce the capacitance so that long-life but expensive capacitors can be adopted, the first attempt is to reduce the required energy to be stored in each line cycle.

As the LED applications are allowed to have PF less than one, it is possible to reduce the input power ripple with the trade-off of a lower PF, which can be realized by manipulating the shape of input current. In [13, 14], specific harmonic signals are injected into the input current reference to reduce the peak-to-average ratio of input power. Similarly, distorted sinusoidal references are utilized for PFC converter in [15, 16] to reduce input power ripple.

Although the required energy storage can be reduced with input current shaping, very large energy-storage capacitance is still necessary if the capacitors are directly parallel with the LED strings, as proved in Appendix A. The required capacitance can be further reduced by decoupling the capacitors from the LEDs. With additional stages placed following energy-storage capacitors and followed by LED load, high dc value and/or large ripple on capacitor voltage are adopted to reduce capacitance in [17, 18]. Although the electrolytic capacitors can be eliminated from these circuits, the drawback is low efficiency as the entire energy is processed by two stages to reach the LEDs. Some integrated LED drivers are also reported in [19-21], in which a single controller is utilized for both stages. However, the issues of energy storage and power loss are not tackled by integration. The active filter technique is also adopted to reduce energy-storage capacitance in [22], where a three-port converter with a dedicated power ripple port is proposed.

Magnetic energy storage is also proposed as a replacement of capacitance in [23, 24]. However, although magnetic components provide much longer lifetime compared with electrolytic capacitors, the required large inductance becomes a significant issue, when considering size and cost.

CHAPTER III

DC LED DRIVER BASED ON SERIES-INPUT MODULAR STRUCTURE

Although some trends in commercial high-brightness LEDs are towards high-power, high-current devices, most applications still require a large number of LEDs to be used in a single system [25-29]. Typical solutions, especially when operating from a high voltage supply or the ac grid, place many LEDs serially in a string and regulate the string current [30]. Such solutions require use of high-voltage components operating at a relatively low switching frequency from tens of kilohertz to low hundreds of kilohertz in order to limit switching loss. Both high voltage and low frequency result in bulky inductors designed for large volt-seconds. The integration of components, such as power transistors and gate driver circuits, also becomes difficult and expensive due to high rated voltage. At the same time, these solutions also risk losing an entire string of LEDs with the failure of a single element.

As an alternative, a series-input modular structure, as shown in Fig. 3.1, enables use of low-voltage integrated circuits (ICs) and components over a scalable range of high dc input voltage buses [12]. The low-voltage cells can operate efficiently at high switching frequencies in the megahertz range using low-profile, light-weight components that match well to the miniature packages typical of LEDs. It also becomes more feasible to achieve a high level of monolithic integration. Furthermore, this structure provides a possible method to respond to individual LED failure by automatically detecting and shorting the affected cell from the series system. The dc

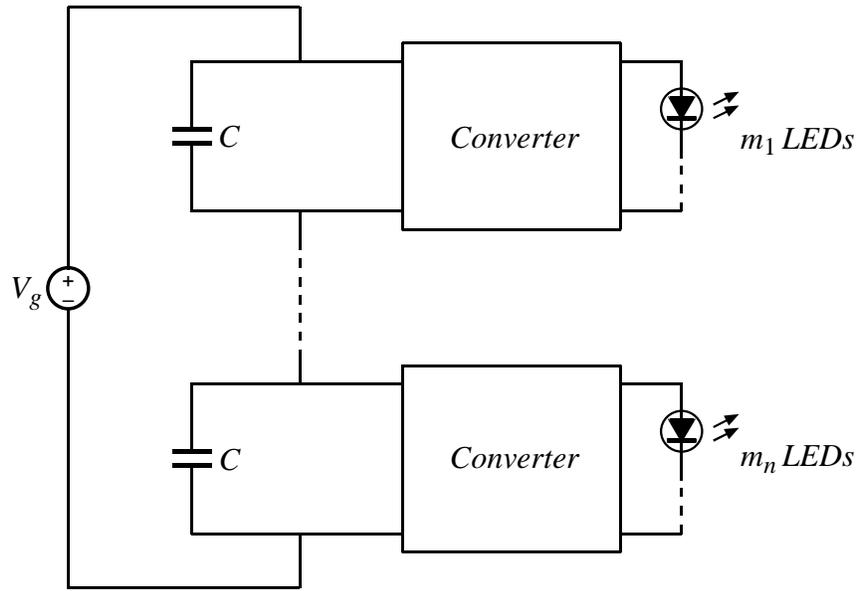


Figure 3.1: An LED application based on series-input converter modules.

input line voltage bus may be the output of a power factor correction (PFC) stage in an off-line ac application or a direct connection in a dc system (e.g. stand-alone solar, aircraft, naval ships or potential future dc wiring in buildings).

One critical issue for the modular structure is distribution of line voltage, which has been investigated for series-input parallel-output converters in [31-40]. However, most approaches require an additional control loop for the line voltage sharing, which complicates system design. The common duty cycle approach, introduced in [36] and inherited in [37-40], achieved good line voltage distribution.

The modular LED driver structure with converters operating in discontinuous conduction mode (DCM) was reported in [12]. The presented approach uses two control loops in each module and relies on communications between the cells to tune the control loops based on relative cell power levels and also achieves proper input voltage sharing.

This chapter introduces a series-input modular structure implemented by converter cells operating in continuous conduction mode (CCM), with common duty cycle control approach to automatically distribute line voltage between the cells. More efficient operation can be achieved with lower peak currents by operating in CCM as opposed to DCM. In addition, only one local feedback loop is necessary in the entire system using the proposed method to achieve well-regulated output LED currents. The control-to-output transfer function of the proposed system is close to that of a single converter and thus easy for system design and compensation. Two drawbacks to the proposed system include an increase in the number of components that scales with the number of modules and the requirement for communications between the series modules. These effects are partially mitigated by reduced voltage ratings that scale down with the number of modules and low isolation requirements, since communications occur only between neighboring modules.

The chapter is organized in the following way. Section 3.1 introduces the series-input system and the reported design solution in DCM. Analyses of the common duty cycle approach are provided in Section 3.2, including the steady-state behavior, small-signal transfer function for the system and compensator design. Some special considerations for system design, including responses to LED open-circuit failure and start-up issues, are presented in Section 3.3. Experimental results for a 25-W 3-cell system with 9 Luxeon K2 high-brightness LEDs are given in Section 3.4, demonstrating line voltage sharing, output current copying and LED failure response. A block diagram of integrated buck modules for series-input system, including schematic for communication blocks, is proposed in Section 3.5, while Section 3.6 concludes this chapter.

3.1 Series-input modular structure

The proposed system is composed of several converter cells, which are serially connected from input ports and have independent output ports, as shown in Fig. 3.1. Each cell drives a sub-string of LEDs, whose numbers can be different between strings. The target behaviors of this system include input voltage distribution and LED current regulation of all the cells. When the system is well balanced with proper design, the high input voltage evenly distributes between the cells. Consequently, the voltage rating of each module can be significantly smaller than the high input voltage of the system. The low-voltage modules can operate at high switching frequencies with low-profile, low-weight components, making it more feasible for monolithic integration.

In order to achieve the desired system behavior, a special control approach has to be applied on the series-input modular system. One solution reported in [12] adopts buck-boost converters in DCM for the converter modules, as shown in Fig 3.2. The input impedance of a buck-boost converter operating in DCM can be emulated as a resistor whose resistance is controllable with the converter duty cycle. Thus, the system input voltage is distributed among the modules according to the ratio of input impedances, which can be adjusted by varying the duty cycle of the converters. In order to implement this control approach, communication between the modules is necessary to share information of power consumption. As the modules take turns to communicate and calculate the duty cycle, the response of this system is limited by the speeds of communication and calculation.

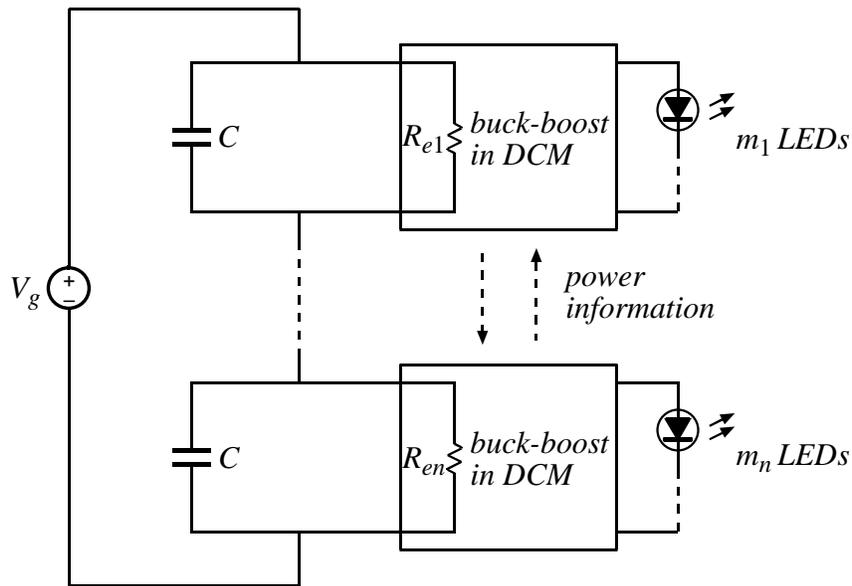


Figure 3.2: An LED driver based on series-input buck-boost modules in DCM.

3.2 Common duty cycle approach

In order to reduce the complexity in control and to improve performance, a common duty cycle approach can be applied to series-input modular systems. Different from the approach in [12], the converters should operate in CCM in order to apply the common duty cycle approach. A proposed system is composed with the converters with the same topology, while one of the cells is the master and the others are slaves. The master cell regulates its own output current and generates a duty cycle, which is adopted by all the slave cells to drive their transistors. Many options are feasible for realizing distribution of the common duty cycle in the series structure, including isolated analog and digital communications and direct gate drive transformer coupling. One solution using digital communications between neighboring cells with very low isolation requirements is presented in Section IV of [12].

3.2.1 Steady state of series-input modular system with common duty cycle

A steady-state equivalent model for the proposed system is shown in Fig. 3.3. The output LED current for each converter cell, I_{o_i} , can be calculated with

$$I_{o_i} = \frac{I_g}{M(D_i)}, \quad i = 1, 2, \dots, n, \quad (3.1)$$

where I_g is the system input current, D_i is the duty cycle of cell i and $M(D_i)$ is the conversion ratio of the cell.

When the system is operating in steady state, the input currents for all converters are the same and equal to I_g . The output LED currents are identical only if the conversion ratios $M(D_i)$ of all the cells are identical, which can be achieved approximately when all the converters share the same topology, operate in CCM and are driven by identical duty cycle. Under this condition, the conversion ratios for all cells are equivalent and given by

$$M(D) = \frac{\sum_{i=1}^n V_{o_i}}{V_g}, \quad (3.2)$$

where D is the common duty cycle of all cells. In steady state V_{o_i} , the output voltage of cell i , is approximately $m_i \cdot V_{LED}$, where V_{LED} is the rated voltage of one LED and m_i is the number of LEDs in the cell i .

Under the common duty cycle condition in Eq. 3.2, the input voltage V_g automatically distributes among the cells. The ratio between input voltages of the converters can be solved from Fig. 3.3 as

$$\frac{V_{in_i}}{V_{in_j}} = \frac{V_{o_i}}{V_{o_j}}. \quad (3.3)$$

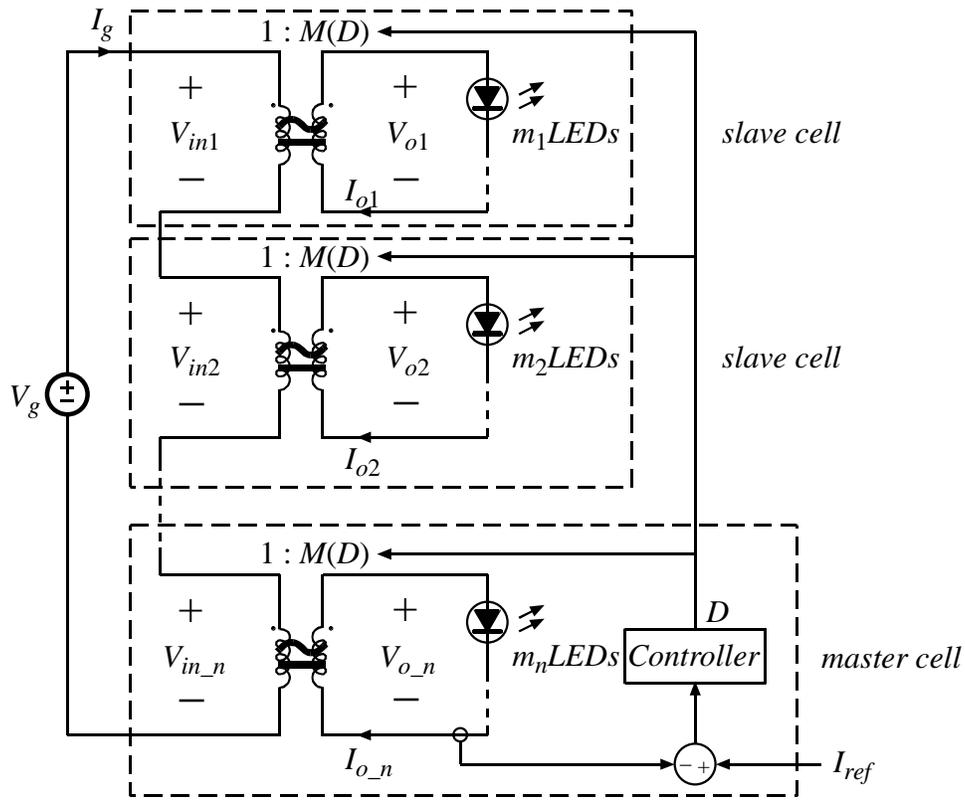


Figure 3.3: Steady-state model of an LED driver based on series-input modules with common duty cycle.

Based on Eq. 3.1 and 3.3, with $D_i = D$ given by Eq. 3.2, all output currents are identical and the input voltage V_g naturally distributes according to the ratio of the output voltages. As a result, regulation of only the LED current of the single master cell results in good matching of all LED currents for an arbitrary number of cells and an arbitrary number of LEDs per cell. The resulting LED current regulation in all cells is also independent of characteristic differences among the LEDs and forward voltage variations during the LED lifetime. Hence, the system has only one master cell at any time, while communication is necessary to transmit the duty cycle to the slave cells. In practical applications, all the cells may be identical and have the ability for

output current regulation while only the master cell is authorized for control. The authority for control may be transferred from one cell to another for averaging of any regulation errors or only transferred in the event of a failure. Furthermore, the slave cells may be allowed to modify or offset the cell duty cycle incrementally to improve accuracy of the output current or to allow LEDs with different current specifications on each cell. Communications can be performed without significant isolation requirements by transferring the duty cycle command between neighboring series cells, similar to the method used in [12]. The extensions mentioned above for transferring control authority among cells or modifying output currents of each cell may be developed in further research.

3.2.2 Small-signal model of series-input system with common duty cycle

One benefit of the common duty cycle approach is that only one single control loop is required. The behavior of this loop is primarily based only on the dynamics of the master cell and is relatively independent of the slave cells. The small-signal model of the series-input system is shown in Fig. 3.4(a), where canonical model for converters is used [5]. The canonical model parameters for basic converters are shown in Table 3.1.

The input capacitor C_{in} places significant impact on the control-to-output-current transfer

TABLE 3.1 CANONICAL MODEL PARAMETERS FOR IDEAL BUCK, BOOST AND BUCK-BOOST CONVERTERS

Converter	$M(D)$	L_e	$e(s)$	$j(s)$
Buck	D	L	$\frac{V}{D^2}$	$\frac{V}{R}$
Boost	$\frac{1}{D'}$	$\frac{L}{D'^2}$	$V\left(1 - \frac{sL}{D'^2 R}\right)$	$\frac{V}{D'^2 R}$
Non-inverting buck-boost	$\frac{D}{D'}$	$\frac{L}{D'^2}$	$\frac{V}{D^2}\left(1 - \frac{sDL}{D'^2 R}\right)$	$\frac{V}{D'^2 R}$

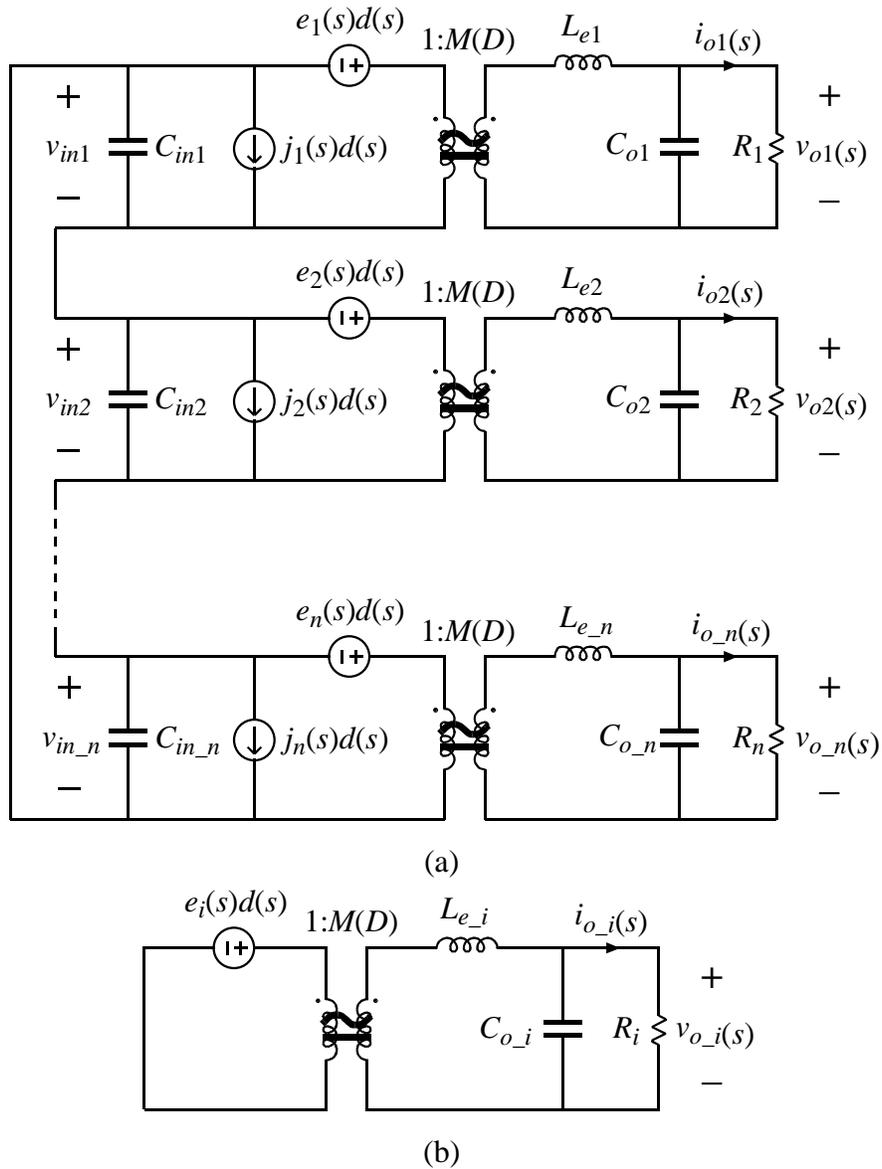


Figure 3.4: Small-signal model for (a) a series-input modular system, and (b) a single converter, both in CCM. The parameters of the model for typical converters are shown in Table 3.1.

function of series-input modular system. As frequency goes high, the impedance of C_{in} gradually decreases and the input port becomes short-circuited. If C_{in} is sufficiently large, the small-signal model for the system can be reduced to that in Fig. 3.4(b), where the component values are identical to those of the master cell. Thus, the high-frequency small-signal model of a series-

input-connected system is close to the model of the master cell. With large enough input capacitors, mismatches in component values and loads between the cells have a small effect on the transfer function, including some variation in the dc gain. However, the effective dominant poles induced by output capacitor C_o and equivalent inductor L_e and the cross-over frequency of the transfer function of master cell are not affected. As a result, it is simple to design the compensator for a series-input system with large C_{in} according to the single converter model.

A comparison is given in Fig. 3.5 of the simulated control-to-output transfer function for a master cell in a four-cell buck-boost system with large input capacitors against that of a single-cell model. For the four-cell system, the master cell has 20 V input voltage, driving 6 LEDs, and the values of its input capacitor, inductor and output capacitor are 20 μF , 10 μH and 1 μF , respectively. The slave cells have 50% less load and a variation of $\pm 20\%$ in component values compared to the master cell. The single converter, selected for comparison, has the same value of load and components as the master cell in the four-cell system. In the Bode plots in Fig. 3.5, G_{system} and P_{system} are the magnitude and phase of the control-to-output transfer function for the master converter of the system while G_{single} and P_{single} are the amplitude and phase of the control-to-output transfer function for the single buck-boost converter. There is a slight difference between the transfer function of the master cell and that of a single converter, but the divergence is insignificant for control loop design.

When small input capacitors are used, they do not behave short-circuited until a very high frequency. Thus, the small-signal model of the system can no longer be estimated as a single converter model, and the dynamics associated with interactions between the master and slave cells become more pronounced. One extreme condition is zero input capacitance, or when input capacitor becomes open-circuited at very low frequency. The small-signal model for the series-

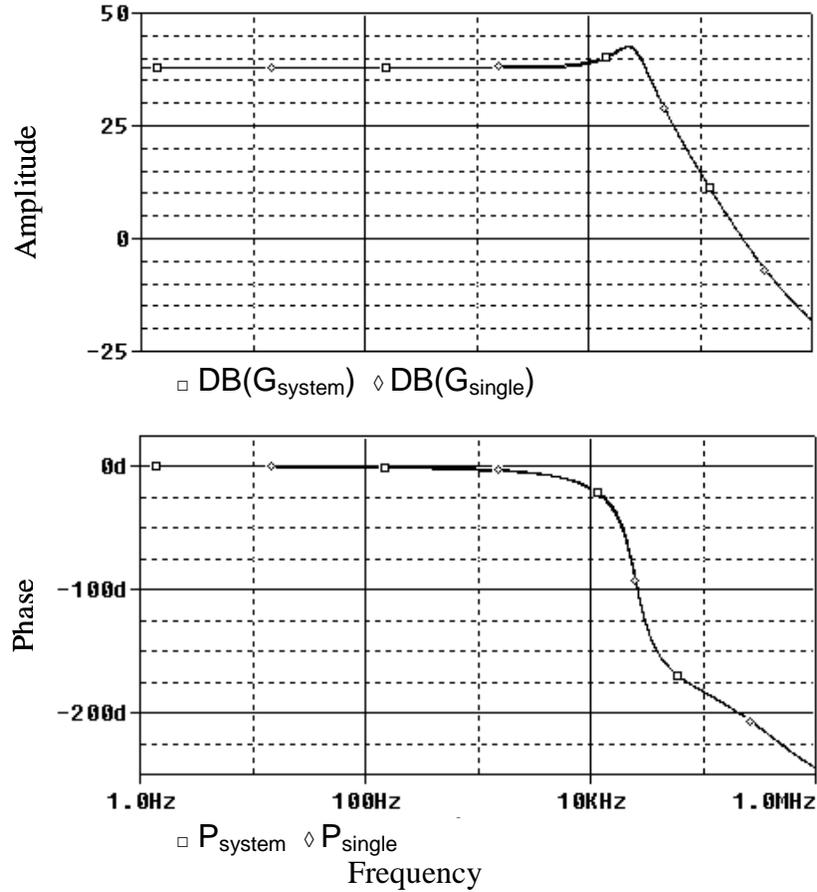


Figure 3.5: Simulated control-to-output current transfer functions for a series-input system with large input capacitor and for a single converter.

input system in this case is shown in Fig. 3.6. The control-to-output-current transfer function for cell j can be derived as

$$\frac{i_{o_j}(s)}{d(s)} = \frac{\sum_{i=1}^n e_i(s)}{\frac{1}{M(D)^2} \sum_{i=1}^n \left(sL_{e_i} + R_i \parallel \frac{1}{sC_{o_i}} \right) R_n + \frac{1}{sC_{o_j}}} \cdot \frac{1}{sC_{o_j}}. \quad (3.4)$$

For comparison, the control-to-output current transfer function for a single converter is

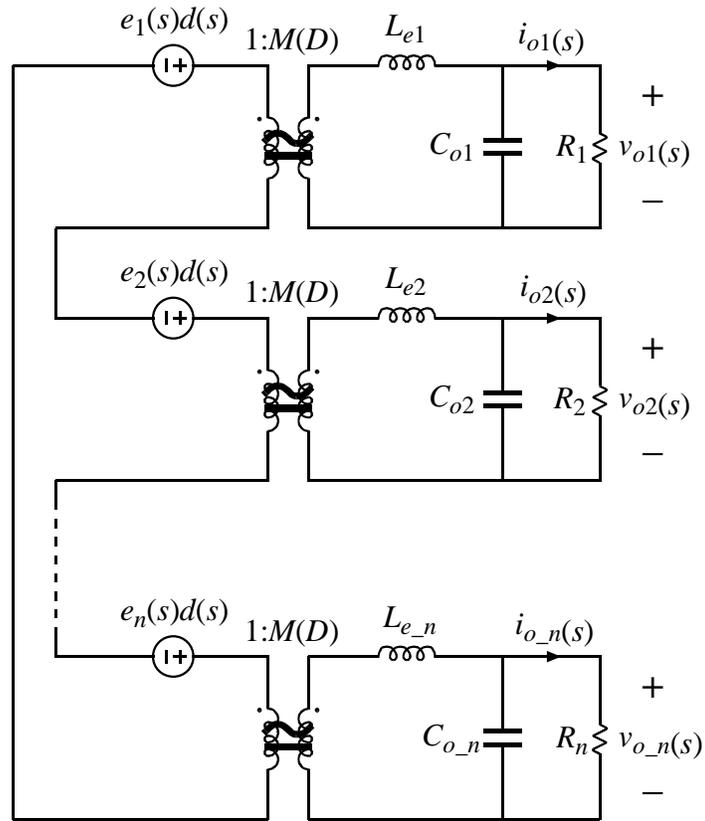


Figure 3.6: Small-signal model of a series-input system without input capacitor.

$$\frac{i_o(s)}{d(s)} = \frac{e(s)}{M(D)^2 \left(sL_e + R \parallel \frac{1}{sC_o} \right)} \frac{1}{R + \frac{1}{sC_o}}. \quad (3.5)$$

The transfer functions shown in Eq. 3.4 and 3.5 are very similar, except that the former is determined by the “average” of the component parameters. Thus the control-to-output current transfer function of a series-input system without input capacitors is close to that of a single converter, while the transfer function is determined by the average component parameters of the whole system rather than by only the parameters of the master cell.

In order to verify the impact of input capacitors on system transfer function, SPICE simulations are performed for a four-cell system with different input capacitor values, 0, 0.2 μF and 20 μF . Variations on component values are included in the simulation, while the parameters are intentionally selected to make the transfer function with average component parameters have split poles (low Q), while the transfer function with master parameters has complex poles (high Q). The final parameters for simulation are shown in Table 3.2. The simulated Bode plots for control-to-output transfer functions are shown in Fig. 3.7. The transfer function for a zero input capacitor gives a well-damped response. The transfer function for 20 μF input capacitor gives the resonant behavior of two complex poles. The transfer function for 0.2 μF input capacitor shows a higher order pole/zero pair resonance, but it is close to the small input capacitor case at low frequency and close to the large input capacitor case at high frequency. For all three cases, a slow PI compensator is suitable for stable operation function of the master cell.

3.2.3 Mismatch of component values between series-input modules

Mismatches in component values, discrepancies in actual duty cycles and communication delays may have an effect on the cross regulation of cell output currents. However, the accuracy of output current copying from master to slave cells is expected to be quite high for realistic tolerances and delays. As long as all cells operate in CCM, differences in filter component values between cells only affect the current ripple but do not affect the average output current. Thus, filter component values do not affect matching of LED currents among the cells. Differences in actual duty cycle due to mismatch in drivers may cause the output current of slave cells to deviate from that of the master. The output current divergence of slave cells from that of the master cell may be calculated by

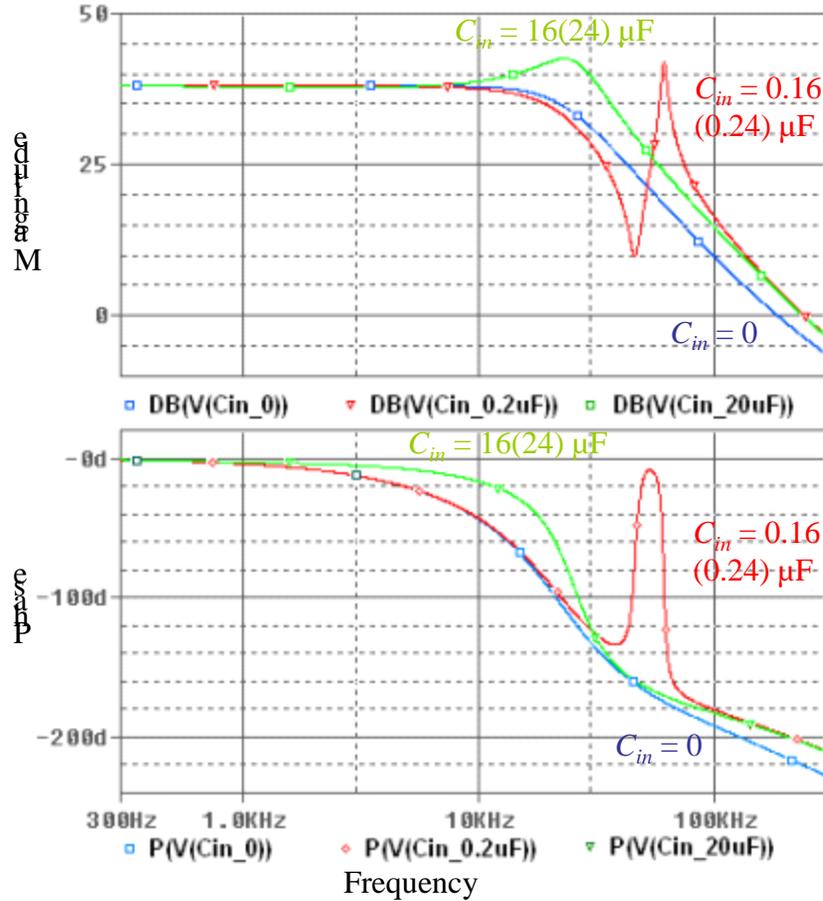


Figure 3.7: Simulated control-to-output current transfer function for series-input system with different input capacitor values. The detail component values are shown in Table 3.2.

TABLE 3.2 COMPONENT PARAMETERS USED IN SPICE SIMULATION

	D	I_{LED} (A)	V_{in} (V)	V_o (V)	R_{LEDs} (Ω)	L (μH)	C_o (μF)	C_{in} (μF)		
Slave \times 3	0.5	0.7	10	10	5	12	0.8	0	0.16	16
Master	0.5	0.7	20	20	10	8	1.2	0	0.24	24

$$\Delta = \left| \frac{\frac{1-D-d}{D+d} - \frac{1-D}{D}}{\frac{1-D}{D}} \right| \times 100\% , \quad (3.6)$$

where D is the duty cycle of the master cell and d is the difference between the duty cycle of the slave cell and the master cell. Table 3.3 shows the worst-case deviation of the output LED current

TABLE 3.3 WORST-CASE VARIATIONS OF LED CURRENTS DUE TO MISMATCH OF DUTY CYCLES

Difference in Duty Cycle	Worst Difference in Output Current
1 %	5 %
0.4 %	2 %
0.1 %	0.5 %

in a slave cell, valid when the master cell duty cycle is $0.25 < D < 0.75$. Although both analog and digital solutions for transmitting the duty cycle command should result in acceptable variations, an advantage of the digital solution is the ability to achieve less-than-0.1% matching in duty cycle despite analog variations in the circuitry used in the data transmission. The difference of gate drivers and gate-to-source capacitors of power transistors between cells may also lead to discrepancies in the effective duty cycle driving the cells, resulting in mismatches of output currents, according to Table 3.3. The delay for duty cycle communication may lead to some variation during transitions in the duty cycle command. The accumulated delay may reduce the phase margin of the loop gain, but should not present a problem if the number of cells is limited or the cross-over frequency for the closed-loop gain is sufficiently low.

3.3 Additional considerations for series-input system design

3.3.1 Start-up of series-input System

Start-up can be a significant issue for the series-input-connected modular structure. When the system is powered up, the input voltage of some cell may grow to a high value and cause damage. Another possible problem is that one cell may start operation earlier than others and immediately pull a high input current. The input voltage of this cell decreases to a low value and turns it off before other cells start to work. This process can take turns happening in the cells. If

the operations of cells do not coincide, the system cannot enter steady state. It is necessary to limit the input voltages of all cells to be within a safe range and also to distribute the line voltage so that all the cells can start operation before the master cell is selected. To meet these requirements, a default start-up duty cycle of $D = 0.2$ is introduced, which is used by all the cells immediately after they are powered up. The low duty cycle keeps all the converters in DCM and maintains both the input current and voltage at acceptable values to guarantee a successful start-up.

3.3.2 Response to LED open-circuit failure

One benefit of the series-input-connected modular structure is the possibility to respond locally to LED failures. This advantage reduces the effect of a single LED failure on the total system light output. If a single LED fails and becomes short-circuited, the cells will continue to operate and input voltage sharing is inherently adjusted according to Eq. 3.1 and 3.3. If a single LED fails open-circuited, the corresponding cell with the LED failure, or “failed cell,” can respond by applying a short circuit to its input port. The remaining cells continue to operate and share the input voltage. In order to utilize this benefit, the system has to be designed with some margin on rated voltage. If the system is required to keep operating when more cells fail, either the number of cells or the rated voltage of each cell has to increase. Circuitry is also required for each cell to measure its output voltage or output current in order to detect the open-LED failure. This circuitry can be coarse in quantization and only has to detect thresholds that indicate a failure.

In order to hold the input port short-circuit and to keep the communications channel open between other cells, a small amount of power must be maintained for the controller of the failed cell. This is achieved by using the output port as the power supply for the controller under the

failure condition. The failed cell operates in a pulse mode by periodically injecting a single pulse in the cell to charge the output capacitor and maintain sufficient voltage at the output port. Resonance at the input port is used in the pulse mode to achieve zero-voltage switching when shorting the input port and thus avoid high currents in the power switches.

The algorithm to respond to LED open-circuit failure is described below. The corresponding switch behavior of a non-inverting buck-boost converter is shown in Fig. 3.8. When LED failure is detected, the corresponding cell holds the power switches S_1 and S_3 on to transfer energy from the input capacitor to the inductor, as shown in Fig. 3.8(a). When zero input voltage is reached, the cell shorts its input port and begins to charge its output capacitor with the inductor current until the inductor current goes to zero, as shown in Fig. 3.8(b). To prevent over-current in the inductor and excessive output capacitor voltage, this process may be finished in several intervals. When the inductor current reaches zero, the output port is disconnected from the inductor while the input port is kept shorted as shown in Fig. 3.8(c). If switch S_4 is realized as a diode, then transition from Fig. 3.8(b) to 3.8(c) is automatic. The failed cell continues to short its input port and power its controller from the output capacitor until the output voltage drops to a low threshold voltage. Then the input port is opened as in Fig. 3.8(a) again and the input capacitor and inductor begin a resonant cycle, and the sequence of Fig. 3.8 is repeated.

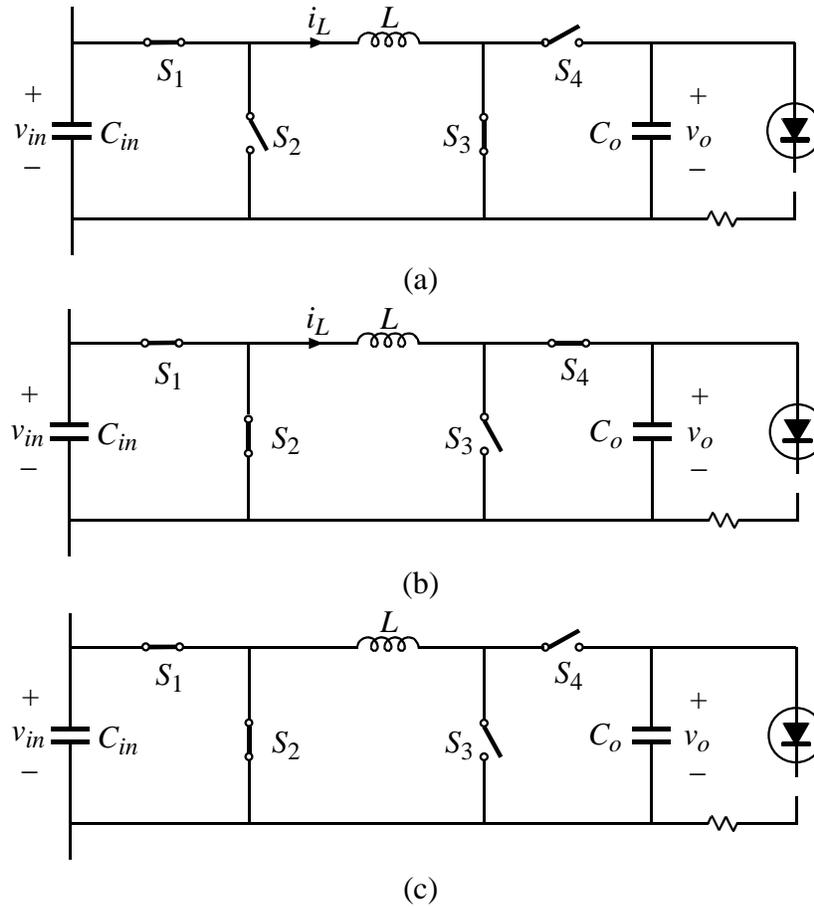


Figure 3.8: Switch behavior during LED failure response procedure: (a) S_1, S_3 on, charging L , (b) S_1, S_2, S_4 on, input port shorted, i_L charging C_o , (c) S_1, S_2 on, input port shorted.

3.4 Experimental results

A prototype has been developed to verify performance of the proposed modular architecture and control approach experimentally. The circuit has separable converters and load stages to employ modularity of the architecture. Each cell is controlled via an on-board floating FPGA and corresponding sensing circuitry and ADCs. Communication of the digital duty cycle command is implemented through the FPGAs and isolator chips. A four-switch buck-boost topology, as shown in Fig. 3.9, is implemented for the experiments described below. The devices

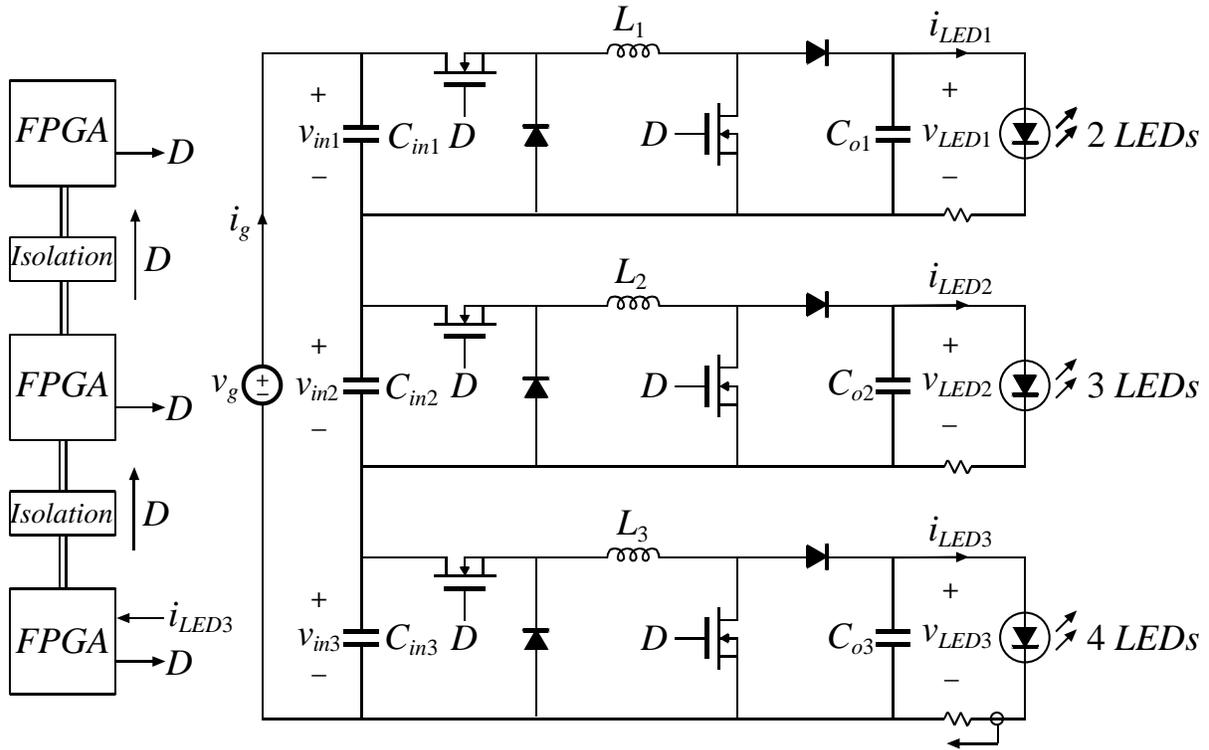


Figure 3.9: Experiment setup, including 3 buck-boost converters with 2, 3, and 4 LEDs as load, respectively. FPGAs are used for control and communication. $C_{in} = 0.4 \mu\text{F}$, $L = 10 \mu\text{H}$, $C_o = 1 \mu\text{F}$, $f_s = 800 \text{ kHz}$.

used are shown in Table 3.4. The values of input capacitor, inductor and output capacitor are $0.4 \mu\text{F}$, $10 \mu\text{H}$ and $1 \mu\text{F}$, respectively. The switching frequency is about 800 kHz . Three cells were used in experiment, with two, three and four LEDs as load, respectively, to verify operation with unbalanced loads. FPGAs are utilized only for experimental verification of the principle. The simple control algorithm can be realized with a small number of logic gates in a customer IC. Four-switch buck-boost converters are used for convenience in experimental development to operate under various conditions including buck, boost or buck-boost modes with a wide range of input voltages, number of cells and LEDs per sub-string. In practice, only a single topology is

TABLE 3.4 DEVICES USED IN EXPERIMENT PROTOTYPE

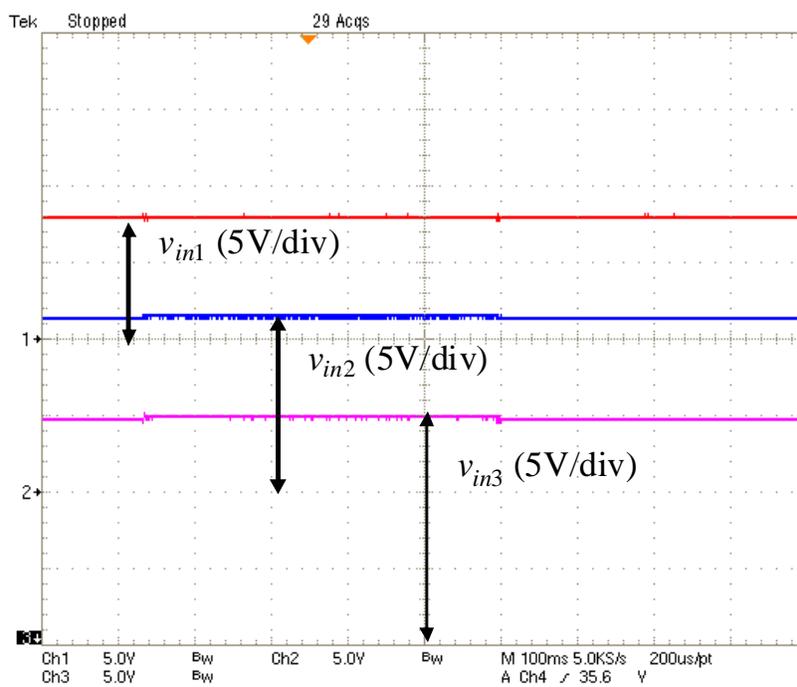
Device	Part Number	Description
FPGA	XC3S500E	Xilinx Spartan 3E
Diode	PDS540	Schottky, 40 V, 5 A
MOSFET	STN3NF06L	N_channel, 60 V, 4 A
ADC	AD7825	8 bit 4 channel Multiplexed
HB Driver	LM5101	Half Bridge Driver
Isolator	ISO7221	Dual Digital Isolator 2MSPS
LED	Luxeon K2	700 mA

required based on the specific system requirements and operating conditions, resulting in fewer switches and lower cost.

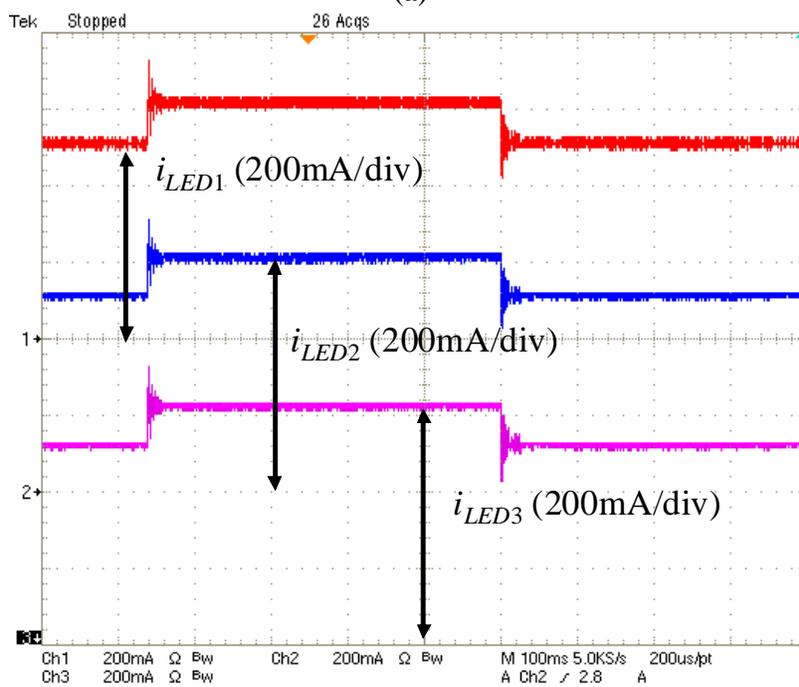
During experimental verification, float voltage supplies are generated with additional converters with isolation for FPGAs and control circuitries. When series-input modules are implemented in custom ICs, the supply voltages can be generated within each module.

A. Reference transient response test

During the test, the target output LED current for the master cell is set to switch from 500 mA to 600 mA and then back to 500 mA. Fig. 3.10 shows the waveforms of input voltages and output currents for the three cells. The three output currents track the reference current change with good cross-regulation as expected. The ratio between the three input voltages is about 2:3:4, which is proportional to the output voltages that are set by the different number of LEDs in each cell. The input voltages do not change significantly during the transition. Thus, the same ratio is maintained.



(a)



(b)

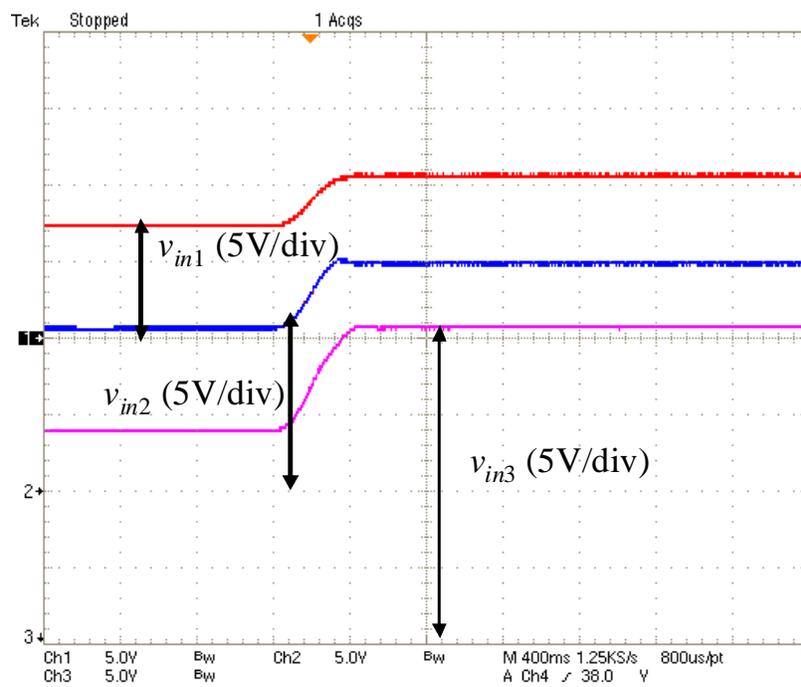
Figure 3.10: Waveforms of (a) input voltages and (b) output LED currents for the three cells during LED current reference transient test. The reference current for the master cell changes from 500 mA to 600 mA, and then back to 500 mA.

B. Line transient response test

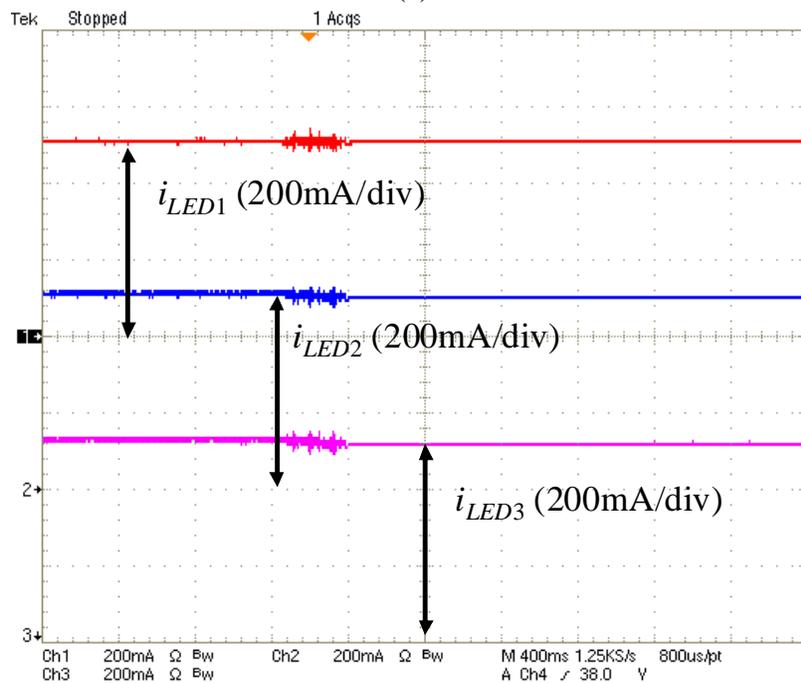
During the test, the line voltage increases from 35 V to 45 V. The input voltages and output currents of the three cells are shown in Fig. 3.11. The ratio of the three input voltages is about 2:3:4 before the transition occurs. When the line supply voltage increases, the three input voltages rise proportionally, and settle at about the same ratio. A small disturbance is seen in the LED currents during the transition, but the currents are regulated to the same value before and after the transition.

C. System start-up test

In order to limit the input voltages of all cells to be within a safe range and also distribute the line voltage at start-up so that all the cells can start operation before the master cell is selected, a default duty cycle of $D = 0.2$ is introduced, which is used by all the cells immediately after they are powered up. Fig. 3.12 shows experimental input voltage waveforms for the three cells during start-up. The line voltage is roughly distributed among the cells almost immediately after the power up. The ratio of the input voltages does not correspond to the load ratio for a short period because the cells are operating in DCM. The line voltage is redistributed when the master cell is selected and begins to control the system. Then the ratio of input voltages becomes the same as that of the loads during normal operation.



(a)



(b)

Figure 3.11: Waveforms of (a) input voltages and (b) output LED currents for the three cells during line transient test. Line voltage increases from 35 V to 45 V.

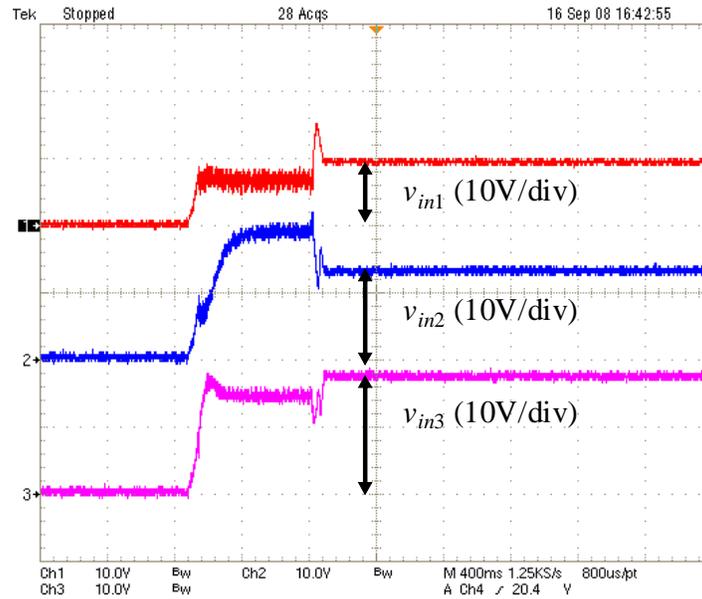


Figure 3.12: Input voltage waveforms of the three cells during system start up.

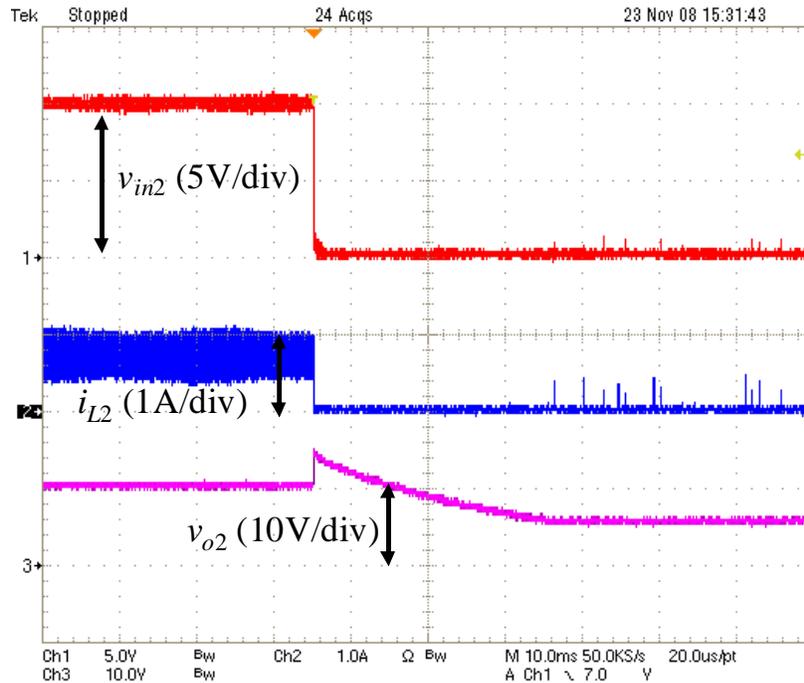
D. LED failure response test

An emulated LED failure response test was performed experimentally by abruptly disconnecting the LED board from cell 2 during operation. Fig. 3.13 shows the behavior of the failed cell, including the waveforms of its input voltage v_{in2} , inductor current i_{L2} and output voltage v_{o2} . The detail waveforms of v_{in2} , i_{L2} and v_{o2} at the instant of LED failure are shown in Fig. 3.13(b), which is a zoom-in on Fig. 3.13(a). When the LED failure is detected, i_{L2} continues integrating, while v_{in2} decreases rapidly. The input port is shorted when v_{in2} reaches zero, at which point the charging of output capacitor begins. The inductor current i_{L2} keeps decreasing until zero current is reached. The recharging process begins when v_{o2} reaches a threshold voltage of 5 V. A zoom-in view of the waveforms for v_{in2} , i_{L2} and v_{o2} during the pulse recharging period is shown in Fig. 3.13(c). The input port of the cell is open briefly to enable the charging pulse. The input voltage v_{in2} resonates to zero after half of a resonance period, at which point i_{L2} reaches its peak

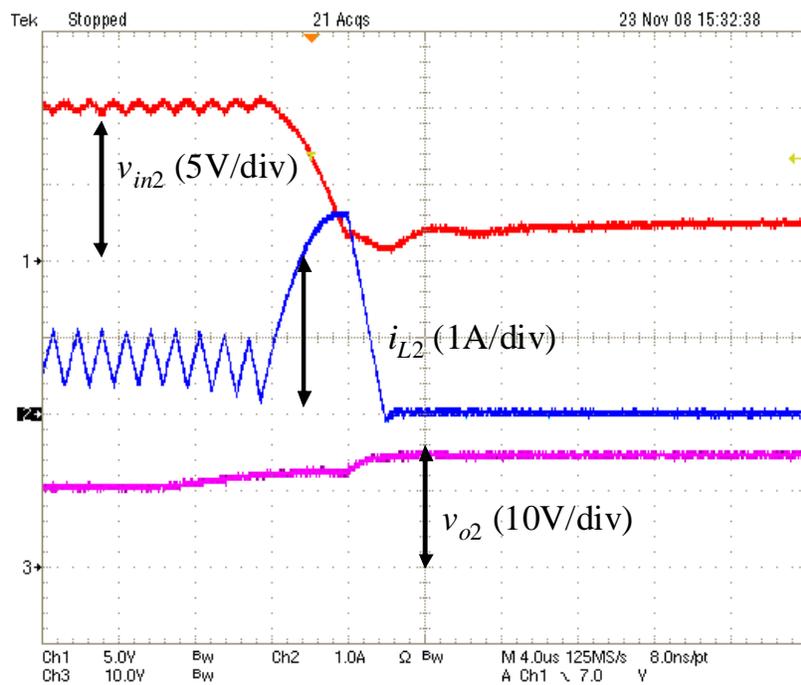
value. The input port is shorted again and the inductor current is used to charge the output capacitor until i_{L2} becomes zero. When this type of failure occurs, the total input voltage will be shared by the other cells according to their load ratio. If desired, the master cell could detect the change in input voltage and modify the LED current to maintain total light output of the system, within the limitations of the LED specifications.

E. Efficiency of series-input-connected converters

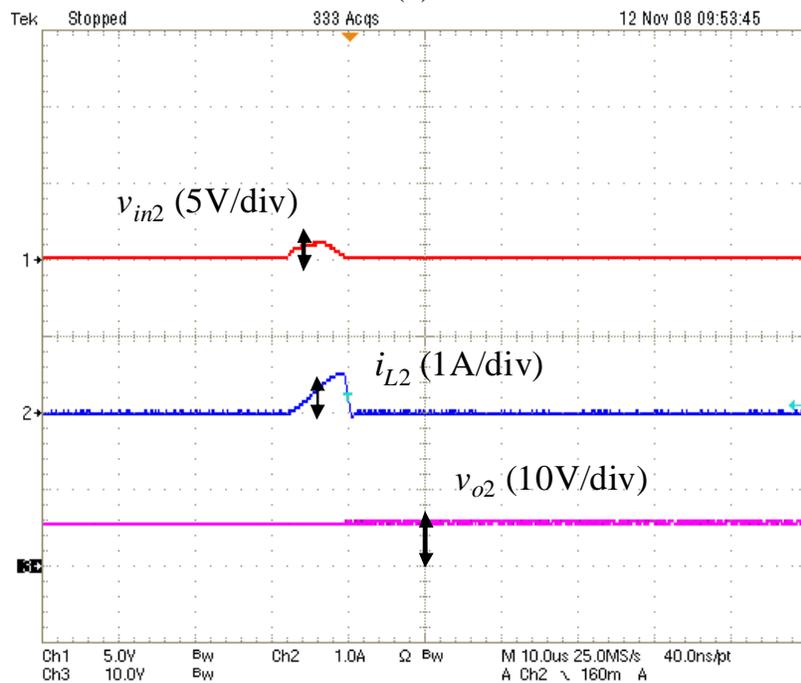
The measured efficiency of the series-input-connected converter circuits for experiment is shown in Table 3.5, which includes values after the LED failure in cell 2 occurs. Similar efficiency is achieved before and after the LED failure. The result is in contrast to typical approaches, where either the entire LED string fails or parallel Zener diodes are used for each LED or sub-set of LEDs. In the case of using parallel Zener diodes, significant loss associated



(a)



(b)



(c)

Figure 3.13: (a) Input voltage, inductor current and output voltage waveforms for a cell with LED open-circuit failure, (b) zoom-in of (a) at the instant when LED failure occurs, (c) zoom-in of (a) when the output capacitor is recharged.

TABLE 3.5 EFFICIENCY OF SERIES-INPUT CONVERTERS FOR EXPERIMENT

	P_{in} (W)	P_{o1} (W)	P_{o2} (W)	P_{o3} (W)	Efficiency
Normal operation	24.28	4.80	6.94	9.13	85.96 %
LED failure	16.25	4.79	0	9.09	85.42 %

with the diodes results in low efficiency when LEDs fail in the system.

3.5 IC Implementation and Communication Circuitry

With series-input modular structure, the voltage stress on each converter module is significantly reduced, which make it feasible for high-level integration. A block diagram of buck converter modules for series-input system is shown in Fig. 3.14, with the circuitry within broken line to be integrated in ICs. Besides the typical function blocks for digital buck converters, a communication block is necessary to transmit duty cycle information between modules, which is indicated as the *Comm.* block in Fig. 3.14.

Within a series-input system, converter modules are series-connected from input port, thus voltage levels between the modules can be quite different. Communication between neighboring modules, rather than a general communication bus connecting all modules, may significantly simplify related circuits. However, special design is still necessary to realize signal transmission between different voltage levels. One solution is to utilize current signal for communication, while a proposed circuit schematic is shown in Fig. 3.15.

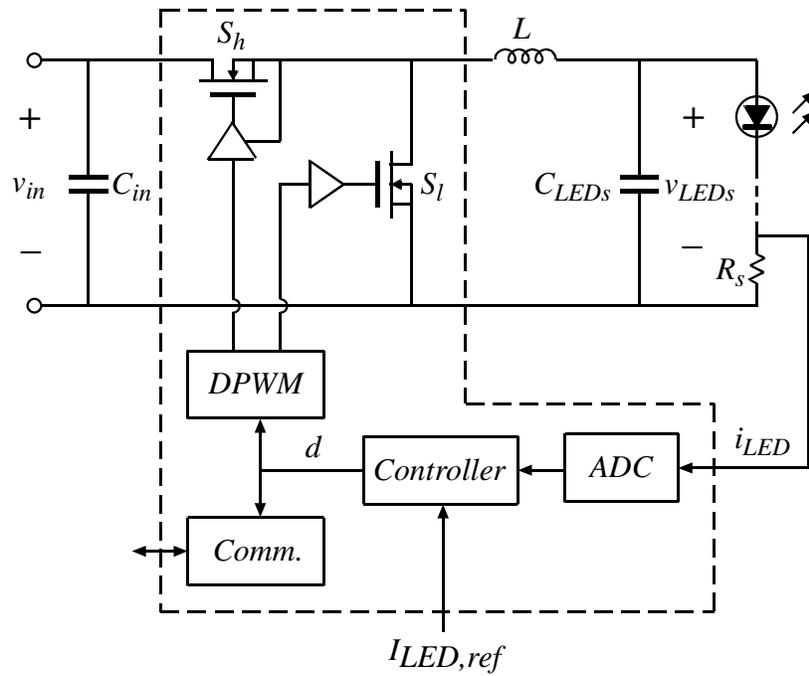
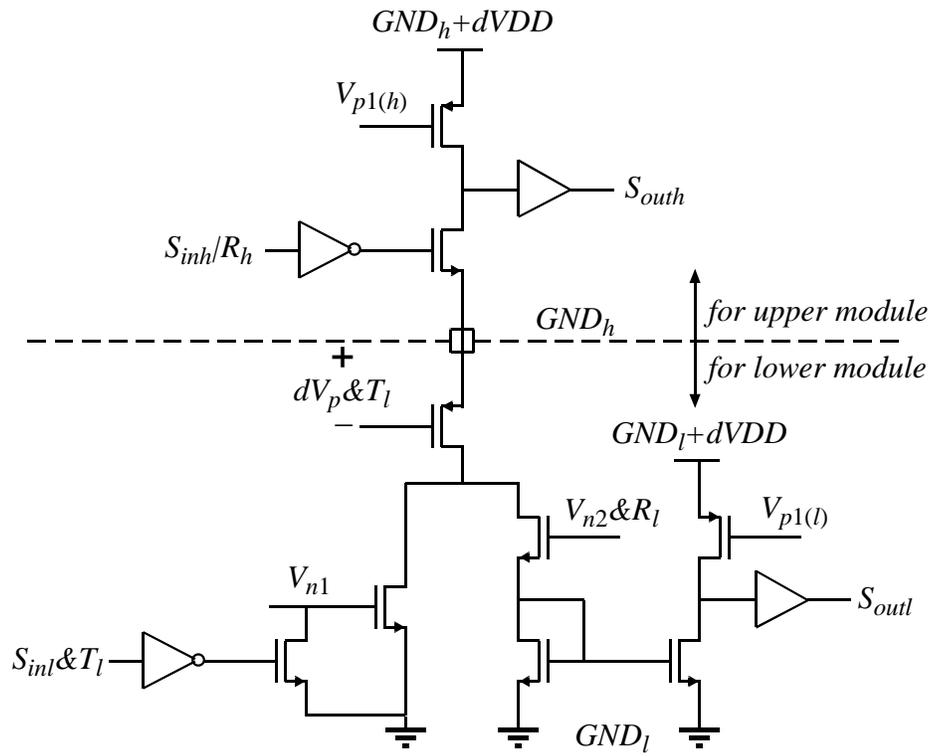
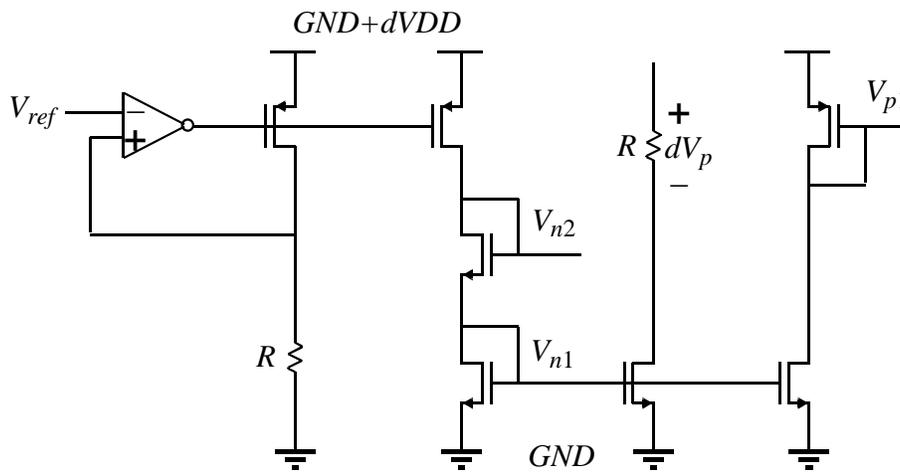


Figure 3.14: Block diagram of buck converter modules for series-input system.

The circuitry in Fig. 3.15 can accomplish communication between two neighboring modules serially connected from input port. The ground for upper module, GND_h , is at the same time the rail voltage for lower module. The top portion of the circuit is within the upper module, while the bottom portion is for the one with lower voltage level, as indicated in Fig. 3.15(a). The circuit to generate required bias signals is shown in Fig. 3.15(b). Signals T and R are the enable flag of transmitting or receiving for the corresponding module. The effective circuit for signal transmission from the lower module to upper one is shown in Fig. 3.16(a), while the circuit for opposite-way transmission is in Fig. 3.16(b).

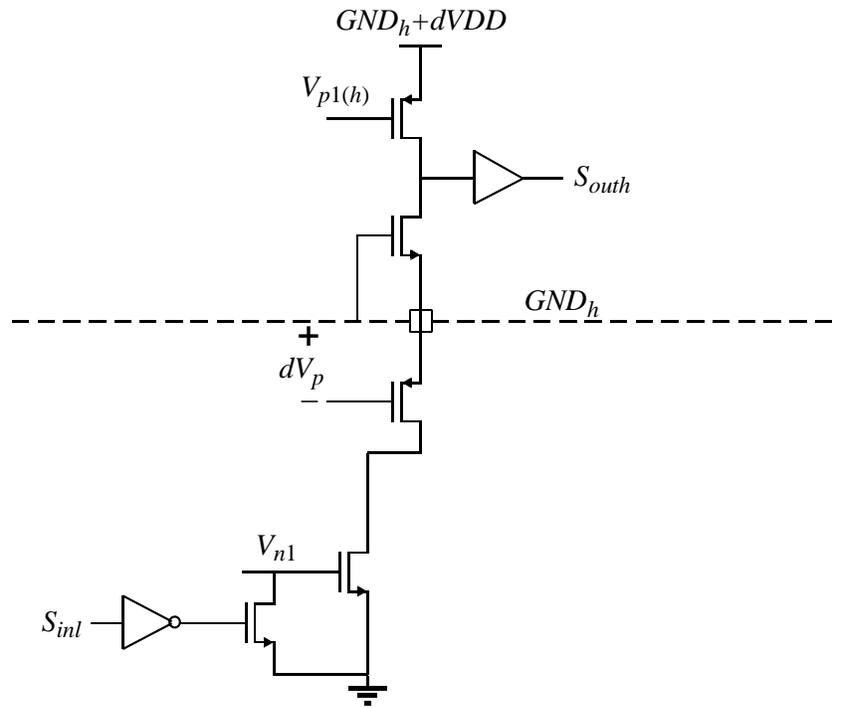


(a)

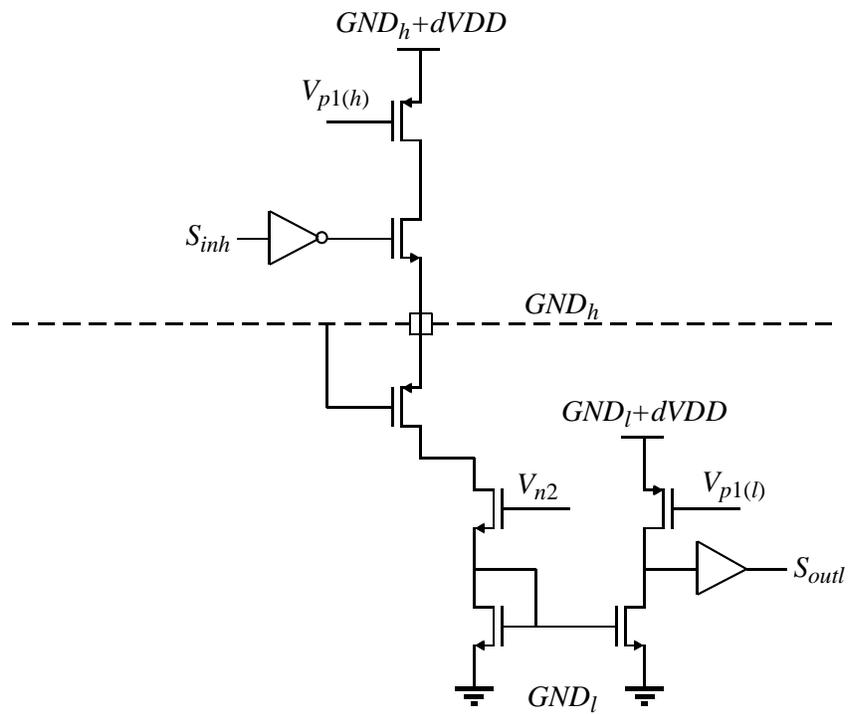


(b)

Figure 3.15: (a) Circuits for communication between series-input modules, and (b) required bias signals. S_{in} and S_{out} represent the input and output signal. $T = 1$ when the corresponding module is transmitting signal, while $R = 1$ when receiving. For a specific module, $T + R = 1$.



(a)



(b)

Figure 3.16: Effective circuit for communication from (a) lower to upper module, and (b) upper to lower module.

3.6 Conclusion

This chapter presents a series-input modular architecture with the common duty cycle control approach for LED drive circuits. When converters with the same topology operate in CCM with identical duty cycle, their conversion ratios are equal, thus their output currents are matched and the input voltage is automatically distributed among the cells according to the ratio of their output voltages. Consequently, only one feedback loop is necessary to control the entire system regardless of the number of modules, which significantly simplify system design and compensation. With the series-input structure and the common duty cycle approach, low-voltage cells and components can be utilized in a high dc bus voltage system with localized control capability of LEDs. Additionally, a special LED failure mode is capable of maintaining efficient operation of the system in the presence of open-circuit LED failures. The performance of this architecture is verified by experiments.

Compared to the single high-voltage converter circuit, more components are required by the proposed modular structure, especially when more modules are designed to leave some margin for LED failure response, which may lead to a higher cost. This drawback is partially mitigated by reduced voltage ratings that scale down with the number of modules. Each low-voltage module can be integrated on a single IC and operated at high frequencies for low-profile and high-power-density applications.

CHAPTER IV

OFF-LINE LED DRIVER WITH REDUCED ENERGY-STORAGE CAPACITANCE

LED applications whose drivers are directly connected to the ac line, often termed “off-line” applications, contribute to a large share of LED lighting market. For these LED applications, standards and regulations place limitations on the input power factor (PF), e.g. 0.9 for commercial products and 0.7 for residential products [3]. Achieving a high PF results in a large input power ripple at twice the line frequency. If this ripple is passed directly to the LED load, it generates significant variation in LED current and may lead to visible flicker [39] and life degradation of LED devices through thermal cycling. Low-quality bulk capacitors are often used in off-line LED drivers to filter the input power ripple at low costs. Unfortunately, the combination of low quality, large ripple and high temperature in lighting applications result in low lifetimes of the bulk capacitors and thus the LED drivers [10].

In order to achieve longer lifetimes for LED applications, it is of significant importance to remove the short-life electrolytic capacitors from the drivers. Magnetic energy storage is suggested in [23, 24] instead of capacitance, with the trade-off of large size, weight and high cost. Another popular topic is the reduction of required energy-storage capacitance, so that high-quality capacitors with long lifetime can be used while maintaining reasonable cost. Methods are reported in [13-16] to reduce the input power ripple with specific input current shaping. Energy

storage capacitors are decoupled from the LED string to make full use of the capacitance in [17, 18].

This chapter introduces and combines multiple techniques to reduce the required energy-storage capacitance in off-line LED drivers. The concept of energy-storage capacitance and the general methods to reduce it are introduced in Section 4.1. Section 4.2 presents the approaches to reduce the energy to be stored and released within each half-line cycle, including constant input current approach to reduce input power ripple, and the trapezoidal LED current waveform approach to minimize storage requirement when certain ripple is allowed on LED current. A special bidirectional second stage is introduced in Section 4.3. With the decoupling from LED load by the second stage, the energy-storage capability of the capacitor can be fully used. Meanwhile, the bidirectional structure reduces the percentage of energy processed by the second stage, leading to relatively small power loss. Section 4.4 presents more details on system design, including control loops, independent regulation of the LED current ripple, and techniques to reduce switching loss on the second stage. All these concepts are verified in experiment, with the experimental set-up and results presented in Section 4.5. Section 4.6 concludes this chapter.

4.1 Energy-storage capacitance for off-line applications

For off-line LED applications, high power factor (PF) is required, which leads to large input power ripple. For example, when $PF = 1$, the input power swings between zero and the peak value which is twice of the average input power. This large variation in power leads to very large current ripple if directly applied onto the LED string. In order to avoid flicker or life degradation associated with large LED current variation at low frequency, energy storage is necessary to filter the input power ripple. The simplest filter is to parallel a capacitor with the LED string. However,

with this approach, very large capacitance may be necessary to achieve small LED current ripple.

The required capacitance can be calculated from

$$C_{ES} = \frac{2E_{stored}}{V_{ESC,peak}^2 - V_{ESC,valley}^2} = \frac{E_{stored}}{2V_{ESC}\Delta V_{ESC}}, \quad (4.1)$$

where E_{stored} is the required energy to be stored within one input power cycle, while $V_{ESC,peak}$, $V_{ESC,valley}$, V_{ESC} and ΔV_{ESC} are the peak, valley, dc value and ripple of the energy-storage capacitor voltage, $V_{ESC,peak} = V_{ESC} + \Delta V_{ESC}$, $V_{ESC,valley} = V_{ESC} - \Delta V_{ESC}$. When the energy-storage capacitor is directly parallel with the LED string, very small ΔV_{ESC} is allowed, as a small variation on LED voltage leads to large change on the current. As a result, the required capacitance can be very large, and electrolytic capacitors become the only practical choice, thus limiting the lifetime of LED lamps.

According to Eq. 4.1, required energy-storage capacitance can be reduced by decreasing energy storage E_{stored} , increasing dc capacitor voltage V_{ESC} or capacitor voltage ripple ΔV_{ESC} . To reduce E_{stored} , either a smaller input power ripple or larger output power ripple should be adopted, which will be discussed in Section 4.2. Manipulation of the capacitor voltage is another important approach to reduce energy-storage capacitance, which will be discussed in Section 4.3.

4.2 Reduction of energy storage

One approach to reduce required energy-storage capacitance is to decrease E_{stored} , the energy needed to be stored in each input power cycle. In order to reduce E_{stored} , either a smaller input power ripple or larger output power ripple should be adopted. As the LED applications are allowed to have input PF less than unity, it is possible to reduce input power ripple by shaping

the input current, with the trade-off of lower PF [13-16]. On the other hand, allowing certain LED current ripple at double-line frequency also helps reduce E_{stored} .

4.2.1 Reducing input power ripple with constant input current

The power factor of a circuit can be calculated by

$$PF = \frac{P_{in,avg}}{V_{in,rms} \times I_{in,rms}} \quad (4.2)$$

where $V_{in,rms}$ and $I_{in,rms}$ are the rms value of input voltage and input current, and $P_{in,avg}$ is the average input power of the circuit. In order to achieve near-unity PF, normally a power factor correction (PFC) stage followed by a bulk capacitor is placed between the ac source (line) and the application circuit, as shown in Fig. 4.1. The PFC stage often requires input voltage and current sensing and can be realized using a wide range of control approaches [5]. For the solid-state lighting industry, ENERGY STAR requirements place limits on the power factor at $PF \geq 0.7$ for residential lighting products and $PF \geq 0.9$ for commercial lighting. The drawbacks to achieving high-quality PF with very low total harmonic distortion (THD) include increased circuit complexity, reduced efficiency and increased requirement for either bulk energy storage or large double-line-frequency current ripple in the LED load. These drawbacks provide motivation to minimize the PF to just meet the requirements in the specification.

The ideal off-line LED driver should achieve input $PF = 1$ and constant LED current, resulting in the input and output power waveforms shown in Fig. 4.2(a). The corresponding input voltage, current and power may be represented as

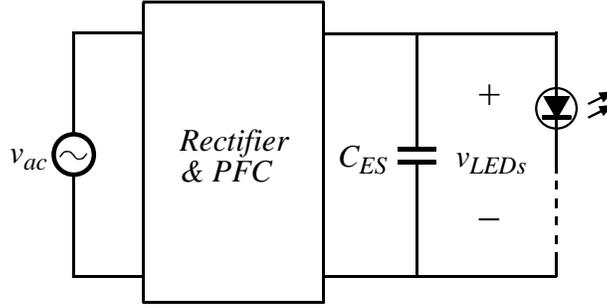


Figure 4.1: An off-line LED driver with PFC stage and bulk energy-storage capacitor.

$$\begin{aligned}
 v_{in}(t) &= |v_{ac}(t)| = V_{in,peak} |\sin(2\pi t / T_{line})|, \\
 i_{in}(t) &= |i_{ac}(t)| = I_{in,peak} |\sin(2\pi t / T_{line})|, \\
 p_{in}(t) &= p_{ac}(t) = v_{in}(t) i_{in}(t) = P_0 (1 - \cos(4\pi t / T_{line})), \\
 P_0 &= V_{in,peak} I_{in,peak} / 2 = P_{LEDs}.
 \end{aligned} \tag{4.3}$$

The shadowed area in Fig. 4.2(a), or E_{stored} , represents the energy to be stored in a half-line cycle $T_{line}/2$, and it can be shown that

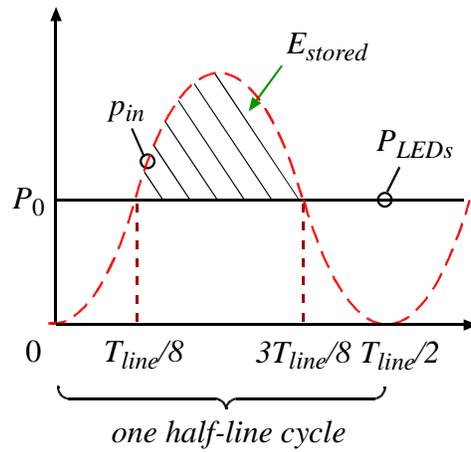
$$E_{stored} \approx 32\% \times P_0 T_{line} / 2 = 32\% \times E_{cycle}. \quad (PF = 1) \tag{4.4}$$

Equation 4.4 means that about 32% of the total input energy within one half-line cycle has to be stored to achieve constant output power.

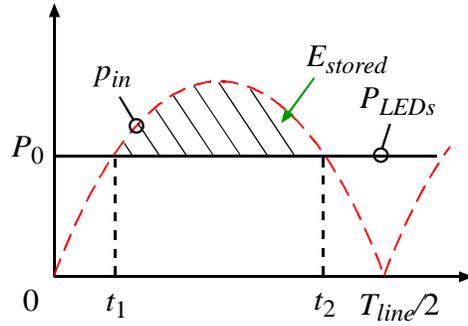
When the input current is regulated to be a constant value, Eq. 4.2 becomes

$$PF = \frac{P_{in,avg}}{V_{in,rms} \times I_{in,rms}} = \frac{V_{in,avg} \times I_{in}}{V_{in,rms} \times I_{in}} = \frac{2 / \pi \times V_{in,peak}}{\sqrt{2} / 2 \times V_{in,peak}} \approx 0.9. \tag{4.5}$$

This leads to a relatively simple controller that meets the PF requirements for lighting products and minimizes the input power ripple at double line frequency. Fig. 4.2(b) demonstrates the input and output power waveforms for an off-line LED driver with constant input current (PF = 0.9) and constant LED current, with input voltage, current and power represented as



(a)



(b)

Figure 4.2: Input and output power waveforms for (a) an LED driver with $PF = 1$ and constant LED current, and (b) an LED driver with constant input current ($PF = 0.9$) and constant LED current.

$$\begin{aligned}
 v_{in}(t) &= |v_{ac}(t)| = V_{in,peak} |\sin(2\pi t / T_{line})|, \\
 i_{in}(t) &= |i_{ac}(t)| = I_{in}, \\
 p_{in}(t) &= p_{ac}(t) = v_{in}(t) i_{in}(t) = \pi/2 \times P_0 |\sin(2\pi t / T_{line})|, \\
 P_0 &= V_{in,peak} I_{in} \times 2/\pi = P_{LEDs}.
 \end{aligned} \tag{4.6}$$

It can also be proved that

$$E_{stored} \approx 21\% \times P_0 T_{line} / 2 = 21\% \times E_{cycle}. \quad (PF = 0.9) \tag{4.7}$$

Comparing Eq. 4.7 to Eq. 4.4, it can be seen that the required energy storage is reduced from 32% to 21% of the total input energy, which helps the reduction of the energy-storage capacitor. Another advantage of the constant input current approach is the relatively easy realization, as the input voltage sensing is unnecessary.

4.2.2 Allowing ripple on LED current

In order to avoid flicker and LED life degradation due to thermal cycling, an ideal LED driver should provide constant LED current. However, a small percentage ripple on LED current may be acceptable in practical applications. Allowing certain ripple on LED current helps reduce energy storage, which is very useful when the available capacitance is limited. Keeping ripple under certain limits, the LED current should be manipulated in a special way to minimize the required energy storage.

The waveforms of input and output power for a unity-PF LED driver with certain LED current ripple are shown in Fig. 4.3(a), with the shadowed areas indicating the energy stored in and released from the capacitor within one half-line cycle. As the LED string voltage is almost constant, the waveform of LED current has the similar shape of LED string power p_{LEDs} , which is close to “trapezoidal” and in phase with input power. It can be seen that the input power waveform is “chopped” only around its peak or valley, resulting in an LED string power stay at the regulation boundaries for most of the time. In this way, the minimum energy storage is achieved for certain LED current ripple, which is proved in Appendix B. Fig. 4.3(b) demonstrates the percentage energy storage, E_{stored}/E_{cycle} , for different percentages of LED current ripple, where E_{cycle} is the total input energy within a half-line cycle. The maximum required energy storage, which happens with zero LED current ripple, is approximately 32% of the total input energy.

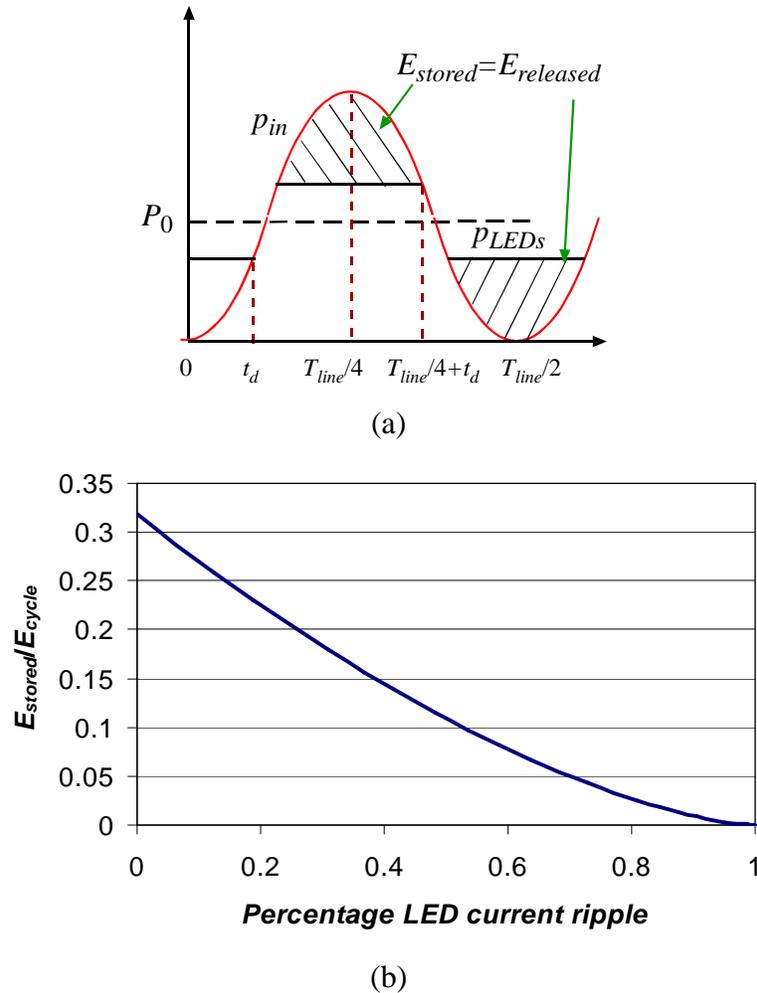


Figure 4.3: (a) Input and output power waveforms for an off-line LED driver with PF = 1 and trapezoidal LED current; (b) required percentage energy storage (E_{stored}/E_{cycle} , E_{cycle} is the total input energy within one half-line cycle) for different LED current ripple values.

When 30% ripple is allowed on LED current, the required energy storage decreases to about 18%, in which case the required energy-storage capacitance is significantly reduced.

The waveforms of input and output power for an off-line LED driver with constant input current and trapezoidal LED current are shown in Fig. 4.4(a), with the shadowed areas indicating the energy to be stored in and released from the capacitor. Similarly, the required energy storage is minimized with this trapezoidal waveform, for each percentage LED current ripple. Fig. 4.4(b)

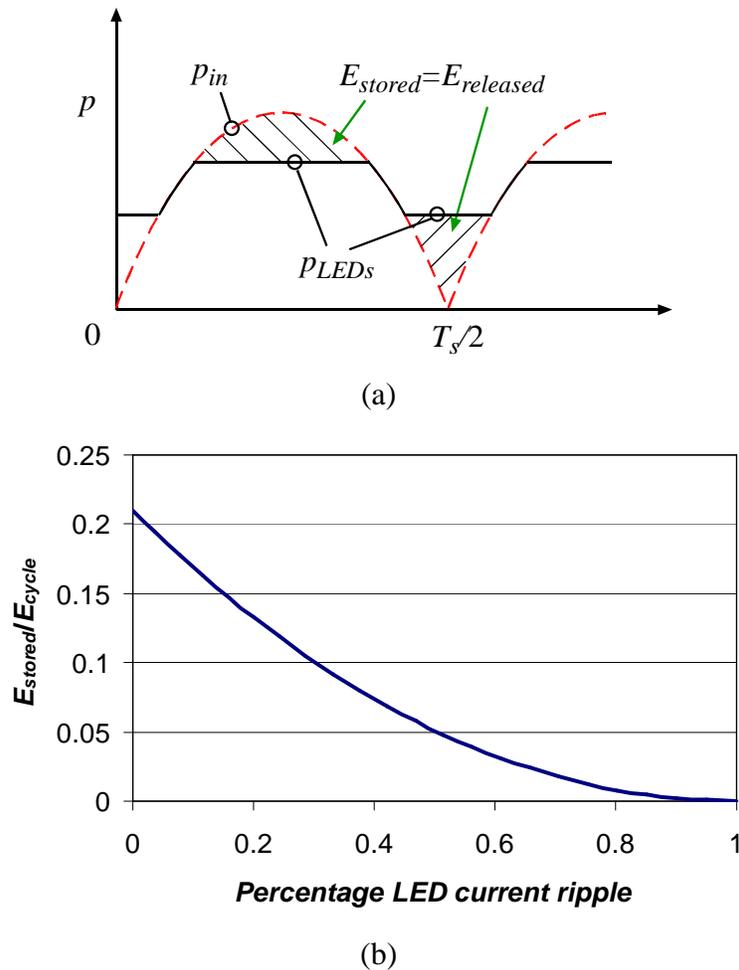


Figure 4.4: (a) Input and output power waveforms for an off-line LED driver with constant input current and trapezoidal LED current; (b) required percentage energy storage (E_{stored}/E_{cycle} , E_{cycle} is the total input energy within one half line cycle) for different LED current ripple values.

demonstrates the percentage energy storage, E_{stored}/E_{cycle} , where E_{cycle} is the total input energy within a half-line cycle for different percentages of LED current ripple. The required energy storage reaches the peak of approximately 21% of total input energy, and decreases significantly when ripple is allowed on LED current. For instance, with 30% LED current ripple, the required energy storage is only about 10% of total input energy.

4.3 Reduction of energy-storage capacitance by manipulating capacitor voltage

4.3.1 Decoupling energy-storage capacitor from LEDs

According to Eq. 4.1, the required energy-storage capacitance can be reduced by increasing the dc value or ripple of capacitor voltage. However, very limited voltage variation is allowed when the energy-storage capacitor is directly parallel with the LED string due to the small dynamic resistance of LED devices. In order to manipulate the capacitor voltage with more freedom, a common approach is to include a second stage in the driver to decouple the capacitor from the LED string. As shown in Fig. 4.5, a dc-dc second stage is placed following the energy-storage capacitor C_{ES} and followed by the LED string. As C_{ES} is decoupled from the LED string, larger voltage ripple is allowed. Furthermore, the capacitor voltage can be boosted higher than the LED string voltage. As a result, the capacitance can be significantly reduced compared to the case of single-stage LED driver.

A comparison is conducted between the required energy-storage capacitances for single-stage and two-stage LED drivers for different LED current ripple, with the result shown in Fig. 4.6. It is assumed that $PF = 1$ and the LED current is trapezoidal, as shown in Fig. 4.3(a). The required capacitances are normalized based on C_0 , the required capacitance for a single-stage LED driver with 50% LED current ripple. The other assumed parameters for this comparison include single LED voltage of 3 V, LED current of 500 mA and small-signal resistance of 0.8Ω for single LED. Meanwhile, the energy-storage capacitor voltage for the two-stage LED driver is assumed to swing between 120% and 180% of V_{LEDs} , where V_{LEDs} is the LED string voltage. As shown in Fig. 4.6, the required energy-storage capacitance is largely reduced with the additional second stage. For example, when 30% LED ripple is allowed, the required capacitance for the two-stage driver is less than 10% of that for the single-stage driver, and it can

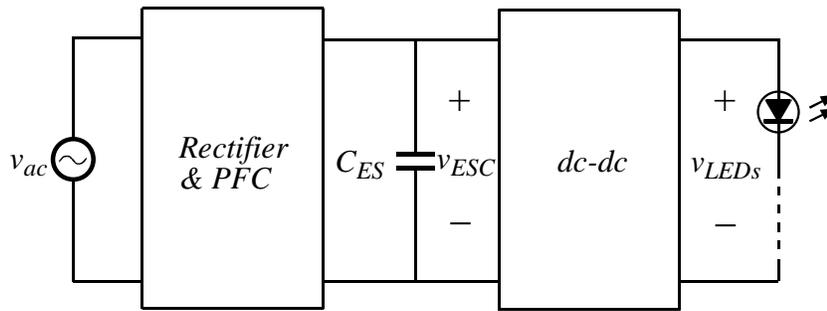


Figure 4.5: Off-line LED driver with PFC first stage and dc-dc second stage.

be seen that the capacitance reduction is even more significant when LED current ripple is small. This comparison is based on an assumption of capacitor v_{ESC} higher than V_{LEDs} , which is the case for a buck second stage. When a boost converter is used in the second stage, v_{ESC} has to be lower than V_{LEDs} always. When a converter with large conversion ratio range, such as a buck-boost converter, is used, a larger swing on v_{ESC} is allowed, and the energy-storage capacitance can be further reduced.

With the cascaded two-stage structure in Fig. 4.5, the efficiency of the second stage is critical, as all the LED power goes through this stage, even when current ripple is allowed on the LED string. As shown in Fig. 4.3 and Fig. 4.4, the maximum required energy storage is 32% of the total input energy when $PF = 1$, and is 21% when $PF = 0.9$. However, even when the required energy storage is further reduced with non-zero LED current ripple, 100% of the output energy must be processed by the second stage, resulting in considerable power loss.

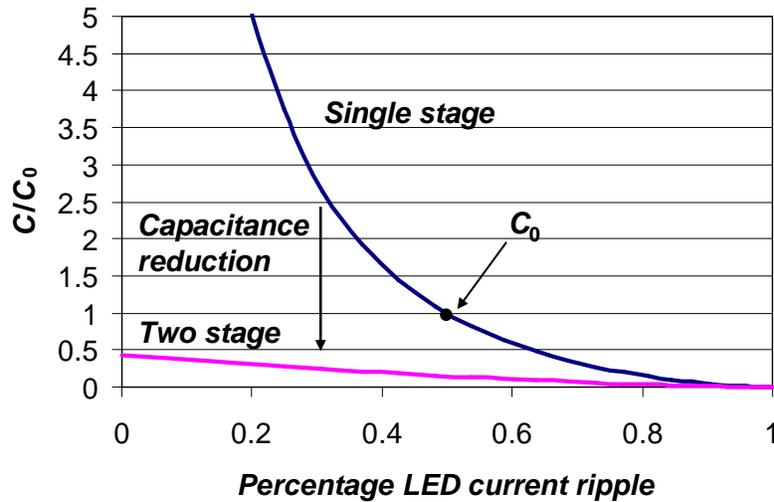


Figure 4.6: Normalized capacitance reduction with additional second stage for different percentage LED current ripples. C_0 is the required energy-storage capacitance for single-stage LED driver with 50% LED current ripple.

4.3.2 Reducing power loss on the second stage with bidirectional structure

An alternative two-stage structure is to switch the positions of the energy-storage capacitor and the LED string, as shown in Fig. 4.7. With this structure, only the excess power goes through the second stage to the energy-storage capacitor C_{ES} when the input power is higher than the desired LED power. When the input power is less than the required amount, portion of the LED string power comes from C_{ES} . Thus, only E_{store} , the shadowed areas in Fig. 4.3(a) and Fig. 4.4(a), is processed by the second stage. The energy processed by the second stage may be largely reduced with this structure, especially when current ripple is allowed on LED string, as shown in Fig. 4.3(b) and Fig. 4.4(b). For example, when 30% ripple is allowed on LED current, only about 18% (for PF = 1) and 10% (for PF = 0.9) of the input energy is processed by the second stage, thus the power loss on the LED driver can be reduced compared with the traditional cascaded structure.

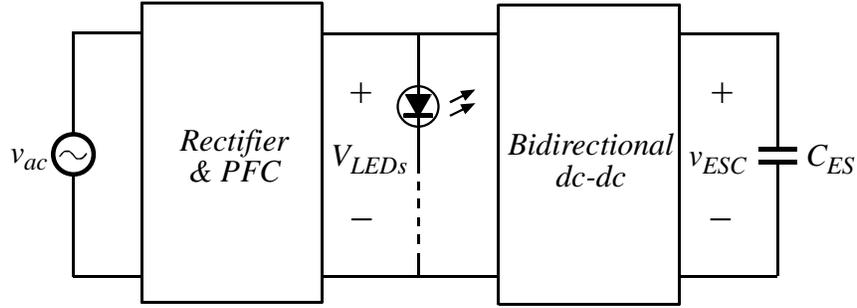


Figure 4.7: LED driver with PFC first stage and bidirectional second stage.

The efficiency of a two-stage LED driver with bidirectional second stage in Fig. 4.7 can be derived as

$$\eta_b = \frac{\eta_{1b}\eta_{2b}^2}{\eta_{2b}^2 + \lambda(1 - \eta_{2b}^2)}, \quad (4.8)$$

where η_{1b} and η_{2b} are the respective efficiencies of the first and second stage, and λ is the percentage of LED energy processed by the second stage, or E_{stored}/E_{cycle} , which is shown in Fig. 4.3(b) and Fig. 4.4(b). For comparison, the efficiency of a traditional two-stage LED driver, which is shown in Fig. 4.5, is represented as

$$\eta_t = \eta_{1t}\eta_{2t}, \quad (4.9)$$

where η_{1t} and η_{2t} are respective efficiencies of the first and second stage. In order to simplify the comparison, it is assumed that $\eta_{1b} = \eta_{1t}$ and $\eta_{2b} = \eta_{2t}$. With this assumption, it can be proved that the overall efficiency η_b is larger than η_t when

$$\eta_{2b} > \frac{\lambda}{1 - \lambda}. \quad (4.10)$$

As shown in Fig. 4.3(b), for 0 to 100% LED current ripple when $PF = 1$, it is always valid that $\lambda < 0.32$, thus $\lambda/(1-\lambda) < 0.47$. As a result, when the second stage efficiency η_{2b} is larger than 0.47,

Eq. 4.10 is always valid, and the efficiency of the two-stage LED driver with the bidirectional second stage is larger than that of traditional cascaded driver. Similarly, when $PF = 0.9$ is achieved with constant input current approach, $\lambda < 0.21$, thus $\lambda/(1-\lambda) < 0.27$, and it is even easier to achieve better overall efficiency with the bidirectional structure.

4.4 System design

4.4.1 Control loops

Compared with the traditional cascaded two-stage structure, more interactions occur between the two stages in proposed LED drivers, thus the system control loops require carefully design. One configuration for the system control is shown in Fig. 4.8. The purpose of the bidirectional second stage is to filter the double-line-frequency power ripple. This function can be realized by regulating the LED current with the second stage. When the LED current, thus LED power, is regulated, the excess input power ripple automatically goes through the second stage to the energy-storage capacitor. Besides the LED current control loop, one additional loop is required to regulate the voltage on the energy-storage capacitor, so as to equalize LED power to average input power. The balance between input and LED power can be achieved by adjusting the average LED current, which can be the reference signal for the LED current regulation. Additionally, the average LED current should be compared to the LED current command, which is the external input signal for this system. The comparison result is fed back to the first stage to control the input power. In all, four loops are necessary, shown in Fig. 4.8, including the PFC, LED current regulation, energy-storage capacitor voltage control and the power control loops.

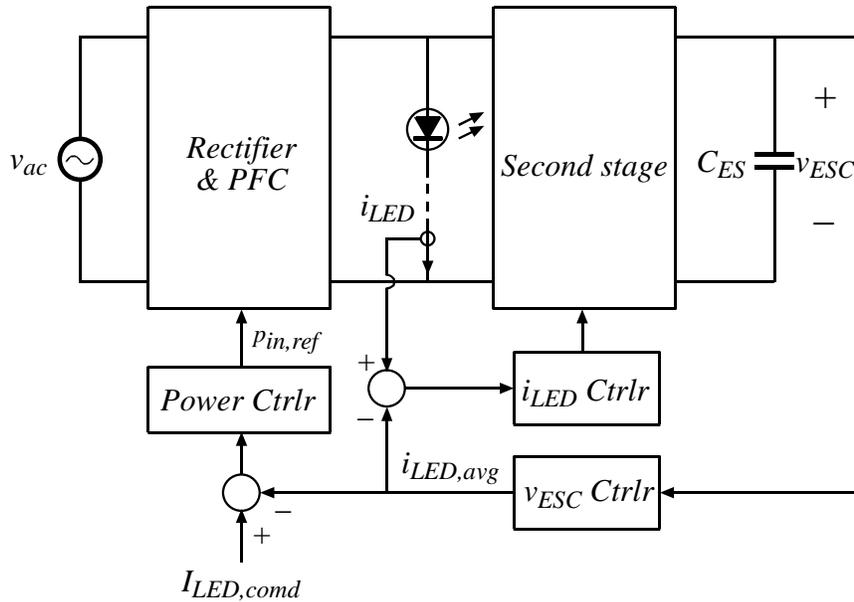


Figure 4.8: Control loops for the proposed two-stage off-line LED driver, including PFC, LED current regulation, energy-storage capacitor voltage regulation and input power control.

It is possible to simplify the control loops of the system to those shown in Fig. 4.9. The external LED current command is directly used to regulate the LED current in the second stage. One other loop regulating energy-storage capacitor voltage directly generates the input power signal for the PFC stage. With this configuration, three loops are necessary for the whole system, which simplifies the design. Furthermore, better regulation on LED current is expected.

The function of LED current ripple control is also included in this system. In order to achieve trapezoidal LED current, two reference values are necessary. The high and low current references are calculated with the average LED current signal $i_{LED,avg}$ in Fig. 4.8, and a ripple current command as shown in Fig. 4.10. The reference transition is realized by detecting energy-storage capacitor voltage v_{ESC} and LED current i_{LED} . As shown in Fig. 4.10(a), the LED current is regulated with high reference during period r_h when input power is large and with low reference during period r_l when input power is small. The LED current controller is disabled during

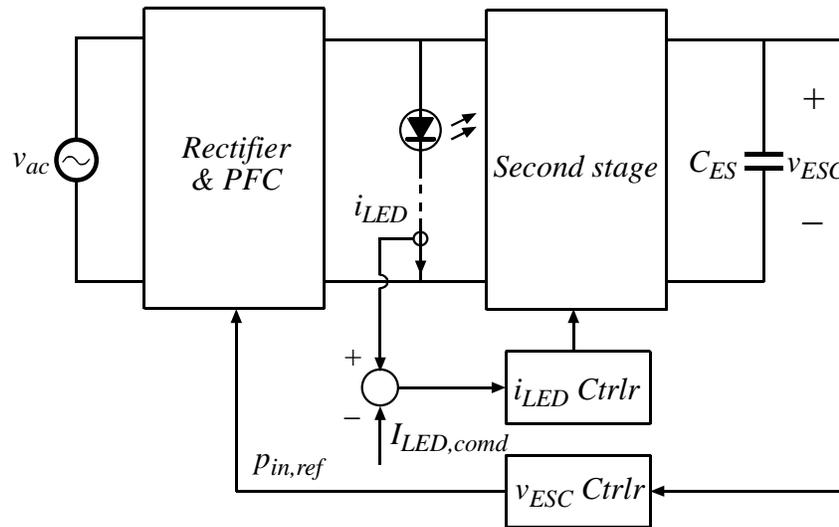
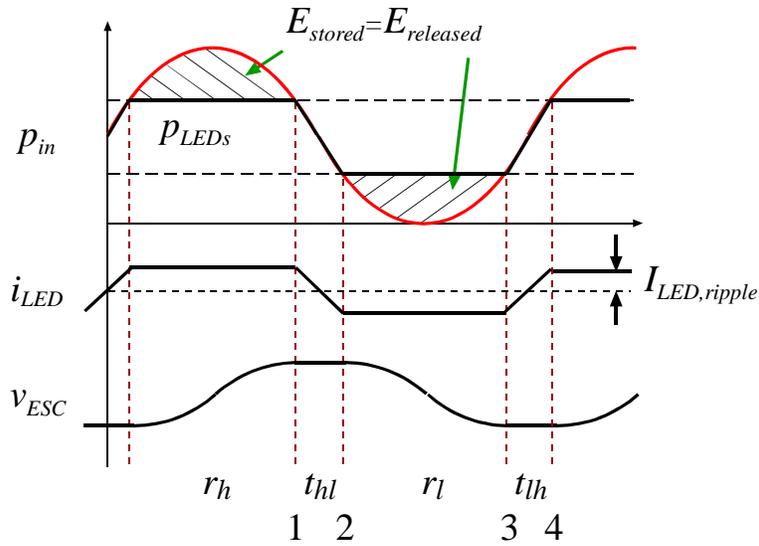
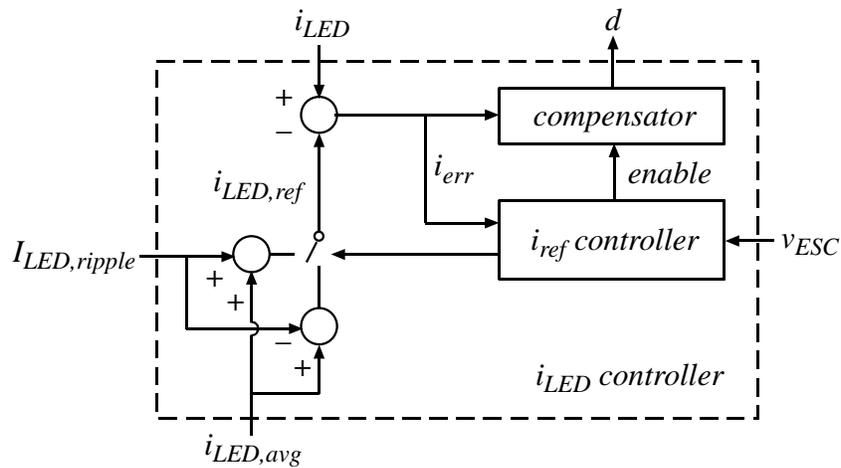


Figure 4.9: Simplified control loops for the proposed two-stage off-line LED driver, including PFC, LED current regulation, energy-storage capacitor voltage regulation.

transition periods t_{hl} and t_{lh} , during which intervals all the input power is directly consumed by the LED load. During period r_h , v_{ESC} keeps increasing, indicating excess input power. At instant 1, the peak of v_{ESC} is detected, indicating input power equal to LED power. After this instant, i_{LED} controller is disabled and i_{LED} decreases following the input power. At instant 2, i_{LED} reaches the low reference, at which point the i_{LED} controller is enabled with low reference value. The current regulation is stopped again when minimum v_{ESC} is detected at instant 3, and starts at instant 4 when i_{LED} hits the high reference value. With this control procedure, the trapezoidal LED current is achieved, thus the required energy storage is minimized.



(a)

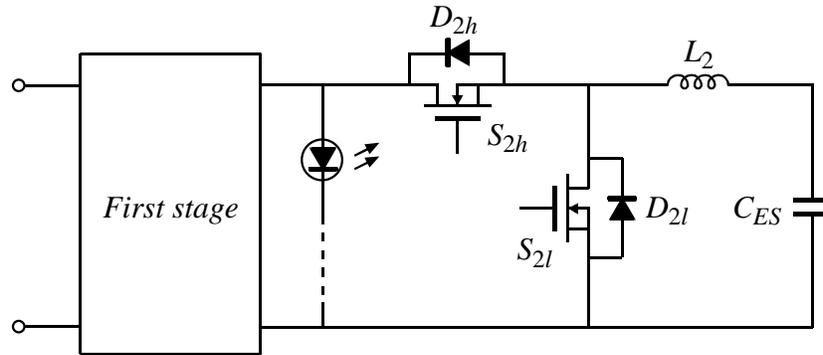


(b)

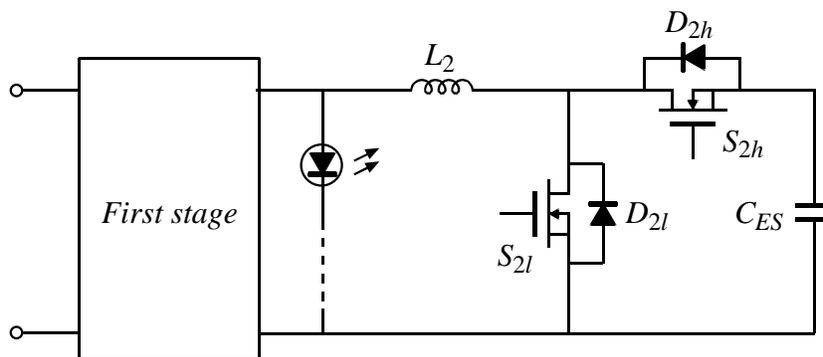
Figure 4.10: (a) Reference transition by detecting v_{ESC} and i_{LED} , (b) i_{LED} controller with ripple control to implement trapezoidal LED current.

4.4.2 Realization of the bidirectional second stage

With the proposed two-stage structure in Fig. 4.7, the second stage has to be bidirectional, as the energy-storage capacitor has to be able to store energy from the first stage and to supply energy back to the LED string according to instant input power level. Several converters are



(a)



(b)

Figure 4.11: (a) A synchronous buck converter, and (b) a synchronous boost converter as bidirectional second stage.

feasible for this function. One option is synchronous converters. One synchronous buck converter as bidirectional second stage is shown in Fig. 4.11(a), while a synchronous boost second stage is in Fig. 4.11(b). For both converters, their high-side and low-side transistors switch on and off complementally within every switching period. As they always operate in continuous conduction mode (CCM) while the inductor current can become negative, energy can be delivered in both directions.

4.4.3 Reducing switching loss on the second stage

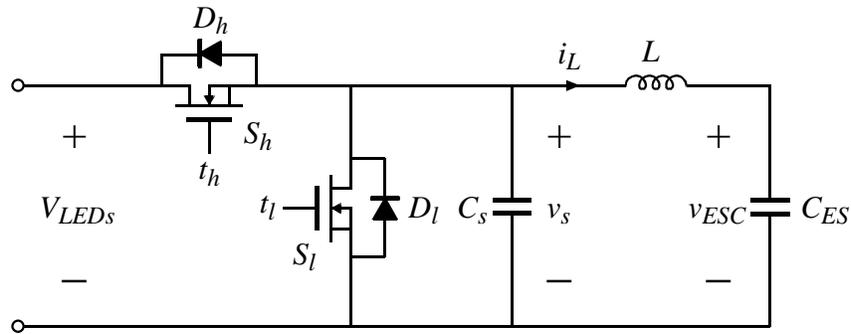
According to Eq. 4.1, it is possible to reduce required energy-storage capacitance by increasing voltage on the capacitor. However, high voltage leads to significant increase of power loss, especially switching losses. In order to limit power loss on the bidirectional second stage, techniques like soft switching may be employed.

Switching loss is normally a major power loss concern for high-voltage applications [5, 42, 43]. This type of loss occurs at the instants of switches turning on. Besides the power loss due to charging or discharging parasitic capacitance at the switching node, reverse recovery effect of diodes may also cause a huge loss. When a conducting diode is forced to go off, it takes a short period to remove the charge stored in the diode semiconductor junction, namely, reverse recovery charge. During this period, the diode stays forward biased, and thus large voltage is placed across the switch/switches turning on, resulting in significant power loss. This type of loss can be eliminated with operation in DCM. When a converter operates in DCM, the inductor current reaches zero before any switch is turned on, thus no diode has to be forced off. Although operation in DCM eliminates power loss associated with diode reverse recovery effect, the remaining switching loss, which is related to the parasitic capacitance at the switching node, still exists. When one switch, across which the voltage is non-zero, is forced to turn on, energy is wasted to reduce this voltage difference, either by charging or discharging parasitic capacitance. Thus, switching loss with converters in DCM can still be large, especially for large parasitic capacitance, high voltage or high switching frequency situations.

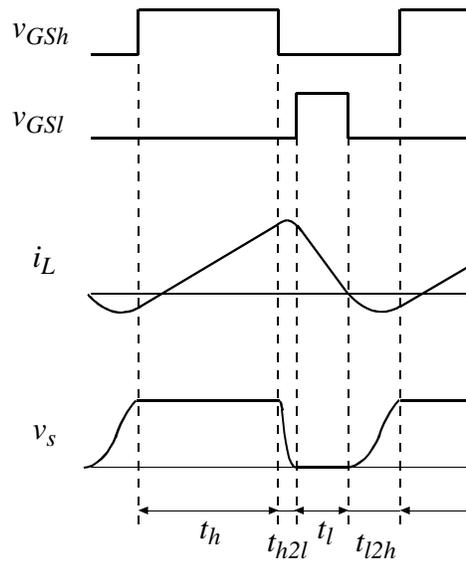
One popular solution to eliminate switching loss entirely is the soft switching technique, which employs the resonance between inductors and parasitic capacitors to manipulate the switching-node voltage, thus to achieve zero-voltage turn-on of the switches [5]. Take the

synchronous buck converter as an example of a soft switching operation. The schematic of the converter is shown in Fig. 4.12(a), and the waveforms of high-side MOSFET gate-to-source voltage v_{GS_h} , low-side MOSFET gate-to-source voltage v_{GS_l} , inductor current i_L and switching-node voltage v_s are shown in Fig. 4.12(b). During time interval t_h , the high-side MOSFET S_h is conducting, and the inductor current gradually increases. During the interval t_{h2l} , when S_h has been turned off while S_l has not been turned on, the inductor L resonates with the switching node capacitor C_s , which decreases the switching-node voltage v_s down to zero. Consequently, the low-side MOSFET S_l may be turned on with zero across voltage, thus with no switching loss. Similarly, resonances may be utilized to achieve zero-voltage turn-on for the high-side MOSFET. To guarantee that v_s can reach input voltage by resonance, the inductor current has to reach a certain negative value in order to charge C_s to V_{LEDs} . As shown by the waveforms in Fig 4.12(b), the inductor current has to be positive for high-side to low-side soft switching and negative to achieve soft switching for low-side to high-side transition. As a result, the ripple on inductor current has to be larger than the average inductor current.

Although with the capability to remove switching loss, the soft switching technique enlarges inductor current ripple, and thus results in larger conduction loss. This drawback, however, is not a big issue for LED lighting application, whose load and inductor currents are normally small.



(a)



(b)

Figure 4.12: (a) Synchronous buck converter and (b) switching control signal, inductor current and switching node voltage for soft switching.

4.4.4 Reducing transient ringing with initial duty cycle estimation

As shown in Section 4.4.1, the ability of the LED current ripple control is included in this off-line LED driver. In order to minimize required energy storage, a trapezoidal LED current waveform is targeted, meaning that LED current is regulated to a high reference when input power is large and to a low reference when input power is small, as shown in Fig. 4.13. Between these regulation periods are the transition periods, during which the second stage is off to reduce

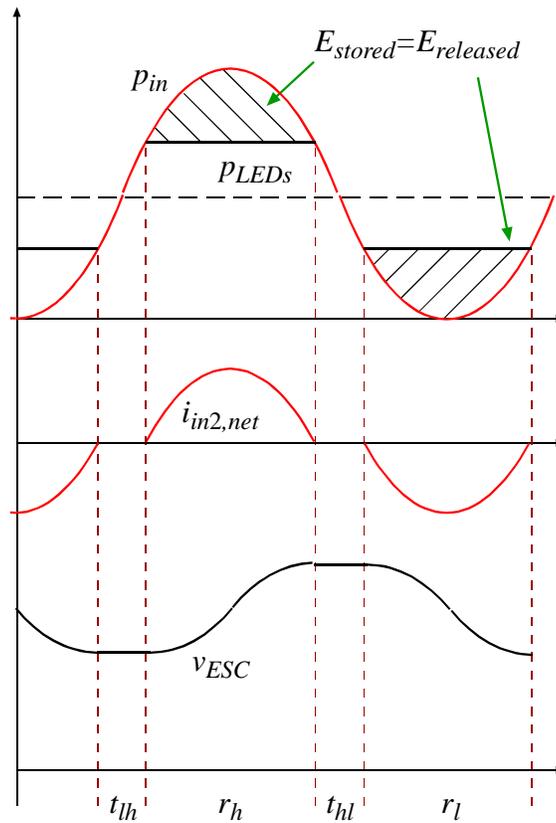


Figure 4.13: Waveforms of input power and LED power, net input current of second stage, and voltage on energy-storage capacitor.

power loss and the input power is directly applied to LED load, as indicated by periods t_{lh} and t_{hl} in Fig. 4.13.

When the second stage operates in CCM, ringing on LED current may occur at the beginning of each regulation period, which is due to inrushing inductor current, including large variation and/or non-zero average value on inductor current.

The inductor current is under control in quasi-steady state, which means the second stage operates very close to a steady state during every short period when voltages on the LED string and the energy-storage capacitor are almost constant. In this case, the integral of volt-seconds on

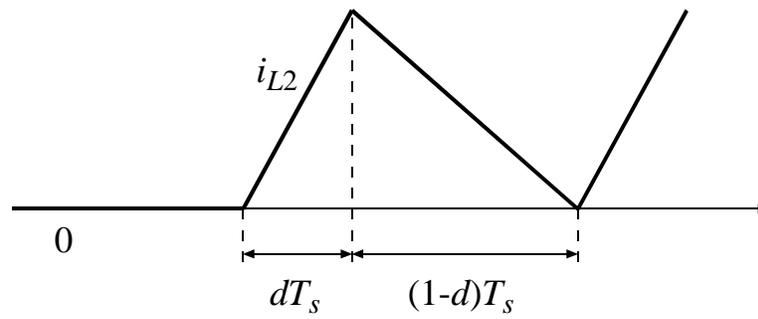
the inductor is approximately zero; thus, no large variation occurs on the inductor current under this condition. Otherwise, a non-zero integral of volt-seconds causes continuous increase or decrease of inductor current and may result in large spikes on the LED current. With volt-second balance on the inductor, the relation of duty cycle and voltages on the LED string and energy-storage capacitor can be derived. The corresponding relation for the boost second stage is shown in Eq. 4.11, which coincides with the conversion ratio of boost converter in CCM.

$$\frac{1}{1-d} \approx \frac{v_{ESC}}{v_{LEDs}} \quad (4.11)$$

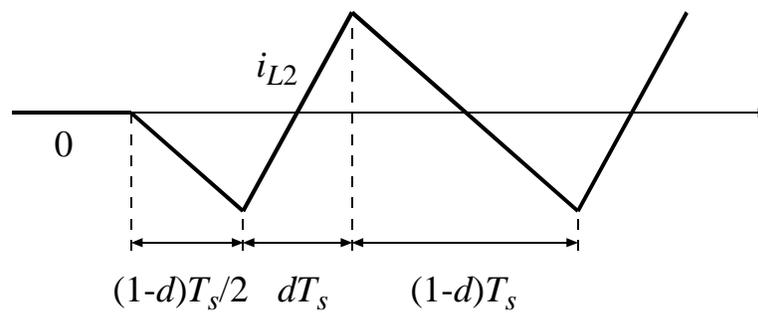
Thus, a proper initial duty cycle is necessary for each regulation period to prevent inrush inductor current and ringing. As shown in Fig. 4.13, the voltage on the energy-storage capacitor stays unchanged during the transition periods. Hence, the final duty cycle of one regulation period seems a good choice to be the initial duty cycle for a following regulation period. However, an adjustment on the duty cycle is necessary, since the LED string voltage does change, which is due to different LED currents for two sequential regulation periods. From Eq. 4.11, it can be derived that the adjustment on duty cycle of boost second stage is equal to

$$\Delta d = -\frac{\Delta v_{LEDs}}{v_{ESC}}. \quad (4.12)$$

Although a proper initial duty cycle achieves volt-second balance on the inductor, thus preventing large inductor current variation, an unsuitable initial inductor current can still cause spikes on LED current, especially when large ripple is designed to be on the inductor current. As shown in Fig. 4.13, the net input current of the second stage should always start from zero in each regulation period. However, when an initial duty cycle complying with Eq. 4.11 is applied, a non-zero average inductor current results and leads to spikes on LED current, as indicated in Fig. 4.14(a). In order to tackle this issue, a half-time conduction period is added before the



(a)



(b)

Figure 4.14: Waveforms of second-stage inductor current (a) without and (b) with additional half-time conduction period indicated as $(1-d)T_s/2$.

normal operation in each regulation period, as shown in Fig. 4.14(b). With this approach, the average inductor current is set to be zero for the first switching period of each regulation period; thus, no spike results on LED current.

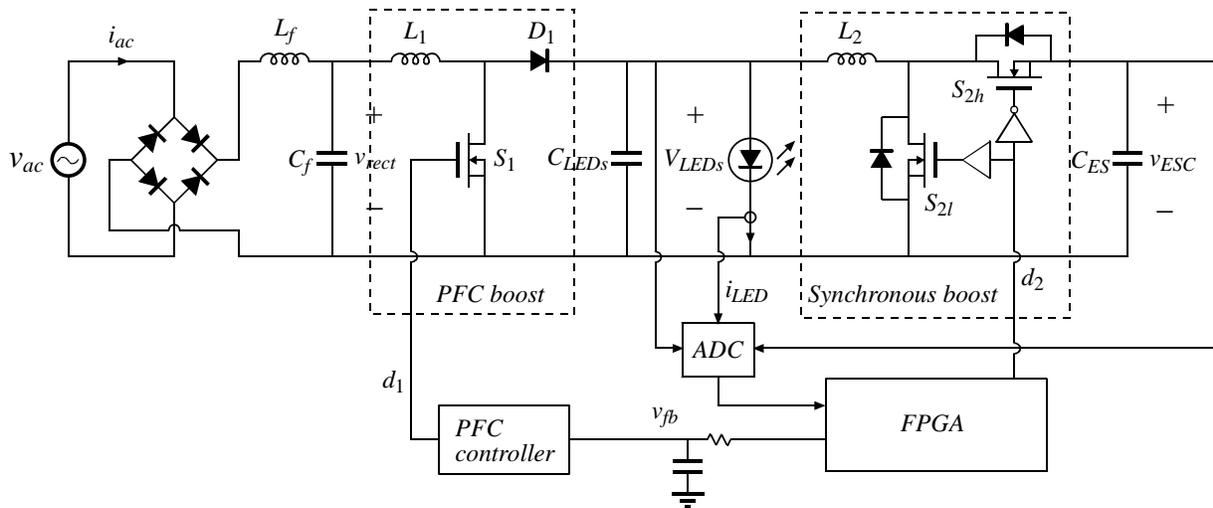


Figure 4.15: Experimental setup: including boost first stage with PFC and synchronous boost second stage.

4.5 Experimental results

A prototype was developed to verify the performance of the proposed techniques and control approach experimentally, with the schematic shown in Fig. 4.15. A two-stage system was implemented for the experiments, with a boost converter operating in CRM as the PFC first stage and a synchronous boost converter as the bidirectional second stage. A commercial PFC control chip is used in the first stage, while the second stage is controlled via FPGA and corresponding sensing circuitry and analog-to-digital converters (ADCs). A simple RC filter is used to convert digital output from FPGA to analog signal v_{fb} , which is fed back to the PFC controller to manipulate the input power. The major devices used in the experiment are shown in Table 4.1, and the major component values are shown in Table 4.2. Two different PFC control ICs are used to achieve $PF = 1$ and $PF = 0.9$, respectively. It can be seen that no electrolytic capacitor is used. The energy-storage capacitor C_{ES} is only $8 \mu\text{F}$ thanks to the bidirectional

TABLE 4.1 MAJOR DEVICES USED IN EXPERIMENT

Device	Part Number	Description
FPGA	XC3S500E	Xilinx Spartan 3E
S_1, S_{2h}, S_{2l}	FDD5N50F	N-channel MOSFET, 500 V, 3.5 A
D_1	ES3G	Diode, 400 V, 3 A
PFC controller	FAN6961	Constant on time CRM
	L6562AT	Transition mode with input current control
ADC	AD7825	8-bit 4-channel multiplexed
HB driver	FAN7382	Half bridge driver, 600 V
LED	Luxeon K2	700 mA

TABLE 4.2 MAJOR COMPONENTS USED IN EXPERIMENT

Component	Description	Parameter
L_f	Input filter inductor	560 μ H
C_f	Input capacitor	0.47 μ F, 250 V, film
L_1	First stage inductor	330 μ H
L_2	Second stage inductor	100 μ H
C_{ES}	Energy storage capacitor	8 μ F, 700 V, film

second stage. Although the double-line-frequency ripple is filtered by C_{ES} with the second stage, another capacitor C_{LEDs} is parallel with the LED string to filter the switching frequency ripple. The estimation of required capacitance for C_{LEDs} is provided in Appendix C. The average switching frequency for the first stage is around 100 kHz, while the frequency for the second stage is approximately 400 kHz. The line voltage is 120 V_{ac} at 60 Hz, and the load is a 200 V LED string with current of 0.5 A.

First stage operation

Only the PFC stage is included in this test, with an additional 600 μ F bulk capacitor parallel to the LED string to limit the LED current variation. The waveforms of rectified line

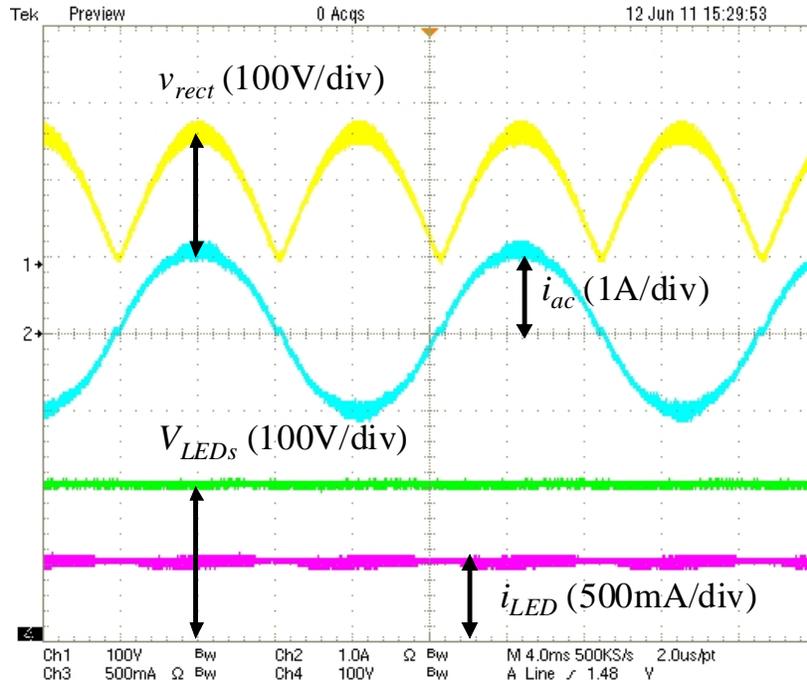


Figure 4.16: Waveforms of rectified line voltage, ac line current, LED string voltage and LED current for PFC stage experiment. Addition bulk capacitor is used to reduce LED current ripple.

voltage v_{rect} , ac input current i_{ac} , LED string voltage V_{LEDs} and LED current i_{LED} are shown in Fig. 4.16. It can be seen that ac line current is sinusoidal and in phase with the ac voltage, indicating good PF, which is measured to be 0.998. The power loss of PFC stage with 200 V 0.5 A load is measured to be approximately 3.5 W.

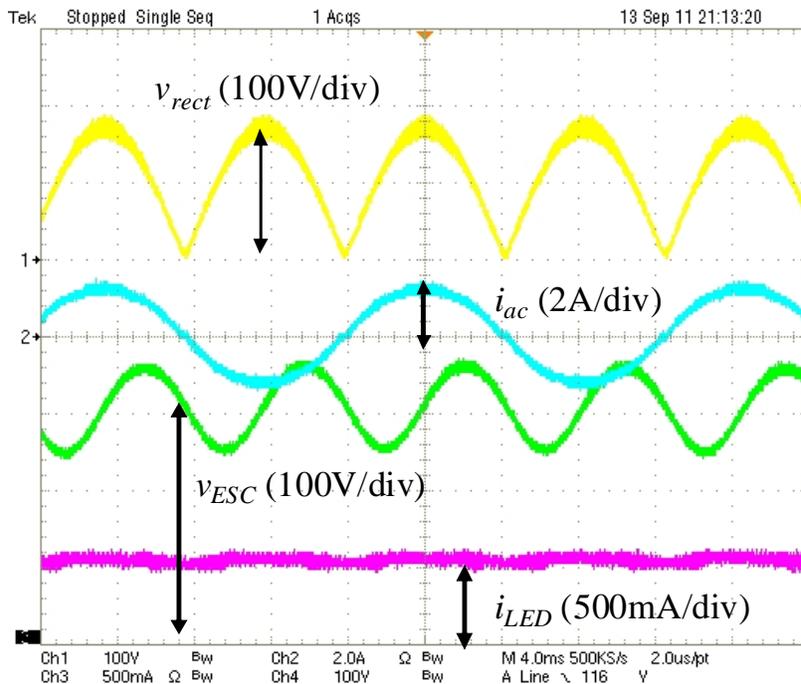
Two stage operation

A bidirectional boost second stage is then tested together with the PFC stage, while the 600 μF capacitor is removed and the energy storage is finished by C_{ES} shown in Fig. 4.15. An capacitor $C_{ES} = 8 \mu\text{F}$ is large enough for energy storage to remove the entire double-line-frequency power ripple from LED current, while limiting the capacitor voltage to less than 400 V. The waveforms for rectified line voltage v_{rect} , ac input current i_{ac} , energy-storage capacitor

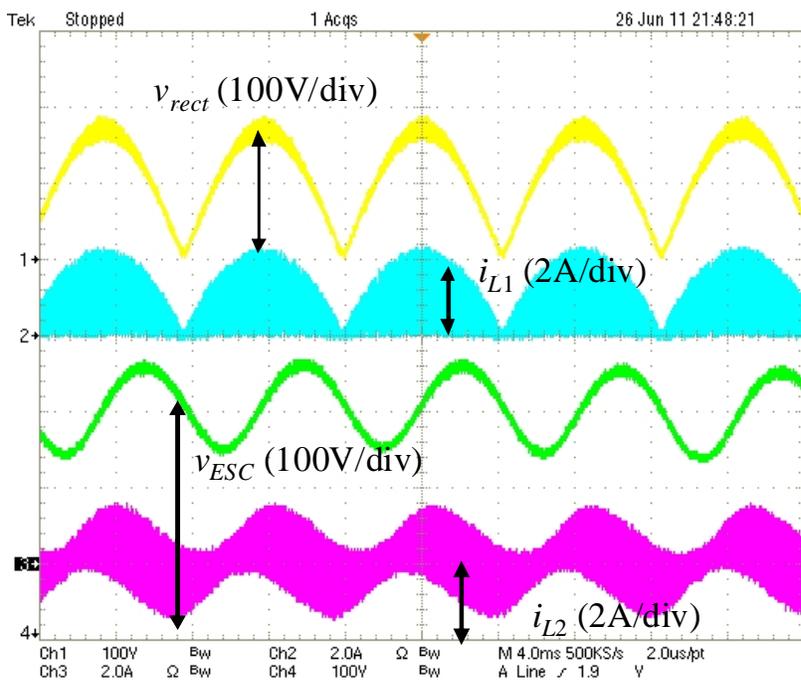
voltage v_{ESC} and LED current i_{LED} are shown in Fig. 17(a) for zero LED current ripple case, and the corresponding waveforms for inductor currents are in Fig. 17(b). The first-stage inductor current i_{L1} shows a sinusoidal envelop which is in phase with the rectified ac voltage, indicating good PF and large input power ripple. With the operation of the bidirectional second stage, there is no double-line-frequency ripple on the LED current, as the low frequency power ripple is filtered. The voltage on the energy-storage capacitor v_{ESC} increases around peak input power, as the excess power is being stored in the capacitor, and v_{ESC} decreases around zero input power, indicating energy in the capacitor is released to the LED string. Fig. 17(b) also demonstrates the inductor current for the second stage i_{L2} , whose average value is in phase with the input power. It can also be seen that i_{L2} crosses zero within every switching period, which is due to soft switching. The measured power loss is 6 W for the entire system when the output power is 100 W.

LED current ripple control

The function of ripple control is also experimentally tested, with a command of +/- 30% ripple on LED current. The corresponding waveforms are shown in Fig. 4.18, including the second-stage inductor current i_{L2} and the LED current i_{LED} . The second stage operates only when the input power is around its upper and lower values, during which intervals the LED current is regulated to either high or low reference values and v_{ESC} , the voltage on energy-storage capacitor, increases or decreases correspondingly. When the second stage stops operation, the input power is directly applied on the LED string and v_{ESC} stays unchanged. When the final duty cycle of the last regulation period is adopted as the initial duty cycle of a new regulation period, ringing occurs on LED current, as indicated in Fig. 4.18(a). Ringing can be removed, as shown in

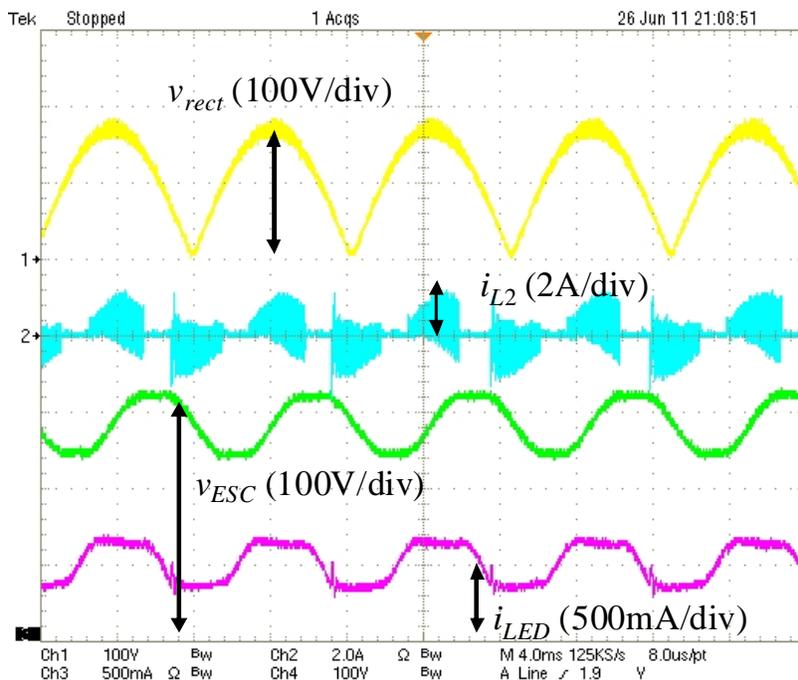


(a)

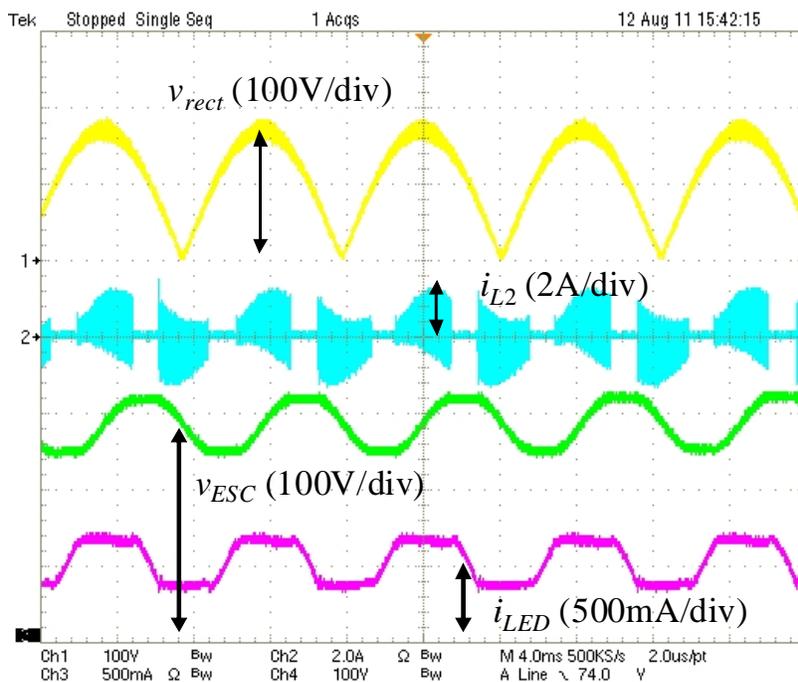


(b)

Figure 4.17: Waveforms of (a) rectified line voltage, ac line current, energy-storage capacitor voltage, LED current and (b) inductor currents for the two-stage LED driver with zero LED current ripple at double-line frequency.



(a)



(b)

Figure 4.18: Waveforms of rectified line voltage, inductor current of second stage, energy-storage capacitor voltage and LED current for the two-stage LED driver with $\pm 30\%$ LED current ripple at double-line frequency. The final duty cycle of last regulation period is directly adopted as initial duty cycle for a new regulation period in (a). The initial duty cycle is further adjusted according to LED string voltage variation in (b).

Fig. 4.18(b), when the initial duty cycle is further adjusted by Δd according to LED string voltage variation as defined in Eq. 4.12 and the additional half-time conduction period,. Compared to the waveforms in Fig. 4.17, the voltage swing of v_{ESC} in Fig. 4.18 is smaller, indicating reduction of energy storage; thus, a smaller energy-storage capacitor can be adopted by allowing larger ripple on LED current. Calculations predict a 5- μ F film capacitor would be sufficient for energy storage when 30% ripple is on the LED current, while keeping v_{ESC} at less than 400 V.

Start-up

The start-up waveforms are shown in Fig. 4.19, including rectified line voltage, ac line current, LED current and energy-storage capacitor voltage. It can be seen that the ac current increases gradually until the LED current reaches the target value during the start-up period. This soft start behavior is realized by giving the PFC stage a slow-increasing power command after power up.

Experiment with constant input current approach

Similar experiments are conducted when a constant input current is achieved for the first stage. A commercial transition-mode PFC control IC is utilized, while a constant voltage, rather than scaled input voltage, is used to shape the input current. The resulting rectified input voltage v_{rect} , ac input current i_{ac} , voltage on energy-storage capacitor v_{ESC} , LED current i_{LED} and inductor currents for the two stages i_{L1} and i_{L2} are shown in Fig. 4.20. It can be seen that the input current for the first stage is constant within each double-line-frequency period. The measured PF is approximately 0.91, which matches well with the theoretical prediction and meets the requirement by standards. Ringing occurs on ac input current i_{ac} around zero crossing of input

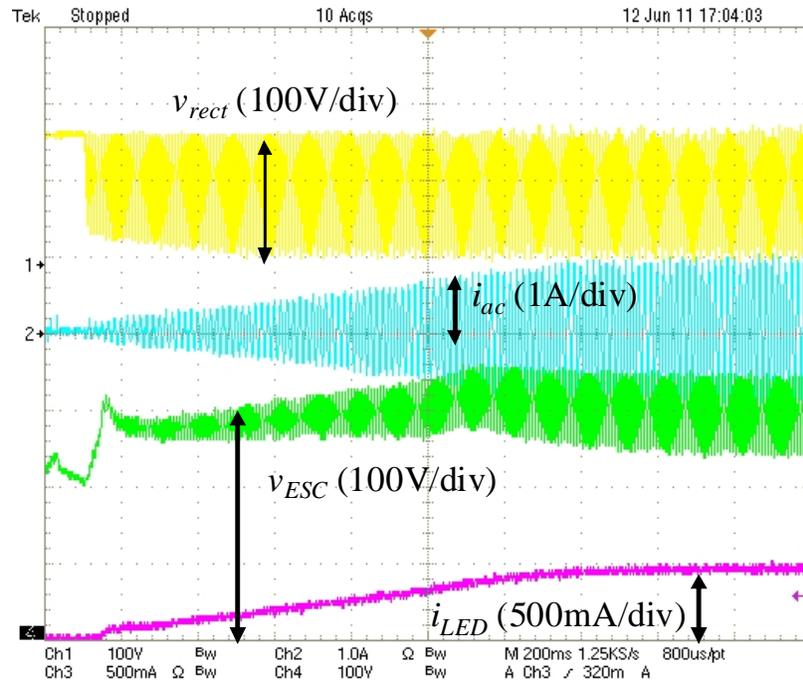
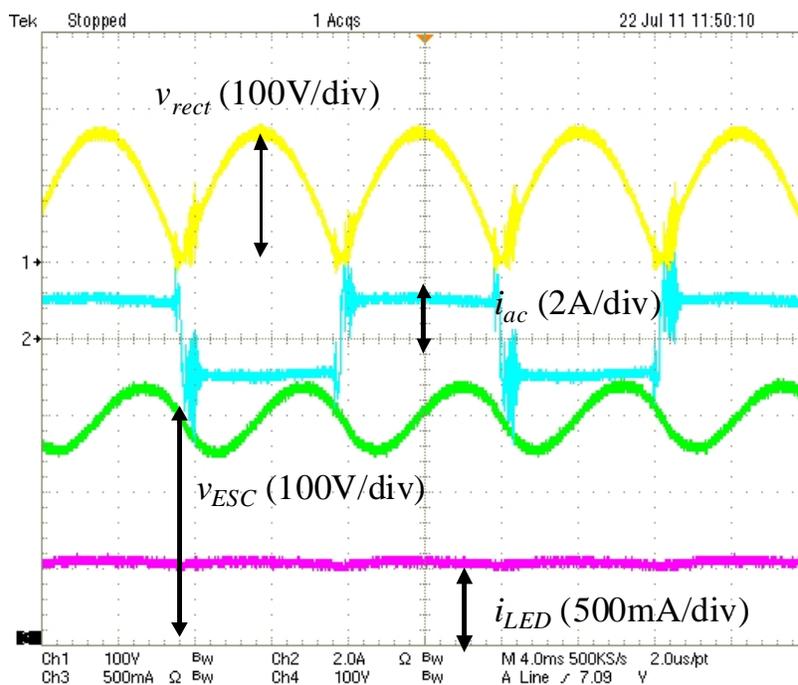


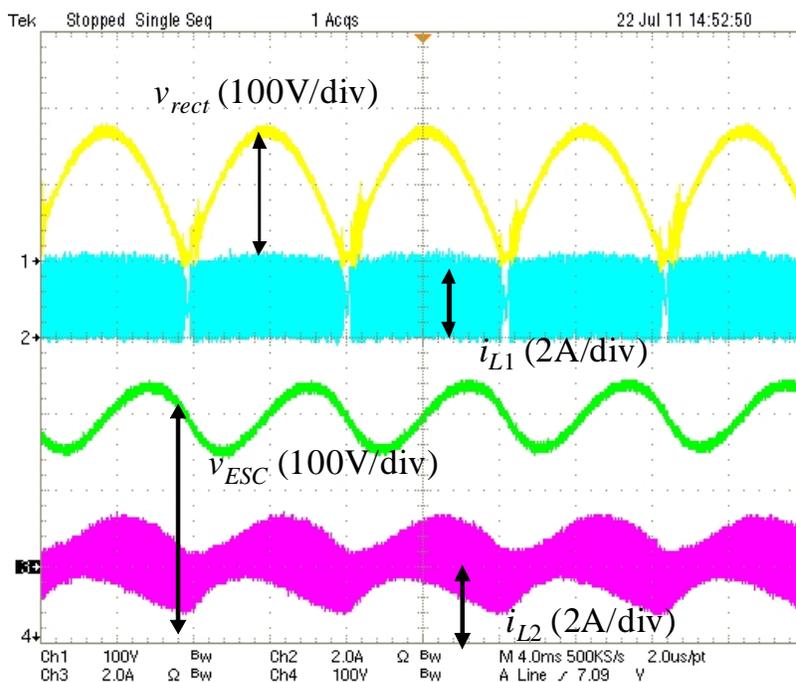
Figure 4.19: Start-up waveforms of rectified line voltage, ac line current, energy-storage capacitor voltage and LED current for the two-stage LED driver.

voltage, which is due to the sharp transition of i_{ac} and could be removed if a function of maximum on time is included in the control IC.

As shown in Fig. 4.20, with the operation of the bidirectional second stage, the double-line-frequency ripple is removed from the LED current as the ripple power goes to the energy-storage capacitor. The capacitor voltage v_{ESC} increases when input power is large and decreases when input power is small, indicating the storing and releasing of energy. Compared to the waveforms in Fig. 4.17, the variation on v_{ESC} is smaller, which is the result of reduced energy storage.



(a)



(b)

Figure 4.20: Waveforms of (a) rectified line voltage, ac line current, energy-storage capacitor voltage, LED current and (b) inductor currents for the two-stage LED driver with constant input current on the first stage and zero LED current ripple at double-line frequency.

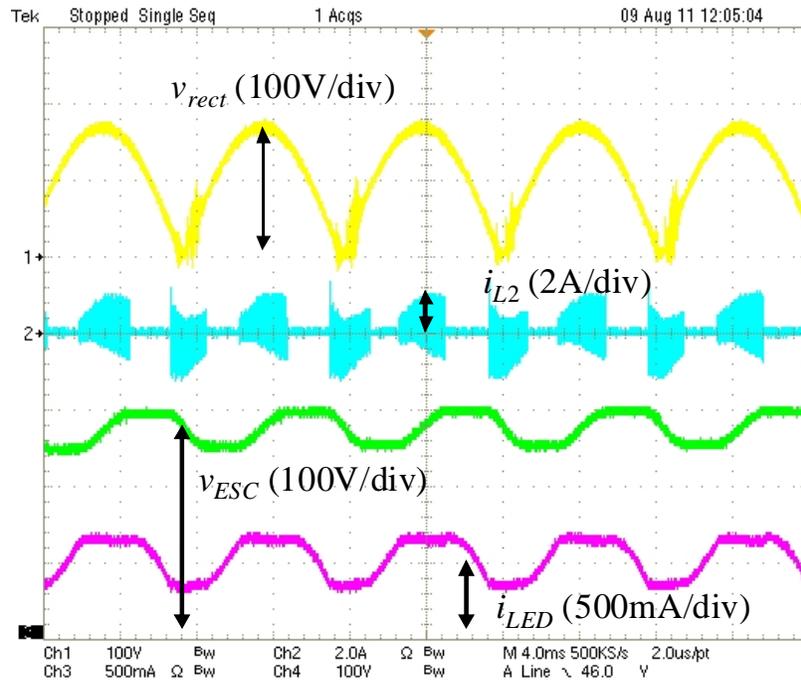


Figure 4.21: Waveforms of rectified line voltage, ac input current, energy-storage capacitor voltage and LED current for the two-stage LED driver with constant input current and $\pm 30\%$ LED current ripple at double-line frequency.

When ripple is allowed on the LED current, the reduction of energy storage is even more significant. The waveforms of rectified line voltage, ac line current, voltage on the energy-storage capacitor and LED current are shown in Fig. 4.21, with constant input current for first stage and 30% ripple on the LED current. As the variation of LED string voltage is considered to adjust the initial duty cycle of each regulation period, there is no transient ringing on the LED current. It can be seen that the swing on v_{ESC} is largely reduced, resulting in v_{ESC} less than 300 V all the time. As a result, a smaller energy-storage capacitor could be adopted. Fig. 4.22 shows the waveforms when a 2.2 μF film capacitor is used for energy storage. It can be seen that v_{ESC} is kept less than 400 V in this case.

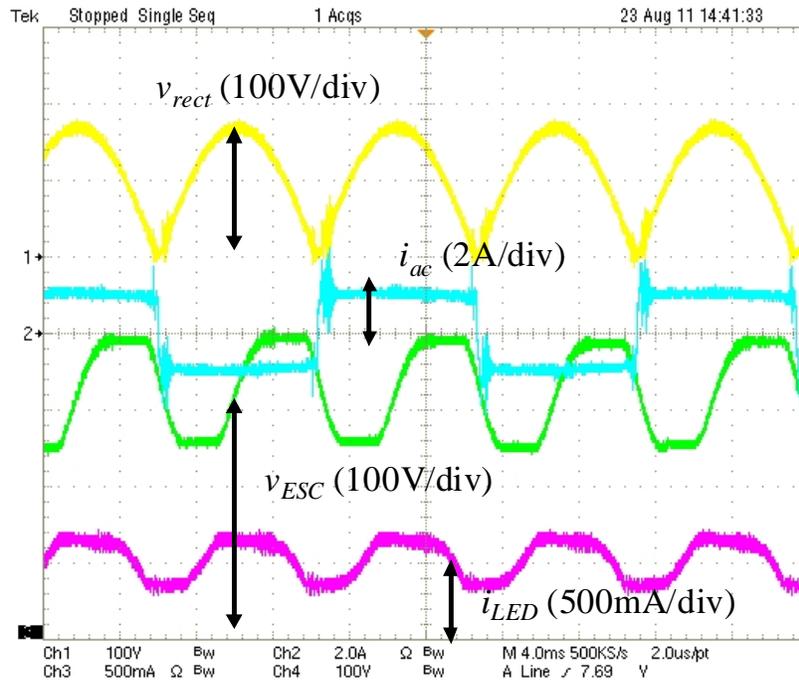


Figure 4.22: Waveforms of rectified line voltage, ac input current, energy storage capacitor voltage and LED current for the two-stage LED driver with constant input current and 30% LED current ripple at double-line frequency. A 2.2- μF film capacitor is used for energy storage.

Although the constant input current approach provides a simple solution to achieve sufficient PF and reduced energy storage, this approach leads to large ringing on ac input current. The input current, which is constant after the diode bridge, contains hard transitions from the ac side. As a result, large oscillation occurs at every transition of ac input current, as shown in Fig. 4.20 and 4.22. These oscillations can be eliminated by mitigating the ac current transition, which can be achieved by reducing input current around zero crossing of line voltage. For a transition-mode PFC controller, a scaled rectified line voltage is utilized to shape input current in order to achieve a high power factor. When a constant voltage is utilized rather than the scaled input voltage, the resulting current is constant, which can achieve $\text{PF} = 0.9$ with reduced energy

storage. In order to remove the oscillation on ac input current, the constant input current reference should be modified.

In order to achieve a modified constant input current reference, a voltage divider is utilized to generate the scaled input voltage signal for input current reference, while a Zener diode is parallel with the bottom resistor. With this configuration, the input current is clamped with a constant value when line voltage is high, and reduces around zero crossing of line voltage. Hence the shape of the input current becomes close to “trapezoidal.” The resulting waveforms are shown in Fig. 4.23. It can be seen that the oscillations in the ac line current are removed. Meanwhile, this approach also improves input PF, which is measured to be 0.96. However, the required energy storage is slightly increased as a trade-off. With the same energy-storage capacitor of 2.2 μF and 150 mA LED current ripple, in order to limit v_{ESC} below 400 V, the average LED current with trapezoidal input current approach cannot exceed 450 mA, which is slightly smaller than the 500 mA average current in Fig. 4.22.

In the method shown above, a voltage divider and a Zener diode are utilized to generate a trapezoidal input current reference, thus avoiding ac input current oscillation for the constant input current approach. The oscillation can also be removed when an ability of maximum on-time is included in the PFC controller. Hence, a controller with inductor current control ability and maximum on-time (duty cycle) is capable to implement the proposed PFC with trapezoidal input current.

A comparison of required energy-storage capacitance with various techniques is presented in Table 4.3, with the assumption of 200 V LED string at 500 mA current. The techniques considered here include constant input current approach, allowing LED current ripple and bidirectional second stage. As show in Table 4.3, the proposed techniques are able to

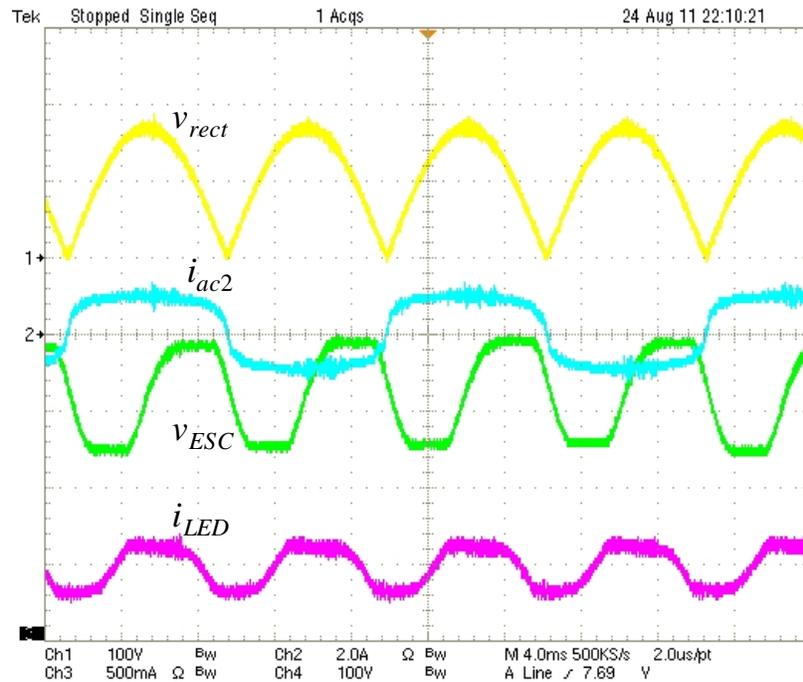


Figure 4.23: Waveforms of rectified line voltage, ac input current, energy-storage capacitor voltage and LED current for the two-stage LED driver with modified constant input current and 30% LED current ripple at double-line frequency. A 2.2- μ F film capacitor is used for energy storage.

effectively reduce required capacitance. Although the rated voltage of energy-storage capacitor increases as a trade-off, the reduction of capacitance is significant enough to limit cost increase for utilizing long-life capacitors. Compared with the cases when electrolytic capacitors are necessary, those drivers with film capacitors are expected to provide much longer life time which is compatible to LED devices.

TABLE 4.3 REQUIRED ENERGY-STORAGE CAPACITANCE WITH VARIOUS TECHNIQUES*

PF	$\frac{\Delta I_{LED}}{I_{LED}}$	2 nd Stage Requirement	C_{ES} (μ F)	Typical C_{ES} **		
				Type	V_{rated} (V)	Size (mm^3)
1	30%	No	120	Electro.	250	
0.9	30%	No	79	Electro.	250	
1	0	Yes, v_{ESC} : 250~400 V	7.4	Film	450	31.5×22×36.5
0.9	0	Yes, v_{ESC} : 250~400 V	4.5	Film	450	26.3×13.8×21.1
0.9	30%	Yes, v_{ESC} : 250~400 V	2.2	Film	450	26.33×10.6×18

* $I_{LED} = 500$ mA, $V_{LEDs} = 200$ V

**based on component information on digikey.com

4.6 Conclusion

This chapter presents several techniques to reduce energy-storage capacitance in off-line LED drivers, so as to replace the electrolytic capacitors with high-quality alternates for longer lifetime at reasonable cost. The constant input current approach reduces the required energy storage by one-third when compared to the unity-PF case, while meeting the PF requirement for lighting products. When certain ripple is allowed on LED current, the current waveform is manipulated to be trapezoidal, thus minimizing required energy storage. The required energy-storage capacitance is significantly reduced by decoupling the capacitor from LEDs with a second stage, whose power loss is limited with the bidirectional structure. All these techniques are combined and verified experimentally, with the result provided in this chapter. For a 200-V 500-mA LED string, when $PF = 1$, energy-storage capacitance is less than 8 μ F to achieve constant LED current, while the capacitor voltage is smaller than 400 V. With constant input current and 30% LED current ripple, the capacitance is further reduced to 2.2 μ F for the same system.

CHAPTER V

MODULAR AC-DC LED DRIVERS BASED ON SERIES-INPUT STRUCTURE WITH REDUCED ENERGY STORAGE

The series-input structure provides an opportunity to apply low-voltage integrated circuits (ICs) and components in high-voltage applications. With proper design, a high input voltage may distribute evenly between several modules that are serially connected from input ports. With reduced rated voltage, integration of semiconductor devices becomes much easier. Meanwhile, the low-voltage cells can operate at high switching frequencies with low-profile, light-weight inductors and capacitors. All these advantages lead to high-level monolithic integration, which matches well with the miniature LED devices.

It is of significant interest to extend the application of series-input techniques to off-line LED systems. For off-line LED applications, standards require a high power factor (PF), which normally leads to bulk electrolytic capacitors to filter input power ripple. The short-life electrolytic capacitors, although providing large capacitance at low price, place a hard limit on the overall lifetime of LED lamps. On the other hand, if the input power ripple is directly passed to LED load, the resulting large current ripple leads to problems such as flickering or degradation of LED lifetime, neither of which is desirable.

In order to avoid electrolytic capacitors in off-line LED applications while limiting the LED current ripple at the same time, several techniques can be applied to reduce required

energy-storage capacitance. The constant input current approach achieves $PF = 0.9$, which meets requirements while reducing the required energy storage by approximately one-third when compared to the case of $PF = 1$. The bidirectional second stages reduce the energy-storage capacitance by decoupling the capacitors from LEDs, and provide a possibility to limit power loss on the second stages, which process only less than one-third of the LED energy.

This chapter presents an approach to combine the series-input structure and reduction of energy-storage capacitance in off-line LED drivers. The concepts of the series-input structure and the common duty cycle approach are reviewed in Section 5.1. Section 5.2 presents the approaches to reduce energy-storage capacitance, including the constant input current approach to reduce input power ripple and the bidirectional second stages to reduce capacitance. More details on the design of system control loops are provided in Section 5.3. The experimental set-up and results are presented in Section 5.4, and Section 5.5 concludes this chapter.

5.1 Off-line LED driver based on series-input structure

Series-input structure provides an approach to reduce voltage stress on devices in high-voltage applications. The system diagram of an off-line LED driver based on series-input modules is shown in Fig. 5.1. The system is composed with several modules, which are serially connected from the input ports and share the same input filter and rectifier. Each module has an individual output port and drives a sub-string of LEDs. Although the numbers of LEDs in the modules do not have to be identical, it is good to balance the power on each module by evenly distributing the LEDs. The ideal behaviors of this system in steady state include distribution of the input (line) voltage and the regulation of all the LED currents.

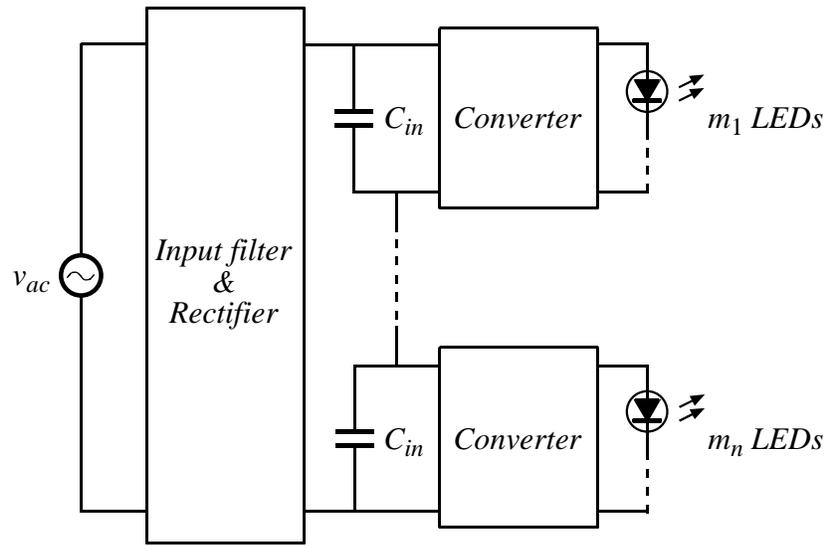


Figure 5.1: An off-line LED driver based on series-input structure.

The common duty cycle approach described in Chapter III provides a simple solution to distribute input voltage and to achieve output current copying. In steady state, a converter operating in continuous conduction mode (CCM) behaves like a “dc transformer”, whose conversion ratio is determined by the topology and duty cycle. Consequently, converters with the same topology operating in CCM with identical duty cycle have the same conversion ratio. The steady-state model of these converters in series-input configuration is provided in Fig. 5.2. With identical conversion ratios and the same input current in steady state, their output currents are naturally equal. Meanwhile, the input voltage is distributed among the modules according to the ratio of output voltages, which, in this case, are the LED sub-string voltages. As a result, only one control loop is necessary for this system, leading to a master-slave configuration. As shown in Fig. 5.2, the single master cell regulates its own LED current and generates a duty cycle. All the

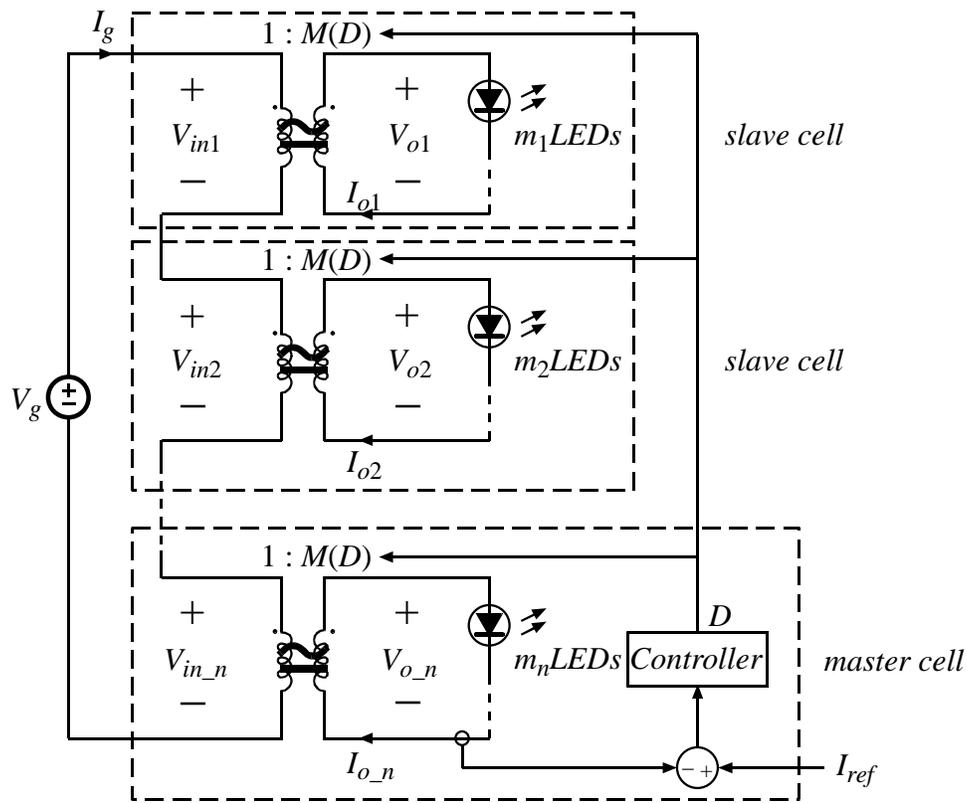


Figure 5.2: Steady-state model of modular converters with series-input configuration and common duty cycle.

slave cells adopt the same duty cycle from the master, achieving the automatic input voltage distribution and output current copying.

The common duty cycle approach can be applied to series-input structure in off-line LED drivers as well, given that certain requirements are met: they must possess the same converter topology, operation in CCM with an identical duty cycle. Although it is easy to guarantee same converter topology and an identical duty cycle, the converters may enter discontinuous conduction mode (DCM) when the input voltage is very low. This problem, however, should not disturb the input voltage distribution too much if the system is well balanced and the DCM period is short enough. Furthermore, when high PF is achieved, the input power is typically very small around

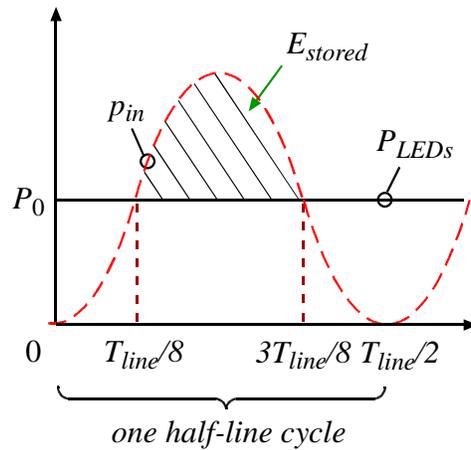
the zero crossing of input voltage, which helps reduce the disturbance due to DCM operation during this period.

5.2 Reduction of LED current ripple

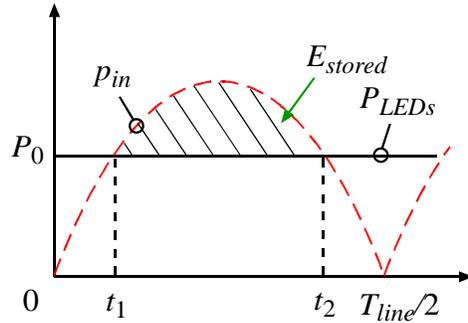
As described in Chapter IV, off-line LED applications are required to achieve high PF, which leads to large ripple on input power. Meanwhile, small ripple on LED power is preferred in order to avoid problems such as flickering or LED lifetime degradation due to thermal cycling. Hence, energy storage is necessary to filter the input power ripple, and is often realized with capacitors. In order to utilize long-life capacitors while maintaining reasonable cost, required energy-storage capacitance should be reduced. All the techniques presented in Chapter IV can be applied to series-input structure. Adjustments are necessary, however, to maintain the merit of low voltage rating for series-input modules.

5.2.1 Reducing input power ripple with the constant input current approach

As described in Chapter IV, it is possible to reduce input power ripple of off-line LED applications with the trade-off of lower PF. By regulating the input current to be constant, a PF = 0.9 is achieved, which can still meet the requirement from Energy Star program. The input and output power waveforms for PF = 1 and PF = 0.9 are shown in Fig. 5.3, in which the shadowed areas E_{stored} represent the required energy storage within each half-line cycle to achieve constant LED current. By adopting the constant input current approach, E_{stored} is reduced from 32% to 21% of total input energy.



(a)



(b)

Figure 5.3: Input and output power waveforms for (a) an LED driver with $PF = 1$ and constant LED current, and (b) an LED driver with constant input current ($PF = 0.9$) and constant LED current.

A non-inverting buck-boost converter is selected to implement the constant input current approach due to its wide range of conversion ratio. The schematic of the circuit is shown in Fig. 5.4. In order to meet the requirements for the common duty cycle approach, the inductor L_1 should be large enough to guarantee CCM operation within the major period of each half-line cycle. A sensing resistor R_{s1} converts the inductor current signal to a voltage signal. The midpoint of this signal is sampled to represent the average inductor current, which is multiplied with the duty cycle to generate input current information. A control loop is built to regulate the input

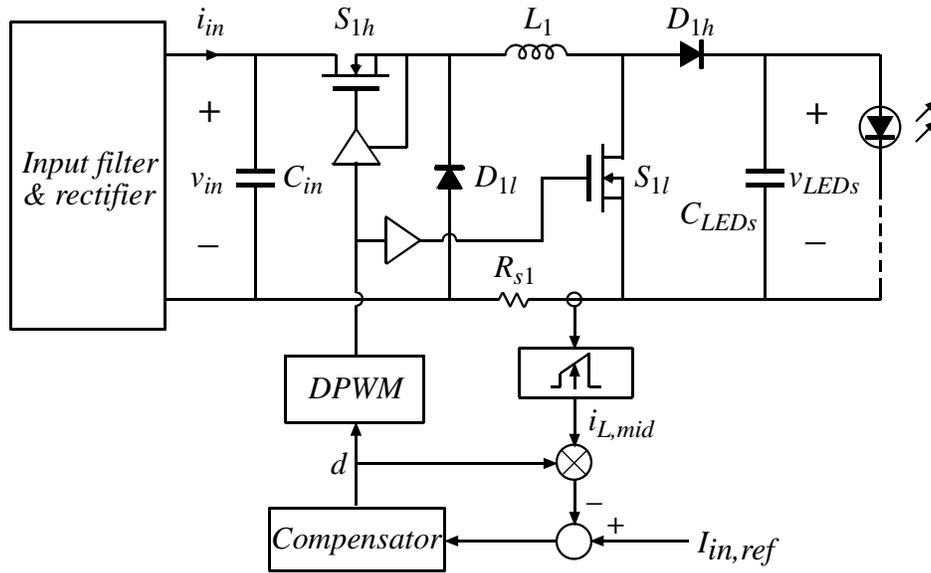


Figure 5.4: A non-inverting buck-boost converter with input current regulation.

current to a reference signal $I_{in,ref}$, which should be constant within each half-line cycle in order to achieve a PF of 0.9. With this approach, sufficient PF for LED drivers is achieved while required energy storage is reduced by one-third compared to unity-PF case. The input power is controlled by adjusting $I_{in,ref}$.

5.2.2 Reducing energy-storage capacitance with bidirectional second stages

Although the constant input current approach is capable of reducing input power ripple by a large portion, the remaining LED current ripple is still considerable. To further reduce the LED current ripple, a second stage can be adopted to make full use of energy-storage capacitance, as described in Chapter IV.

The required capacitance for energy storage can be calculated from

$$C_{ES} = \frac{2E_{stored}}{V_{ESC,peak}^2 - V_{ESC,valley}^2} = \frac{E_{stored}}{2V_{ESC}\Delta V_{ESC}}, \quad (5.1)$$

where E_{stored} is the required energy storage within one input power cycle, $V_{ESC,peak}$, $V_{ESC,valley}$, V_{ESC} and ΔV_{ESC} are the peak, valley, dc value and ripple of the energy-storage capacitor voltage, $V_{ESC,peak} = V_{ESC} + \Delta V_{ESC}$, $V_{ESC,valley} = V_{ESC} - \Delta V_{ESC}$. When the energy-storage capacitor is directly parallel with the LED string, very small ΔV_{ESC} is allowed because a small variation on LED voltage leads to a large change on its current. As a result, the required capacitance can be very large. When the capacitor is decoupled from the LED string, much larger ΔV_{ESC} is allowed, which can reduce the required capacitance significantly.

In order to limit the disturbance of second stages on the series-input system, a bidirectional structure is adopted, which keeps the LED strings at the output of PFC stages and places the energy-storage capacitor at the output of second stages, as demonstrated in Fig. 5.5. With this configuration, the common duty cycle approach is still applicable, given that the PFC stages operate in CCM for most of the time and the input voltage will still distribute according to the ratio of LED sub-string voltages. This bidirectional structure also helps limit the power loss associated with the second stages, as only the ripple power is processed by the second stages.

Although an ideal LED driver is assumed to achieve constant LED current, a small percentage ripple on LED current may not cause too much trouble. Allowing certain LED current ripple helps reduce energy storage, which is very useful when the available capacitance is limited. Under some requirements of ripple percentages, the LED current should be manipulated in a certain way to minimize the required energy storage.

The waveforms of input and output power for an LED driver with $PF = 0.9$ and LED current ripple are shown in Fig. 5.6(a), with the shadowed areas indicating the energy stored in and released from the capacitor within one half-line cycle. As the LED string voltage is almost constant, the waveform of LED current has the similar shape of LED string power p_{LEDs} , which is

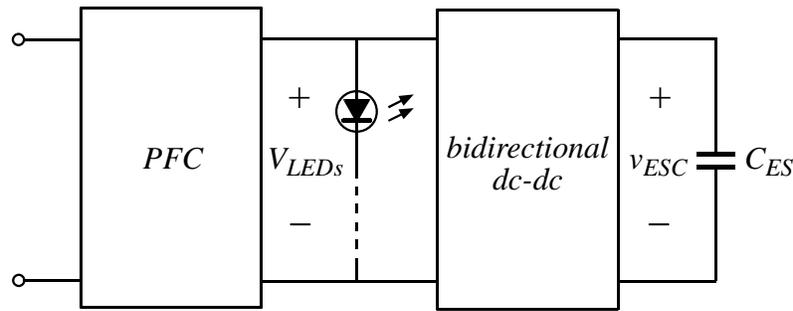


Figure 5.5: An LED driver with PFC first stage and bidirectional second stage.

close to “trapezoidal” and in phase with input power. It can be seen that the input power waveform is “chopped” only around its peak or valley, resulting in the LED string power at the regulation boundary for most of the time. In this way, the minimum energy storage is achieved for certain LED current ripple. Fig. 5.6(b) demonstrates the percentage of energy storage, E_{stored}/E_{cycle} , for different LED current ripple values, where E_{cycle} is the total input energy within one half-line cycle. The maximum required energy storage, which happens with zero LED current ripple, is approximately 21% of the total input energy. When 30% ripple is allowed on LED current, the required energy storage decreases to about 10% of the total input energy.

As the energy-storage capacitor has to be able to absorb energy from the first stage when input power is high and to supply energy back to the LED string when input power is low, the second stage has to be bidirectional. Several converters with different topologies are capable to realize this function. In order to remain low rated voltage, which is the purpose to use series-input structure, a bidirectional buck converter is selected, with the schematic shown in Fig. 5.7(a). As switching loss is not a major issue for low voltage circuits, the second stage converter is determined to operate in DCM. When the input power is larger than the required value, the excess

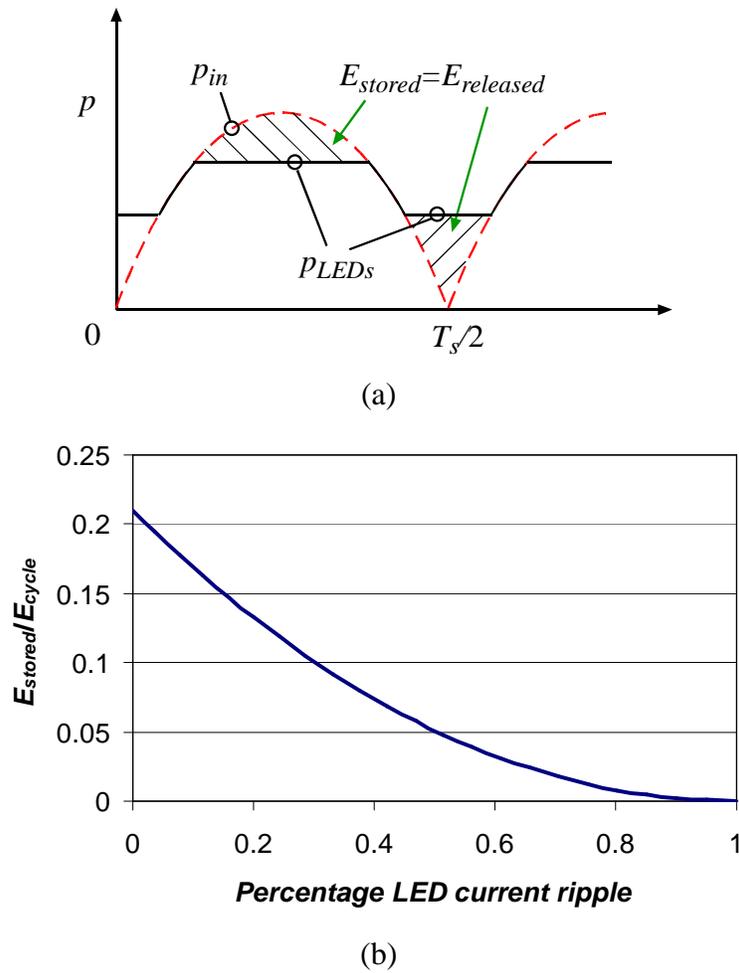


Figure 5.6: (a) Input and output power waveforms for an off-line LED driver with constant input current and trapezoidal LED current; (b) required percentage energy storage (E_{stored}/E_{cycle} , E_{cycle} is the total input energy within one half line cycle) for different LED current ripple values.

power goes through the second stage to the capacitor. As shown in Fig. 5.7(b), the low-side transistor S_{2l} is kept open, and the second stage operates as a buck converter. When the input power is less than required, the high-side transistor S_{2h} is kept open, and the second stage operates as a boost converter from a reversed direction to transfer energy from the energy-storage capacitor to the LED string, as shown in Fig. 5.7(c). The buck and boost operation modes within one half-line cycle are indicated in Fig. 5.7(d).

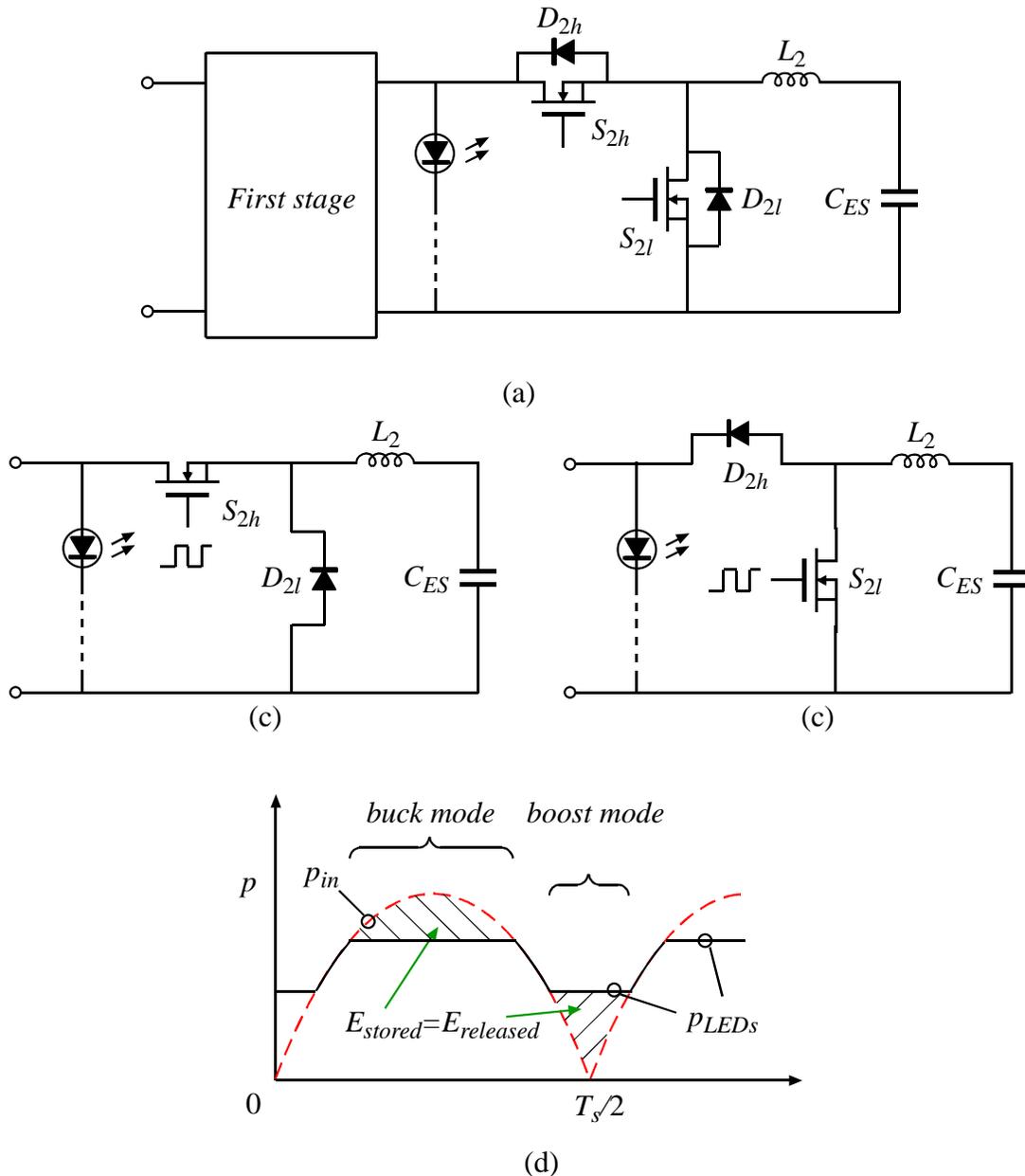


Figure 5.7: (a) A bidirectional buck converter operating in DCM as second stage; (b) buck mode; (c) reversed boost mode; (d) operation mode alternation within one half-line period.

The purpose of the bidirectional second stage is to filter the double-line-frequency power ripple. This function can be realized by regulating the LED current with the second stage. When the LED current, thus LED power, is regulated, the excess input power ripple naturally goes

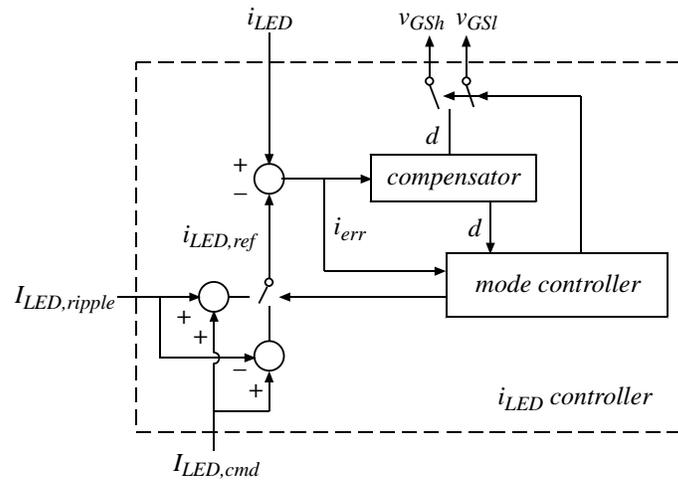


Figure 5.8: LED current controller for the bidirectional buck second stage with mode selection and ripple control.

through the second stage to the energy-storage capacitor. As the second stage operates in either buck or reverse boost mode with the potential for different LED current reference, the ability for mode selection should be included in the second stage controller, whose block diagram is shown in Fig. 5.8. The high and low references for the LED current are calculated with LED current command $I_{LED,cmd}$ and ripple command $I_{LED,ripple}$. The mode selection can be realized by detecting and analyzing LED current err i_{err} and duty cycle d , which together carry the information of instant input power level. When input power is large enough, buck mode is selected with the high LED reference signal. The duty cycle is generated for high-side transistor while low-side is off. Boost mode is applied with low LED reference signal when input power is low. High-side transistor is kept off while low-side is driven with the duty cycle v_{GSl} . The detail circuit diagram for buck and reverse boost mode are shown in Fig. 5.9.

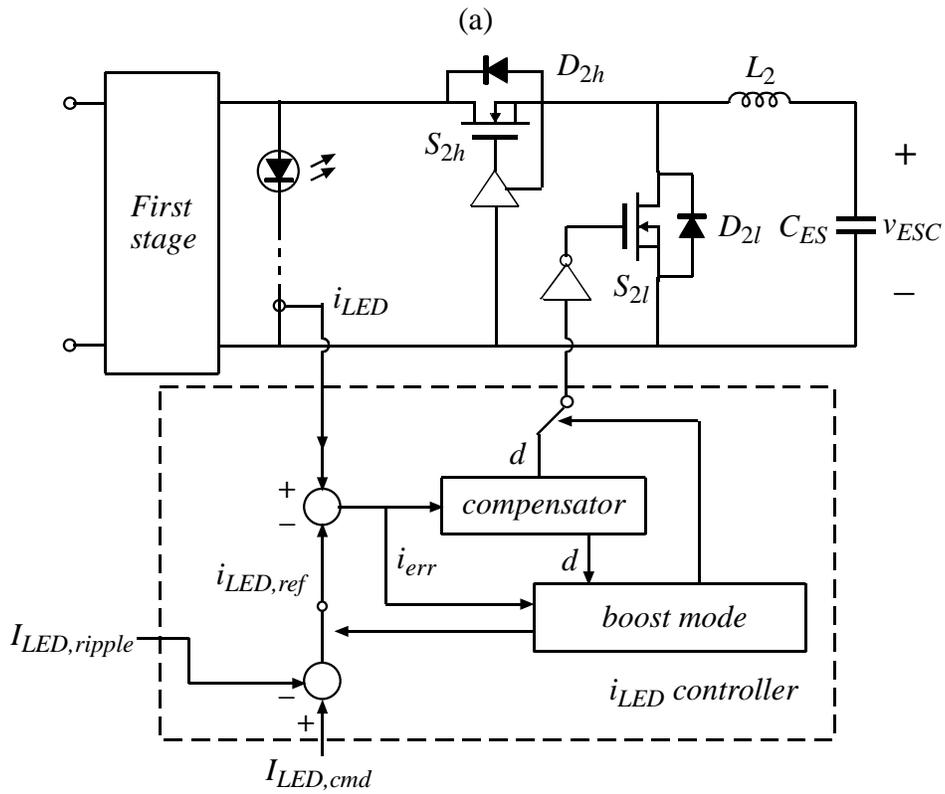
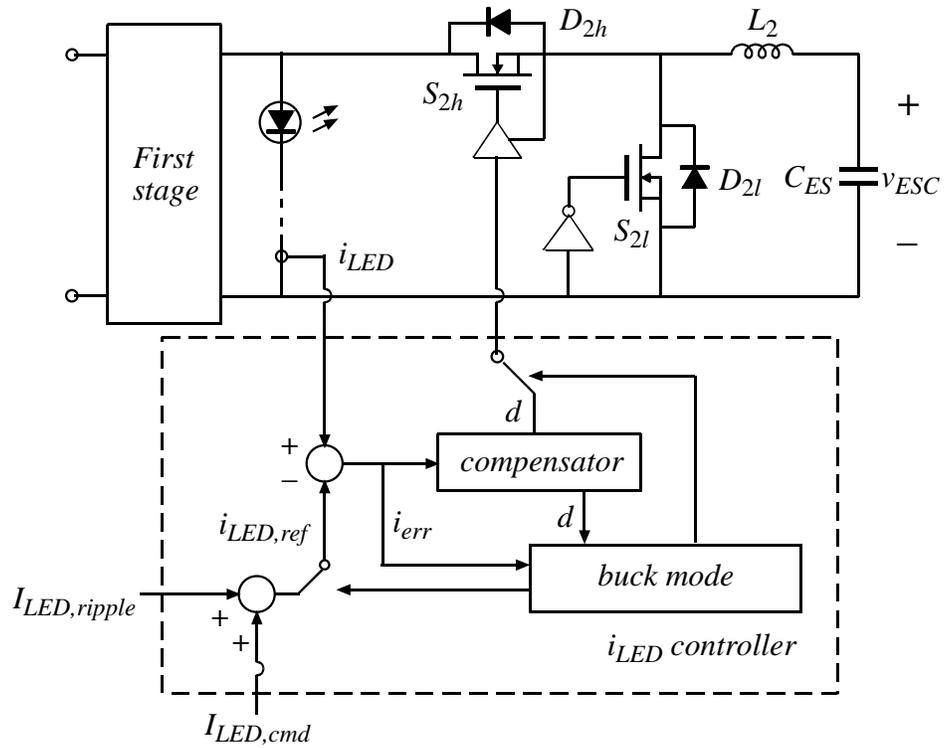


Figure 5.9: LED current control diagram: (a) buck mode and (b) boost mode. The two controllers are integrated together.

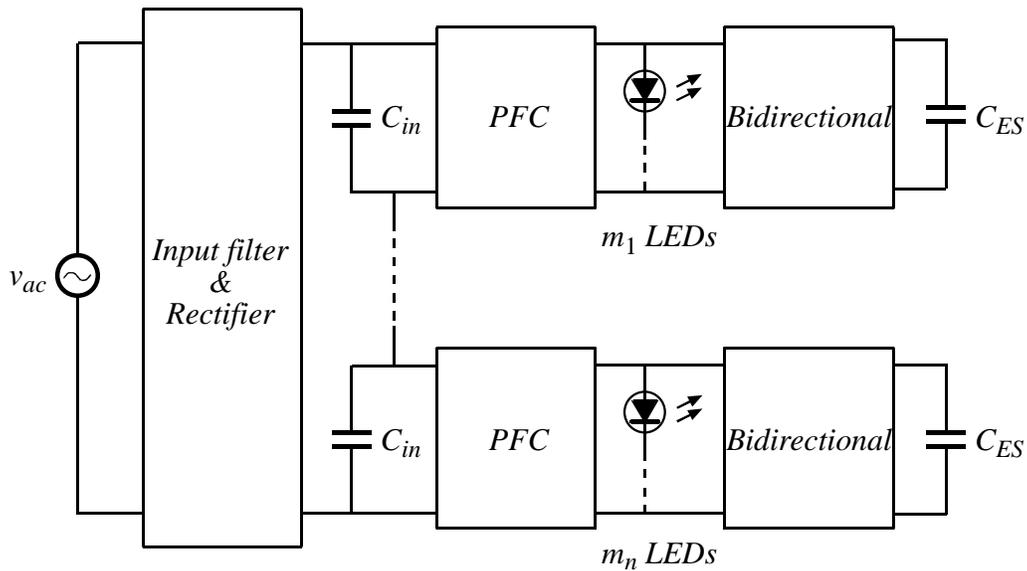


Figure 5.10: Off-line LED driver based on series-input structure built with two-stage modules.

5.3 System control loops

The system diagram of an off-line LED driver based on series-input-connected two-stage modules is shown in Fig. 5.10. The modules are serially connected from the input ports, and share the same input filter and rectifier. Each module contains two stages: a PFC first stage and a bidirectional second stage.

In order to achieve automatic input voltage distribution and LED current copying, all the PFC stages use the same duty cycle, which is generated by the single master module and then adopted by all the slave modules. Different from the common duty cycle in the PFC stages, the control loops associated with the second stages are conducted locally within each module. At least two local control loops are included in each module. One of them is to regulate the LED current, while the other is to balance the stored and released energy through the second stage, which can be realized by adjusting the average LED current to stabilize the voltage on energy-

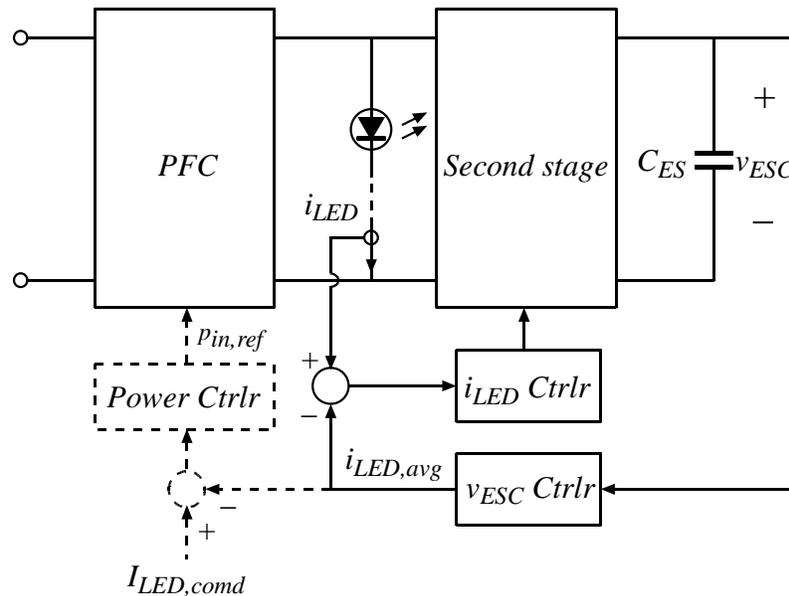
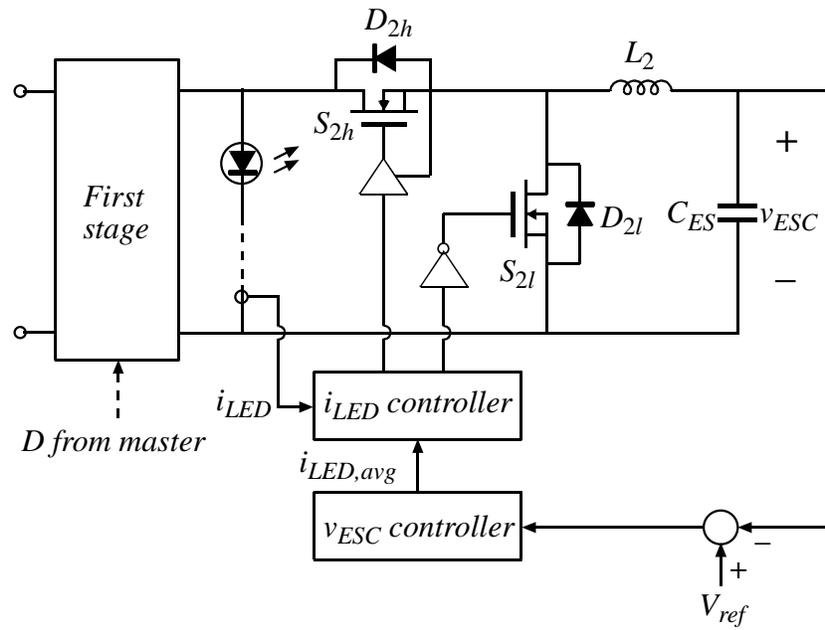


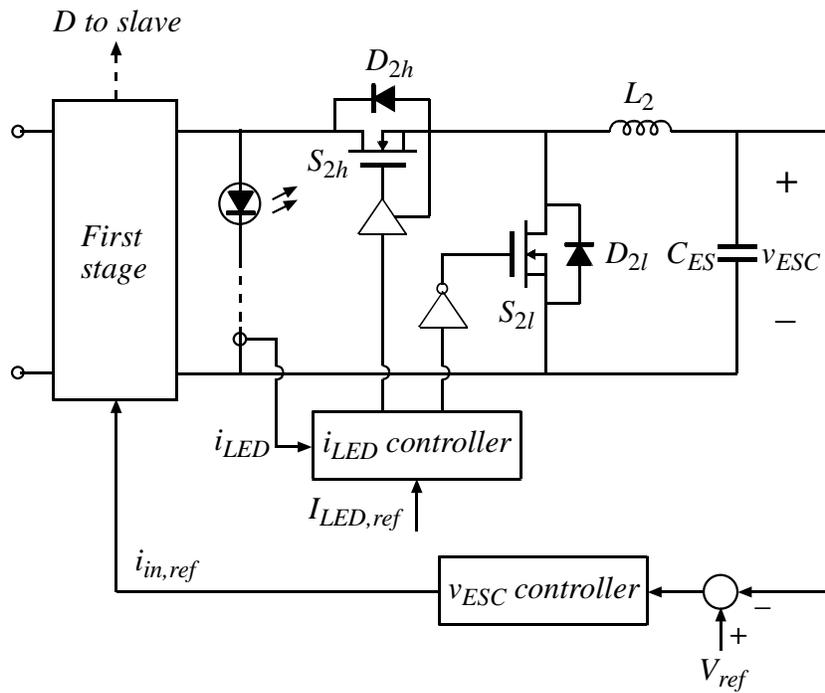
Figure 5.11: Control loops for the two-stage LED drive modules, including LED current regulation, energy-storage capacitor voltage regulation and input power control. The input power control is for master module only.

storage capacitors. One additional loop is necessary for the master module to control the average input power, which can be realized by regulating average LED current according to the external LED current command. These control loops are demonstrated in Fig. 5.11, where the dashed lines indicate the power control loop that is specific for the master module.

As indicated in Fig 5.11, four control loops are utilized for the master module, including PFC, LED current regulation, energy-storage capacitor voltage regulation and input power control. It is possible to simplify the control loops for the master module by regulating LED current with external current command directly. Meanwhile, the input power reference is generated by regulating voltage on energy-storage capacitor. The resulting control loops for slave and master modules are shown in Fig. 5.12, where three control loops are required for the master cell.

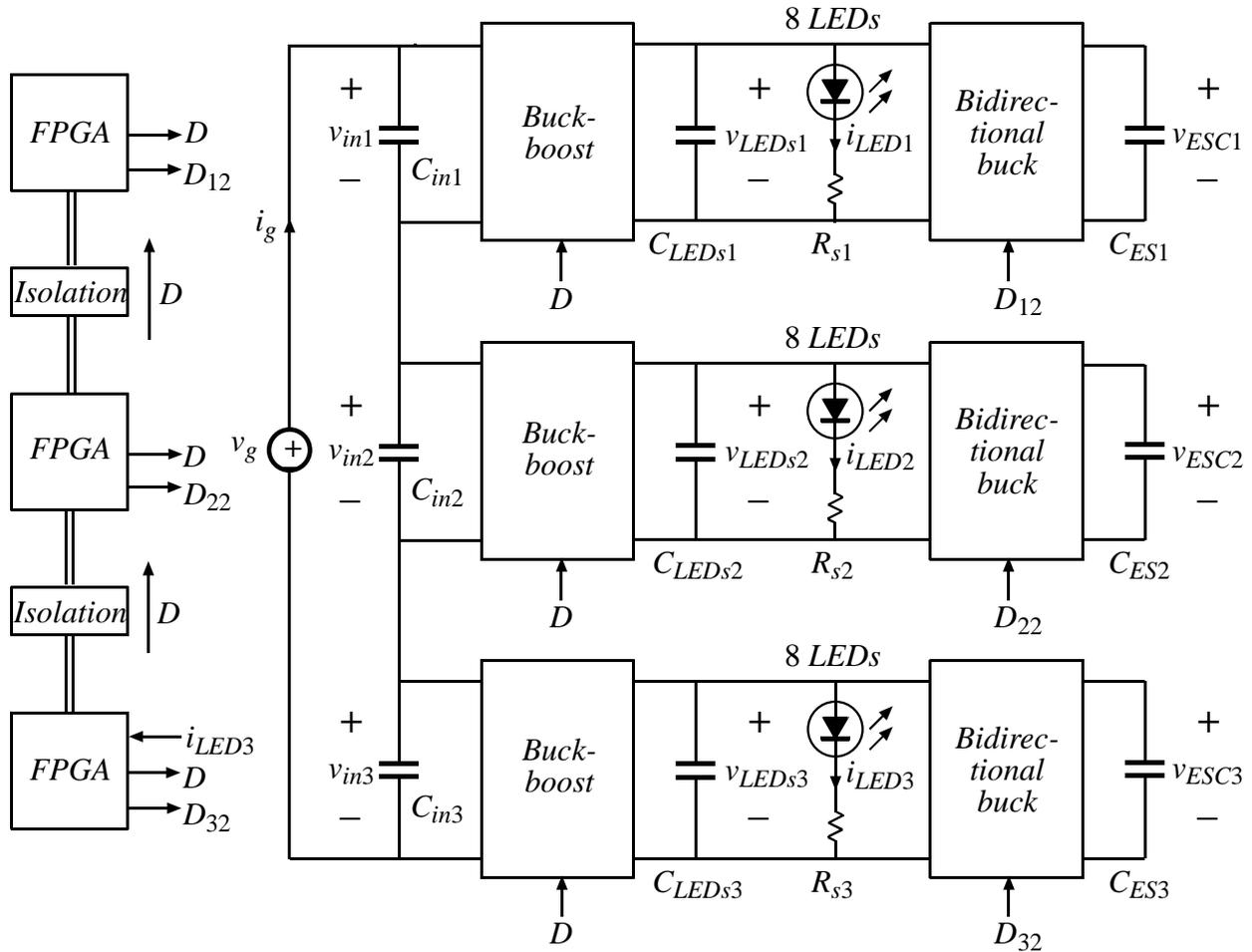


(a)

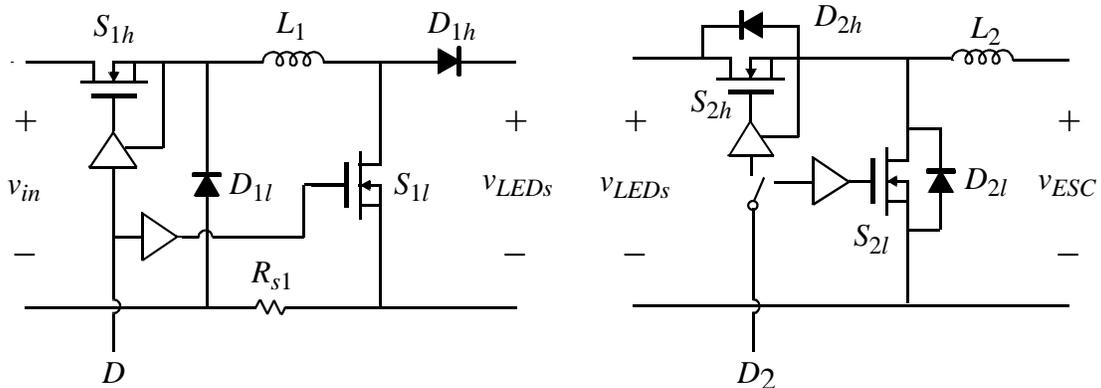


(b)

Figure 5.12: Control loops for (a) slave modules and (b) master module in a series-input modular LED driver.



(a)



(b)

(c)

Figure 5.13: (a) Experimental setup. Input voltage v_g is rectified ac input signal. FPGAs are used to control the modules and transmit duty cycle. Three modules are used, driving eight LEDs respectively. (b) Non-inverting buck-boost first stage used in experiment. (c) Bidirectional buck second stage used in experiment.

TABLE 5.1 MAJOR DEVICES USED IN EXPERIMENT

Device	Part Number	Description
FPGA	XC3S500E	Xilinx Spartan 3E
Diode	PDS540	Schottky, 40 V, 5 A
MOSFET	STN3NF06L	N channel, 60 V, 4 A
ADC	AD7825	8-bit 4-channel Multiplexed
HB Driver	LM5101	Half Bridge Driver
Isolator	ISO7221	Dual Digital Isolator 2 MSPS
LED	Luxeon K2	700 mA

TABLE 5.2 MAJOR COMPONENTS USED IN EXPERIMENT

Component	Description	Parameter
C_{in}	Input capacitor	0.47 μ F, 40 V, ceramic
L_1	First stage inductor	22 μ H
C_{LEDs}	First stage output capacitor	10 μ F, 40 V, ceramic
L_2	Second stage inductor	10 μ H
C_{ES}	Energy storage capacitor	10 μ F \times 5, 25 V, ceramic

5.4 Experimental results

A prototype was developed to verify the performance of the proposed techniques and control approach experimentally, with the schematic shown in Fig. 5.13. The circuit has separable converters and load stages to employ the modularity of the architecture. Each cell is controlled via an onboard floating FPGA and corresponding sensing circuitry and ADCs. A two-stage structure, with four-switch non-inverting buck-boost first stage and a bidirectional buck second stage, was implemented for the experiments. The major devices used are shown as Table 5.1, and the component values are shown in Table 5.2. The first stages operate in CCM while the second stages are in DCM. The switching frequency is approximately 780 kHz for all converters. Three cells were used for the experiment, with eight LEDs as load for each.

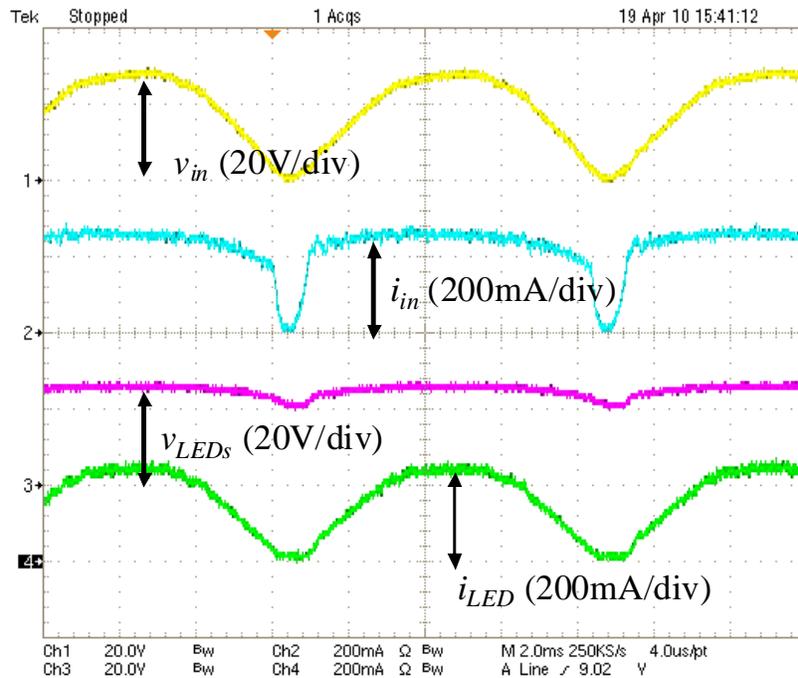


Figure 5.14: Input voltage, input current, LED string voltage and LED current of a buck-boost first stage with constant input current regulation.

Constant Input Current Regulation

The first experiment is to test the constant input current regulation. A single buck-boost first stage with constant-input-current regulation, as shown in Fig. 5.4, is used in the experiment. The waveforms of the rectified input voltage v_{in} , input current i_{in} , output voltage v_{LEDs} and LED current i_{LED} are shown in Fig. 5.14. The input current is regulated to 250 mA over the majority of the ac line cycle, and reaches zero when the input voltage goes to zero and the duty cycle saturates. The measured power factor of this circuit is between 0.93 and 0.95 when the input voltage is between 20 Vac and 40 Vac, and the average current of an 8-LED string is between 100 mA and 300 mA. The efficiency of this circuit is measured at approximately 85%.

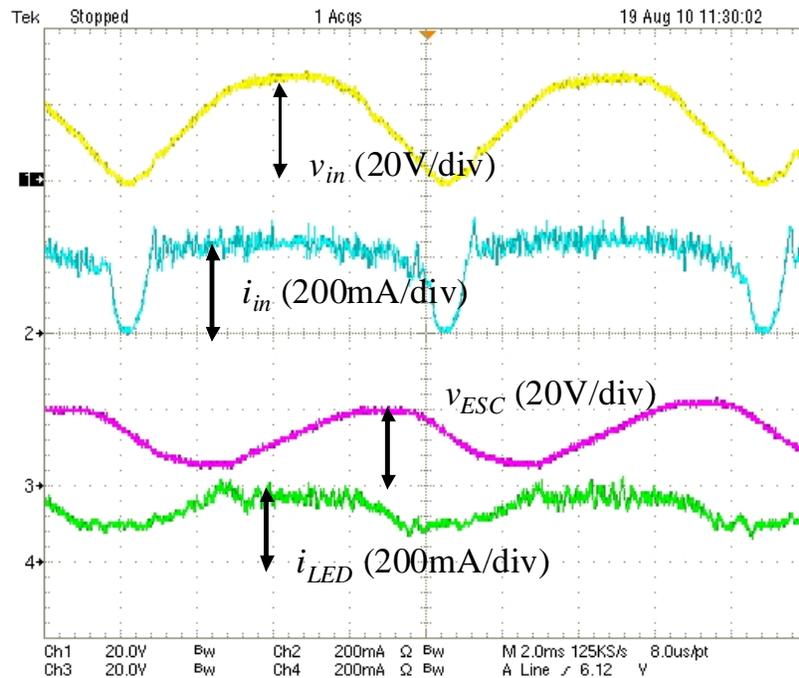


Figure 5.15: Input voltage, input current, voltage on energy-storage capacitor and LED current of an LED driver with 0.9 PF first stage and bidirectional second stage. The LED current is set to be 150 ± 50 mA.

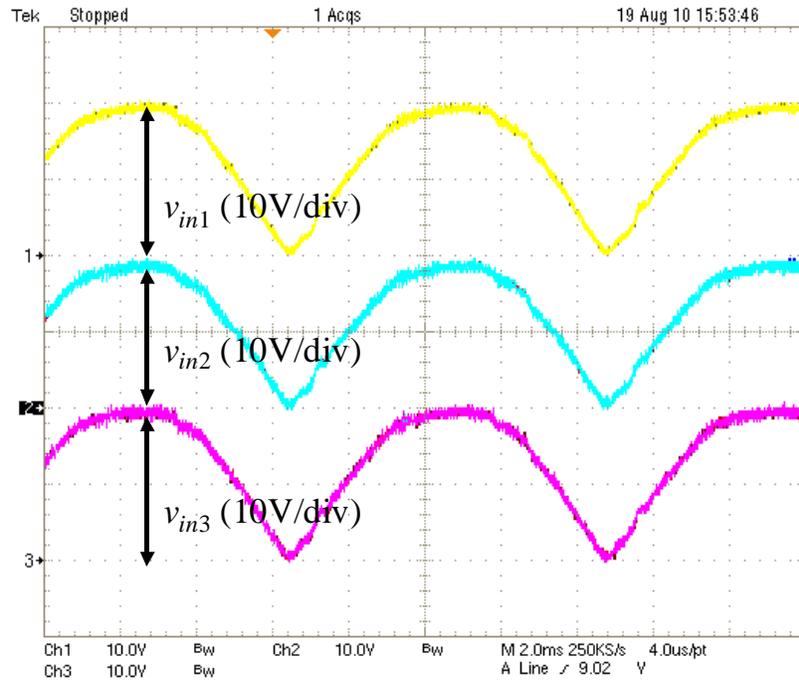
Two-stage LED Driver with 0.9 PF First Stage and Bidirectional Second Stage

An LED drive module with a constant-input-current first stage and bidirectional buck second stage is tested in the second experiment. A selection of the experimental results is given here. The experimental results use a module that drives 8 LEDs at 150 ± 50 mA current, with first stage output capacitor $C_{LEDs} = 10 \mu\text{F}$ and energy-storage capacitor $C_{ES} = 50 \mu\text{F}$. Waveforms of rectified input voltage v_{in} , energy-storage capacitor voltage v_{ESC} and the LED current i_{LED} are shown in Fig. 5.15, demonstrating reduced 120-Hz LED current ripple compared to single stage case. For comparison, a ten times higher capacitance (approximately $500 \mu\text{F}$) is necessary to achieve the same LED current ripple reduction without the second stage, in which case

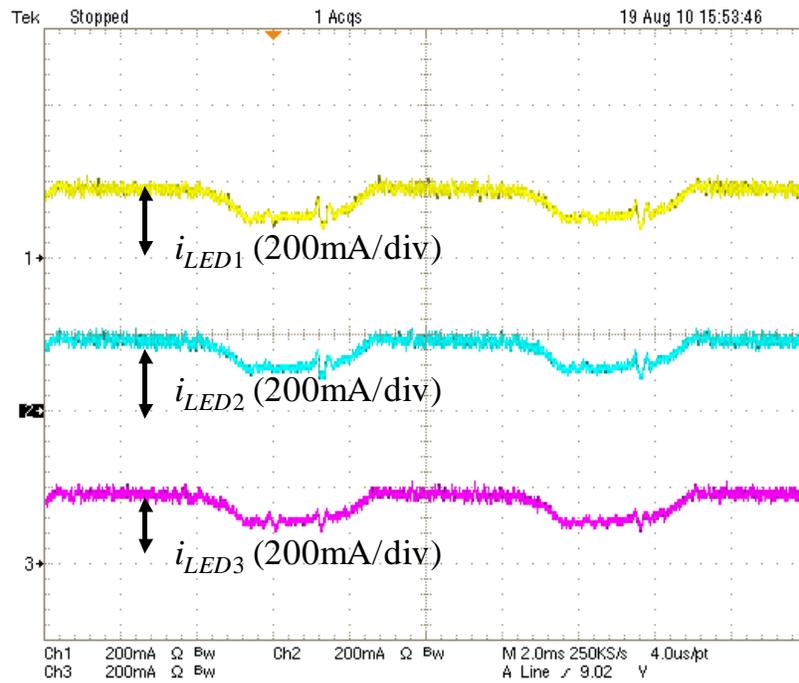
electrolytic capacitors are the only practical choice. The required energy-storage capacitance would increase to 760 μF when the single-stage driver achieves $\text{PF} = 1$. The efficiency of this two-stage driver is measured at approximately 80%. With an overall efficiency of 80%, first stage efficiency of 85% and 10% energy processed by the second stage, the efficiency for second stage is calculated to be about 77%. When a traditional cascaded two-stage structure is used, the second stage efficiency has to be 94% to achieve the same overall efficiency when the first stage remains the same.

Series-input Connected Modules with Second Stages

A series-input system with three modules was implemented in this experiment. The master module utilizes the simplified feedback loop in Fig. 5.12(b) to regulate LED current and generate first-stage duty cycle. The slave modules use the duty cycle from the master for the first stage, and adopt the self-balance method in Fig. 5.12(a) to regulate their own energy-storage capacitor voltage and LED current. The target LED current is 150 ± 50 mA. The input voltages and LED currents of the three modules are shown in Fig. 5.16. The three input voltages are roughly identical, demonstrating input voltage distribution, as shown in Fig. 5.16(a). The three LED currents are also identical with reduced double-line-frequency ripple, demonstrating output current copying, as shown in Fig. 5.16(b). The efficiency of the series-input system is approximately 80%.



(a)



(b)

Figure 5.16: (a) Input voltages and (b) LED currents of the series-input LED driver built with two-stage LED drive modules. The LED current is set to be 150 ± 50 mA.

5.5 Conclusion

An approach to combine the series-input structure and the techniques to reduce energy storage is presented in this chapter. An off-line LED driver is built with several two-stage LED drive modules which are serially connected from input ports. For each module, LEDs are connected to the output of PFC first stage, followed by a bidirectional second stage with an energy-storage capacitor. The common duty cycle approach is applied on the first stages to achieve automatic input voltage distribution and LED current copying. The constant input current approach achieves $PF = 0.9$ with small input power ripple, while the bidirectional second stages reduce required energy-storage capacitance without disturbing the input voltage distribution. With the required energy-storage capacitance significantly reduced, the LED current ripple is reduced without using bulk electrolytic capacitors.

CHAPTER VI

CONCLUSION

Two major topics are included in this thesis. The first one is to reduce the size or thickness of LED drivers, so as to take advantage of the small form factor of LED devices and to offer flexibility for diverse applications. The series-input modular structure with the common duty cycle approach provides a relatively easy method to achieve this target, by reducing voltage stress on the components. With smaller rated voltage, integration of semiconductor devices becomes much easier while converters can operate with low-profile and light-weight components, both of which lead to high-level integration. Another major target is to achieve long lifetimes for off-line LED drivers, mainly by eliminating short-life electrolytic capacitors. In order to utilize long-life but expensive capacitors, the required capacitance should be reduced to limit cost increase. Several techniques are addressed in this thesis to minimize required energy-storage capacitance, while limiting additional cost, power loss and control effort.

All of these principles and control approaches are verified experimentally, with the results provided in this thesis.

The next section summarizes the contributions of these work followed by potential future research directions.

6.1 Contributions

(1) Development of the common duty cycle approach for series-input modular systems

The common duty cycle approach can significantly simplify the design of series-input modular systems. The advantage of series-input system is reduced voltage stress on each module. The resulted circuit can operate at a high frequency with small-sized and light-weight components even in high-voltage applications, leading to high-level integration and flexibility for diverse applications. With the common duty cycle approach, input voltage distribution and output current copying can be automatically achieved in a series-input system, and the control-to-output transfer function is very close to that of a single converter, and is therefore easy for system design and compensation. Detail analyses with small-signal model are provided, which are also verified with simulation and experiment.

(2) Development of the response procedure to LED open-circuit failure for series-input modular systems

When a number of LEDs are series-connected in a long string, the entire string will be off when a single LED fails and becomes an open circuit. To deal with this risk, series-input structure provides an approach by shorting the input port of the module with open-circuited LED, so as to keep other LEDs in operation. With this approach, the effect of LED open-circuit failure on system efficiency is mitigated. In order to keep the controller of the “failed” module in operation so as to short its input port and provide a communication channel, the controller is powered from the output capacitor, which is charged by occasional pulses of power injection. A response procedure is designed and verified to deal with LED open-circuit failure and implement occasional power injections.

(3) Development of the constant input current approach to achieve $PF = 0.9$ with reduced energy storage

In order to replace electrolytic capacitors with high-quality capacitors while limiting cost increase for off-line LED applications, the required energy-storage capacitance should be reduced. As LED products are allowed to have PF less than unity, it is possible to reduce energy storage with the trade-off of lower PF. The constant input current approach provides a simple solution to reduce required energy storage by one-third compared to the case of $PF = 1$, while achieving $PF = 0.9$ which meets the PF requirement on lighting products. Converters achieving constant input current, one in CRM (Chap. IV), another in CCM (Chap. V), are presented in this thesis.

(4) Development of bidirectional second stages to reduce energy-storage capacitance

When an energy-storage capacitor is directly parallel with an LED string, very large capacitance is required due to the limited capacitor voltage variation. With a second stage to decouple the capacitor from the LEDs, large variations and high dc value are allowed on the capacitor voltage, leading to significant reduction of required capacitance. Furthermore, the special bidirectional structure helps limit power loss, as less than one-third of the LED energy is processed by the second stage. Bidirectional second stages are also utilized in off-line LED driver based on series-input structure, without any disturbance on the common duty cycle approach. The corresponding design and control approaches are presented in Chap. IV and Chap. V.

(5) Development of the trapezoidal LED current ripple control approach

The required energy storage is reduced when ripple is allowed on LED current. With certain percentage of ripple, the energy storage is minimized when LED power is in phase with input power. This can be achieved with relatively small effort by implementing a trapezoidal LED current waveform. With this approach, the LED current is regulated to either high or low reference according to input power level, and input power is directly applied on LEDs between regulation periods. The transitions of control modes are determined according to voltage on the energy-storage capacitor and LED current. Proper initial duty cycles are generated to avoid ringing at the beginning of each regulation period.

6.2 Future research directions

(1) Trapezoidal input current approach to meet both PF and THD requirements while reducing energy storage

As described in Chapter IV, with sinusoidal input current in phase with ac line voltage, $PF = 1$ is achieved, while E_{stored} , the energy to be stored and released in order to achieve constant output power, is 32% of total input energy. With constant input current, the achieved $PF = 0.9$ meets ENERGY STAR requirement, while E_{stored} is reduced to 21% of total input energy, which helps the reduction of capacitance. However, this constant input current approach cannot meet harmonics requirement on lighting products with power greater than 25 W, which is defined by IEC 61000-3-2 [44], as shown in Table 6.1.

In order to meet the requirements on both PF and THD, while reducing the E_{stored} , the advantages of sinusoidal and constant input current should be combined, which leads to a “trapezoidal” input current approach. With this trapezoidal i_{in} approach, the input current follows

TABLE 6.1 HARMONICS, PF AND ENERGY STORAGE FOR CONSTANT AND TRAPEZOIDAL INPUT CURRENT

Harmonics [n]	Maximum harmonic currents limit * [% of fund] (by IEC 61000-3-2)	Constant i_{in} [% of fund]	Trapezoidal i_{in} ** [% of fund]
2	2	0	0
3	30×PF	33.3	26.4
5	10	20	9.1
7	7	14.3	1.6
9	5	11.1	1.5
11≤n≤39	3	100/n	≤1.9
	Power factor (PF)	0.9	0.96
	Percentage E_{stored}	0.21	0.23

* for lighting products with power greater than 25 W

** for the case of i_{in} clamped when $v_{in} \geq 0.4 \times V_{in_peak}$

sinusoidal envelop $i_{in,env}$ at low input voltage, and is clamped to a constant value I_{clamp} when input voltage is high, as shown in Fig. 6.1, where $I_{in,peak}$ is the peak value of $i_{in,env}$. In general, as the clamp value I_{clamp} gets closer to $I_{in,peak}$ (or clamp period t_2-t_1 decreases), a higher PF and a larger E_{stored} result, while THD is reduced. The threshold to meet THD requirements is $I_{clamp} \geq 0.4 \times I_{in,peak}$ (same as the case if i_{in} is clamped when $v_{in} \geq 0.4 \times V_{in,peak}$ when $i_{in,env}$ is scaled line voltage v_{in}), which results in 74% clamp time within each half-line period ($t_2-t_1 \leq 74\% \times T_{line}/2$). The corresponding percentage harmonic currents are shown in the fourth column of Table 6.1. It can be seen that all the harmonic currents are under the limits placed by IEC 61000-3-2, while a PF = 0.96 is achieved with 23% of total input energy to be filtered.

This trapezoidal input current approach provides an opportunity to meet the PF and THD requirements, while reducing required energy storage at the same time compared to the unity PF case. The key point is to select a proper clamp threshold for input current. One option is to generate a specific trapezoidal envelop for input current, which can be a scaled input voltage clamped at a certain level. In order to make this method a general solution for universal input

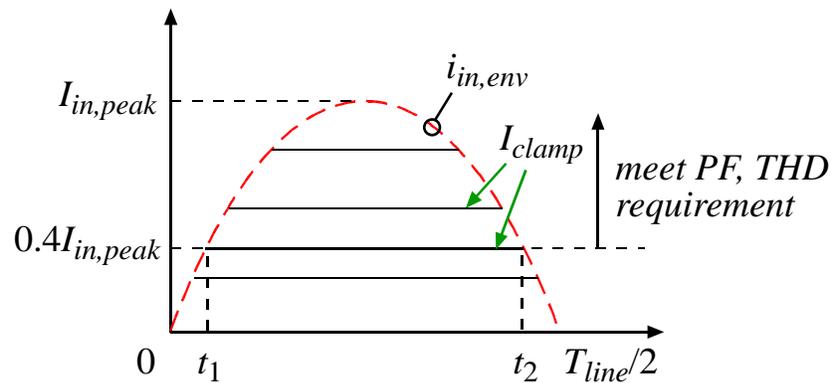


Figure 6.1: Trapezoidal input current.

voltages, the clamp voltage should be variable according to peak input voltage, which might require additional circuitry, such as peak detecting blocks and voltage dividers. Additional research is necessary to find a simple solution to implement this trapezoidal input current approach.

(2) Application of energy storage reduction techniques to flyback converters

The flyback converter is a popular choice for industrial applications, due to its simplicity to achieve isolation and wide conversion ratio. Hence, it is of practical interest to apply the constant or trapezoidal input current approach on flyback converters to reduce required energy storage. However, for flyback converters, a constant input current is much more difficult to achieve, primarily due to the discontinuity of input current. Analysis is necessary to find a simple solution for reduction of energy storage in a flyback converter.

(3) Critical conduction mode (CRM) operation of the bidirectional second stages

When a bidirectional second stage is utilized to reduce energy-storage capacitance, the capacitor voltage might be boosted high, which potentially increase switching loss. In order to avoid high switching loss, soft switching techniques can be adopted, as discussed in Chap. IV. However, the resultant large current ripple increases conduction loss, which might be an issue for high-power applications. Operation in CRM might be a good compromise between conduction and switching loss; however, additional research is required to apply this technique to bidirectional second stages.

(4) Individual output current control in series-input modular systems

Within a system with multiple LEDs, it is possible that different drive currents are required, for instance, for LEDs with different colors. A common approach is to connect the LEDs in several strings according to their types, and then control the currents string by string. These LED strings might be paralleled and powered by a single converter in order to reduce cost. With this configuration, individual current control can be realized by approaches like independent regulators in series with each string. As LEDs of different types require various forward voltages, the single converter normally generate the output voltage for the string with highest voltage. As a result, large voltage drop might result on the regulators in other strings, leading to a considerable power loss.

The series-input structure can be applied in this situation to reduce power loss, with each module powering an LED sub-string. Since different currents are required for the sub-strings, these modules should no longer utilize a common duty cycle, but various values according to necessary conversion ratios. In order to maintain system stability, a master-slave configuration may still be feasible, which means a master cell has the authority to increase or decrease the duty

cycle of all of the modules. Meanwhile, the slave cells will be able to adjust their own duty cycles with a slower speed. Future research is necessary to investigate system stability and control approach for this configuration.

BIBLIOGRAPHY

- [1] "U.S. lighting market characterization, volume I: national lighting inventory and energy consumption estimate," [on line]. Available: <http://www.ssl.energy.gov/>
- [2] "U.S. lighting market characterization, volume II: energy efficient lighting technology options," [on line]. Available: <http://www.ssl.energy.gov/>
- [3] "ENERGY STAR program requirements for solid state lighting luminaires," [on line]. Available: <http://www.energystar.gov/>
- [4] "Solid-state lighting research and development: manufacturing roadmap," [on line]. Available: <http://www.ssl.energy.gov/>
- [5] R. Erickson and D. Maksimovic, Fundamentals of Power Electronics, Second Edition, Springer, (ISBN 0-7923-7270-0), 2001.
- [6] Datasheet: IR1155S, "Programmable frequency, one cycle control PFC IC," International Rectifier, [Online]. Available: <http://www.irf.com>
- [7] Datasheet: UCC28019A, "8-pin continuous conduction mode (CCM) PFC controller," Texas Instruments, [Online]. Available: <http://www.ti.com>
- [8] R. Zane, and D. Maksimovic, "Nonlinear-carrier control for high-power-factor rectifier based on up-down switching converters," IEEE Transactions on Power Electronics, vol. 13, no. 2, Mar. 1998, pp. 213-221.
- [9] B. Mather, B. Ramachandran, and D. Maksimovic, "A digital PFC controller without input voltage sensing," in Proc. IEEE Applied Power Electronics Conference, Anaheim, CA, Feb. 2007, pp. 198-204.
- [10] L. Han, and N. Narendren, "Developing an accelerated life test method for LED drivers," in Proc. Ninth International Conference on Solid State Lighting, Aug. 2009.
- [11] W. Chen, and S. Hui, "Elimination of electrolytic capacitor in an AC/DC light-emitting diode (LED) driver with high input power factor and constant output current," IEEE Transactions on Power Electronics, no. 99, pp. 1, May 2011.
- [12] J. Patterson, and R. Zane, "Series input modular architecture for driving multiple LEDs," in Proc. Power Electronics Specialist Conference, Rhodes, Greece, June 2008, pp. 2650-2656.
- [13] L. Gu, X. Ruan, M. Xu, and K. Yao, "Means of eliminating electrolytic capacitor in AC/DC power supplies for LED lightings," IEEE Transactions on Power Electronics, vol. 24, no. 5, pp. 1399-1408, May 2009.
- [14] B. Wang, X. Ruan, K. Yao, and M. Xu, "A method of reducing the peak-to-average ratio of LED current for electrolytic capacitor-less AC-DC drivers," IEEE Transactions on Power Electronics, vol. 25, no. 3, pp. 592-601, Mar. 2010.

- [15] D. G. Lamar, J. Sebastián, M. Arias and A. Fernández, "Reduction of the output capacitor in power factor correctors by distorting the line input current," in Proc. IEEE Applied Power Electronics Conference and Exposition, Palm Springs, Feb. 2010, pp. 196-202.
- [16] J. Shao, "Single stage offline LED driver," in Proc. IEEE Applied Power Electronics Conference and Exposition, Washington, DC, Feb. 2009, pp. 582-586.
- [17] B. Zhang, X. Yang, M. Xu, Q. Chen and Z. Wang, "Design of boost-flyback single-stage PFC converter for LED power supply without electrolytic capacitor for energy-storage," in Proc. IEEE International Power Electronics and Motion Control Conference, Wuhan, China, May 2009, pp. 1668-1671.
- [18] K. Yao, M. Xu, X. Ruan and L. Gu, "Boost-flyback single-stage PFC converter with large DC bus voltage ripple," in Proc. IEEE Applied Power Electronics Conference and Exposition, Washington, DC, Feb. 2009, pp.1867-1871.
- [19] J. Garcia, A. J. Calleja, E. L. Corominas, D. Cacio, and J. Ribas, "Electronic driver without electrolytic capacitor for dimming high brightness LEDs," in Proc. IEEE Industrial Electronics Conference, Nov. 2009, pp. 3518-3523.
- [20] D. Gacio, J. M. Alonso, A. J. Calleja, J. Garcia, and M. Rico-Secades, "A universal-input single-stage high-power-factor power supply for HB-LEDs based on integrated buck-flyback converter," IEEE Transactions on Industrial Electronics, vol. 58, no. 2, pp. 589-599, Feb. 2011.
- [21] J. M. Alonso, J. Vina, D.G. Vaquero, G. Martinez, and R. Ssorio, "Analysis and design of the integrated double buck-boost converter as a high-power-factor driver for power-LED lamps," IEEE Transactions on Industrial Electronics, vol. 59, no. 4, pp. 1689-1697, Apr. 2012.
- [22] P. T. Krein, and R. S. Balog, "Cost-effective hundred-year life for single-phase inverters and rectifiers in solar and LED lighting applications based on minimum capacitance requirements and a ripple power port," in Proc. IEEE Applied Power Electronics Conference and Exposition, Washington, DC, Feb. 2009, pp. 620-625.
- [23] S. Y. R. Hui, S. N. Li, X. H. Tao, W. Chen and W. M. Ng, "A novel passive off-line light-emitting diode driver with long lifetime," in Proc. IEEE Applied Power Electronics Conference and Exposition, Palm Springs, CA, Feb. 2010, pp. 594-600.
- [24] Y. X. Qin, H. S. H. Chung, D. Y. Lin and S. Y. R. Hui, "Current source ballast for high power lighting emitting diodes without electrolytic capacitor," in Proc. IEEE Industrial Electronics Conference, Nov. 2008, pp. 1968-1973.
- [25] C. Chen, C. Wu, Y. Chen, and T. Wu, "Sequential color LED backlight driving system for LCD panels," IEEE Transactions on Power Electronic, vol. 22, no. 3, May 2007, pp. 919-925.
- [26] M. Doshi, and R. Zane, "Digital architecture for driving large LED arrays with dynamic bus voltage regulation and phase shifted PWM," in Proc. IEEE Applied Power Electronics Conference and Exposition, May 2007, pp. 287-293.
- [27] K. Hwu, Y. Yau, and L. Lee, "Powering LED using high-efficiency SR flyback converter," in Proc. IEEE Applied Power Electronics Conference and Exposition, Washington, DC, Feb. 2009, pp. 563-569.
- [28] Y. Hu, and M. M. Javanovic, "LED driver with self-adaptive drive voltage," IEEE Transactions on Power Electronics, vol. 23, no. 6, Nov. 2008, pp. 3116-3125.

- [29] Datasheet: TLC5940, "16 Channel LED Driver w/DOT Correction & Grayscale PWM Control," Texas Instruments, [Online]. Available: <http://focus.ti.com/>
- [30] Datasheet: HV9910, "HV9910 Universal High Brightness LED Driver," Supertex, [Online]. Available: www.supertex.com/
- [31] A. Bhinge, N. Mohan, R. Giri and R. Ayyanar, "Series-parallel connection of dc-dc converter modules with active sharing of input voltage and load currents," in Proc. Applied Power Electronics Conference and Exposition, Aug. 2002, pp. 648-653.
- [32] R. Ayyanar, R. Giri, and N. Mohan, "Active input-voltage and load-current sharing in input-series and output-parallel connected modular DC-DC converters using dynamic input-voltage reference scheme," IEEE Transactions on Power Electronics, vol. 19, no. 6, Nov. 2004, pp. 1462-1473.
- [33] J. W. Kim, J. S. Yon, and B. H. Cho, "Modeling, control, and design of input-series-output-parallel-connected converter for high-speed-train power system," IEEE Transactions on Industrial Electronics, vol. 48, no. 3, Jun. 2001, pp. 536-544.
- [34] K. Siri, M. Willhoff, C. Truong and K. Conner, "Uniform voltage distribution control for series connected dc-dc converters," IEEE Transactions on Power Electronics, vol. 22, no. 4, July 2007, pp. 1269-1279.
- [35] X. Ruan, L. Chen, and T. Zhang, "Control strategy for input-series output-parallel converter," in Proc. Power Electronics Specialist Conference, June 2006, pp. 1-8.
- [36] R. Giri, V. Choudhary, R. Ayyanar, and N. Mohan, "Common-duty-ratio control of input-series connected modular DC-DC converters with active input voltage and load-current sharing," IEEE Transactions on Industrial Applications, vol. 42, no. 4, July/Aug. 2006, pp. 1101-1111.
- [37] V. Choudhary, E. Ledezma, R. Ayyanar, and R. M. Button, "Fault tolerant circuit topology and control method for input-series and output-parallel modular DC-DC converters," IEEE Transactions on Power Electronics, vol. 23, no. 1, Jan. 2008, pp. 402-411.
- [38] P. T. Krein, and J. W. Kimball, "Series-parallel approaches and clamp methods for extreme dynamic response with advanced digital loads," in Proc. IEEE Workshops on Computers in Power Electronics, Aug. 2004, pp. 85-88.
- [39] J. W. Kimball, J. T. Mossoba, and P. T. Krein, "Control technique for series input-parallel output converter topologies," in Proc. Power Electronics Specialist Conference, June 2005, pp. 1441-1445.
- [40] J. W. Kimball, J. T. Mossoba, and P. T. Krein, "A stabilizing, high-performance controller for input series-output parallel converters," IEEE Transactions on Power Electronics, vol. 23, no. 3, May 2008, pp. 1416-1427.
- [41] "A review of the literature on light flicker: ergonomics, biological attributes, potential health effects, and methods in which some LED lighting may introduce flicker," [on line]. Available: <http://grouper.ieee.org/groups/1789/>
- [42] O. Trescases and W. T. Ng, "Variable output, soft-switching DC/DC converter for VLSI dynamic voltage scaling power supply applications," in Proc. IEEE Power Electronics Specialists Conference, Aachen, Germany, 2004, pp. 4149-4155.
- [43] T. Takayama and D. Maksimovic, "A power stage optimization method for monolithic DC-DC converters," in Proc. IEEE Power Electronics Specialists Conference, Jeju, South Korea, June 2006, pp. 1-7.

- [44] IEC61000-3-2: Limits for harmonic current emissions.
- [45] I. Oh, "A single-stage power converter for a large screen LCD back-lighting," in Proc. IEEE Applied Power Electronics Conference and Exposition, Dallas, TX, Mar. 2006, pp. 1058-1063.
- [46] C. Y. Hsu, and H. Y. Wu, "A new single-phase active power filter with reduced energy-storage capacity," IEE Proc. Electric Power Applications, vol. 143, no. 1, pp. 25-30, Jan. 1996.
- [47] K. Zhou, J. Zhang, S. Yuvarajan, and D. Weng, "Quasi-active power factor correction circuit for HB LED driver," IEEE Transactions on Power Electronics, vol. 23, no. 3, pp. 1410-1415, May 2008.
- [48] R. Wang, F. Wang, D. Boroyevich and P. Ning, "A high power density single phase PWM rectifier with active ripple energy storage," in Proc. IEEE Applied Power Electronics Conference and Exposition, Palm Springs, CA, Feb. 2010, pp. 1378-1383.
- [49] C. Hsieh, C Yang, and K. chen, "A charge-recycling buck-store and boost-restore (BSBR) technique with dual outputs for RGB LED bucklight and flashing Module," IEEE Transactions on Power Electronics, vol. 24, pp. 1914-1924, Aug. 2009.
- [50] M. R. Krames, O. B. Shchekin, R. Mueller-Mach, G. O. Mueller, L. Zhou, G. Harbers, and M. G. Craford, "Status and future of high-power light-emitting diodes for solid-state lighting," Journal of Display Technology, vol. 3, no. 2, pp. 160-175, Jun. 2007.
- [51] M. S. Shur and R. Zukauskas, "Solid-state lighting: toward superior illumination," Proceedings of the IEEE, vol. 93, no. 10, pp. 1691-1703, Oct. 2005.
- [52] K. Loo, W. Lun, S. Tan, Y. Lai, and C. Tse, "On driving techniques for LEDs: toward a generalized methodology," IEEE Transactions on Power Electronics, vol. 24, no. 12, pp. 2967-2976, Dec. 2009.
- [53] C. K. Tse, M. H. L. Chow, and M. K. H. Cheung, "A family of PFC voltage regulator configurations with reduced redundant power processing," IEEE Transactions on Power Electronics, vol. 16, no. 6, pp. 794-802, Nov. 2001.
- [54] C. Qiao, and K. M. Smedley, "A topology survey of single-stage power factor corrector with a boost type input-current-shaper," IEEE Transactions on Power Electronics, vol. 16, no. 3, pp. 360-368, May 2001.
- [55] M. Krames, O. Shchekin, R. Mueller-Mach, G. Mueller, L. Zhou, G. Harbers, and M. Craford, "Status and future of high-power light-emitting diodes for solid-state lighting," Journal of Display Technology, vol. 3, pp. 160-175, June 2007.
- [56] S. Hui, and Y. Qin, "A general photo-electro-thermal theory for light emitting diode (LED) systems," in Proc. IEEE Applied Power Electronics Conference and Exposition, Washinton, DC, Feb. 2009, pp. 554-562.
- [57] A. C. Kyritsis, N. P. Papanikolaou, E. C. Tatakis, "A novel parallel active filter for current pulsation smoothing on single stage grid-connected AC-PV modules," in Proc. European Conference on Power Electronics and Applications, Aalborg, Denmark, Sep. 2007, pp. 1-10.
- [58] M. Ryu, J. Baek, J. Kim, S. Park, and H. Kim, "Electrolytic capacitor-less, non-isolated PFC converter for high-voltage LEDs driver," in Proc. International Conference on Power Electronics, Shilla Jeju, Korea, May 2011, pp. 499-506.

- [59] X. Qu, S. Wong, and C. K. Tse, "Noncascading structure for electronic ballast design for multiple LED lamps with independent brightness control," IEEE Transactions on Power Electronics, vol. 25, no. 2, pp. 331-340, Feb. 2010.
- [60] M. Albach, T. Durbaum, and A. Brockmeyer, "Calculating core losses in transformer for arbitrary magnetizing currents a comparison of different approaches," in Proc. IEEE Power Electronics Specialists Conference, 1996, pp. 1463-1468.
- [61] A. Van den Bossche, V. C. Valchev, and G. B. Georgiev, "Measurement and loss model of ferrites with non-sinusoidal waveforms," in Proc. IEEE Power Electronics Specialists Conference, Aachen, Germany, 2004, pp. 4814-4818.
- [62] "Capacitors age and capacitors have an end of life," [Online]. Available: <http://www.emersonnetworkpower-partner.com/>
- [63] M. Doshi, and R. Zane, "Control of solid-state lamps using a multiphase pulsewidth modulation technique," IEEE Transactions on Power Electronics, vol. 25, no. 7, pp. 1894-1904, Jul. 2010.
- [64] P. T. Krein, "Current quality and performance tradeoffs under active power factor correction," in Proc. IEEE Workshop on Computers in Power Electronics, 2004, pp. 97-101.
- [65] G. M. Buiatti, S. M. A. Cruz, and A. J. M. Cardoso, "Lifetime of film capacitors in single-phase regenerative induction motor drives," in Proc. IEEE International Symposium on Diagnostics for Electric Machines, Power Electronics and Drives, 2007, pp. 356-362.
- [66] K. Yao, X. Ruan, X. Mao, and Z. Ye, "Variable-duty-cycle control to achieve high input power factor for DCM boost PFC converter," IEEE Transactions on Industrial Electronics, vol. 58, no. 5, May 2011, pp. 1856-1865.
- [67] M. H. L. Chow, K. W. Siu, C. K. Tse, and T. Lee, "A novel method for elimination of line-current harmonics in single-stage PFC switching regulators," IEEE Transactions on Power Electronics, vol. 13, no. 1, pp.75-83, Jan. 1998.
- [68] B. Singh, K. Al-Haddad, and A. Chandra, "A universal active power filter for single-phase reactive power and harmonic compensation," in Proc. Power Quality, Hyderabad India, June 1998, pp. 81-87.
- [69] T. Shimizu, Y. Jin, and G. Kimura, "DC ripple current reduction on a single-phase PWM voltage-source rectifier," IEEE Transactions on Industry Applications, vol. 36, no. 5, pp. 1419-1429, Sep./Oct. 2000.
- [70] Z. Pan, F. Z. Peng, and S. Wang, "Power factor correcting using a series active filter," IEEE Transactions on Power Electronics, vol. 20, no. 1, pp. 148-153, 2005.
- [71] K. Siri, and M. Willhoff, "Independently-sourced series-input connected converters with uniform current-sharing," in Proc. IEEE Aerospace Conference, 2008, pp. 1-11.
- [72] J. Kim, J. You, and B. H. Cho, "Modeling, control and design of input-series-output-parallel-connected converter for high-speed-train power system," IEEE Transactions on Industrial Electronics, vol. 48, no. 3, pp. 536-544, Jun. 2001.
- [73] V. Vorperian, "Synthesis of medium voltage dc-to-dc converters from low-voltage, high-frequency PWM switching converters," IEEE Transactions on Power Electronics, vol. 22, no. 5, pp. 1619-1635, Sep. 2007.
- [74] O. Garcia, J. A. Cobos, R. Prieto, P. Alou, and J. Uceda, "Power factor correction: a survey," in Proc. IEEE Power Electronics Specialists Conference, 2001, pp. 8-13.

- [75] N. Narendran, L. Deng, R. M. Pysar, Y. Gu and H. Yu, "Performance characteristics of high-power light-emitting diodes," in Proc. International Conference on Solid State Lighting, 2004, pp. 267-275.
- [76] T. Jin, K. Zhang, K. Zhang, and K. Smedley, "A new interleaved series input parallel output (ISIPO) forward converter with inherent demagnetizing features," IEEE Transactions on Power Electronics, vol. 23, no. 2, pp. 888-895, Mar. 2008.
- [77] Q. Hu, and R. Zane, "LED drive circuit with series input connected converter cells operating in continuous conduction mode," in Proc. IEEE Applied Power Electronics Conference and Exposition, Washington, DC, Feb.2009, pp. 1511-1517.
- [78] Q. Hu, and R. Zane, "A 0.9 PF LED driver with small LED current ripple based on series-input digitally-controlled converter modules," in Proc. IEEE Applied Power Electronics Conference and Exposition, Palm Springs, CA, Feb. 2010, pp. 2314-2320.
- [79] Q. Hu, and R. Zane, "LED driver circuit with series-input-connected converter cells operating in continuous conduction mode," IEEE Transactions on Power Electronics, vol. 25, no.3, pp. 574-582, Mar. 2010.
- [80] Q. Hu, and R. Zane, "Off-line LED driver with bidirectional second stage with reduced energy storage," in Proc. IEEE Energy Conversion Congress and Exposition, Phoenix, AZ, Sep. 2011, pp. 2302-2309.
- [81] Q. Hu, and R. Zane, "Minimizing required energy storage in off-line LED drivers based on series-input converter modules," IEEE Transactions on Power Electronics, vol. 26, no 10, pp. 2887-2895, Sep./Oct. 2011.

APPENDIX A

ESTIMATION OF REQUIRED ENERGY-STORAGE CAPACITANCE IN SINGLE-STAGE OFF-LINE LED DRIVERS

A high power factor (PF) leads to a large double-line-frequency input power ripple, which results in a huge variation of LED current, if directly applied on LED strings. The large ripple on the LED current not only limits the maximum average LED power under ratings of components, but also causes problems like flicker and LED life degradation. In order to limit LED current ripple, energy storage is necessary for filtering the power ripple. The simplest method of filtering is to parallel a capacitor with the LED string, as show in Fig. A.1. However, very large capacitance might be required with this configuration.

In order to simplify the estimation of required energy-storage capacitance for single-stage LED driver shown in Fig. A.1, all power loss is neglected, while $PF = 1$ is assumed. The input voltage and current can be expressed as

$$v_{ac}(t) = V_{ac} \sin(\omega t), \quad (\text{A.1})$$

$$i_{ac}(t) = I_{ac} \sin(\omega t), \quad (\text{A.2})$$

where $\omega = 2\pi f_{line}$, f_{line} is the line frequency. Then, the input power can be derived as

$$p_{ac}(t) = v_{ac}(t)i_{ac}(t) = \frac{V_{ac}I_{ac}}{2}(1 - \cos(2\omega t)) = P_0 - P_0 \cos(2\omega t), \quad (\text{A.3})$$

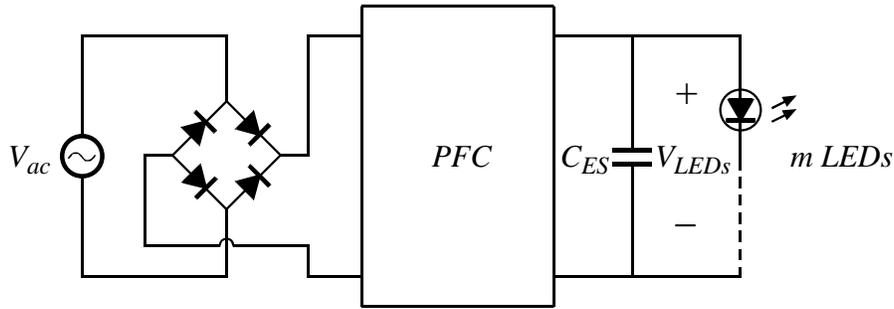


Figure A.1: A single-stage LED driver with PFC and bulk filtering capacitor.

where $P_0 = V_{ac}I_{ac}/2$ is the average input power, which is equal to LED power.

The voltage on the energy-storage capacitor C_{ES} can be expressed as

$$v_C = V_C + \hat{v}_C, \quad (\text{A.4})$$

where V_C is the dc value and \hat{v}_C is the ripple. The ripple on capacitor voltage is normally small due to the small dynamic resistance of LED devices in nominal operation.

The waveforms of input power p_{ac} and output LED-string power p_{LEDs} are demonstrated in Fig. A.2. With the assumption of perfect efficiency, p_{ac} and p_{LEDs} have an identical average value, and the peak and valley of p_{LEDs} locate at the intersections of the two waveforms. Assuming the valley of p_{LEDs} occurs at time t_d , the ripple on p_{LEDs} is

$$\Delta P_{LEDs} = P_0 \cos(2\omega t_d). \quad (\text{A.5})$$

With small ripple on LED string voltage, the LED current ripple is approximately

$$\Delta I_{LED} = \frac{\Delta P_{LEDs}}{V_{LEDs}} = \frac{P_0}{V_{LEDs}} \cos(2\omega t_d). \quad (\text{A.6})$$

Assuming p_{LEDs} is sinusoidal with dc value P_0 , the waveform of p_{LEDs} is

$$p_{LEDs}(t) = P_0 - \Delta P_{LEDs} \cos(2\omega(t - t_d)). \quad (\text{A.7})$$

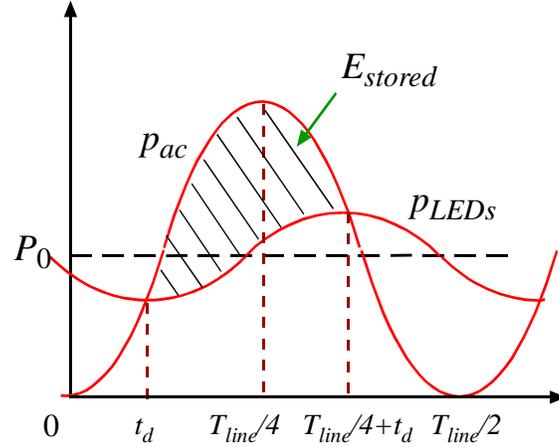


Figure A.2: Input and output power waveforms for a single-stage LED driver.

So, the energy stored into the capacitor C_{ES} within one half-line cycle, the E_{stored} in Fig. A.2, can be expressed as

$$\begin{aligned}
 E_{stored} &= \int_{t_d}^{T_{line}/4+t_d} (p_{ac}(t) - p_{LEDs}(t)) dt \\
 &= \int_{t_d}^{T_{line}/4+t_d} (P_0 \cos(2\omega t_d) \cos(2\omega(t-t_d)) - P_0 \cos(2\omega t)) dt \\
 &= \frac{P_0}{\omega} \sin(2\omega t_d).
 \end{aligned} \tag{A.8}$$

The storage of E_{stored} causes the voltage increase on capacitor C_{ES} , yielding

$$E_{stored} = \frac{1}{2} C_{ES} (V_{LEDs} + \Delta V_{LEDs})^2 - \frac{1}{2} C_{ES} (V_{LEDs} - \Delta V_{LEDs})^2 = 2C_{ES} V_{LEDs} \Delta V_{LEDs}. \tag{A.9}$$

The combination of Eq. A.6, A.8 and A.9 leads to

$$\begin{aligned}
 C_{ES} &= \frac{\sqrt{P_0^2 - \Delta I_{LED}^2 V_{LEDs}^2}}{2\omega V_{LEDs} \Delta V_{LEDs}} = \frac{\Delta I_{LED} V_{LEDs} \sqrt{(I_{LED} / \Delta I_{LED})^2 - 1}}{2\omega V_{LEDs} \Delta V_{LEDs}} \\
 &= \frac{\sqrt{1/\gamma^2 - 1}}{4\pi f_{line} R_{LEDs}},
 \end{aligned} \tag{A.10}$$

where $\gamma = \Delta I_{LED}/I_{LED}$ is normalized LED current ripple and R_{LEDs} is the equivalent dynamic resistance of LED string. When LED current ripple is small, i.e., γ is small, Eq. A.10 can be further simplified to be

$$C_{ES} \approx \frac{1}{4\pi f_{line} R_{LEDs} \gamma}. \quad (A.11)$$

With line frequency of 60 Hz, LED string resistance of several tens ohms, and 10~30% LED current ripple, Eq. A.11 predicts required energy-storage capacitance of several hundred micro farads. As a result, electrolytic capacitors become the only reasonable choice, considering the large capacitance and cost.

Considering the general situation, where the required energy storage can be expressed as

$$E_{stored,gnl} = \alpha \frac{P_0}{\omega}. \quad (A.12)$$

The parameter α is included to indicate possible reduction of energy storage, which can be the result of input current shaping or ripple on the LED current.

With Eq. A.9 and Eq. A.12, the required capacitance becomes

$$\begin{aligned} C_{ES,gnl} &= \frac{\alpha V_{LEDs} I_{LED}}{2\omega V_{LEDs} \Delta V_{LEDs}} = \frac{\alpha I_{LED} / \Delta I_{LED}}{2\omega \Delta V_{LEDs} / \Delta I_{LED}} \\ &= \frac{\alpha}{4\pi f_{line} R_{LEDs} \gamma}. \end{aligned} \quad (A.13)$$

It can be seen that Eq. A.13 is very similar to Eq. A.11, except for the parameter α . According to Eq. A.13, even when energy storage is reduced, the required capacitance can still be very large, especially when small current ripple is targeted.

The large capacitance is mainly due to the ΔV_{LEDs} in the denominators of Eq. A.10 and Eq. A.13, which brings $R_{LEDs} \times \gamma$ in the final formulas. When the energy-storage capacitor is directly parallel with the LED string, the allowed voltage ripple on the capacitor is very limited

due to the small dynamic resistance of LEDs, especially when LED current ripple reduces. As the capacitor has to store and release energy without significant voltage variation, its capacitance has to be very large.

APPENDIX B

ENERGY STORAGE AND LED CURRENT RIPPLE

When a high input power factor (PF) is achieved, a large ripple at double-line frequency is included in input power. As low-frequency LED current ripple is preferred to be small, energy storage is necessary to filter input power ripple. Different ripple control strategies result in large differences in energy storage, even when resulting LED current ripples are identical.

The typical input and output power waveforms for passive filtering are shown in Fig. B.1, with the assumptions of PF = 1 and no power loss. The input and output powers can be described as

$$p_{in}(t) = p_{ac}(t) = P_0 - P_0 \cos(2\omega t), \text{ and} \quad (\text{B.1})$$

$$p_{out}(t) = p_{LEDs}(t) = P_0 - \Delta P_{LEDs} \cos(2\omega(t - t_d)), \quad (\text{B.2})$$

where P_0 is the average power, $\omega = 2\pi/T_{line}$, T_{line} is the line period and t_d is the time shift between input and output powers.

The peak and valley of LED power occur at the intersections of two power waveforms, so the LED power ripple equals to

$$\Delta P_{LEDs} = P_0 \cos(2\omega t_d). \quad (\text{B.3})$$

With small ripple on LED string voltage, the LED current ripple is approximately

$$\Delta I_{LED} = \frac{\Delta P_{LEDs}}{V_{LEDs}} = \frac{P_0}{V_{LEDs}} \cos(2\omega t_d) = I_{LED} \cos(2\omega t_d), \quad (\text{B.4})$$

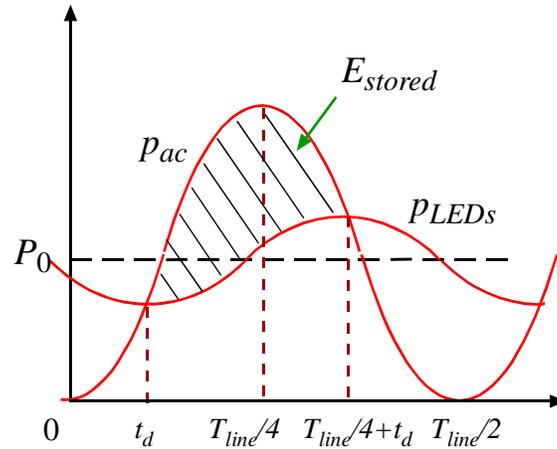


Figure B.1: Input and output power waveforms for passive filtering.

and the percentage LED current is

$$\lambda = \frac{\Delta I_{LED}}{I_{LED}} = \cos(2\omega t_d). \quad (\text{B.5})$$

The energy storage can be derived as

$$\begin{aligned} E_{stored} &= \int_{t_d}^{T_{line}/4+t_d} (p_{ac}(t) - p_{LEDs}(t)) dt \\ &= \int_{t_d}^{T_{line}/4+t_d} (P_0 \cos(2\omega t_d) \cos(2\omega(t - t_d)) - P_0 \cos(2\omega t)) dt \\ &= \frac{P_0}{\omega} \sin(2\omega t_d). \end{aligned} \quad (\text{B.6})$$

The total input energy within one half-line period equals to

$$E_{cycle} = P_0 \times \frac{T_{line}}{2} = \frac{P_0 \pi}{\omega}. \quad (\text{B.7})$$

So the percentage energy storage is

$$\frac{E_{stored}}{E_{cycle}} = \frac{\sin(2\omega t_d)}{\pi} = \frac{\sqrt{1 - \lambda^2}}{\pi}. \quad (\text{B.8})$$

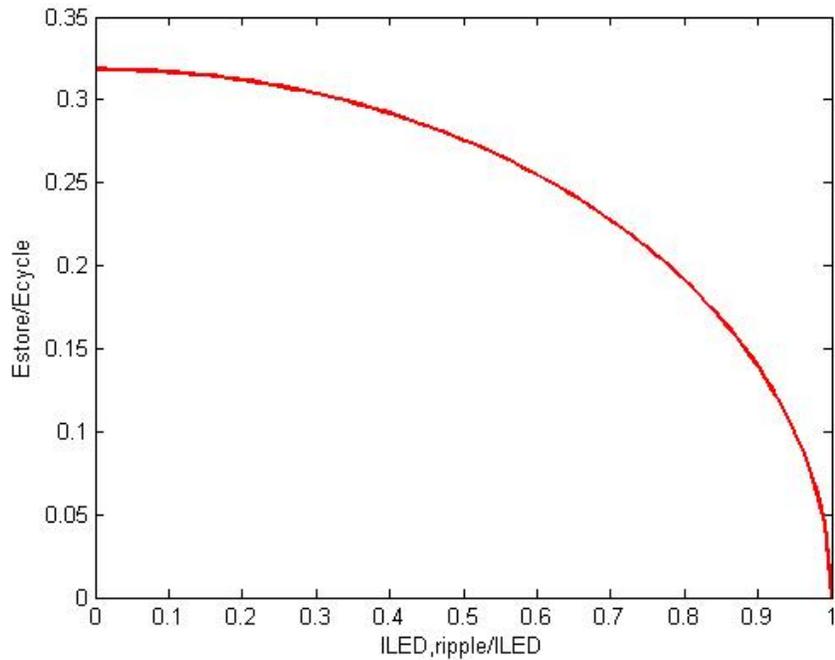


Figure B.2: Percentage energy storage for various percentage LED current ripple.

The relation of percentage energy storage and percentage LED current ripple is shown in Fig. B.2. The peak energy storage is approximately 32% of total input energy, which occurs at zero current ripple. The energy storage is reduced when ripple increases. However, the decrease is relatively slow when ripple is small.

The relatively large energy storage at low current ripple is due to the large time shift between input and output powers. For the following proof, the output power is assumed to have a fixed ripple but arbitrary time shift compared to input power, as shown in Fig. B.3. In this case, the intersections of input and output powers, which occur at times t_1 and t_2 , are not guaranteed to coincide with the peak and valley of output power. However, t_1 and t_2 hold the relation of

$$t_2 = \frac{T_{line}}{4} + t_1. \quad (\text{B.9})$$

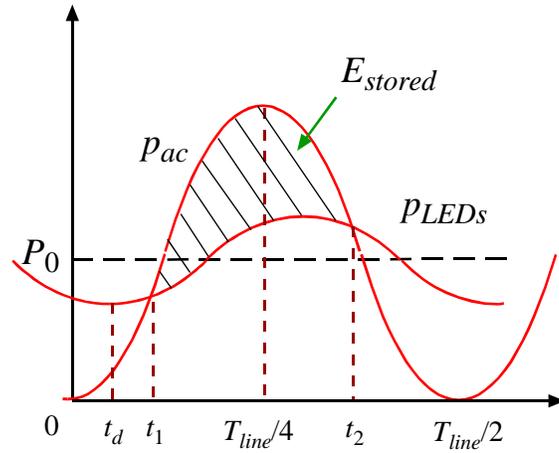


Figure B.3: Input and output power waveforms with time shift of t_d .

In this case, the energy storage can be derived as

$$\begin{aligned}
 E_{stored} &= \int_{t_1}^{t_2} (p_{ac}(t) - p_{LEDs}(t)) dt \\
 &= \int_{t_1}^{T_{line}/4 + t_1} (\Delta P_{LEDs} \cos(2\omega(t - t_d)) - P_0 \cos(2\omega t)) dt \\
 &= \frac{P_0}{\omega} \sin(2\omega t_1) - \frac{\Delta P_{LEDs}}{\omega} \sin(2\omega(t_1 - t_d)).
 \end{aligned} \tag{B.10}$$

The input and output powers are identical at time t_1 , thus

$$P_0 \cos(2\omega t_1) = \Delta P_{LEDs} \cos(2\omega(t_1 - t_d)). \tag{B.11}$$

With Eq. B.11, the energy storage becomes

$$E_{stored} = \frac{P_0^2 - \Delta P_{LEDs}^2}{\omega(P_0 \sin(2\omega t_1) + \Delta P_{LEDs} \sin(2\omega(t_1 - t_d)))} \tag{B.12}$$

When the phase shift of output to input power is less than π , it can be shown that $0 < 2\omega t_1 < \pi/2$, and $-\pi/2 < 2\omega(t_1 - t_d) < \pi/2$. Thus, energy storage becomes larger when t_d increases, and the minimum energy storage occurs at zero phase shift, as shown in Fig. B.4(a).

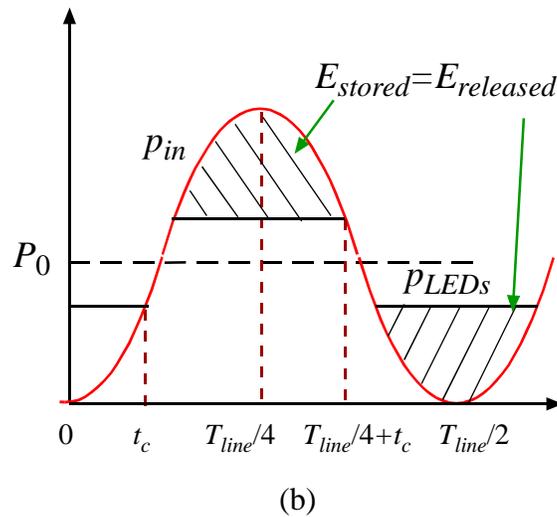
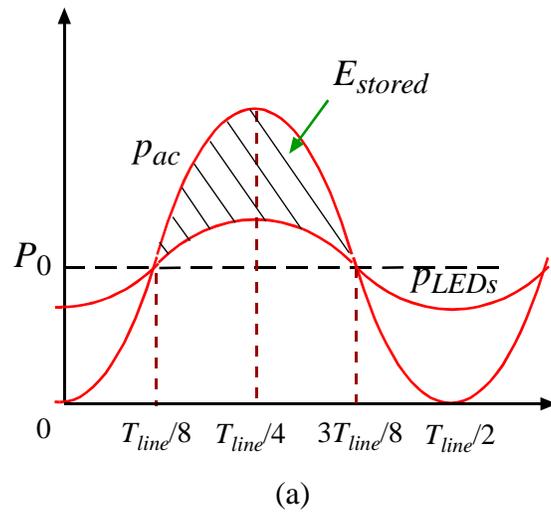


Figure B.4: Input and output power waveforms without time shift for (a) sinusoidal and (b) trapezoidal output current.

However, a special reference is necessary to achieve LED current waveform like Fig. B.4(a), which complicates the design. Instead, a “trapezoidal” LED current waveform results in zero time shift between input and output powers, and is relatively easy to achieve. As shown in Fig. B.4(b), two reference values are necessary to achieve trapezoidal waveform. When input power is larger than the high reference value, the excess power is stored in capacitor. When

input power is smaller than the low reference value, energy is supplied back to the LED string from the capacitor. The shadowed area in Fig. B.4(b) represents the energy to be stored and released in each cycle. As there is no time shift between input and output powers, the energy storage is minimized for a fixed LED current ripple.

The energy storage for trapezoidal LED current can be derived as

$$\begin{aligned}
 E_{stored} &= \int_{T_{line}/4-t_c}^{T_{line}/4+t_c} (p_{ac}(t) - p_{LEDs}(t)) dt \\
 &= \int_{T_{line}/4-t_c}^{T_{line}/4+t_c} (-P_0 \cos(2\omega t) - P_0 \cos(2\omega t_c)) dt \\
 &= \frac{P_0}{\omega} \sin(2\omega t_c) - P_0 \cos(2\omega t_c) 2t_c.
 \end{aligned} \tag{B.13}$$

And the percentage energy storage is

$$\frac{E_{stored}}{E_{cycle}} = \frac{\sin(2\omega t_c) - \cos(2\omega t_c) 2\omega t_c}{\pi} = \frac{\sqrt{1-\lambda^2} - \lambda \arccos(\lambda)}{\pi}, \tag{B.14}$$

which is plotted in Fig. B.5 with a black line. For comparison, the percentage of energy storage for passive filtering is also plotted with a red line. It is obvious that energy storage is smaller for the LED current with trapezoidal waveform.

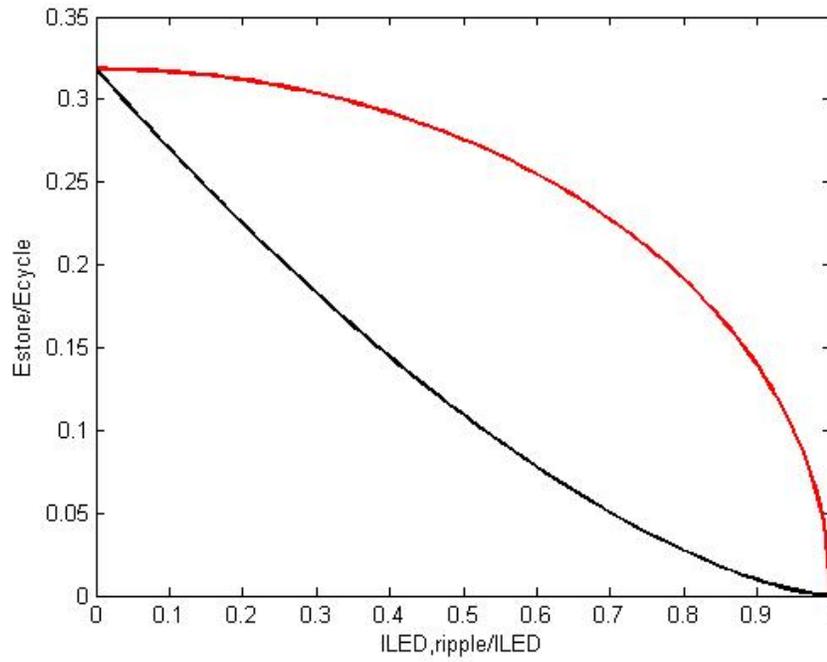


Figure B.5: Percentage energy storage for various percentage LED current ripple. Black line is for trapezoidal output current case. Red line is for passive filtering case.

APPENDIX C

ESTIMATION OF SWITCHING-FREQUENCY RIPPLE ON LED CURRENT AND REQUIRED FILTER CAPACITANCE

The circuit diagram of a two-stage off-line LED driver is shown in Fig. C.1, with a first stage for power factor correction (PFC) and a bidirectional second stage to filter double-line-frequency power ripple. Although the energy-storage capacitance can be significantly reduced with the bidirectional second stage, resulting in a small film capacitor C_{ES} , another capacitor is necessary to filter the high-frequency LED current ripple due to the switching behavior of the converters. As indicated in Fig. C.1, the filter capacitor C_{LEDs} is parallel with the LED string, with the purpose of bypassing the high-frequency components on PFC-stage output current and second-stage input current. Estimation of these high-frequency components is necessary in order to select sufficient capacitance to limit LED current ripple.

Assuming double-line-frequency component of input power is perfectly filtered by the second stage and C_{ES} , the filter capacitor C_{LEDs} only has to deal with the high-frequency ripple, of which the harmonic at switching frequency is the most important for filter design. When the PFC stage with $PF = 1$ operates in critical conduction mode (CRM), its switching frequency varies throughout half-line periods, achieving minimum frequency at peak line voltage, which coincides with maximum inductor current ripple. The combination of low frequency and large ripple results in worse-case LED current ripple. On the other hand, the second stage may operate

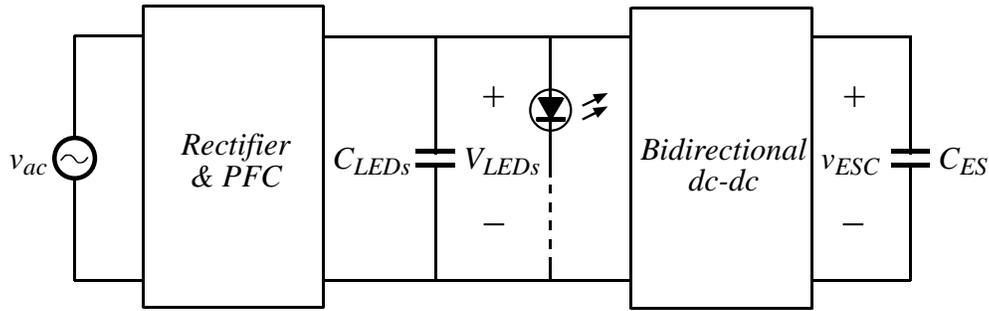


Figure C.1: An LED driver with PFC first stage and bidirectional second stage.

with soft switching at relatively high frequency. Consequently, the switching-frequency ripple on LED current is considered primarily due to PFC stage.

The longest switching period of PFC stage happens at peak input voltage. As shown in Fig. C.2, the output current waveform of PFC stage is pulsated and triangular and with zero value during t_{on} , which is the low-side transistor conduction period. Of all the switching harmonics of i_{out} , the one at switching frequency $f_s = 1/t_s$ is of the most interest for the estimation of the high-frequency ripple on LED current.

The parameters of the waveform in Fig. C.2, including amplitude and periods, can be calculated with Eqs. C.1 ~ C.3. Note that these equations are specifically for boost converters operating in CRM and with PF = 1.

$$I_{L,pk} = 2\sqrt{2} \frac{P_{ac,avg}}{V_{ac,rms}} \quad (C.1)$$

$$t_{on} = \frac{I_{L,pk}}{\frac{\sqrt{2}V_{ac,rms}}{L}} \quad (C.2)$$

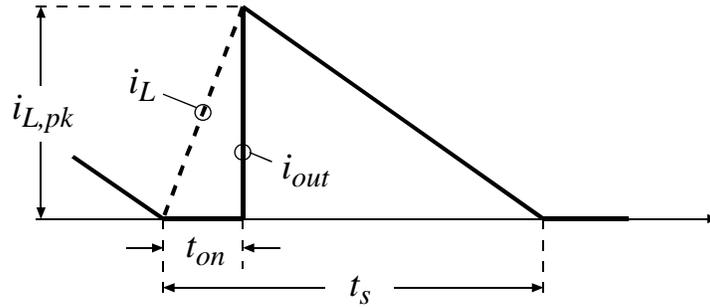


Figure C.2: Output current waveform of boost PFC first stage.

$$t_s = \frac{V_{LEDs}}{V_{LEDs} - v_g} t_{on} \quad (C.3)$$

Around peak line voltage v_g is normally close to V_{LEDs} , thus t_{on} period is comparably small within t_s period according to Eq. C.3. Hence, the target harmonic component of i_{out} at f_s can be estimated with waveform of i_L in stead of i_{out} . Note that this step leads to overestimation of switching-frequency harmonic of i_{out} .

The target harmonic component can be estimated from the waveform shown in Fig. C.3(a), which is the triangular inductor current without double-line-frequency component. With concrete parameters, like voltages and inductance, the harmonics can be calculated with numerical method. However, a general approach for estimation will be provided here rather than a specific answer.

With peak-to-peak amplitude identical to the waveform in Fig. C.3(a), Fig. C.3(b) demonstrates a triangular waveform with infinite increasing slope, while Fig. C.3(c) shows one with identical increasing and decreasing slopes. For triangular waveforms with a fixed peak-to-peak value, the two in Figs. C.3(b) and C.3(c) contain minimum and maximum magnitudes of the harmonic component at f_s , which are $i_{L,pk}/\pi \approx 0.32i_{L,pk}$ and $i_{L,pk} \times 4/\pi^2 \approx 0.4i_{L,pk}$, respectively. As

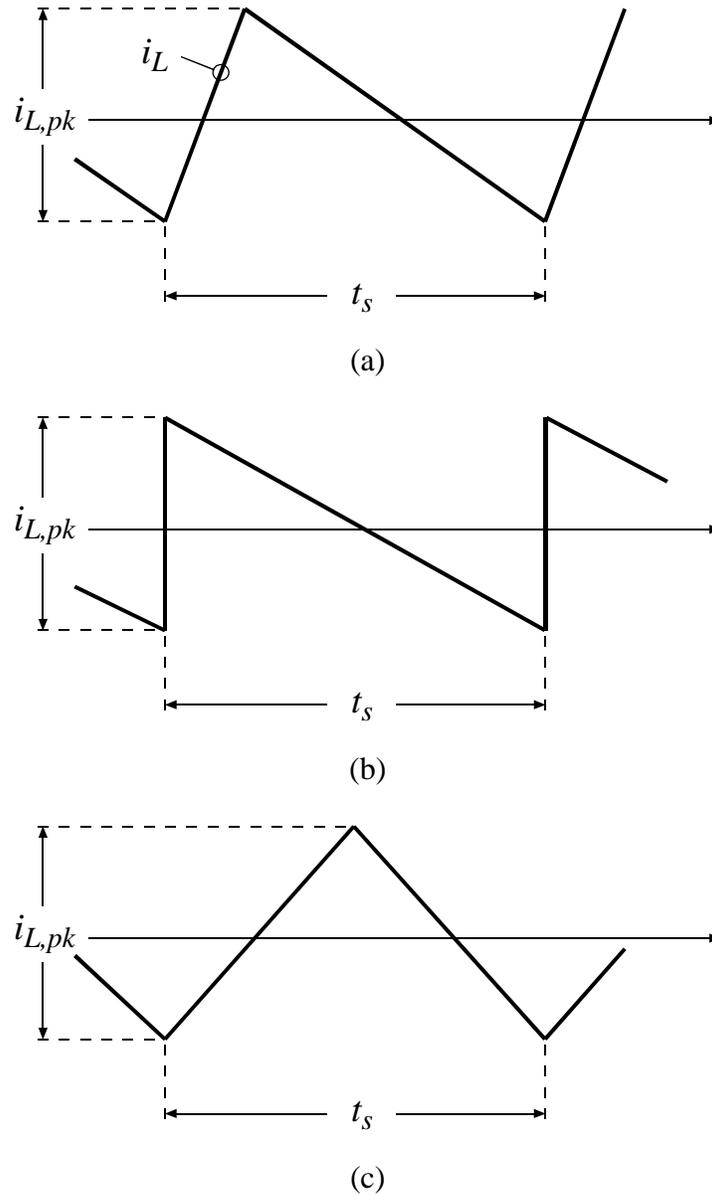


Figure C.3: (a) Inductor current without double-line-frequency component, triangular waveforms with (b) infinite increasing slope and (c) identical increasing and decreasing slopes. All three waveforms have identical amplitude and frequency $f_s = 1/t_s$.

a result, the switching-frequency harmonic for i_L has a magnitude between $0.32i_{L,pk}$ and $0.4i_{L,pk}$.

The lower value is selected here, as it will compensate the overestimation due to utilizing i_L rather than i_{out} for estimation.

With the above two steps, the harmonic component of i_{out} at switching frequency f_s is estimated to be

$$i_{out@f_s} \approx 0.32 \times i_{L,pk} . \quad (C.4)$$

A portion of this harmonic component goes to the LED string, which can be calculated as

$$i_{LED,ripple} = \frac{\frac{1}{2\pi f_s C_{LEDs}}}{\frac{1}{2\pi f_s C_{LEDs}} + R_{LEDs}} i_{out@f_s} = \frac{1}{1 + 2\pi f_s R_{LEDs} C_{LEDs}} i_{out@f_s} . \quad (C.5)$$

With Eq. C.2 to Eq. C.5, the switching-frequency LED current ripple can be derived as

$$i_{LED,ripple} = \frac{0.32 i_{L,pk}}{1 + 2\pi \frac{R_{LEDs} C_{LEDs}}{L} \frac{(V_{LEDs} - v_g) v_g}{V_{LEDs} i_{L,pk}}} . \quad (C.6)$$

In order to meet certain limits on high-frequency LED ripple, the required filter capacitance can be calculated from

$$C_{LEDs} = \frac{1}{2\pi} \frac{L}{R_{LEDs}} \frac{V_{LEDs}}{(V_{LEDs} - v_g) v_g} \frac{i_{L,pk} (0.32 i_{L,pk} - i_{LED,ripple})}{i_{LED,ripple}} . \quad (C.7)$$

When a smaller high-frequency LED current ripple is required, a larger filter capacitor C_{LEDs} should be used. A smaller inductor can help reduce C_{LEDs} by increasing switching frequency. Reduction of peak inductor current can also help, e.g., by adopting the constant input current approach in PFC stage.