Performance Analysis and Design of Distributed Static Series Compensators for Transmission Line Reactance Control

by

Alexander McGrath Brissette

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Annabelle Pratt

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Thesis directed by Prof. Dragan Maksimović

The growth and diversification of the electric utility grid has required the expanded use of compensation devices. One class of compensation devices of interest are distributed static series compensators (DSSCs). DSSCs are power electronics devices that can inject positive or negative reactive impedance into a transmission line by connecting to it in series through a transformer suspended from the line. This thesis addresses the deployment, performance, and design of DSSCs. In order to analyze the impact of DSSCs on a transmission network, a method for linearizing the network is presented. The linearized network model allows the relationships between the network operating points and the injected reactances to be easily derived, thereby illuminating how best to deploy DSSCs. The model, which is general and applies to arbitrarily complex systems, is further simplified into a proposed new form called "line efficacy," which provides additional insights without knowledge of the system topology or operating state.

This thesis additionally proposes an advanced design for DSSCs, allowing them to improve upon the compensation performance requirements given by the linearized transmission system model. The advanced design is an alternative method for controlling the inverter stage of active DSSCs. It is shown that three-level, constant duty cycle switching increases the energy available from the inverter dc-side capacitor and thus the magnitude of injected reactance, compared to traditional, sinusoidally modulated three-level switching. These results are validated on a 5kVA single-phase inverter implemented in hardware. Both the design and experimental results are presented in detail.

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Introduction

The United States Energy Information Administration predicts that nationwide demand for electricity will grow by about 25% over the next 20-30 years [1,2], and the electric grid must likewise grow and modernize in order to maintain efficiency and reliability. Improvements in system capacity and functionality are necessary to ensure generation assets are more fully utilized, especially in the case of increased penetration of intermittent sources like solar and wind [3–7].

Compensation devices are often employed to increase system capacity. Mechanically switched shunt capacitor banks and rotating synchronous compensators, for example, have traditionally been employed to inject and absorb reactive power, stabilizing the system by maintaining proper voltage levels and reducing line currents [8–10]. More recently, power electronics-based flexible AC transmission system (FACTS) devices, such as static VAr compensators, static synchronous series compensators, unified power flow controllers, and static synchronous compensators (STATCOM), have been introduced to improve compensation control and functionality [11–16]. Such devices may operate in shunt or series (or both, as with unified power flow controllers [17, 18]), and can be designed for transmission levels as high as 345kV and 200MVA [19]. While FACTS have been demonstrated in many utility-scale installations [20,21], widespread deployment has been hampered by technical and cost challenges [19].

A new class of FACTS devices, called distributed static series compensators (DSSC), has been developed that may overcome the drawbacks of existing FACTS technologies [19, 22–25]. DSSCs are small, modular units that connect to the transmission system through a single turn

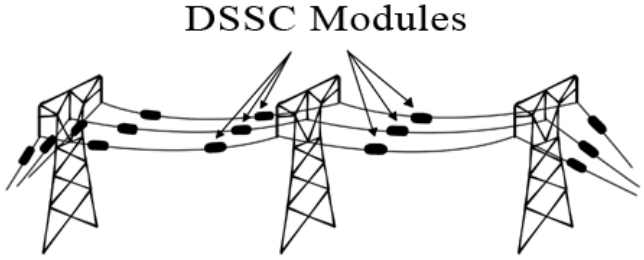


Figure 1.1: Illustration of DSSC modules suspended from power lines [19]

transformer (STT) suspended from a transmission line. Through some combination of passive and active components on the secondary side of the STT, the DSSC may emulate a small series reactance on the line. A large number of these units may be deployed in a transmission system, allowing careful control of the system power flows. DSSCs' small size, easy installation, and relatively low power capacity also make them a highly scalable alternative to existing FACTS solutions. Fig. 1.1 shows a simple illustration of DSSCs deployed, as intended, along the length of a transmission line. Whereas most transmission system upgrades require a large upfront capital investment and an oversized design to accommodate growing system capacity over the long life of the device, single DSSCs may be added to the transmission system as needed [24].

The modular and distributed nature of DSSCs allows them to be deployed throughout a transmission system; however, thorough analysis of their impact on a system is limited in the literature. The complex, nonlinear nature of a large power system makes it difficult to predict what changes a DSSC may cause. Likewise, without the computational intensity of repeated load flow solutions, it is not apparent to a system operator which installed DSSCs should be used, and in what amount, to achieve some compensation goal. This thesis presents a model that reduces a power system to a set of linear coefficients that relate system operating points to the reactance injected by the DSSC. Similar work has been shown in [26], which relates power system quantities using sensitivity analysis. In Chapter 2, this thesis presents a more complete derivation of the model, an additional calculation for DSSC analysis, and an in-depth discussion of how system behavior relates to DSSC deployment.

The method for creating the model presented here is based on the DSSC as a controllable series reactance. Practical design considerations limit the injected reactance to a small fraction of the connected line impedance; as such, the DSSC reactance may be considered a small perturbation to the existing line impedance. Consequently, a linearized model of a transmission system may be developed using standard perturbation and linearization methods on the network power balance equations. In contrast to well-known methods of transmission system linearization [27], which include work related to FACTS devices [28], this method is derived from the DSSCs' *physical*, rather than purely mathematical, perturbations to line impedances. Thus, they linearize the system for the resulting actual perturbations to the system operating points. This model quickly and efficiently reveals how a DSSC on one line effects all bus operating points (voltage, power, etc.), or how DSSCs are best used on any or all lines to influence a given operating point.

The model is further used to derive a figure of merit, called line efficacy, to indicate whether DSSCs on that line will have a large impact on system operation. The efficacy of a line can be determined based solely on the current and impedance on the line. Within limitations that will be discussed, efficacy measurements can be used to compare lines to identify which are best suited for DSSC deployment. Unlike the complete linearized model, efficacy can be calculated without knowledge of the system operating points or even the system topology.

1.1 Reactive Power Compensation

1.1.1 Effects of a DSSC on a two-bus system

Like other compensation devices, DSSCs may be used to increase power system capacity. As a simple introductory example, consider the effect of DSSCs on the real power capacity of a simple two-bus system, pictured in Fig. 1.2. For this basic system, the relationship between line impedance and system operating points is well known and easy to derive. This simple example is used to highlight the use of DSSCs for three compensation benefits: line current reduction, bus voltage correction, and generator reactive power reduction. In this case, closed-form expressions

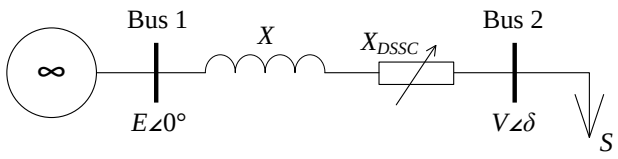


Figure 1.2: Simple two-bus system with, generator, load, and transmission line with connected DSSC

can be found for all three.

In the system pictured in Fig. 1.2, Bus 1 is the slack bus with voltage $\bar{E}$ and a reference phase of zero ($\bar{E} = E\angle 0 = E$), and Bus 2 is a load bus with voltage V and phase δ ($\bar{V} = V\angle\delta$). The load power ($S = P + jQ$) is constant, with power factor angle $\phi = \tan^{-1}(Q/P)$. The line impedance is approximated to be purely a series reactance X, with losses and shunt impedance neglected. A DSSC is also connected, adding a variable series reactance X_{DSSC}.

1.1.2 Load bus voltage control

The relationship between transferred power and load bus voltage V may be expressed in a few different ways. First, the maximum allowed load power – i.e., the system capacity – is

$$P_{max} = \frac{E^2 \cos\phi}{2X_{tot}(1 + \sin\phi)} \ , \tag{1.1}$$

where $X_{tot} = X + X_{DSSC}$. Traditionally, the system capacity is increased by adjusting the load power factor ($pf = \cos\phi$) using compensation devices connected to the load bus, while the line impedance is fixed. However, (1.1) shows that the capacity may also be increased by reducing the total line reactance X_{tot}, which can be achieved by controlling DSSCs to emulate series capacitance ($X_{DSSC} < 0$).

Given a fixed load power, increasing the system capacity has the effect of raising the load bus voltage. If P and Q are the real and reactive power absorbed by the load, respectively, the load bus voltage magnitude V may be derived as a function of the system operating points:

$$V = \sqrt{\frac{E^2}{2} - X_{tot}Q \pm \sqrt{\frac{E^4}{4} - {X_{tot}}^2 P^2 - X_{tot}E^2 Q}} \ . \tag{1.2}$$

For V as a function of P, (1.2) gives the well-known PV load characteristic curves. Fig. 1.3 illustrates how these PV curves relate to the line reactance. For a given P, there are two solutions for V. It is necessary to choose the upper solution on the curve, both for stability purposes and to maintain $V \approx E$ [30]. Fig. 1.3 shows that decreasing X_{tot} raises P_{max}, which is the right-most vertex point of each curve. The plot also shows that, for a fixed load power P, decreasing X_{tot} increases V. Simply put, raising load bus voltage has the effect of increasing system capacity, and vice versa; X_{DSSC} can be used to control both.

1.1.3 Generator reactive power control

Rotating machines typically have limited reactive power output capacity, due to limits on their excitation voltage [10]. DSSCs can be used to prevent generators from exceeding these limits, potentially allowing load to be increased at fixed power factor. This is the clearest illustration of DSSCs as reactive power compensators: they can be controlled to inject reactive power into the system in order displace reactive power from a generator.

Considering the system in Fig. 1.2, the reactive power required from the generator is

$$Q_g = \frac{E^2}{2X_{tot}} \pm \sqrt{\left(\frac{E^2}{2X_{tot}}\right)^2 - \frac{QE^2}{X_{tot}} - P^2}\ . \tag{1.3}$$

Equation (1.3) is illustrated in Fig. 1.4, where Q_g is plotted against load power (with fixed ϕ) for

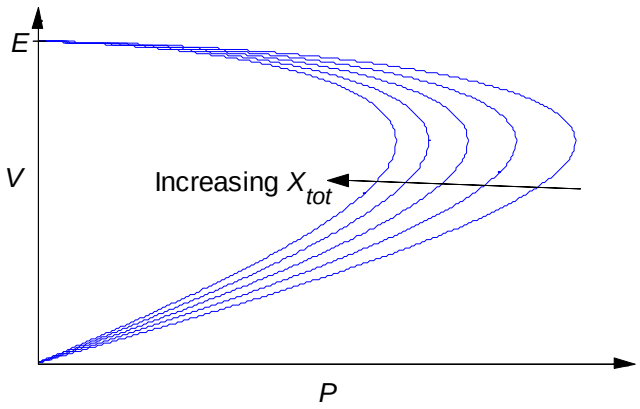


Figure 1.3: Load bus voltage V vs. load power P for a two-bus system, with varying line impedance X_{tot}

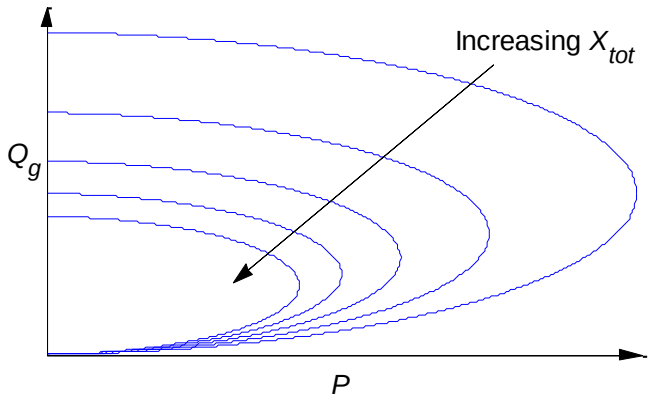


Figure 1.4: Generator reactive power Q_g vs. load power P for a two-bus system, with varying line impedance X_{tot}

different values of X_{tot}. For a given P, the lower corresponding value of Q_g is desired. Fig. 1.4 shows that, for fixed P, decreasing X_{tot} (corresponding to $X_{DSSC} < 0$ and thus positive injected reactive power) also decreases Q_g.

Fig. 1.4 also shows that, similar to the PV relationship (Fig. 1.3), there is a maximum value of P (the right-most point on the curve) above which the generator cannot supply sufficient reactive power. This capacity can be increased by using DSSCs to decrease X_{tot}.

1.1.4 Line current control

According to [19], the primary benefit of DSSCs is their ability to reduce line current, especially in an overload condition. This functionality is easily illustrated by a slightly different two-bus system, pictured in Fig. 1.5. The line current magnitude is

$$I = \frac{\sqrt{V_1^2 + V_2^2 - 2V_1V_2\cos(\delta_1 - \delta_2)}}{X_{tot}} \,. \tag{1.4}$$

Obviously, raising X in this case will reduce the line current. As [23] describes in detail, line current overload conditions are a frequent cause of system capacity limitations. On larger transmission systems, a line may be operating at or near its current limit, preventing the active power present in the system from being increased, even when the system itself is not near its mathematical power limit P_{max} (as in Sections 1.1.2 and 1.1.3) and no other lines or devices are overloaded. In this

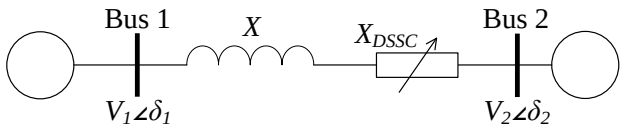


Figure 1.5: Alternative two-bus system with DSSC and two generators

situation, DSSCs may be used to steer current to more lightly loaded lines so that, by relieving an existing overload condition, the capacity of the entire system is raised.

1.2 Distributed Static Series Compensators

DSSCs may be used to achieve the compensation functionality described above. They consist, at the minimum, of a single turn transformer (STT) that clamps directly to a transmission line. Different functionality and performance levels may be achieved depending on the hardware connected to the secondary side of the STT. Advanced designs are capable of emulating both inductance and capacitance, and the deployment of many devices on a system allows them to achieve the applications described in Section 1.1.

1.2.1 Economic benefit of DSSCs

The economic justification has been studied in-depth in [24]. The authors present two side-by-side 20-year growth cases for the hypothetical IEEE 39-bus test system. In one case, load growth is accommodated by installing new transmission lines where needed. In the other case, DSSCs are deployed on the transmission line to increase its capacity.

In the test case simulation, the system load increases by 2% annually, while wind generation capacity increases by 1% per year in order to meet mandated renewable energy requirements. Other generation assets do not change. The system load flows are found in each iteration, and it is determined if any transmission line has reached its thermal capacity while ensuring that the wind assets are not curtailed. If a line exceeds its limit, then either (1) a new, equally rated line is installed in parallel to the overloaded line; or (2) DSSCs are installed, and new lines are also built

if necessary.

The system investments are calculated in terms of MW-miles. For a transmission line, this is simply the product of a line's rating and its length. It is necessary to represent DSSC investment in equivalent terms. If DSSCs cost \$100 per unit kVA of capacity, and transmission lines cost \$1000/MW-mile, then 1MVA of DSSC capacity costs the same as 100MW-miles of new line capacity.

Tables 1.1 and 1.2, reproduced from [24], show the results of the simulation. The required investment if only new lines are installed is twice the investment if DSSCs are used as well. Multiple upgrades to a single transmission path are especially costly, as the number of parallel lines is doubled each time an upgrade is required. Without DSSCs, Line 30 is upgraded four times and Line 20 is upgraded twice, while with DSSCs Line 30 is only upgraded three times.

1.2.2 DSSC designs

The most basic DSSC is a passive design, presented in [19]. It uses only a switch on the secondary side of the STT connected to the transmission line. When the switch is closed, the STT magnetizing inductance is shorted and the device has no effect. When the switch is open, the magnetizing inductance is reflected through the STT in series with the line. This design is simple but limited in functionality, as the device can supply only a fixed value of series inductance.

An improved design, the active DSSC proposed in [19, 23, 25] features a voltage source in-

Table 1.1: Transmission system investment required with only added line capacity [24]

Year	Line Number	Line Length (mi)	Capacity added (MW)	MW-mi added (×1000)
6	20	100	90	9
	29	167	130	21.7
	30	183	50	9.2
8	30	183	100	18.3
11	30	183	200	36.6
17	30	183	400	73.2
18	20	100	180	18
			Total	**186**

Table 1.2: Transmission system investment required with DSSCs and added line capacity [24]

Year	Line Number	Line capacity added (MW)	DSSC capacity added (MVA)	Equivalent MW-mi added (×1000)
6	29	–	6.2	0.62
	30	–	34	3.4
7	30	–	18.1	1.82
8	29	–	5.6	0.56
	30	–	17.9	1.8
9	30	–	17	1.7
10	30	50	–	9.2
	29	–	5.2	0.52
11	30	–	1.9	0.2
12	29	–	4.8	0.5
	30	–	8.3	0.84
13	30	100	–	18.3
14	3	–	4.9	0.5
	30	–	6	0.6
15	30	200	–	36.6
17	29	–	4.4	0.44
	3	–	4.1	0.42
18	3	–	8.2	0.82
	20	–	26.7	2.68
19	20	–	66.7	6.68
	30	–	21.6	2.16
	3	–	3.1	0.32
			Total	**90.7**

verter (VSI) in parallel with the magnetizing inductance on the secondary side of the STT (see Fig. 1.6). By measuring the secondary-side current I_{ac}, the VSI can be controlled to produce an injected series reactance $X_{inj} = V_{ac}/\left(n^2 I_{ac}\right)$ on the line, where the VSI ac-side voltage V_{ac} is synthesized from the dc-side voltage V_{dc} by the VSI. If V_{ac} is controlled to a $\pm 90^\circ$ phase difference with respect to I_ℓ, then its addition allows X_{inj} to be inductive or capacitive, respectively. Equivalently,

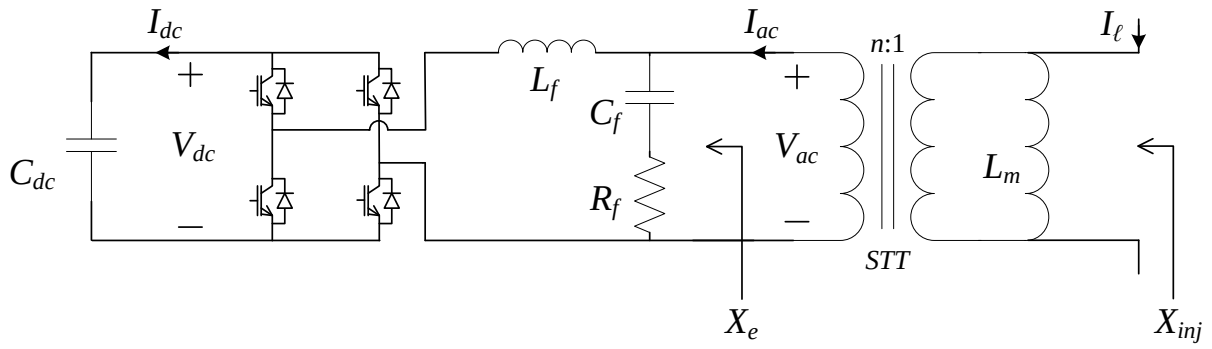


Figure 1.6: Complete circuit for active DSSC

the VSI can emulate positive or negative reactance $X_e = V_{ac}/I_{ac}$, corresponding to inductance or capacitance, respectively.

The VSI design presented in [19,23,25] uses an H-bridge with conventional sinusoidally pulse-width modulated (SPWM) control. Under this control scheme, the dc-side voltage is approximately fixed, but with some small ripple. Because this is a purely reactive power application, the dc side only requires a capacitor to store and cycle the energy required by the DSSC. Under SPWM control, the capacitor voltage is not allowed to vary widely, limiting the accessible amount of capacitor energy. In Chapter 3 and 4, a new control scheme is proposed in which the VSI H-bridge operates at constant duty cycle, allowing the dc-side capacitor voltage to cycle from some maximum value to 0 so that the full amount of capacitor stored energy is available to the DSSC.

1.3 Thesis Outline

This thesis addresses two important topics related to DSSCs. Chapter 2 describes a method of power system linearization specific to DSSCs. This method is useful for identifying where in a transmission system DSSCs are best deployed for a given compensation application. Chapters 3 and 4 discuss the design of a single active DSSC unit. Chapter 3 focuses on the operating principles of the DSSC and presents a process for choosing important system components. Chapter 4 then describes in detail the design, implementation, and experimental results of a DSSC VSI constructed

for this thesis. Finally, Chapter 5 concludes the thesis with a summary of the contributions and potential areas of future research.

Chapter 2

DSSC Deployment Linearization Model

Similar to other compensation devices, DSSCs may be used to increase the capacity of a transmission system by controlling the flow of reactive power. For systems with an arbitrary number of buses, closed-form expressions that relate DSSC injected reactance and system operation may not exist. This chapter discusses the method of perturbing and linearizing a transmission system to produce proportional relationships between system quantities and DSSC injected reactances.

2.1 Linearization Model Derivation

2.1.1 Linearization of network power balance equations

A power system is modeled, by common convention [31], as a collection of N buses connected by lines with known impedances. A bus is characterized by its voltage magnitude V, voltage angle δ, and real and reactive power (P and Q, respectively) injected into the network. For a given bus, two of these values are unknown and two are known and, for the purpose of this analysis, fixed. For a PV bus, P and V are fixed; for a PQ bus, P and Q; for a slack bus, V and δ.

A line is defined by the two buses it connects and is characterized by its admittance:

$$y_{ij} = g_{ij} + jb_{ij} = \frac{1}{r_{ij} + jx_{ij}}, \tag{2.1}$$

where i and j are the buses at either end of the line. In this work, line and bus shunt impedance values are neglected. The admittance matrix $\mathbf{Y}$ for the system is formed with all the line admittances

in conventional fashion:

$$\mathbf{Y} = \mathbf{G} + j\mathbf{B} = \begin{bmatrix} \sum_{k=1}^{N} y_{1k} & \cdots & -y_{1N} \\ \vdots & \ddots & \vdots \\ -y_{1N} & \cdots & \sum_{k=1}^{N} y_{Nk} \end{bmatrix}.$$

Here, Y_{ij}, G_{ij}, B_{ij}, etc, represent elements of $\mathbf{Y}$ and their constituent real and reactive parts, while y_{ij}, g_{ij}, and b_{ij} are actual admittance and constituent values of Line i-j (e.g., $Y_{22} = \sum_{k=1}^{N} y_{2k}$ and $Y_{12} = -y_{12}$).

The network power balance equations relate bus voltages and line admittances to the real and reactive power injected into a network of N buses at a given Bus i. They are:

$$P_i = V_i \sum_{k=1}^{N} V_k |G_{ik}\cos(\delta_i - \delta_k) + B_{ik}\sin(\delta_i - \delta_k)| \tag{2.2a}$$

$$Q_i = V_i \sum_{k=1}^{N} V_k |G_{ik}\sin(\delta_i - \delta_k) - B_{ik}\cos(\delta_i - \delta_k)| \,. \tag{2.2b}$$

In order to perturb and linearize (2.2), an incremental perturbation, denoted by a $\hat{}$ symbol, is added to each term. For example, $P_i \to P_i + \hat{p}_i$, or $\bar{V}_i = V_i\angle\delta_i \to (V_i + \hat{v}_i)\angle\left(\delta_i + \hat{\delta}_i\right)$, where $\bar{V}_i$ is a phasor with magnitude V_i and angle δ_i. It must be noted that $\hat{y}$ is a perturbation to y, not Y. Therefore

$$Y_{ij} \to Y_{ij} + \begin{cases} \hat{y}_{ij} \;\; for \;\; i = j \\ -\hat{y}_{ij} \;\; for \;\; i \neq j \end{cases}.$$

The same holds for g and b.

In order to linearize the power balance equations, first the original operating points of the unperturbed system are determined using traditional load flow techniques. Next, the terms in (2.2) are perturbed and the resulting expressions are expanded. Finally, the original values (i.e., the terms from (2.2)) are subtracted, leaving equations that interrelate the incremental values by constants:

$$0 = -\hat{p}_i + u^{pg}_{i,mn}\hat{g}_{mn} + u^{pb}_{i,mn}\hat{b}_{mn} + \sum_{k=1}^{N} A^{pv}_{ik}\hat{v}_k + A^{p\delta}_{ik}\hat{\delta}_k \tag{2.3a}$$

$$0 = -\hat{q}_i + u^{qg}_{i,mn}\hat{g}_{mn} + u^{qb}_{i,mn}\hat{b}_{mn} + \sum_{k=1}^{N} A^{qv}_{ik}\hat{v}_k + A^{q\delta}_{ik}\hat{\delta}_k \ , \tag{2.3b}$$

where Line m-n is the perturbed line. The constants A and u are formed with the original operating point values (e.g. $V,\ G,\ \delta$, etc; see Appendix A for further details).

2.1.2 Solving for the bus perturbations

For each bus, (2.3) is a pair from a system of equations representing all buses of the linearized network. The system of equations may be expressed as follows:

$$0 = \mathbf{u}^{\mathbf{g}}_{mn}\hat{g}_{mn} + \mathbf{u}^{\mathbf{b}}_{mn}\hat{b}_{mn} + [-\mathbf{I}_{2N}\ \mathbf{A}]\left[\hat{\mathbf{p}}\ \hat{\mathbf{q}}\ \hat{\mathbf{v}}\ \hat{\boldsymbol{\delta}}\right]^{\mathrm{T}}, \tag{2.4}$$

where

$$\mathbf{u}^{\mathbf{g}}_{mn} = \left[u^{pg}_{1,mn}\ u^{pg}_{2,mn}\cdots\ u^{pg}_{N,mn}\ u^{qg}_{1,mn}\ u^{qg}_{2,mn}\cdots\ u^{qg}_{N,mn}\right]^{\mathrm{T}},$$

$$\mathbf{u}^{\mathbf{b}}_{mn} = \left[u^{pb}_{1,mn}\ u^{pb}_{2,mn}\cdots\ u^{pb}_{N,mn}\ u^{qb}_{1,mn}\ u^{qb}_{2,mn}\cdots\ u^{qb}_{N,mn}\right]^{\mathrm{T}},$$

$$\mathbf{A} = \begin{bmatrix} A^{pv}_{11} & \cdots & A^{pv}_{1N} & A^{p\delta}_{11} & \cdots & A^{p\delta}_{1N} \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ A^{pv}_{N1} & \cdots & A^{pv}_{NN} & A^{p\delta}_{N1} & \cdots & A^{p\delta}_{NN} \\ A^{qv}_{11} & \cdots & A^{qv}_{1N} & A^{q\delta}_{11} & \cdots & A^{q\delta}_{1N} \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ A^{qv}_{N1} & \cdots & A^{qv}_{NN} & A^{q\delta}_{N1} & \cdots & A^{q\delta}_{NN} \end{bmatrix},$$

$$\hat{\mathbf{p}} = [\hat{p}_1\ \hat{p}_2\cdots\hat{p}_N]\,,\ \hat{\mathbf{q}} = [\hat{q}_1\ \hat{q}_2\cdots\hat{q}_N]\,,$$

$$\hat{\mathbf{v}} = [\hat{v}_1\ \hat{v}_2\cdots\hat{v}_N]\,,\ \text{and}\ \hat{\boldsymbol{\delta}} = \left[\hat{\delta}_1\ \hat{\delta}_2\cdots\hat{\delta}_N\right]\,,$$

and $\mathbf{I}_{2N}$ is an identity matrix of size $2N$.

The bus types (PV, PQ, or slack) provide constraints to the linearization, and the system (2.4) may be simplified by removing the constrained terms. They are defined by the two known,

fixed quantities for a given bus, so perturbations to these values must be zero. First, all constrained terms may be removed from $\left[\hat{\mathbf{p}}\ \hat{\mathbf{q}}\ \hat{\mathbf{v}}\ \hat{\boldsymbol{\delta}}\right]$, reducing the vector length from $4N$ to $2N$. The reduced vectors are denoted as $\hat{\mathbf{p}}'$, $\hat{\mathbf{q}}'$, etc.

Next, columns may be removed from $-\mathbf{I}_{2N}$ and $\mathbf{A}$. For the slack Bus i, remove column i from $\mathbf{A}$ and column $N+i$ from $-\mathbf{I}_{2N}$. For a PQ Bus i, remove columns i and $N+i$ from $-\mathbf{I}_{2N}$. For a PV Bus i, remove column i from $-\mathbf{I}_{2N}$ and $\mathbf{A}$. Concatenating these reduced versions of $-\mathbf{I}_{2N}$ and $\mathbf{A}$, as in (2.4), results in a new matrix $\mathbf{A}'$. $\mathbf{A}'$ is square and invertible, allowing a solution for $\left[\hat{\mathbf{p}}'\ \hat{\mathbf{q}}'\ \hat{\mathbf{v}}'\ \hat{\boldsymbol{\delta}}'\right]$ to be found:

$$\left[\hat{\mathbf{p}}'\ \hat{\mathbf{q}}'\ \hat{\mathbf{v}}'\ \hat{\boldsymbol{\delta}}'\right]^{\mathrm{T}} = -\mathbf{A}'^{-1}\left(\mathbf{u}^{\mathbf{g}}_{mn}\hat{g}_{mn} + \mathbf{u}^{\mathbf{b}}_{mn}\hat{b}_{mn}\right). \tag{2.5}$$

2.1.3 Perturbation in g and b

Equation (2.5) relates the bus parameters to incremental perturbations in g_{mn} and b_{mn} of the perturbed Line m-n and not directly to $\hat{x}_{mn}$ injected by the DSSC ($\hat{x}_{mn} = X_{inj}$, as used in Section 1.1.1). The complete solution is a proportional relationship between each bus parameter and $\hat{x}_{mn}$, so $\hat{g}_{mn}$ and $\hat{b}_{mn}$ must be expressed as functions of $\hat{x}_{mn}$. This relationship is derived using the same perturb-and-linearize method described for the bus operating points. Borrowing from (2.1):

$$y = \frac{r - jx}{r^2 + x^2}. \tag{2.6}$$

$\hat{y}$ is found by replacing r and x with their perturbed values and subtracting y:

$$\hat{y} = \hat{g} + j\hat{b} = \frac{r + \hat{r} - j\left(x + \hat{x}\right)}{\left(r + \hat{r}\right)^2 + \left(x + \hat{x}\right)^2} - \frac{r - jx}{r^2 + x^2}. \tag{2.7}$$

Simplifying, discarding higher-order terms, and separating the real and imaginary parts gives

$$\hat{g} = \frac{x^2 - r^2}{\left(x^2 + r^2\right)^2}\hat{r} - \frac{2rx}{\left(x^2 + r^2\right)^2}\hat{x} \tag{2.8}$$

$$\hat{b} = \frac{2rx}{\left(x^2 + r^2\right)^2}\hat{r} + \frac{x^2 - r^2}{\left(x^2 + r^2\right)^2}\hat{x}. \tag{2.9}$$

For an ideal DSSC, $\hat{r} = 0$, so (2.8) and (2.9) can be further rearranged to

$$\hat{g} = 2gb\hat{x} \tag{2.10a}$$

$$\hat{b} = \left(b^2 - g^2\right)\hat{x}. \tag{2.10b}$$

While these expressions use g and b, the actual physical values of the line admittance, it is preferred to use G and B, from the admittance matrix, for use in the full system solution. The conversion for this purpose is simple, as $gb = GB$, $g^2 = G^2$, and $b^2 = B^2$ in all cases. Therefore,

$$\hat{g} = 2GB\hat{x} \tag{2.11a}$$

$$\hat{b} = \left(B^2 - G^2\right)\hat{x}\,, \tag{2.11b}$$

which can be combined into

$$\mathbf{u}^{\mathbf{x}}_{mn} = 2G_{mn}B_{mn}\mathbf{u}^{\mathbf{g}}_{mn} + \left({B_{mn}}^2 - {G_{mn}}^2\right)\mathbf{u}^{\mathbf{b}}_{mn}. \tag{2.12}$$

Now, by substituting in (2.12) into (2.5), the solution to (2.4) to can be expressed in its final form:

$$\left[\hat{\mathbf{p}}'\ \hat{\mathbf{q}}'\ \hat{\mathbf{v}}'\ \hat{\boldsymbol{\delta}}'\right]^{\mathrm{T}} = -\mathbf{A}'^{-1}\mathbf{u}^{\mathbf{x}}_{mn}\hat{x}_{mn}\,. \tag{2.13}$$

The end result is that the system may be modeled by proportional relationships between the operating point perturbations and injected reactance on Line m-n, with coefficients given by the vector $-\mathbf{A}'^{-1}\mathbf{u}^{\mathbf{x}}_{mn}$.

2.1.4 Line current perturbations

The preceding method may also be applied to the line currents. The current on Line i-j is

$$\bar{I}_{ij} = y_{ij}\left(\bar{V}_i - \bar{V}_j\right). \tag{2.14}$$

Starting with ${I_{ij}}^2$, the procedure of Section 2.1.1 may be followed to derive the coefficients directly that relate line current magnitude to bus operating points and injected reactance (in this case, with $\hat{v}$ and $\hat{\delta}$ found, there is no need to solve for these coefficients as a matrix equation):

$$\hat{\imath}_{ij} = A^{iv}_{ij}\hat{v}_i + A^{iv}_{ji}\hat{v}_j + A^{i\delta}_{ij}\hat{\delta}_i + A^{i\delta}_{ji}\hat{\delta}_j + u^{ix}_{ij}\hat{x}_{ij}. \tag{2.15}$$

The full model, given by (2.13) and (2.15), shows that, depending on bus constraints, a perturbation to the reactance of Line m-n may cause a perturbation to the operating points of any

bus, even if that bus is not connected to Line m-n. It is reasonable to expect that the deployment of DSSCs on one line may change operating points throughout the system; likewise, DSSCs may be deployed on any and all lines to cause a desired change on one particular bus or line. On the other hand, the determination of which DSSCs to deploy and in what amount may not be intuitive, necessitating this analysis. See Appendix A for a detailed derivation of (2.15).

2.2 Three-Bus System Examples

This section gives a series of examples, using the three-bus system pictured in Fig. 2.1, of the method described in Section 2.1 and the benefits of DSSCs as introduced in Section 1.1.1: voltage correction, line current reduction, and generator reactive power reduction. The required change in line reactance is calculated for a given amount of correction to some system quantity.

2.2.1 Determining the linear coefficients

For the system of Fig. 2.1, Bus 2 and 3 are load (PQ) buses and Bus 1 is the generator/slack bus. The load flow solution is found with the open source power system simulation package MatPower, which uses the Newton-Raphson method to solve the system [32]. Table 2.1 shows the bus operating points, with the previously unknown, variable quantities in bold. Line impedance for the system is $z = (0.893 + j4.13) \times 10^{-3}$ p.u./mile. Table 2.2 gives the line lengths and resulting values

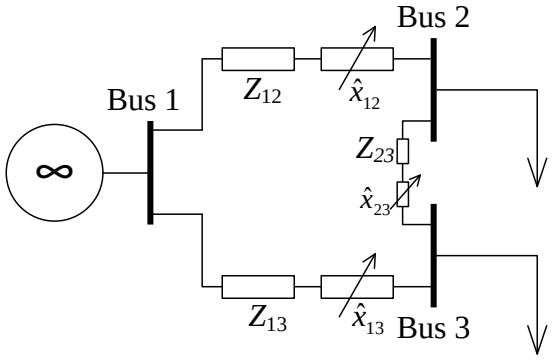


Figure 2.1: Example three-bus system with DSSCs on all lines

Table 2.1: Three-bus system unperturbed load flow solution

	P (p.u.)	Q (p.u.)	V (p.u.)	δ (deg.)
Bus 1	**0.978**	**0.579**	1	0
Bus 2	0.5	0.25	**0.926**	**-5.22**
Bus 3	0.45	0.20	**0.925**	**-5.35**

Table 2.2: Three-bus system line parameters ($z = (0.893 + j4.13) \times 10^{-3}$ p.u./mile)

	Length (mi)	G (p.u.)	B (p.u.)
Line 1-2	40	-1.24	5.76
Line 1-3	60	-0.826	3.84
Line 2-3	8	-6.19	28.8

for G and B.

Using the detailed process described in Appendix A, values are found for $\mathbf{A}$ and $\mathbf{u}^{\mathbf{x}}_{mn}$. Based on the bus constraints, the vector of incremental operating point changes is reduced to

$$\left[\hat{\mathbf{p}}'\ \hat{\mathbf{q}}'\ \hat{\mathbf{v}}'\ \hat{\boldsymbol{\delta}}'\right] = \left[\hat{p}_1\ \hat{q}_1\ \hat{v}_2\ \hat{v}_3\ \hat{\delta}_2\ \hat{\delta}_3\right].$$

Also, columns 2, 3, 5, and 6 are removed from $-\mathbf{I}_{2N}$, and columns 1 and 4 are removed from $\mathbf{A}$, so that

$$\mathbf{A}' = \begin{bmatrix} -1 & 0 & A^{pv}_{12} & A^{pv}_{13} & A^{p\delta}_{12} & A^{p\delta}_{13} \\ 0 & 0 & A^{pv}_{22} & A^{pv}_{23} & A^{p\delta}_{22} & A^{p\delta}_{23} \\ 0 & 0 & A^{pv}_{32} & A^{pv}_{33} & A^{p\delta}_{32} & A^{p\delta}_{33} \\ 0 & -1 & A^{qv}_{12} & A^{qv}_{13} & A^{q\delta}_{12} & A^{q\delta}_{13} \\ 0 & 0 & A^{qv}_{22} & A^{qv}_{23} & A^{q\delta}_{22} & A^{q\delta}_{23} \\ 0 & 0 & A^{qv}_{32} & A^{qv}_{33} & A^{q\delta}_{32} & A^{q\delta}_{33} \end{bmatrix}.$$

Following the rest of the procedure from Section 2.1 and repeating for each line, the coefficients presented in Table 2.3 are derived.

Table 2.3: Linear coefficients derived for three-bus system

	$\hat{p}_1$	$\hat{q}_1$	$\hat{v}_2$	$\hat{v}_3$	$\hat{\delta}_2$	$\hat{\delta}_3$
$\hat{x}_{12}$	0.014	0.52	-0.236	-0.214	-0.41	-0.362
$\hat{x}_{13}$	0.006	0.241	-0.097	-0.112	-0.164	-0.198
$\hat{x}_{23}$	0.0002	0.006	0.007	-0.013	0.028	-0.042

2.2.2 Voltage correction in a three-bus system

As Fig. 1.3 indicates, bus voltage drops with increasing load power up to a certain power level. Typically, system operators require the bus voltage to remain between 0.95p.u. and 1.05p.u. [34]. If DSSCs are already installed throughout the system, they may be deployed to prevent the load bus voltages from further deviating outside this range. As power electronics devices, they act quickly to restore the voltage as much as possible before other measures can be taken.

Table 2.1 indicates that both load buses are below 0.95p.u. According to Table 2.3, injecting reactance into Line 1-2 will have the biggest impact on V_2 and V_3. In order to add the necessary 0.025p.u. to V_3, the required change in X_{12} is simple to compute. From Table 2.3:

$$\hat{v}_3 = -0.214\hat{x}_{12},$$

so

$$\hat{x}_{12} = .025/(-0.214) = -0.119\,\text{p.u.}$$

Similarly, if X_{13} or X_{23} are used individually to raise V_3, then $\hat{x}_{13} = -0.227$p.u. or $\hat{x}_{23} = -2.04$p.u., respectively.

2.2.3 Graphical representation of system coefficients

In order to make these results more intuitive and accessible, Fig. 2.2 presents a graphical representation of the linear coefficients for the example given in Section 2.2.2. In Fig. 2.2, Bus 3 is highlighted to indicate that its voltage is the quantity of interest and colored blue to indicate that it should be raised. The arrows indicate how the line reactances may be changed to achieve that

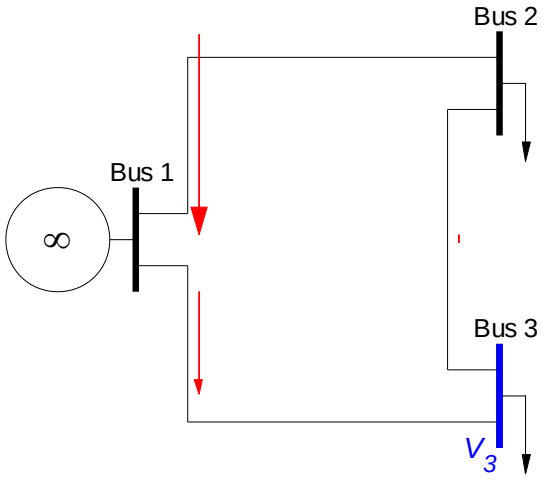


Figure 2.2: Graphical representation to illustrate raising Bus 3 voltage V_3 in the system of Fig. 2.1

goal. The size of an arrow (and arrowhead) is proportional to the magnitude of the coefficient that relates the reactance of the neighboring line to V_3. The arrow sizes are not absolute, but relative to each other for the specific compensation goal (raising V_3 in this case). The direction of the arrow indicates whether the reactance must be raised or lowered in order to raise V_3. For example, Fig. 2.2 shows that lowering X_{12} has the greatest impact on raising V_3, while changing X_{23}, the arrow for which is almost too small to be pictured, has almost no effect.

This graphical representation is especially useful for large systems. A complete system of linear coefficient values is best presented in a simple table (as in Table 2.3), but this would be exceedingly cumbersome and difficult to read for a system with large N. With a compensation goal already in mind, a diagram like Fig. 2.2 provides a simple and intuitive indication of how the line reactances relate to the system quantity of interest. Section 2.4 will use these diagrams in more detail.

2.2.4 Generator reactive power reduction in a three-bus system

As also mentioned in Section 1.1.1, control of line reactance using DSSCs may be useful to reduce generator reactive power. Consider, for example, that in the system of Fig. 2.1, the generator reactive power must be less than 0.5p.u. $Q_1 = 0.579$p.u., so $\hat{q}_1 = -0.079$p.u. If any

one of the line reactances is changed to achieve this goal, then Table 2.3 may be used to find the required individual values of $\hat{x}$:

$$\hat{x}_{12} = -0.079/0.52 = -0.152\text{p.u.}$$

$$\hat{x}_{13} = -0.079/0.241 = -0.327\text{p.u.}$$

$$\hat{x}_{23} = -0.079/.006 = -12.9\text{p.u.}$$

These results are intuitive: the DSSCs act as series capacitors to lower X, injecting Q into the system so that less is required from the generator.

2.2.5 Line current reduction in a three-bus system

As shown in the final example of Section 1.1.1, DSSCs may be used to reduce line current, especially in the case of an overload. In this example, the load on the system of Fig. 2.1 is increased (see Table 2.4) in order to demonstrate an overload condition. Using base values of 100MVA and 138kV, $I_{12} = 785$A, more than the 770A limit for a 138kV line [19]. Therefore, $\hat{\imath}_{12} = -15\text{A} = -0.037$p.u. The procedure given in Section 2.1.4 is followed to find the coefficients (for all lines) given in Table 2.5.

These results match intuition. Raising X_{12} and/or lowering X_{13} will redirect current from Line 1-2 to Line 1-3 and relieve the overload condition on Line 1-2. Also, since Line 2-3 is very short, changing X_{23} has little impact on line current relative to the other line impedances.

Table 2.4: Alternative three-bus system load flow solution for current overload

	P (p.u.)	Q (p.u.)	V (p.u.)	δ (deg.)
Bus 1	2.62	1.83	1	0
Bus 2	1.1	0.20	0.799	-15.92
Bus 3	1.3	0.60	0.785	-16.72

Table 2.5: Three-bus small signal line current coefficients in alternative overload case

	$\hat{\imath}_{12}$	$\hat{\imath}_{13}$	$\hat{\imath}_{23}$
$\hat{x}_{12}$	-1.28	1.55	-1.46
$\hat{x}_{13}$	1.06	-0.929	1.01
$\hat{x}_{23}$	-0.147	0.151	-0.153

2.3 Model Accuracy

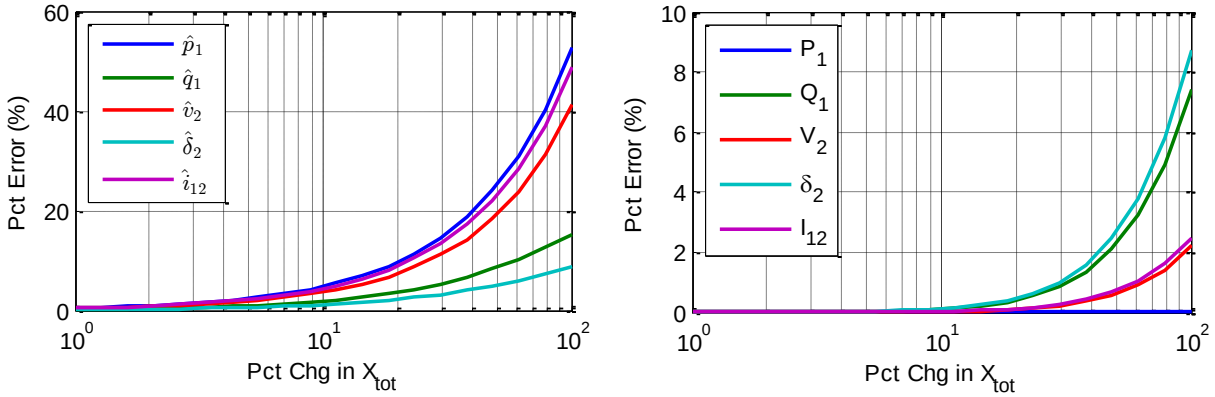
It is important to understand the limitations of the "small, incremental" conditions the model developed in Section 2.1 assumes. As a simple example, consider that in the case of the previous section it is desired to lower I_{12} far below the line current limit (770A). DSSCs may be deployed on all lines, and because the model is linear, their impact may simply be added by superposition. In other words,

$$\hat{\imath}_{12} = -1.28\hat{x}_{12} + 1.06\hat{x}_{13} - 0.147\hat{x}_{23} \tag{2.16}$$

according to Table 2.5. To keep to the assumption of small, incremental perturbation, let the change in reactance not exceed ±10% ($|\hat{x}_{ij}| \leq |X_{ij} \times \pm 10\%|$). By changing the line reactances by 10% in the appropriate direction ($\hat{x}_{12} = 0.017$p.u., $\hat{x}_{13} = -0.025$p.u., and $\hat{x}_{23} = 0.003$p.u.), the model predicts a new value of $I_{12} = 731$A. This is verified by repeating the load flow simulation with adjusted line impedances: MatPower gives a new system solution with $I_{12} = 726$A. The model error in the incremental change in current $\hat{\imath}_{12}$ is 8.5%, but the error in the final value for I_{12} is only 0.7%.

The two-bus system of Fig. 1.2 offers a more general understanding of the model accuracy. Fig. 2.3 shows a plot of the percent error in all the operating points of interest, comparing accuracy of the (a) predicted incremental change in operating point values and (b) the final values. Percent change in the total line reactance is given in log scale on the x-axis, while percent error is on the linear y-axis.

These figures show that, as expected, the model accuracy drops as the small, incremental change assumption is weakened. Still, in this example the error in the predicted final operating



(a) (b)

Figure 2.3: For two bus system, model prediction error in (a) incremental change in value and (b) final value vs. change in line reactance

point values (after the DSSCs have been turned on) is acceptably low ($\leq 3\%$) up to as high as a 50% change in line reactance.

However, these results only pertain to this two-bus example, in which the system is operating at a stable operating point (far to the left on a curve from Fig. 1.3). The model accuracy drops as the system becomes less stable, as illustrated in Fig. 2.4. In this case, the system is operating very close to P_{max}, far to the right on a curve from Fig. 1.3.

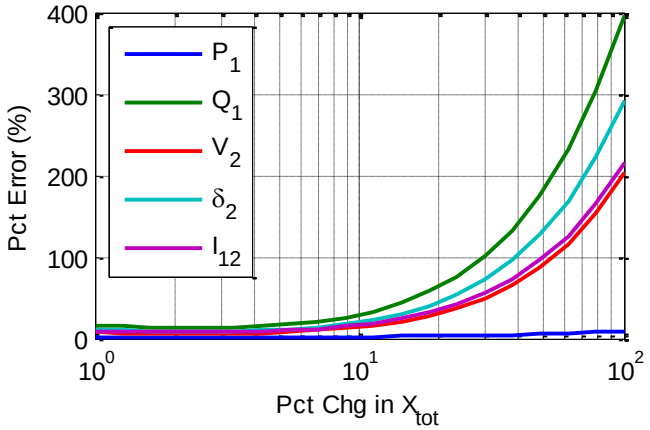


Figure 2.4: Model final value prediction error vs. change in line reactance for nearly unstable system

These results indicate that the model presented in this thesis is best suited for systems in or near normal operation. By the examples given in Section 2.2, DSSCs are most useful in stable situations where small adjustments are required. Bus voltage-out-of-range, line current overload, and generator reactive power overload are all problems that can occur without the entire system operating on the brink of instability, when more drastic measures are needed.

2.4 Nine-Bus System Examples

Extending the model to a larger system helps illustrate that DSSC deployment may lead to unintuitive results. In this section, the standard IEEE nine-bus test system (Fig. 2.5) is used, and the model results are analyzed with the graphical representation shown in Fig. 2.2. Table 2.6 shows the bus operating points for the nine-bus system in this example, with the previously unknown, variable quantities in bold.

As a first example, it is desired to lower the current in Line 2-8. Fig. 2.6 shows the graphical representation of the linear coefficients in this situation. Line 2-8 is colored pink to indicate that its current will be lowered. As in Section 2.2.3, each arrow is associated with its adjoining line.

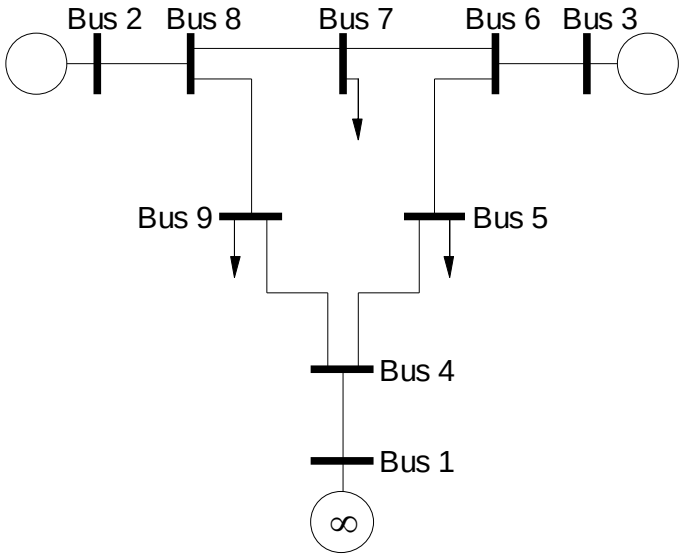


Figure 2.5: IEEE standard nine-bus test system

Table 2.6: Nine-bus system unperturbed load flow solution

	P (p.u.)	Q (p.u.)	V (p.u.)	δ (deg.)
Bus 1	**4.05**	**1.52**	1	0
Bus 2	1.63	**1.81**	1	**-23.3**
Bus 3	0.85	**1.58**	1	**-26.2**
Bus 4	0	0	**0.914**	**-9.72**
Bus 5	-0.9	-0.3	**0.881**	**-18.6**
Bus 6	0	0	**0.92**	**-27.6**
Bus 7	-4.0	-1	**0.829**	**-36.3**
Bus 8	0	0	**0.903**	**-26.9**
Bus 9	-1.0	-0.7	**0.857**	**-18.2**

The size of the arrow is proportional to the magnitude of the coefficient relating a change in the reactance of that line to a change in I_{28}. The direction of the arrow indicates whether the reactance should be raised or reduced in order to decrease I_{28}.

In this case, raising X_{28} has a significant effect on lowering I_{28}. This fits with expectations in that raising a line's impedance should reduce its current, as in Section 1.1.4. The model also

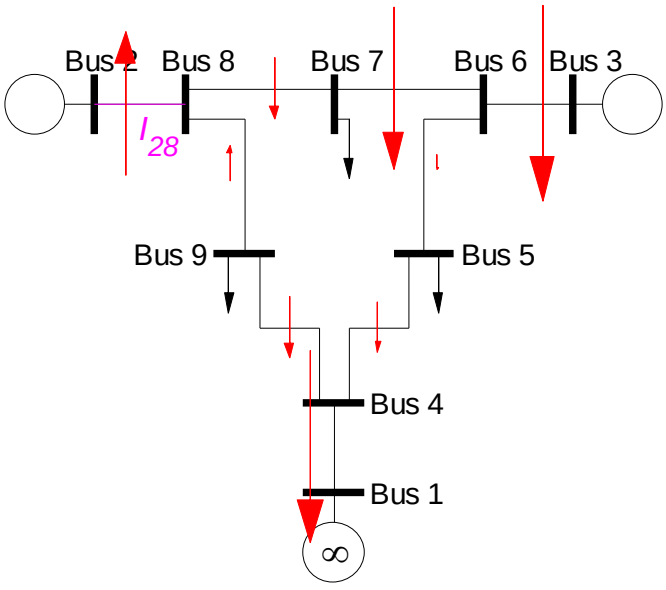


Figure 2.6: Graphical representation of DSSC effect on lowering I_{28}

shows that lowering the X_{14} or X_{36} will also have a large impact on I_{28}. This suggests that the current out of the generator on Bus 2 can be reduced by lowering other impedances to encourage the other generators to supply more reactive power to the system.

As a second example, it is desired to reduce the current on Line 1-4. Fig. 2.7 shows the graphical model results for this compensation goal. This case suggests, counterintuitively, the opposite effect from the previous example. Here, the current on Line 1-4 is decreased by *lowering* its own reactance. The model also indicates that lowering X_{14} raises V_4, decreasing the voltage drop across Z_{14} and lowering I_{14}.

As a final example, note that V_7 is very low. Fig. 2.8 shows the model results relating the line reactances to raising V_7. As explained in Section 1.1.2, lowering line reactance will raise load bus voltage, and Fig. 2.8 confirms that the reactances of the lines connected to Bus 7 should be lowered in this case. Unexpected here is that lowering the reactance of Line 2-8, which is not connected to Bus 7, has the largest impact on V_7. In other words, if the operator of this system needs to raise V_7, the first step should be to activate DSSCs on Line 2-8; using DSSCs on the lines connected to Bus 7 will have less effect. This would be difficult to predict without the linearized system model.

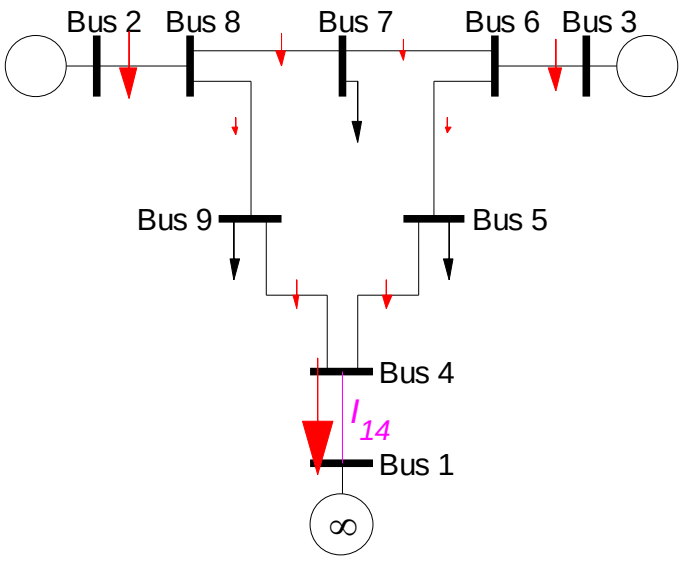


Figure 2.7: Graphical representation of DSSC effect on lowering I_{14}

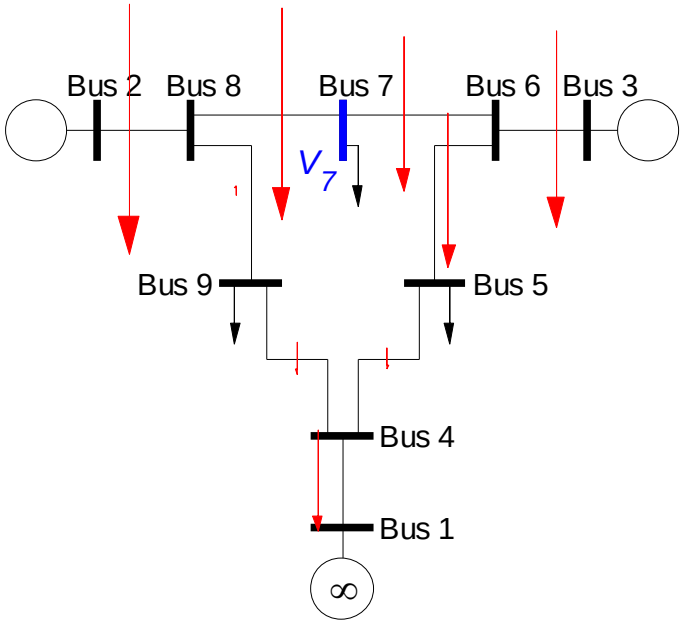


Figure 2.8: Graphical representation of DSSC effect on raising V_7

2.5 Line Efficacy

From the model of the preceding sections, it is apparent that some lines are more suitable for DSSC deployment by virtue of their relatively large coefficients. In order to facilitate deployment and real-time control of DSSCs, it is of interest to quantify all the coefficient magnitudes of the line collectively as the "line efficacy." It will be shown that, using the model from the previous section, efficacy can be represented as a positive, scalar value that is based on measurements local to the line and independent of the rest of the system. Efficacy can be compared for multiple lines using only the current and impedance on each line; the system load flow solution and knowledge of the system topology are not necessary.

Section 2.6 presents system examples illustrating the usefulness and limitations of efficacy measurements. It is shown how efficacy can be nearly as useful as the full linearized model to select lines for DSSC deployment, especially when considering the lines close to a bus of interest.

2.5.1 Deriving line efficacy

The line efficacy is derived from (2.13). It is desired to express incremental changes in operating points in terms of a single value related only to local line measurements. Note that $\mathbf{A}'$, which is computed using all the bus voltages, does not depend on m or n, where Line m-n is the line for which coefficients are being calculated (see Appendix A). On the other hand, $\mathbf{u}^{\mathbf{x}}_{mn}$ relies only on the voltage phasors of Bus m and n and the admittance of Line m-n, which are local measurements.

Let $\hat{\mathbf{f}}$ stand for any subset of $\begin{bmatrix}\hat{\mathbf{p}}' & \hat{\mathbf{q}}' & \hat{\mathbf{v}}' & \hat{\boldsymbol{\delta}}'\end{bmatrix}$. Substituting $\hat{\mathbf{f}}$ for the left side of (2.13) requires only the corresponding rows from $-\mathbf{A}'^{-1}$ to be used, which are denoted $\mathbf{A}_{\mathbf{f}}$:

$$\hat{\mathbf{f}}^{\mathrm{T}} = \mathbf{A}_{\mathbf{f}}\,\mathbf{u}^{\mathbf{x}}_{mn}\hat{x}_{mn}\,. \tag{2.17}$$

If the length of $\hat{\mathbf{f}}$ is M, then $\mathbf{A}_{\mathbf{f}}$ must be $M \times 2N$.

Next, each side of (2.17) is multiplied by its transpose and normalized by ${\hat{x}_{mn}}^2$, and the result is rearranged to:

$$\frac{\hat{\mathbf{f}}\hat{\mathbf{f}}^{\mathrm{T}}}{{\hat{x}_{mn}}^2} = {\mathbf{u}^{\mathbf{x}}_{mn}}^{\mathrm{T}}{\mathbf{A}_{\mathbf{f}}}^{\mathrm{T}}\mathbf{A}_{\mathbf{f}}\,\mathbf{u}^{\mathbf{x}}_{mn}\,. \tag{2.18}$$

The product ${\mathbf{A}_{\mathbf{f}}}^{\mathrm{T}}\mathbf{A}_{\mathbf{f}}$ is a $2N \times 2N$ symmetric matrix $\mathbf{H}$. $\mathbf{H}$ can be diagonalized:

$$\mathbf{H} = {\mathbf{A}_{\mathbf{f}}}^{\mathrm{T}}\mathbf{A}_{\mathbf{f}} = \mathbf{V}_H\mathbf{D}_H{\mathbf{V}_H}^{\mathrm{T}}\,, \tag{2.19}$$

where the eigenvectors of $\mathbf{H}$ ($\mathbf{v}_{H,1},\ \mathbf{v}_{H,2}$, etc.) form the columns of $\mathbf{V}_H$ and the eigenvalues of $\mathbf{H}$ ($\lambda_{H,1},\ \lambda_{H,2}$, etc.) are the diagonal elements of $\mathbf{D}_H$. $\mathbf{H}$ is positive definite, so its eigenvalues are real and non-negative. Substituting $\mathbf{H}$ into (2.18) and expanding gives:

$$\frac{\hat{\mathbf{f}}\hat{\mathbf{f}}^{\mathrm{T}}}{{\hat{x}_{mn}}^2} = \sum_{i=1}^{2N}\lambda_{H,i}\left({\mathbf{u}^{\mathbf{x}}_{mn}}^{\mathrm{T}}\mathbf{v}_{H,i}\right)^2\,. \tag{2.20}$$

Consider the minimum and maximum eigenvalues of $\mathbf{H}$: λ_{min} and λ_{max}, respectively. Substituting these into (2.20) bounds the value of $\hat{\mathbf{f}}\hat{\mathbf{f}}^{\mathrm{T}}$:

$$\lambda_{min}\sum_{i=1}^{2N}\left({\mathbf{u}^{\mathbf{x}}_{mn}}^{\mathrm{T}}\mathbf{v}_{H,i}\right)^2 \le \frac{\hat{\mathbf{f}}\hat{\mathbf{f}}^{\mathrm{T}}}{{\hat{x}_{mn}}^2} \le \lambda_{max}\sum_{i=1}^{2N}\left({\mathbf{u}^{\mathbf{x}}_{mn}}^{\mathrm{T}}\mathbf{v}_{H,i}\right)^2\,. \tag{2.21}$$

Because $\mathbf{V}_H$ represents a spanning set in $\mathbb{R}^N$, these bounds may be equivalently expressed as:

$$\lambda_{H,min}\mathbf{u}_{mn}^{\mathbf{x}\,\mathrm{T}}\mathbf{u}_{mn}^{\mathbf{x}} \leq \frac{\hat{\mathbf{f}}\hat{\mathbf{f}}^{\mathrm{T}}}{\hat{x}_{mn}{}^2} \leq \lambda_{H,max}\mathbf{u}_{mn}^{\mathbf{x}\,\mathrm{T}}\mathbf{u}_{mn}^{\mathbf{x}}\,. \tag{2.22}$$

(2.22) indicates how a set of system operating points changes with DSSCs deployed on a particular line. The term $\hat{\mathbf{f}}\hat{\mathbf{f}}^{\mathrm{T}}$ is the sum of squares of incremental changes in a particular quantity for all buses, broadly capturing the total effect of DSSC deployment on a system operating point:

$$\hat{\mathbf{f}}\hat{\mathbf{f}}^{\mathrm{T}} = \hat{q}_1{}^2 + \cdots + \hat{q}_N{}^2\,,\ \text{or}\ \hat{\mathbf{f}}\hat{\mathbf{f}}^{\mathrm{T}} = \hat{v}_1{}^2 + \cdots + \hat{v}_N{}^2\,,\text{etc.}$$

The eigenvalues bounds, λ_{min}, and λ_{max}, are derived from $\mathbf{A}'$, which is independent of the line under consideration. The bounds for $\hat{\mathbf{f}}\hat{\mathbf{f}}^{\mathrm{T}}/\hat{x}_{mn}$ scale with $\mathbf{u}_{mn}^{\mathbf{x}\,\mathrm{T}}\mathbf{u}_{mn}^{\mathbf{x}}$, leaving $\mathbf{u}_{mn}^{\mathbf{x}}$ as the only calculation necessary to estimate the efficacy of a line. Therefore, a figure of merit for the efficacy of Line m-n can be expressed as a positive, scalar value:

$$e_{mn} = \sqrt{\mathbf{u}_{mn}^{\mathbf{x}\,\mathrm{T}}\mathbf{u}_{mn}^{\mathbf{x}}} \tag{2.23}$$

The square root is used because (2.18), from which e is derived, is effectively the square of (2.17). Also, note that while (2.17) is a subset case of (2.13), the same value of $\mathbf{u}_{mn}^{\mathbf{x}}$ is used regardless of what $\hat{\mathbf{f}}$ stands for. Therefore, the value of e relates to the whole system, rather than specific system quantities.

2.5.2 Relating efficacy to line measurements

Using (2.12), efficacy can be expressed as

$$e_{mn} = \frac{I_{mn}\sqrt{V_m{}^2 + V_n{}^2}}{|z_{mn}|}\,. \tag{2.24}$$

Efficacy can be further approximated by noting that bus voltage magnitudes tend to operate near a nominal value (typically 1p.u.). Assuming $V \approx 1$p.u. for all buses,

$$e_{mn} \approx \frac{I_{mn}\sqrt{2}}{|z_{mn}|}\,. \tag{2.25}$$

Using (2.25) requires very few measurements. Assuming line impedances are known, lines may be compared for DSSC deployment based only on line current measurements, which can be

performed by the DSSCs locally. This is especially valuable because it does not require global knowledge of the network.

2.5.3 Limitations of line efficacy

It must be reiterated that local line measurements only provide bounds for $\hat{\mathbf{f}}\hat{\mathbf{f}}^{\mathrm{T}}$, and more information (i.e., a load flow solution) is needed to compute $\hat{\mathbf{f}}$ exactly. Therefore, efficacy is only a prediction, and conclusions based on efficacy may require further analysis. In particular, some knowledge of system topology may indicate when e is not accurate, as discussed in an example in the following section. Additionally, if it is possible to calculate λ_{min} and λ_{max} (if the values of $\mathbf{A_f}$ are known), the relative difference between the two indicates the width of the bounds on e.

Also, line reactance may need to be raised or lowered depending on the compensation goal. Efficacy pertains only to the relative *magnitude* of changes in line reactance. Because e is always positive, efficacy does not indicate whether DSSCs should emulate inductance or capacitance. Finally, as discussed in Section 2.3, just as the full linearized model, predictions based on the efficacy are limited by the assumptions of small, incremental changes and by the system stability.

2.6 14- and 30-Bus System Examples

This section presents more realistic application examples of the linearized model using the IEEE standard 14- and 30-bus systems [33]. The examples show the use of the full model and line efficacy to achieve the goals of generator reactive power reduction, voltage correction, and line current reduction.

2.6.1 Generator Reactive Power Reduction in a 14-Bus System

As a practical example, consider the IEEE 14-bus test network shown in Fig. 2.9. The system has five synchronous machines (generators) that sink or supply reactive power. Table 2.7 gives the reactive power processed by each generator, as well as the total reactive power injected from each generator (PV) bus into the network. The total reactive power supplied by the generators is 1.07p.u

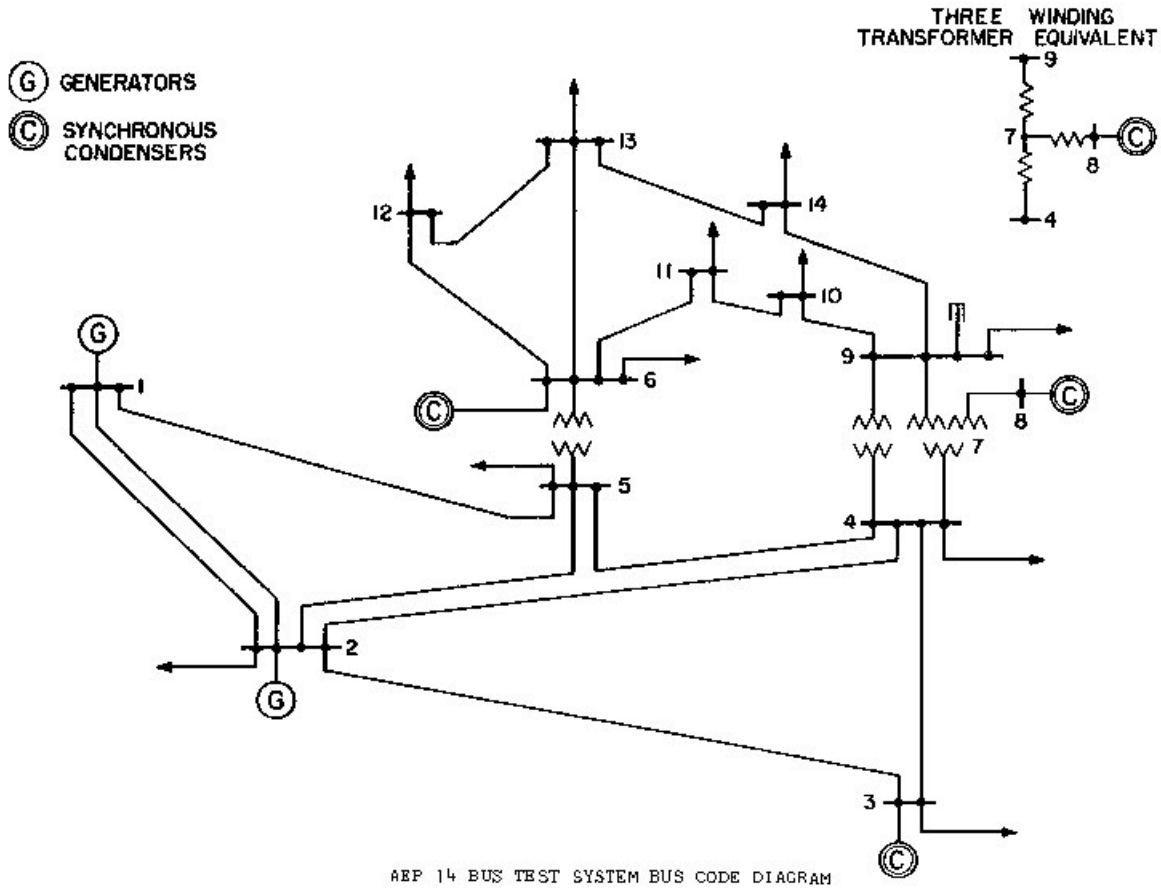


Figure 2.9: IEEE 14-bus test case [33]

(or 107MVAr, using a base power $S_{base,3\phi} = 100$MVA).

The generator on Bus 2 sources the most reactive power, so reducing Q_{gen2} may be a target for DSSC deployment. The coefficients that relate changes in line impedance to change in Q_2 may be found by first solving the system load flow, then by using the process developed in Section 2.1.

Table 2.7: Generator Reactive Power in 14-Bus System

Bus	1	2	3	6	8
Q_{gen} (p.u.)	-0.097	0.552	0.292	0.141	0.182
Q_{bus} (p.u.)	-0.097	0.425	0.102	0.066	0.182

DSSCs should be deployed where they are most effective, and for Q_2, the model indicates that Line 1-2 is best: $\hat{q}_2/\hat{x}_{12} = -3.7$, which is greater in magnitude than any other $\hat{q}_2/\hat{x}_{mn}$ coefficient. In order to lower Q_{gen2} by 5% ($\hat{q}_2 = -0.028$p.u.), for example, the required change in x_{12} is easily computed:

$$\hat{x}_{12} = \frac{\hat{q}_2}{-3.7} = \frac{-0.028}{-3.7} = 0.0075\text{p.u.} \tag{2.26}$$

The resulting estimated value of Q_{gen2} is 0.525p.u. Repeating the load flow analysis with the altered value of x_{12} gives $Q_{gen2} = 0.529$p.u., for an error of 0.8%.

The new load flow solution also gives the current through the activated DSSCs, $I_{12} = 1.491$p.u. The DSSCs emulate inductance, so the three-phase reactive power they absorb is:

$$Q_{DSSC,12} = {I_{12}}^2 \hat{x}_{12} = 0.017\text{p.u.} = 1.67\text{MVAr}, \tag{2.27}$$

while Q_{gen2} is reduced by 2.33MVAr. In this case, Q_{gen2} is reduced even when additional power is absorbed by Line 1-2 because the reactive power sunk by Bus 1 is also reduced. The effect on other generators cannot be neglected, and here the total generator Q output is in fact *increased* by 1.57MVAr.

This example shows once again that, for generator reactive power control, the effect of DSSCs may not be intuitive. Capacitive injected reactance may be expected to displace and decrease generator reactive power ($\hat{q}/\hat{x} > 0$), but a complex, highly meshed system may behave with the opposite effects. The linearized model is useful to identify conditions where $\hat{q}/\hat{x} < 0$ – decreasing generator Q by absorbing more reactive power on the line – which would otherwise be difficult to predict.

Rather than solve for the effects on one generator, it is possible to use multiple lines to reduce the total system Q. Choosing the five best lines, for example, for reactive power reduction on the five generators can provide an exact solution for the required change in line reactance. The best lines are chosen here by adding all $|\hat{q}/\hat{x}_{mn}|$ values for each generator. (While transformer branches are considered lines for the purpose of load flow analysis, they are disregarded from this model.)

Table 2.8 lists all the $\hat{q}/\hat{x}$ coefficients of the five best lines for Q reduction. They are Lines

Table 2.8: Coefficients relating selected five lines to five generators

	$\hat{q}_1$	$\hat{q}_2$	$\hat{q}_3$	$\hat{q}_6$	$\hat{q}_8$
$\hat{x}_{12}$	5.75	-3.70	0.043	0.020	0.015
$\hat{x}_{45}$	0.214	0.409	-0.317	0.129	-0.072
$\hat{x}_{15}$	-0.091	0.500	0.030	0.069	0.017
$\hat{x}_{34}$	0.021	0.201	-0.261	0.057	0.036
$\hat{x}_{23}$	0.069	-0.005	0.411	0.026	0.018

1-2, 4-5, 1-5, 3-4, and 2-3. Let $\mathbf{A}_q$ be Table 2.8 expressed as a matrix. Then:

$$[\hat{q}_1\ \hat{q}_2\ \hat{q}_3\ \hat{q}_6\ \hat{q}_8] = [\hat{x}_{12}\ \hat{x}_{45}\ \hat{x}_{15}\ \hat{x}_{34}\ \hat{x}_{23}]\,\mathbf{A}_q\,. \tag{2.28}$$

As before, it is desired to reduce each $|Q_{gen}|$ by 5%. Table 2.9 shows the solution to (2.28), as well as the desired reduced values of Q_{gen}, the actual new values of Q_{gen} based on the new load flow solution, the resulting error, and the power injected into the network by the DSSCs on each line. With these small changes to impedance and reactive power, the model accurately predicts that the total generator reactive power is reduced by 5.87MVAr. The total power processed (either absorbed or injected) by the DSSCs is 8.72MVAr.

If the load flow solution for this example is not available, line efficacy provides a good substitute. Based on only line current and impedance, the five highest efficacy values are $e_{12} = 33.9$, $e_{45} = 19.9$, $e_{23} = 4.9$, $e_{15} = 4.41$, and $e_{24} = 4.09$. Assume that available measurements (for example, with a perturb-and-observe algorithm) also indicate whether these DSSCs should emulate induc-

Table 2.9: Results for 5% reduction in all generator reactive power

	x_{12}	x_{45}	x_{15}	x_{34}	x_{23}
$\hat{x}$ (p.u.)	7×10^{-4}	0.034	-0.027	-0.128	-0.089
Q_{DSSC} (MVAr)	-0.152	-0.869	1.42	0.141	6.15
	Q_1	Q_2	Q_3	Q_6	Q_8
Desired (p.u.)	-0.093	0.525	0.277	0.134	0.173
Actual (p.u.)	-0.092	0.521	0.263	0.14	0.179
Error (%)	0.18	0.68	5.35	4.22	3.57

tance (Line 1-2) or capacitance (Lines 4-5, 2-3, 1-5, and 2-4), and that the units are commanded to some nominal change in line reactance. For $\hat{x} = x \times 20\%$ on each line, the total Q saved from all generators is 3.69MVAr, and the total VAr processed by the DSSCs is 8.56MVAr . This result is on the same scale as with the full model, indicating that efficacy measurements are useful for reactive power reduction.

2.6.2 Voltage Correction in a 14-Bus System

Typically, system operators require the bus voltage to remain between 0.95p.u. and 1.05p.u. [34]. In this case, the voltage of Buses 9, 11, and 12 are out of range: $V_9 = V_{12} = 1.055$p.u. and $V_{11} = 1.057$p.u. Selecting the three best lines for voltage correction provides an exact solution for required $\hat{x}$.

By summing the $\hat{x}/\hat{v}$ magnitudes for each line, the best lines for voltage correction are Lines 4-5, 6-13, and 9-10. Table 2.10 gives the coefficients that relate these lines to the out-of-range load buses. The required $\hat{x}$ values to reduce these voltages to 1.05 may be computed exactly by expressing Table 2.10 as a matrix. The results are given in Table 2.11.

The small magnitudes of the values in Table 2.10 indicate that DSSCs have a weaker impact on bus voltages than on generator reactive power. Indeed, previous work on series compensators has shown that they are best-suited for power flow control rather than voltage regulation [11,19,22–25]. The results confirm this, as the required injected reactance values $\hat{x}_{45}$, $\hat{x}_{613}$, $\hat{x}_{910}$, etc. are an order of magnitude larger than in the example of Section 2.6.1 (see Table 2.9). These $\hat{x}$ values are also large relative to their respective line impedances, increasing the model error such that one bus

Table 2.10: Coefficients relating selected three lines to load bus voltages

	$\hat{v}_9$	$\hat{v}_{11}$	$\hat{v}_{12}$
$\hat{x}_{45}$	-0.0041	-0.0054	0.0014
$\hat{x}_{613}$	-0.0062	-0.0033	-0.014
$\hat{x}_{910}$	0.0068	-0.0139	0.0003

Table 2.11: Results for voltage correction to Buses 9, 11, and 12

	x_{45}	x_{613}	x_{910}
$\hat{x}$ (p.u.)	0.712	0.442	0.087
Q_{DSSC} (MVAr)	-1.67	-0.61	-0.04
	V_9	V_{11}	V_{12}
Desired (p.u.)	1.05	1.05	1.05
Actual (p.u.)	1.048	1.051	1.049
Error (%)	0.15	0.05	0.14

remains out of range. On the other hand, the DSSC reactive power (2.32MVAr total) is on the same scale as in the previous example, suggesting that roughly the same number of DSSC units are necessary for voltage correction, provided large enough DSSC voltage limitations to allow such high emulated impedance.

In general, lines tend to have a relatively large effect on the voltage of buses to which they are connected. Also, lines connected to one generator, but not two, typically have a relatively large impact on the voltage of nearby buses. Efficacy measurements can make useful predictions when applied locally, ignoring lines connecting two generators. More broadly, the model and the efficacy measurements indicate lines for DSSC deployment equally well.

It is also necessary to determine whether inductive or capacitive injected reactance is required. With traditional compensation devices, reactive power is injected into the network to raise voltage and absorbed to lower voltage. Likewise with DSSCs, most $\hat{v}/\hat{x}$ coefficients are negative. However, the linearized model can reveals counterintuitive cases where $\hat{v}/\hat{x} > 0$. For example, the voltage on Bus 4 is most effectively lowered by decreasing the reactance on Line 4-5. The model predicts this effect with the coefficient $\hat{v}_4/\hat{x}_{45} > 0$.

2.6.3 Line Current Reduction in a 30-Bus System

This example considers line currents in the IEEE 30-bus test case system shown in Fig. 2.10. In [19, 22–25], DSSCs are introduced for current overload applications, and reducing line currents

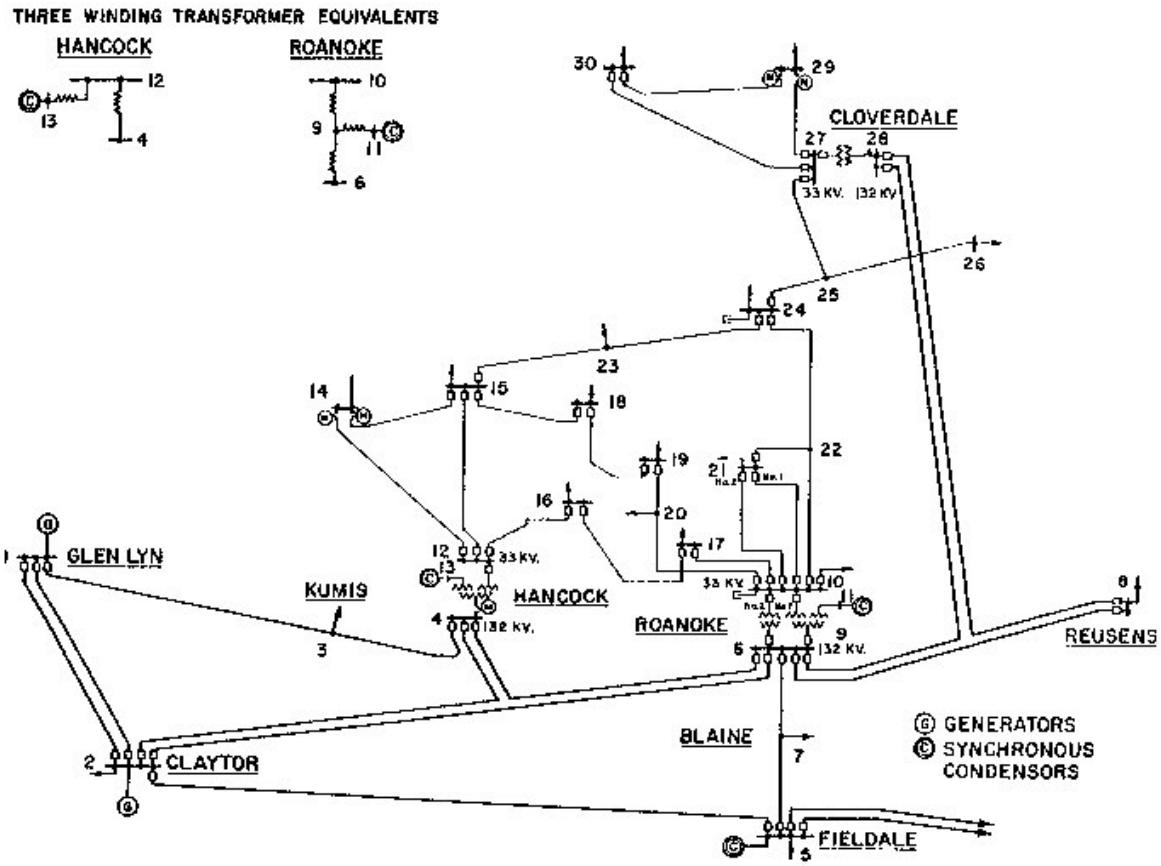


Figure 2.10: IEEE 30-bus test case [33]

also improves system efficiency. In this example, Lines 1-2, 10-21, and 12-15 are nearly overloaded, based on 132kV (Line 1-2) and 33kV (Lines 10-21 and 12-15) base voltages and $S_{base,3\phi} = 100$MVA.

DSSCs are typically most effective in reducing their own line current. In order to lower these three currents by 20%, $\hat{x}$ is calculated separately for each line, and the results are given in Table 2.12. The DSSCs relieve multiple overload conditions by absorbing a total of about 13MVAr.

In general for a highly meshed network, current on a line may be reduced by raising the impedance on that line and lowering the impedance on a neighboring line. Efficacy can be used to determine which neighboring lines are most effective. For example, to reduce I_{12}, the neighbor of Line 1-2 with the highest efficacy, Line 1-3, also has the highest $\hat{\imath}/\hat{x}$ coefficient. Efficacy also

Table 2.12: Results for current reduction in 30-bus system

	x_{12}	x_{1021}	x_{1215}
$\hat{x}$ (p.u.)	0.066	0.055	0.1
Q_{DSSC} (MVAr)	-12.9	-0.126	-0.24
	I_{12}	I_{1021}	I_{1215}
Initial (A_{rms})	721	314	318
Desired (A_{rms})	577	251	254
Actual (A_{rms})	612	265	271
Error (%)	5.7	5.4	6.2

correctly predicts the best neighboring line for I_{1215}. To reduce I_{1021}, the model predicts that Line 10-22 is the most effective neighbor of Line 10-21, while efficacy measurements suggest Line 21-22. If the x_{1021} is increased by 20% and the neighboring x is decreased by 20%, the model predicts a $31A_{rms}$ reduction in I_{1021} with 6% error, and using efficacy produces an $18A_{rms}$ reduction in I_{1021} with 9% error. The actual new current values are $267A_{rms}$ and $271A_{rms}$ using x_{1022} and x_{2122}, respectively. These results disagree, but the practical difference is small: using efficacy to choose DSSCs for current reduction produces a significant benefit. When a line has no neighbor, as with Line 25-26, it may be necessary to *lower* the impedance of the line, perhaps counterintuitively. This will decrease the voltage drop across the line, causing the current to drop. The linearized model confirms this, as $\hat{\imath}_{2526}/\hat{x}_{2526} > 0$.

Chapter 3

DSSC Operation and Design Principles

As the examples of Chapter 2 indicate, the benefit of DSSCs for their compensation applications increases with the magnitude of injected reactance. In other words, it is desired to maximize the capacity for injected reactance. This can be done most directly by adding more DSSC units to a line. But a less costly approach would be to maximize the reactance capability of the individual units. This can be achieved with an active DSSC design that uses a voltage source inverter to emulate reactance. This thesis presents a method for increasing the reactance capabilities further by controlling the VSI with a constant duty cycle.

3.1 Emulated Reactance and Injected Reactance

The basic passive DSSC design has a switch on the secondary side of the single turn transformer, and it is only capable of injecting a single, fixed value of inductive reactance $X_m = \omega_\ell L_m$. Reactance X_e may be added to the secondary side to interact with X_m, as in Fig. 3.1, potentially allowing the DSSC to emulate capacitance or inductance. X_e and X_m are in parallel through the transformer, so the total injected reactance is

$$X_{inj} = \frac{X_e X_m}{X_e + n^2 X_m}. \tag{3.1}$$

For a desired value of X_{inj}, then, the required X_e is

$$X_e = \frac{n^2 X_m X_{inj}}{X_m - X_{inj}}. \tag{3.2}$$

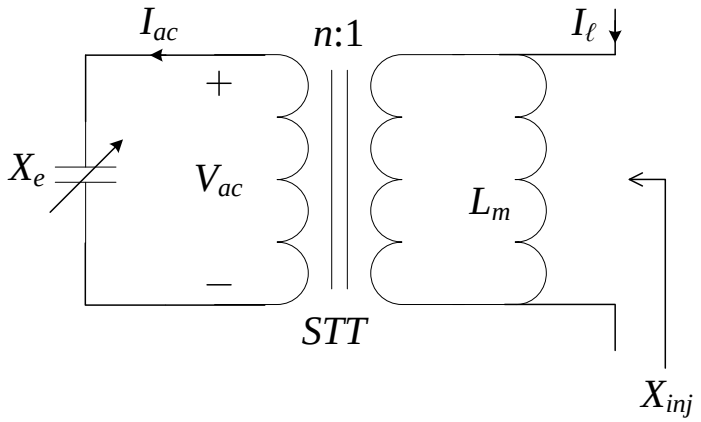


Figure 3.1: DSSC with emulated reactance X_e

Fig. 3.2 shows the relationship between X_e and X_{inj}. There are three regions of operation: X_e is capacitive and X_{inj} is inductive (pink); X_e is capacitive and X_{inj} is capacitive (red); X_e is inductive and X_{inj} is inductive (blue). By emulating capacitance exclusively, it is possible to achieve $|X_{inj}| > X_m$.

The advantage of capacitive X_e would be most easily achieved with one or more capacitors on the secondary side of the STT. Multiple capacitors, activated with switches, would allow the

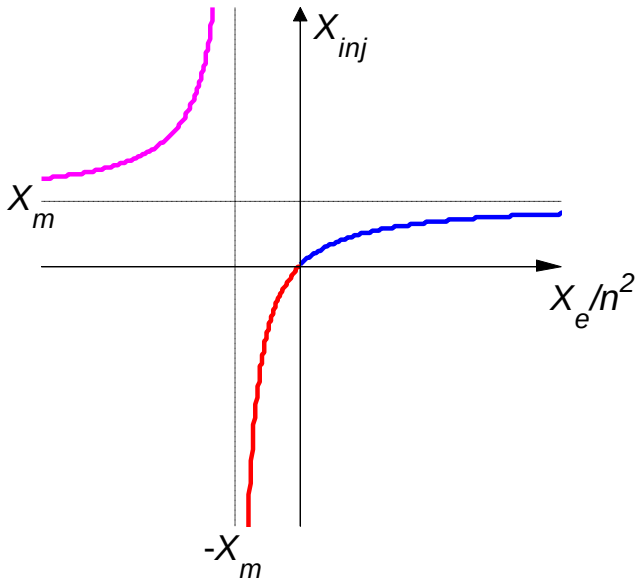


Figure 3.2: Injected reactance X_{inj} vs. emulated reactance X_e

DSSC to operate on either side of the vertical X_m asymptote in Fig. 3.2. However, this would suffer the same drawback as the basic passive design, in that the DSSC reactance would be fixed for any value of transmission line current.

An active design using a voltage source inverter (VSI) on the secondary side can greatly improve the functionality of the DSSC. Upon measuring the line current, the device can automatically set its operating point to maximize X_{inj}. For example, consider an active DSSC design where $X_{inj} = 2X_m$ at the maximum rated current of the transmission line $I_{\ell,max}$. It is possible that, at a value of $I_\ell < I_{\ell,max}$, the VSI may be controlled so that $X_{inj} > 2X_m$. This improves the performance of the DSSC so that the compensation benefits from Chapters 1 and 2 can be maximized using fewer total devices in the system.

The VSI may alternatively be considered a voltage source, which is controlled to some desired magnitude and with a phase $\pm 90°$ relative to I_ℓ. Fig. 3.3 shows the relationship between the injected voltage magnitude – reflected to the secondary side of the STT – V_{ac} and X_e. The figure also labels the phase of the voltage for each operating region. As will be discussed in subsequent sections, the primary limiting factor for the DSSC operation is a maximum voltage; Fig. 3.3 indicates how that

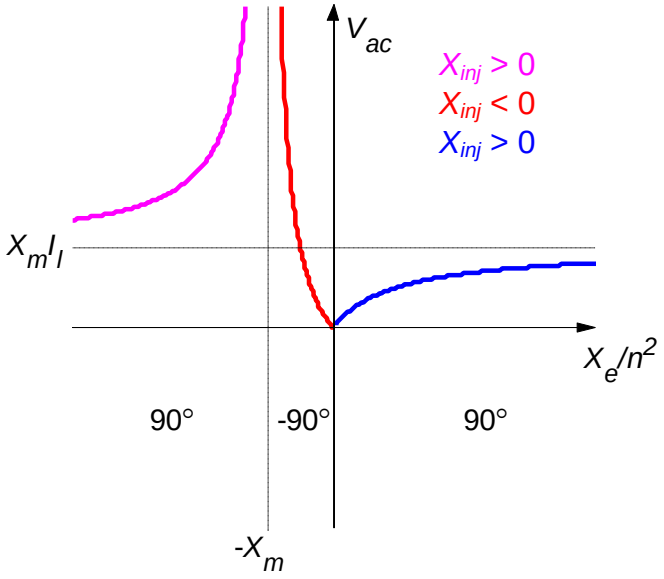


Figure 3.3: Injected voltage V_{ac} vs. emulated reactance X_e

limit relates to X_e and in turn to X_{inj}.

This thesis presents a VSI using two control schemes: conventional sinusoidally pulse-width modulated (SPWM) control and constant duty cycle control, a new contribution. This chapter presents the operating principles of the DSSC VSI, a general approach to designing the STT and VSI, and comparison of SPWM control and constant duty cycle control.

3.2 Basic DSSC Operation Principles

3.2.1 DC-side ripple

First, it is necessary to understand the relationship between the dc- and ac-side switching-average signals. It assumed for this analysis that the VSI includes a filter (likely an LC filter – see Chapter 4) that sufficiently attenuates current and voltage components at and above the switching frequency f_{sw}, while having no effect at the line frequency f_ℓ.

In the case of SPWM control, the dc side will have some constant average voltage V_{dc} with some ripple signal $v_r(t)$. The ripple is due to the need to balance the time varying ac side power, and it oscillates at twice the line frequency $2\omega_\ell$. The ripple signal magnitude may be derived based on this balance.

Consider an inverter operating with ac-side voltage and current signals:

$$v_{ac}(t) = V_{ac}\sqrt{2}\sin(\omega_\ell t) \tag{3.3}$$

and

$$i_{ac}(t) = \frac{|S_{ac}|}{V_{ac}}\sqrt{2}\sin(\omega_\ell t + \phi), \tag{3.4}$$

respectively, where S_{ac} is a fixed complex power and ϕ is the phase offset. The instantaneous ac-side power is the product of the output voltage and current:

$$p_{ac}(t) = v_{ac}(t)\, i_{ac}(t), \tag{3.5}$$

which reduces by trigonometric identities to

$$p_{ac}(t) = |S_{ac}|\cos(\phi) - |S_{ac}|\cos(2\omega_\ell t + \phi) = P_{ac} - |S_{ac}|\cos(2\omega_\ell t + \phi). \tag{3.6}$$

Equation 3.6 indicates that, as expected, the instantaneous ac-side power consists of the real power plus a time-varying component.

Assuming the VSI is ideal, the dc-side power $p_{dc}(t) = p_{ac}(t)$, with both a constant real power and a time-varying component. Assume that C_{dc} sufficiently suppresses the switching ripple on the dc side, so that $i_{dc}(t) \approx \langle i_{dc}(t) \rangle_{Tsw}$. If it is also assumed that $V_r \ll V_{dc}$, then the dc-side current is the instantaneous power divided by V_{dc}:

$$i_{dc}(t) = \frac{p_{dc}(t)}{V_{dc}} = \frac{1}{V_{dc}}(P_{ac} - |S_{ac}| \cos(2\omega_\ell t + \phi)). \tag{3.7}$$

Again, this current has a dc component, which must come from a dc source (e.g. PV panel) and a time-varying component, which must come from the dc link capacitor:

$$i_c(t) = -\frac{|S_{ac}|}{V_{dc}} \cos(2\omega_\ell t + \phi). \tag{3.8}$$

Integrating $i_c(t)$ and dividing by the dc link capacitance gives an expression for the dc bus ripple:

$$v_r(t) = \frac{1}{C_{dc}} \int i_c(t)\, \mathrm{d}t = const - \frac{|S_{ac}|}{2\omega_\ell V_{dc} C_{dc}} \sin(2\omega_\ell t + \phi), \tag{3.9}$$

where the constant is V_{dc}. Therefore, the dc ripple magnitude is

$$V_r = \frac{|S_{ac}|}{2\omega_\ell V_{dc} C_{dc}}. \tag{3.10}$$

3.2.2 SPWM Control

The energy stored by the VSI varies with time. In order to emulate a reactance X_e, the VSI must store a peak quantity of energy E_{req} twice per line cycle. This energy can be expressed as:

$$E_{req} = \frac{V_{ac} I_{ac}}{\omega_\ell}. \tag{3.11}$$

For the DSSC application, this energy is transferred to and from the dc-side capacitor C_{dc}. The selection of C_{dc} is central to the overall design, and it is desired to minimize the size of the capacitor both to reduce system cost and to improve reliability. Under SPWM control, the capacitor is chosen with the appropriate voltage rating for the desired dc-side voltage V_{dc} and sized to limit the dc-side

$2\omega_\ell$ voltage ripple. As a result, the energy storage available in C_{dc} is a function of the dc-side voltage:

$$E_{dc} = \frac{2C_{dc}{V_{dc,max}}^2 r}{(1+r)^2}, \tag{3.12}$$

where $V_{dc,max}$ is the maximum voltage allowed across C_{dc}, and r is the magnitude of the voltage ripple as a fraction of V_{dc}:

$$r = \frac{V_{dc,max} - V_{dc}}{V_{dc}}. \tag{3.13}$$

3.2.3 Constant duty cycle control

In order to provide a high injected series reactance, it is desired for V_{ac} to be as high as possible for a given input current, necessitating as much energy stored in C_{dc} as possible. In common VSI applications, where the dc port is a real power source at a fixed dc voltage (such as a battery or PV panel), it is also desired to limit the ripple magnitude, which limits the performance of the VSI under SPWM control. The DSSC application, however, supplies no real power and does not require a fixed dc voltage. Therefore, the energy available from C_{dc} may be increased by allowing a larger ripple.

As shown in Fig. 3.4, when $X_e < 0$, the troughs of the ripple waveform align with the

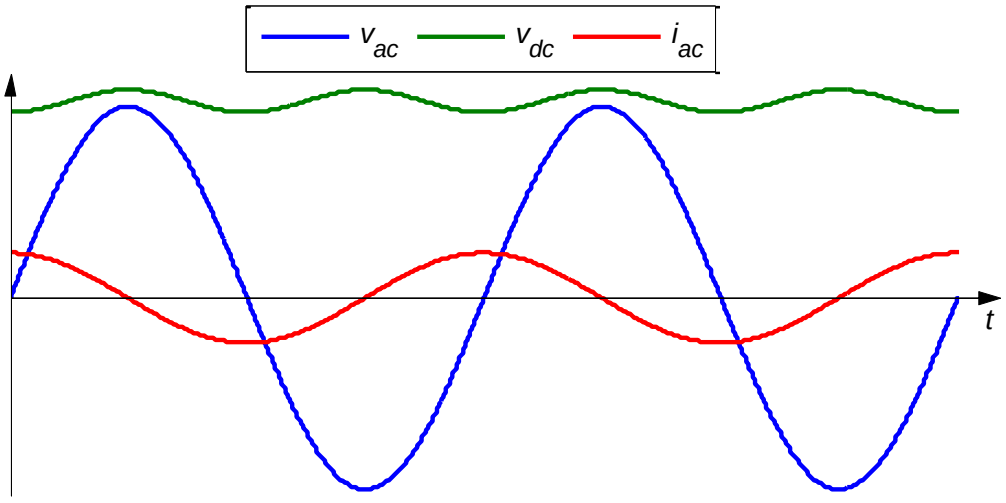


Figure 3.4: VSI signals for capacitive operation

zero-crossings of the $v_{ac}(t)$. If the ripple is increased until the dc-side voltage reaches zero, the VSI may still produce a sinusoidal waveform by simply operating at constant duty cycle. The resulting dc-side voltage waveform becomes a rectified sinusoid that follows the VSI ac-side voltage. The available energy is increased because $r = 1$ and the capacitor voltage sweeps the full range of voltage between 0 and $V_{dc,max}$, so

$$E_{dc} = \tfrac{1}{2} C_{dc} {V_{dc,max}}^2, \tag{3.14}$$

which is a factor of

$$\frac{(1+r)^2}{4r} \tag{3.15}$$

greater than with SPWM control.

3.3 Full DSSC Design

It is necessary to consider the STT together with the VSI in order to design the complete DSSC system. For this work, the design variables of the STT are the magnetizing inductance L_m, which is referenced to the primary side of the STT, and the number of secondary side turns n. A complete design using constant duty cycle control, including the value of C_{dc} and the duty cycle required for a given X_{inj}, may be determined iteratively in several steps.

3.3.1 DSSC design process

STEP 1: Determine the maximum line current $I_{\ell,max}$, the maximum dc-side capacitor voltage $V_{dc,max}$, the desired injected inductive reactance X_{des} at $I_{\ell,max}$, and L_m. $I_{\ell,max}$ should be known based on the nominal voltage level of the transmission line where the DSSC will be deployed (e.g., 138 kV system) [23]. A preliminary value of $V_{dc,max}$ may be chosen from among typical values of capacitor and power semiconductor component ratings. It is in the designer's judgment to select a value that balances performance and cost; common values are in the range of hundreds of volts.

A value of X_{des} may be arbitrarily chosen, provided the functionality of the VSI is leveraged

so that $X_{des} > \omega_\ell L_m$. Inductive operation ($X_{des} > 0$) is preferred because the purpose of the active DSSC design is to produce a reactance greater than the magnetizing inductance alone. On the other hand, any amount of capacitive reactance represents an improvement over the passive design.

Finally, the value of L_m is based on the design of the STT core, as detailed in [25]. It is desired to achieve a large value of L_m while minimizing the STT size and weight.

STEP 2: Find n. The design goal is to achieve X_{des} at $I_{\ell,max}$ and $V_{ac}\sqrt{2} = V_{dc,max}$, where the duty cycle $D = 1$. Therefore,

$$n = \frac{V_{dc,max}}{X_{des} I_{\ell,max} \sqrt{2}}. \tag{3.16}$$

n must be rounded to an integer value; whether it is rounded up or down may depend on subsequent steps.

STEP 3: Find the required dc-side stored energy. First, consider the reactive power processed by the system components: the total reactive power of the DSSC Q_{DSSC}, the reactive power absorbed by the magnetizing inductance Q_m, and the reactive power injected by the VSI Q_{req}. For an ideal system,

$$Q_{DSSC} = Q_m + Q_{req}, \tag{3.17}$$

where $Q > 0$ represents absorbed VAr. Then:

$$Q_{req} = V_{ac} I_{ac} = \frac{V_{ac} I_\ell}{n} - \frac{{V_{ac}}^2}{n^2 \omega_\ell L_m}. \tag{3.18}$$

Q_{req} is the magnitude of the time-varying power required from the VSI, and by the convention stated above, $Q_{req} < 0$. The expression for the required time-varying power is $p_{req}(t) = -V_{ac} I_{ac} \sin(2\omega_\ell t + \phi)$, which may be integrated to find the time-varying energy required from the VSI:

$$e_{req}(t) = -\frac{V_{ac} I_{ac}}{\omega_\ell} \left[1 + \tfrac{1}{2} \cos(2\omega_\ell t + \phi)\right]. \tag{3.19}$$

The integration constant is set so that $e_{req}(t)$ never reverses its sign, and the peak VSI stored energy E_{req} is the same as in (3.11). If the VSI is lossless and transmits the full amount of energy

available in C_{dc} (from (3.12) or (3.14)), then

$$E_{dc} = -E_{req} = \frac{1}{\omega_\ell}\left(\frac{{V_{dc,max}}^2}{2n^2\omega_\ell L_m} - \frac{V_{dc,max}I_{\ell,max}}{n\sqrt{2}}\right). \tag{3.20}$$

E_{dc} is the energy C_{dc} must store in order for the DSSC to inject X_{des}.

STEP 4: Determine if component current ratings are exceeded. While the VSI filter must be incorporated for a full analysis of the system currents, a preliminary value of the maximum current magnitude can be determined from E_{req}. From (3.11):

$$I_{ac,max} = \frac{2E_{req}\omega_\ell}{V_{dc,max}}. \tag{3.21}$$

$I_{ac,max}$ may be lowered by raising n at the cost of reduced performance (lower X_{des}). However, there is a limit to n if the active design is to improve on the inductive performance of the passive design. From (3.16):

$$n < \frac{V_{dc,max}}{\omega_\ell L_m I_{\ell,max}\sqrt{2}}. \tag{3.22}$$

STEP 5: Find the required capacitor value. This is the step where SPWM control is distinguished from constant duty cycle control. Given $V_{dc,max}$, E_{dc} from (3.20), and r if necessary, C_{dc} is easily calculated from (3.12) or (3.14):

$$C_{dc} = \frac{E_{dc}\,(1+r)^2}{2{V_{dc,max}}^2 r} \tag{3.23}$$

under SPWM control; or

$$C_{dc} = \frac{2E_{dc}}{{V_{dc,max}}^2} \tag{3.24}$$

under constant duty cycle control, respectively.

STEP 6: Find the duty cycle for constant duty cycle control. For this step, it is useful to approximate the VSI as a transformer with a D:1 turns ratio (assuming three-level switching; with two-level switching this would be $(2D-1)$:1). X_e can be expressed using the duty cycle and capacitor:

$$X_e = -\frac{D^2}{\omega_\ell C_{dc}}. \tag{3.25}$$

Any desired value of X_{inj}, either inductive or capacitive, is the parallel combination of X_e and $\omega_\ell L_m$ through the STT. The parallel sum can be rearranged to find an expression for D:

$$D = n\omega_\ell \sqrt{\frac{L_m C_{dc} X_{inj}}{X_{inj} - \omega_\ell L_m}}. \tag{3.26}$$

The asymptote at which the DSSC operates as an open circuit occurs for $D = n\omega_\ell\sqrt{L_m C_{dc}}$. For $D > n\omega_\ell\sqrt{L_m C_{dc}}$, the DSSC emulates an inductor. For $D < n\omega_\ell\sqrt{L_m C_{dc}}$, the DSSC emulates a capacitor.

3.3.2 Capacitive DSSC operation

This design process does not explicitly regard capacitive operation because it is more important to justify the presence of the VSI by maximizing the inductive performance. Capacitive operation is important, but this work considers it an added benefit of the active DSSC. Certainly a different design process is necessary to optimize capacitive operation.

Neglecting the VSI component ratings, the maximum capacitive value of X_{inj} should be achieved when the VSI supplies all of E_{dc} and is controlled so that V_{ac} lags I_ℓ. The maximum value of V_{ac} can be found from (3.18) by converting from Q_{req} to E_{dc} and solving for V_{ac}:

$$V_{ac} = \tfrac{1}{2} n\omega_\ell L_m I_\ell \left(1 \pm \sqrt{1 + \frac{4E_{dc}}{L_m {I_\ell}^2}}\right), \tag{3.27}$$

then $X_{inj} = V_{ac}/(nI_\ell)$. The positive solution to (3.27) is the inductive case, and the negative solution is the capacitive case. The resulting VSI current is

$$I_{ac} = \frac{E_{dc}\omega_\ell\sqrt{2}}{V_{ac}}. \tag{3.28}$$

In the capacitive case, the DSSC injects reactive power into the transmission system, so the VSI must supply that amount plus the reactive power absorbed by L_m. Consequently, the VSI current for the maximum capacitive case is higher than for the maximum inductive case. The maximum capacitive reactance may be limited more by the VSI component ratings than by available energy in C_{dc}, depending on I_ℓ. Alternatively, inductive performance may be sacrificed to reduce the system current by raising n.

3.3.3 VSI filter design

The VSI requires a filter on its ac side to attenuate the significant switching components of v_{ac}. The filter must also be designed so that it has no effect on the line frequency signals. In other words, the filter must act as a short circuit at f_ℓ and an open circuit at and above f_{sw}.

The VSI acts as a controllable voltage source connected in series with a transmission line, which acts as a fixed current source. Whereas an LCL filter, as in Fig. 3.5, is typical for grid tied inverters [35], only an LC filter, as in Fig. 3.6, is necessary for the DSSC application. The voltage transfer function v_{ac}/v_{sw} is not dependent on L_g, and the connection of L_g in series with a current source may cause unwanted voltage spikes. Figs. 3.5 and 3.6 also show the damping resistor R_f, which is necessary to prevent resonance between C_f and L_i.

The exact design of the filter depends on the VSI operating points and switching frequency. Sections 3.1-3.3.2 regard the design and behavior of the device at the line frequency and assume that the filter may be neglected. Details of the filter implemented for this thesis are based on [35] and are discussed in Chapter 4. Specific details of the VSI implementation are also used in the following section on power loss.

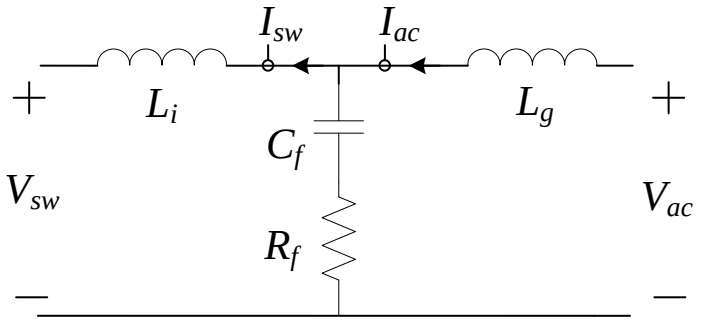


Figure 3.5: LCL filter schematic

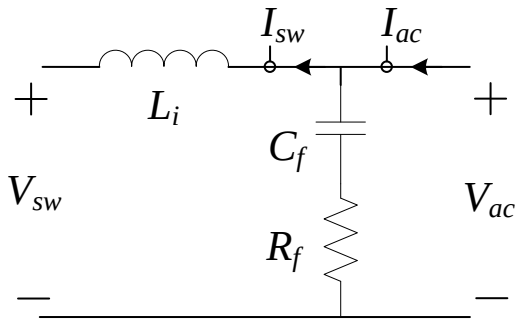


Figure 3.6: LC filter schematic

3.3.4 Design example

Iterations on a basic active SPWM design have been presented in [19, 23, 25]. In [25], details of an STT design are presented: the core, in the shape of a cylindrical annulus, is chosen to achieve $L_m \approx 50$ μH with the least possible weight while still fitting around the transmission line. The STT is intended for a 138 kV line, which has a maximum current $I_{\ell,max} = 750$ A_{rms}. For example, then, let $X_{des} = 2X_m = 2\omega_\ell L_m = 37.7$ mΩ. Also, taking from the VSI design presented in [23], the voltage rating of the dc-side capacitor $V_{dc,max} = 900$ V, which means the maximum injected voltage, referenced to the secondary side of the STT, is $V_{ac} = 900/\sqrt{2} = 636$ V_{rms}.

Using (3.16), n=22.5. In order to keep the VSI currents low, n should be rounded up, so that $n = 23$. The reactive power injected by the VSI is

$$Q_{req} = \frac{636 \times 750}{23} - \frac{636^2}{23^2 \times 18.9 \cdot 10^{-3}} = -19.8\text{kVAr}. \tag{3.29}$$

Because the convention used here is that $Q > 0$ corresponds to absorbed reactive power, it is expected that $Q_{req} < 0$ when emulating capacitance. C_{dc} is required to store

$$E_{dc} = \frac{1}{\omega_\ell}\left(\frac{900^2}{2 \times 23^2 \times 18.9 \cdot 10^{-3}} - \frac{900 \times 750}{23\sqrt{2}}\right) = 52.7 \text{ J}. \tag{3.30}$$

The VSI output current at the peak of the ac cycle under maximum operating conditions is $I_{ac,max} = 44.1$ A. This is well within the specifications of available switching devices, such as

the IGBT modules discussed in Chapter 4, even when accounting for some filter inductor current ripple.

Finally, the difference between SPWM control and constant duty cycle control may be highlighted in the choice of C_{dc}. Using constant duty cycle control,

$$C_{dc} = \frac{2 \times 52.7}{900^2} = 130 \ \mu\text{F}. \tag{3.31}$$

The required duty cycle to achieve X_{des} is

$$D = 23\omega_\ell \sqrt{\frac{50 \cdot 10^{-6} \times 130 \cdot 10^{-6} \times 37.7 \cdot 10^{-3}}{37.7 \cdot 10^{-3} - 18.9 \cdot 10^{-3}}} = 0.989. \tag{3.32}$$

In order to find a value for C_{dc} under SPWM control, a value for r must be defined. Assuming $r = 1\%$, a typical value, rearranging (3.12) yields:

$$C_{dc} = \frac{E_{dc}(1+r)^2}{2{V_{dc,max}}^2 r} = \frac{52.7 \times 1.01^2}{2 \times 900^2 \times 0.01} = 3.3 \text{ mF}, \tag{3.33}$$

which is about 25 times larger. Even with a less conservative value of r – say, 10% – $C_{dc} = 394 \ \mu$F is required, which is three times as large in the SPWM case compared to constant duty cycle control.

Equation (3.27) may be used to find the maximum capacitive value of X_{inj}. The maximum capacitive value of V_{ac} is

$$V_{ac} = .5 \times 23 \times 18.9 \cdot 10^{-3} \times 750 \left(1 - \sqrt{1 + \frac{4 \times 52.7}{50 \cdot 10^{-3} \times 750^2}}\right) = -311 \ \text{V}_{\text{rms}}, \tag{3.34}$$

which is equivalent to $V_{ac} = 311 \ \text{V}_{\text{rms}} \angle -90°$, and the resulting value of DSSC reactance at $I_{\ell,max}$ is

$$X_{inj} = \frac{-311}{23 \times 750} = -18\text{m}\Omega. \tag{3.35}$$

At $I_{\ell,max}$, the duty cycle required to reach this value of X_{inj} is

$$D = 23\omega_\ell \sqrt{\frac{50 \cdot 10^{-6} \times 130 \cdot 10^{-6} \times (-18 \cdot 10^{-3})}{(-18 \cdot 10^{-3}) - 18.9 \cdot 10^{-3}}} = 0.489. \tag{3.36}$$

This also establishes the limits of operation at $I_{\ell,max}$: for $0.489 < D < 0.989$, $V_{dc,max}$ will be exceeded.

As mentioned in Section 3.1, the VSI improves the DSSC performance relative to a fixed capacitor on the secondary side of the STT. The VSI may be controlled so that the maximum available energy is drawn from C_{dc} under all conditions. If the system is designed as described in this chapter, the magnitude of injected impedance would *rise* as the line current is lowered from its maximum value $I_{\ell,max}$. Fig. 3.7 shows the capabilities of the DSSC designed in this section vs. I_ℓ, as well as the duty cycle required to maximize the DSSC performance vs. I_ℓ.

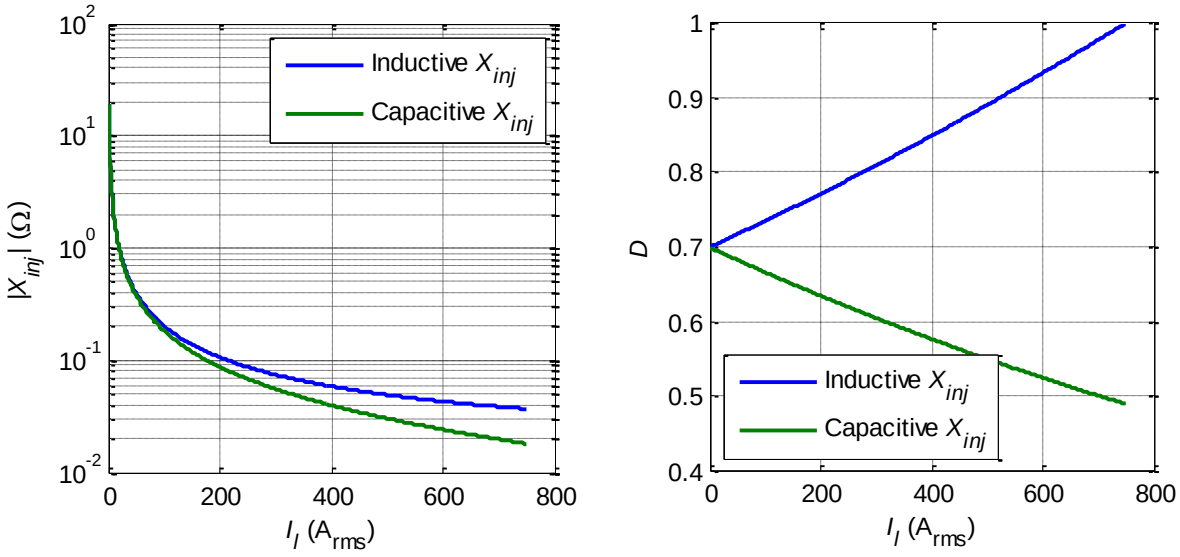
The peak VSI current for the capacitive case comes from (3.28):

$$|I_{ac,max}| = \frac{52.7\omega_\ell\sqrt{2}}{|V_{ac}|} = 90.3 \text{ A}. \tag{3.37}$$

This is higher than in the maximum inductive case, but may still be within device limits. For example, the IGBTs used in the hardware design described in Chapter 4 are rated for 150 A. Still, if it is desired to lower this current, the turns ratio may be raised as high as

$$n_{max} = \frac{900}{18.9 \cdot 10^{-3} \times 750\sqrt{2}} = 45, \tag{3.38}$$

from (3.22), before the VSI has no benefit in the inductive case. Say, for example, n is raised to



(a) (b)

Figure 3.7: For inductive and capacitive operation, as a function of I_ℓ, (a) the maximum possible value of $|X_{inj}|$, and (b) the duty cycle required to achieve the corresponding value in (a)

35. The design process from Section 3.3.1 is started over at Step 3:

$$E_{dc} = \frac{1}{\omega_\ell}\left(\frac{900^2}{2 \times 35^2 \times 18.9 \cdot 10^{-3}} - \frac{900 \times 750}{35\sqrt{2}}\right) = 10.4 \text{ J}$$

and

$$C_{dc} = \frac{2 \times 10.4}{900^2} = 25.6 \ \mu\text{F},$$

so, using (3.27):

$$X_{inj} = \frac{V_{ac}}{nI_{\ell,max}} =$$
$$\tfrac{1}{2} \times 35 \times 18.9 \cdot 10^{-3} \times 750 \left(1 \pm \sqrt{1 + \frac{4 \times 10.4}{50 \cdot 10^{-3} \times 750^2}}\right) = \{24.2, -5.39\} \text{ m}\Omega,$$

The resulting peak current values are $I_{ac,max} = \{8.73, 39.1\}$ A for the inductive and capacitive cases, respectively. This process may be repeated iteratively until a suitable design has been found.

3.3.5 Transmission system applications

With the practical design given in Section 3.3.4, it is possible to analyze the benefit of active DSSC designs and constant duty cycle control in the context of the system examples presented in Chapter 2.

Consider the first design described in Section 3.3.4. A VSI with $C_{dc} = 130$ μF is connected to the secondary side of an STT with $L_m = 50$ μH and $n = 23$. The maximum line current is $I_{\ell,max} = 750$ A_{rms}, where $X_{inj,max} = \{36.9, -18.0\}$ mΩ using constant duty cycle control. Under SPWM control with $r = 5\%$, the same design produces $X_{inj,max} = \{23.9, -5.05\}$ mΩ at $I_{\ell,max}$. Consider, also, a passive design that includes a fixed capacitance C_{fix} on the STT secondary that, when activated, allows $X_{inj} = -X_m$:

$$X_e = \frac{-n^2 {X_m}^2}{2X_m} = \tfrac{1}{2}(-23)^2(18.9 \cdot 10^{-6}) = -4.99 \ \Omega, \tag{3.39}$$

from (3.2), so

$$C_{fix} = \frac{-1}{\omega_\ell X_e} = 532 \ \mu\text{F}. \tag{3.40}$$

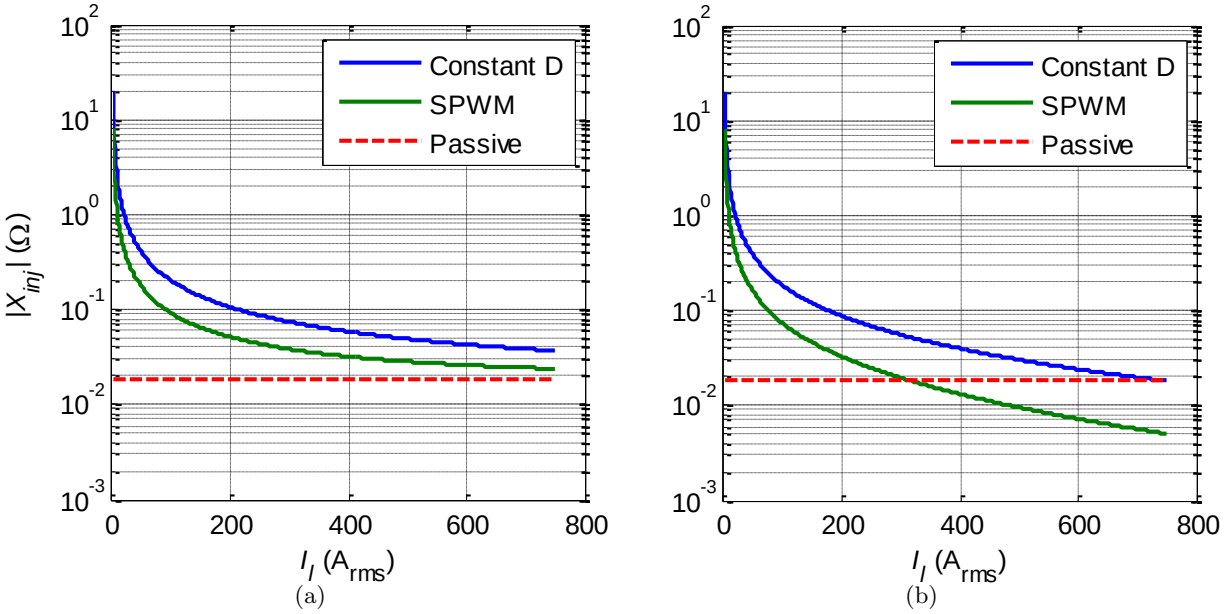


Figure 3.8: Maximum (a) inductive X_{inj} and (b) capacitive X_{inj} for all three designs

The resulting performance of all three designs is given in Fig. 3.8. Note that because the VSI is designed for constant duty cycle control, performance under SPWM control is *worse* that the passive performance for capacitive operation.

It is possible to calculate the number of DSSC devices needed for the compensation functions from Chapter 2, given the required values of $\hat{x} = X_{inj}$ and resulting $I_\ell = I_{mn}$. Consider the three-bus voltage correction example from Section 2.2.2. If DSSCs on Line 1-2 are used to correct V_3, the required injected reactance is $\hat{x}_{12} = -0.119$ p.u.. The system uses an apparent power base value of $S_{base,3\phi} = 100$ MVA and a line-line voltage base value of $V_{base,\ell\ell} = 138$ kV. Therefore, the impedance base is $Z_{base} = V^2_{base,\ell\ell}/S_{base,3\phi} = 190\ \Omega$, so for $\hat{x}_{12} = -0.119$, $X_{inj} = -22.6\ \Omega$. The passive design would require $X_{inj}/X_m = 1,200$ devices per phase, or 3,600 devices total on Line 1-2.

The current base is $I_{base} = S_{base,3\phi}/(V_{base,\ell\ell}\sqrt{3}) = 418$ A_{rms}, so the resulting line current is $I_{12} = I_\ell = 366$ A_{rms}. At this current $X_{inj,max} = -0.044\ \Omega$ under capacitive operation and constant duty cycle control. Therefore, a total of 1,531 devices are required for all three phases, less than half as many as with the passive design. Also, at this current, the passive design outperforms the

active device using SPWM control with $r = 5\%$, so the SPWM design would require more than 3,600 devices.

As a more realistic case, consider the generator reactive power reduction example in Section 2.6.1. DSSCs are deployed on Lines 1-2, 4-5, 1-5, 2-3, and 3-4, and both capacitive and inductive reactance is injected. Table 3.1 shows the required total number of DSSCs on all lines for each of the three designs. The active design with constant duty cycle control requires, on some lines, an order of magnitude fewer devices, clearly justifying the addition of the VSI. SPWM control also requires far fewer devices on some of the lines, but as Fig. 3.8 indicates, a different design approach – resulting in a larger value of C_{dc} – would be necessary for SPWM control to outperform the passive design at all values of line current.

3.4 VSI Power Loss

An additional benefit of constant duty cycle control is that it reduces the power loss in the VSI. In order to analyze this loss for the purpose of comparison and prediction, it is necessary to model the predominant loss mechanisms in the VSI.

This section assumes the VSI uses three-level switching. Under three-level switching, the H-bridge legs alternate with half-cycles of the ac-side voltage: one H-bridge leg switches at high frequency during one half-cycle, while the switch node of the other leg is fixed to the dc-side negative rail. During the other half-cycle, the legs swap operation. The resulting conversion ratio is D.

Table 3.1: DSSC operating points and total required number of devices for three design examples using 14-bus generator Q reduction example

	X_{inj} (Ω)	I_ℓ (A_{rms})	Passive	SPWM control, $r = 5\%$	Constant duty cycle control
Line 1-2	0.132	620	21	16	10
Line 4-5	6.45	212	1,027	392	192
Line 1-5	-5.19	302	825	799	281
Line 3-4	-24.4	43.8	3,890	410	170
Line 2-3	-16.9	348	2,695	3,160	1,081

3.4.1 Inductor loss

The primary sources of power loss in the inductors is the resistance of the windings and the hysteresis of the cores. As Chapter 4 explains in more detail, the inductor L_i is implemented as a pair of series inductors, $\frac{1}{2}L_i$, on the high and low branches of the ac side. See Fig. 4.5. In order to find the total resistive loss, first the RMS inductor current over one switching cycle must be determined. The inductor current during a given switching cycle is equal to the ac-side current I_{ac} at that time (which is approximated as constant during a switching cycle) plus some switching ripple. The RMS current of the waveform, with an average value i_{ac} and ripple magnitude Δi_L, is:

$$i_{Lrms,sw} = \sqrt{{i_{ac}}^2 + \tfrac{1}{3}{\Delta i_L}^2}. \tag{3.41}$$

During each switching cycle, there is an amount of energy lost related to this RMS current:

$$W_{cu,sw} = \frac{{i_{Lrms,sw}}^2 R_{cu}}{f_{sw}}. \tag{3.42}$$

This value of energy varies over the ac system cycle. The total energy lost over a cycle is the sum of the energies lost in each switching cycle. However, because the switching period is very short compared to the grid period, this sum may be approximated as an integral, with $T_s \approx \mathrm{d}t$. This approximation is used frequently in subsequent calculations. The total power loss, then, is the switching cycle power loss averaged over $T_\ell = 1/f_\ell$ (and doubled to reflect the two inductors):

$$P_{cu} = \frac{2}{T_\ell T_{sw}} \int_0^{T_\ell} W_{cu,sw}\,\mathrm{d}t. \tag{3.43}$$

The core loss may be calculated in a similar fashion. The core experiences a swing in magnetic flux density, ΔB, over each switching cycle, which is related to the core size and duty cycle:

$$\Delta B = \frac{(1-d)v_{ac}}{2n_L A_c f_{sw}}, \tag{3.44}$$

where d is the H-bridge duty cycle, n_L is the number of inductor turns, and A_c is the cross-sectional area of the inductor core. With $f_\ell \ll f_{sw}$, ΔB may be considered a continuous function of time. The power lost in the core during each switching cycle is related to ΔB with the following expression:

$$P_{fe,sw}(t) = K_{fe}(\Delta B(t))^\beta A_c l_g, \tag{3.45}$$

where l_g is the length of the inductor air gap, and the values of K_{fe} and β are typical for ferrite cores operating at the switching frequency f_s. $P_{fe,sw}$ may then averaged over the grid period T_ℓ and doubled to get the total core loss of both inductors:

$$P_{fe} = \frac{2}{T_\ell} \int_0^{T_\ell} P_{fe,sw} \, \mathrm{d}t. \tag{3.46}$$

3.4.2 Conduction loss

Typically, the most significant sources of loss in a converter are the solid state switches, which dissipate power both when they are conducting and when they are turned on and off. The VSI design described in Chapter 4 uses IGBTs in the H-bridge. The H-bridge conduction losses, which are due to equivalent on-state resistance and voltage drop of the IGBT and its antiparallel body diode, will be present under any operating condition. In this model, the on-state resistance and forward voltage drop of the IGBT and body diodes are estimated by fitting a line to the I-V characteristic curves given in the device datasheet [45].

The switching average and RMS currents are calculated separately for two different modes that may occur during a grid cycle: unidirectional conduction, where $\Delta i_L < i_{ac}$, and bidirectional conduction, where $\Delta i_L > i_{ac}$. With high output power and low inductor current ripple, the bidirectional conduction mode may be very brief, perhaps only a couple switching cycles. However, with low output power and high inductor current ripple, the unidirectional conduction mode may not occur at all. It is valuable to develop a model that accounts for any operating condition.

Thanks to the symmetry of the system, it is only necessary to analyze the loss for one H-bridge leg. The top switch only operates during one half-cycle of v_{ac}; e.g., Q_1 switches at high frequency when $v_{ac} > 0$. Whether the transistor channel or body diode conducts depends on the sign of i_{ac}. When $v_{ac} < 0$, Q_1 does not conduct. The bottom switch is always conducting: Q_2, for example, switches at high frequency along with Q_1 when $v_{ac} > 0$ and is fixed on when $v_{ac} < 0$. As with Q_1, whether the transistor channel or body diode conducts depends on the sign of i_{ac}. It is necessary to find the RMS and average current values for both switches Q_1 and Q_2, including their transistor channels and body diodes separately, for all intervals of the v_{ac} cycle.

When Q_1 is switching, the switching-cycle RMS currents for the transistor channel and diode are, respectively,

$$i_{Q1rms,cont} = \sqrt{d\left({i_{ac}}^2 + \tfrac{1}{3}\Delta {i_L}^2\right)} \tag{3.47}$$

and

$$i_{D1rms,cont} = \sqrt{d\left({i_{ac}}^2 + \tfrac{1}{3}\Delta {i_L}^2\right)}. \tag{3.48}$$

Either one or the other will conduct, depending on the sign of i_{ac}. The average Q_1 transistor channel and diode current values are, respectively,

$$i_{Q1avg,cont} = d\, i_{ac} \tag{3.49}$$

and

$$i_{D1avg,cont} = d\, i_{ac}. \tag{3.50}$$

When $v_{ac} > 0$, the average and RMS currents of Q_2 are complementary to those of Q_1:

$$i_{Q2rms,cont} = \sqrt{(1-d)\left({i_{ac}}^2 + \tfrac{1}{3}\Delta {i_L}^2\right)}, \tag{3.51}$$

$$i_{D2rms,cont} = \sqrt{(1-d)\left({i_{ac}}^2 + \tfrac{1}{3}\Delta {i_L}^2\right)}, \tag{3.52}$$

$$i_{Q2avg,cont} = (1-d)\, i_{ac}, \tag{3.53}$$

and

$$i_{D2avg,cont} = (1-d)\, i_{ac}. \tag{3.54}$$

When $v_{ac} < 0$, Q_2 conducts all of the inductor current, either through its transistor channel or its body diode:

$$i_{Q2rms,cont} = i_{D2rms,cont} = \sqrt{{i_{ac}}^2 + \tfrac{1}{3}\Delta {i_L}^2} \tag{3.55}$$

and

$$i_{Q2avg,cont} = i_{D2avg,cont} = i_{ac}. \tag{3.56}$$

In the bidirectional conduction mode, Q_2 may commutate between its transistor channel and body diode even when $v_{ac} > 0$. During the d sub-interval, with $v_{ac} > 0$, conduction commutates

from the body diodes to the transistor channels of one top and bottom switch. During the $1-d$ interval, conduction commutates between the body diodes and transistor channels of both bottom switches. Fig. 3.9 illustrates the switching behavior of a bidirectional conduction interval. When $v_{ac} > 0$, the top and bottom transistor channels have an effective duty cycle during bidirectional conduction of

$$d_{effQ1} = d_{effQ2} = d\left(\frac{\Delta i_L + i_{ac}}{2\Delta i_L}\right), \tag{3.57}$$

and the effective duty cycle of the f_{sw}-switching body diodes is

$$d_{effD1} = d_{effD2} = (1-d)\left(\frac{\Delta i_L + i_{ac}}{2\Delta i_L}\right). \tag{3.58}$$

When $v_{ac} < 0$, Q_2 (whose behavior is equivalent to that of Q_4 in Fig. 3.9) conducts through the transistor channel while $i_{sw} > 0$ for an effective duty cycle of

$$d_{effQ2,on} = \left(\frac{\Delta i_L + i_{ac}}{2\Delta i_L}\right), \tag{3.59}$$

and through the body diode while $i_{ac} < 0$, for an effective duty cycle of

$$d_{effD2,on} = \left(\frac{\Delta i_L - i_{ac}}{2\Delta i_L}\right). \tag{3.60}$$

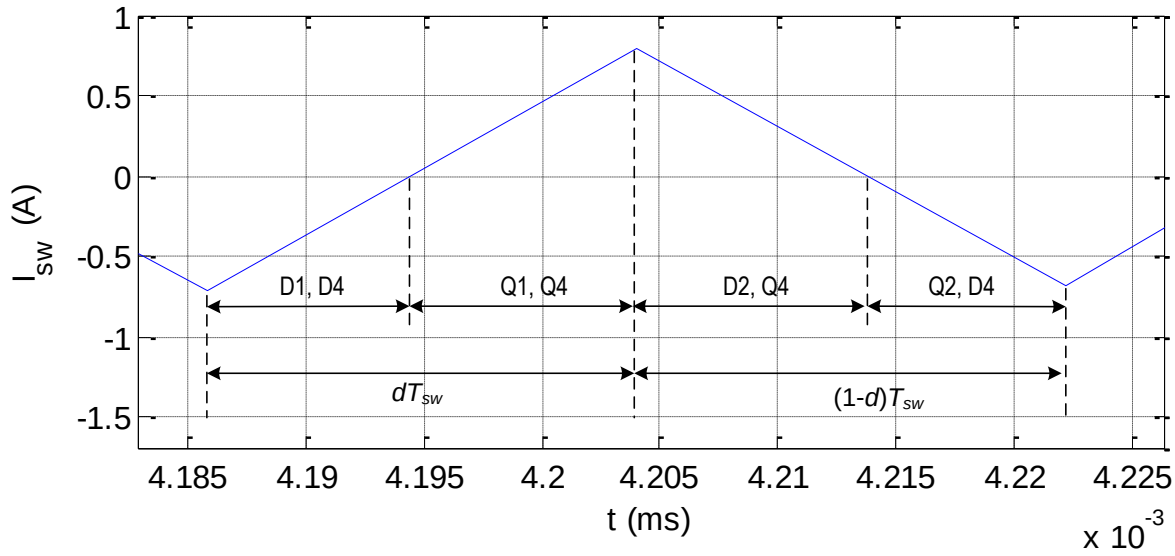


Figure 3.9: Example of bidirectional conduction mode, with conducting devices labeled

The transistor channel currents in the high-frequency switching leg ramp from 0 to $i_{ac}+\Delta i_L$, while, in their interval, the body diode currents ramp from $i_{ac}+\Delta i_L$ to 0. The transistor channel and body diode RMS currents for both switches are, respectively,

$$i_{Qrms,disc} = (i_{ac} + \Delta i_L)\sqrt{\frac{d_{effQ1}}{3}} \tag{3.61}$$

and

$$i_{Drms,disc} = (i_{ac} + \Delta i_L)\sqrt{\frac{d_{effD1}}{3}}, \tag{3.62}$$

and the average currents are

$$i_{Qavg,disc} = \tfrac{1}{2}\, d_{effQ1}(i_{ac} + \Delta i_L) \tag{3.63}$$

and

$$i_{Davg,disc} = \tfrac{1}{2}\, d_{effD1}(i_{ac} + \Delta i_L). \tag{3.64}$$

The RMS currents for the transistor channel and body diode of Q_2 when $v_{ac} < 0$ are

$$i_{Q2rms,disc} = (i_{ac} + \Delta i_L)\sqrt{\frac{d_{effQ2,on}}{3}} \tag{3.65}$$

and

$$i_{D2rms,disc} = (i_{ac} + \Delta i_L)\sqrt{\frac{d_{effD2,on}}{3}}, \tag{3.66}$$

and the average currents are

$$i_{Q2avg,disc} = \tfrac{1}{2}\, d_{effQ2,on}(i_{ac} - \Delta i_L) \tag{3.67}$$

and

$$i_{D2avg,disc} = \tfrac{1}{2}\, d_{effD2,on}(i_{ac} - \Delta i_L). \tag{3.68}$$

These equations account for all the conduction modes of both the transistor channels and body diodes of Q_1 and Q_2. Thus, piecewise equations may be built to describe the RMS and average currents through each device over a full ac line cycle. They are called $i_{Q1rms,sw}$, $i_{Q1avg,sw}$, $i_{D1rms,sw}$, $i_{D1avg,sw}$, $i_{Q2rms,sw}$, $i_{Q2avg,sw}$, $i_{D2rms,sw}$, and $i_{D2avg,sw}$. The full form of each is given in Appendix B.

As with the calculation of inductor loss, these current expressions may be used to find switching cycle energy loss, which is then averaged over a grid cycle to find total loss. The RMS current is used to find the resistive loss in the transistor channel and body diode of Q_1, respectively:

$$P_{Q1,R} = \frac{1}{T_\ell}\int_0^{T_\ell} {i_{Q1rms,sw}}^2(t) R_{on,q}\,\mathrm{d}t \tag{3.69}$$

and

$$P_{D1,R} = \frac{1}{T_\ell}\int_0^{T_\ell} {i_{D1rms,sw}}^2(t) R_{on,d}\,\mathrm{d}t, \tag{3.70}$$

where $R_{on,q}$ and $R_{on,d}$ are the series on-resistance of the device conduction paths. The average current is used to calculate power lost to voltage drops across the transistor channel and body diode of Q_1, respectively:

$$P_{Q1,V} = \frac{1}{T_\ell}\int_0^{T_\ell} i_{Q1avg,sw}(t) V_{f,q}\,\mathrm{d}t \tag{3.71}$$

and

$$P_{D1,V} = \frac{1}{T_\ell}\int_0^{T_\ell} i_{D1avg,sw}(t) V_{f,d}\,\mathrm{d}t, \tag{3.72}$$

where $V_{f,q}$ and $V_{f,d}$ are the forward voltage drops across each device conduction path. The same can be done for Q_2:

$$P_{Q2,R} = \frac{1}{T_\ell}\int_0^{T_\ell} {i_{Q2rms,sw}}^2(t) R_{on,q}\,\mathrm{d}t, \tag{3.73}$$

$$P_{D2,R} = \frac{1}{T_\ell}\int_0^{T_\ell} {i_{D2rms,sw}}^2(t) R_{on,d}\,\mathrm{d}t, \tag{3.74}$$

$$P_{Q2,V} = \frac{1}{T_\ell}\int_0^{T_\ell} i_{Q2avg,sw}(t) V_{f,q}\,\mathrm{d}t, \tag{3.75}$$

and

$$P_{D2,V} = \frac{1}{T_\ell}\int_0^{T_\ell} i_{D2avg,sw}(t) V_{f,d}\,\mathrm{d}t. \tag{3.76}$$

The total switch conduction power loss is the sum of these terms multiplied by the number of legs. Although the current expressions were developed for specific devices, the total power loss is equal in all devices due to the symmetry of the circuit and of the ac cycle.

$$P_{cond} = 2(P_{Q1,R} + P_{D1,R} + P_{Q1,V} + P_{D1,V} + P_{Q2,R} + P_{D2,R} + P_{Q2,V} + P_{D2,V}). \tag{3.77}$$

3.4.3 Switching loss

The dominant loss mechanism of this inverter design is the energy lost to non-ideal switching of the IGBTs. In particular, the diode reverse recovery loss, which occurs upon diode turn-off, and the IGBT current tailing loss, which occurs upon transistor channel turn-off, are modeled here.

Diode reverse recovery is the process, upon diode turn-off, of removing minority charge stored during diode conduction. When an opposing IGBT is turned on, the stored charge is removed as the diode conducts negative current while remaining forward biased. Consequently, the voltage across the IGBT is v_{dc} while it conducts the current necessary to reverse-recover the diode, and it experiences a significant loss in energy. According to [36], the recovered charge Q_{rr} and the time required for recovery t_{rr} are functions of the diode forward current. During the unidirectional conduction portion of the grid cycle, the diodes turn off at the "inner" values of the inductor current; that is, the diode forward current $I_F = |i_{ac}| - \Delta i_L$ (see Fig. 3.10). During the bidirectional conduction portion of the grid cycle, the diodes experience zero-current switching, and the reverse recovery loss is neglected. From [36], the most appropriate approximations of the relationships

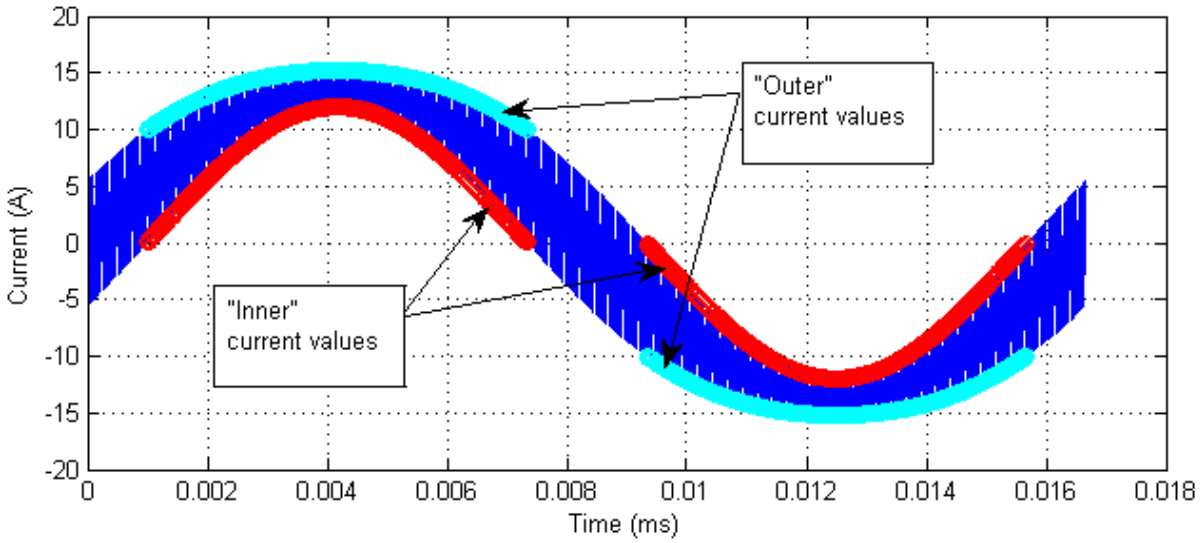


Figure 3.10: Inductor current with "inner" and "outer" ripple current values

between forward current and reverse recovery parameters are

$$Q_{rr} = K_{Qrr}\sqrt{v_{dc} i_F} \tag{3.78}$$

and

$$t_{rr} = K_{trr}\sqrt[4]{i_F}\,. \tag{3.79}$$

The parameters K_{Qrr} and K_{trr} are approximated from [45], which provides graphs of diode turn-off energy vs. forward current. Considering the entire grid cycle, the energy lost to reverse recovery in Q_2 (for example) at each turn-off instance is

$$W_{rr}(t) = \begin{cases} v_{dc} i_F(t) t_{rr}(t) + v_{dc} Q_{rr}(t)\,, & \text{for } i_{ac}(t) > 0 \text{ and } \Delta i_L(t) < i_{ac}(t) \\ 0\,, & \text{for } i_{ac}(t) < 0 \text{ or } \Delta i_L(t) > i_{ac}(t)\,. \end{cases} \tag{3.80}$$

The average power loss per switching cycle is $W_{rr} f_{sw}$, which may be averaged over a grid cycle to find total power loss:

$$P_{rr} = \frac{1}{T_{sw} T_\ell} \int_0^{T_\ell} W_{rr}\,\mathrm{d}t\,. \tag{3.81}$$

The other switching loss mechanism considered here is the IGBT current tail. Upon turn-off of a transistor channel, the collector current ramps slowly to 0 after the device has already started blocking its off-state voltage. In this case, the current through the transistor channel upon turn-off is the "outer" value of the inductor current waveform (see Fig. 3.10), $i_{ac} + \Delta i_L$, and the blocked voltage is v_{dc}. According to [36], the total conducted charge during the current tail is proportional to the current at turn-off:

$$Q_{tail} = K_{qtail}(i_{ac} + \Delta i_L)\,. \tag{3.82}$$

This value is used similarly to Q_{rr}, although in this case there is only loss in one device. Also, transistor channel current does not ramp to 0 during bidirectional conduction, meaning that for a given IGBT, current tailing loss occurs during the bidirectional conduction portions and the unidirectional conduction portions for half of the grid cycle. For Q_1, as an example, the expression

for current tailing energy loss is

$$W_{tail}(t) = \begin{cases} v_{dc} Q_{tail}(t)\,, & \text{for } i_{ac}(t) > 0 \text{ or } \Delta i_L(t) > i_{ac}(t) \\ 0\,, & \text{for } i_{ac}(t) < 0 \text{ and } \Delta i_L(t) < i_{ac}(t)\,. \end{cases} \tag{3.83}$$

The total current tailing power loss is the power lost per switching cycle averaged over the grid cycle:

$$P_{tail} = \frac{1}{T_{sw} T_\ell} \int_0^{T_\ell} W_{tail}\, \mathrm{d}t\,. \tag{3.84}$$

Finally, the total switching power loss is the sum of reverse recovery loss and current tailing loss for all devices:

$$P_{sw} = 4(P_{rr} + P_{tail}). \tag{3.85}$$

3.4.4 Total power loss and effective efficiency

The total power loss in the inverter modeled in Fig. 1.6 has been approximated, as described, by the inductor losses ($P_L = P_{fe} + P_{cu}$), the switching device conduction losses, and the switching loss:

$$P_{loss} = P_L + P_{cond} + P_{sw}. \tag{3.86}$$

The definition of effective efficiency compares watts to VArs:

$$\eta = 1 - \frac{P_{loss}}{Q_{req}}. \tag{3.87}$$

It can be compared easily with conventional real power efficiency figures, where 100% is ideal.

The model has been programmed as a MATLAB script to predict the effective efficiency of an inverter under different control schemes and operating points. The parameters are based on the hardware design described in Chapter 4. The script can calculate the individual loss mechanisms, and allows for an arbitrary dc-side voltage waveform.

For example, the SPWM design from Section 3.3.4 prescribes a sinusoidal dc-side voltage signal at twice the line frequency with a maximum value $V_{dc,max} = 900$ V, a ripple of $r = 1\%$ or $V_r = rV_{dc}/(1+r) = 8.91$ V, and an average value of $V_{dc} = 891$. The VSI ac-side voltage is 636 V_{rms}

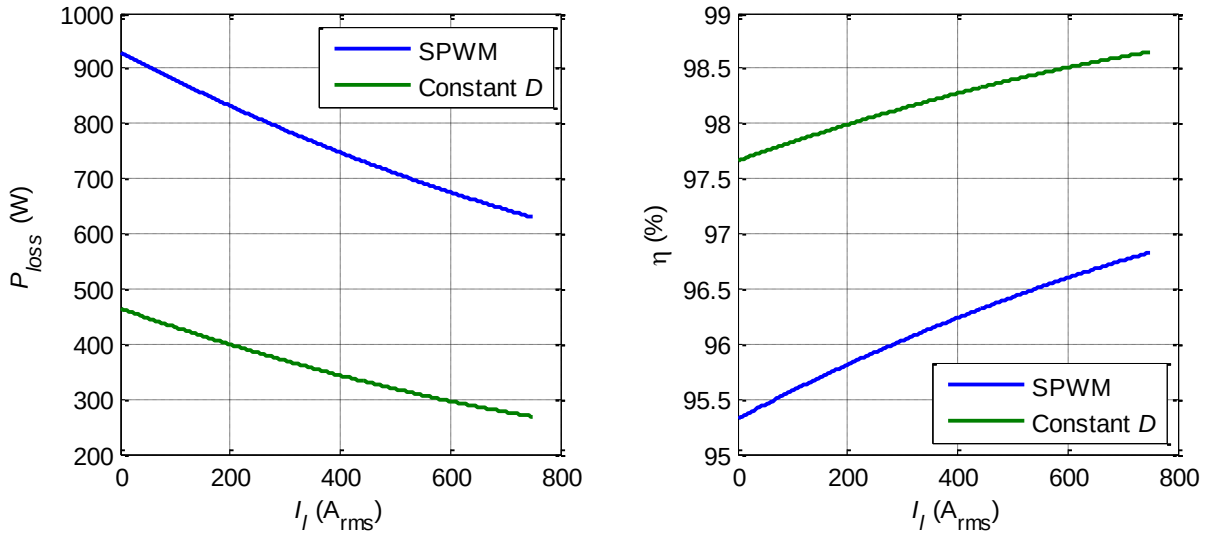
and the ac-side current is 31.2 A_{rms}, for a total power injected by the VSI of $Q_{req} = 19.9$ kVAr. In contrast, the constant duty cycle design uses the same ac-side operating point, but the dc-side voltage waveform is a rectified sinusoid with a peak value of $V_{dc,max} = 900$ V and in phase with v_{ac}. Table 3.2 shows the component and total loss values, as well as the effective efficiency, calculated by the model.

As expected, the inductor loss and IGBT conduction loss are not significantly reduced by the use of constant duty cycle control. Instead, the improvement in effective efficiency comes from the switching loss, which is highly dependent on V_{dc}. The model confirms that allowing V_{dc} to fall cyclically to 0 greatly lowers the switching loss and overall loss.

Fig. 3.11 presents a plot of total loss and effective efficiency using both control schemes

Table 3.2: Power loss comparison of VSI under SPWM vs. constant duty cycle control schemes

	P_L (W)	P_{cond} (W)	P_{sw} (W)	P_{loss} (W)	η (%)
SPWM	29.4	145	456	**630**	**96.8**
Constant D	29.1	138	101	**269**	**98.7**



(a) (b)

Figure 3.11: For both control schemes, modeled total power loss (a) and effective efficiency (b) vs. I_ℓ for design from Section 3.3.4

for the inductive case from $I_\ell = 0$ to $I_{\ell,max}$. While it may be surprising that the loss rises with decreasing I_ℓ, recall that the VSI for this application is designed to operate at maximum power for any value of I_ℓ. The loss rises, then, because V_{ac} falls with I_ℓ, requiring I_{ac} to rise, and loss, especially conduction loss, is highly dependent on I_{ac}. Fig. 3.11 also shows that constant duty cycle control is more efficient for all values of I_ℓ. While the capacitive case is not shown here, the results are similar. Finally, Fig. 3.12 shows the effective efficiency of the constant duty cycle design for all values of D within the operating range of the design.

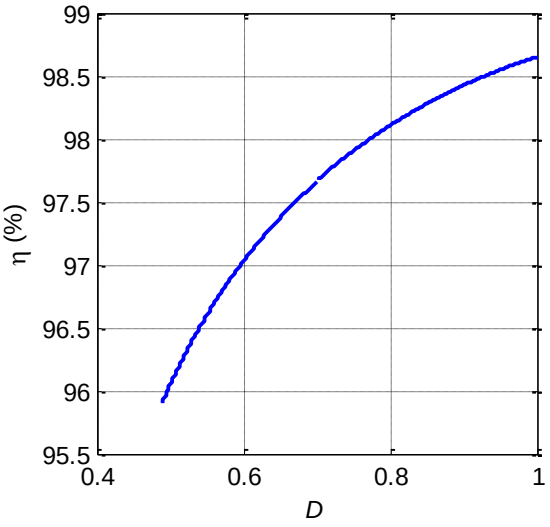


Figure 3.12: VSI effective efficiency vs. duty cycle under constant duty cycle control

Chapter 4

Hardware Design and Experimental Results

In an effort to experimentally test and verify concepts related to transmission and distribution system control, a 5kVA, four-quadrant inverter has been designed and built. Initially, this inverter served as one of several components in a lab-scale microgrid test bed. The inverter, along with a second of similar design, was successfully used to demonstrate microgrid behavior with high photovoltaic penetration [37]. This chapter details the design and results of the hardware experiments, with particular focus on the DSSC application.

4.1 Basic Inverter Design

The hardware experiments are based on a basic inverter design: a dc bus with an energy storage capacitor feeds an IGBT-based H-bridge and LCL filter, which synthesize a 60Hz ac signal using sinusoidally modulated high frequency switching (see Fig. 4.1). The inverter may be controlled in a number of ways. It may act as a voltage source connected to a fixed load, as a voltage source connected to a stiff current source, or as a current source connected to a stiff voltage source.

4.1.1 Parts selection

IGBTs are a standard choice for high voltage applications such as a grid-connected inverter. Relative to power MOSFETs, IGBTs offer a low on-state resistance and forward voltage drop, allowing them to be rated at a high voltage while maintaining high efficiency [29]. This inverter

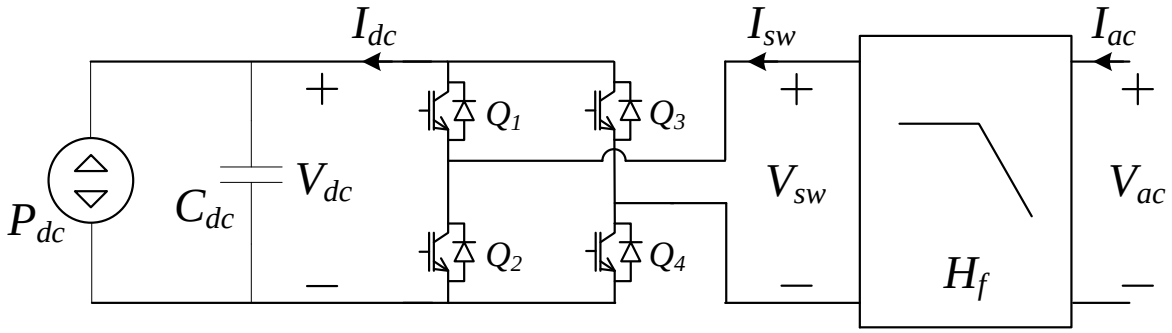


Figure 4.1: Basic inverter design

is designed for 208-240 V_{rms} ac, requiring IGBTs rated for several hundred volts. With a desired power rating of 5kVA, the IGBT current may be as high as 34 A; it is likely to be 5-10% higher when accounting for current ripple. A current rating of > 60 A is desired for this application.

The selection of a gate driver must be considered in addition to the switches themselves. Thankfully, IGBTs for inverter applications are so common that dual-switch modules are easily found. Furthermore, gate drivers for such modules are also common. Gate driver manufacturer Concept produces PCBs custom-designed for a variety of IGBT modules. With the desire to use Concept devices, a compatible IGBT module was selected with ratings close to the desired values. The chosen IGBTs are Infineon FF150R12ME3G "EconoDUAL" modules, which have a 1200 V and 150 A rating [45][1] . The chosen gate drivers are Concept 2SP0115T Plug-and-Play drivers, which may be soldered directly to the IGBT module [46].

The energy storage capacitor must have a high enough voltage rating to support the dc level required for 240 V_{rms} ac-side voltage. It must additionally accommodate some voltage ripple. Derating suggests capacitors rated for > 500 V. If the maximum ripple is chosen to be 5% at 5kVA and $V_{dc} = 500$ V, the required capacitor is

$$C_{dc} = \frac{5000}{2\omega_\ell \times 500^2 \times 5\%} = 530.5\ \mu\text{F}. \tag{4.1}$$

[1] These are the lowest rated devices compatible with Concept gate drivers

In order to reduce cost, C_{dc} may be achieved with two parallel capacitors. The best capacitors to meet these requirements were found to be 275μF AVX film capacitors [48].

Finally, an IC is required for measurement and control of the inverter. The Microchip dsPIC33FJ64GS610 is chosen for its array of features, including a high-resolution dedicated PWM module [49]. In addition to the microcontroller itself, Microchip offers evaluation components (the plug-in module (PIM) and Explorer 16 development board) for easy integration of the device into the system.

4.1.2 Sensors

In order to achieve robust feedback and control, it is necessary to measure several system operating points. This circuit is designed with sensors for voltage and current on most nodes and branches – more than necessary to allow for debugging and future extensions.

There are current sensors on the high side filter branches on either side of the $C_f - R_f$ branch (see Fig. 4.5). They are Allegro ACS758LCB bidirectional Hall effect sensors rated for up to $\pm$50 A peak current [47]. The voltage response of the sensor is

$$V_{out} = k_{sense,i} I_{in} + \frac{V_{cc}}{2}. \tag{4.2}$$

According to [47], k_{sense} = 40 mV/A, but measurements show k_{sense} = 24 mV/A. V_{cc} = 3.3 V and is supplied by the Explorer 16 development board. Additionally, the output of the sensor is configured with a small RC filter to attenuate high frequency signals and noise.

The sensed voltages are V_{dc}, V_{sw}, V_f, and V_{ac}. They are stepped down and offset using a Microchip MCP6L04 quad general purpose op-amp. One channel of the op-amp generates the $V_{cc}/2$ offset for the other three channels. Fig. 4.2 shows an example of one sensor channel. The oscilloscope measurement shows significant switching noise on the sensor output; this noise is filtered by averaging the measurements in the microcontroller code. The sensor channels convert the differential input voltage according to:

$$V_{out} = k_{sense,v}(V_{in+} - V_{in-}) + \frac{V_{cc}}{2}, \tag{4.3}$$

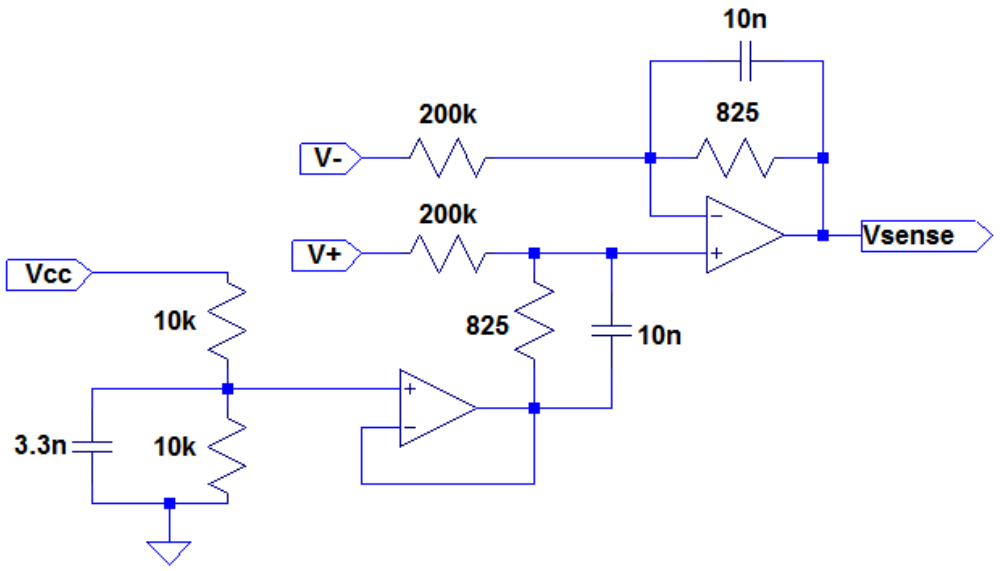


Figure 4.2: Schematic for single voltage sensor channel

where $k_{sense,v} \approx 4$ mV/V. k_{sense} was chosen so that at the maximum $V_{ac} = 240$ V_{rms}, the sensor output would cover the full range of the microcontroller ADC input (0-3.3 V – see Fig. 4.3). One

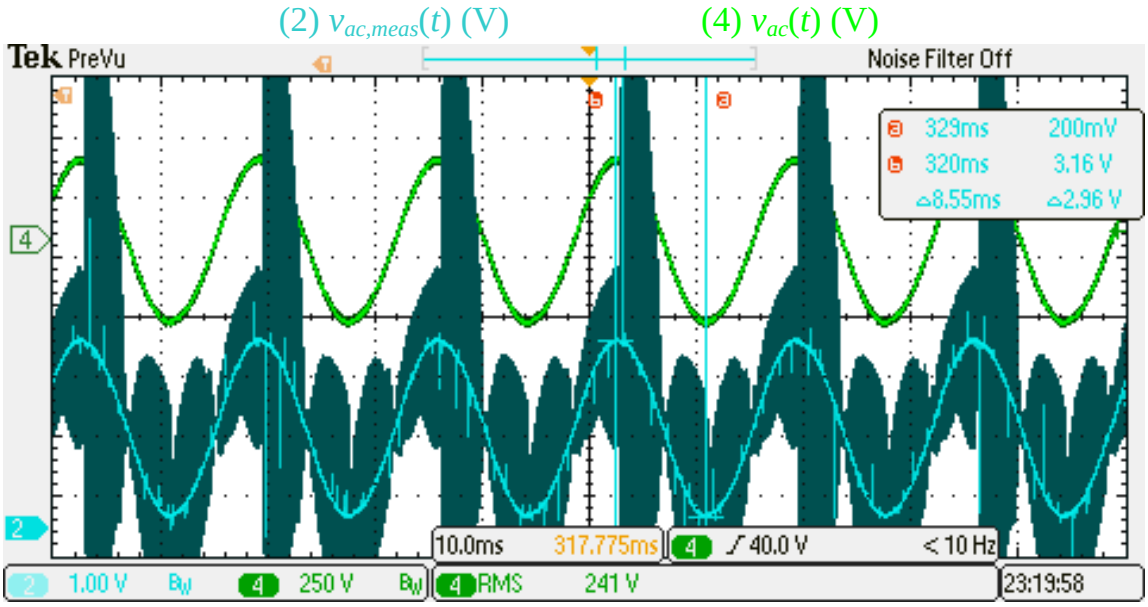


Figure 4.3: Hardware measurement of v_{ac} and resulting sensor output

quad op-amp chip converts V_{sw}, V_f, and V_{ac}, while a second chip is dedicated to V_{dc}.

Ultimately, the sensor for V_{sw} was disabled because it introduced excessive switching noise into the rest of the sensor circuitry. Additionally, considerable common-mode noise was present in the V_{dc} sensor output, requiring further averaging of the measurement in the microcontroller (see Section 4.2.3).

4.1.3 Switching frequency selection

In order to select an appropriate switching frequency, first a nominal compensator design was considered for the condition where the VSI acts as a current source connected to a stiff voltage source. Also, the inverter-side current i_{sw} is used as the control variable in order to simplify the analysis. This allows the filter to be approximated as simply a series inductor. The resulting small-signal ac model of the inverter is given in Fig. 4.4. It is assumed that the perturbations $\hat{v}_{dc}$ and $\hat{v}_{ac}$ may be ignored, so that the circuit is reduced to the voltage source $\hat{d}V_{dc}$ connected to the inductor L_i. Therefore, the control to output transfer function is

$$G_{id}(s) = \frac{\hat{i}_{sw}}{\hat{d}} = \frac{V_{dc}}{sL_i}. \tag{4.4}$$

A PI compensator is used to ensure high gain at f_ℓ and to allow the phase margin to be specified. The PI corner frequency should be moderately high, $f_z > f_\ell$, but not higher than the

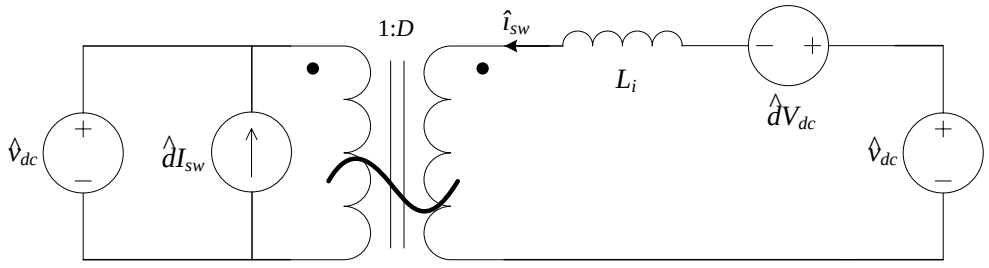


Figure 4.4: Small signal ac model for VSI with series inductor filter, acting as a current source connected to a voltage source

crossover frequency f_c. Let $f_z = 1kHz$, and the desired phase margin $\phi_m = 70°$. The crossover frequency may be calculated:

$$f_c = \frac{f_z}{\tan(90° - \phi_m)} = 2.75kHz. \tag{4.5}$$

Finally, the switching frequency is chosen to be $f_{sw} = 10\ f_c$, as is common to ensure that the switching signals are well attenuated. Therefore, $f_{sw} = 27.5$ kHz. This is high enough for good regulation, while remaining within the operating limits of the gate drivers and IGBTs.

4.1.4 Filter design

The design of the LCL filter for a three-phase inverter that acts as a voltage source is described in [35]. The design process optimizes the values of $L_i,\ L_g,\ C_f,\ R_f$ (see Fig. 4.5) based on the desired current ripple, harmonic attenuation, and reactive power in C_f. The work was also reproduced in the form of a MATLAB script for generating a filter for both single- and three-phase designs. The filter constraints and resulting component values are given in Table 4.1. Fig. 4.6 shows filter transfer functions: one when the VSI acts as a current source connected to a stiff voltage source (green), and one when it acts as a voltage source connected to a stiff current source (blue) (as in the DSSC application).

The inductors are split into series pairs, as in Fig. 4.5, in order to balance the ac-side circuit and eliminate undesired common-mode effects. They are implemented using the K_g design method

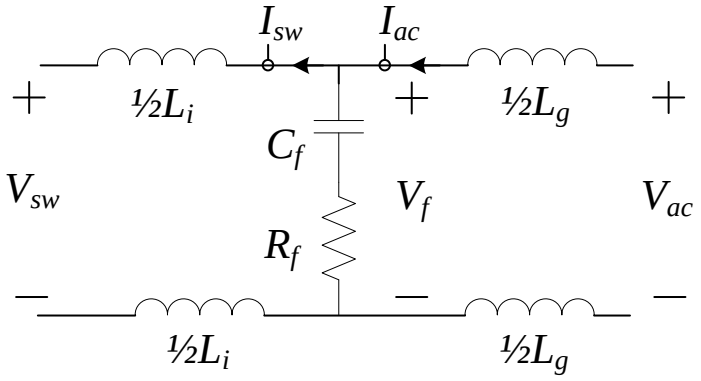


Figure 4.5: Inverter LCL filter

Table 4.1: Inverter LCL filter design parameters and resulting filter component values.

Design Parameters	
P_{rated}	5000 W
V_{ac}	240 V_{rms}
f_ℓ	60 Hz
V_{dc}	500 V
f_{sw}	27.5kHz
L_i current ripple	10% of I_{Li}
C_f reactive power	1% of P_{rated}
Component Values	
L_i	586 μH
L_g	186 μH
C_f	2.3 mF
R_f	2.6 mΩ

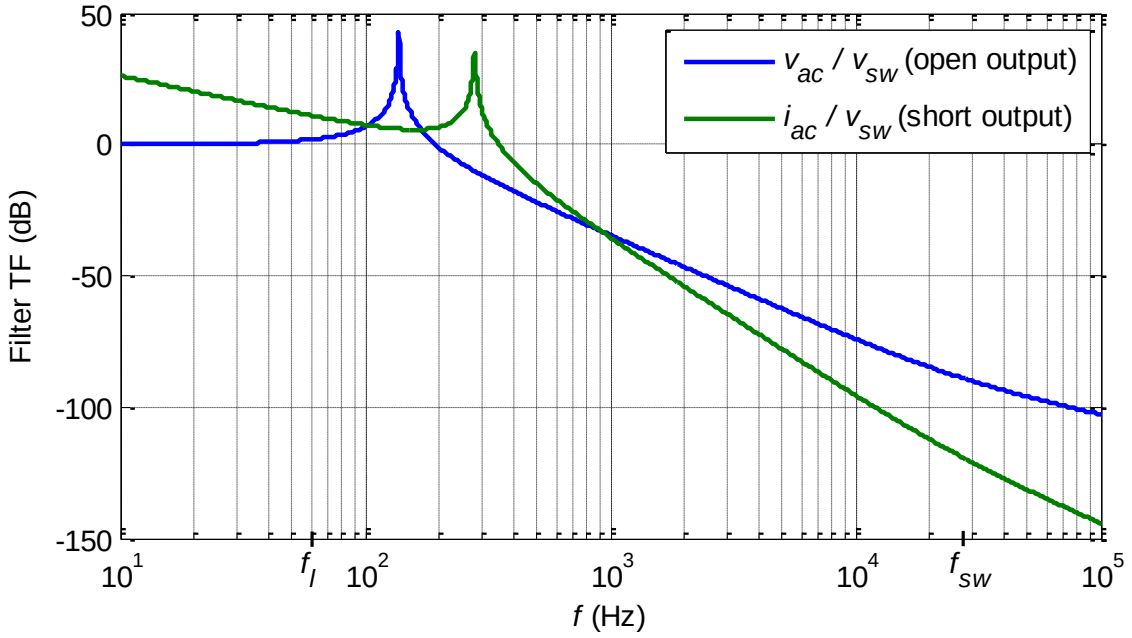


Figure 4.6: LCL filter transfer functions: VSI as a current source connected to voltage source (green) and VSI as a voltage source connected to a current source (blue)

[29]. See Table 4.2 for a complete list of inductor design parameters. For $L_1 = \frac{1}{2}L_i = 293$ μH:

$$K_g \geq \frac{\rho {L_1}^2 {I_{max}}^2 {I_{rms}}^2}{{B_{max}}^2 P_{1cu} K_u} = 9.87 \text{ cm}^5. \tag{4.6}$$

The chosen core to meet this requirement is a ferrite EE70-54-32 core, which has

$$K_g = \frac{{A_c}^2 W_A}{MLT} = 39.7 \text{ cm}^5. \tag{4.7}$$

It should be noted that this core is larger than necessary. The suggested gap length is

$$\ell_g = \frac{\mu_0 L_1 {I_{max}}^2}{{B_{max}}^2 A_c} = 3.52 \text{ mm}. \tag{4.8}$$

The required number of turns is

$$n = \frac{L_1 I_{max}}{B_{max} A_c} = 33.9 \approx 34. \tag{4.9}$$

Finally, the wire size is

$$A_w \leq \frac{K_u W_A}{n_1} = 0.096 \text{ cm}^2. \tag{4.10}$$

Table 4.2: LCL filter inductor design

Operation	$L_1 = \frac{1}{2}L_i$	$L_2 = \frac{1}{2}L_g$
Desired inductance L (μH)	293	92.5
Wire resistivity ρ ($\mu\Omega-$cm)	1.72	
Max current I_{max} (A)	33	32
RMS current I_{rms} (A_{rms})	30	31
Maximum flux density B_{max} (T)	0.4	1.2
Maximum copper loss P_{cu} (W)	30	10
Winding fill factor K_u	0.3	0.2
Minimum geometrical constant K_g (cm^5)	9.87	0.72
Design		
Core designation	EE70	E187
Core cross-sectional area A_c (cm^2)	7.06	2.48
Core window area W_A (cm^2)	10.9	1.93
Mean length per turn Air gap length ℓ_g (mm)	3.52	9.5
Number of turns n	34	20
Wire size (AWG#)	10 ($4 \times$ #16)	15
Performance		
Inductance (μH)	291.5	98.4
Maximum flux density (T)	0.401	0.6
Copper loss (W)	13.7	19

AWG #10 sized wire is chosen to reduce resistive loss; however, as this would be too difficult to wind, a set of four parallel strands of AWG #16 is chosen as the closest approximation. In order to validate the design, the operating parameters may be recalculated for the chosen design parameters:

$$L_1 = \mu_0 n^2 A_c \ell_g = 291.5\ \mu\text{H}, \tag{4.11}$$

$$P_{cu} = \frac{{I_{rms}}^2 \rho n MLT}{A_w} = 13.7\ \text{W}, \tag{4.12}$$

and

$$B_{max} = \frac{\mu_0 n I_{max}}{\ell_g} = 0.401\ \text{T}. \tag{4.13}$$

The design process used for $L_2 = \frac{1}{2} L_g$ is mostly the same as for L_1. L_2 is made with a powdered iron core that features a higher maximum flux density and lower relative permeability compared to ferrite. The design process assumes that permeability of the core material is large enough that the reluctance of the core can be neglected. For the material used in L_g, the core reluctance cannot be neglected, and it is found that the desired value of inductance is best achieved with no air gap. The results of the L_2 design are given in Table 4.2.

4.2 DSSC Application

The hardware has been used to demonstrate an advanced control scheme for active DSSCs. By using pulse-width modulation with a constant duty cycle on the active DSSC voltage source inverter (VSI), as opposed to the more common sinusoidally pulse-width modulated (SPWM) control, the device may operate with improved performance, increased efficiency, and simplified control. This section describes the design process of both control schemes (SPWM control is implemented for comparison).

The VSI described in this chapter is scaled down relative to a DSSC suitable for most transmission systems. Section 3.3.4 presents a realistic production-scale design. Additionally, the operating points of the hardware experiments are limited by the equipment available to drive and measure the device. See Table 4.4 for the experimental operating points. The primary limitation is that a controllable ac current source is not available. Instead, a current source is approximated

by connecting a large resistance in series with a variac powered by the line (see Fig. 4.7). Both the variac and power resistors are limited to about 15 A_{rms}. Also, the most suitable available capacitor for C_{dc} is a 100 μF with a rated voltage of 450 V, which is de-rated to $V_{dc} = 350$ V.

There are two important differences between the original design approach and that for the DSSC that must be highlighted. First, the original design uses two-level switching, where both legs of the H-bridge are switching at all times in a complementary fashion. The resulting conversion ratio is $2D-1$, where D refers to the duty cycle of Q_1 (see Fig. 4.1). In order to improve efficiency, the DSSC inverter application uses three-level switching, where the H-bridge legs alternate with half-cycles of the ac voltage: one H-bridge leg switches at high frequency during a half-cycle, while the switch node of the other leg is fixed to the dc-side negative rail by leaving the bottom switch on. The duty cycle of both Q_1 and Q_3 when switching is D, and the conversion ratio is D. Two-level switching was used in the original design for its simple implementation and reliable control. Three-level switching reduces the switching loss by nearly one half, as only two IGBTs switch at high frequency at any given time. The drawback of three-level switching is that it is more difficult to control at the zero-crossings of the voltage waveform, where the H-bridge legs alternate and D goes to 0.

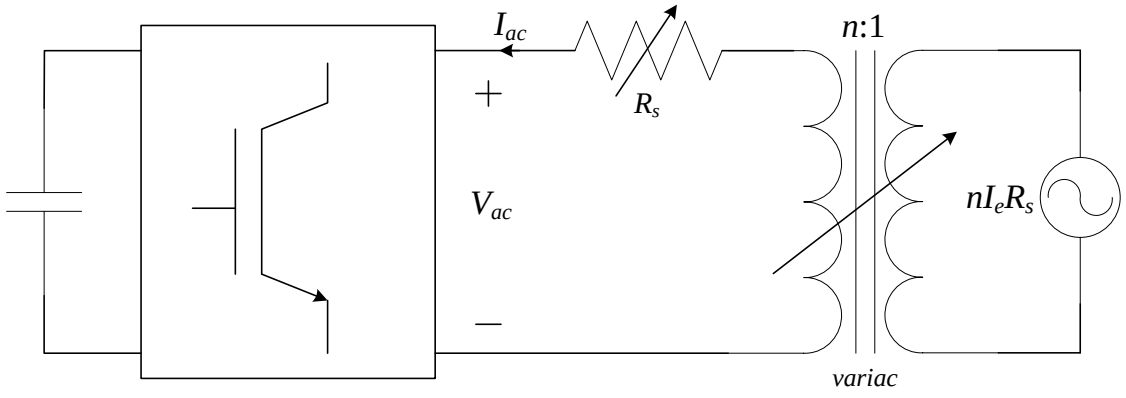


Figure 4.7: VSI hardware test setup, with a voltage source and series resistance to emulate a current source

The other difference is that the filter for the DSSC application does not include the grid-side inductor L_g, as explained in Section 3.3.3.

4.2.1 AC synchronization

In a grid-tied inverter application, it is necessary to synchronize the inverter ac-side signals with the phase and frequency of the connected system. Typically, synchronization is achieved with a phase-locked loop (PLL), wherein a feedback loop measures the grid voltage or current and controls the phase of the inverter ac reference signal. PLLs have been well-studied, both for single-phase [38–40] and three-phase [41–43] systems, as well as for FACTS applications specifically [44].

A simple PLL was developed for this system and demonstrated in simulation. However, the computational burden of the PLL, requiring fast measurements and floating point calculations, was too great for it to be implemented in the microcontroller. Instead, synchronization is achieved by detecting the zero-crossings of the ac signals. At its simplest – for example, where the VSI acts as a current source connected to a voltage source – the controller jumps to the first index of a sinusoidal current reference lookup table each time the grid voltage crosses zero. Additionally, the control system must track the sign of the grid voltage to ensure power flow in the correct direction.

The hardware developed for this work also uses a software latch to aid the synchronization. Merely reacting to zero-crossings would cause many unintended consequences, as noise in the measurement may result in multiple detected zero-crossings when the measured signal crosses zero only once. This is especially problematic in this design because the current sensors (rated for 50 A) have poor resolution at low current. The control system code reduces this problem first by averaging the current measurement over 16 switching cycle samples. The problem is further reduced by locking out the zero crossing detection immediately after one crossing is detected per half-cycle. When a zero-crossing is detected, the zero-crossing code is disabled for the next 20 averaged current measurements, ensuring that the next detected zero-crossing does not occur until the next half cycle.

For this VSI application, additional detection and control is necessary. The three-level switch-

ing control method, combined with the 90° phase lag of v_{ac} relative to i_{ac}, requires the zero-crossings to be detected independently of the i_ℓ zero crossings. First, the v_{ac} reference lookup table is a cosine function. Whenever i_{ac} crosses from negative to positive, the lookup table is reset to its 0 index. Second, when the lookup table index, which is incremented 256 times per ac cycle, reaches the index for which v_{ac} crosses zero, the bridge legs are swapped. Assuming that the phase and frequency of i_{ac} are steady, this enforces the synchronization of v_{ac} at 90° relative to i_{ac}. Section 4.2.3 discusses how the synchronization may be altered to control the flow of real power in the VSI.

4.2.2 SPWM ac-side regulation

SPWM control must use a control system similar that described in Section 4.1.3 to regulate the ac-side waveform. The DSSC application requires some important modifications, however. One is the three-level switching, as discussed above. The other is that the application is a VSI connected to a stiff current source. These differences result in the switching-averaged model shown in Fig. 4.8.

Perturbing and linearizing the model in Fig. 4.8 results in the small-signal ac model shown in Fig. 4.9. The transfer function relating duty cycle perturbations to ac-side voltage perturbations is required to design the closed loop control system. It is assumed that both v_{dc} and i_{ac} are constant over the time scale of a switching period, resulting in the small signal model shown in Fig. 4.10.

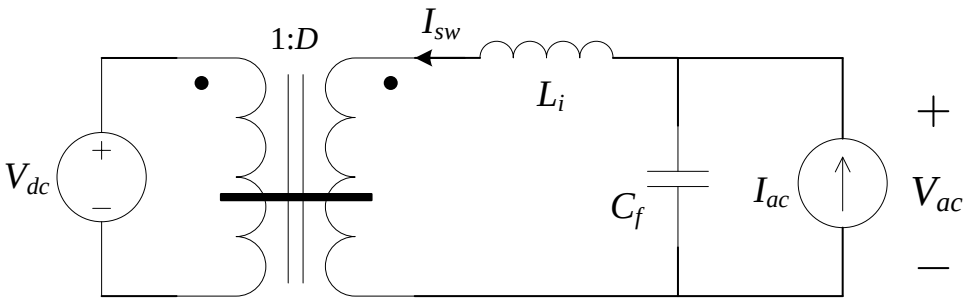


Figure 4.8: Switching-averaged model of DSSC VSI

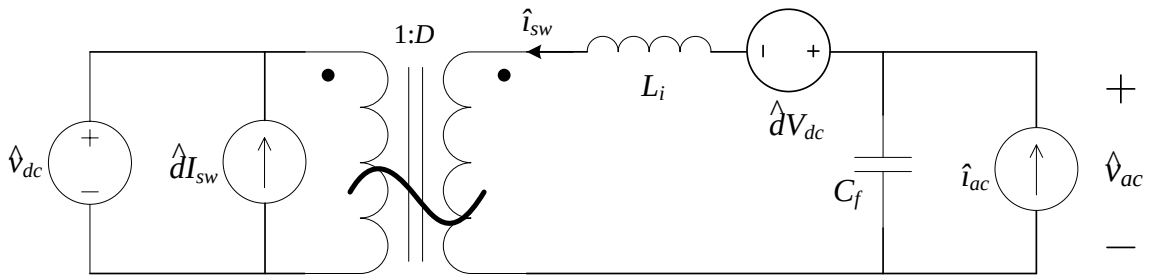


Figure 4.9: Small signal ac model of DSSC VSI

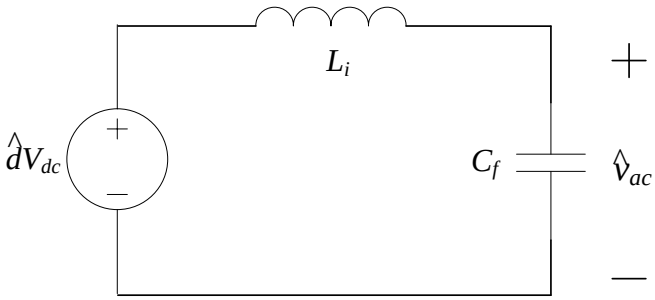


Figure 4.10: Reduced small signal ac model of DSSC VSI

This model may be solved to find the control-to-output transfer function:

$$\frac{\hat{v}_{ac}}{\hat{d}} = \frac{V_{dc}}{1 + s^2 L_i C_f}. \tag{4.14}$$

This expression for $\hat{v}_{ac}/\hat{d}$ is incomplete, however, as the filter also includes a resistor R_f in series with C_f. The n-extra element theorem may be employed to find the effect of R_f [50]. The modified transfer function is:

$$\frac{\hat{v}_{cf}}{\hat{d}} = \left(\frac{\hat{v}_{ac}}{\hat{d}}\bigg|_{R_f \to 0} \right) \left(\frac{1 + \frac{R_f}{Z_N(s)}}{1 + \frac{R_f}{Z_D(s)}} \right), \tag{4.15}$$

where $\hat{v}_{cf}$ is the voltage across C_f: $\hat{v}_{cf} \neq \hat{v}_{ac}$ with the insertion of R_f. Z_D is the Thévenin equivalent of the model circuit as seen from R_f, while Z_D is the equivalent impedance of the circuit as seen

from R_f but with the input source present and $v_{ac} \to 0$. The correction term reduces to

$$\frac{1+\frac{R_f}{Z_N(s)}}{1+\frac{R_f}{Z_D(s)}} = \frac{1+s^2L_iC_f}{1+sR_fC_f+s^2L_iC_f}, \tag{4.16}$$

and the resulting transfer function is

$$\frac{\hat{v}_{cf}}{\hat{d}} = \frac{V_{dc}}{1+sR_fC_f+s^2L_iC_f}. \tag{4.17}$$

The transfer function for $\hat{v}_{ac}$ may be found by finding the voltage across R_f –

$$\hat{v}_{rf} = \hat{d}V_{dc} - \hat{v}_{cf} \tag{4.18}$$

– and adding it to $\hat{v}_{cf}$ to find the actual control-to-output transfer function:

$$G_{vd}(s) = \frac{\hat{v}_{ac}}{\hat{d}} = V_{dc}\frac{1+sR_fC_f}{1+sR_fC_f+s^2L_iC_f}. \tag{4.19}$$

Note that the VSI dynamics do not depend on any of the ac quantities in this application. In other cases, it may be necessary to calculate $G_{vd}(s)$ at different points in the ac cycle, but here the transfer function is approximately independent of v_{ac} and i_{ac}.

The complete uncompensated feedback loop also includes the sensor gain H_{sense} and the pulse-width modulator gain V_m:

$$T_u(s) = \frac{G_{vd}(s)H_{sense}}{V_m}. \tag{4.20}$$

The Bode plot of T_u is shown in Fig. 4.11. As with the original inverter design in Section 4.1, it is desired to achieve high gain at f_ℓ. It may also be desired to control the phase margin ϕ_m precisely. In order to control the phase margin, a PID compensator is designed:

$$G_{c,ac}(s) = G_{cm}\frac{\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{\frac{s}{\omega_{z2}}\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)}. \tag{4.21}$$

The crossover frequency should be above the filter resonant frequency $f_0 = 4.32$ kHz and sufficiently lower than f_{sw}: let $f_c = \frac{1}{3}f_{sw} = 9.17$ kHz. In order to achieve a desired phase margin $\phi_m = 45°$, f_{z1} and f_{z2} can be found:

$$f_{z1} = f_c\sqrt{\frac{1-\sin(\phi_m)}{1+\sin(\phi_m)}} = 3.80 \text{ kHz} \tag{4.22a}$$

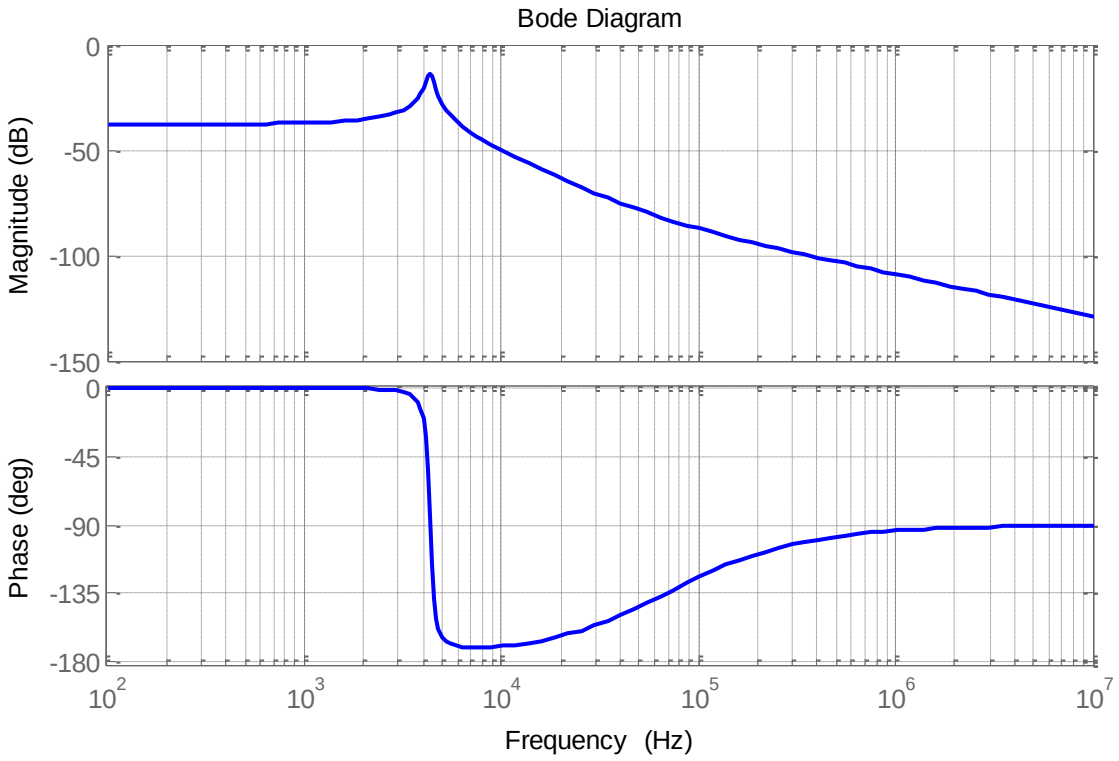


Figure 4.11: Bode plot of VSI $G_{vd}(s)$ response for DSSC SPWM application

$$f_{z1} = f_c\sqrt{\frac{1+\sin(\phi_m)}{1-\sin(\phi_m)}} = 22.1 \text{ kHz}. \tag{4.22b}$$

As in Section 4.1.3, the PI frequency is chosen so that $f_\ell < f_{z2} < f_c$; again, let $f_{z2} = 1$ kHz. Also, the upper pole frequency should be sufficiently greater than f_{sw} so that it suppresses switching harmonics without interfering with the design: let $f_{p2} = 2f_{sw} = 55$ kHz. Finally, the gain G_{cm} is adjusted so that the desired crossover frequency is met: $G_{cm} = 190.5$. The design parameters are summarized in Table 4.3. The total closed loop gain is shown in Fig. 4.12.

The VSI has been modeled using PLECS simulation software. In this case, only the ac regulation loop is tested, so a fixed voltage source is connected to the dc bus: $V_{dc} = 350$ V. Fig. 4.13 shows the results of the simulation. The ac-side voltage tracks the reference well, with minimal distortion (THD $< 5\%$). There is distortion near the v_{ac} zero-crossing, however, because the legs need to alternate and because the duty cycle is difficult to control near 0.

In order to implement the compensator in the hardware, it must be converted to the discrete-

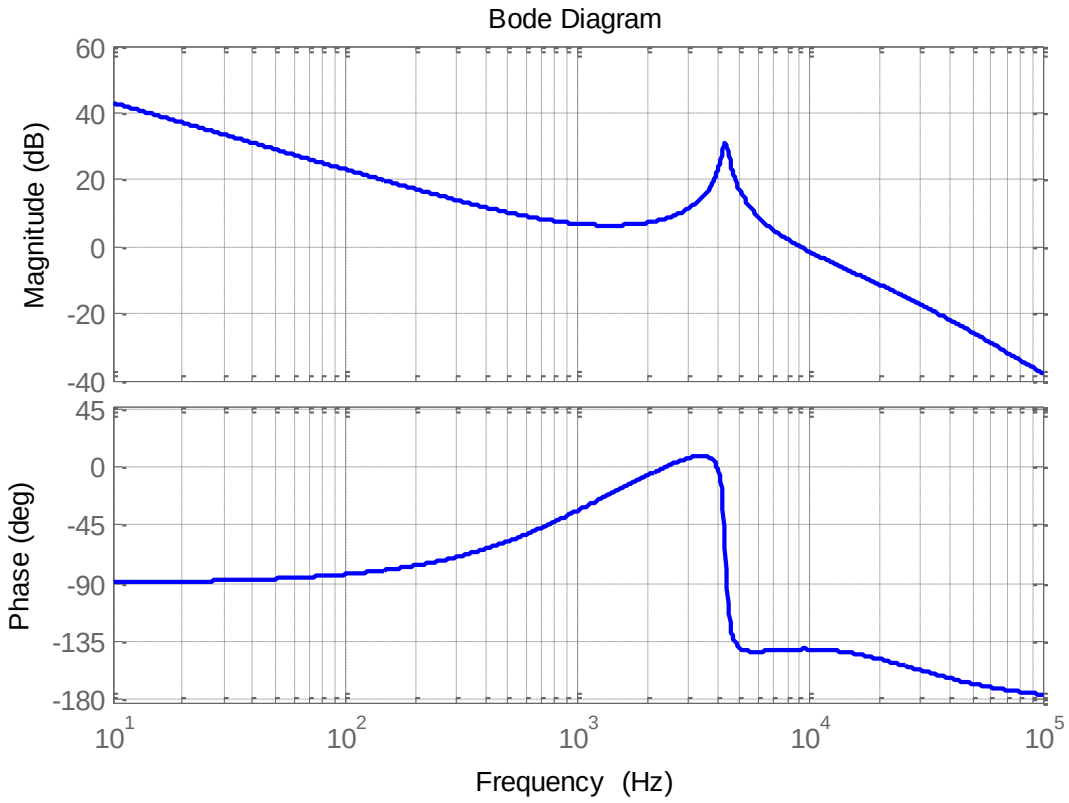


Figure 4.12: Bode plot of VSI v_{ac} closed loop gain for DSSC SPWM application

time Z-domain. The dsPIC PWM module is programmed to update the duty cycle 256 times per line cycle, so the sampling rate is $f_s = 1/(256 \cdot 60) = 15.4$ kHz. Employing a sample-and-hold conversion at f_s produces the following discrete-time transfer function:

$$G_{c,ac}[z] = \frac{d[z]}{e[z]} = \frac{189.5z^{-1} - 135.8z^{-2} + 0.121z^{-3}}{1 - z^{-1} + 1.17 \cdot 10^{-4}z^{-2} - 1.53 \cdot 10^{-13}z^{-3}}, \tag{4.23}$$

which can be expressed as a difference function for implementation:

$$\begin{aligned} d[k] &= 189e[k-1] - 135.8e[k-2] + 0.121e[k-3] \\ &\quad + d[k-1] - 1.14 \cdot 10^{-4}d[k-2] + 1.53 \cdot 10^{-13}d[k-3]. \end{aligned}$$

4.2.3 SPWM dc-side regulation

Unlike with many VSI applications, there is nothing to fix the dc-side voltage of this system. Moreover, under ideal steady-state conditions, there is no real power flowing through the VSI to

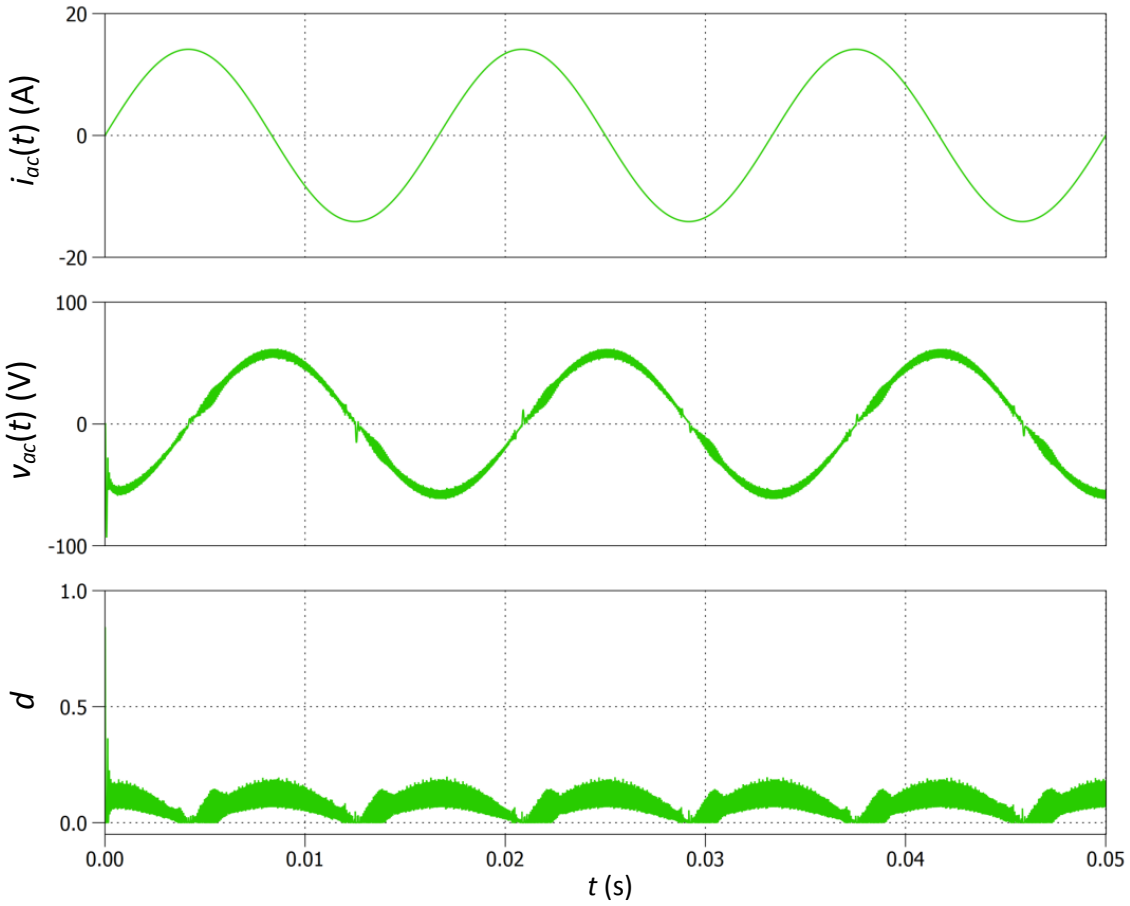


Figure 4.13: Simulation of VSI ac-side regulation, with $v_{ac} = 41.6\text{V}_{\text{rms}}$ and $i_{ac} = 10\text{A}_{\text{rms}}$

regulate V_{dc} and charge or discharge C_{dc}. In this application, v_{ac} must lag i_{ac} by 90°. The flow of real power to C_{dc} is accomplished by controlling the phase difference ϕ between the SPWM duty cycle signal, and thus v_{ac}, and i_{ac}.

The relation between ϕ and real power flow can be found by modeling the loss in the VSI with a resistor R_{dc} parallel to C_{dc}. They form an equivalent dc-side impedance $Z_{dc} = R_{dc}||1/(\omega_\ell C_{dc})$. Under ideal conditions, where $R_{dc} = \infty$, $\phi = \pi/2$. If real power is required to supply lossy elements, there must be some phase offset $\delta = \pi/2 - \phi > 0$. The steady-state value of δ necessary to maintain V_{dc} – that is, the value of δ such that the real power into the VSI equals the power loss – is

$$\delta_0 = \frac{\pi}{2} - \tan^{-1}\left(\omega_\ell C_{dc} R_{dc}\right). \tag{4.24}$$

The resulting real power into Z_{dc} is

$$P_{dc} = V_{ac} I_{ac} \sin \delta_0 = \frac{{v_{dc}}^2}{Z_{dc}}, \tag{4.25}$$

which may be perturbed and linearized:

$$V_{ac} I_{ac} (\hat{\delta} \cos \delta_0 + \sin \delta_0) = ({V_{dc}}^2 + 2 V_{dc} \hat{v}_{dc}). \tag{4.26}$$

This may be solved, after eliminating the steady-state components, to find the small signal transfer function $G_{v\delta}(s)$ relating $\hat{v}_{dc}$ to $\hat{\delta}$:

$$G_{v\delta}(s) = \frac{\hat{v}_{dc}}{\hat{\delta}} = \frac{V_{ac} I_{ac} {R_{dc}}^2 \omega_\ell C_{dc}}{V_{dc} \sqrt{1 + (\omega_\ell C_{dc} R_{dc})^2}} \cdot \frac{1}{1 + s R_{dc} C_{dc}}. \tag{4.27}$$

(Recall that V_{ac} and I_{ac} are rms values.)

The v_{dc}-δ loop, shown in Fig. 4.14, also includes gains related to the microcontroller, as well as an averaging filter to eliminate the common-mode noise from the V_{dc} sensor measurement. First, the sensor gain, using the circuit from Fig. 4.2, is $H_{sense} = -1.4$. This incorporates both the gain of the analog sensor and the ADC conversion from a 0-3.3 V scale to a 0-512 scale in the microcontroller memory. Next, the averaging filter, which operates over samples of length $T_\ell = 1/f_\ell$, may be approximated as a first-order Padé function:

$$G_{avg}(s) = \frac{1}{s T_\ell} \left(1 - e^{-T_\ell s}\right) \approx \frac{1}{s T_\ell} \left(1 - \frac{1 - \frac{1}{2} T_\ell s}{1 + \frac{1}{2} T_\ell s}\right) = \frac{1}{1 + \frac{1}{2} T_\ell s}. \tag{4.28}$$

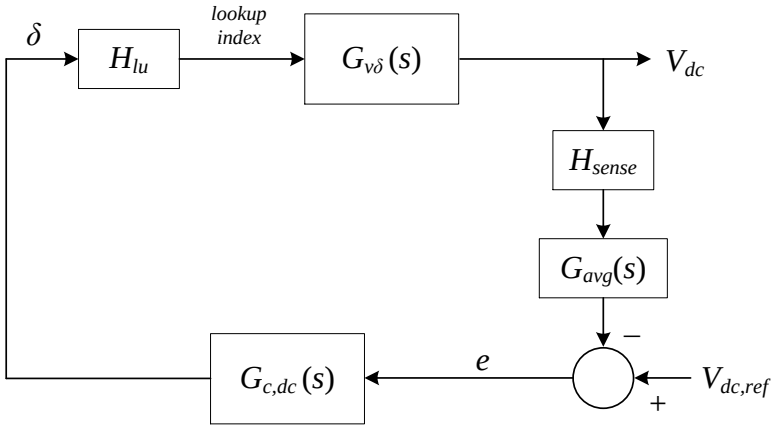


Figure 4.14: Control loop diagram for V_{dc} regulation

Finally, the loop includes a gain term representing the quantization of δ. The v_{ac} reference signal is generated from a lookup table that maps a 60 Hz sinusoid to a 256-point array. Therefore, 360° of phase adjustment is equivalent to shifting the lookup table by all 256 points: $H_{lu} = \pi/128$. The total uncompensated loop gain is shown in Fig. 4.15.

In order to approximate R_{dc}, first consider the case where it is ignored; that is, $R_{dc} \to \infty$. The v_{dc} transfer function (4.27) is reduced to

$$G_{v\delta}(s)\Big|_{R_{dc}\to\infty} = \frac{V_{ac}I_{ac}}{V_{dc}} \cdot \frac{1}{sC_{dc}}. \tag{4.29}$$

Without R_{dc}, the feedback loop only requires a proportional compensator to achieve near-zero steady-state error. However, if a proportional compensator is implemented in hardware, there will be some steady-state error due to real power loss; this error may be used to estimate R_{dc}.

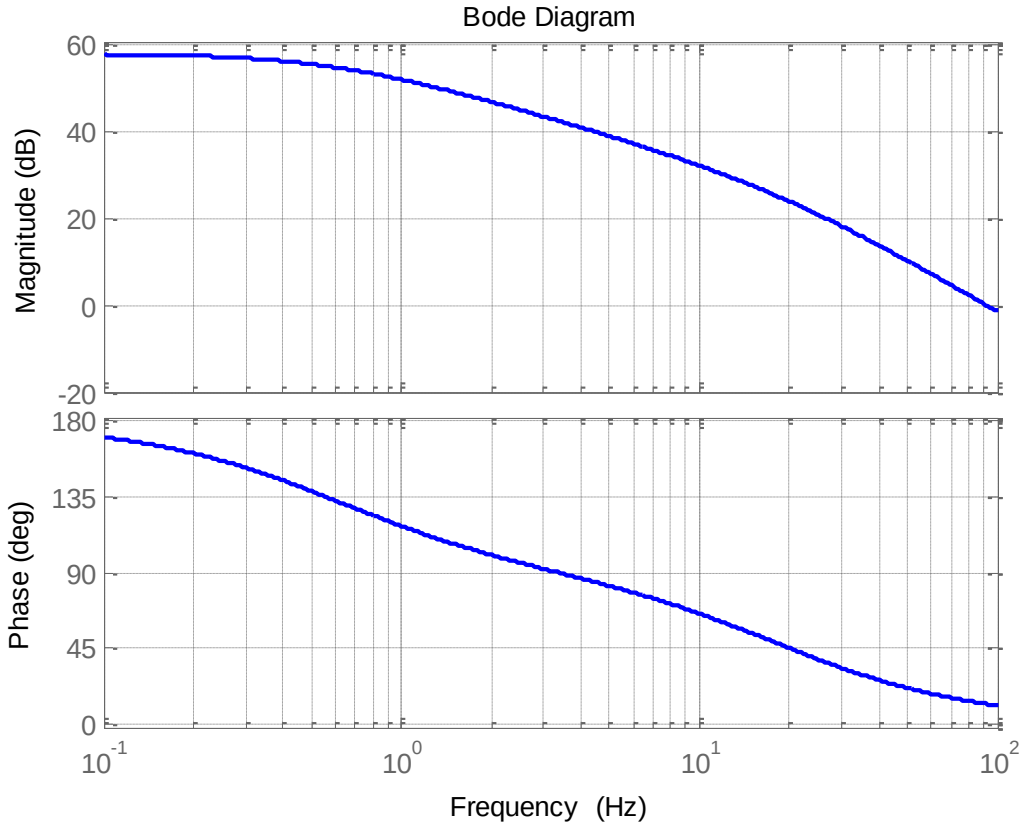


Figure 4.15: Bode plot of VSI uncompensated V_{dc} closed loop gain for DSSC SPWM application

The dc-side control loop is designed with $R_{dc} = 2.7$ kΩ, which was found by a trial and error comparison of the circuit simulation with the measured steady-state value of V_{dc} in hardware. The dc-side regulation must be very slow, and a sufficient compensator may be designed without an exact value of R_{dc}. However, R_{dc} may be estimated more precisely if necessary. From the control loop in Fig. 4.14, the steady-state error is related to the measured V_{dc} as

$$V_{dc} = eG_{c,dc}H_{lu}G_{v\delta}(0) = (V_{dc,ref} - H_{sense}V_{dc})G_{c,dc}H_{lu}G_{v\delta}(0), \tag{4.30}$$

where $G_{c,dc}$ is a scalar. The actual dc gain of $G_{v\delta}$, from (4.27), is

$$G_{v\delta}(0) = \frac{V_{ac}I_{ac}{R_{dc}}^2\omega_\ell C_{dc}}{V_{dc}\sqrt{1 + (\omega_\ell C_{dc}R_{dc})^2}}, \tag{4.31}$$

so (4.30) may be solved for R_{dc}:

$$R_{dc} = \frac{{V_{dc}}^2\sqrt{1 + \sqrt{1 + \left[\frac{2(V_{dc,ref} - H_{sense}V_{dc})(G_{c,dc}H_{lu}V_{ac}I_{ac})}{\omega_\ell C_{dc}{V_{dc}}^2}\right]^2}}}{\sqrt{2}(V_{dc,ref} - H_{sense}V_{dc})(G_{c,dc}H_{lu}V_{ac}I_{ac})}. \tag{4.32}$$

This derivation of R_{dc} was validated in hardware with reasonable success. The specifications used for the hardware test were slightly different than those in Section 4.3: $C_{dc} = 275$ μF, $V_{ac} = 34$ V_{rms}, $I_{ac} = 4$ A_{rms}, and $G_{c,dc} = 1/16$. $V_{dc,ref}$, H_{sense}, and H_{lu} are the same, and V_{dc} is measured to be 282 V. Using (4.32), $R_{dc} = 4$ kΩ, which is sufficiently close to the value used (2.7 kΩ) that the compensator will work as required. It is possible that, under the conditions used in Section 4.3, the measured value of R_{dc} is closer to 2.7 kΩ.

Given R_{dc}, the actual v_{dc} compensator $G_{c,dc}$ must be designed so that the loop gain has very high gain at dc and that the crossover frequency $f_c < 60$ Hz. In this case, it is necessary to preserve the dc-side ripple in order to maintain the proper power balance. A simple integral compensator, with a gain chosen to achieve a desired phase margin $\phi_{m,dc}$, is sufficient. Finally, the gain must be negative to account for $H_{sense} < 0$. For a critically damped phase margin of $\phi_{m,dc} = 76^\circ$,

$$G_{c,dc}(s) = \frac{-8.16 \cdot 10^{-3}}{s}, \tag{4.33}$$

found empirically, and $f_c = 0.138$ Hz. These results are summarized in Table 4.3.

Table 4.3: DC- and ac-side regulation parameters and design for SPWM control

Operation	DC Loop $G_{c,dc}(s) = \frac{G_{cm}}{s}$	AC Loop $G_{c,ac}(s) = G_{cm}\frac{\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{\frac{s}{\omega_{z2}}\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)}$
AC-side current I_{ac} (A_{rms})	10	n/a
AC-side voltage V_{ac} (V_{rms})	41.6	n/a
DC-side voltage V_{dc} (V)	350	350
Phase margin ϕ_m (degrees)	30	45
Design		
G_{cm} (V)	$-8.16 \cdot 10^{-3}$	110
f_{z1} (Hz)	n/a	3,797
f_{z2} (Hz)	n/a	1,000
f_{p1} (Hz)	n/a	22,130
f_{p2} (Hz)	n/a	55,000
f_c (Hz)	0.138	9,167

The dc-side regulation is validated in simulation, the results of which are shown in Figs. 4.16 and 4.17. In Fig. 4.16, a SPWM reference lookup table is not used, so the reference phase offset is not discretized. The gain is adjusted to exclude the phase-to-lookup table conversion, so $G_{c,dc}(s) = -2 \cdot 10^{-4}/s$. V_{dc} ramps up slowly due to the low bandwidth of the control loop.

In contrast, Fig. 4.17 shows the results of a simulation where the lookup table is used. Because the lookup table discretizes δ, the exact phase offset value cannot be reached, causing V_{dc} to oscillate as the compensator steps between the lookup table values nearest the required offset. This oscillation grows with V_{ac} and I_{ac}, as increased power into the dc side ramps V_{dc} up and down more quickly.

To implement the compensator in the microcontroller, it is converted to the Z-domain, as before. The sampling rate here is limited to f_ℓ, the same as the averaging interval. The discrete-time compensator is

$$G_{c,dc}[z] = \frac{\delta[z]}{e[z]} = \frac{-1.36 \cdot 10^{-4} z^{-1}}{1 - z^{-1}}, \tag{4.34}$$

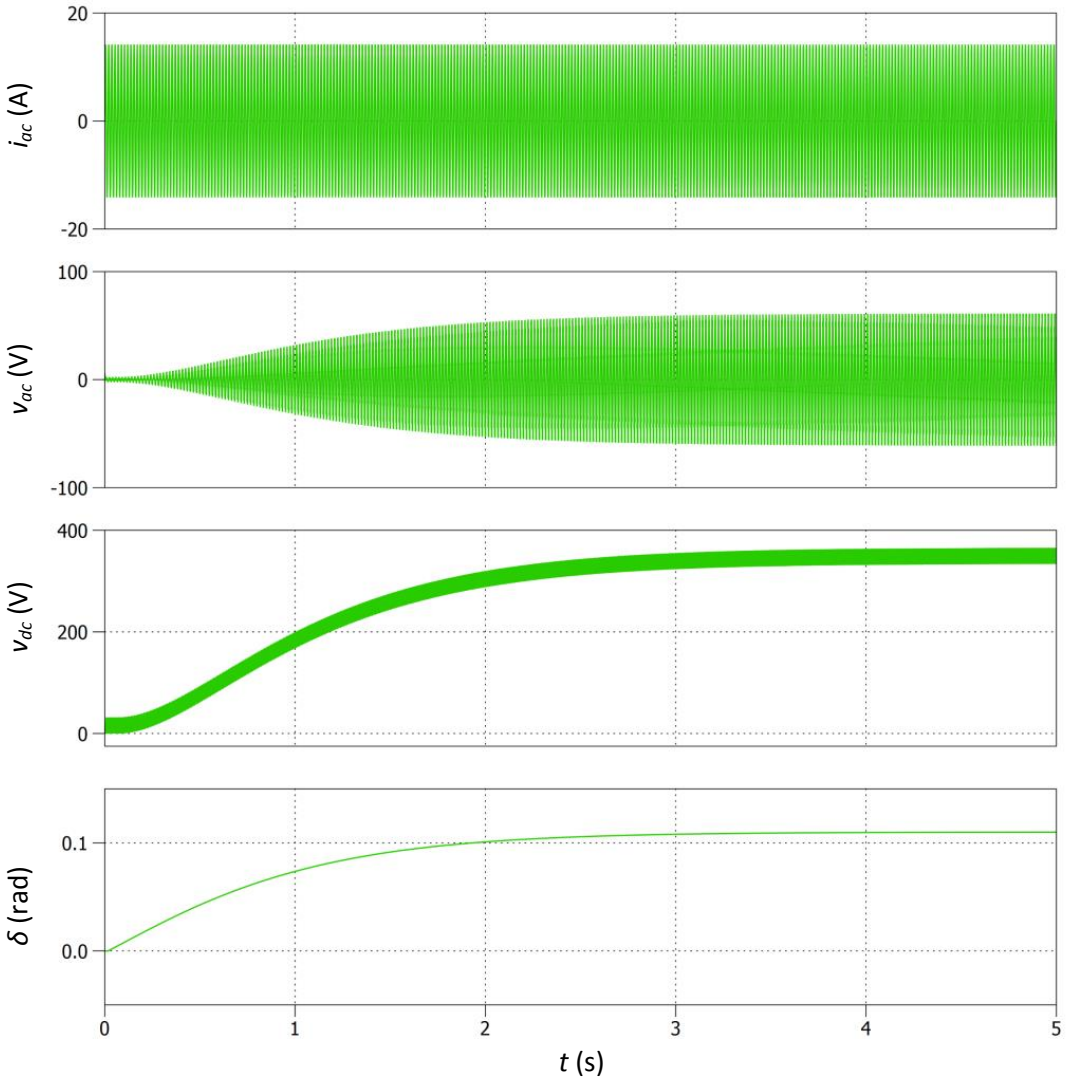


Figure 4.16: Simulation of VSI dc-side regulation, with $v_{ac} = 41.6\text{V}_{\text{rms}}$ and $i_{ac} = 10\text{A}_{\text{rms}}$ and no use of a lookup table

which can be converted to the difference function

$$\delta[k] = -1.36 \cdot 10^{-4} e[k-1] + \delta[k-1].$$

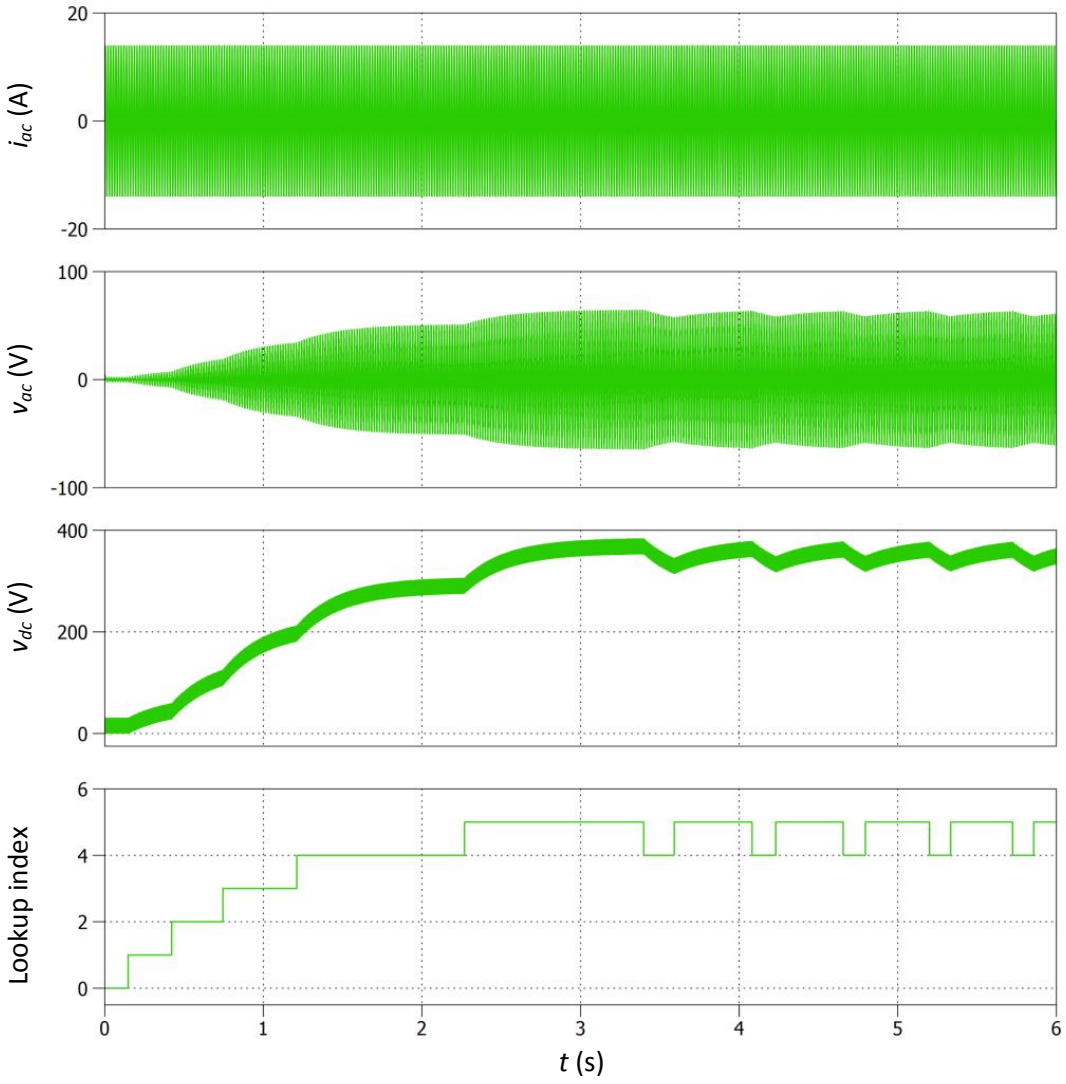


Figure 4.17: Simulation of VSI dc-side regulation, with $v_{ac} = 41.6\text{V}_{\text{rms}}$, $i_{ac} = 10\text{A}_{\text{rms}}$ and sinusoid reference lookup table employed

4.2.4 SPWM control with ac- and dc-side regulation

Fig. 4.18 shows the complete block diagram of the VSI and its control system. Figs. 4.19 and 4.20 show the behavior of the simulated VSI with both control loops implemented. The effects seen in Figs. 4.13 and 4.17 are present in the full system as well: the shape of v_{ac} is properly sinusoidal, but with ringing at the zero-crossings, while V_{dc} oscillates with the cycling of the lookup

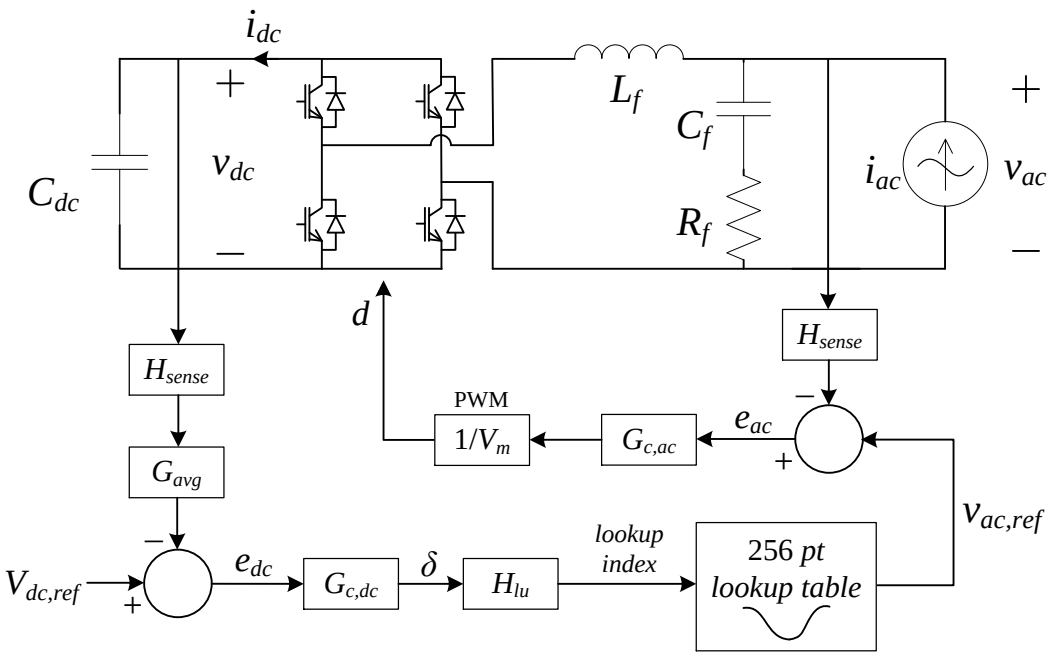


Figure 4.18: Complete feedback system for VSI SPWM control

table index. Note that the regulation of v_{ac} allows it to maintain the desired magnitude while V_{dc} oscillates.

When both control loops are implemented in hardware, however, interaction between the loops and the synchronization process prevent the V_{dc} from ramping up properly. Consequently, the control loops need to be altered. $G_{c,dc}(s)$ remains an integral controller, but its discrete-time gain is changed to -1/4096:

$$G_{c,dc}[z] = \frac{-1}{4096} \cdot \frac{1}{z-1}. \tag{4.35}$$

Power-of-two multipliers and divisors are advantageous for their computational efficiency, and this value is approximately equal to the original value, while providing a slightly higher bandwidth – the equivalent continuous-time compensator is $G_{c,dc}(s) = -0.0147/s$, for a bandwidth of 0.267 Hz and phase margin of 67°.

$G_{c,ac}(s)$ is simplified to an integral compensator as well. Refer to Fig. 4.11: a low bandwidth

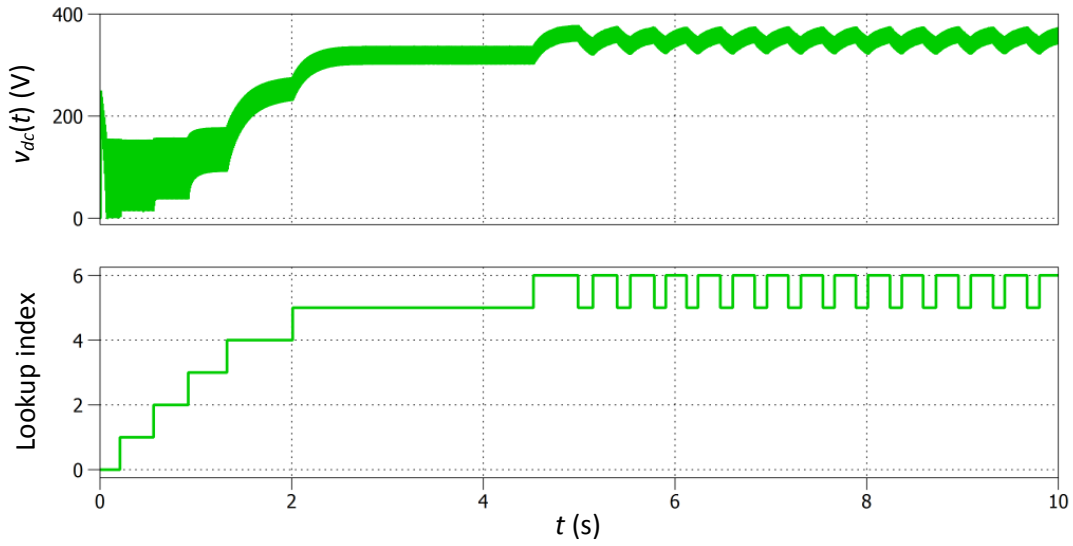


Figure 4.19: Long-time scale simulation of VSI with ac- and dc-side regulation implemented

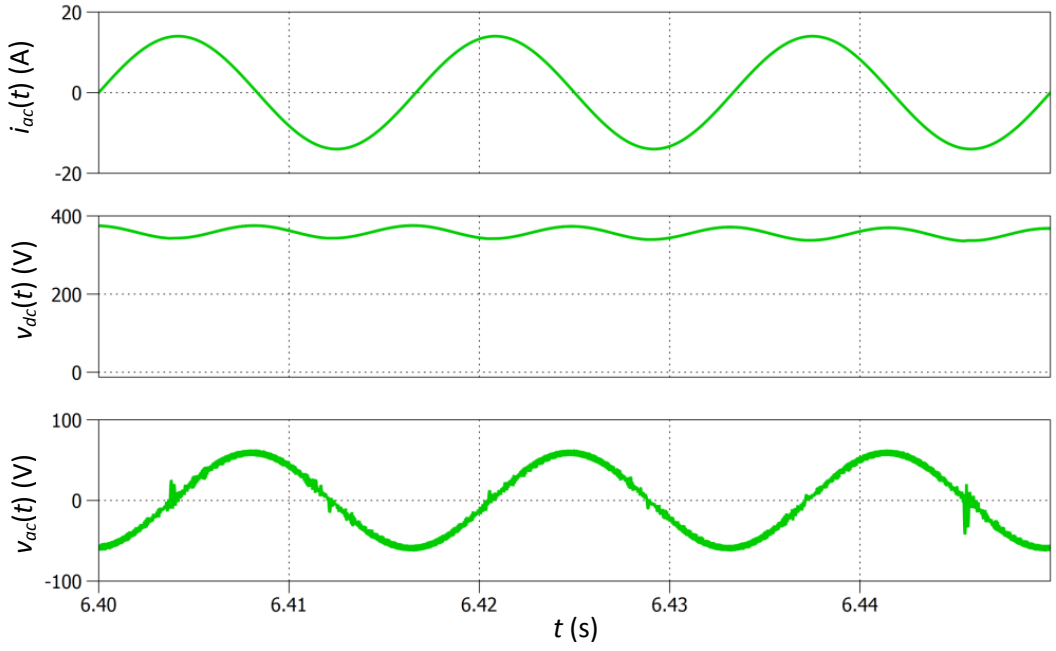


Figure 4.20: Short-time scale simulation of VSI with ac- and dc-side regulation implemented

control loop can be implemented, using an integrator, with a crossover frequency below the second-order dynamics. The discrete time integrator gain is chosen to be 16, again a power of two for computational efficiency:

$$G_{c,ac}[z] = \frac{16}{z-1}. \tag{4.36}$$

The equivalent continuous-time compensator is $G_{c,ac}(s) = \frac{245760}{s}$, for a bandwidth of 517 Hz and a phase margin of 90°. This bandwidth is low by the standards of most converter systems, but is high enough to suppress many harmonics of f_ℓ.

The hardware experiment results of the full system, with both control loops, is presented in Section 4.3.

4.2.5 Constant duty cycle control

One of the advantages of constant duty cycle control of the VSI is its simple implementation. The inverter operates similar to a dc-dc synchronous buck converter, where the dc-side voltage is stepped down to the ac-side. The H-bridge may be modeled as a transformer with a turns ratio of $1 : D$ and a polarity that reverses every half-cycle of v_{ac}, so that $v_{dc}(t) = |v_{ac}(t)|$. Taking one quarter cycle at a time, C_{dc} may be reflected through this transformer, so that at f_ℓ the VSI is modeled solely as a capacitor equal to C_{dc}/D^2. The capacitor voltage is driven directly by the stiff current source i_{ac}, so there is no need for regulation of v_{dc}. Three-level switching ensures that v_{ac} is a rectified sinusoid, and the capacitor behavior ensures that v_{ac} is 90° out of phase with i_{ac}. Likewise, v_{ac} is simply a reflection of v_{dc} through the transformer, with reversing polarity, so there is no need to regulate the shape of v_{ac} with a feedback loop.

It would be difficult to regulate the ac-side voltage using conventional linear control system methods. Equation (4.19) indicates that, under ideal conditions, the only operating point on which the control-to-output transfer function depends is v_{dc}. Because v_{dc} swings from its maximum value $V_{dc,max}$ to 0, a single compensation system, as in (4.21), would be unable to control v_{ac} with satisfactory phase margin and bandwidth across the entire grid cycle.

Instead, it should be sufficient to rely on the circuit to set its duty cycle according to (3.26)

for a desired X_{inj} given a measured I_ℓ. This can be done slowly and without the use of negative feedback, because the line current in a transmission system is not expected to change abruptly. Further research may be directed toward designing a control system that ramps slowly between different values of D.

Fig. 4.21 shows the results of a PLECS simulation of a VSI with constant duty cycle control. Two operating points are demonstrated: low I_{ac} and high D, corresponding to inductive X_{inj}; and high I_{ac} and low D, corresponding to capacitive X_{inj}. In both cases, v_{dc}, as expected, is a rectified sinusoid with $V_{dc,max}$=350 V. The only control is the alternating of H-bridge legs for three-level switching. The filter eliminates switching ripple very well, and, aside from a small startup transient, the circuit operation is nearly ideal.

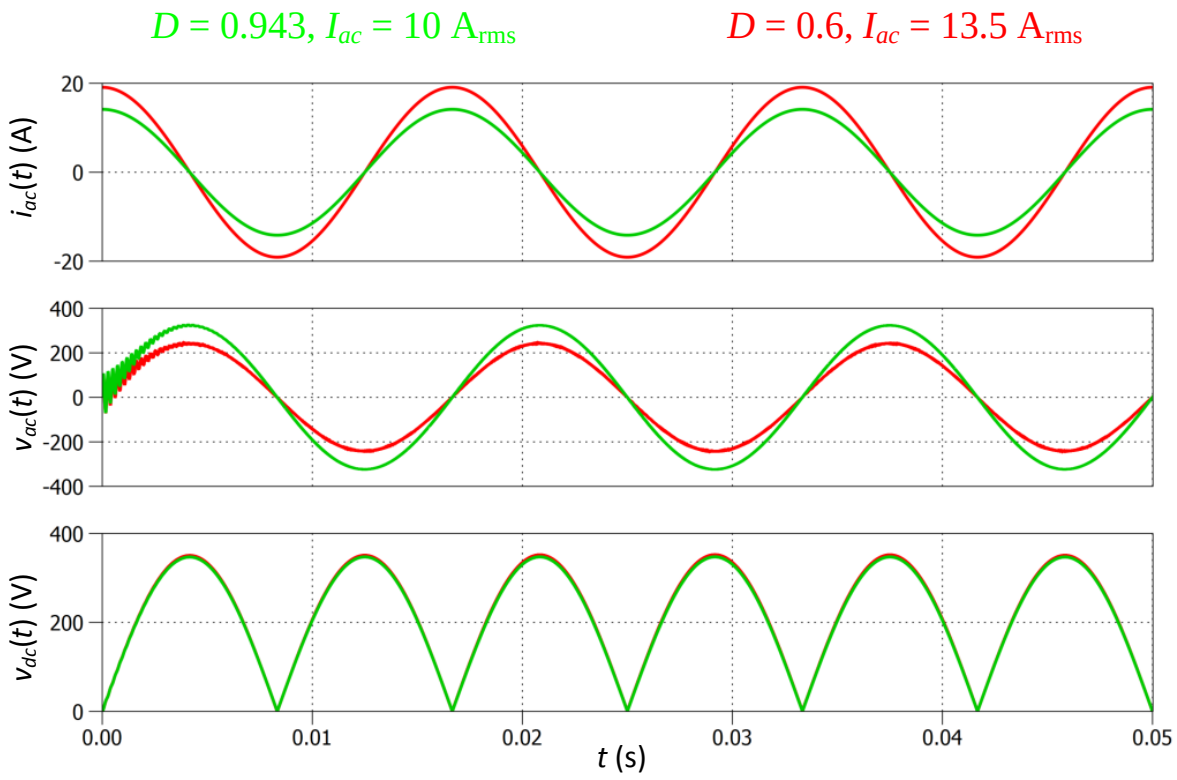


Figure 4.21: Simulation of constant duty cycle control under two different operating conditions

4.3 Hardware Experiments

This section presents hardware experiment results to demonstrate the operation of both control schemes and the benefit of constant duty cycle control over SPWM control. The tests relate to the VSI; an STT was not built for this system. First, the ac-side and dc-side regulation loops for SPWM control were tested independently. Fig. 4.22 shows hardware test results for the compensator given in (4.23), with a fixed voltage source on the dc bus of $V_{dc} = 100$ V. The hardware results do not show the same tight regulation as in the simulation, with some distortion due to high-frequency ringing. This ringing may be due to unmodelled hardware non-idealities not accounted for in the compensator design.

The dc-side control loop is tested with the duty cycle commands coming directly from the v_{ac} reference lookup table and scaled for the appropriate value of V_{ac}. That is, the ac-side control loop is not used. Both circuits are driven using two high-power rheostats ($R_{s1} = 14.2\ \Omega$ and

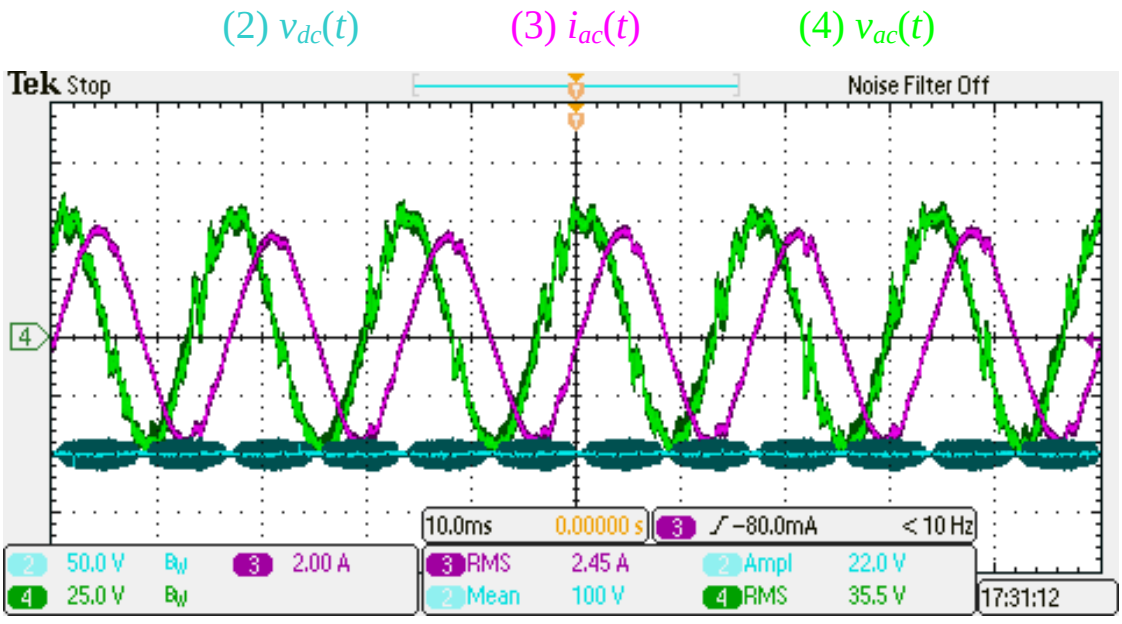


Figure 4.22: Hardware test of VSI ac-side regulation, with $v_{ac} = 41.6\text{V}_{\text{rms}}$, $i_{ac} = 10\text{A}_{\text{rms}}$, and $V_{dc} = 100$ V

$R_{s2} = 16.8\ \Omega$) connected in series between the VSI and a single-phase variac fed by the grid.

Figs. 4.23 and 4.24 show results from one hardware test of the v_{dc} control loop. Fig. 4.23 uses a horizontal scale of 10 ms per division, and Fig. 4.24 uses 1 s per division. Fig. 4.23 shows that without ac-side regulation, the v_{ac} waveform exhibits distortion at the i_{ac} zero-crossings. Fig. 4.24 shows the oscillating effect of phase discretization discussed in Section 4.2.3.

Fig. 4.25 shows the performance of SPWM control using both loops, simplified as described in Section 4.2.4. The regulation of the shape of v_{ac}, relative to Fig 4.22, is improved thanks to the simplified compensator. The operating points are chosen to use all the energy available in C_{dc} when $r = 5\%$. The VSI is driven with $I_{ac} = 10\ \mathrm{A_{rms}}$, and the resulting ac-side voltage is $V_{ac} = 41.7\ \mathrm{V_{rms}}$. Fig. 4.25 shows the ac-side voltage and current, dc-side voltage, and duty cycle, scaled as the output of the microcontroller DAC.

Figs. 4.26 and 4.27 show the results of the same hardware test on the switching time scale. The displayed waveforms are i_{dc}, v_{sw}, i_{sw}, and v_{ac}. Fig. 4.27 captures the operation near $v_{ac} = 0$ and Fig. 4.26 near the maximum value of v_{ac}. This scale highlights the similarity of the VSI to

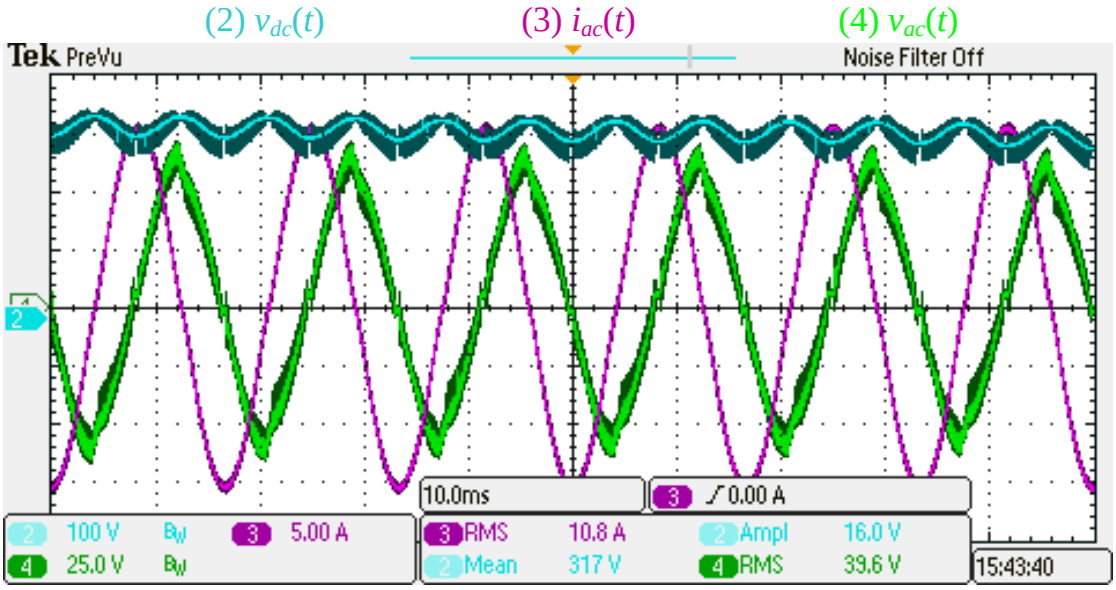


Figure 4.23: Hardware test of VSI dc-side regulation, with $v_{ac} \approx 40\mathrm{V_{rms}}$ and $i_{ac} = 10\mathrm{A_{rms}}$; horizontal scale is 10 ms per division

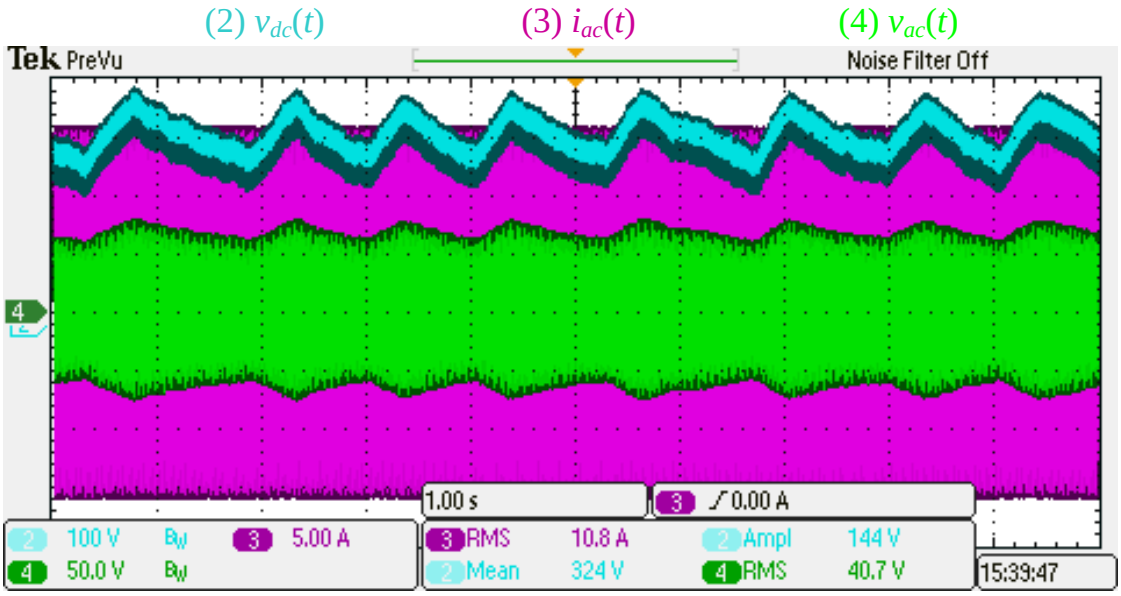


Figure 4.24: Hardware test of VSI dc-side regulation, with $v_{ac} \approx 40\text{V}_{\text{rms}}$ and $i_{ac} = 10\text{A}_{\text{rms}}$; horizontal scale is 1 s per division

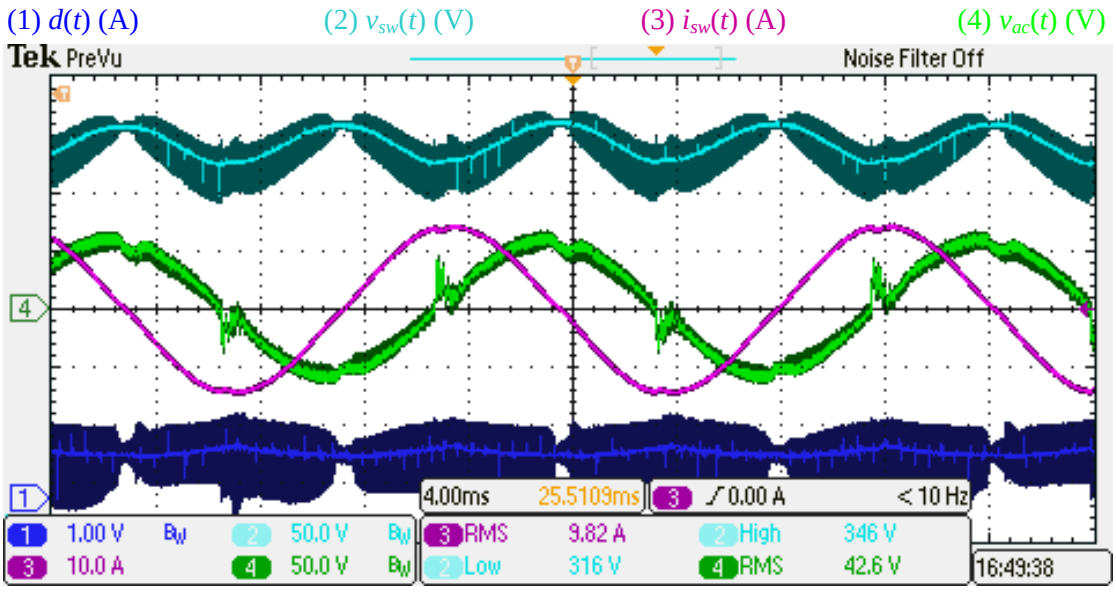


Figure 4.25: Hardware test of VSI under SPWM control with both ac- and dc-side regulation

an ordinary dc-dc buck converter. The switch node voltage v_{sw} steps between 0 and V_{dc}, which causes the filter inductor current i_{sw} to ramp up and down. The filtered voltage, v_{ac}, shows the

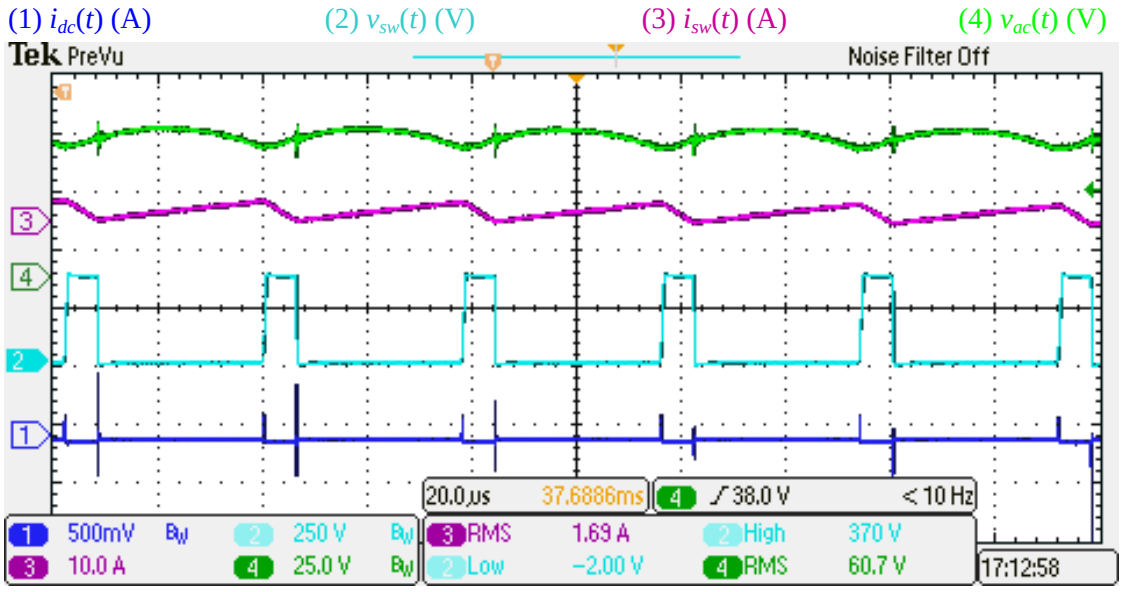


Figure 4.26: Hardware test of VSI under SPWM control with both ac- and dc-side regulation, zoomed in to time scale of switching period (20 μs per division) near maximum value of v_{ac}

second-order ripple caused by filtering the i_{sw} ripple.

Fig. 4.27 shows the point where the H-bridge legs alternate from $Q_3 - Q_4$ to $Q_1 - Q_2$: v_{sw} switches between 0 and -V_{dc} to begin, then alternates to switching between 0 and V_{dc}. The rise in v_{ac} toward the right is the ringing that v_{ac} exhibits at the zero-crossing of v_{ac}. The dc-side capacitor current i_{dc} also exhibits ringing, but it is not seen in the i_{sw} or v_{ac}.

It is beyond the scope of this thesis to validate the ac- and dc-side closed loop gains in hardware. Such an experimental measurement presents a number of challenges that have not been addressed; moreover, one advancement presented here is that loop gain analysis is far less relevant for an active DSSC with constant duty cycle control. However, techniques exist to measure the loop gain of a digitally controlled system. A simple method is to convert an analog signal, generated outside of the digital controller, to a duty cycle perturbation in the controller code. A more comprehensive method is presented in [51, 52]: by adding a white noise signal to the converter duty cycle, the control-to-output impulse response can be identified. This may be implemented by generating a pseudo-random binary signal in the controller code and measuring the properly

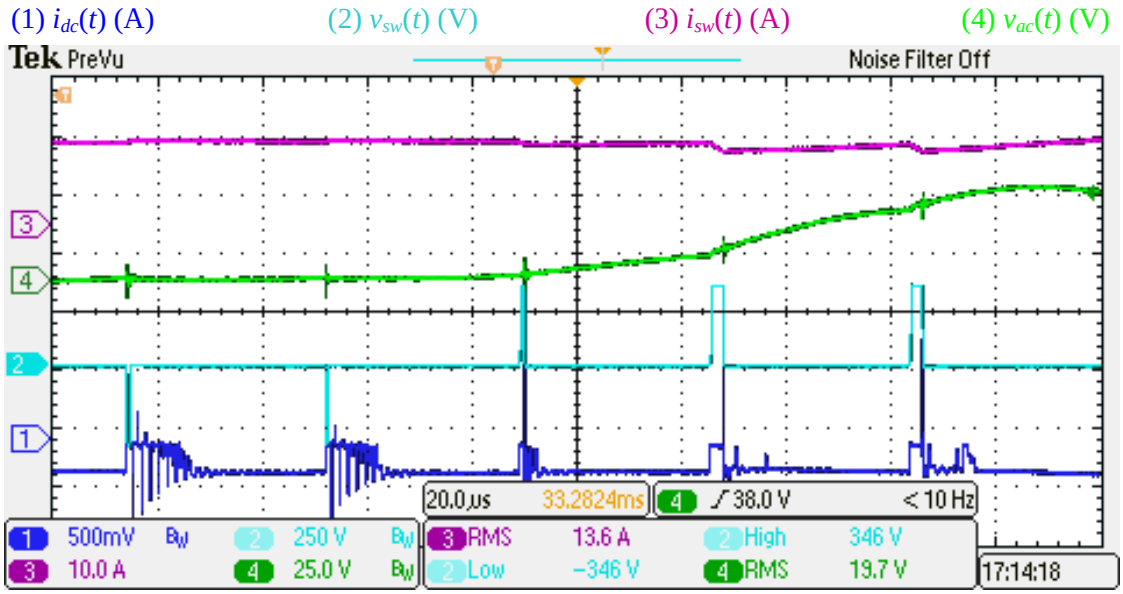


Figure 4.27: Hardware test of VSI under SPWM control with both ac- and dc-side regulation, zoomed in to time scale of switching period (20 μs per division) near zero-crossing of v_{ac}

filtered output voltage.

The operation of the VSI as an ac system presents an additional difficulty for experimental loop gain measurements, in that there is no true steady state operation in the sense of a dc-dc converter. Because $f_\ell \ll f_{sw}$, a quasi-static approximation may be used to analyze the VSI steady-state behavior. Using this approximation, it was found in Section 4.2.2 that that ac-side control-to-output transfer function does not depend on the operating point along the length of the line cycle. However, non-idealities and loss mechanisms not modeled in Section 4.2.2 cause the loop gain to vary. Consequently, loop gain measurements require that perturbations to d and v_{ac} be considered signals in superposition with the predominant component at f_ℓ. Further analysis is necessary to isolate the effects of the loop gain measurement from the f_ℓ component.

Fig. 4.28 shows the results of a test of constant duty cycle control. In order to compare constant duty cycle control directly with SPWM control, the VSI uses the same C_{dc}. As a result of the additional energy provided by the capacitor, V_{ac} and, consequently, X_{inj} are much higher. Equation (3.15) predicts that V_{ac} should be increased by a factor of $1.05^2/(4 \times 0.05) = 5.5$). Table

4.4 indicates that this is the case, as V_{ac} is about 42 V_{rms} vs. 236 V_{rms} under SPWM vs. constant duty cycle control, respectively, an increase of 5.6 times. In order to achieve this operating point, the VSI uses $D = 0.943$.

Fig. 4.28 also shows the much improved waveform shapes provided by constant duty cycle control. The only control used here is zero-crossing detection of v_{ac} necessary to apply three-level switching. As described in Section 4.2.5, the shape of the waveforms is almost entirely determined by the driving current.

Figs. 4.29 and 4.30 show the behavior of the device on the time scale of f_{sw} near $v_{ac} = 0$ and $v_{ac} = V_{ac,max}$, respectively. In this test, the duty cycle is lowered to $D = 0.7$ in order to show the switching waveforms clearly, while I_{ac} is raised to 13.6 A_{rms} to maintain the same level of V_{ac}. In both cases it is clear, once again, that the VSI operates similarly to a dc-dc buck converter. In Fig. 4.29, both v_{dc} and v_{ac} are very low, so there is minimal ripple on i_{sw}. The average value of i_{sw} is at its peak at this point, however, because of the reactive power application.

Table 4.4 summarizes the side-by-side performance of the VSI under the two control schemes.

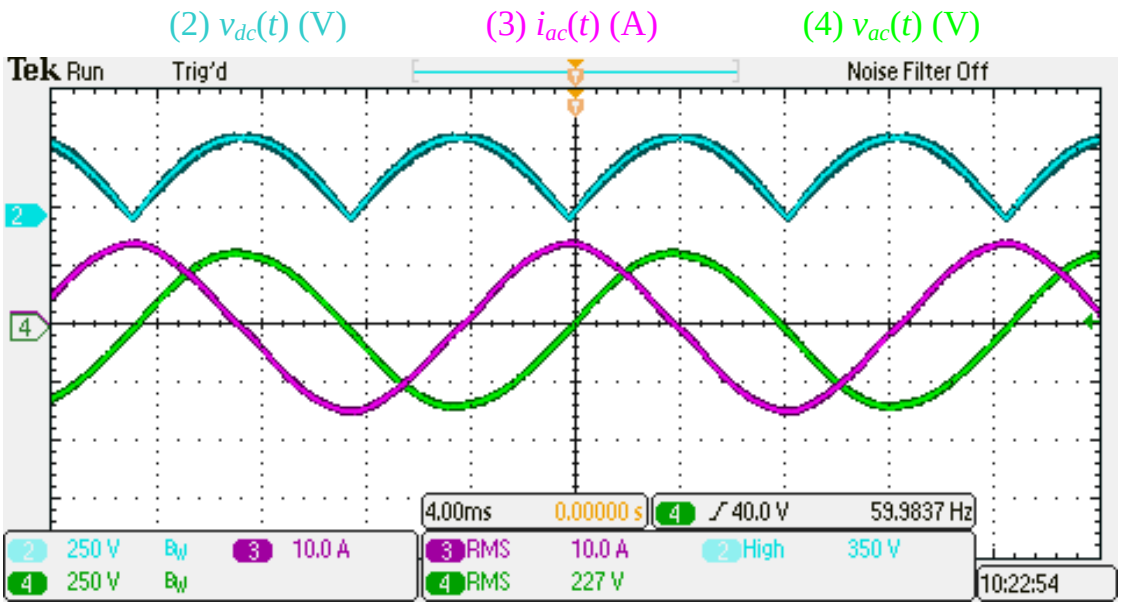


Figure 4.28: Hardware test of VSI under constant duty cycle control control

The table also provides the processed reactive power Q_{req} in each case, as well as the total power loss (measured by averaging the instantaneous power over several cycles) and effective efficiency

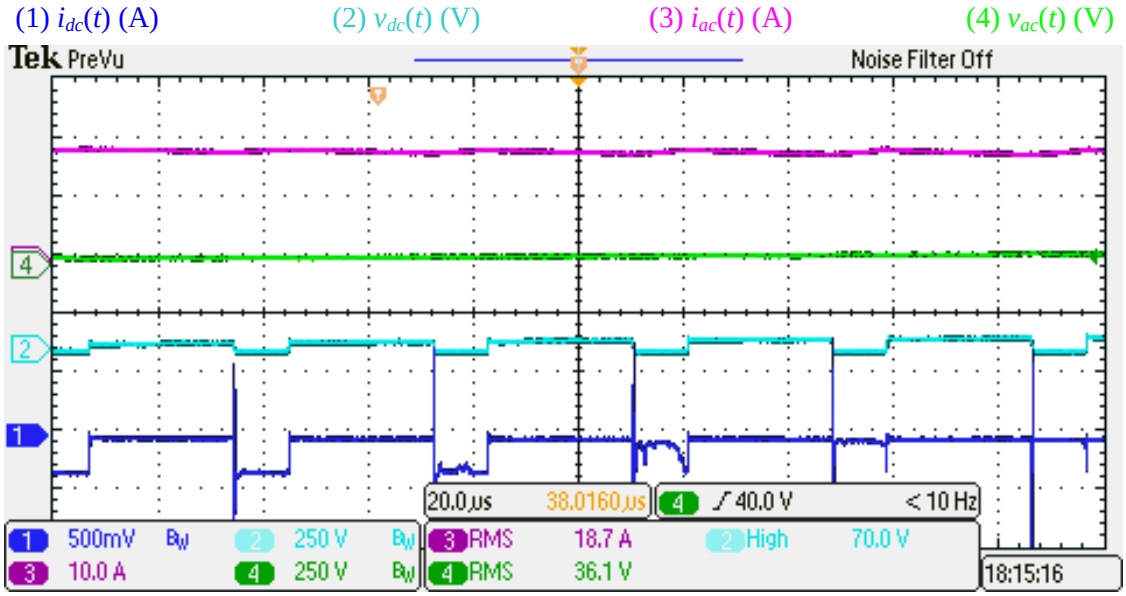


Figure 4.29: Hardware test of VSI under constant duty cycle control control, zoomed in to time scale of switching period (20 μs per division) near zero-crossing of v_{ac}

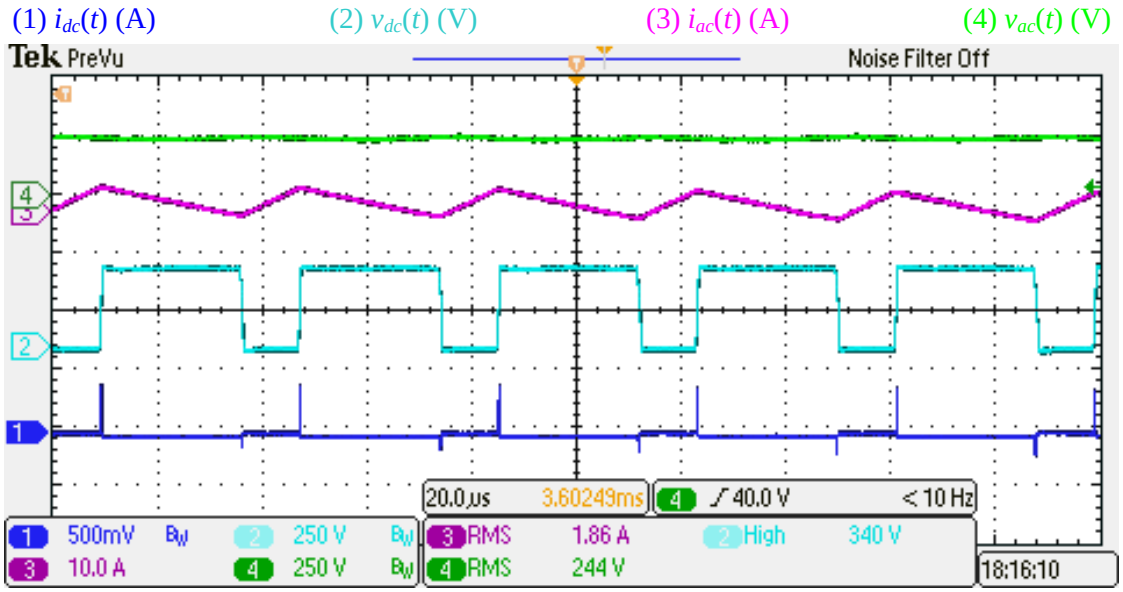


Figure 4.30: Hardware test of VSI under constant duty cycle control control, zoomed in to time scale of switching period (20 μs per division) near maximum value of v_{ac}

(as defined in Chapter 3: $\eta = 1 - P_{loss}/Q_{req}$). As predicted in Chapter 3, the VSI is much more efficient under constant duty cycle control. Table 4.5 gives the loss components predicted by the model for each test. While the model loses some accuracy at high values of duty cycle, it still validates the expectation that constant duty cycle switching reduces IGBT switching loss. Though not presented in the table, the model is further validated using the results of the test in Figs. 4.29 and 4.30: the measured loss is 73 W and the predicted loss is 79 W.

Table 4.4: Experimental results comparing SPWM and constant duty cycle control operation ($C_{dc} = 100\ \mu$F)

	SPWM Control	Constant duty cycle control
I_{ac} (A_{rms})	10	
V_{ac} (V_{rms})	41.6	236
E_{dc} (J)	1.11	6.26
Q_{req} (VAr)	416	2,360
Max V_{dc} (V)	346	350
Min V_{dc} (V)	316	0
P_{loss} (W)	88.6	42.5
Efficiency (%)	78.7	98.2

Table 4.5: Predicted power loss components from inverter loss model

	SPWM Control	Constant duty cycle control	
I_{ac} A_{rms}	10	10	13.6
L_i loss (W)	3.43	3.0	5.42
Conduction loss (W)	30.3	23.9	38.6
Switching loss (W)	56.9	28.3	35.6
Total loss (W)	90.7	55.2	79.4

Chapter 5

Conclusions

5.1 Summary of Contributions

This thesis has presented two primary contributions to the field of transmission system reactive power compensation; specifically, the design, operation, performance, and deployment of distributed static series compensators (DSSCs).

First, a transmission-system-level view of DSSCs is taken in Chapter 2. DSSCs are intended for deployment throughout a system, but the impact of such deployment has not yet been thoroughly and systematically analyzed. One major contribution of this work has been to develop a linearized transmission system model for use in studying DSSCs [53]. The model is based on the fact that DSSCs may be used to incrementally change transmission line reactance. This allows the transmission system to be linearized around the reactance injected onto a given line by DSSCs. The impact of DSSC deployment on the four quantities that describe system operation – real power flow, reactive power flow, bus voltage magnitude, and bus voltage angle; also transmission line current – may be calculated. This allows system operators and planners to understand more deeply where in a system DSSCs are best used, and in what amount.

A further contribution is the development of the concept of "line efficacy" [53]. The closed form of the linearized model may be reduced to a single value that broadly represents the impact DSSCs on a particular line have on all the system operating parameters. In other words, for a typical compensation application, a line with high efficacy is better suited for DSSC deployment than a line with low efficacy. Moreover, efficacy may be accurately determined using only measurements local

to the line in question. In contrast, the complete linearized model requires complete knowledge of the system topology and operating state – that is, a load flow solution.

Chapter 2 also presents several examples of systems for which both the linearized model and line efficacy are used to decide how best to deploy DSSCs for some compensation goal. Section 2.2.3 presents DSSC "deployment diagrams," a graphical representation of the system of coefficients produced by the linearized model. The deployment diagrams illustrate the signs and relative magnitudes of the coefficients that relate each line's DSSCs to a particular system parameter. The examples also discuss the merits of line efficacy, including the conditions under which efficacy is not accurate.

Chapters 3 and 4 focus on the DSSC unit itself. The second major contribution of this thesis is an active DSSC design that improves upon existing designs by use of constant duty cycle control of the DSSC voltage source inverter (VSI) [54]. Chapter 3 presents the theory of the improvement. By connecting a VSI to the secondary side of a single turn transformer (STT), the DSSC may achieve injected reactance greater than with the STT alone. The DSSC may also inject capacitive reactance, which is impossible with the STT alone.

Constant duty cycle control is presented as an alternative to conventional sinusoidal pulse-width modulation. Constant duty cycle control increases the energy available from the VSI dc-side capacitor, improving the performance of the DSSC. Chapter 3 presents a process for designing a DSSC, including the STT and VSI dc-side capacitor selection. Chapter 3 also presents a loss model for a single-phase inverter, which is used to show that constant duty cycle control improves the efficiency of the DSSC.

Finally, Chapter 4 presents the details of a VSI design. The hardware is a typical IGBT-based H-bridge, 5 kVA, four-quadrant inverter initially developed for general purpose inverter applications. With few modifications, the inverter is configured to act as a DSSC VSI (without the STT). The VSI is tested using both SPWM and constant duty cycle control. The design of the voltage regulation loops necessary for SPWM control is presented in detail. Lastly, the hardware operation is measured to validate the designs and simulations of both control schemes and to show

a side-by-side comparison of SPWM control and constant duty cycle control. Using constant duty cycle control, the VSI is proven to provide greater injected reactance at lower power loss.

The overall contribution of this thesis is to advance the use of DSSCs. DSSCs are a promising alternative to existing compensation solutions; they may improve the operation of transmission systems at lower cost and higher reliability relative to existing FACTS solutions. This thesis addresses two open areas of research related to DSSCs: the impact of DSSCs on a transmission system, and design improvements for active DSSCs.

5.2 Future Work

There are a number of areas of potential future research related to the topics presented in this thesis. First, recognize that the linearized transmission system model is a tool for studying DSSC deployment, not a solution to any one deployment problem. As such, optimization methods based on the model and/or efficacy may be developed to find exact solutions for DSSC deployment based on system constraints. Advanced deployment solutions may be customized for specific systems to account for real-time changes in operating points and topology (e.g. the network is reconfigured when a generator unit goes offline).

A related area of study is the coordination of and communication with individual DSSC units. There may be dozens or hundreds of units in a system. It may be advantageous for them to operate autonomously, in which case the dynamics of their interactions must be studied. On the other hand, they may be controlled in groups by a system operator, requiring a new analysis of how the units are networked. It may also be necessary to account for communication latency and to study the resulting system dynamics.

There is much room for further study of the design of individual DSSC units. This thesis, along with [25], presents a strong foundation for the design of an STT best suited for use with a VSI, but considerable research may be done to perfect the STT design. Whereas this thesis began with a STT core design from [25], it may be possible to optimize the design of the entire unit from the ground up.

Finally, in a practical design, it is necessary to charge the STT magnetizing inductance and VSI input capacitance in order to avoid large, potentially damaging startup transients. This topic is introduced in [19, 22, 23, 25], and may need further study for the constant duty cycle design presented in this thesis.

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Appendix A

Derivation of Transmission System Linear Coefficients

This chapter will give more detail on the calculation of the coefficients described in Section 2.1. As explained, the power balance equations (2.2) are perturbed and linearized for each bus, resulting in (2.3). Equation (2.3) includes several coefficients, which are formed with the original system values ($V,\ G,\ \delta$, etc.). Equation (2.3) is given again here:

$$0 = -\hat{p}_i + u_i^{pg}\hat{g}_{mn} + u_i^{pb}\hat{b}_{mn} + \sum_{k=1}^{N} A_{ik}^{pv}\hat{v}_k + A_{ik}^{p\delta}\hat{\delta}_k$$

$$0 = -\hat{q}_i + u_i^{qg}\hat{g}_{mn} + u_i^{qb}\hat{b}_{mn} + \sum_{k=1}^{N} A_{ik}^{qv}\hat{v}_k + A_{ik}^{q\delta}\hat{\delta}_k\ ,$$

Performing the perturbation and linearization process results in the following relationships for the coefficients in (2.3):

$$A_{ij}^{pv} = \begin{cases} V_i G_{ii} + \\ \sum\limits_{k=1}^{N} V_k \left(G_{ik}\cos\theta_{ik} + B_{ik}\sin\theta_{ik}\right),\ \text{for } i = j \\ V_i \left(G_{ij}\cos\theta_{ij} + B_{ij}\sin\theta_{ij}\right),\ \text{for } i \neq j \end{cases} \tag{A.1a}$$

$$A_{ij}^{qv} = \begin{cases} -V_i B_{ii} + \\ \sum\limits_{k=1}^{N} V_k \left(G_{ik}\sin\theta_{ik} - B_{ik}\cos\theta_{ik}\right),\ \text{for } i = j \\ V_i \left(G_{ij}\sin\theta_{ij} - B_{ij}\cos\theta_{ij}\right),\ \text{for } i \neq j \end{cases} \tag{A.1b}$$

$$A_{ij}^{p\delta} = \begin{cases} -{V_i}^2 B_{ii} + \\ V_i \sum_{k=1}^{N} V_k \left(B_{ik} \cos\theta_{ik} - G_{ik} \sin\theta_{ik} \right), \text{ for } i = j \\ -V_i V_j \left(B_{ij} \cos\theta_{ij} - G_{ij} \sin\theta_{ij} \right), \text{ for } i \neq j \end{cases} \tag{A.1c}$$

$$A_{ij}^{q\delta} = \begin{cases} -{V_i}^2 G_{ii} + \\ V_i \sum_{k=1}^{N} V_k \left(G_{ik} \cos\theta_{ik} + B_{ik} \sin\theta_{ik} \right), \text{ for } i = j \\ -V_i V_j \left(G_{ij} \cos\theta_{ij} + B_{ij} \sin\theta_{ij} \right), \text{ for } i \neq j \end{cases} \tag{A.1d}$$

$$u_{i,mn}^{pg} = \begin{cases} {V_m}^2 - V_m V_n \cos\theta_{mn}, \text{ for } i = m \\ {V_n}^2 - V_m V_n \cos\theta_{mn}, \text{ for } i = n \\ 0, \text{ otherwise} \end{cases} \tag{A.2a}$$

$$u_{i,mn}^{qg} = \begin{cases} -V_m V_n \sin\theta_{mn}, \text{ for } i = m \\ V_m V_n \sin\theta_{mn}, \text{ for } i = n \\ 0, \text{ otherwise} \end{cases} \tag{A.2b}$$

$$u_{i,mn}^{pb} = u_{i,mn}^{qg} \tag{A.2c}$$

$$u_{i,mn}^{qb} = -u_{i,mn}^{pg} \ , \tag{A.2d}$$

where $\theta_{ij} = \delta_i - \delta_j$ and Line m-n is the only perturbed line. For clarification, the term A_{ij}^{pv}, for example, refers to the perturbation in P_i caused by the perturbation to V_j, as from (2.3), while the term $u_{i,mn}^{qg}$ refers to the perturbation in Q_i caused by the perturbation to g_{mn}. Also recall from the footnote in Section 2.1.1 that G and B are terms from the admittance matrix, while g and b, which are not used here, refer to the actual admittance values.

Note that all of the A coefficients are independent of m and n. The $\mathbf{A}$ matrix from Section 2.1.2 need only be calculated once for a given system. This allows for more efficient calculation of the effect on the system of perturbations in multiple line impedances. Only the calculation of the u coefficients must be repeated if more than one line impedance is considered.

Finally, the coefficients for line current perturbations, as in Section 2.1.4, must be found. Equation (2.14) gives the current on any line i-j. It is the square of (2.14) −

$$\begin{aligned} {I_{ij}}^2 = &\left({g_{ij}}^2 + {b_{ij}}^2\right) \times \\ &\left(\left(V_i \cos\delta_i - V_j \cos\delta_j\right)^2 + \left(V_i \sin\delta_i - V_j \sin\delta_j\right)^2\right) \end{aligned} \tag{A.3}$$

− that is perturbed and linearized. The left side of the resulting equation, where $I_{ij} \to I_{ij} + \hat{\imath}_{ij}$, is

$${I_{ij}}^2 + 2I_{ij}\hat{\imath}_{ij} + {\hat{\imath}_{ij}}^2 .$$

Following the standard perturb-and-linearize procedure, ${I_{ij}}^2$ is subtracted away and ${\hat{\imath}_{ij}}^2 \approx 0$. The linearized result of the right side of (A.3) must then be divided by $2I_{ij}$ to find $\hat{\imath}_{ij}$. The resulting expression is:

$$\hat{\imath}_{ij} = A^{iv}_{ij}\hat{v}_i + A^{iv}_{ji}\hat{v}_j + A^{i\delta}_{ij}\hat{\delta}_i + A^{i\delta}_{ji}\hat{\delta}_j + u^{ig}_{ij}\hat{g}_{ij} + u^{ib}_{ij}\hat{b}_{ij}.$$

This process is only used to find the perturbation in current on one line due to the reactance perturbation on one line (not necessarily the same line). The coefficients consist of original operating point values:

$$A^{iv}_{ij} = \frac{1}{I_{ij}}\left({G_{ij}}^2 + {B_{ij}}^2\right)\left(V_i - V_j \cos\theta_{ij}\right) \tag{A.4a}$$

$$A^{iv}_{ji} = \frac{1}{I_{ij}}\left({G_{ij}}^2 + {B_{ij}}^2\right)\left(V_j - V_i \cos\theta_{ij}\right) \tag{A.4b}$$

$$A^{i\delta}_{ij} = \frac{1}{I_{ij}}\left({G_{ij}}^2 + {B_{ij}}^2\right) V_i V_j \sin\theta_{ij} \tag{A.4c}$$

$$A^{i\delta}_{ji} = -\frac{1}{I_{ij}}\left({G_{ij}}^2 + {B_{ij}}^2\right) V_i V_j \sin\theta_{ij} \tag{A.4d}$$

$$u^{ig}_{ij} = -\frac{G_{ij}}{I_{ij}}\left({V_i}^2 + {V_j}^2 - 2V_i V_j \cos\theta_{ij}\right) \tag{A.5a}$$

$$u^{ib}_{ij} = -\frac{B_{ij}}{I_{ij}}\left({V_i}^2 + {V_j}^2 - 2V_i V_j \cos\theta_{ij}\right) \tag{A.5b}$$

In (A.4), ${g_{ij}}^2$ and ${b_{ij}}^2$ have been substituted directly with ${G_{ij}}^2$ and ${B_{ij}}^2$, respectively, for the reasons discussed above. In (A.5), $g_{ij} = -G_{ij}$ and $b_{ij} = -B_{ij}$ since $i \neq j$ always in line current calculations.

The last step is to find the coefficient for $\hat{x}$ instead of $\hat{g}$ and $\hat{b}$. Similar to (2.12),

$$u_{ij}^{ix} = 2G_{ij}B_{ij}u_{ij}^{ig} + \left(B_{ij}{}^2 - G_{ij}{}^2\right) u_{ij}^{ib}\,. \tag{A.6}$$

Reducing this gives:

$$u_{ij}^{ix} = -\frac{B_{ij}}{I_{ij}} \left(G_{ij}{}^2 + B_{ij}{}^2\right) \left(V_i{}^2 + V_j{}^2 - 2V_iV_j\cos\theta_{ij}\right), \tag{A.7}$$

which is used in the final expression, (2.15).

Appendix B

Complete Piecewise Transistor Current Equations

The following equations represent the current through the transistor channel and body diode of one each of the top- and bottom-side H-bridge IGBTs. The equations relate to the currents over one full ac line cycle.

$$i_{Q1rms,sw}(t) = \begin{cases} i_{Q1rms,cont}(t)\,, & \text{for } v_{ac}(t) > 0 \text{ and } i_{ac}(t) > 0 \text{ and } \Delta i_L(t) < i_{ac}(t) \\ i_{Qrms,disc}(t)\,, & \text{for } v_{ac}(t) > 0 \text{ and } \Delta i_L(t) > i_{ac}(t) \\ 0\,, & \text{for } v_{ac}(t) < 0, \text{ or } i_{ac}(t) < 0 \text{ and } \Delta i_L(t) < i_{ac}(t) \end{cases} \tag{B.1}$$

and

$$i_{Q1avg,sw}(t) = \begin{cases} i_{Q1avg,cont}(t)\,, & \text{for } v_{ac}(t) > 0 \text{ and } i_{ac}(t) > 0 \text{ and } \Delta i_L(t) < i_{ac}(t) \\ i_{Qavg,disc}(t)\,, & \text{for } v_{ac}(t) > 0 \text{ and } \Delta i_L(t) > i_{ac}(t) \\ 0\,, & \text{for } v_{ac}(t) < 0, \text{ or } i_{ac}(t) < 0 \text{ and } \Delta i_L(t) < i_{ac}(t). \end{cases} \tag{B.2}$$

For the body diode of Q_1, the piecewise RMS and average currents are

$$i_{D1rms,sw}(t) = \begin{cases} i_{D1rms,cont}(t)\,, & \text{for } v_{ac}(t) > 0 \text{ and } i_{ac}(t) < 0 \text{ and } \Delta i_L(t) < i_{ac}(t) \\ i_{Drms,disc}(t)\,, & \text{for } v_{ac}(t) > 0 \text{ and } \Delta i_L(t) > i_{ac}(t) \\ 0\,, & \text{for } v_{ac}(t) < 0, \text{ or } i_{ac}(t) > 0 \text{ and } \Delta i_L(t) < i_{ac}(t) \end{cases} \tag{B.3}$$

and

$$i_{D1avg,sw}(t) = \begin{cases} i_{D1avg,cont}(t)\,, & \text{for } v_{ac}(t) > 0 \text{ and } i_{ac}(t) < 0 \text{ and } \Delta i_L(t) < i_{ac}(t) \\ i_{Davg,disc}(t)\,, & \text{for } v_{ac}(t) > 0 \text{ and } \Delta i_L(t) > i_{ac}(t) \\ 0\,, & \text{for } v_{ac}(t) < 0, \text{ or } i_{ac}(t) > 0 \text{ and } \Delta i_L(t) < i_{ac}(t) \end{cases} \tag{B.4}$$

The piecewise equations for all the current functions of Q_2 are

$$i_{Q2rms,sw}(t) = \begin{cases} i_{Q2rms,cont}(t)\,, & \text{for } v_{ac}(t) > 0 \text{ and } i_{ac}(t) < 0 \text{ and } \Delta i_L(t) < i_{ac}(t) \\ i_{Lrms,sw}(t)\,, & \text{for } v_{ac}(t) < 0 \text{ and } i_{ac}(t) < 0 \text{ and } \Delta i_L(t) < i_{ac}(t) \\ i_{Qrms,disc}(t)\,, & \text{for } v_{ac}(t) > 0 \text{ and } \Delta i_L(t) > i_{ac}(t) \\ i_{Q2rms,disc}(t)\,, & \text{for } v_{ac}(t) < 0 \text{ and } \Delta i_L(t) > i_{ac}(t) \\ 0\,, & \text{for } i_{ac}(t) < 0 \text{ and } \Delta i_L(t) < i_{ac}(t), \end{cases} \tag{B.5}$$

$$i_{Q2avg,sw}(t) = \begin{cases} i_{Q2avg,cont}(t)\,, & \text{for } v_{ac}(t) > 0 \text{ and } i_{ac}(t) < 0 \text{ and } \Delta i_L(t) < i_{ac}(t) \\ i_{Lavg,sw}(t)\,, & \text{for } v_{ac}(t) < 0 \text{ and } i_{ac}(t) < 0 \text{ and } \Delta i_L(t) < i_{ac}(t) \\ i_{Qavg,disc}(t)\,, & \text{for } v_{ac}(t) > 0 \text{ and } \Delta i_L(t) > i_{ac}(t) \\ i_{Q2avg,disc}(t)\,, & \text{for } v_{ac}(t) < 0 \text{ and } \Delta i_L(t) > i_{ac}(t) \\ 0\,, & \text{for } i_{ac}(t) < 0 \text{ and } \Delta i_L(t) < i_{ac}(t), \end{cases} \tag{B.6}$$

$$i_{D2rms,sw}(t) = \begin{cases} i_{D2rms,cont}(t)\,, & \text{for } v_{ac}(t) > 0 \text{ and } i_{ac}(t) > 0 \text{ and } \Delta i_L(t) < i_{ac}(t) \\ i_{Lrms,sw}(t)\,, & \text{for } v_{ac}(t) < 0 \text{ and } i_{ac}(t) > 0 \text{ and } \Delta i_L(t) < i_{ac}(t) \\ i_{Drms,disc}(t)\,, & \text{for } v_{ac}(t) > 0 \text{ and } \Delta i_L(t) > i_{ac}(t) \\ i_{D2rms,disc}(t)\,, & \text{for } v_{ac}(t) < 0 \text{ and } \Delta i_L(t) > i_{ac}(t) \\ 0\,, & \text{for } i_{ac}(t) > 0 \text{ and } \Delta i_L(t) < i_{ac}(t), \end{cases} \tag{B.7}$$

and

$$i_{D2avg,sw}(t) = \begin{cases} i_{D2avg,cont}(t)\,, & \text{for } v_{ac}(t) > 0 \text{ and } i_{ac}(t) > 0 \text{ and } \Delta i_L(t) < i_{ac}(t) \\ i_{Lavg,sw}(t)\,, & \text{for } v_{ac}(t) < 0 \text{ and } i_{ac}(t) > 0 \text{ and } \Delta i_L(t) < i_{ac}(t) \\ i_{Davg,disc}(t)\,, & \text{for } v_{ac}(t) > 0 \text{ and } \Delta i_L(t) > i_{ac}(t) \\ i_{D2avg,disc}(t)\,, & \text{for } v_{ac}(t) < 0 \text{ and } \Delta i_L(t) > i_{ac}(t) \\ 0\,, & \text{for } i_{ac}(t) > 0 \text{ and } \Delta i_L(t) < i_{ac}(t). \end{cases} \tag{B.8}$$

Appendix C

Component Parameters for Inverter Loss Model

The following discussion of inverter losses is based on the 5kW, four-quadrant design given here.

- **Switching frequency** $f_s = 27.474\text{kHz}$
- **Grid frequency** $\omega_g = 60 \times 2\pi$ rad/s
- **Inductance** $L = 590\mu\text{H}$
- **Inductor windings** $n = 34$
- **Inductor series resistance** $R_{cu} = 15\text{m}\Omega$
- **Inductor core cross-sectional area** $A_c = 7.06\text{cm}^2$
- **Inductor gap length** $l_g = 0.35\text{cm}$
- **Inductor core loss exponent** $\beta = 2.7$
- **Inductor geometrical constant** $K_{fe} = 7.9\text{cm}^{2.6}$
- **IGBT MOSFET on-state resistance** $R_{on,q} = 4.57\text{m}\Omega$
- **IGBT MOSFET forward voltage drop** $V_{f,q} = 1.03\text{V}$
- **IGBT Body diode on-state resistance** $R_{on,d} = 92.3\text{m}\Omega$
- **IGBT Body diode forward voltage drop** $V_{f,d} = 3.18\text{V}$
- **Diode reverse recovery charge constant** $K_{qrr} = 6.2 \cdot 10^{-8}\text{C}/\sqrt{\text{W}}$
- **Diode reverse recovery time constant** $K_{trr} = 2.53 \cdot 10^{-8}\text{s}/\sqrt[4]{A}$
- **IGBT tailing charge constant** $K_{qtail} = 2.7 \cdot 10^{-7}\text{s}$