GRAPHENE GEOMETRIC DIODES FOR OPTICAL RECTENNAS

by

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Graphene Geometric Diodes For Optical Rectennas

Thesis directed by Prof. Garret Moddel

Optical rectennas, which are micro-antennas to convert optical-frequency radiation to alternating current combined with ultrahigh-speed diodes to rectify the current, can in principle provide high conversion efficiency solar cells and sensitive detectors. Currently investigated optical rectennas using metal/insulator/metal (MIM) diodes are limited in their RC response time and poor impedance matching between diodes and antennas. A new rectifier, the geometric diode, can overcome these limitations. The thesis work has been to develop geometric diode rectennas, along with improving fabrication processes for MIM diode rectennas. The geometric diode consists of a conducting thin-film, currently graphene, patterned into a geometry that leads to diode behavior. In contrast with MIM diodes that have parallel plate electrodes, the planar structure of the geometric diode provides a low RC time constant, on the order of 10^{-15} s, which permits operation at optical frequencies. Fabricated geometric diodes exhibit asymmetric DC current-voltage characteristics that match well with Monte Carlo simulations based on the Drude model. The measured diode responsivity at DC and zero drain-source bias is 0.012 A/W. Since changing the gate voltage changes the graphene charge carrier concentration and can switch the majority charge type, the rectification polarity of the diode can be reversed. Furthermore, the optical rectification at 28 THz has been measured from rectennas formed by coupling geometric diodes with graphene and metal bowtie antennas. The performance of the rectenna IR detector is among the best reported uncooled IR detectors. The noise equivalent power (NEP) of the rectenna detector using geometric diode was measured to be 2.3 nW $Hz^{-1/2}$. Further improvement in the diode and

antenna design is expected to increase the detector performance by at least a factor of two. Applications for geometric diodes and graphene bowtie antennas include detection of terahertz and optical waves, ultra-high speed electronics, and optical power conversion.

Dedicated to my parents

Jie Sun and Ning Zhu

&

my wife

Meng Lin

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CHAPTER I

INTRODUCTION TO RECTENNAS

A. Rectennas

An antenna-coupled diode for optical frequency operation, also called optical rectenna, incorporates a submicron antenna and an ultra-high-speed diode. The optical rectenna absorbs electromagnetic radiation and converts it to current. A diode rectifies the AC current, providing DC electrical power. Compared with conventional solar cells, which absorb photons and generate electron-hole pairs to provide electrical power, rectennas seem to rely on Maxwell's electromagnetic wave view of light.

Although the concept of using optical rectennas for harvesting solar energy was first introduced by Bailey in 1972 (Bailey 1972), owing to lack of efficient optical antennas and ultrafast diodes, optical rectenna research had not been drawing much interest from the solar cell field until recently (Eliasson and Moddel 2003), (Hagerty 2004), (Singh 2006), (Mashaal and Gordon 2011), (Joshi and Moddel 2013). The result is a technology that can be efficient and inexpensive, requiring only low-cost materials. Similar cost and efficiency requirements are imposed on infrared detector technologies for applications such as automotive night vision.

A rectenna circuit consists of an antenna connected to a diode, as shown in Figure I-1. The ultrafast diode rectifies the optical frequency signal absorbed by the antenna into DC voltage. The most straightforward way to use the rectified DC energy is to connect a load through a low-pass DC filter to the diode. Performing a classical circuit

analysis, we find that the output DC voltage at the load can be as high as the peak input AC voltage across the antenna (Grover 2011).

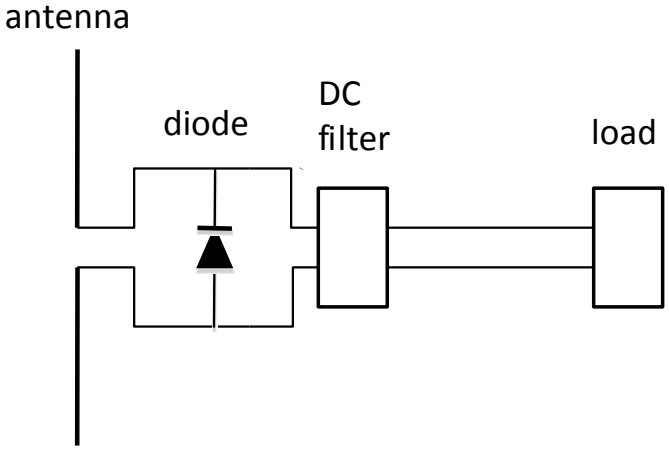


Figure I-1. Rectenna circuit.

B. Ultrafast diodes

Investigation of various parts of the optical rectenna technology is required, especially on finding suitable diodes working at terahertz or even optical frequencies. My thesis focuses on the ultrafast diodes used in optical rectennas. Choosing a suitable diode depends on its operating frequency, which will be above the terahertz and infrared (IR) 28 THz frequency.

The operation frequency of conventional semiconductor diodes is in the order of gigahertz because these diodes with p-n junctions are limited by the transit time of charges(Sedra and Smith 2010). Schottky diodes are able to operate at terahertz and up to far-infrared frequencies(Brown 2003), (Kazemi 2007).

In this thesis, two types of ultrafast diodes are discussed: metal-insulator-metal (MIM) diodes and geometric diodes. MIM diodes are capable of operating at terahertz frequencies, while geometric diodes can operate up to optical frequencies.

1. Metal-insulator-metal diodes

Our group started investigating MIM diodes for use in optical rectenna applications (Eliasson 2001), (Eliasson and Moddel 2003) in 1998, supported by ITN Energy Systems (NR 2012). Extensive research work was conducted by my colleagues, Blake Eliasson, Sachit Grover, and Saumil Joshi.

A typical band diagram of a MIM diode is shown in Figure I-2. In MIM diodes, the charge carriers tunnel through an oxide, which is some nanometers thick, from one metal layer to the other. Although the tunneling time of the carriers is on the order of femtoseconds, the factors described below limit the diode response time and overall rectenna efficiency.

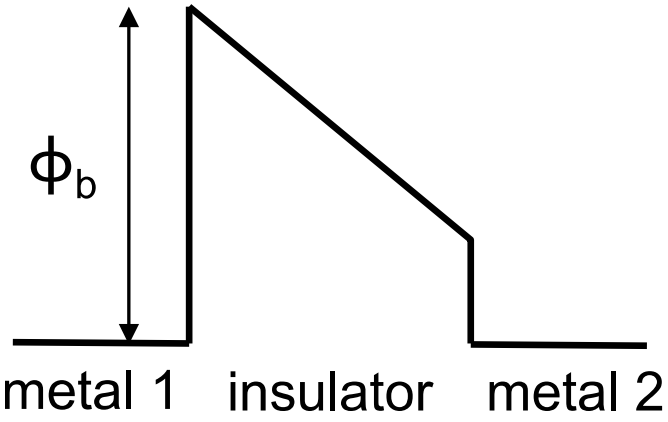


Figure I-2. Typical band diagram of metal-insulator-metal diode under zero bias. Fermi levels of the two metal layers and conduction band edge of the insulator are shown as functions of position. In this diode, the barrier height of metal 1 is ϕ_b.

For efficient power transfer, the impedance of the diode must match the antenna impedance from the circuit analysis. In the quantum mechanical model of the rectenna system, the secant resistance derived from the diode *I(V)* characteristics has to match the antenna impedance (Grover 2013). The impedance of the antenna varies from a few tens to hundreds of ohms at terahertz frequencies (Kocakarin and Yegin 2013) and can be up to a thousand ohms at visible light frequencies (de Arquer 2011). Thus, the diode resistance is limited to be within the same range for high coupling

efficiency. Details of the coupling efficiency analysis is discussed in chapter 9 and Sachit Grover's thesis (Grover and Moddel 2011), (Grover 2011).

A MIM diode with an antenna matched resistance of ~100 Ω is a low resistance diode that requires a low barrier height (typically no more than ~0.2 eV), and thin insulators (typically thinner than 3 nm) (Joshi 2013), (Zhu 2013). An easy method to reduce the MIM diode resistance is to increase the diode area, but because of the capacitance requirement described below this approach is not practical.

Diode capacitance is a crucial efficiency-limiting factor, because the rectenna circuit RC time constant must be smaller than the time constant corresponding to the visible light frequency. For operating at visible frequencies, the diode capacitance C must be less than a few attofarads for a diode resistance R of 100 Ω.

For MIM diodes, a diode with an extremely small area of ~10 nm × 10 nm is able to provide a sufficiently low diode capacitance on the order of attofarads. Assuming that such a small area is achievable, the diode resistance would be unacceptably high (~10 kΩ), and would reduce the coupling efficiency to below a few percent (Sanchez 1978), (Grover and Moddel 2011).

Thus, to use MIM diodes for efficient energy transfer or even signal detection, the operational frequencies of the rectennas are lowered to ~1 THz. My work on rectennas using MIM diodes operating at 1 THz is discussed in chapter 7.

2. Geometric diodes

Because MIM diodes are limited in frequency response by the fundamental RC constraints in the parallel-plate devices, we propose and demonstrate a new type of diode called a geometric diode that is not restricted by the RC constraints of parallel-plate devices for its planar structure. At the same time, since geometric diodes are formed from a conductive material, the resistance of the diodes is also sufficiently low to match the antenna impedance.

Imagine a conductive thin film patterned into an inverse arrowhead shape shown in Figure I-3. Charge carriers move from left to right (forward direction) more easily than in the opposite direction because of the funneling effect of the arrowhead shaped edges. This asymmetric charges transport probability in different directions causes the diode behavior in the *I(V)* characteristics of the geometric diodes. The operation principle of the geometric diodes is introduced and discussed in detail in chapter 2.

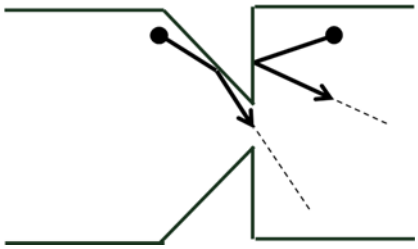


Figure I-3. Schematic plot of an inverse arrowhead shape geometric diode. Charge carriers reflect off the edges of a geometric diode.

The simulated results of the above inverse arrowhead-shaped geometric diodes are shown in chapter 3, followed by several methods to fabricate geometric diodes in chapter 4. Since the geometric diode is formed from a conductive material that supplies the ballistic charge carriers, I have fabricated geometric diodes using thin-film metal and graphene. The DC *I(V)* characteristics and optical measurement results will then be shown and discussed in chapters 6 and 7, followed by an in-depth analysis of device performance and a discussion on methods for future improvement in the remaining chapters.

CHAPTER II

CONCEPTS OF GEOMETRIC DIODE

A. Introduction

We coined the term "geometric diode" for a conductive thin-film device that we proposed (Moddel 2011) and demonstrated at DC (Zhu 2011), (Moddel 2012) and 28 THz (Zhu 2013). It makes use of an asymmetric triangular-shaped conductive thin film. Geometric diodes rely on physical asymmetry to impart the diode-like behavior.

Similar devices using a geometric effect have been demonstrated for 3-terminal T-shape and Y-shape devices in theory (Wesström 1999) and experimentally (Song 1998), (Hieke and Ulfward 2000), (Shorubalko 2001). Song demonstrated a gallium arsenide based semiconductor device, which used hot electrons as charge carriers and could work as a full wave rectifier (FWR) operating at 50 GHz (Song 2002). Later, he developed similar high frequency diodes that depend on taking the advantage of an asymmetric nanochannel formed in a GaAs-based semiconductor structure. Its depletion layer varies with the applied voltage, and the device has been demonstrated to operate at 1.5 THz in rectennas (Balocco 2011). With some modifications or by changing the diode materials, it might prove to be a very good candidate for operation at higher optical frequencies. Most recently, the full wave rectification behavior of a Y-shape device made from graphene was reported (Händel 2014).

In parallel with Song's work, extensive research work was done in the 1990s and 2000s related to rectification in ballistic devices, mainly using III-V semiconductor materials (Lorke 1998), (Sassine 2008). High- and low-frequency magnetotransport of antidot lattice with a chevron shape, was discussed in reference (Lorke 1998). The shape of the antidot lattice was triangles. Reference (Sassine 2008) show the "ratchet" effect caused by the directed transport induced by external energy sources in another

asymmetric system, in which the antidot structure was in a half circular shape. These devices ware claimed to represent a significant step towards the realization of new microwave detectors and current generators.

As for metal devices, optical rectification and field enhancement resulting from the asymmetric metal nanogap have also been observed under high illumination intensity (Ward 2010). By using electron-beam (e-beam) lithography followed by electromigration, the metal nanogaps were formed. The rectification effect was observed after performing statistical analysis on thousands of measurements. Therefore, not only was the fabrication process unreliable, but the geometric effect was also weak.

A graphene diode using geometric asymmetry in the form of an oblique gate over a graphene channel was proposed and simulated (Dragoman 2010), (Dragoman 2013). The electrical doping asymmetry caused by the oblique gate is low, leading to weakly asymmetric *I(V)* characteristics.

B. Operation principle of geometric diodes

In geometric diodes, *I(V)* asymmetry results from an asymmetry in the physical shape of the device. Imagine a conductive thin film patterned into an inverse arrowhead shape, as shown in Figure II-1. The critical region of the device is the inverse arrowhead-shaped construction (the neck region). Charge carriers move from left to right (forward) more easily than in the opposite direction because of the funneling effect caused by the arrowhead-shaped edges. The forward moving charge carriers have a higher probability of reflecting off the diagonal walls on the left side of the neck and channeling through the arrowhead region than the reverse moving carriers, which are more likely to be blocked by the flat walls on the right side of the arrowhead. This difference in probability causes dissimilar current levels for forward

(driving left-to-right motion) and reverse (driving right-to-left motion) bias voltages. As opposed to the MIM diodes mentioned in chapter 1, which have a parallel-plate structure, geometric diodes have a miniscule capacitance because of their planar structure. In addition, as geometric diodes are continuous conducting thin films, their resistance can be small enough for antenna impedance matching. Therefore, the overall resistor–capacitor (RC) time constant of geometric diodes is significantly lower than that of MIM diodes.

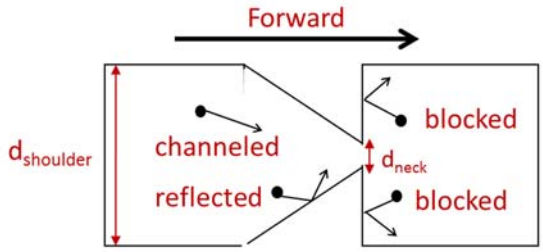


Figure II-1. Inverse arrowhead geometric diode structure. The width of the neck (d_{neck}) is on the order of the charge carrier's mean-free path length (MFPL) in the material. Charge carriers reflect off the interior boundaries of the geometric diode. On the left side of the neck, electrons or holes can either channel directly through the neck region or reflect at the sloped edge and keep moving forward. On the right side of the neck, the vertical edge blocks a majority of the electrons or holes. The inverse arrowhead direction from left to right is termed as the forward direction for carrier transport.

The fundamental physical requirement for the geometric diode is that its critical dimensions must be on the order of the charge mean free path length (MFPL) of the charge carriers in the material. At this scale, charge carrier transport within the diode around the neck region can be considered ballistic, such that the boundaries and the geometry of the device have substantial impact on the charge movement (Zhu 2011), (Zhu 2013).

CHAPTER III

SIMULATION OF GEOMETRIC DIODES

In this chapter, I introduce two methods to simulate graphene geometric diodes and subsequently discuss one of the methods, the Monte Carlo method, in detail. The first simulation method is based on quantum simulations using electron wave transport model developed by Sachit Grover in our group (Grover 2011). The simulation using the same method has also been implemented by Dr. Dragoman's group at IMT, Romania (Dragoman and Dragoman 2013). Their simulation results agree with our quantum simulation results. Another simulation method is based on the classical Drude model of electron movement (Ashcroft and Mermin 1976), (Zhu 2013). It does not suffer the disadvantages of the quantum simulator and is more practical for simulating the behavior of large-sized devices.

C. Quantum mechanical simulator

Our quantum mechanical simulator is capable of proving the concept of small-sized graphene geometric diodes. The simulator simultaneously calculates the solution of the Poisson's equation and the non-equilibrium Green's function (NEGF) (Datta 2000), (Datta 2002) to find the self-consistent device potential profile and charge distribution. Because of the computational complexity of the method, a relatively small device geometry confined to an area of 5 nm × 5 nm was simulated. As shown in Figure III-1, only a few atoms comprise the 1.5-nm neck. Figure III-2 displays the *I(V)* curves generated from quantum simulation of the small device. The shape of the *I(V)* curve agrees with Dr. Dragoman's quantum simulator result (Dragoman and Dragoman 2013).

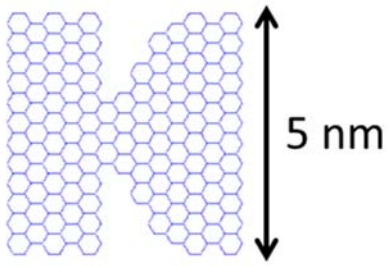


Figure III-1. The atomic structure of the graphene device used in the quantum simulation. This figure is from Sachit Grover's thesis (Grover 2011).

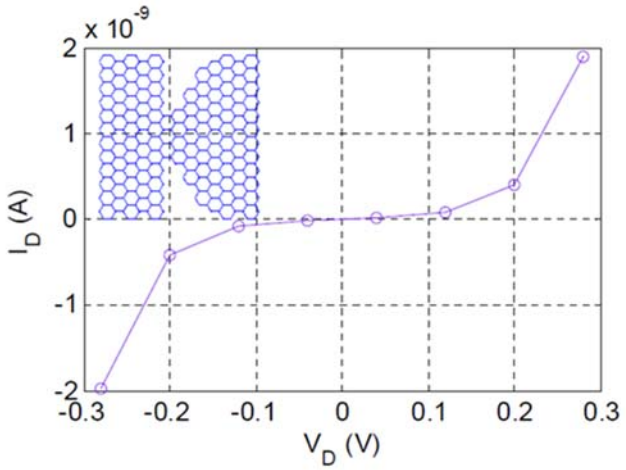


Figure III-2. Asymmetric *I(V)* characteristics of the geometric diode shown in Figure III-1. This figure is from Sachit Grover's thesis (Grover 2011).

Our quantum simulator simulates the effect of the gate voltage on a graphene device by changing the Bloch energy at each carbon atom (Reich 2002), (Wu and Childs 2010). Such energy change by an amount E_{offset} is equivalent to moving the Fermi level of the graphene. The graphene is p-type for $E_{offset} > 0$ eV and n-type for $E_{offset} < 0$ eV. In Figure III-3, the polarity of the diode is different at positive and negative E_{offset}. The reason is that the forward transport direction of the charge carriers is always the same for a certain device geometry, regardless of the carriers charge type (p- or n- type). The direction of the forward current changes with the change in the carrier type. As a result, the asymmetry ($A = |I(V_{DS})/I(-V_{DS})|$) of the net diode *I(V)* behavior will change direction with the change in the type of charge

carriers. This reversible polarity effect will be discussed in more detail in chapter 5 and will be confirmed in Figure V-8.

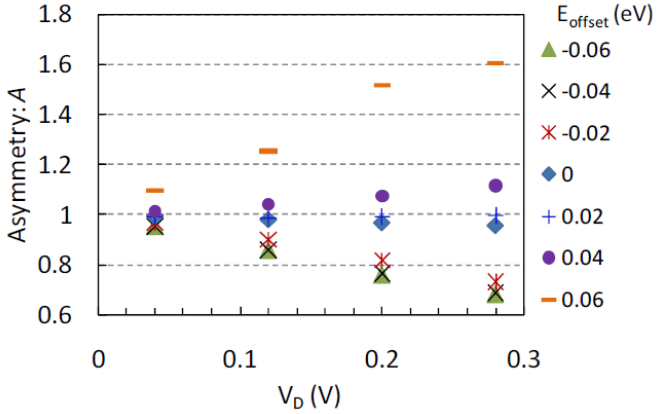


Figure III-3. Quantum simulation of diode asymmetry ratio A versus V_{DS} with changing energy E_{offset} in the Bloch energy of each carbon atom for the device shown in Figure III-1. Changing E_{offset} is equivalent to applying gate voltage. When E_{offset} is positive, the graphene is p-type and $A < 1$. When E_{offset} is negative, the graphene is n-type and $A > 1$. This figure is from Sachit Grover's thesis (Grover 2011).

D. Monte Carlo simulator

Prior to and in parallel with the development of the quantum simulator, I developed a Monte Carlo simulation based on the Drude model (Ashcroft and Mermin 1976) to simulate the electron movement in geometric diodes. After the device shape and boundaries have been defined, the simulator places an electron randomly within the device and sets it to move with a velocity (v_{tot}) until the electron collides with defects or phonons. The MFPL is the key material parameter, and is determined by the average electron collision time (τ). Between each collision, v_{tot} is a combination of the random Fermi velocity (v_F) and the constant drift velocity (v_{drift}) for a certain bias-dependent electric field; v_{drift} was calculated using Eq. III-1.

$$v_{drift} = \frac{\varepsilon e \tau}{m_e}$$

Eq. III-1

where, ε is the electric field caused by the applied voltage, e is the charge of the electron, and m_e is the effective mass of the charge.

In the simplified version of the simulation, the electric field within the diode is assumed to be the ratio between the applied voltage and the device length and to be uniform within the device. The electron specularly reflects at all the boundaries with the same magnitude of v_{tot}. The motion of the electron is tracked, and the Monte Carlo simulation continues to run until 10^6 collisions have occurred. Such a large number of collisions ensures a statistically reliable result that is independent of the starting position of the electron. The net current at a given bias voltage is calculated using the electron density of graphene and by counting the number of times an electron crosses a certain device cross-section per unit time.

The logic flow of the simulator is shown in Figure III-4. The main loop for the electron to move within a τ starts from the generation of a velocity (a combination of random Fermi velocity and applied drift velocity) for electron transport. The simulation calculates a predicted new electron location based on its previous location under the assumption of a constant v_{tot} within τ. The electron hops across the right to the left edge of the device and vice versa, under the assumption of periodic boundary condition for these two boundaries. If the predicted position of the electron is still within the boundaries of the device, the predicted position is assigned to the new location of the electron and the loop for the next τ would start. Otherwise, the simulator would divide τ by 100 segments and allow the electron to move one step at a time. The electron position after every small time step is examined to determine whether it is within the boundaries. As shown in Figure III-5, the closest boundary of the device is treated as the mirror plane. If the predicted nth electron position (A')

is outside the boundaries, the electron position at the start of the (n+1)th time step is the mirrored position along the normal to the closest boundary. The new velocity of the electron after this reflection is calculated assuming the electron is specularly reflected from the mirror plane. The advantage of using this method for simulating the electron specular reflection at the boundaries is its easiness of handling multiple reflections that occur within one τ with the assumption that 1/100th of the electron MFPL is much shorter than the critical dimension of the geometric diode. At the end of the loop for each τ, the total charge Q_{tot} is updated on the basis of whether the electron had hit the right or left edge of the device.

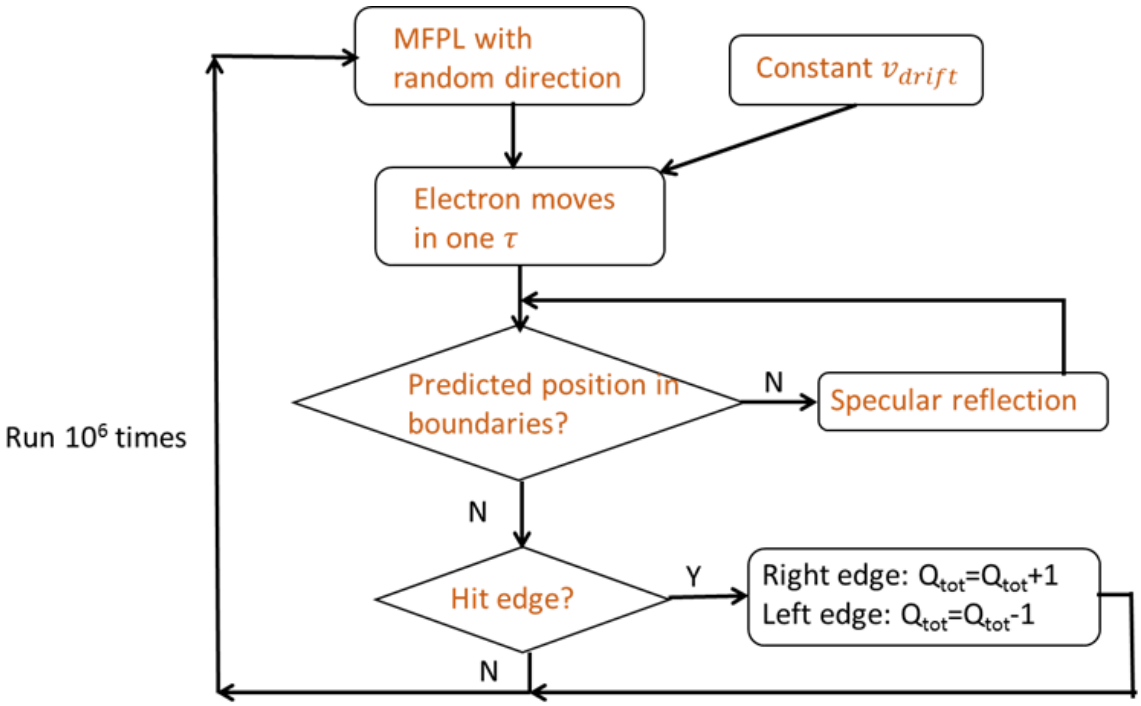


Figure III-4. Logic flow of Monte Carlo Simulation for geometric diodes.

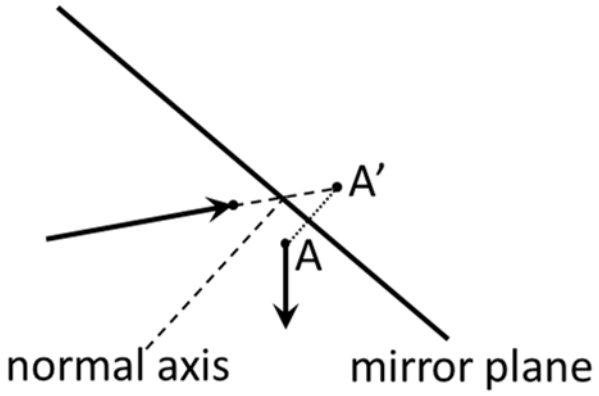


Figure III-5. Reflection of the electron from the predicted nth location A' to its reflected location, which is also the start location A for the (n+1)th movement. The mirror plane is the closest boundary of the device to the electron.

According to the device principle discussed in chapter 2, the diode's geometric asymmetry and the constriction width d_{neck} determines the *I(V)* asymmetry of the diode. Figure III-6(a) shows the *I(V)* curves at various d_{neck} values in the simulator to visualize the impact of changes in the d_{neck} values. The *I(V)* curves with varying shoulder width ($d_{shoulder}$) are presented in Figure III-6(b). Based on the *I(V)* data presented in Figure III-6(a), the diode asymmetry value (*A*) is plotted as a function of the absolute value of V_{DS} in Figure III-6(c) for different d_{neck} values. Figure III-6(d) shows the impact of varying the neck slope between 30° and 70° on the *A* of the diode. In all simulations, MFPL was set to 200 nm.

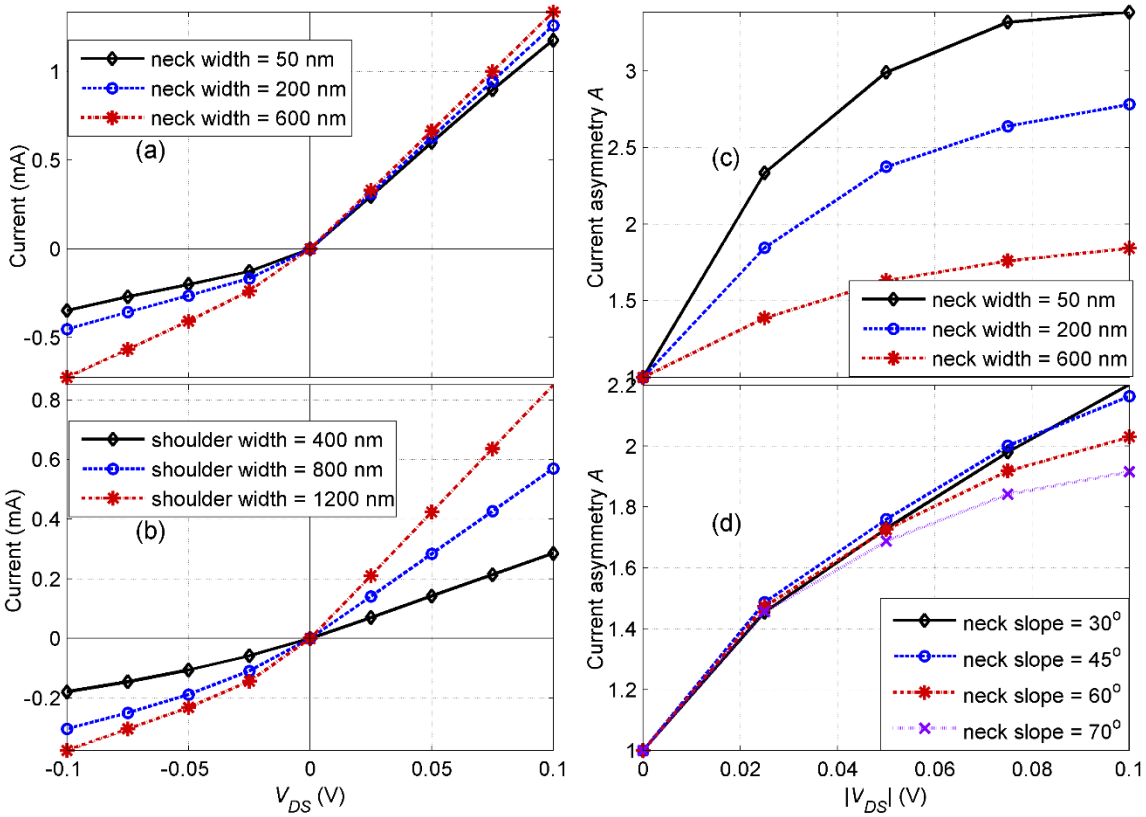


Figure III-6. Monte Carlo simulation results. (a) Simulated *I(V)* curves of the geometric diode with different neck widths: 50 nm, 200 nm and 600 nm. The shoulder width is fixed at 1 μm. The neck width has strong effect on the diode reverse current. A smaller neck restricts the reverse current more efficiently. (b) Simulated *I(V)* curves of geometric diode with different shoulder widths: 400 nm, 800 nm and 1200 nm. The neck width is fixed at 50 nm. Simulated *I(V)* curves for a geometric diode with different shoulder widths for a fixed neck width of 50 nm. Wider shoulders increase the forward and reverse current magnitudes. (c) Varying neck width using the data from Figure S1a. Increasing V_{DS} and reducing neck width leads to higher asymmetry. (d) Varying arrowhead slope angle from 30 to 70 degrees. Within this range, the slope angles do not have a great impact on the asymmetry ratio. The MFPL in all the simulations is fixed to be 200 nm.

The *I(V)* curves in Figure III-6(a) indicate that a decrease in d_{neck}, while maintaining all other device dimensions, increases the *I(V)* asymmetry. This effect can be better observed in Figure III-6(c), in which smaller d_{neck} values have higher *A* levels. In addition, Figure III-6(c) shows that an increase in V_{DS} also increases *A*.

With larger drift velocity under higher V_{DS}, the transport of the electrons is more sensitive to the device geometric asymmetry. When V_{DS} increases further, the electron flow becomes insensitive to the physical structure. The reason is that when the drift velocity is large compared to the Fermi velocity, the transmission probabilities of charges in both forward and reverse directions are the same. As a result, A will eventually drop back to 1.

Besides d_{neck}, another factor that affects the *I(V)* asymmetry is the $d_{shoulder}$. A comparison of Figures III-6 (a) and (c) reveals that a reduction of d_{neck} has stronger depressing impact on the reverse current, because d_{neck} acts as a blocking mechanism for the electrons traveling in the reverse direction. On the other hand, an increase in the $d_{shoulder}$ results in a greater forward current, because the larger $d_{shoulder}$ reduces the probability of electrons bouncing back to the neck region after they funnel through the neck region. Thus, larger $d_{shoulder}$ increases the forward current and smaller d_{neck} reduces the reverse current. Overall, they all improve the diode *I(V)* asymmetry.

The effect of the other geometric parameter, the neck slope, is not as strong as those of the shoulder and neck widths. As shown in Figure III-6(d), no obvious effect of the neck slope on A is observed between 30 and 45 degrees. When the slope is increased to 60 and 70 degrees, A begins to reduce. This conclusion for the neck slope effect is qualitative and only for the specific diode that was simulated. More work will be required in the future to study the quantitative impact of changing the neck slope.

All the simulation results shown above were based on an assumption that charges specularly reflected at the boundaries of the device. As mentioned in chapter 2, the ballistic region of geometric diodes is the neck region. Within the neck region, the reflection of the charges at the boundaries is ideally specular - outgoing angle equal to incoming angle (Song 1998). Due to phonon and surface roughness scattering, the reflection of the charges at the boundaries is expected to have a diffusive component in real devices. The outgoing angle of the reflected charge has a probability

distribution averaged at the perfectly specular reflected angle (Löfgren 2003). I also studied the impact of diffusive reflection of the charges on the diode *I(V)* asymmetry, as shown in Table III-1. For a diode with fixed geometry (d_{neck} = 40 nm, $d_{shoulder}$ = 400 nm), the charge reflection at the edge occurred locally, when the MFPL was shorter than d_{neck}. Both specular reflection and diffusive reflection models showed similar diode *I(V)* asymmetry. When the MFPL was larger than d_{neck} but much smaller than $d_{shoulder}$, specular reflection model of charges gave larger asymmetric *I(V)* characteristics, because of the directionality of specular reflection. In the extreme case for the MFPL being on the order of $d_{shoulder}$, specular reflection of charges lost its directional advantage, because the physical geometry started limiting the direction of either type of reflection.

MFPL (in nm)	**Diode *I(V)* asymmetry (specular reflection model)**	**Diode *I(V)* asymmetry (diffusive reflection model)**
10	1.3	1.3
20	1.29	1.26
40	1.31	1.25
60	1.4	1.29
100	1.46	1.3
200	1.47	1.62

Table III-1 Lists of diode *I(V)* asymmetry ratio A values simulated using the specular reflection model and the diffusive reflection model. The geometry of all the simulated device was all same: d_{neck} = 40 nm, $d_{shoulder}$ = 400 nm. Charge MFPL varies from 10 nm to 200 nm.

The previously described simplified Monte Carlo simulator assumes a uniform electrical field across the whole device. A full-version simulator was also developed using finite-difference time-domain (FDTD) software to simulate the real electrical field (E-field) map within the device. In the full-version simulator, COMSOL simulates the E-field map of the device and passes the result to the Monte Carlo

simulator through the COMSOL Livelink MATLAB package. Figures III-7 and III-8 show the simulated E-field map of a reverse arrowhead-shaped geometric diode. In the case of inverse arrowhead-shaped geometric diodes, the E-field was reasonably uniform within the device, except at a few sharp corners.

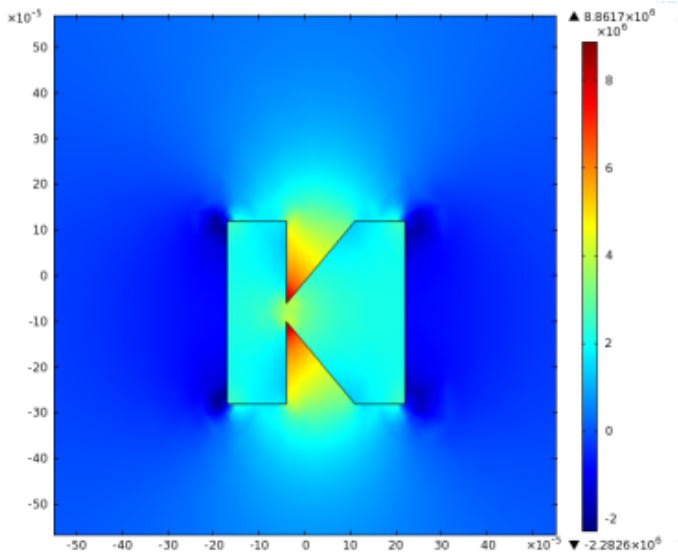


Figure III-7. Simulated x-direction electrical field map within geometric diode by COMSOL. The 1 V voltage was applied to the left edge of the device and the right edge of the device was grounded. The unit of the scale in the figure is in mm.

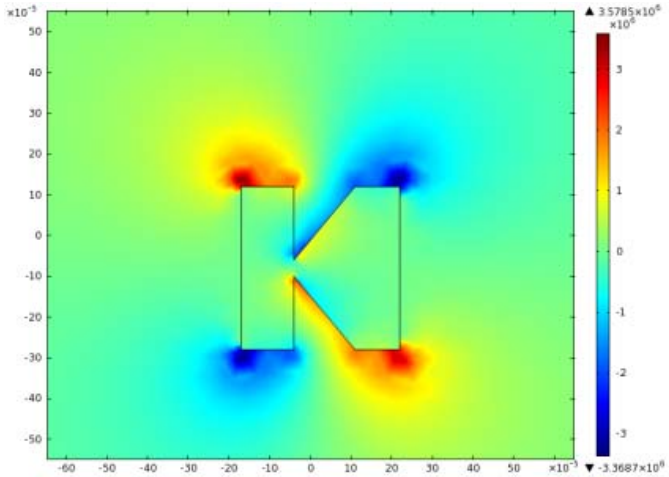


Figure III-8. Simulated y-direction electrical field map within geometric diode by COMSOL. The 1 V voltage was applied on the left edge of the device and the right edge of the device was grounded. The unit of the scale in the figure is in mm.

Another new feature of the full-version Monte Carlo simulator is that it includes the effects of the electron–electron interaction forces instead of assuming that the electrons move independently of each other. Unlike invoking the Green's function to calculate the net force (Datta 2000), (Datta 2002), the classical Monte Carlo simulator calculates the net force from all the Coulomb forces between each electron pair. Although the exact number of free electrons within graphene depends on its Fermi level, only ~4000 free electrons are present within a 500 nm × 1 μm graphene piece. Thus, the computation is not as time consuming as it first appears.

To maintain charge neutrality within the device, a background E-field has been included with the externally applied E-field and electron-electron interaction forces by assuming that an equal amount of stationary positive charges have been uniformly spread within the device. Figure III-9 shows the simulated results for the same device obtained using both the full- and the simplified-version simulators. The *I(V)* curves provided by the two simulators are very similar to each other. Figure III-9 shows the simulated *I(V)* characteristics of allowing 100 charges to run 10^3 τ averaged from 10 runs of the simulation labeled as 'Full Simulator I', and of allowing 100 charges to

run 10^4 τ marked as 'Full Simulator II'. They show almost no difference between each other.

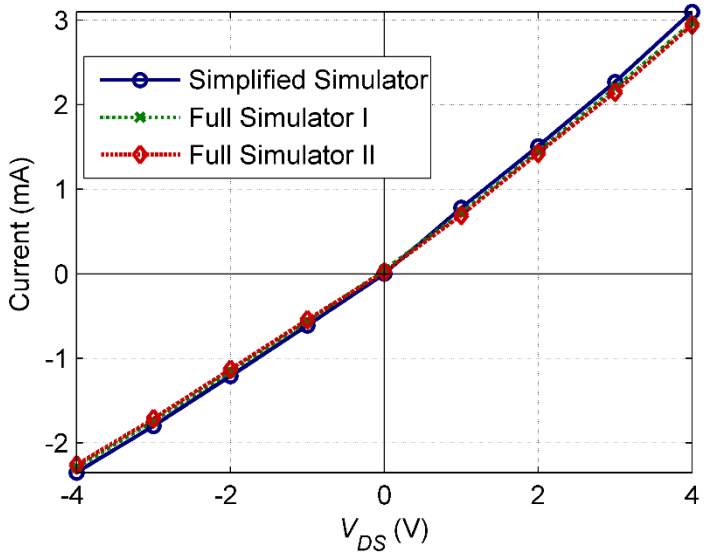


Figure III-9. Monte Carlo simulation results: simulated *I(V)* curve using the simplified-version simulator by allowing one charge to run 10^6 τ (blue line with circle marks), simulated *I(V)* curve using the full-version simulator by allowing 100 charges to move 10^3 τ (green line with cross marks) averaged from 10 runs of the simulation, and simulated *I(V)* curve using the full-version simulator by allowing 100 charges to move 10^4 τ (red line with diamond marks). The geometric diode has a neck width of 50 nm and a shoulder width of 500 nm. The charge mean free path length (MFPL) in all the simulations is 100 nm.

The full-version Monte Carlo simulator has at least three advantages compared to the simplified-version. First, the E-field map in the full-version simulator is more realistic than that in the simplified-version.

Second, by counting the electron-electron interaction forces, the full-version simulator simulates the local charge build-up effect at the corners of geometric diodes. The charge build-up effect may reduce or enhance the geometric effect, depending on the geometry of the diode. As shown in Figure III-8, such a charge build-up effect has almost no impact on the *I(V)* characteristics of the inverse arrowhead shape geometric diode. In chapter 8, a geometric diode with a new shape, i.e., a Z-shape, is introduced,

which is more asymmetric than the inverse arrowhead shape. The charge build-up effect has more influence on its *I(V)* characteristics. Details of this analysis are discussed in chapter 8.

Third, the diffusion effect of the charges is included in the full-version simulator. In the simplified-version simulator, there is always a small current offset at 0 V V_{DS}, because without taking into account of the electron-electron interactions, only the drift velocity of the charges is encountered in the simplified-version simulator. Compared to the current level of geometric diodes under bias, this tiny current offset can be normally ignored. However, diffusion of charges exists in the real physical model of geometric diodes and it creates a built-in E-field to balance out the offset of the current at 0 V V_{DS}, as occurs in conventional semiconductor diodes.

CHAPTER IV

FABRICATION OF GEOMETRIC DIODES AND RECTENNAS

A. Metal geometric diodes

1. Charge mean-free path length of metal geometric diodes

The material used to fabricate the geometric diode must meet two requirements. First, it must have a sufficiently large charge-carrier mean-free path length (MFPL), and second, it must have the ability to withstand high current density through the neck, up to 10^6 A/cm^2. This high current density is estimated from the simulated *I(V)* behavior in chapter 3.

Obviously, metal was my initial choice for fabricating geometric diodes. The MFPL of charge carriers in metals at room temperature is up to 50 nm (Ashcroft and Mermin 1976), (Zhu 2013) which may necessitate impractically small neck geometries. Table IV-1 lists the MFPL of different types of metals at 77 and 300 K temperatures. The calculation is based on the Drude model of metals (Ashcroft and Mermin 1976). Although at 77 K, bulk copper has the longest MFPL, ~335 nm, it was not the first choice as the material for fabricating geometric diodes, because the final goal of our project is to harvest solar energy at room temperature. At room temperature, silver has the longest MFPL, ~50 nm. However, thin film metals have shorter MFPL than bulk metals because of the grain boundaries in thin film metals (Durkan 2013). The conductivity of a thin film metal is normally two to four times lower than that of the same bulk metal.

Metal	MFPL at 300K (nm)	MFPL at 77K (nm)	Melting T (ºC)
Ag	50	290	960
Au	30	170	1064
Cr	4.3		1907
Pt	6		1768
Al	11.3	134	660
W	12		3422
Cu	30	335	1084

Table IVV-1 Important properties of different types of metals.

2. Fabricated metal geometric diodes using focused ion beam (FIB)

Figure IV-1 shows a geometric diode made from silver using the focused ion beam (FIB) patterning method with the FEI Nova 600 Nanolab system in the Nanomaterials Characterization Facility (NCF) at the University of Colorado. The thickness of the silver film was ~50 nm and a neck width (d_{neck}) of 100 nm was achieved. To achieve smooth cutting edges, I deposited a 1 - 2 nm thick platinum layer over the silver to absorb the extra ion beam energy during the cutting process.

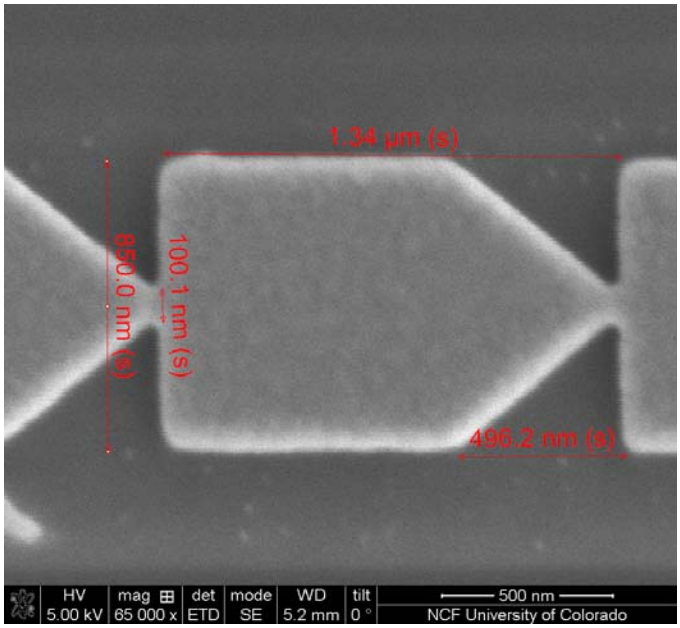


Figure IV-1. Scanning electron microscope (SEM) image of a fabricated silver geometric diode using the focus ion beam (FIB) method. The achieved neck width is ~100 nm.

3. Fabricated metal geometric diodes using glancing-angle evaporation

I also used the glancing-angle evaporation method, as shown in Figure IV-2, to produce a SiO surface with sloped structures. The atomic force microscope (AFM) image in Figures IV-3 and IV-4 shows the existence of triangular structures on the surface. The shape and size of these triangular structures was inconsistent and difficult to control.

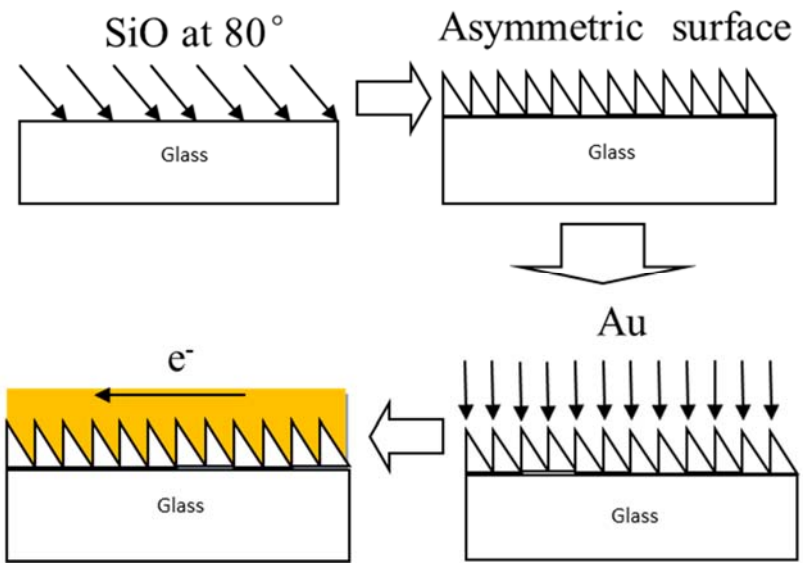


Figure IV-2. Process flow of glancing angle evaporation.

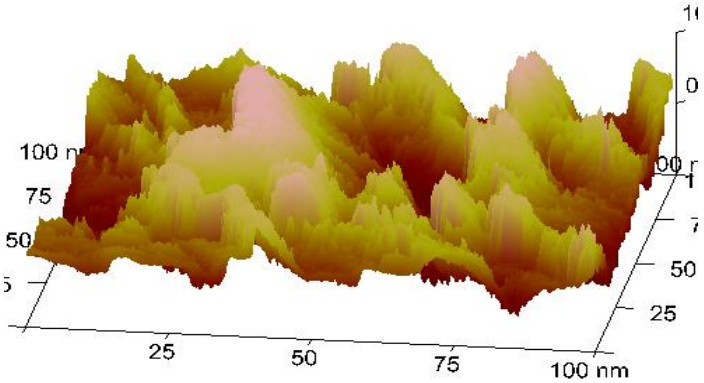


Figure IV-3. Atomic force microscope (AFM) image of the SiO surface structure using the glancing angle evaporation method.

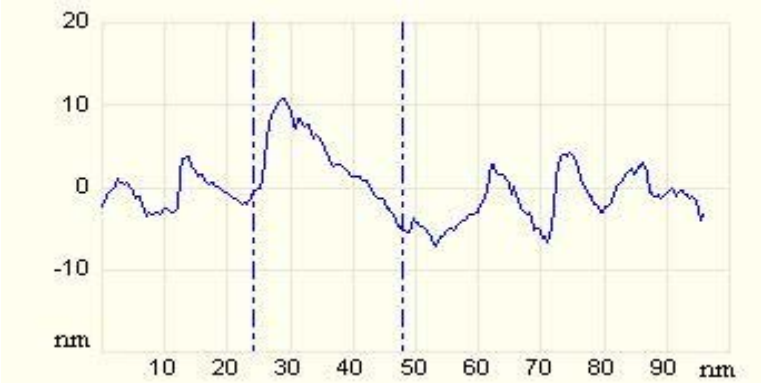


Figure IV-4. The height profile of the SiO surface structure in Figure IV-3.

B. Graphene geometric diodes

1. Preparation of graphene samples

To circumvent the disadvantages of metals as described above, I incorporated graphene instead. The MFPL of graphene can be up to 1 μm, which corresponds to a carrier mobility of 200,000 cm^2/V^{-s} (Castro 2009). The long MFPL of graphene not only eases the requirement for nano-scale patterning, but also gives a larger geometric effect. In addition, graphene can withstand a current density of up to 10^8 A/cm^2 (Avouris 2010). Exfoliation and chemical vapor deposition (CVD) are the two most frequently used methods to prepare graphene samples. To achieve high-quality graphene samples, exfoliation is currently the best method. The process steps of our graphene exfoliation method are summarized below and shown in Figure IV-5.

1. Peel thin flakes from large purified mineral graphite flakes and place these small flakes at one end of the sticky side of a piece of scotch tape.
2. Re-adhere the region with graphite to an empty region of the tape's sticky side and pull apart again. Repeat this step 4 or 5 times on the remaining empty regions with the same piece of tape until small graphite flakes are evenly spread out throughout the tape.
3. If the graphite region on the tape still looks dark black, get a fresh piece of tape, adhere it to the tape used in step 2, and pull them apart. Repeat this step until the tape is gradually covered with a shiny-gray graphite "film."
4. Next, adhere the sticky side of the bottom piece of the tape to the silicon wafer piece. Press the tape firmly onto the wafer and brush it with a plastic card.

   The silicon wafer is highly doped with a sheet resistance of 1–5 Ω/sq. A 90 or 300 nm thick SiO_2 layer was thermally grown on the top of the silicon wafer to give highest optical contrast of the graphene pieces. The doping of the SiO_2 surface layer significantly impacts the charge-neutral-point voltage (V_{CNP}) of

the exfoliated graphene. To reduce the surface doping level, I etched 300 nm SiO_2 to 90 nm SiO_2 with BOE solvent.

5. The silicon wafer can now be viewed under an optical microscope. The color and thickness will vary. A single layer of graphene has a faint color, as shown in Figure IV-5. The thickness of the graphene pieces can also be verified under an AFM for verification.

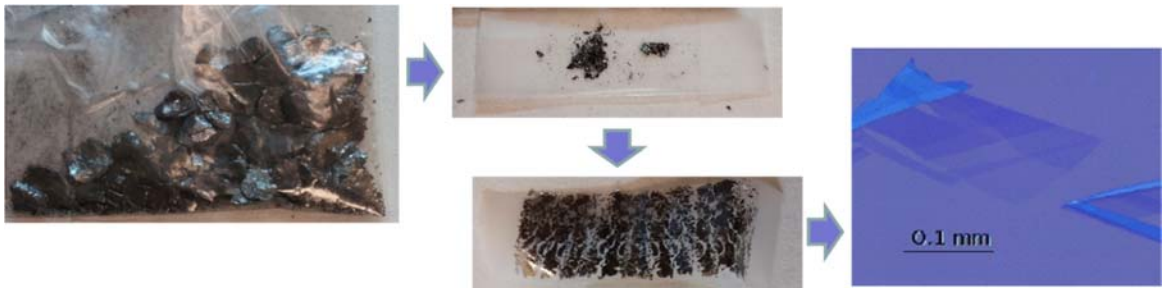


Figure IV-5. Process flow of exfoliating graphene pieces.

Although the exfoliated graphene samples have the best quality, they are randomly located on the wafer. The sizes of the exfoliated graphene pieces are also small, normally on the order of 10-100 μm^2. Therefore, the mass production of graphene devices is difficult.

Large-area graphene samples can be achieved using the CVD method. For a good lattice match, CVD graphene layers are first grown on copper foil pieces, and then transferred to silicon wafer substrate. During the process, a layer of poly-methyl methacrylate (PMMA) was first spun onto the graphene surface as a holder substrate. After etching out the bottom copper foil using copper etch, the graphene with PMMA layer on top would float in the solvent. The membrane of graphene will PMMA was picked with tweezers and could be laid on any other substrate. We received CVD samples from several groups: Mark Keller's group at NIST, McEuen's group at Cornell, and Graphenea Inc. Figure IV-6 shows a CVD graphene sample from McEuen's group at Cornell. Unfortunately, the MFPLs of all CVD graphene samples

were still shorter than that of the exfoliated graphene pieces. Mark Keller's group in NIST produced the best CVD graphene samples. The MFPL of their graphene samples was ~30 nm with a V_{CNP} ~10 V. For research purpose, we focused on developing geometric diodes from the exfoliated graphene pieces.

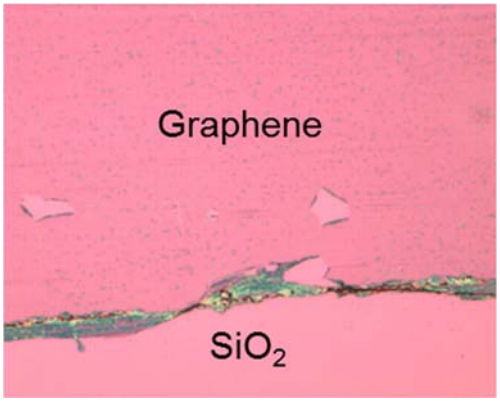


Figure IV-6. Graphene samples prepared by the chemical vapor deposition (CVD) method.

2. Fabricated graphene geometric diodes using FIB

At the beginning of the project, geometric diodes were patterned using the FIB method. Figure IV-7 shows the fabricated graphene geometric diodes. The devices had smooth edges and the achieved minimum d_{neck} was ~75 nm. However, except for a few devices, almost all the graphene devices lost their conductivity after the FIB patterning process. Such effect could be caused by the doping/damaging from the gallium ion beam (Prével 2011). A possible solution is to use the FIB system with the helium ion beam (Lemme 2009), but only a few helium ion beam systems exist in USA. Thus, I shifted to the e-beam lithography patterning technique to fabricate graphene geometric diodes.

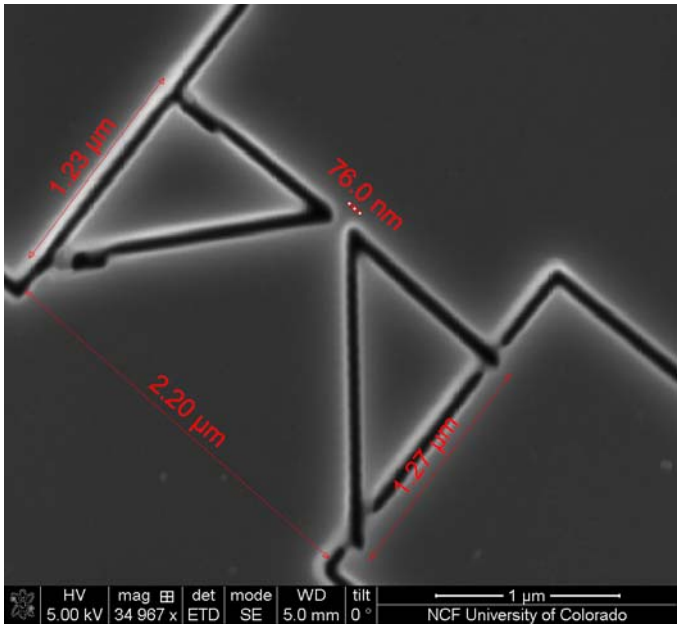


Figure IV-7. Graphene geometric diode patterned using focus ion beam (FIB) method. The achieved neck width is ~75 nm.

3. Fabricated graphene geometric diodes using e-beam lithography

To reliably fabricate graphene geometric diodes, I used photolithography and e-beam lithography methods. Before patterning the graphene pieces, four metal contacts were patterned onto the graphene flake using optical lithography and liftoff. The metal contacts (15 nm Cr/40 nm Au) were thermally evaporated and lifted off from the NR9-1000PY photoresist. With the coordinates of the exfoliated graphene pieces, I used the JEOL 9300 e-beam writer at the Cornell NanoScale Science and Technology Facility (CNF) to pattern the asymmetric geometric shape in the negative-tone maN resist. The process flow of patterning graphene geometric diodes is shown in Figure IV-8. After developing the resist, O_2 plasma etching at 50 W power and 30 mTorr pressure was applied for 15 s to etch the unprotected graphene region.

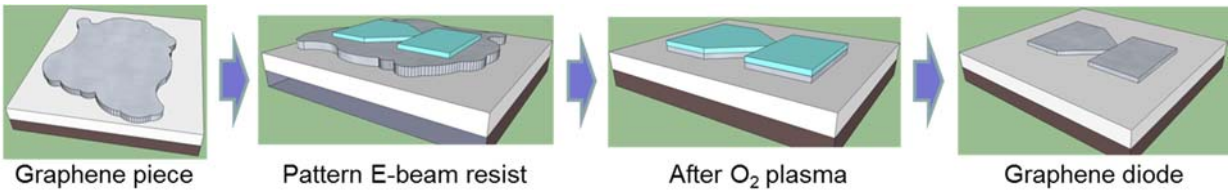


Figure IV-8. Process flow of patterning graphene pieces into geometric diode.

An automatic e-beam writer system, such as the JEOL 9300 system, requires knowing the exact location of the graphene flakes for auto-alignment. To process randomly located exfoliated graphene pieces, I designed a grid map system for the silicon wafer substrate to locate graphene pieces precisely. In the mapping system, the 4" silicon wafer was divided into 23 × 23 cells. Each cell, as shown in Figure IV-10, was filled with grid points set 50 μm apart in both x and y directions, including a set of local alignment marks for e-beam lithography. This grid map system was implemented by evaporating and lifting off 15 nm/30 nm Cr/Au onto the silicon wafer before performing the exfoliation process. After inspection under an optical microscope and verification of the graphene thickness using an AFM, I selected single-layer graphene pieces. Screen shots of the graphene flakes were taken using an optical microscope and a computer. These images were imported into the CAD software L-edit and placed at the location that matched the grid points in the mapping CAD file. After going through this process, I could read the exact corresponding coordinate of each graphene piece and perform a virtual alignment to place the geometric diodes, as shown in Figure IV-9.

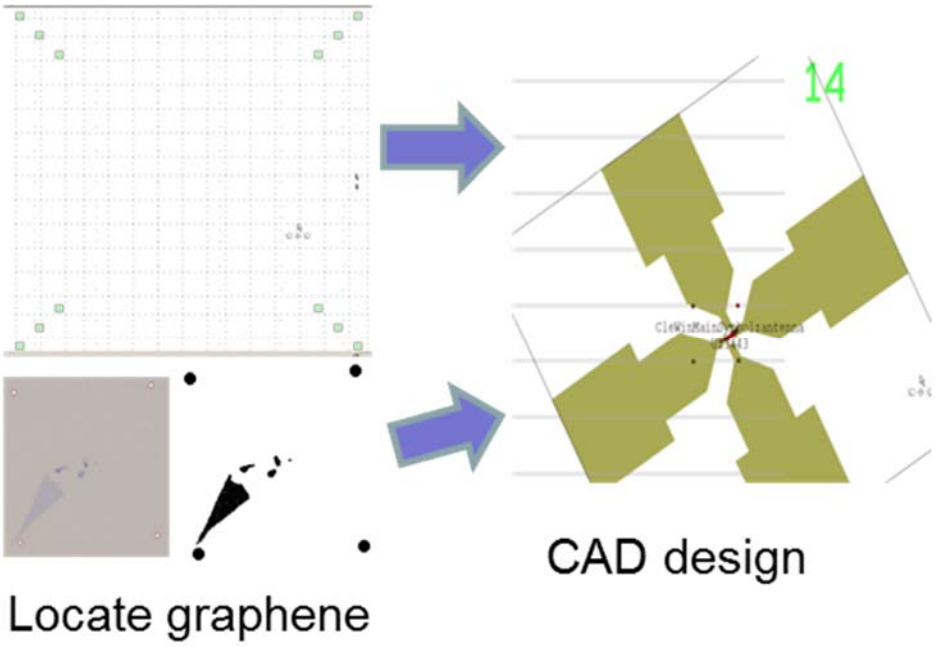


Figure IV-9. CAD file screen shots of the grid map system for locating the exfoliated graphene for virtually aligning the geometric diodes pattern.

The patterned negative-tone maN e-beam resist is shown in Figure IV-10 and a patterned positive-tone PMMA resist is shown in Figure IV-11.

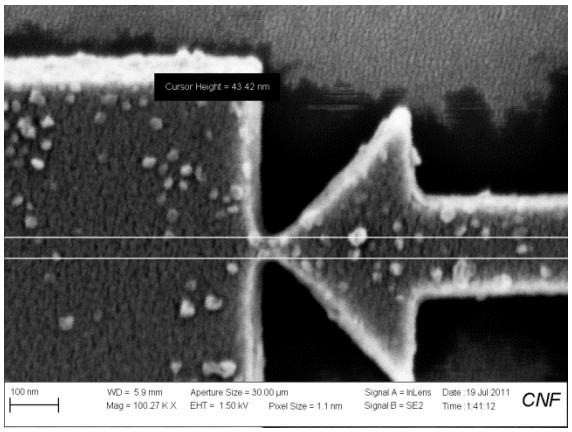


Figure IV-10. Scanning electron microscope (SEM) image of the negative maN electron beam (e-beam) resist after developing. The corners of the pattern are reasonably sharp.

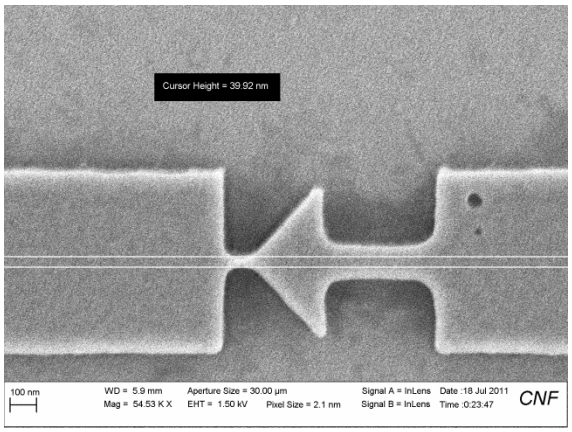


Figure IV-11. Scanning electron microscope (SEM) image of the positive PMMA electron beam (e-beam) resist after developing. Because positive resist uses an inverse pattern of that for the negative resist, the corners at the neck region of the geometric diode are rounded.

Another commonly used negative e-beam resist, hydrogen silsesquioxane (HSQ), is not suitable for patterning graphene. HSQ resist is difficult to strip off from graphene after performing the O_2 plasma etch. Figure IV-12 shows a semi-stripped HSQ resist pattern.

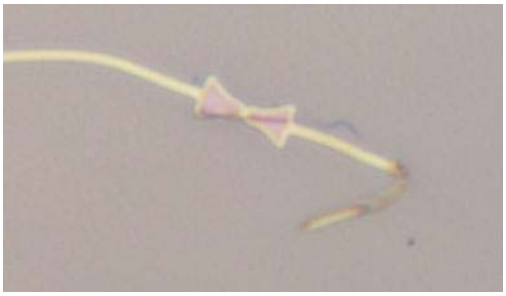


Figure IV-12. Optical microscope image of the HSQ resist pattern after been stripped in the 60 ºC heated 1165 stripper solvent for 4 hours.

A fabricated graphene geometric diode is shown in Figure IV-13 and Figure IV-14. The d_{neck} of the diode was measured to be ~75 nm.

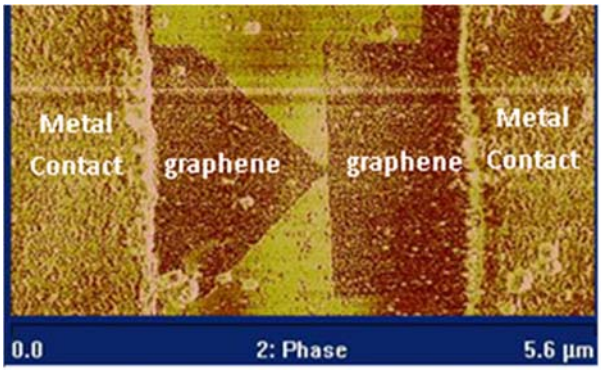


Figure IV-13. Atomic force microscope (AFM) image of a graphene geometric diode between two metal contacts. The neck width of the diode was measured to be ~75 nm. The graphene surface followed the surface roughness of the SiO_2 substrate causing the texture structure in the image.

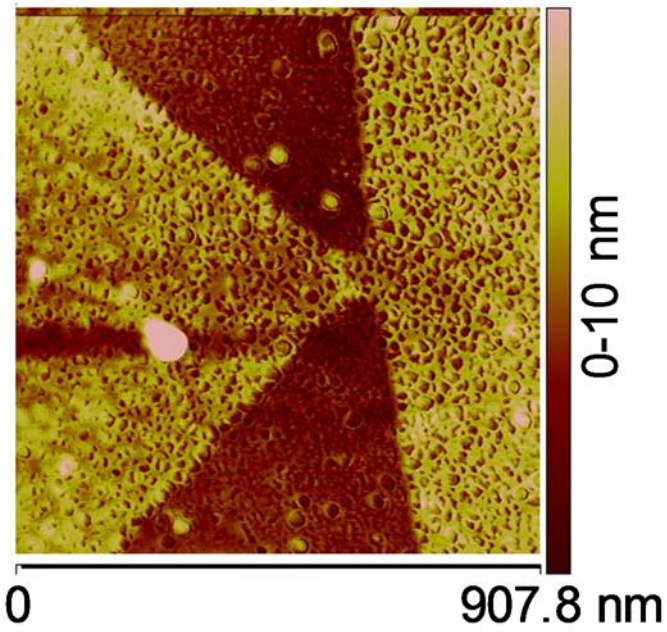


Figure IV-14. Atomic force microscope (AFM) zoom in image of the fabricated graphene geometric diode in Figure IV-11.

Besides the JEOL e-beam writing system, I also used a converted scanning electron microscope (SEM) system with PMMA and ZEP positive resist to pattern Z-shape geometric diodes, as shown in Figure IV-15. This part of the work was conducted in the JILA Keck laboratory at the University of Colorado. This system was a Nova SEM controlled by a third party add-on software, called Nanometer Pattern Generation System (NPGS), requiring a semi-manual alignment process. To

minimize the external doping to the graphene from e-beam, I used line dose to define the conductive pattern forming the geometric diode. In addition, to improve the line width resolution, I developed PMMA resist in the MIBK/IPA developer cooled at -4 ºC (Hu 2004).

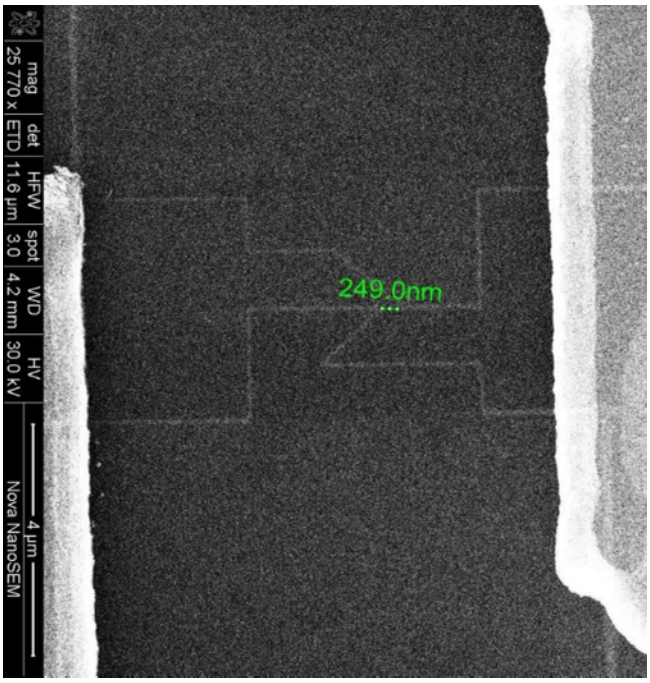


Figure IV-15. Scanning electron microscope (SEM) image of the Z-shape geometric diode. The achieved neck width is ~250 nm.

C. Fabricated rectennas

The fabrication process of rectennas is similar to that of making diode-only devices. Two types of rectennas have been fabricated. One is a coupling system consisting of graphene geometric diodes, and metal bowtie antennas. The antenna was designed to operate at 28 THz. An AFM image of the fabricated rectenna system is shown in Figure IV-16. The gold bowtie antenna consisted of two 2.3-µm-long triangular arms with 0.5 µm gap in the center (González and Boreman 2005). The graphene geometric diode was patterned using e-beam lithography and was placed in the antenna gap region, so that it was electrically connected to the antenna arms. I

used an edge-fed configuration (Weiss 2004) to lead the DC voltage and current out from the edges of the antenna to the probe contact pads. The metal antennas and contact leads were patterned using the conventional optical lithography method with a Suss MicroTec MJB4 contact aligner.

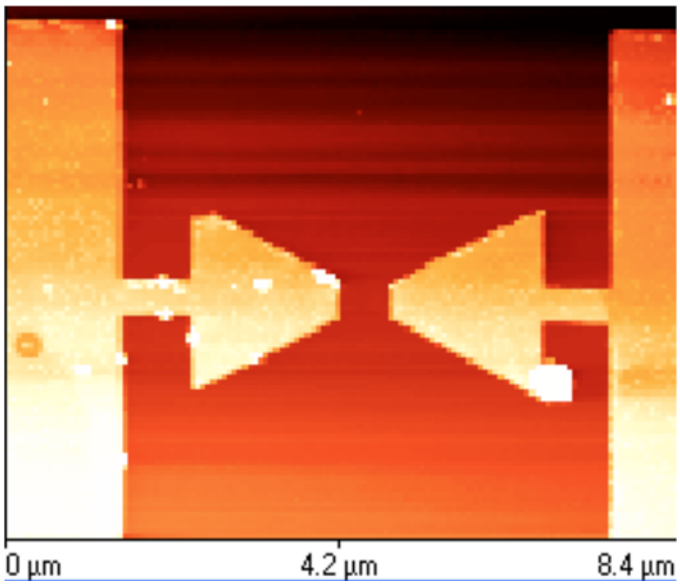


Figure IV-16. Atomic force microscope (AFM) image of a graphene geometric diode coupled to a metal bowtie antenna. Compared to the thickness of graphene, the significantly thicker metal antenna leaves the geometric diode invisible.

The second type of rectenna devices are graphene geometric diodes/graphene antenna rectennas. The graphene antenna and diode were patterned during a single e-beam lithography step. Figure IV-17 shows an AFM image of the graphene rectenna. It has the same dimensions as the metal antenna/graphene diode rectenna.

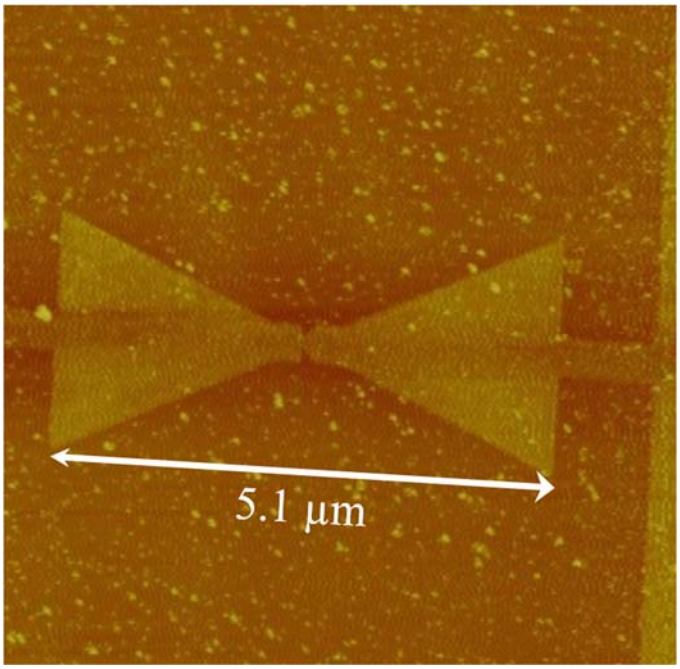


Figure IV-17. Atomic force microscope (AFM) image of a graphene rectenna system consisting of a graphene geometric diode and a graphene antenna.

CHAPTER V

DEVICE MEASUREMENT RESULTS

A. Metal geometric diodes

Metal geometric diodes suffer from electomigration effects (Black 1969) (Lienig 2013). Figure V-1 shows the silver device of Figure IV-1 after applying 0.1 V DC voltage for approximately 1 ms using a HP 4145B parameter analyzer. The high density of electrons physically pushed the metal atoms.

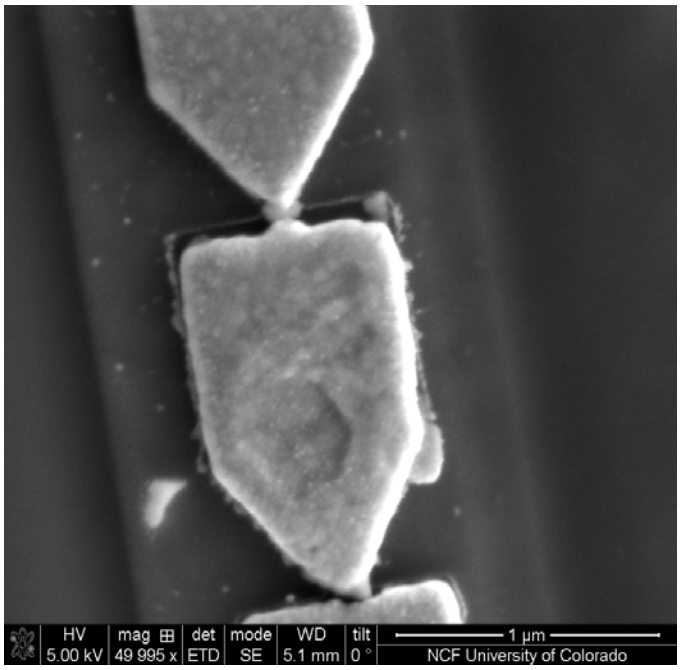


Figure V-1. Scanning electron microscope (SEM) image of the fabricated silver geometric diode of Figure IV-1 after applying 0.1 V DC voltage.

As for the geometric diodes fabricated using the glancing-angle evaporation, their performance was difficult to control due to the inconsistency of the SiO surface as shown in Figure IV-2. The *I(V)* characteristics of this thin layer of geometric diodes did not show significantly nonlinear asymmetric diode behavior, because it was a serial and parallel combination of the devices with good and bad nonlinearity.

In parallel, we have fabricated gold geometric diodes with ~20 nm d_{neck} using the electron beam (e-beam) lithography and metal liftoff method. In the DC measurements, the gold devices that did not suffer from electromigration exhibited linear *I(V)* behavior because of the short MFPL in the thin film, but their I(V) characteristics showed linear behavior (Durkan 2013).

B. Graphene device measurement at DC

As described in Chapter IV, I chose graphene as the material owing to its long charge MFPL and its capability to handle extremely high current density such as ~10^8 A/cm^2 (Avouris 2010). This characteristic allows fabrication of devices that are sufficiently large within the capabilities of the current lithography techniques.

1. Graphene gate-effect measurement

A unique property of graphene is its conic band structure (Castro 2009), which allows the carrier concentration of the graphene to be controlled by the gate voltage. Such a gate effect can be observed by measuring the drain-source current (I_{DS}) versus the gate voltage (V_G) of a graphene strip. The gate voltage can be applied to the substrate or by adding a top gate structure. The I_{DS}-versus-V_G curve is called a Dirac curve (Castro 2009). The charge neutral point (CNP) occurs for a gate voltage at which the electron and hole concentrations are equal, corresponding to a conductivity minimum.

Before measuring fabricated graphene geometric diodes, the MFPL in graphene was calculated from the measured graphene gate effect described above (Nayfeh 2011). The gate effect measurement setup using four-point contacts is shown in Figure V-2. Four-point measurements with pulsed bias voltage were carried out to eliminate the contact resistance by separating the current-carrying and voltage-sensing electrodes (Zhu 2013), although the contact resistance of our devices were measured to be only ~20 ohms, which is much lower than kilohms resistance for the graphene devices. The DC voltage was applied at the outer two metal contacts, and current I_{DS} was

simultaneously measured. Simultaneously, the actual voltage drop V_{DS} across the diode between the inner two contacts was measured. For graphene devices, the ability to perform gate-effect measurement is required. I implemented the gate voltage by connecting a power source to the metal holder of the probe station. Furthermore, the wafer's silicon substrate had an ohmic contact with the metal holder of the probe station. The ohmic contact was achieved by using highly doped silicon wafers, as mentioned in chapter 4, and applying the gate voltage to the large area wafer substrate. I have also measured the actual gate voltage on the wafer surface by etching out the top SiO_2 layer. The difference between the voltage on the wafer top surface and on the metal holder was negligible.

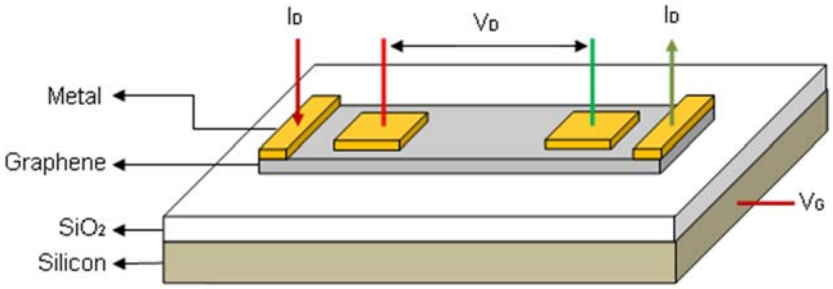


Figure V-2. Four-point probe measurement setup circumvents contact resistance that distorts two-point measurements. A voltage was applied to provide drain-source current (I_{DS}) through the outer two metal contacts. The actual voltage drop across the diode (V_{DS}) was measured between the inner metal contacts. A back gate voltage (V_G) was applied directly to the silicon substrate to control the carrier type and concentration in the graphene.

For our graphene, the CNP was obtained for a gate voltage of 24 V, as shown in Figure V-3. The suppression of the current at 0 V gate voltage indicates that graphene has a small mesoscopic CNP inhomogeneity (Connolly 2010) (Lohmann 2009). When the gate voltage is below the CNP voltage, holes are the majority charge carriers, and for gate voltages above the CNP voltage, electrons are the majority charge carriers.

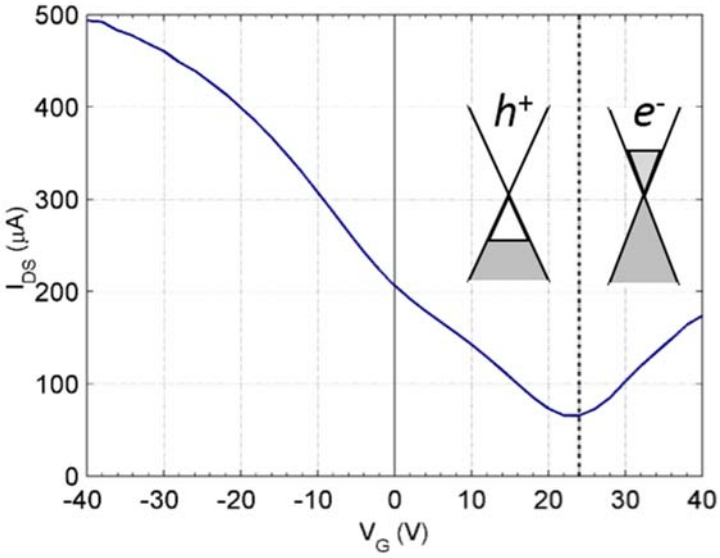


Figure V-3. Dirac curve [drain-source current (I_{DS}) versus back gate voltage (V_G)] of the graphene used for fabricating the graphene geometric diode. The drain-source voltage V_{DS} was 1.5 V. The charge neutral point voltage (V_{CNP}) is 24 V. When V_G is less than V_{CNP}, the majority charge carriers within graphene are holes (h^+). When V_G is larger than V_{CNP}, the charge carrier type of graphene is electron (e^-).

We calculated the MFPL of our graphene sample using the Dirac curve in Figure V-3 (Castro 2009). The backscattering MFPL for the charge carriers in graphene was calculated to be 45 nm, corresponding to a collision time of 5×10^{-14} s. The MFPL was experimentally determined from the conductivity versus gate voltage measured in a region adjacent to the diode. The backscattering MFPL was obtained by multiplying the elastic MFPL by $\pi/2$, which is an averaging factor for scattering in two dimensions (Castro 2009). Because the backscattering MFPL is a closer approximation to the inelastic MFPL used in the Drude model than is the elastic MFPL, it is the number I have used in the simulation for fabricated devices (Zhu 2013).

2. Graphene geometric diodes measurement

At the start of the project, I used an HP HP4145B parameter analyzer to perform the four-point measurement described above. However, most devices were found to be electrically broken down to form an open circuit after the measurements, even when a mercury switch was used to short all contacts to the ground potential while the connections were made. After connecting the output of the parameter analyzer to an oscilloscope, a strange output waveform was observed, as shown in Figure V-4. When the output of the parameter analyzer was programmed to sweep from $-V_p$ to $+V_p$, the actual output would start from the 0-V idle state, sweep to $-V_p$, and then sweep to $+V_p$. Finally, when the parameter analyzer finished sweeping the voltage, instead of turning off the output (back to 0 V), it yielded a short-pulsed $-V_p$ output and then swept back to a 0 V output. Such a pulse gave a short electrical burst with a magnitude of $2V_p$ and damaged many devices.

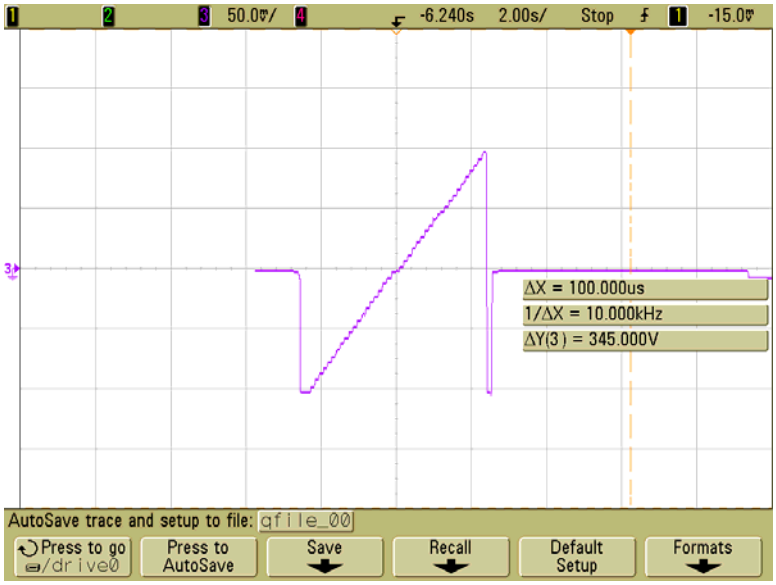


Figure V-4. The voltage output wave form of the HP4145B parameter analyzer sweeping from −0.1 V to 0.1 V.

Because of the abnormal behavior of the parameter analyzer, a Keithley 2612 Sourcemeter was used for the DC measurement of the geometric diodes. Figure V-5 shows the full setup of the four-point measurement using the Sourcemeter. Channel A of the Keithley 2612 Sourcemeter was used to provide and measure I_{DS}. By configuring the same channel of the Sourcemeter to be in a

"four-wire" mode, V_{DS} across the inner two contacts was simultaneously measured. In the gate-effect measurement, Channel B of the same Sourcemeter was used to apply the back gate voltage V_G to the silicon substrate. At room temperature and atmospheric-pressure environment, graphene electronic devices suffer from hysteresis effects (Joshi 2010). To achieve accurate *I(V)* characteristics of the geometric diodes, the applied DC voltage was pulsed with a pulse width of 26 μs and followed the pattern 0 V, $+V_1$, $-V_1$, $+V_2$, $-V_2$, …. $+V_{end}$, $-V_{end}$.

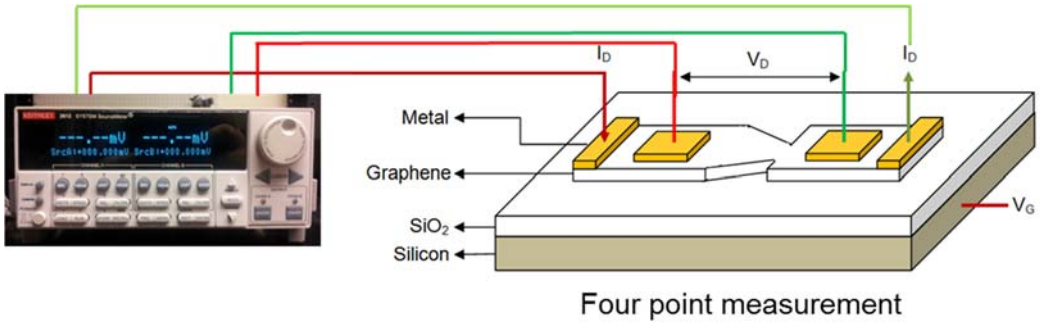


Figure V-5. Four-point probe measurement setup using a Keithley 2612 Sourcemeter. A pulsed voltage was applied to provide drain-source current (I_{DS}) through the outer two metal contacts. The actual voltage drop across the diode (V_{DS}) was measured between the inner metal contacts. A back gate voltage (V_G) was applied directly to the silicon substrate to control the carrier type and concentration in the graphene.

The graphene geometric diode shown in Figure IV-13 exhibited a nonlinear asymmetric *I(V)* relationship at V_G = 20 and 40 V, as shown in Figure V-6(a). The measured *I(V)* characteristics matched with the simulated diode *I(V)* behavior. To accurately simulate the *I(V)* behavior of the diode, the charge carrier concentration was calculated to be 1.1×10^{12} cm^{-2} at a gate voltage of 20 V.

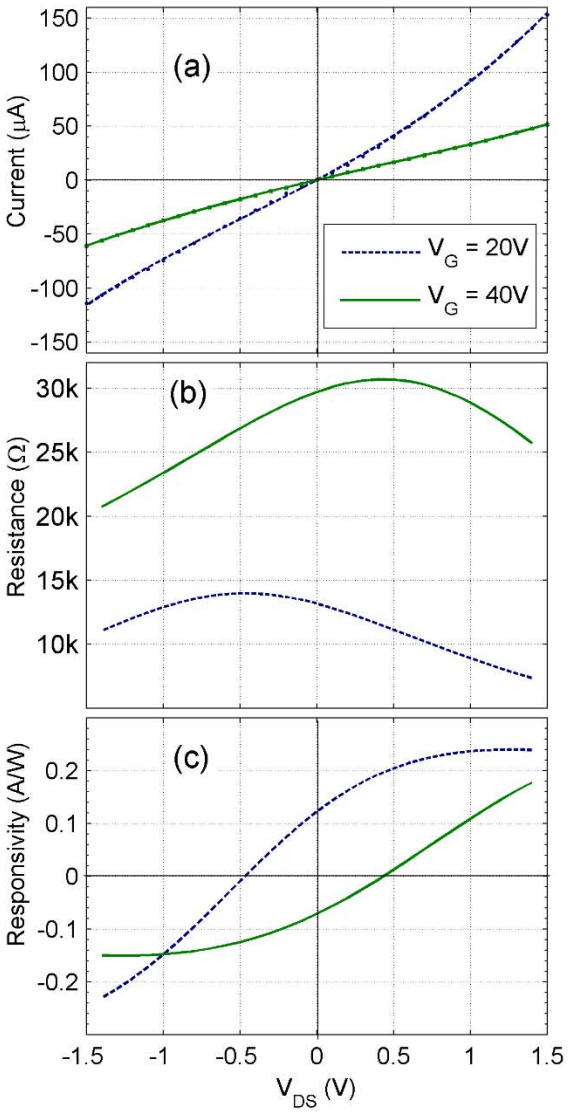


Figure V-6. (a) DC *I(V)* characteristics (solid blue) of an exfoliated graphene geometric diode at gate voltages of 20 V and 40 V. The measured mean-free path length = 45 nm; (b) Calculated differential resistance of using the *I(V)* data in (a); (c) Calculated responsivity [1/2 |*I''(V)/I'(V)*|] as a function of the applied drain-source bias. At 0 V bias, the responsivity is 0.12 A/W.

To better visualize the diode behavior, Figure V-6(b) shows the nonlinear differential resistance curves using the data from the *I(V)* curves shown in Figure V-6(a). A figure of merit for the diodes used in rectenna systems is the responsivity, which is defined as one-half of the ratio of the second derivative to the first derivative of the *I(V)* [1/2 × *I''(V)/I'(V)*]. Responsivity indicates how much DC current can be generated for a given AC input power. I show the calculated

responsivity curves in Figure V-6(c). For this diode, the responsivity at V_{DS} = 0 V and V_G = 20 V is 0.12 A/W, which is sufficient for IR and terahertz detection applications.

3. Geometric effect verification measurement

To verify the geometric effect, I also fabricated CVD graphene graphene geometric diodes and graphene symmetric junction devices. The diodes made from CVD graphene had approximately the same neck width as those made using exfoliated graphene. CVD graphene had a shorter MFPL compared with that of exfoliated graphene owing to the impurity doping during the CVD process and the small grain size of CVD graphene, as described in Chapter IV. In Figure V-7, I show that CVD graphene diodes have lower asymmetry *A* than the exfoliated devices. In addition, the symmetric junction devices showed no asymmetry in the *I(V)* behavior and *A* remains at one, as predicted.

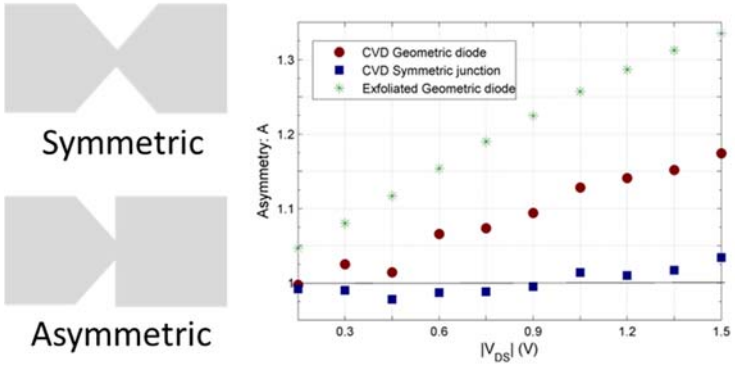


Figure V-7. Asymmetry A vs. drain source voltage $|V_{DS}|$ curves of exfoliated graphene diode (green stars), CVD graphene diode (red circles), and CVD graphene symmetric junction device (blue squares). CVD graphene has a shorter charge carrier mean-free path length (MFPL) than the exfoliated graphene. This causes the CVD graphene diode to have a lower asymmetry than the exfoliated graphene diode. CVD graphene symmetric junction device has no asymmetry (A = 1) in its electrical behavior.

A unique property of the graphene geometric diode is that its rectification polarity is reversible and can be controlled by the gate voltage (Moddel 2012). Owing to the conical band structure of graphene, the majority charge-carrier type and the carrier concentration can be controlled by changing V_G. In geometric diodes, the electrons and holes are both subject to the same geometric

effect and have the same forward current direction. Therefore, because of the opposite charges of the electrons and holes, the polarity of the diodes can be reversed by switching V_G from one side of V_{CNP} to the other. An indication of this behavior can be seen from the diode current–voltage characteristics measured at two gate voltages on opposite sides of the charge neutral point voltage (V_{CNP}), as shown in Figure V-6(a).

To clearly observe the reversal, I varied V_G from −40 to 40 V and measured I_{DS}, keeping V_{DS} constant. $A > 1$ means that the current flows more easily in the positive V_{DS} direction, whereas $A < 1$ indicates that the current flows more easily in the negative V_{DS} direction. Figure V-8 shows the A versus V_G plots for three different drain–source voltages of 0.5, 1, and 1.5 V. The reversal in the diode polarity can be clearly seen at the voltage where the asymmetry drops sharply, which corresponds to where V_G sweeps through V_{CNP}.

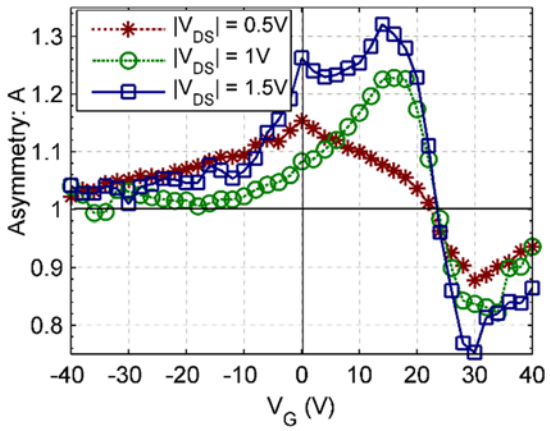


Figure V-8. Measured asymmetry (A = |I(V_{DS})/I(-V_{DS})|) as a function of the gate voltage (V_G) for the geometric diode in Figure V-6, at three different drain source voltages: $|V_{DS}|$ = 0.5 V, $|V_{DS}|$ = 1 V, and $|V_{DS}|$ = 1.5 V. Diode asymmetry increases with $|V_{DS}|$. The polarity of the diode switches as the V_G is varied from -40 V to 40 V, due to the change of the charge carrier type from holes to electrons near V_{CNP} (= 24 V). The diode asymmetry ratio reaches its maximum at V_G = 12 V and 32 V.

The plots in Figure V-8 are a confirmation of the geometric effect. Because the diode asymmetry is bias-voltage dependent, the relative magnitude of A increases with the increase in the magnitude of V_{DS}. This result agrees well with the simulation results presented in Chapter III.

Furthermore, by increasing the voltage difference between V_G and V_{CNP} ($|V_G - V_{CNP}|$), the charge carrier concentration n_s increases and provides a longer MFPL ($\propto \sqrt{n_s}$) (Nayfeh 2011), which increases the magnitude of A between V_G = 12 and 24 V and between 24 and 32 V. However, the diode asymmetry decreases as $|V_G - V_{CNP}|$ increases further because the current in the device starts to saturate (Dorgan 2010), and the transport of the charges can no longer be considered as ballistic. Such a current-saturation effect influences the *I(V)* characteristics, and A drops back to one.

C. Rectenna devices measurement at 28 THz

4. Optical response measurement setup

The optical measurement setup of the rectennas is shown in Figure V-9. A SYNRAD 48-1SWJ infrared CO_2 laser generated the 28-THz radiation. The power from the CO_2 laser was controlled by changing the pulse width from the pulse generator. We used a red He–Ne laser to assist in aligning the CO_2 laser to the device. A half-wave plate on the optical path rotated the laser polarization relative to the antenna axis. A Stanford Research Systems (SRS) chopper with 25 blades was used to mechanically chop the laser beam at 280 Hz. The same chopper produced a reference for the SR830 lock-in amplifier; thus, the lock-in amplifier was able to detect the modulated output current and voltage signal at the chopping frequency. Before and after every optical measurement, a mercury switch shorted the probes to the ground potential to avoid damage to the devices from electrostatic discharge. Two-point measurements were performed on the antenna-coupled diodes in air at room temperature.

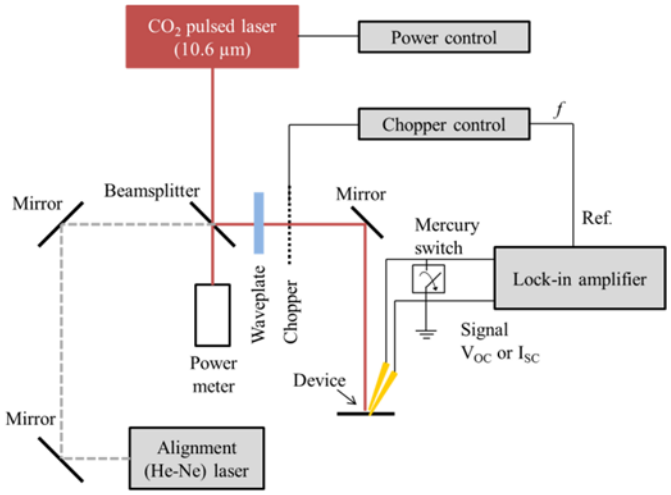


Figure V-9. Optical response measurement setup of the rectenna. We used a red He-Ne laser to align the CO_2 laser. A two-point probe setup was used for measuring the open circuit voltage and short circuit current. The lock-in amplifier used a 280 Hz signal from a chopper as the reference. To study the effect of changing the angle between the antenna axis and the incident wave polarization, a half-wave plate was used.

5. Optical response measurement of rectennas

The measured optical responses of the metal antenna/graphene-diode rectenna and the graphene antenna/graphene-diode rectenna are shown in Figures V-10 and V-11, respectively. Although the maximum responsivity occurs at $V_{DS} > 1$ V DC bias, as shown in Figure V-6(c), no external V_{DS} or V_G was needed during the optical measurements. Both rectified open-circuit voltage and short-circuit current shown in Figures V-10 and V-11 have cosine-squared dependence on the polarization angle, confirming that the optical response was due to the radiation coupled through the bowtie antenna. This angular dependence of the optical response indicated that the rectification was neither caused by diffusion of the optically generated charge carriers nor a result of the thermoelectric effects due to the non-uniform illumination of the diode. Additionally, no gate voltage was applied during the measurement, and we discharged the device to the ground through a mercury switch before the measurement. Therefore, no p-n junctions could have been formed as a result of any applied V_{DS} and V_G (Williams 2007).

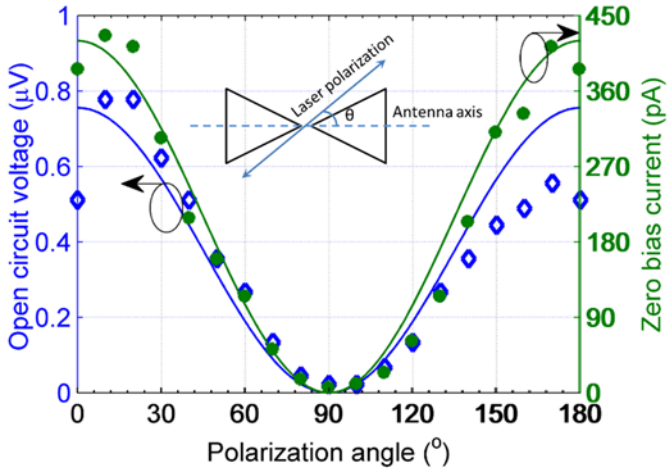


Figure V-10. Metal antenna / graphene diode rectenna short-circuit current (green circles) and open-circuit voltage (blue diamonds) as a function of polarization angle (θ).

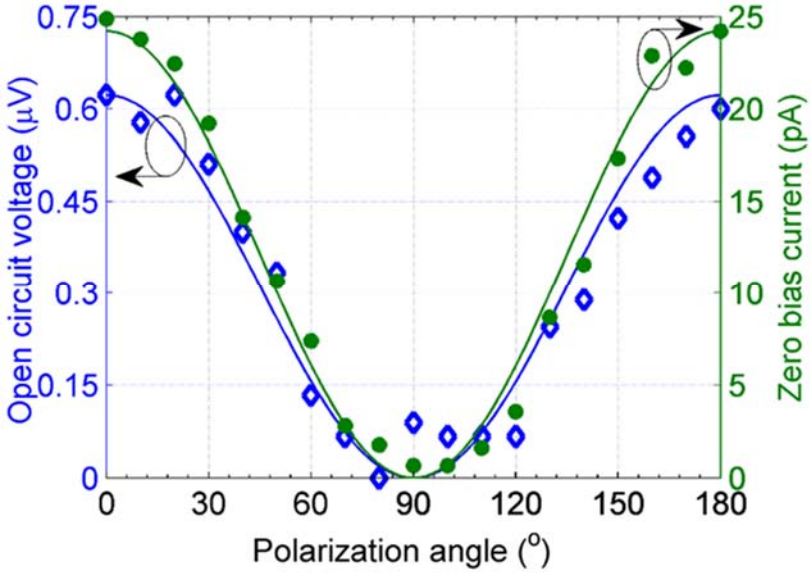


Figure V-11. Graphene antenna/graphene diode rectenna zero bias current (green circles) and open circuit voltage (blue diamonds) response at different polarization angles. The open circuit voltage response is close to the metal antenna / graphene diode rectenna. The lower current response in the graphene rectenna is due to a larger graphene antenna series resistance than the metal antenna.

By comparing Figures V-10 and V-11, we found that the open-circuit voltage response of our graphene rectenna device was similar to that of the graphene diode/metal-antenna rectenna. However, the short-circuit current response of the graphene rectennas was significantly lower

owing to the large DC series resistance (~1 kΩ) of the graphene antenna compared with the few ohms of the metal antenna. More discussion on the optical measurement results will be shown in chapter 6.

6. Verification measurement for rectenna optical response

To confirm that our metal bowtie antenna resonance at 28 THz, the antenna near-field measurement was performed using the scanning near-field optical microscopy (snom) method. The achieved z-direction near-field pattern in Figure V-12 clearly shows the antenna resonance response at 28 THz and matches that of the other similar antennas (Olmon 2008). The near field in the z-direction above the two arms of the bowtie antenna was symmetrically 180º out of phase along the vertical y-axis. This near-field measurement was carried out in Markus Raschke's group at University of Colorado at Boulder.

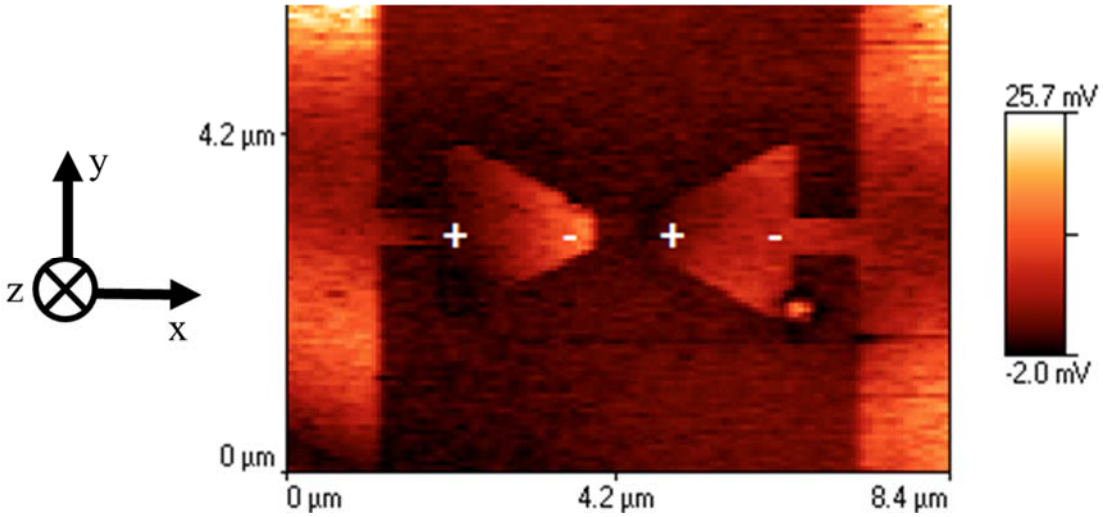


Figure V-12. A z-direction near field pattern of our metal bowtie antenna. The scale bar shows the arbitrary magnitude of the near field in the z-direction.

Two additional measurements were performed to confirm that the rectenna responds at 28 THz. First, we illuminated the graphene geometric diodes without the coupled antennas. As expected, the diodes without antennas did not show any optical response, which indicates that the

optical response shown in Figures V-10 and V-11 was not caused by in-situ p-n doping in the graphene (Williams 2007). Second, as shown in Figure V-13, the amplitude of the on-axis polarization ($\theta = 0°$) response increased as the incident radiation intensity increased. In contrast, for the misaligned case ($\theta = 90°$), the detector output remained at the noise voltage level regardless of the change in the laser intensity. In addition, the partially aligned detector ($\theta = 45°$) showed an optical response proportional to the laser power, but the magnitude of the response was lower than that of the fully aligned detector. The estimation of the laser power is based on the assumption that the device is 1 mm misaligned to the center of the laser beam. Thus, the graphene geometric diode genuinely rectified the 28-THz signal absorbed by the antenna.

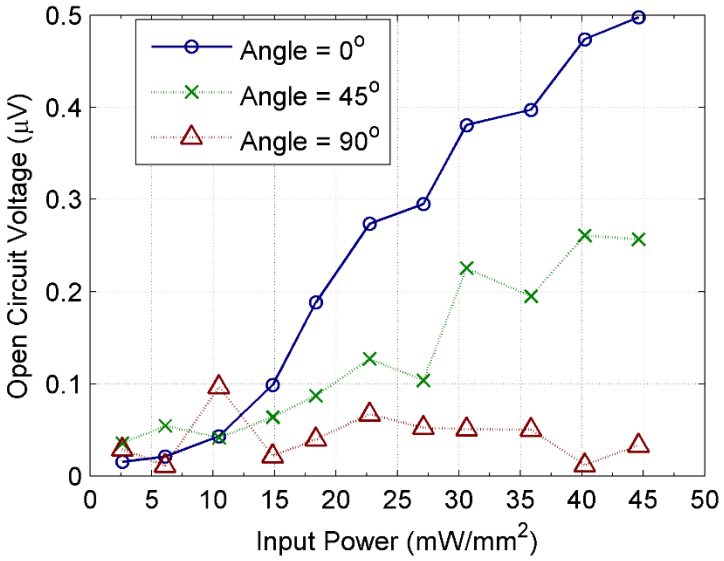


Figure V-13. Open circuit voltage versus laser input intensity at three polarization angles: 0°, 45° and 90°. The response at 0° (blue circles) indicates perfect alignment between the laser polarization and the antenna, which gives the strongest open circuit voltage signal. At 90° (green crosses), the antenna is perpendicular to the laser polarization and gives a near zero output voltage at all input intensities.

CHAPTER VI

DISCUSSION

A. Frequency limitation

To operate at terahertz and higher frequencies, the diodes in the terahertz rectenna system must be intrinsically fast and have an extremely low RC time constant. An additional requirement for harvesting energy using rectennas is that the diode impedance must also match the antenna impedance for efficient power coupling between the antenna and the diode (Grover and Moddel 2011).

1. The intrinsic speed of geometric diodes

The intrinsic device speed is ultimately limited to the frequency response of the material and the device substrate. Graphene is ideally suited to terahertz electronics because of its high carrier mobility at room temperature and frequency-independent absorption (Nair 2008). Furthermore, high-quality graphene samples support weakly damped plasma waves (Liu 2008), (Bostwick 2010). The surface plasmon frequency is gate-tunable (Jablan 2009) up to the graphene optical phonon frequency of 48.3 THz, corresponding to an energy of 0.2 eV (Park 2008). At operating frequencies exceeding 176 THz, corresponding to a wavelength of 1.7 μm, the performance of graphene devices is affected by inter-band loss (Jablan 2009).

2. The RC time constant of geometric diodes

The small RC time constant for the diodes used in rectennas is realized by extremely low capacitance of the graphene geometric diodes. The capacitance of the planar geometric diodes results from the fringing electric fields (E-fields) between both sides of the reverse arrowhead structure. As shown in Figures VI-1 and VI-2, the fringing E-fields are established in the air above the device, between the two planar side walls, and in the 90 nm SiO_2

bottom substrate below the devices. An air gap of approximately 100 nm × 100 nm is assumed in the neck region of the geometric diode (see Figure VI-2).

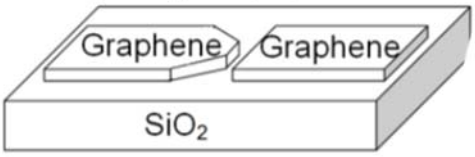


Figure VI-1. 3D model of a graphene geometric diode. For the calculation of the device capacitance, I assume that there is a 100 nm × 100 nm air gap at the neck region of the geometric diode.

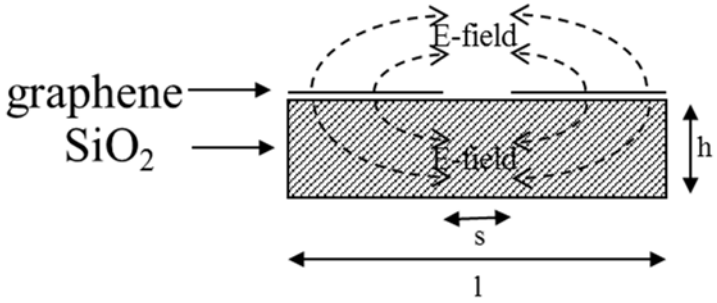


Figure VI-2. Cross section of a graphene geometric diode. The gap width (*s*) at the neck region is assumed to be 100 nm. The total length (*l*) of the device is assumed to be 1.5 μm. The thickness (*h*) of the substrate SiO_2 layer is 90 nm. The fringing electrical fields (E-fields) storing the charges exists in the air above the device and in the SiO_2 substrate.

By planar thin film capacitance analysis (Vendik 1999), the capacitance of the graphene geometric diode can be calculated using Eq. VI-1, assuming the device total length (l) is much longer than the air gap width (s) as shown in Figure VI-2.

$$C = \frac{w\varepsilon_0(\varepsilon_1 - \varepsilon_2)}{\frac{s}{h} + \frac{4}{\pi} ln2}$$

Eq. VI-1

where ε_1 is the dielectric constant of graphene; ε_2 is the dielectric constant of SiO_2; s is the air gap width; w is the width of the geometric diode; and h is the thickness of the SiO_2 substrate.

Due the arrowhead shape of the geometric diodes, I integrated the device capacitance through the width from 0 to 450 nm as shown in Eq. VI-2.

$$C = 2 \times \int_0^{450\,nm} \frac{\varepsilon_0(\varepsilon_1 - \varepsilon_2)}{\frac{s}{h} + \frac{4}{\pi} ln2} dw$$

Eq. VI-2

The dielectric constant is 3.9 for SiO_2 and 2.5 for graphene (Chen and Appenzeller 2008). The capacitance of the graphene geometric diode was calculated to be 3.6 aF. In general, the capacitance of geometric diodes is on the order of a few attofarads.

The overall RC time constant of the device is the product of the estimated device capacitance and the measured resistance. The measured resistance of the graphene geometric diodes is approximately 1 kΩ. Thus, the RC time constant of the diodes is on the order of femtoseconds, corresponding to a cutoff frequency of 100 THz. The estimation of the device capacitance used the worst case assumption, which assumed that the device was disconnected at the neck. The actual RC cutoff frequency could be higher than 100 THz. Besides, by reducing the area of the non-critical region around the neck, the RC time constant can be further reduced.

B. Simulated versus measured results

1. Simulated DC *I(V)* versus measured DC *I(V)*

In chapter V, I show the measured *I(V)* curves of graphene geometric diodes. I have also simulated the fabricated diode using the measured device parameters: MFPL = 45 nm, charge concentration = 1.1×10^{12} cm^{-2}, neck width = 75 nm, shoulder width = 400 nm and the arrowhead slope = 45º. As shown in Figure VI-3, the simulated *I(V)* characteristic and the measured *I(V)* characteristic at DC match well with each other for the device in Figure IV-13. No other adjustable parameters were used for this simulation.

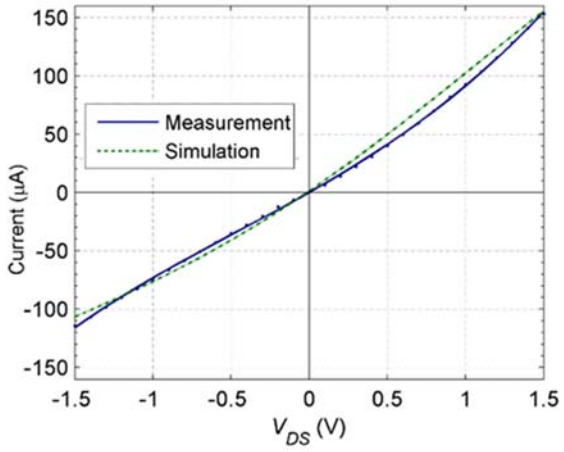


Figure VI-3. DC *I(V)* characteristics (solid blue) of an exfoliated graphene geometric diode at a gate voltage of 20 V. The Monte Carlo simulation (dashed green) uses the dimensions of the fabricated device: neck width = 75 nm, shoulder width = 400 nm, and the measured mean-free path length = 45 nm.

2. Estimation of output current for rectennas

To confirm that the measured results at 28 THz are also consistent with our model of the device operation, I estimated the output signal of the rectennas on the basis of the measured DC *I(V)* behavior of the geometric diode. When the rectenna axis was aligned with the laser polarization, the measured short-circuit current output of the rectenna was 420 pA as shown in Figure V-10. In calculating the expected short-circuit current, the following system parameters are

required: measured laser intensity (P_{in}), reported antenna absorption efficiency (η_a), measured diode responsivity (β_d), and calculated rectenna coupling efficiency (η_c). Using a Scientech Astral AC25FXS power meter, we measured the illumination intensity (P_{in}) as 68 mW/mm^2 at the center of the laser. The laser has a Gaussian distribution power profile. The alignment tolerance of our device to the center of the beam is ~ 2 mm. The P_{in} is 49 mW/mm^2 and 25 mW/mm^2 at the locations 1 mm and 2 mm, respectively, away from the beam center. The effective area (A_{eff}) of a 28 THz metal bowtie antenna with the same configuration was reported as 37.5 μm^2. The measured antenna absorption efficiency was reported to be 37% (González and Boreman 2005). The antenna impedance (R_a) is assumed to be 100 Ω, typical for an antenna operating at terahertz frequencies (Kocakarin and Yegin 2013). For the diode in Figure IV-16 used for the optical response measurement, I measured its DC *I(V)* behavior and calculated its responsivity as 0.0285 A/W at zero bias. Based on the *I(V)* data, the calculated diode resistance (R_d) was ~3000 Ω. As mentioned in section A of this chapter, the diode capacitance (C_d) was calculated to be ~10^{-18} F. The rectenna coupling efficiency can be calculated using the impedance matching model (Grover and Moddel 2011) and Eq. VI-3.

$$\eta_c = \frac{4\dfrac{R_a R_d}{(R_a + R_d)^2}}{1 + \left(\omega \dfrac{R_a R_d}{(R_a + R_d)} C_d\right)^2}$$

Eq. VI-3

where ω is the radiation frequency, equal to 2π × 28 THz. The rectenna coupling efficiency was calculated as 12%.

Inserting all of the above parameters into Eq. IV-4, the current in the metal antenna/graphene geometric diode rectenna can be estimated.

$$I_{est} = P_{in} A_{eff} \eta_a \beta_d \eta_c.$$

Eq. VI-4

The estimated output current is 3.7 nA at the center of the beam and 2.6 nA and 1.3 nA 1 mm and 2 mm, respectively, away from the beam center. The measured short circuit current is ~ 0.42 nA. The estimated and measured current output are off by a factor between three and nine. Many factors could cause this. One is that the 37 % antenna optical efficiency was measured for the antennas without load and any metal contact leads. In our rectenna devices, the actual antenna optical absorption efficiency could be much lower than the reported value. The second unknown factor is the actual antenna impedance, which has a large impact on the system coupling efficiency. In the current output estimation calculation, the antenna impedance was assumed to be 100 Ω. More measurement is required to verify the antenna impedance at 28 THz.

CHAPTER VII

RECTENNAS USING METAL-INSULATOR-METAL DIODES

A. Metal-insulator-metal diodes

Rectennas using Metal-Insulator-Metal (MIM) diodes provide an alternative approach for radiation detection, especially at terahertz frequencies (Eliasson 2001), (Grover 2011). These diodes operate on the principle of electron tunneling through an insulator (Heiblum 1978). Electron tunneling through thin insulators is an inherently fast process, occurring in less than a femtosecond. Such high-speed operation makes MIM diodes attractive for operation at terahertz frequencies. Since electron tunneling is a nonlinear process, these diodes have current–voltage characteristics that are nonlinear. A fast response with nonlinearity in the *I(V)* characteristics allows for rectification of high-frequency AC signals into DC. The DC current is directly proportional to the AC input power, with the diode responsivity as the proportionality factor.

Although conventional lumped element MIM diodes are fundamentally limited in performance by their RC time constant at 28 THz, room temperature rectennas using MIM diodes can achieve high detectivity at 1 THz (Grover and Moddel 2011). A resistance-matched Ni-NiO-Ni MIM diode in a rectenna (100 Ω at 0.33 V with 0.74 mA bias) (Joshi 2013) has a coupling efficiency of 77% and a system responsivity of 5.2 A/W. The Ni-NiO-Ni diode has a NiO layer ~2 nm thick with a diode edge length of 400 nm for impedance matching with the antenna. The relative permittivity of NiO is ~6.5 at 1 THz (Thacker 2013). The calculated diode capacitance is ~4 fF. Simulated curves for current density (*J*) and responsivity vs. applied bias voltage are shown in Figure VII-1.

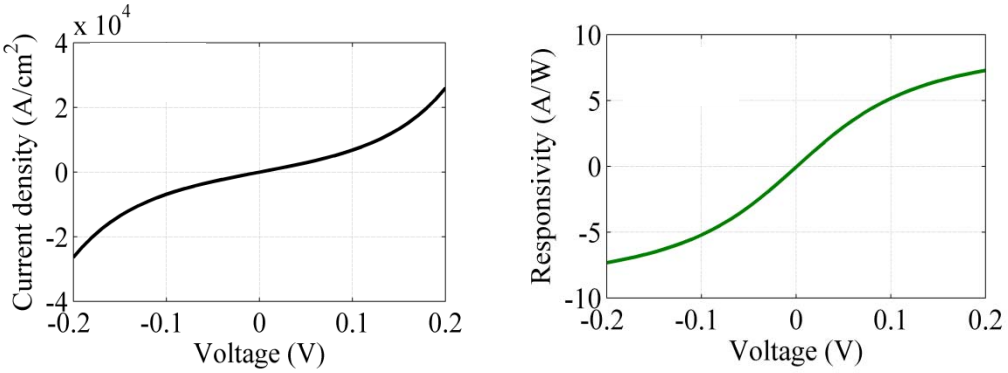


Figure VII-1. (a) Simulated diode tunneling current density vs. applied bias voltage [*J(V)*]. The oxide thickness is 2 nm; barrier height is 0.2 eV. (b) Calculated diode responsivity vs. applied bias voltage for the simulated *J(V)* shown in (a). This simulation work was carried by Saumil Joshi in our group.

The MIM diode materials and structure were chosen to meet the requirements for overall system efficiency, as described in chapter 6. As described above, Ni was chosen as the material for the top and bottom metal layers in the MIM diodes. The ideal method to fabricate MIM diodes is to first grow the Ni-NiO-Ni stack together and then to etch the stack into the devices with different areas. This method will prevent the non-uniform oxidation of Ni at the edges of the devices and will produce devices with consistent quality. However, Ni cannot be etched using the conventional reactive ion etch (RIE) method. Therefore, I used an overlap process to fabricate MIM diodes. The process was: patterning and liftoff bottom layer Ni, growing NiO, and patterning and liftoff top layer Ni.

For our purposes, liftoff of the bottom Ni layer required a bilayer photoresist structure (AZ 4210 resist or deep ultraviolet (DUV) resist UV6-0.7 as the top layer and SF5 resist as the bottom layer) to provide an undercut so that deposited material does not adhere to the vertical edges of the photoresist pattern, which would otherwise lead to undesirable structures at the pattern edges. The cross-section of the bilayer resist after development is shown in Figure VII-2. Using this method and DUV lithography, 150-nm lines with clean edges could be fabricated. The DUV lithography process was done using an ASML 300/5500 stepper in the University of California at Santa Barbara (UCSB) nanofabrication facility.

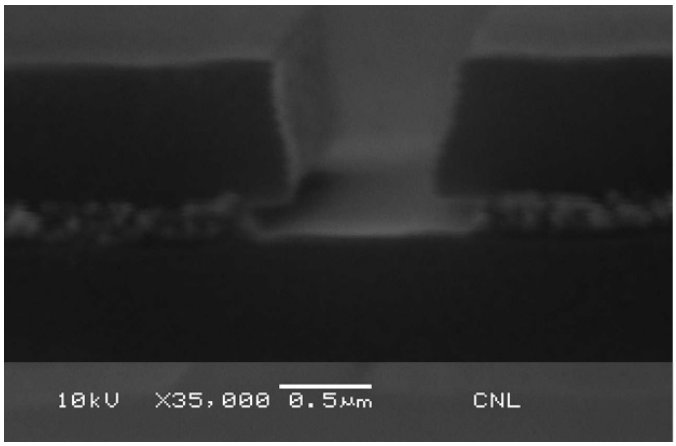


Figure VII-2. Scanning electron microscope (SEM) illustrating the bilayer liftoff stencil. The bottom layer resist is 150 nm thick SF5. The top layer resist is ~1 µm thick AZ 4210 positive resist. The line width of the top layer is approximately 500 nm. The width of the undercut region in the bottom layer is ~150 nm. The substrate is a silicon wafer with a 300 nm thermally grown SiO_2 layer on top.

As for the insulator layer, it is difficult to grow a controlled 2-nm-thick NiO layer with conventional thermal oxidation; therefore, I used the oxygen plasma method to consistently grow thin NiO layers. The oxygen plasma was generated in the ISE sputtering system without any target. The RF power of the O_2 plasma was 30 W at a pressure of 50 mTorr.

A disadvantage of the overlap process is that to prevent additional growth of NiO, the O_2 plasma descum cleaning process cannot be performed before the deposition of the top layer Ni. I found that using the PMMA resist would leave an ultra-thin resist residue after development, but SF5 resist would provide a clean surface after being removed in the MIF AZ300 developer. This was verified by the measurement of devices with 0 nm thick NiO. The resistance of such shorted Ni-NiO-Ni diodes with areas > 250 × 250 nm^2 is negligible.

B. 1 THz rectennas using Metal-insulator-metal diodes

The design and fabrication processes used for rectennas working at 1 THz were guided by the requirements for the diode and antenna. The antenna requires a low-loss metal at terahertz frequencies. Gold was used for its high conductivity and surface and bulk stability. The gold

bowtie antenna consisted of two 49-μm-long triangular arms with 2 μm gap in the center. The overlapped MIM diode was places in the center gap of the antenna. The whole rectenna system was fabricated on high resistivity (>2,000 Ω-cm) silicon wafers with thermally grown oxides of thickness ~300 nm. Figure VIII-3 and Figure VIII-4 show the CAD design and optical microscope images of a fabricated rectenna device with MIM diodes in the lumped element configuration.

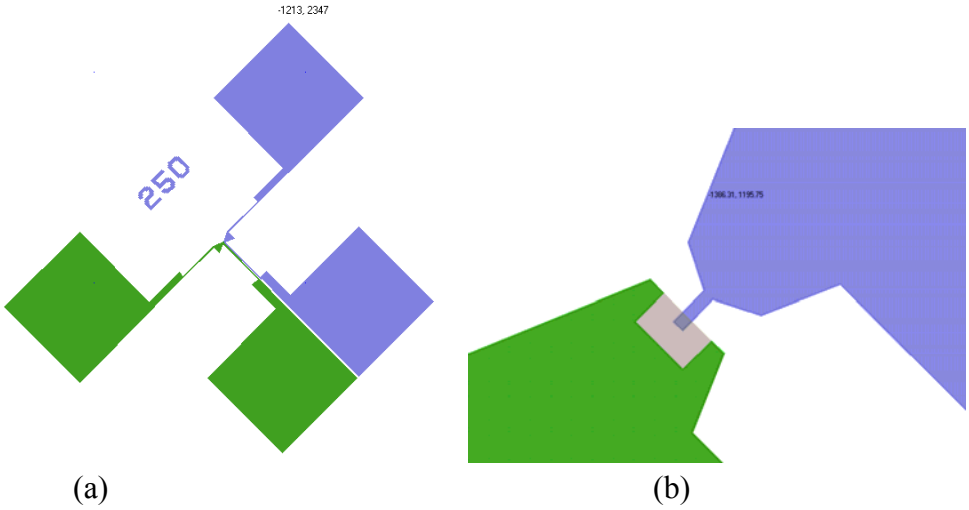
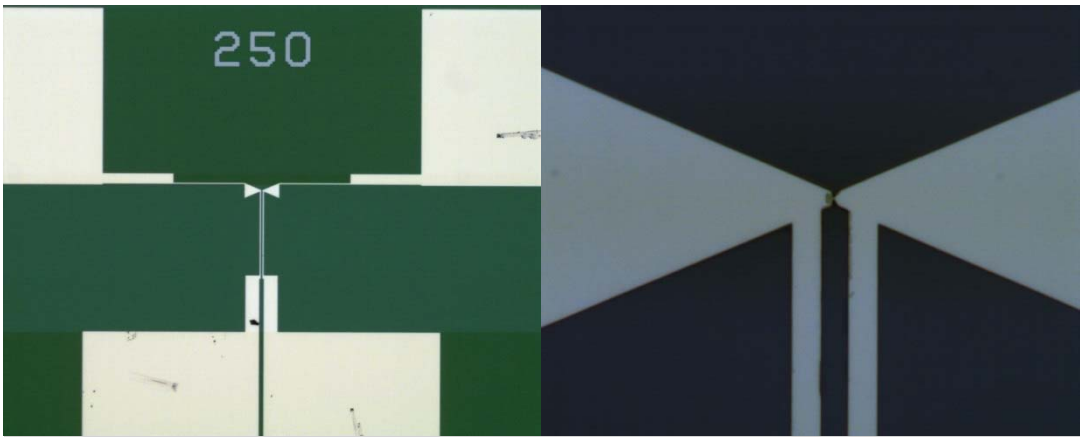


Figure VII-3. (a) Layout of the rectenna including the test pads. The antenna, composed of two triangles, is near the center. The different colors represent the layers of the device. (b) The center region at the apexes of the triangles. The gray rectangle is the first Ni layer, and the green area is the first Ni layer covered with the second Ni/Au layer. The purple area is the second Ni/Au layer. The overlap of the purple layer and the gray layer forms the MIM diode. For this pattern, the area of the MIM is nominally 250 nm × 250 nm.



(a) (b)

Figure VII-4. Optical microscope images of the devices after fabrication and DC testing were complete. (a) Antenna and the probe test pads. (b) Center portion of the antenna and the overlap region forming the diode.

The fabricated diodes were tested for DC *I(V)* characteristics using a four-point probe method. The measurement setup, as shown in Figure VII-5, is similar to the one used for measuring geometric diodes. Current was applied between the two outer electrodes (high and low), and the voltage was measured between the two inner electrodes (sense high and sense low). The DC *I(V)* curve for one such diode (diode edge length = 400 nm) is shown in Figure VII-6. From the *I(V)* data, the barrier height of the Ni-NiO interface was calculated to be close to 0.1 eV. The barrier height was determined by adjusting the its value in the simulator to match the simulated *I(V)* characteristics with the measured *I(V)* characteristics (Joshi 2013). We have fabricated diodes with diode responsivity in the range of 1.5–3 A/W for small area diodes (250 nm × 250 nm to 500 nm × 500 nm) with diode resistance in the range of 50–300 Ω. As shown in Figure VII-7, the MIM diode in Figure VII-6 has a responsivity up to 2.3 A/W at a bias voltage of 0.08V.

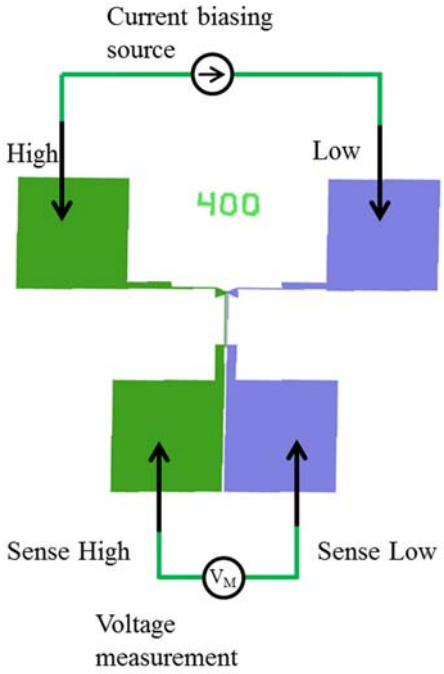


Figure VII-5. Setup used for diode DC current-voltage measurements. The setup consists of a current source and a voltage measurement unit. The probes connected to the device contact pads are labeled *High*, *Low*, *Sense High*, and *Sense Low*. Current is applied between the *High* and *Low* probes. Voltage drop across the diode is measured between the *Sense High* and *Sense Low* probes using a voltage meter.

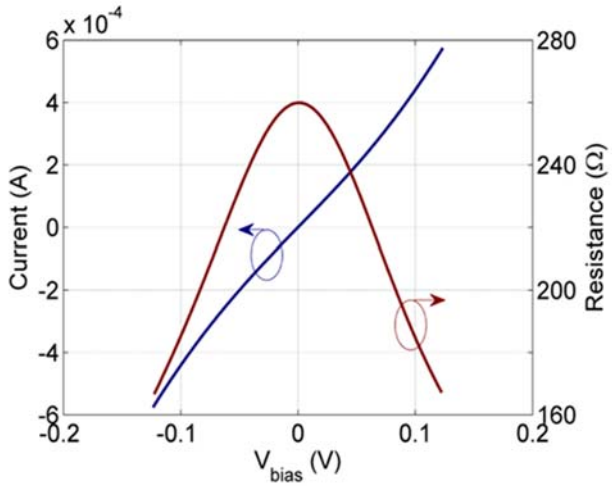


Figure VII-6. Measured DC *I(V)* and resistance vs. bias voltage characteristics of a diode with an area of 250 nm × 250 nm. These DC *I(V)* measurement results were carried out by Saumil Joshi in our group and myself.

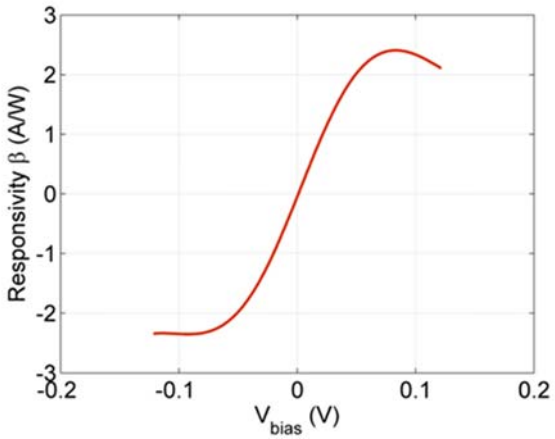


Figure VII-7. The calculated diode responsivity is ~ 2.3 A/W at a bias voltage of 0.08 V for the device in Figure VII-6. These DC *I(V)*measurement results were carried out by Saumil Joshi in our group and myself.

Modified THz-time domain spectroscopy (THz-TDS) (Tomasino 2013), (Skjeie 2012) was employed to verify the performance of the 1 THz rectenna devices. The setup, as shown in Figure VII-8, was built at the University of Missouri (MU). In conventional THz-TDS, a femtosecond optical laser is split via a beam splitter into individual pump and probe beams. Both of these beams are linearly polarized and temporally separated using a time delay. The pump beam creates a THz pulse via a photoconductive antenna (PCA), while the probe beam is used to measure the THz pulse via the Pockel's effect in a nonlinear crystal of zinc telluride (ZnTe). The THz pump pulse is optically focused onto a plane where a specimen of interest is mounted vertically.

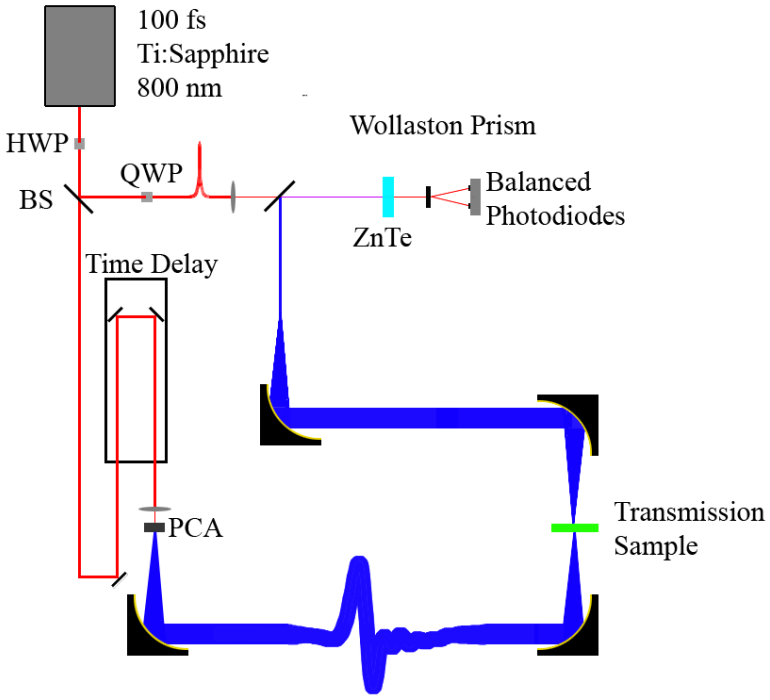


Figure VII-8. Traditional THz-TDS optical arrangement where the sample is mounted vertically.

In the MU modified THz-TDS system, the optics are arranged so that the THz beam propagates vertically, while the sample is mounted horizontally within a translatable x-y-z manipulator. This configuration serves two purposes: First, it allows us to mount a camera and focus the center spot from a He–Ne laser, so we can insert 4-point probes onto individual rectenna devices to measure electrical response in the plane of the most intense THz illumination. Second, the x-y-z manipulator makes it possible to image specimens both spatially and spectrally.

The signal from the rectenna is recorded first when the beam is blocked to provide a suitable noise floor; subsequently, the beam block is removed to measure the true response. Several iterations of blocking/unblocking are required to account for any bolometric (i.e., heating) effects and to determine device hysteresis and degradation. For a typical good device, we observe a rectenna current of 8.5 nA with a terahertz illumination of 19.1 nW absorbed by the antenna. This corresponds to a system responsivity of 0.44 A/W.

C. Improvement in MIM diode fabrication process

The MIM rectennas with a 2-nm-thick NiO layer, fabricated using the overlapping fabrication process, demonstrated an optical response at 1 THz. However, the resistances of the MIM diodes with small area and thin NiO layer were not consistent, while the resistance of Ni–NiO–Ni diodes fabricated with a 4- to 7-nm-thick NiO layer showed consistency among devices and scaled with the area of the diode. Owing to the large variation in the resistance for small MIM diodes, determining whether or not the diode resistance scales up with the diode area was difficult. The most likely reason for the observed inconsistency is the nonuniform oxidization of the surface and the edge leakage conduction of the overlapped devices.

I have developed a new fabrication process using the "via hole" process, which is expected to prevent the possible diode edge conduction. The first two steps for this process are similar to that of the overlapping process. A bottom Ni/Au layer of thickness 10 nm/30 nm was patterned using DUV lithography and deposited by thermal evaporation. Subsequently, a metal lift-off process was performed at 60 ºC for 1 hr using a resist remover 1165. Then, the stack 30-nm-thick Ni/2-nm-thick NiO/30-nm-thick Ni/10-nm-thick Au layer was patterned and lifted off to define the active diode area. The 2-nm-thick NiO layer was also grown by oxidizing the wafer in presence of O_2 plasma. Next, a SiO_2 layer of thickness 80 nm was grown using the plasma-enhanced chemical vapor deposition (PECVD) method. Following that, DUV lithography and reactive-ion etching process were performed to pattern and form via holes on top of the diodes. Lastly, a 10-nm-thick Ni/80-nm-thick Au wiring layer was defined by the DUV lithography and metal lift-off process. To ensure the absence of resist residue, O_2 plasma descum at 100 W and 300 mTorr was performed for 2 min after each DUV lithography step. Figure VII-9 presents the fabricated MIM diode with a patterned contact via hole. Figure VII-10 illustrates the cross-sectional schematic of the device presented in Figure VII-9.

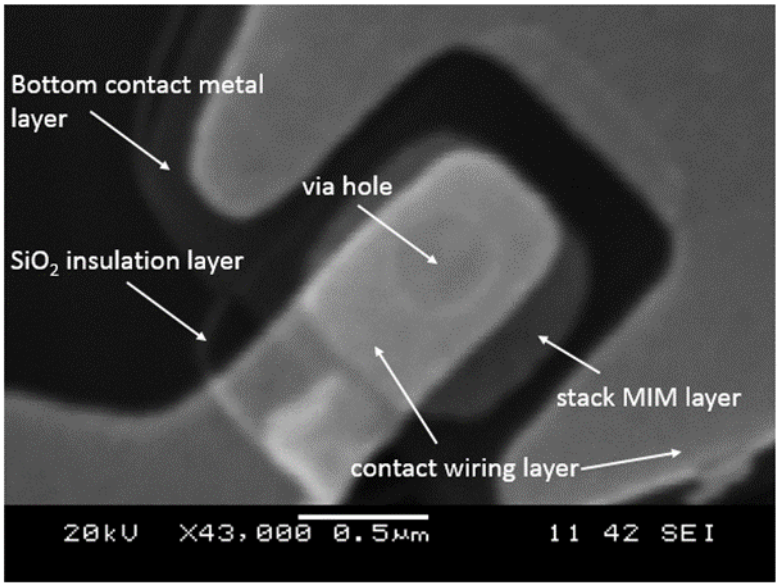


Figure VII-9. Scanning electron microscope (SEM) image of MIM diode fabricated using the via hole process.

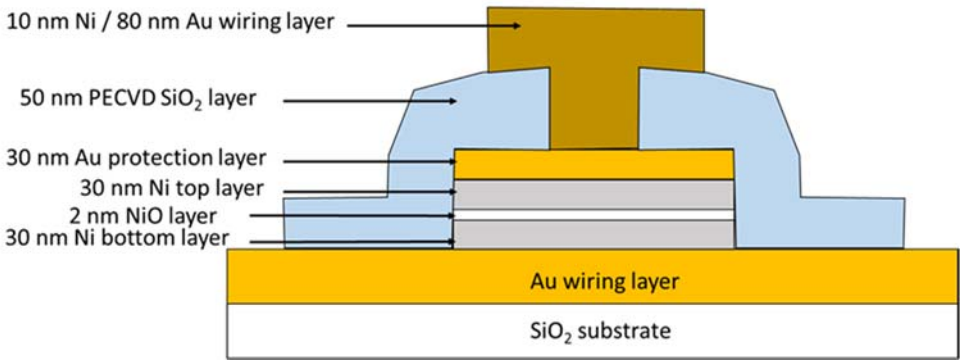


Figure VII-10. A cross-sectional image of the MIM diode fabricated using the via hole process.

The via hole fabrication process is still at its early development stage. Initial electrical measurement results show great improvement in the consistency of the diode resistance. The variation between the diodes within the same group has been reduced from 1-3 orders of the magnitude down to only about ±10% to ±30%. The edge conduction is eliminated by using the via hole process for two reasons. One reason is that the top Ni layer contacts the bottom Ni layer only on its surface. The second reason is that the PECVE SiO_2 via layer around the edges of the top Ni layer blocks the wiring Au layer to form any type of edge conduction to the bottom MIM structure.

CHAPTER VIII

FUTURE IMPROVEMENT

A. Methods to improve the rectenna performance

The detector performance of our geometric diode rectenna can be improved in at least five ways. The simplest way is to apply V_{DS} to maximize the diode *I(V)* asymmetry, which alters the diode operating point (Moddel 2012). Both simulation and measured results indicate that the geometric effect increases as V_{DS} increases from zero. As shown in Figure V-8, the diode asymmetry is higher at V_{DS} = 1.5 V than at V_{DS} = 1 V and 0.5 V. The same drain–source voltage effect is observed in Figure V-6(c), where applying V_{DS} doubles the β_d from 0.12 A/W at zero bias to ~0.24 A/W at 1 V bias. However, increasing V_{DS} also increases the shot noise. For the diode in Figure V-10, the rectenna D* first improves as V_{DS} is applied and degrades at higher V_{DS}. Thus, for this geometric diode in the rectenna, V_{DS} between 0.1 V and 0.3 V yields the optimal detection performance.

Increasing the voltage difference ($|V_G - V_{CNP}|$) between V_G and the charge neutral point voltage V_{CNP} also induces greater geometric effects (Moddel 2012). As discussed in chapter 5, when the charge transport within graphene is still considered as ballistic (low $|V_G - V_{CNP}|$), the *I(V)* asymmetry of the graphene geometric diode increases when V_G shifts from 24 V to 12 V, and also from 24 V to 32 V. Thus, without physically modifying the device, we can increase the asymmetry by a factor of 2 to 5 by varying V_{DS} and V_G.

Third, the diode responsivity may be increased by changing the geometric shape of the diodes. In the next section of this chapter, I will introduce a novel geometric diode, termed as the Z-shaped diode, which produces an *I(V)* response that is much more asymmetric than that of the inverse-arrowhead-shaped diode.

Alternatively, the rectenna detection performance may be improved by raising the quality of the graphene and hence the charge MFPL. This can be achieved by improving both the fabrication

process and the purity of the graphene (Fan 2011). The quality of exfoliated graphene can improved by using a lattice matched boron nitride (BN) substrate (Liu 2013), (Levendorf 2012). It is very challenging to prepare large area single crystal BN substrates. In fact, similar to the method I used to prepare graphene flakes, the exfoliation method is the best way to create single crystal BN flakes. The throughput of successfully exfoliated BN flakes is low. The chance of achieving a usable graphene piece on BN will be even lower. As a result, better process to prepare large area BN substrate is appreciated.

Finally, the performance of the whole rectenna can be improved by optimizing the antenna design. I selected the simplest bowtie antenna for its ease of fabrication and polarization-selective absorption efficiency. Many more efficient antenna designs, such as log periodic antennas, have been reported in the literature (González and Boreman 2005).

B. Z-shape geometric diodes

Unlike the inverse arrowhead diode, the abovementioned Z-shape geometric diode (see Figure VIII-1) uses the electric field in the y-direction to achieve high $I(V)$ asymmetry. The simulation result of this device is shown in Figure VIII-2 and Figure VIII-3. The $I(V)$ characteristics of the Z-shape diode is more nonlinear compared to that of the inverse arrowhead diode with the same neck and shoulder widths.

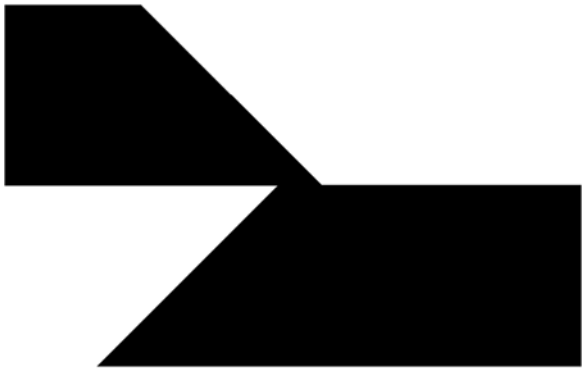


Figure VIII-1. Schematic of a Z-shape geometric diode.

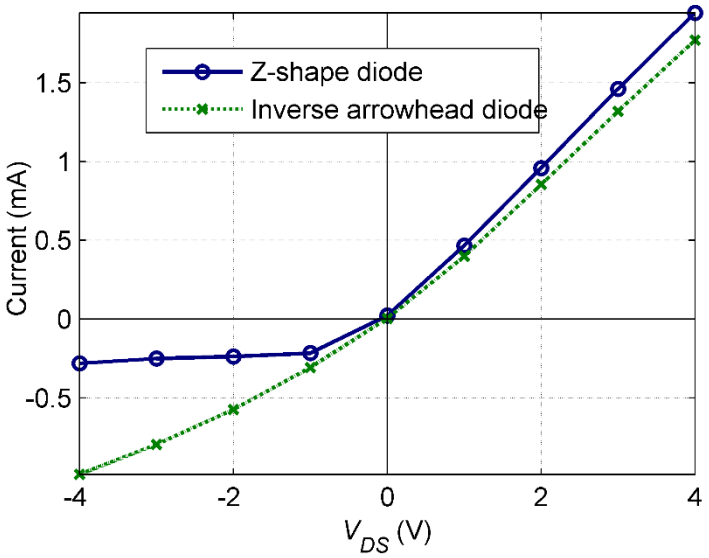


Figure VIII-2. Simulated *I(V)* characteristics of the Z-shape diode and the inverse arrowhead diode. The neck width of the two diodes is 250 nm. The MFPL of graphene used in the simulations is 200 nm.

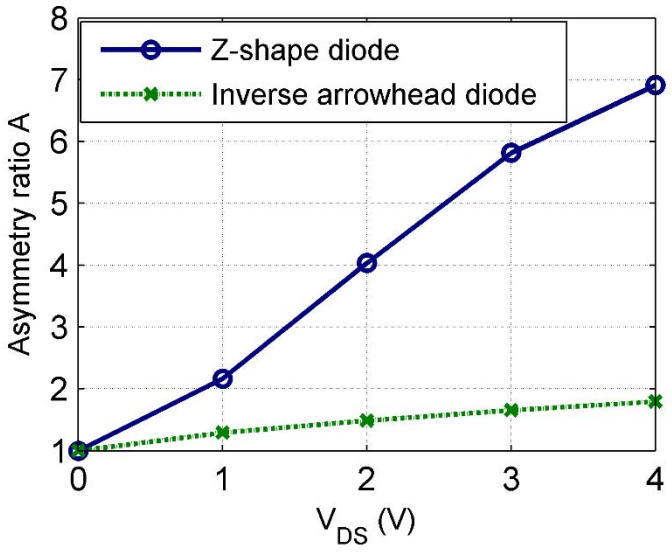


Figure VIII-3. Calculated asymmetry ratio curve of the Z-shape diode and the inverse arrowhead diode using the data in Figure VIII-2. With same neck width and MFPL, Z-shape geometric diode is capable of achieving much higher asymmetry than the inverse arrowhead diode.

As described in chapter 3, the full-version simulator uses real E-field maps of geometric diodes and has the capability to simulate the impact from the charge build-up effect on the diode *I(V)* characteristics by including the charge-charge interactions. Figure VIII-4 shows the 2D voltage potential map of the Z-shape diode. Figures VIII-5 shows the x-direction E-field map of the Z-shape diode derived from the potential map in Figure VIII-4. Compared to the E-field map of the arrowhead diode in Figure III-7, as expected, the E-field is much less uniform within the Z-shape diode, because of its much greater geometry asymmetry.

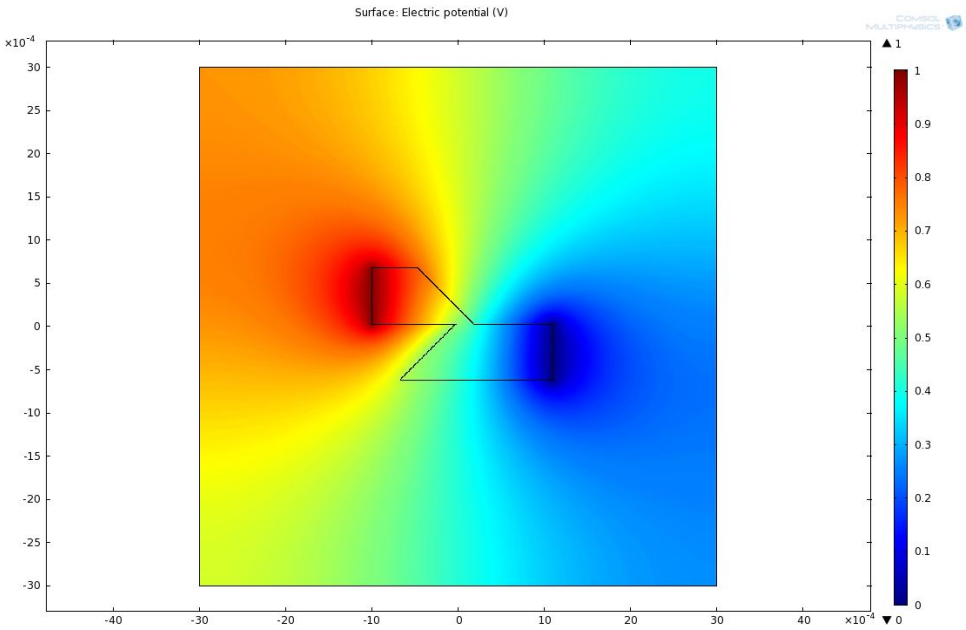


Figure VIII-4. Simulated voltage potential map within the Z-shape geometric diode by COMSOL. The 1 V voltage was applied on the left edge of the device and the right edge of the device was grounded. The horizontal and vertical scale is in mm.

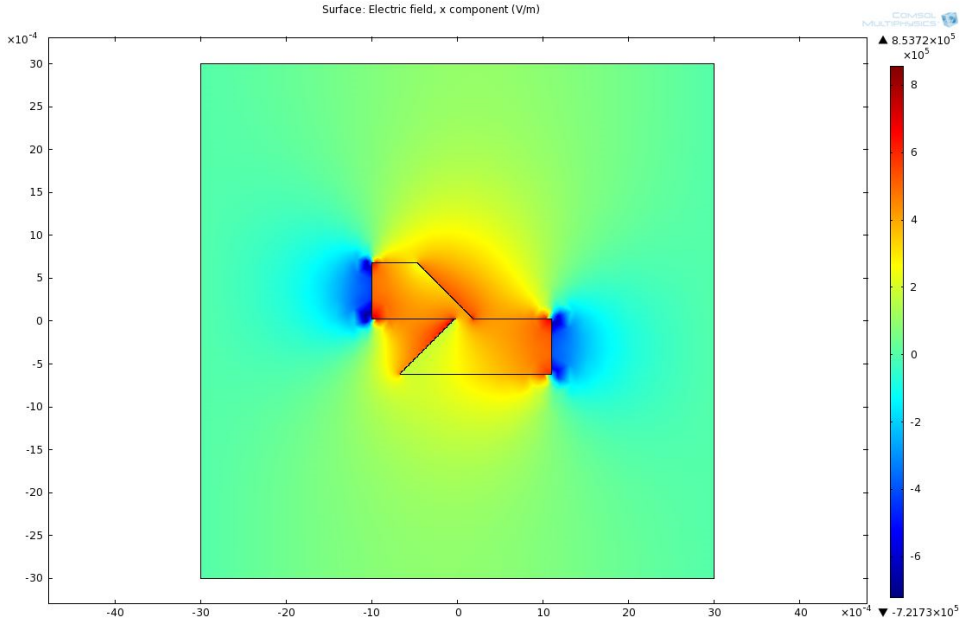


Figure VIII-5. Simulated x-direction electric field map within the Z-shape geometric diode by COMSOL. The 1 V voltage was applied on the left edge of the device and the right edge of the device was grounded. The horizontal and vertical scale is in mm.

The simulated *I(V)* characteristics of the Z-shape diode using the simplified-version simulator and the full-version simulator were compared, as shown in Figure VIII-6. Due to the non-uniformity of the E-field map, especially the weak E-field at the bottom left corner, where charges are trapped, the asymmetry of the *I(V)* curve simulated from the full-version simulator is less than that from the simplified-version. This effect is also shown in the asymmetry ratio *A* plots in Figure VIII-7.

Figure VIII-6 shows the simulated *I(V)* characteristics of allowing 100 charges to run 10^3 τ averaged over 10 runs of the simulation and of allowing 100 charges to run 10^4 τ. The comparison reveals the behaviors of the Z-shape diode at different frequencies. The diode *I(V)* characteristics are more asymmetric in the simulation with fewer collisions than that with more collisions, which is also according well to the result in Figure VIII-7. The reason is that with fewer collisions (at lower frequencies), there are fewer charges trapped in the left bottom corner region of the Z-shape diode to repel other charges therefore blocking them from being trapped. This charge build-up effect is greater for Z-shape diodes than that for the inverse arrowhead diodes in Figure III-8.

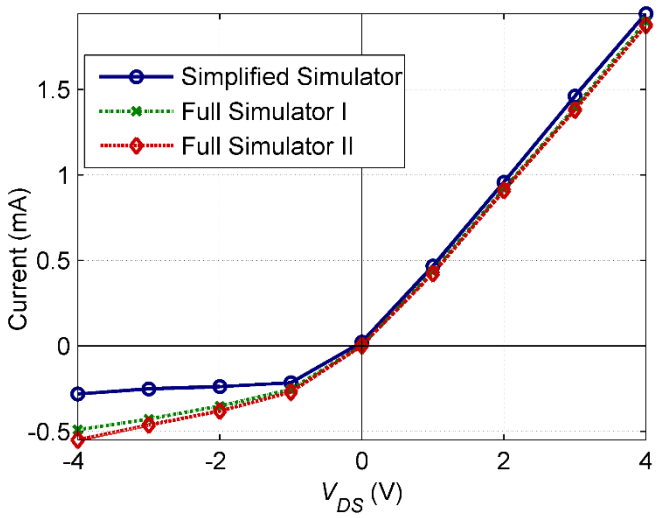


Figure VIII-6. Monte Carlo simulation results: simulated *I(V)* curve using the simplified-version simulator by allowing 1 charge to run 10^6 τ (blue line with circle marks), simulated *I(V)* curve using the full-version simulator by allowing 100 charges to move 10^3 τ (green line with cross marks) averaged from 10 runs of the simulation, and simulated *I(V)* curve using the full-version simulator by allowing 100 charges to move 10^4 τ (red line with diamond marks). The neck width of the Z-shape diode is 250 nm. The charge mean-free path length (MFPL) in all the simulations is 200 nm.

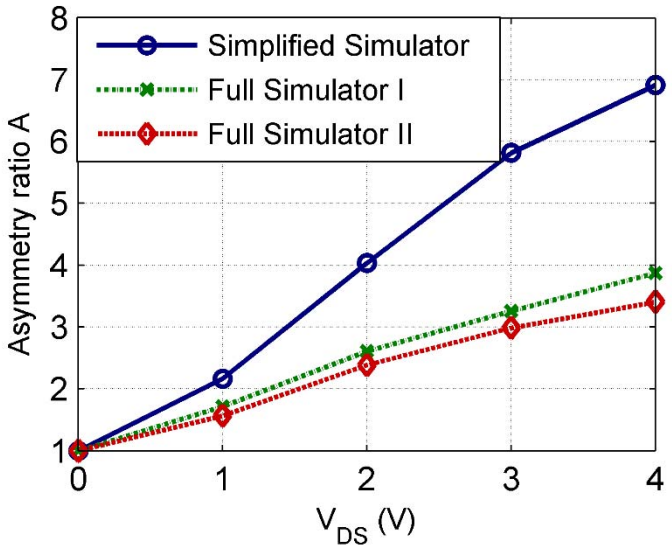


Figure VIII-7. Calculated plots of asymmetry ratio *A* versus drain-source voltage (V_{DS}) using the data of Figure VIII-6. The blue line with circle marks represents the curve using the simplified-version simulator by allowing 1 charge to run 10^6 τ. The green line with cross marks represents the curve using the full-version simulator by allowing 100 charges to move 10^3 τ averaged from 10 runs of the simulation. The red line with diamond marks represents the curve using the full-version simulator by allowing 100 charges to move 10^4 τ. The neck width of the Z-shape diode is 250 nm. The charge mean-free path length (MFPL) in all the simulations is 200 nm.

A fabricated Z-shape geometric diode is shown in Figure IV-15. The neck width of this Z-shape geometric diode is ~250 nm. Its *I(V)* characteristic, calculated differential resistance, and responsivity are shown in Figure VIII-8. The V_{CNP} of this graphene sample is approximately 20 V. The maximal responsivity, relative to the other gate voltage, is achieved at V_G = 40 V. This Z-shape diode with neck width ~250 nm achieved the same responsivity magnitude as the arrowhead geometric diode with 75 nm neck width (see Figure V-6(c)), namely ~0.11 A/W at zero bias.

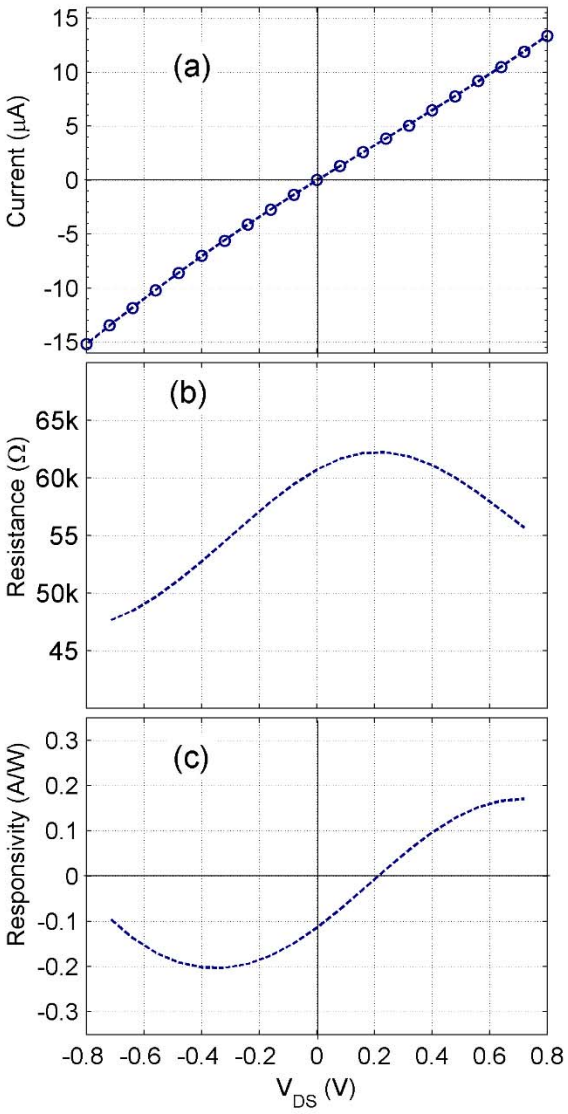


Figure VIII-8. (a) DC *I(V)* characteristics of a graphene Z-shape geometric diode described in the text at gate voltages of 40 V. (b) Calculated differential resistance of using the *I(V)* data in (a); (c) Calculated responsivity [1/2 |I"(V)/I'(V)|] as a function of the applied drain-source bias. At 0 V bias, the responsivity is -0.12 A/W.

The optical response of rectennas using Z-shape diodes has also been demonstrated. The fabricated rectenna device is shown in Figure VIII-9. The metal antennas were configured identically to the antenna in Figure V-10. The offset of the Z-shape diode to the center of the antenna gap region was caused by the misalignment from the e-beam lithography process. The critical neck region of the diode was intact.

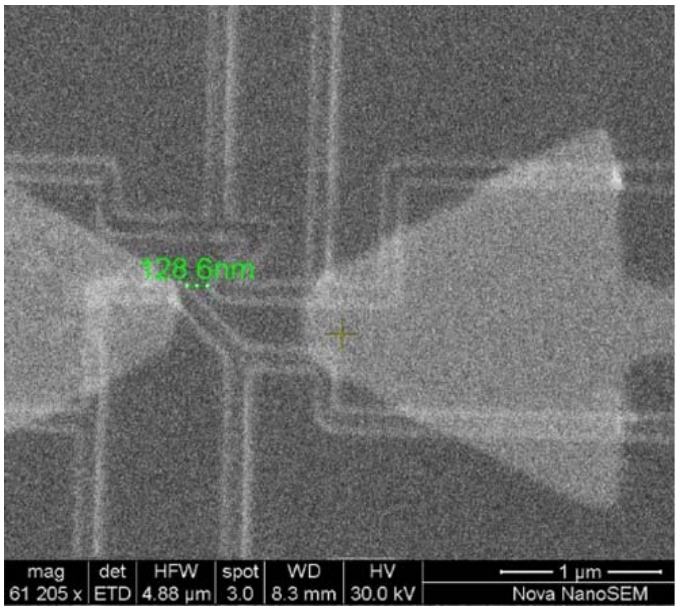


Figure VIII-9. Scanning electron microscope (SEM) image of the metal bowtie antenna coupled to a Z-shape diode. The right arm of the bowtie antenna and part of the left arm of the antenna is shown in the figure. The Z shape diode was patterned and defined using line dose writing. The line width is ~150 nm. The achieved critical dimension width of this diode is ~130 nm as marked in the figure, but the corner at the neck region was not as sharp as the diode in Figure IV-15. Although the diode is offset from the antenna center, the optical response of this device was adequately measurable.

As shown in Figure VIII-10, the open circuit voltage and the short circuit current of the perfectly aligned rectenna using the Z-shape diode were 0.62 μV and 7.2 nA. The corresponding system responsivity was 3.3 mA/W, assuming the device was misaligned by 1 mm from the center of the beam, corresponding to a P_{in} of 49 mW/mm^2. The D* and NEP of this rectenna were 4.3×10^7 cm Hz$^{1/2}$ W^{-1} and 2.6 nW Hz$^{-1/2}$.

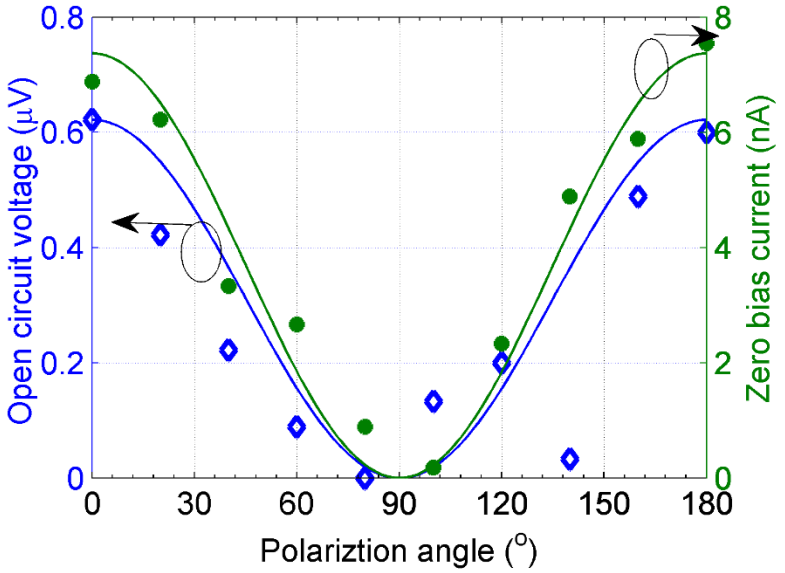


Figure VIII-10. Metal antenna / Z-shape geometric diode rectenna short-circuit current (green circles) and open-circuit voltage (blue diamonds) as a function of polarization angle (θ).

The D* of the rectenna using the Z-shape geometric diode in Figure VIII-5 is about ten times greater than that of the rectenna using the inverse arrowhead geometric diode in Figure V-10. The improvement of the performance is due to the low responsivity of that particular inverse arrowhead diode in Figure V-10. If the inverse arrowhead geometric diode in Figure V-6 were connected to a bowtie antenna, its D* would be similar to that of this Z-shape diode, which had a much larger neck width.

Thus, the above measurement results show that with larger neck width, the rectification performance of Z-shape diodes is equivalent to or even better than that of the inverse arrowhead diode with much smaller neck width.

CHAPTER IX

TERAHERTZ AND INFRARED (IR) DECTORS

Rectenna solar cells are indeed attractive for their potential high efficiency and low cost, but the required research work is at a nascent stage. In order to develop practical and high efficiency rectennas, the following diode requirements must be met: matched diode resistance with the antenna impedance for high coupling efficiency, low diode capacitance for an overall short RC time constant, and low reverse leakage current for energy harvesting (Zhu 2013). Geometric diodes have the potential to lead to practical rectenna solar cells, because they meet the first two requirements. However, the *I(V)* characteristics' asymmetry of geometric diodes is still not large enough to provide low reverse leakage current for harvesting energy. Further research investigation is required. On the other hand, the existing fabricated rectennas using geometric diodes are already excellent detectors at terahertz and infrared (IR) frequencies.

A. Types of terahertz and IR detectors

Conventional infrared (IR) and terahertz detectors are classified into two types—thermal detectors and photon detectors (Rogalski 2002). Neither type of IR detector has dominated the market because each has its limitations. Low frame rates limit thermal IR detectors, while the need for cryogenic cooling limits photon IR detectors. Rectenna detectors belong to neither of the two categories, nor suffer from their limitations.

The development of IR detectors began with thermal detectors, which can be traced back to Herschel's experiment with thermometers about 200 years ago (Herschel 1800) and Langley's bolometer in 1880 (Barr 1963). Thermal detectors absorb the incident radiation to change the temperature of the material within the

detectors. This results in a change in their electrical properties; for example, the resistance of a bolometer changes with temperature. The magnitude of the change is proportional to the incident radiation power. Thermal detectors can operate at room temperature and normally require a heat sink. Their detection performance is generally wavelength independent, but the response is relatively slow compared to that of photon detectors (Rogalski 2002), (Rogalski 2010).

The development of photon detectors relates closely with that of semiconductor technology. The first IR photoconductor was invented by Case in 1917 (Case 1917). Sixteen years later, Kutzscher discovered that lead sulfide was photoconductive and could be used as a photon detector for a wavelength of 3 μm (Cashman 1959). The electrical output of a photon detector is the photocurrent generated in response to the absorption of a photon by the semiconductor material. Because the absorbed photon energy has to be larger than the bandgap energy of the semiconductor material, photon detectors are wavelength dependent. Photon detectors usually respond much faster than thermal detectors. However, IR and terahertz photons have much lower energy than photons at visible frequencies; therefore, IR and terahertz photon detectors require cryogenic cooling to achieve good signal-to-noise performance to keep the thermally generated current below the level of the photocurrent. IR systems based on semiconductor photon detectors are normally expensive, heavy, and inconvenient to use (Rogalski 2002).

B. Performance of rectenna detectors using geometric diodes

To compare the geometric-diode rectenna with the above two detector technologies used in IR and terahertz radiation detection, several detector characteristics need to be considered: system responsivity, normalized detectivity (D*), noise-equivalent power (NEP), working temperature, and imaging frame rate.

1. Detector system responsivity

We define the rectenna system responsivity (β_{sys}) in Eq. IX-1 to be the product of the antenna absorption efficiency (η_a), the diode responsivity (β_d), and the system coupling efficiency (η_c). The rectenna system responsivity is the current output of the rectenna system for a given incident optical power.

$$\beta_{sys} = \eta_a \beta_d \eta_c$$

Eq. IX-1

The system responsivity of the rectenna detector in Figure V-10 is calculated to be 0.2 mA/W, assuming the device was misaligned by 1 mm from the center of the beam, corresponding to a P_{in} of 49 mW/mm^2.

2. Normalized detectivity

D* is a measure of the noise performance of the detector and is defined as shown below:

$$D^* = (A_d \Delta f)^{1/2} \frac{\beta_{sys}}{I_n}$$

Eq. IX-2

where, $I_n = \sqrt{(2eI_{bias} + \frac{4KT}{R_d})\Delta f}$

Eq. IX-3

For the rectenna system, Δf is the bandwidth of the detector and A_d is the area of the detector, which equals the effective area (A_{eff}) of the antenna for rectennas. The noise current (I_n) is calculated as the sum of the shot noise from the diode DC bias current (I_{bias}) and Johnson thermal noise from the diode resistance. Our rectenna detectors in Figure V-10 work at zero bias (I_{bias} = 0 A) and room temperature (T = 300 K). D* is calculated to be 2.6×10^6 cm Hz$^{1/2}$ W^{-1}, assuming the device was misaligned by 1 mm from the center of the beam. For the rectenna using Z-shape geometric diode in Figure VIII-9, D* is 4.3×10^7 cm Hz$^{1/2}$ W^{-1}.

3. Noise equivalent power

Another detector characteristic, NEP, is a measure of the minimum incident optical power required for unity system signal to-noise ratio (Richards 1994). A lower NEP value represents better detector sensitivity. NEP is related to D* and is defined as shown below (Rogalski 2002), (Zhu 2013):

$$NEP = \frac{\sqrt{A_d}}{D^*}$$

Eq. IX-4

The NEP of the metal antenna/graphene geometric-diode rectenna IR detector is calculated to be 43 nW $Hz^{-1/2}$, assuming the device was misaligned by 1 mm from the center of the beam. For the rectenna using Z-shape geometric diode in Figure VIII-9, NEP is 2.6 nW $Hz^{-1/2}$.

C. Comparison to other detectors

Thermal bolometer IR detectors working at wavelengths of 2 to 40 μm typically have a D* between 10^8 and 10^{10} cm $Hz^{1/2}$ W^{-1} at 77 K (Rogalski 2010) and between 10^6 to 10^8 cm $Hz^{1/2}$ W^{-1} at room temperature (Richards 1994). They are capable of operating at room temperature with a frame rate on the order of a few milliseconds. Our rectenna IR detectors using graphene geometric diodes have a much faster frame rate than thermal IR detectors. The fundamental limit of the frame rate is the circuit RC time constant, which is shorter than 10^{-12} s.

Compared to photon detectors, rectenna IR detectors are able to operate at room temperature and also are sensitive to the polarization of the incoming radiation. Photon detectors based on mercury cadmium telluride (HgCdTe) have become the most widely used IR detectors for mid- and long-wavelength (3–30 μm) infrared radiation. The III–V (InGaAs, InAsSb, InGaSb) detectors are used mostly for short-wavelength IR. At 77 K and 10.6 μm wavelength, HgCdTe IR detectors have achieved

D* on the order of 10^{10} cm $Hz^{1/2}$ W^{-1} (Rogalski 2002). The D* of semiconductor photon detectors generally decays by a factor of 10 for every 10 K increase in temperature (Rogalski 2010). A number of concepts (Rogalski 2002), (Piotrowski 2000), (Razeghi 1998) have been proposed to improve performance of photon detectors operating at near-room temperature. Multijunction HgCdTe photodiodes are capable of achieving a D* of 10^{8} cm $Hz^{1/2}$ W^{-1} at 10.6 μm wavelength (Piotrowski 2000).

At the time of the writing of this thesis, no other graphene detectors exist for 28 THz detection. When the incident radiation frequency is below the RC limit of the rectenna, the size of the antenna can be adjusted to any frequency. Therefore, we can compare our rectenna to graphene detectors operating at ~1 THz. Vicarelli et al. have experimentally demonstrated a graphene field-effect transistor (FET) working at 1 THz (Vicarelli 2012). In this graphene FET detector, the top gate of a graphene transistor is coupled with one arm of a terahertz metal bowtie antenna while the other arm of the antenna acts as the source terminal of the transistor. The detector responsivity is produced by a second-order nonlinear effect when an oscillating terahertz field is applied between the gate and the source terminals. The DC photovoltage output is proportional to the derivative of the drain-source channel conductivity with respect to the gate voltage. The performance of the graphene FET is fundamentally limited to the graphene top-gate capacitance coupling efficiency, which also limits its operating frequency. Our current graphene geometric-diode rectenna is at least ten times more effective than this graphene FET terahertz detector, which has an NEP of 30 nW $Hz^{-1/2}$ for double-layer graphene devices, and 200 nW $Hz^{-1/2}$ for single-layer graphene devices.

IR rectennas using MIM diodes have been demonstrated by several groups (Fumeaux 1998), (Codreanu 2003). An impedance-matched MIM diode operating at 28 THz requires a diode area of 0.001 μm^2 with 0.3 nm insulator thickness (Sanchez 1978). Such a diode will provide a theoretical NEP as low as 5 nW $Hz^{-1/2}$ to the

rectenna system. IR rectennas using practical MIM diodes have a typical NEP value on the order of 10^{-6} W $Hz^{-1/2}$ (Wang 1975). We proposed a potential solution to the RC coupling issue by using rectennas with MIM traveling-wave diodes for 28 THz detection (Estes and Moddel 2006), (Grover 2010). The approach is to fabricate MIM diodes into a traveling-wave configuration. The predicted D* of traveling-wave MIM diode rectennas can be as high as 10^9 cm $Hz^{1/2}$ W^{-1}.

Although conventional lumped-element MIM diodes are limited in performance by their RC time constant at 28 THz, room-temperature rectennas using MIM diodes can achieve high D* and low NEP at 1 THz. For the calculation of I_n and D* of the rectennas using MIM diodes in Figure VII-4, we assumed T at 300 K (room temperature) and measured I_{bias} to be 600 μA with an R_D of 94 ohms. As mentioned in chapter 6, to calculate $ß_{sys}$, the power transmitted to the diode was estimated to be 19.1 nW. With the measured short-circuit current of 8.48 nA at 0.057 V, $ß_{sys}$ was calculated to be 0.44 A/W. Using the parameters listed above, the system NEP value is 4.3×10^{-11} W $Hz^{-1/2}$, which is one or two orders of magnitude lower than that of the rectennas using geometric diodes. This NEP value indicates that our MIM terahertz detector is among the most effective existing room-temperature terahertz detectors.

Table IX-1 presents a performance summary of the IR and terahertz detectors presented above. Both D* and NEP data are not available for other types of IR detectors in the existing literature; however, I provided both D* and NEP values for our detectors for convenient comparison. The rectenna detector using a graphene geometric diode provides among the best room-temperature IR and terahertz detection performance along with high frame rates.

Detector type	D* (cm $Hz^{1/2}$ W^{-1})	NEP (W $Hz^{-1/2}$)	Incident radiation frequency / wavelength	Frame time
Bolometer (VWO) (Rogalski 2010), (Chi-Anh 2005)	10^8–10^{10} at 77 K (Rogalski 2010) 10^6–10^8 at 300 K (Chi-Anh 2005)		2–40 μm	>1 ms, ultimately limited by the thermal time constant (Rogalski 2010), (Chi-Anh 2005)
Photon detector (HgCdTe) (Rogalski 2002), (Piotrowski 2000)	10^{10} at 77 K (Rogalski 2002) 10^8 at 300 K (Piotrowski 2000)		3–30 μm (Rogalski 2002) 10.6 μm (Piotrowski 2000)	<1 μs, ultimately limited by the device RC time constant (Rogalski 2010)
Graphene FET detector (Vicarelli 2012)		2×10^{-7} (single layer) at 300 K 3×10^{-8} (double layer) at 300 K	1 THz / 299.8 μm	
Ni-NiO-Ni lumped-element MIM rectenna (Moddel and Grover 2013)	1.89 x 10^8 at 300 K 8.89×10^5 at 300 K	4.3×10^{-11} at 300 K 10^{-6} at 300 K	1 THz / 299.8 μm 28 THz / 10.6 μm	
Ni-NiO-Ni traveling-wave MIM rectenna (Grover 2010)	up to 10^9 at 300 K		28 THz / 10.6 μm	
Graphene geometric-diode rectenna	10^6–10^7 at 300 K (inverse arrowhead shape diode) 10^7–10^8 at 300 K (Z-shape diode)	10^{-8} – 10^{-9} at 300 K 10^{-9} – 10^{-10} at 300 K	28 THz / 10.6 μm	>1 fs, ultimately limited by the rectenna RC time constant

Table IX-1 Performance of existing terahertz and IR detectors.

D. Night vision application analysis

A major application of the low-cost rectenna IR detectors is in night vision systems, e.g., for use in automobiles. We consider the noise-equivalent temperature difference (NETD) to quantify detector performance for night vision applications. NETD is the incident signal temperature required to match the internal noise of the detector, so that the signal-to-noise ratio equals one (Rogalski 2003) and corresponds to the lowest temperature difference that can be detected (Meyer 2012). The requirement for reasonable automotive night vision is to have an IR detector with a NETD value less than 0.3 K (ADOSE 2008). The NETD is calculated as (Rogalski 2010):

$$NETD = \frac{I_n\sqrt{f_F}}{\beta_{sys} dP/dT}$$

Eq. IX-5

In Eq IX-5, dP/dT refers to the thermal variation of the spectral emittance, I_n is still the noise current, f_F is the video frame rate, and $ß_{sys}$ is the rectenna system responsivity.

At a drain source bias of 0 V, the noise current is 12 pA $Hz^{-1/2}$. For night vision application, a video frame rate of 30 Hz is assumed. Faster frame rate is better but not required. The geometric diode in Figure V-6, though far from optimal, is used for the following analysis. The device has a diode responsivity of 0.12 A/W at a V_{DS} of 0 V. I use a β_{sys} of 0.06 A/W assuming a 50% antenna absorption efficiency and perfect impedance matching. The differential dP/dT can be calculated by subtracting the integral of Planck's law at two temperatures with a temperature difference of 1 K, in a 30 Hz bandwidth over the spectral range of 8 to 14 μm (Grover 2011). A typical bolometer night vision system has a pixel pitch of 35 μm (Meyer 2012). Assuming that the antenna absorbs the radiation with such area, dP/dT can be calculated to be 3.2 nW/K (Grover 2011). Using the above parameters, the NETD of geometric diodes is

~0.3 K. Using the simulated *I(V)* and responsivity data, the NETD of geometric-diode rectennas can potentially drop to 0.03 K or even lower. This is on the same order of magnitude as the NETD of night vision bolometers, which is ~0.06 K (Yon 2003). Photon IR detectors are predicted to have an NETD value of less than 0.1 K at the same frame rate of 30 Hz (Piotrowski 2000). Because of the poor coupling efficiency, rectennas using MIM diodes have a much higher NETD value of ~140 K (Grover 2011). Thus, geometric-diode rectennas are expected to have NETD values that are lower than those of photon IR detectors, and at least as low as those of bolometers, but with the capability of much higher frame rates.

CHAPTER X

CONCLUSION

In summary, I have developed a new kind of ultrafast graphene diode with an ultra-low RC time constant for optical rectenna application. Geometric diodes are one of the fastest diodes in the world. In the thesis, two types of geometric diodes were discussed: inverse arrowhead-shape and Z-shape geometric diodes. With the same constriction region width, Z-shape geometric diodes exhibit much larger I(V) asymmetry than the inverse arrowhead diode.

I conducted computer simulations and performed electrical measurements to demonstrate that the diode's geometric asymmetry creates an I(V) asymmetry. I used the simplified simulator to simulate the I(V) characteristics for the inverse-arrowhead shape diodes. For the devices with greater geometry asymmetry, such as the Z-shape diodes, a full-version simulator has to be used for more accurate results. Comparing to the simplified simulator, the full-version simulator includes the real E-field map and the charge-charge interaction forces. Therefore, the charge built-up effect at the charge trapping region can be simulated with the full-version simulator. Furthermore, the frequency response resulting from such charge built-up effect can be studied in the future.

Fabrication of working geometric diodes requires materials with long MFPL and an extremely fine nano lithography patterning technique. Using graphene as the material was quite a breakthrough in the geometric diode project. The measured electrical characteristics of graphene geometric diodes are consistent with the Monte Carlo simulations. The diode responsivity at zero drain-source bias is 0.012 A/W. Unlike traditional p-n diodes, the turn-on drain-source voltage of geometric diodes is 0 V. An additional notable unique property of graphene geometric diodes is its polarity-reversal capability by applying the gate voltage.

Fabricating graphene geometric diodes with high I(V) asymmetry is not an easy task. Graphene exfoliation is a complicated process and cannot be used for mass production. Also, graphene is easily contaminated. The electrical quality of graphene degrades with increasing fabrication processing steps. Unwanted doping was added to graphene from the PMMA coating process and the ebeam writing process. In the future, the ideal process to pattern graphene should totally prevent any chemical and lithography process. A possible approach could be using the hydrogen plasma to etch the graphene following its lattice structure at atomic level. If possible, the ideal device measurement environment would be under vacuum and at low temperature.

Rectenna solar cells using graphene geometric diodes are indeed attractive for their high ultimate efficiency and low cost of production. Without any tuning for optimization, current geometric diode rectennas are already among the best terahertz and infrared detectors in the world. The rectenna using the Z-shape geometric diode has an NEP value of 2.3 nW $Hz^{-1/2}$ at 28 THz. In theory, rectennas using current Z-shape geometric diodes can achieve an NEP value as low as 10^{-10} W $Hz^{-1/2}$ at IR frequencies.

However, the research on geometric diodes is still at a nascent stage. To harvest thermal or even solar optical frequency energy, a breakthrough in improving the diode I(V) asymmetry is needed. Indeed, increasing the device geometry asymmetry leads to greater I(V) asymmetry, but it is not enough to achieve the required high I(V) asymmetry to harvest energy. The proposed methods described in chapter 8 were only able to linearly improve the diode I(V) asymmetry. Without any external field, the constriction region of geometric diodes will always act as the leakage path for the charges flowing in the reverse direction. Creative innovation to change the intrinsic charge carrier profile within the device may be able to completely block the leakage path and exponentially improve the diode I(V) asymmetry. This could be achieved by adding a local gate field and by applying an external electrical field and magnetic

field. Three terminal graphene devices may be another way to improve the rectenna system efficiency.

In conclusion, geometric diodes are still among the best candidates for using optical rectennas to harvest energy, and more follow-up work is required to make rectenna solar cells using geometric diodes a reality.

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