Digital Control of LFSW HID Lamp Drivers with Soft Saturation Magnetic Materials and Integrated Resonant Lamp Ignition

By

RYAN WEI-MING SCHNELL

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Thesis co-directed by Associate Professor Regan Zane and Associate Professor Francisco Azcondo

Electronic HID ballasts provide many advantages over magnetic HID ballasts including size, weight, overall efficiency, and greater control of operating conditions. Electronic ballasts add complexity to the system, requiring a greater understanding of the operation of HID lamps. Electronic ballasts also introduce a host of issues for the HID ballast designer including possible acoustic resonances, arc stability issues, and operation across broad operating conditions. In this work, research of a Low-Frequency Square-Wave (LFSW) HID solution is performed that includes use of a non-linear soft saturation core material for the inductor. Modeling of the converter with this core is presented as well. Difficulties with operation of HID lamps are outlined, as well as the previous methods to overcome such obstacles.

Ignition and steady-state operation of HID lamps occur with very different operating conditions. Ignition occurs with very little lamp current, but large lamp voltage, and steady-state operation is the opposite. Due to this mismatch, any single ignitor/ballast design requires the inductor to be able to handle both operating points.

Use of a soft saturation material allows for a reduction in size and weight of the overall system due to the higher magnetic capacity of the material as compared to hard saturation alternatives. The downside to using this material is inductance varies with magnetizing force on

the core. A resonant ignition approach with soft saturation material is presented, motivating the need for phase control of the system.

A fast transition between resonant and LFSW mode operation is presented, which requires a large design space for possible lamp impedances. Transition times between LFSW modes are dependent on natural frequency and Q factor of a buck filter response, which is shaped beneficially by the soft saturation material. A design method for this is presented, along with considerations for core selection.

A two loop control method is analyzed with an inner current loop that stabilizes the lamp arc and an outer power loop in order to obtain regulated light output. The current loop is able to monitor currents of a positive and negative buck mode operation using a single sense point. A system that uses input power sensing to ultimately control output power is analyzed and experimentation is presented.

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1 Introduction

Chances are the reader is currently using some form of artificial light in order to read this. Combustion was the main source of artificial lighting until Thomas Edison's famous 1879 invention of the electric light bulb. With each new development in lighting technology, efficacy improvements were seen. Today, the old boundaries of lumens per watt are being shattered, but with the new technologies come more complexity of operation.

Currently, it is projected that about 7% of energy consumption in the United States of America is due to lighting. This number increases to approximately 20% if only electrical energy consumption is considered [1]. This is significant, and improvements in the efficiency are greatly welcomed at this time. Discounting combustion lighting sources, as they have mostly fallen to the wayside as a main means of lighting due to practicality, low efficiency, and low luminance, lighting is currently achieved by incandescence, electrical discharge, or electroluminescence. Table 1.1 shows a sample of current commercially available lighting solutions. It can be seen that incandescent bulbs have a low efficacy as compared to many of the newer types of lighting available. Reasons for slow adoption include initial cost of system, as well as difficulties in operation of some types of lighting technologies.

The basic principle of incandescent lighting is emission of visible spectrum radiation due to temperature. For a regular incandescent light bulb, this is currently performed by running current through a tungsten filament. The filament is housed in a vacuum, allowing for explosion free operation in an environment without oxygen or other easily combustible materials.

Table 1.1 Example lighting technologies lumens and efficacy

Light Source	lm/W	% of 683.002 lm
Candle	0.3	0.04
Gas light	1-2	0.29
Incandescent Bulb	5-35	5.12
Xenon Arc	30-50	7.32
Mercury-Xenon	50-55	8.05
Compact Fluorescent	46-72	10.54
Tube Fluorescent	60-100	14.64
Metal Halide	65-115	16.83
White LED	10-150	21.96
High Pressure Sodium	85-150	21.96
Low Pressure Sodium	100-200	29.28

Operation of incandescent light bulbs is relatively simple compared to other lighting technologies due to the readily available AC lines across the United States. The filament and bulb have been engineered to provide an acceptable lifetime per bulb, and tungsten provides a good color rendering, which is close to a perfect black body radiator. Tuned to the standard AC lines of different world regions, incandescent lighting requires no additional power conditioning at the point of use, and the most complicated addition to the operating circuit of such lighting is often merely a switch.

In contrast to incandescent lighting, both electrical discharge and electroluminescence lighting require a sizeable amount of operational circuitry in order to obtain operation. The trade-offs include a chance for: an increase in useable light compared to energy input into the system, longer operation times, more flexibility in operation modes, ability to control color spectrum, and better light output maintenance. Required circuitry often includes a power factor corrector (PFC) in order to condition incoming power, some kind of power conversion circuit, and in the case of

electrical discharge lamps an external ignitor [2]-[10]. Use of a universal PFC front end can lead to a lighting solution that can be used on various AC line voltages and frequencies.

Electrical discharge lighting is performed by applying a current through a medium, which is often gas, and obtaining a radiation from it. Examples include Xenon arc, Mercury-Xenon, Fluorescent (Compact and Tube), Metal Halide, and Sodium Lamps. A higher light output class of discharge lamps is referred to as High Intensity Discharge (HID) lamps. In their extremes, HID lamps have been made that can outperform incandescent lights in the order of seven times the lumens per Watt, or the human useable light efficacy measurement. Difficulties in operating gas discharge lamps include, but are not limited to: ignition that often requires a high voltage spike [11], cataphoretic phenomenon leading to migration of charged gas molecules, acoustic resonance which leads to flickering or even catastrophic lamp failure [12], and electrode maintenance issues [2]-[8], [13]-[15]. These issues require a relatively large infrastructure, and as such, add size, weight, and complexity to operation of the bulbs. A simplified block diagram is shown in Figure 1.1.

In addition to the above mentioned issues, a gas discharge lamp exhibits a negative small signal resistance to slow variations in lamp current. A qualitative display of the small signal lamp impedances is shown in Figure 1.2. A fast change in

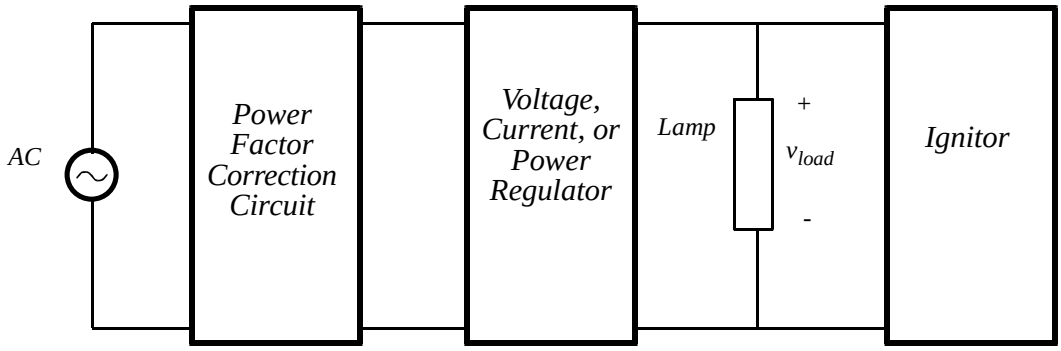


Figure 1.1: Block Diagram of HID Lamp Operation

current leads to a slope close to S_1, a slow change in current can exhibit a slope closer to S_2 [16]-[18]. A negative small-signal resistance driven by a voltage source may react in an unstable manner, and as such a current source is preferred. One method to counteract this negative resistance is to place a larger positive resistance in series with it, but this leads to unnecessary conduction losses, and thus poor efficiency.

Electroluminescence can be seen in light emitting diodes (LED), as well as powder and other thin film manifestations. In low light output applications, electroluminescence has found uses as night lights, dashboard indicators, wrist watch backlighting, and more. For higher light output applications the LED is the current leader in the market due to its compact nature, and high light output efficacy.

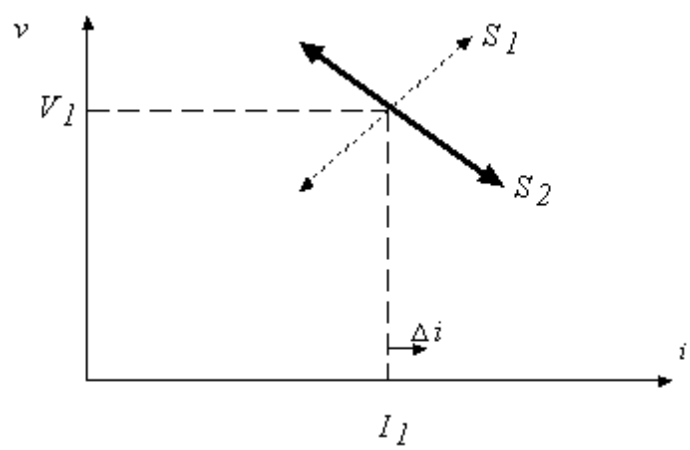


Figure 1.2: Small signal resistance of HID Lamps with fast (S1) and slow (S2) Variations.

A common circuit for operating high brightness LED's may look similar to Figure 1.1, but does not require an external ignitor element. One issue that arises when designing LED circuits is that the high speed of the LED turn on and off allows for a noticeable flickering effect to occur if only rectified 120 Hz AC line current is used. If a large capacitor is used directly on the output of the rectifier, the problem of poor power factor arises, leading to the need of a PFC.

Operation of LEDs has proven to be cumbersome due to the non-linear nature of operation, as they are in essence, a diode in forward conduction. Another problem the high wattage LEDs has encountered is a drop in current when the temperature increases above a temperature break point. This is known as LED “droop”, and is the cause for a large drop in efficiency at higher power levels [19].

1.1 Power Conversion Introduction

It has been mentioned that some form of power conditioning is required in order to operate newer lighting technologies than incandescent light bulbs. It is useful to give a brief background on the need and implementation of basic power conversion. Consider a simple DC voltage and a known load resistance. It is desired to operate the load at a lower voltage than is provided by the source, be it a battery, large capacitor, or a switching power supply. For a given load, the simplest solution that does not consider efficiency is merely a resistor divider, as seen in Figure 1.3.

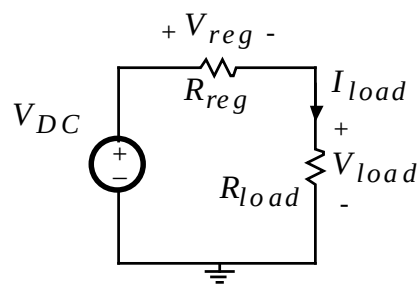


Figure 1.3: Resistor divider voltage source

The voltage of the source is indeed higher than the load voltage, and in the theoretical case that the load is to be driven at 50% of the voltage found at the source, $R_{reg} = R_{load}$. Although this voltage divider obtains the requested result, there are two major problems that must be

addressed [20]. If efficiency, η, is defined as $\frac{P_{out}}{P_{in}}$, one can see that the efficiency of this circuit is at 50%. In fact, the efficiency of a voltage regulator like this will always be equal to the drop in voltage required, as the extra voltage is merely dropped across a resistor to dissipate the energy. The second problem with this voltage converter topology is that it only works for a given load. If the load resistance were to vary, the output voltage would follow. This problem can be controlled by using a linear regulator in place of R_{reg}, but the efficiency is still dependent on the voltage division required.

Since the problem with this converter stems from the use of a resistor, consider two other passive elements, the capacitor and the inductor. The equations relating voltage and current to these devices are

$$i_L = L\frac{dv_L}{dt} \tag{1.1}$$

$$v_C = C\frac{di_C}{dt}. \tag{1.2}$$

These passive parts are known as the reactive components, as energy is stored within them, rather than dissipated as in a resistor. If these components are paired together as shown in Figure 1.4, a resonant pair is created.

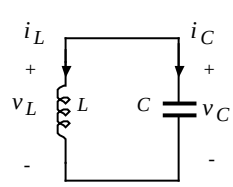


Figure 1.4: LC Resonant Pair

Now that the voltage and current of the two elements are related as

$$i_L = -i_C$$
$$v_L = v_C \tag{1.3}$$

,

an ordinary differential equation (ODE) is created. It can be shown that the solution to this ODE is

$$i_C(t) = Ae^{+j\omega t} + Be^{-j\omega t} \tag{1.4}$$

,

where

$$\omega = \frac{1}{\sqrt{LC}} \tag{1.5}$$

.

This is a physical system, so one can set $A = B$, and the particular solution using Euler's identity [21]-[23] becomes

$$i_C(t) = 2A\cos(\omega t) \tag{1.6}$$

.

This solution says that the current in the inductor will oscillate with a frequency of

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \tag{1.7}$$

indefinitely. The same can be found for the voltage, although the phase will be shifted. The capacitor and inductor are known as lossless elements as theoretically, once this circuit is energized, it will keep ringing forever. In reality, resistances exist, creating a damping factor, and causing the circuit to decrease in oscillation over time.

Energy is stored within the capacitor in the form of a voltage potential, while the inductor stores energy in a magnetic field. The equations for the amount of energy in each element are

$$u_C = \frac{1}{2} C v_C{}^2$$
$$u_L = \frac{1}{2} L i_L{}^2 \tag{1.8}$$

Using these lossless elements, a theoretically lossless converter capable of reducing input voltage can be constructed [20].

The voltage, v_{switch}, is either V_{DC} or zero, depending on the state of the high side MOSFET. Defining the impedance, or voltage divided by current of the inductor and capacitor in terms of the characteristic equation using the Laplace transform, and defining $s = \omega\sqrt{-1} = j\omega$, one obtains

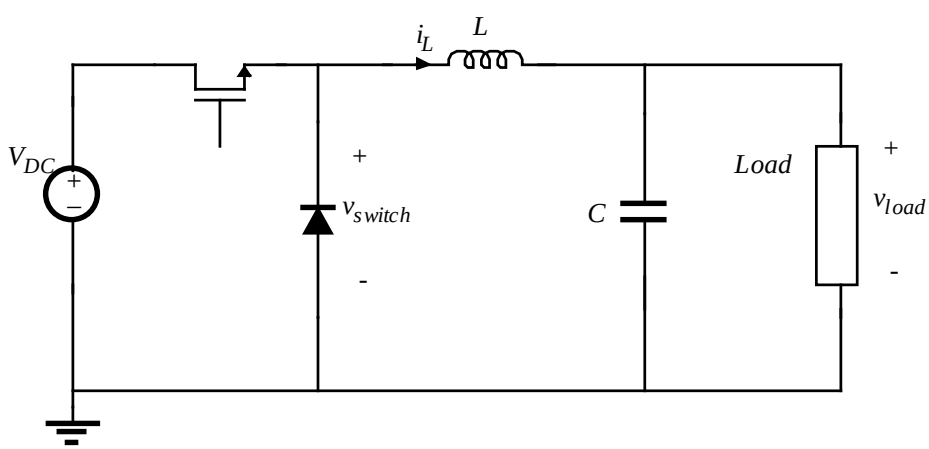


Figure 1.5: Lossless buck converter schematic

$$Z_C = \frac{1}{sC}$$
$$Z_L = sL \tag{1.9}$$

Calculating the load voltage in terms of the switch voltage by use of a resistor divider of the impedance of the parallel combination of the load and capacitor, and the inductor, one arrives at

$$\frac{v_{load}}{v_{switch}} = \frac{Z_C // Z_{load}}{Z_L + Z_C // Z_{load}} = \frac{1}{1 + s\frac{L}{R} + s^2 LC} \quad (1.10)$$

This is a two pole response, and can be written in terms of resonant frequency and quality factor, Q, and defining the load as a simple resistance,

$$\frac{1}{1 + s\frac{L}{R} + s^2 LC} = \frac{1}{1 + s\frac{1}{Q\omega_0} + s^2 \omega_0^{\ 2}} \quad (1.11)$$

Choosing C = 1 F, L = 1 H for demonstrative purposes, the resonant frequency is found to be $f_0 = \frac{1}{2\pi}$. The frequency responses of the system from the switching voltage to the output voltage follow the plots shown in Figure 1.6. Various resistances are shown, illustrating different Q factors.

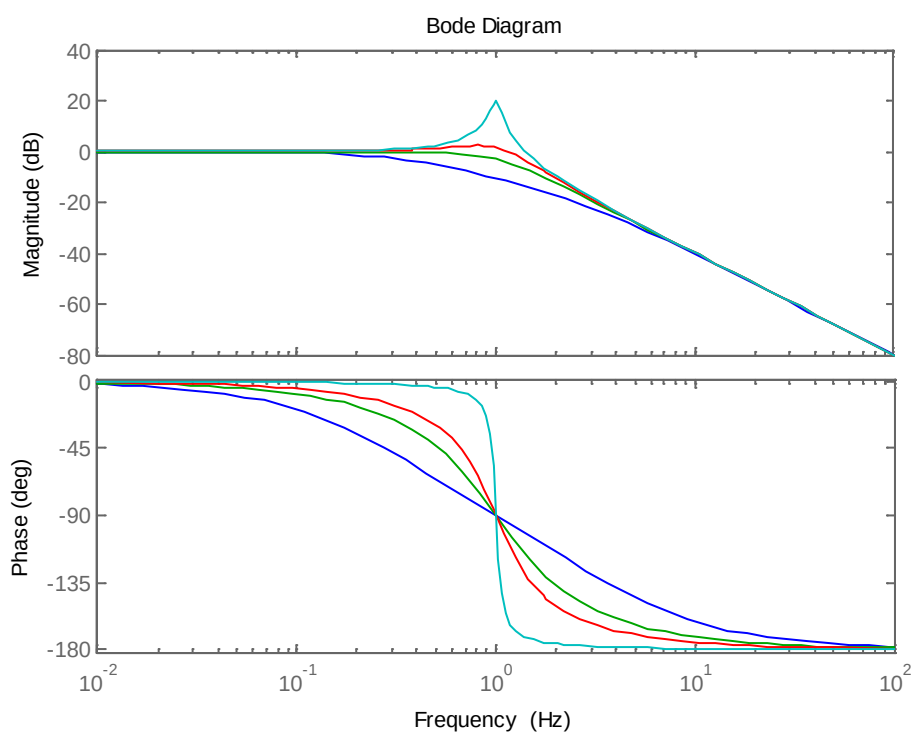


Figure 1.6: *Q* factor of a 2-pole system. *Q* = 0.3 (blue), *Q* = 0.7 (green), *Q* = 1.2 (red), *Q* = 10 (teal)

It can be seen that the low frequencies are passed much easier than the higher frequencies, and the circuit behaves like a low pass filter. If the switching frequency is much higher than the resonant frequency of the *LC* pair, essentially only the DC term of the Fourier components is passed, and the DC offset of v_{switch} is passed. This equates to a conversion ratio, *M*, of

$$M = \frac{V_{load}}{V_{switch}} = \frac{1}{D}, \tag{1.12}$$

where *D* is defined as the percentage of a period the MOSFET is on. It can be observed that near resonance, if the *Q* factor is above about 0.7, the output amplitude is higher than 0 dB, meaning the output voltage is higher than the input voltage [20]. Operating in such a condition can be useful, but it must also be said that the output voltage waveform assumes more of a single frequency, and the output begins to look sinusoidal as resonance is approached. A common approximation of this effect is called the high-*Q* fundamental approximation, where the output voltage can be described mainly by the sinusoidal contribution from v_{switch} near resonance. This is the basis for many resonant power converters.

Since lighting applications tend to occur where people are, there is a distinct interest in not only providing high-efficiency lighting for cost reasons, but also compact design in order to not interfere with living spaces. One method to reduce the size of magnetic components in power converters specifically is to increase the switching frequency. The magnetic components are often the heaviest within power circuitry, and often take up a sizeable portion of the physical volume. A higher operating frequency can lead to smaller magnetic components, but comes with its own host of problems. The first issue is switching loss. Switching losses can occur from the repeated charging and discharging of capacitance on switching elements. The exact mode of loss

can be the actual charge of the gate capacitance on a MOSFET being lost, although this is normally small. Another form of switching loss is called hard-switching. This is a shoot-through like condition in which a reverse recovery of a diode creates a short time where other elements experience both high voltage and current. In order to deal with this loss, a class of converters called resonant converters has been studied.

The basic operation of a resonant converter is to use an LC resonance in order to time turn-on or shutdown of a switching element. With knowledge of the LC values, correct timing can be employed in order to obtain zero-voltage switching (ZVS) or zero-current switching (ZCS). Zero-voltage switching occurs when the voltage across an element in consideration is brought to zero prior to device turn-on by a natural ringing between an inductor and a capacitor, and zero-current switching is the same case, but involving current through the element in question.

Two common HID ballast resonant converter configurations [8], [24] are shown in Figure 1.7. The LC_PC_S converter finds use in applications where the DC input voltage needs to be boosted, and the LC_SC_P is generally the more efficient choice in which the DC input voltage needs to be lowered for the load application.

The LC_SC_P converter often finds use as an electronic ballast for HID lights as a second stage after a universal input (~90-240 VAC) PFC unit. Its advantages include the ability to operate as a near lossless high output impedance source, and can provide high efficiency running at high frequencies.

Operation of a resonant converter is usually defined by the operating frequency, which is further defined as being above or below resonance. Figure 1.8 shows an input-to-output bode plot of an LC_SC_P converter. The values are: L = 190 µH, C_S = 68 nF, C_P = 1.5 nF, R = 1500 Ω.

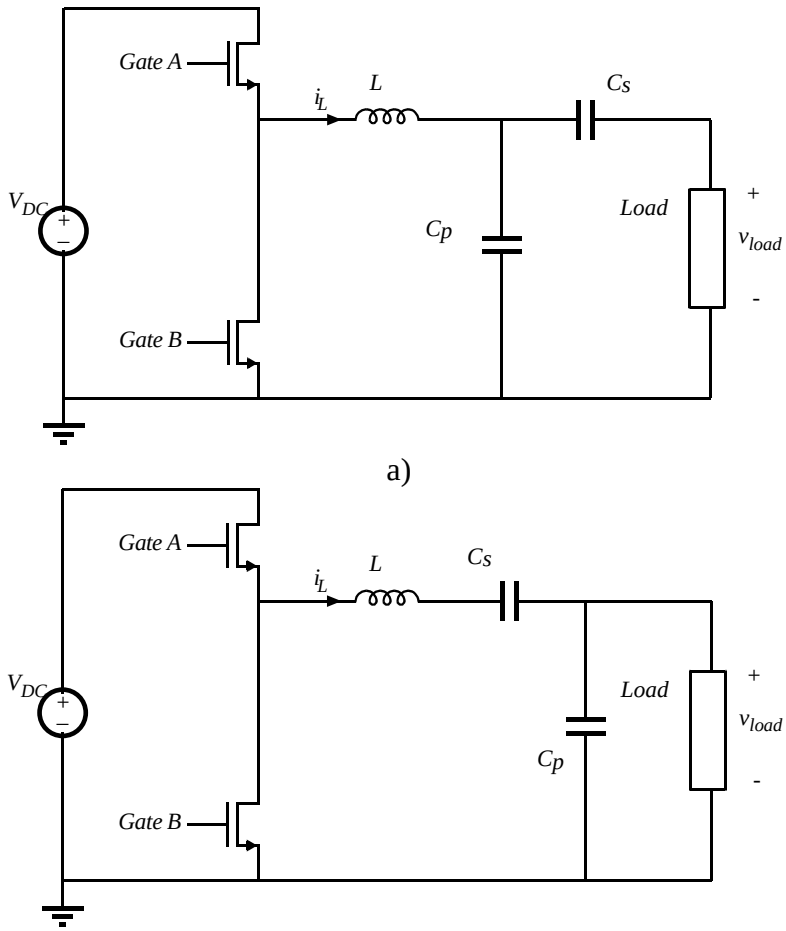


Figure 1.7: a)LCPCS Resonant Converter b) LC_SC_P Resonant Converter

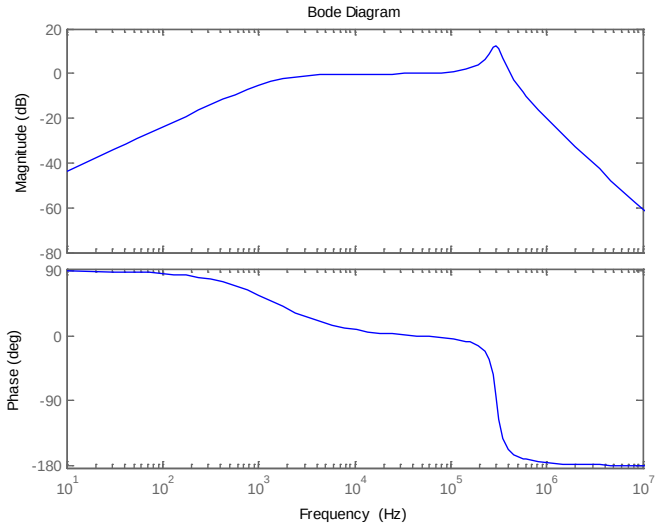


Figure 1.8 Bode Plot of Input-to-Output Transfer Function of an LC_SC_P Resonant Converter

Resonance is observed at 300 kHz, and the existence of resistance leads to the Q factor not diverging to infinity.

Operation above 300 kHz leads to operation in the ZVS region, and also coincides with operation where the tank impedance looks more inductive than capacitive. Operation below resonance in this converter leads to ZCS operation. Lower switching losses are generally found with ZVS conditions.

Another class of converters that provide the benefit of reduced switching loss, but free it from the completely sinusoidal requirements of most resonant topologies, is the quasi-resonant converters. One example is the quasi-resonant flyback, shown in Figure 1.9.

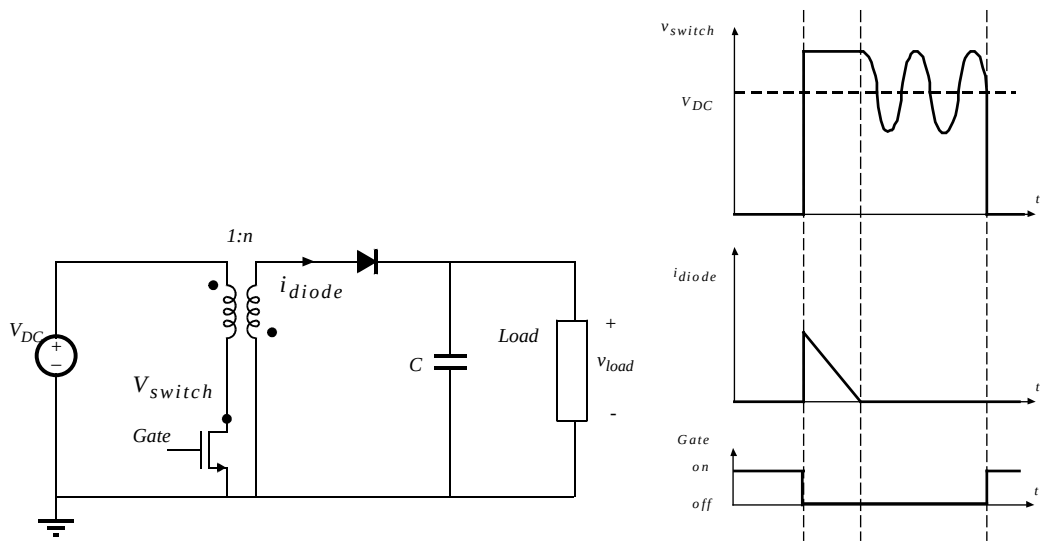


Figure 1.9: Quasi-resonant Flyback Converter with typical waveforms

The ringing observed in operation is brought about due to a discontinuous conduction mode (DCM) occurring due to the diode being reverse biased. Once the DCM mode begins, a resonance between the transformer leakage inductance and parasitic capacitance begins to ring. This ringing allows the drain-to-source voltage on the MOSFET to ring towards zero, and in some cases reach zero. If the timing of the MOSFET turn on were to be placed at the low point

of the voltage ringing, low voltage switching (LVS) would be obtained, and a lower switching loss would be observed.

A simplified overview of basic power conversion techniques has been presented. These basic principles serve as the backdrop to operating more complex lighting systems from already existing electrical infrastructures. Capabilities of digital circuits allow the application of diverse control and driving strategies, involving soft and hard switch operation, over a power topology to solve the specifications required by all type of HID lamps of a given power rating from different manufacturers in any of the operation stages. Combination of linear and non-linear control techniques result in the most suitable combination of transients optimization, stability performance, adjustment of the operation point, light quality, and efficiency. Soft saturation magnetic materials pave the way to reduce the size of the inductor taking advantage of their higher saturation magnetic flux density. Additionally, the current dependent inductor can compensate the quality factor deviation of the power filter caused by the lamp aging. All of this results in new limits for the electronic ballast technology in terms of power conversion density, warm-up time reduction and harmonic content of the lamp power.

Current HID lamp ballasts fall into two main categories of magnetic and electronic. Electronic ballasts can provide better lamp efficiency and control of operating conditions. Within electronic ballasts, there are resonant and non-resonant converters. In this work, a non-resonant converter has been chosen in order to avoid certain special problems that occur in HID lamps. The particular converter type is Low-Frequency Square-Wave, and the motivation for the choice will become apparent in the following chapters. One of the research topics centers around the use of soft saturation magnetic materials to obtain size reduction, and improvement of converter performance.

1.2 Thesis Outline

Chapter 2 gives detailed information on operation of HID lamps and common problems addressed in existing solutions. It describes discharge lamp modes, stability issues, and discusses problems such as acoustic resonance and cataphoretic phenomenon.

Chapter 3 details operation of HID lamps with resonant converters using phase control as well as a soft saturation core material. It shows analysis and design proposal of the soft saturation core inductor, and discusses operation concerns this brings about. This chapter also details the difficulties seen at ignition, and presents a modeling method to simulate ignition with a soft saturation core inductor.

Chapter 4 deals with the design and implementation of a LFSW ballast for steady-state operation of the lamp. This discusses the reasoning for choosing this topology, and its advantages over existing choices. Improvements in warm-up operation are also presented.

Chapter 5 discusses design considerations for a power factor correction stage. Utilizing a standard PFC, design constraints are presented in order to allow for large PFC output voltage ripple. This translates to a decreased design effort for the PFC designer, reducing implementation time and/or cost.

Chapter 6 goes into detail about the experimental test bed created to verify design methods in the thesis. Experimental results are presented showing stable and reliable lamp ignition and operation.

Chapter 7 serves as a conclusion to the thesis, summarizing the conclusions. The work presents analysis of use of soft saturation material to obtain a robust HID lamp ignition. Additionally, a two loop control method is presented in order to both stabilize the lamp current while resulting in a constant power operation. Design criteria are defined in order to create lamp

ballasts that can accept large input voltage ripples without detrimental effects to the operation of the lamp. This chapter also presents possible paths of future work that are extensions to the groundwork laid out in this thesis.

2 HID Lamp Operation Background

Although operation of an incandescent light bulb is relatively simplistic due to the electrical standard in the United States, the benefit of increased lighting efficiency when using high intensity discharge (HID) lamps outweighs the added complexity of their operation. In this chapter, basic operation of HID lamps and common issues found during operation are discussed, and some example existing solutions are presented. Types of HID lamps include but are not limited to: metal halide (MH), high pressure sodium (HPS), Xenon, and Mercury Vapor (MV) [2]-[8]. A focus is given in this work on the operation of MH and HPS lamps due to their available power levels, efficacy ratings, and widespread use in lighting systems.

2.1 Basic Lamp Operation

High intensity discharge lamps are a type of gas discharge lamp. The basic mode of radiation is ionization. Gas discharge lamps are usually filled with a noble gas, such as argon, neon, and/or xenon, as well as halide metals, mercury, and/or sodium. The lamps create emissions by ionizing the gas which in turn excites electrons in the gas or metal molecules. The excited electrons are forced into a higher state of energy, and when the electron settles to its original state, a photon is emitted. The frequency of the photon depends on the energy state transition, and is directly related to the amount of energy difference there is between the two states the electron transitions from. This is shown in (2.1) where c is the speed of light, h is Planck's constant, λ is wavelength, f is frequency, and E is the energy difference between electron states,

$$E = \frac{hc}{\lambda} = fh \quad . \tag{2.1}$$

In order to obtain a situation where gas ionization can occur, a current is applied through the gas between two electrodes. These electrodes are often made out of tungsten. The gas filled chamber exhibits a break down voltage that is dependent on gas mixture, temperature, distance between electrodes, pressure in the tube, and condition and shape of electrodes [13], [25]. Once this breakdown voltage is overcome, an arc can occur within the tube. The arc at this stage is characterized as a glow-arc, and can be identified by a low current. Arcing voltages for MH and HPS lamps can be found as high as 5 kV on manufactures recommended specifications for lamps with powers below 400 W [2]. Once an arc occurs, the resistance in the tube drops, allowing for a smaller required voltage to sustain the arc [16], [17], [25].

Immediately after ignition, the lamp must perform what is called the warm-up phase. The warm-up phase can last several minutes, and depends greatly on both the lamp dynamics, and the operating conditions of the ballast running the lamp. Conventionally, it is believed a constant current source is the desired operating mode during warm-up [2]-[8], [26]-[28]. During the warm-up process, lamp voltage is lower than nominal, and imposing a nominal power on the system increases the lamp current above the normal operating range [29]. The warm-up current is controlled by the limits found in the converter, and once the lamp impedance increases to a suitable value, power regulation is able to take over. In this way, warm-up can be shortened as the lamp is driven harder than normal by use of the higher than steady state currents. The warm-up step is dictated by a need to vaporize the metal salts in the tube, allowing plasma to form, which aids in providing molecules that can exhibit ionization, and therefore photon emission.

During the warm-up period, the color of the light output of the lamp can change drastically, as the mixture of available molecules in the plasma change.

The warm-up phase is complete once the lamp reaches its rated operating power level and the lamp large-signal impedance has settled to a constant value. The lamp can achieve rated power before the lamp resistance has settled, necessitating the control of both the lamp current in order to stabilize the arc and the lamp power in order to control brightness. Common design solutions are closed-loop, but solutions exist where the operating power is assumed from knowledge of component values, lamp resistances, and a known acceptable window of operation. This allows for a much simpler open–loop operation, at the expense of precision of power output. There are arguments for and against this, as light output is not exactly directly related to lamp power, for reasons such as electrode sputtering which will be described later.

2.2 Lamp Ballasting Stability

During normal operation of a high frequency or DC HID lamp ballast, a steady-state lamp large-signal model can be described as a simple resistor [25]. The small-signal dynamics are more complex, and lead to the requirement of a ballast. Figure 2.1 shows a qualitative representation of the small-signal i-v curves of an HID lamp in full power operation.

A fast change in current leads to a positive slope such as S_1, while a slow change in current can exhibit a slope that is negative like S_2. If the variation is slow, a drop in voltage will lead to a rise in current [16], [17]. If the ballast were acting like a voltage source, a drop in voltage would request a larger current in most control schemes, thereby feeding the problem, and causing an even greater rise in current. If the current in the lamp either grows too large or too small, the arc can either break the bulb, or extinguish, resulting in non-desirable lamp operation.

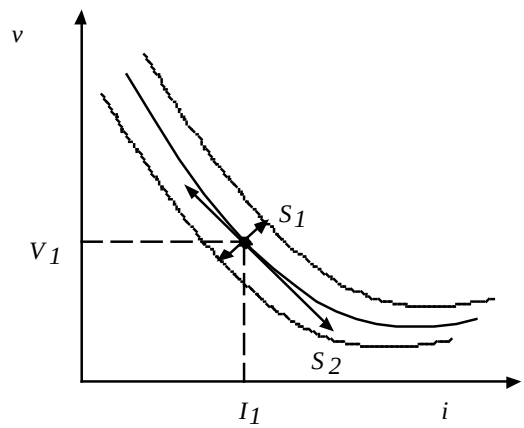


Figure 2.1: Small Signal Resistance of HID Lamps with Slow (S2) and Fast (S1) Variations

It can be said that to insure stability, the output impedance of the ballast must be larger than the magnitude of the negative resistance. In the case of a voltage source, the output impedance is close to zero by definition. One method to combat this is to use a positive resistor in series that is larger than the maximum magnitude of the negative resistance that could be encountered during operation. This would lead to stability with a voltage source, but would reduce efficiency of the ballast to a maximum of the lamp's positive resistance divided by the sum of the lamps positive resistance and the series ballast resistance. The alternative approach is to use a current source, which by definition has a high output impedance. In this manner, current is controlled, and the system will be stable.

2.3 Example LC_SC_P Ballast

One example HID ballast is the LC_SC_P resonant converter [30]. The ballast operates in resonant mode, and depending on the controller, can provide ignition, warm-up, and operation modes. In some converters, an external ignitor may be required to initiate the arc in the gas tube. The circuit topology is shown in Figure 2.2. The values are: L=190 µH, C_S=68 nF, C_P=1.5 nF, R=1500 Ω to simulate the lamp before ignition.

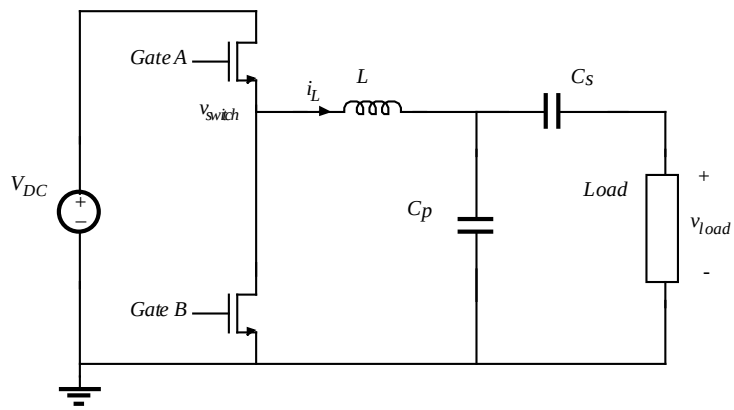


Figure 2.2: LCSCP Resonant Converter

Operation of the LC_SC_P converter is performed by applying complimentary gate drive signals at a 50% duty cycle, obtaining a sinusoidal output at the load. The amplitude of the output, and therefore power control, is obtained by operating the converter at different frequencies. A bode plot of the input-to-output transfer function as defined by $\frac{v_{load}}{v_{switch}}$ is shown in Figure 2.3.

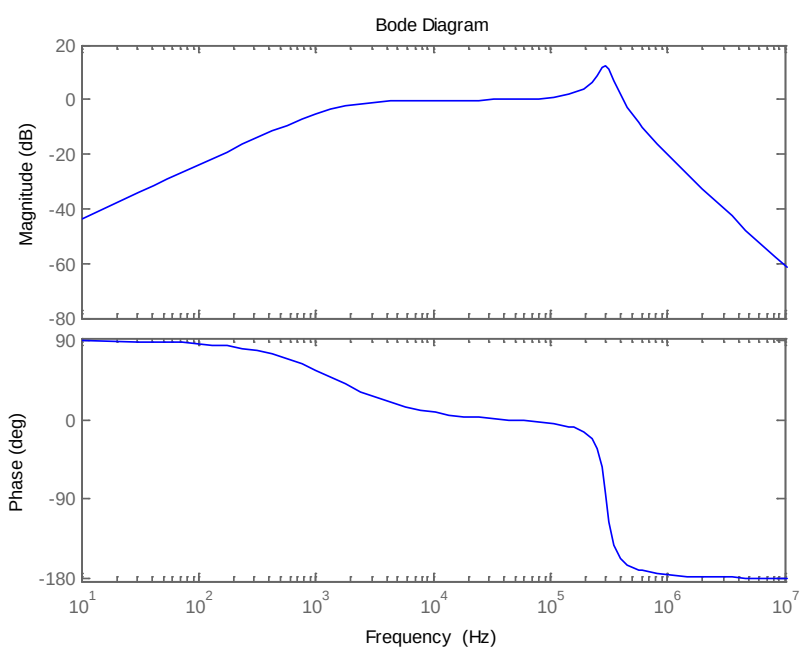


Figure 2.3: Bode Plot of Transfer Function of an LC_SC_P Resonant Converter

Alternatively, one can look at the input impedance of the converter to examine the converter operation. The input impedance is seen in Figure 2.4.

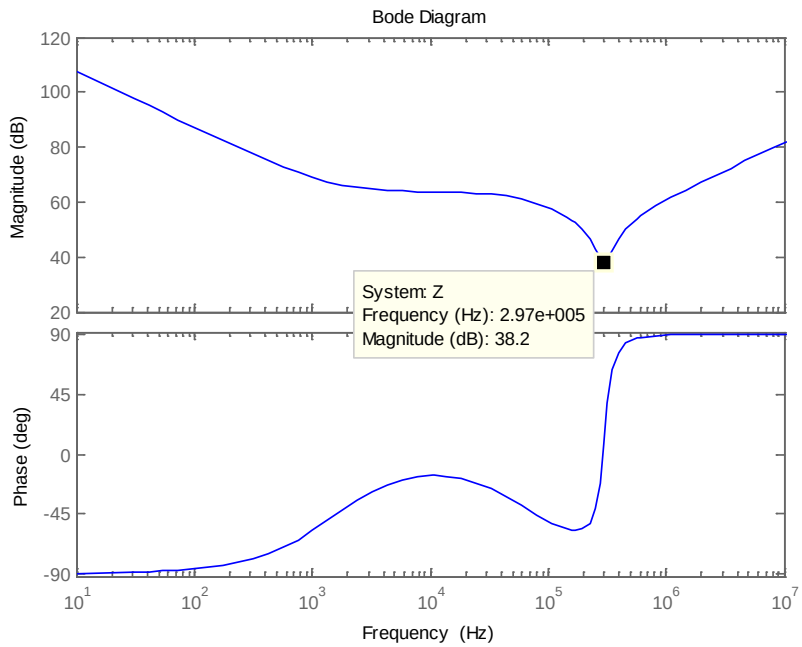


Figure 2.4: Input Impedance of an LC_SC_P Resonant Converter

What should be observed by the input impedance is that operation above resonance, or around 300 kHz for this particular converter, results in a positive phase, indicating an inductor quality. This also corresponds with operation in the Zero Voltage Switching (ZVS) region and thus has lower switching losses.

Methods for ignition include the aforementioned external ignitor circuit, but this topology also allows for a frequency sweep to ignite the lamp. If the operating frequency of the converter begins well above resonance, and goes down towards resonance, the voltage seen on the lamp will rise, as shown in the input-to-output transfer function. Assuming the *Q* factor of the converter is large enough to create a suitably large voltage to obtain breakdown in the lamp, an ignition will occur. Once ignition occurs, the lamp impedance, modeled by *R* in the circuit, will

drop from approximately 1500 Ω to around 10-150 Ω [2]-[6], [16], [17]. This change in input-to-output transfer function as defined by $\frac{v_{load}}{v_{switch}}$ is shown in Figure 2.5.

It should be noted that once ignition occurs, the converter output drops, and if the drop is significant enough, the lamp could extinguish. Operation in the warm-up phase and steady-state mode are both resonant, differing only in the fact that a power loop often controls the lamp power in the operation mode, once the lamp is warmed up. Operation of a lamp using a resonant mode can provide good performance, but a common issue in high frequency (above 6 kHz) operation of HID lamps is acoustic resonance.

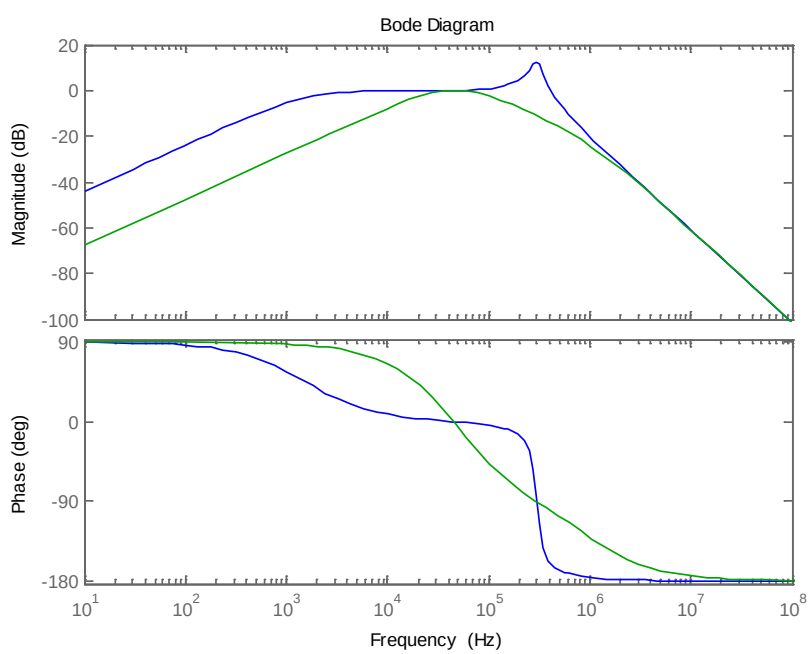


Figure 2.5: Input-to-output Transfer Functions of *R* = 1500 Ω (Higher *Q* factor, blue) and *R* = 100 Ω (Lower *Q* factor, green)

2.4 Acoustic Resonance

Gas discharge lamps are by nature, filled with a gas. This statement seems redundant, but the implications are great. When a closed vessel contains a gas, the ideal gas law comes to mind,

$$PV = nRT \,, \tag{2.2}$$

where P is the absolute pressure of the gas in Pascals, V is the volume of the gas in cubic meters, n is the number of moles of the gas, R is the gas constant 8.314472 $\mathrm{J{\cdot}K^{-1}{\cdot}mol^{-1}}$, and T is the temperature in Kelvin. An increase in temperature increases the pressure of the gas. Taken as a whole, an increasing temperature in a gas discharge tube does not pose a problem, assuming the tube is designed to withstand the increased pressure. The problem arises in the fact that if the tube is driven by a sinusoidal current or AC current, pressure waves could be introduced, and resonances may be present.

These resonances in pressure waves are called acoustic resonance [31]-[33]. The problems that stem from them can be as minor as a flickering light source which is unpleasant to the user, to lamp extinguishment, and even to catastrophic bulb failure if the pressure difference become so great as to overcome the physical strength of the bulb.

Acoustic resonance exhibits itself as standing waves in an arc tube as the sources of the disturbance emanate from the electrodes in the tube. Figure 2.6 shows an example of arc disturbance caused by acoustic resonance.

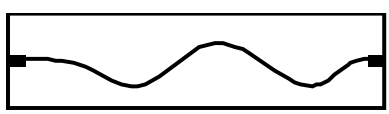


Figure 2.6: Example acoustic resonance in HID tube

Operation in a resonant mode, or more specifically, operation with power that exhibits a sinusoidal power waveform can excite these acoustic resonances. The frequencies in which acoustic resonance is exhibited depend greatly on the lamp arc tube geometry, gas mixture

in the tube, and initial pressure of the gas. Estimations of the problematic frequencies can be obtained through calculation. Because of the nature of harmonics of standing waves to exist in infinite frequencies above the fundamental, higher frequencies contain higher densities of possible problematic acoustic resonance regions for a given lamp arc tube design. Fortunately, higher harmonics also correspond with lower magnitude responses, resulting in less sensitivity in ultra-high frequencies. If an acoustic resonance free region is known, reliable operation with particular resonant ballasts can be achieved. Additionally, the resonance free region changes with lamp age, so a full lamp characteristic across possible lifetime must be known otherwise another solution must be presented.

2.5 Cataphoretic Phenomenon

One issue that has been mentioned previously is cataphoretic phenomenon. The basic problem is that since the gas discharge tube is filled with a metal salt, for example sodium ions, the tube is filled with charged particles. If one electrode exhibits a stronger tendency towards one polarity, the oppositely charged particles in the tube will migrate towards that side. This issue is mitigated with the use of either 50% duty cycle resonant converters, or LFSW type ballasts, as in these modes, both electrodes act as the cathodes and anodes an equal amount of time [34]. If a direct DC driven ballast were used, migration of the charged particles could lead to early lamp failure, uneven gas distribution leading to visible color differences in the arc, and other similar problems [2], [4], [7].

One example pertaining to cataphoretic phenomena includes the existence of Faraday dark space in DC driven lamps [35]. During normal operation of a lamp, there are various discharge regions. The largest region is usually the positive column. This region is closer to the

anode than the cathode, and separated from the anode by the anode sheath. On the opposite side of the positive column is a region called the Faraday dark space sandwiched between the negative glow region and positive column. The negative glow region is characterized by a drop in potential as distance increases from the cathode of the lamp. The Faraday dark space is a region that does not emit radiation, and occurs where the slope of the potential of the lamp goes from negative to positive going from the cathode to the anode. In practice, this dark spot is actually as the name suggests, and exhibits a break in the visible arc of the lamp. Visually this is detrimental to the value of the bulb, but does not directly harm the lifetime of the system. If the system were driven with an AC current, the Faraday dark space would be averaged out between the two current directions, and not be visible.

2.6 Electrode Sputtering

The electrodes in gas discharge lamps are commonly solid cylinders of tungsten. For ignition, especially with an open loop external ignitor element, excessive voltage can be introduced to the lamp electrodes, in which tungsten is evaporated from the electrode [3]-[6]. This disintegration is called electrode sputtering, and can cause an increase in arc tube breakdown voltage, as well as a physical blockage of light output when the metal is deposited to the outside of the lamp. This has been attributed to be the largest factor affecting light maintenance and lamp lifetime in HID lamps. Another cause of electrode sputtering is premature arc extinguishment. If the HID lamp is shutdown prior to obtaining full power, the tube would not have had enough temperature to vaporize the metal salts, resulting in a non-homogenous mixture of the metals inside the tube. If the arc is extinguished early, either by user choice, or

lamp arc failure, sputtering may occur. This motivates the requirement for a reliable startup and warm-up operation of an HID lamp.

2.7 Low-Frequency Square-Wave Ballasts

Since acoustic resonance is excited by a sinusoidal perturbance in lamp power, if the power contains no sinusoidal energy, acoustic resonance will be avoided. One solution to this is to drive the lamp with DC voltage. This operation must occur after lamp ignition, and a DC drive is usually employed after the warm-up period has ended, to aid in load stability. One method of operation is to create a low-frequency square-wave, in order to avoid cataphoretic phenomenon. Figure 2.7 demonstrates ideal waveforms of lamp current, voltage, and power.

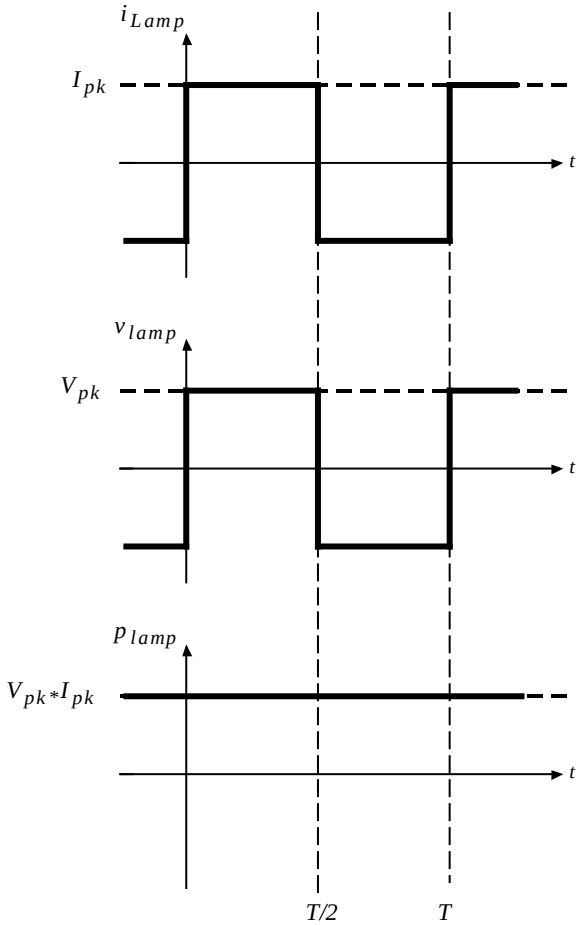


Figure 2.7: Ideal LFSW Waveforms Lamp Current (top), Lamp Voltage (middle), Lamp Power (bottom)

It can be seen that the lamp power is a constant value, assuming perfect switching. In reality, the waveforms will contain a small amount of sinusoidal harmonics, but through empirical testing, it has previously been found that if the harmonic power is below 5% of total lamp power, acoustic resonance is avoided [2].

3 Ignition of High-Intensity Discharge Lamps

3.1 Review of Lamp Ignition Concerns

One of the major portions of the design aspects for HID lamp ballasts is the ignition of the lamp. Unlike many other lighting alternatives, the ignition of HID lamps requires dramatically different conditions than the stable operating modes. Before an arc is established in either a Metal Halide (MH) or a High Pressure Sodium (HPS) lamp, the resistance of the lamp is in the order of 10-100 times larger than during operation. For a typical commercial MH or HPS lamp in the 150W to 400W range, this is usually represented by a pre-ignition impedance of around 1500 Ω, while during operation can take on a resistance of anywhere from 10-150 Ω.

Typical steady-state voltages of the lamp are around 100 V, while ignition voltages of approximately 3.5 kV are regularly recommended by lamp manufacturers. In order to achieve these high ignition voltages, ignition is usually obtained through use of an external ignitor circuit, or a resonant mode of the converter.

External ignitor circuits can come in the form of a capacitive discharge, a physical relay type spark gap on a high turns ratio transformer, or many other topologies. The drawbacks to external ignitors include higher parts count, a requirement to protect the steady-state circuitry that may not be otherwise designed to protect against the high voltages seen on the lamp for ignition, and an extra element to control adding to system complexity. An alternative to external ignitors is to use a resonant mode that may already exist in the lamp ballast topology.

A direct example of this is using either of the previously mentioned LC_SC_P or LC_PC_S ballast topologies. In this example, a resonant ballast is utilized in order to obtain a large voltage multiplication, while also allowing for reliable steady-state operation. By using the fact that the

lamp impedance is relatively high before ignition, an LC tank can be realized in the circuit, and thus, by operating near resonance of the LC pair, suitable ignition voltages can be achieved.

Some commercially available ballasts utilize these resonant circuits, but during ignition, the inductor sees overly high volt-seconds relative to the majority of its operation time. In order to have an inductor made of the most common materials that does not saturate during ignition, it is required to oversize the core as well as increase the air-gap. This translates directly to compromises in size, weight, and power loss. An improvement to this is to utilize a soft saturation material, instead of the more common hard saturation material that exhibits a more sudden drop off in the inductance when the volt-seconds exceed the allowable limits.

For comparison, a typical hard saturation core material (ferrite core) saturates around 4,000 gauss, while a soft saturation material such as the Kool-mu powdered cores can withstand around 10,000 gauss before full saturation is seen. In addition to the larger magnetic capacity than the ferrite cores, soft saturation cores provide a smoother transition of reduced inductance for a given DC bias. The larger saturation limit translates to decreased overall size and weight of the inductor, which is important as the inductor is one of the largest contributors to ballast size and weight. Figure 3.1 shows a comparison of a hard saturation core next to a soft saturation core designed for use in the same circuit.

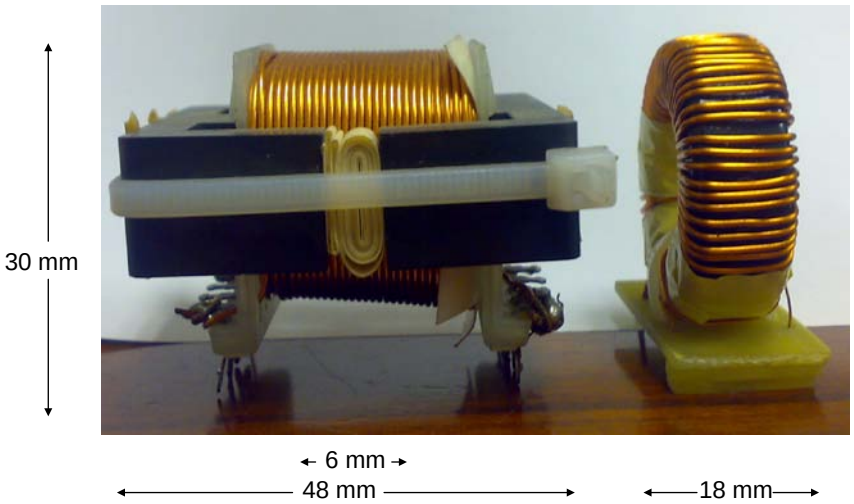
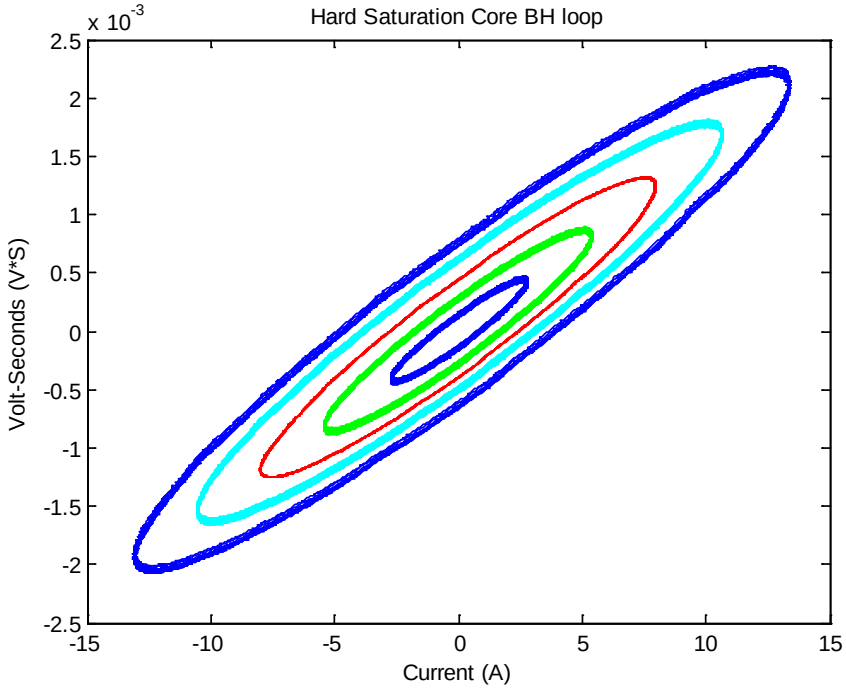
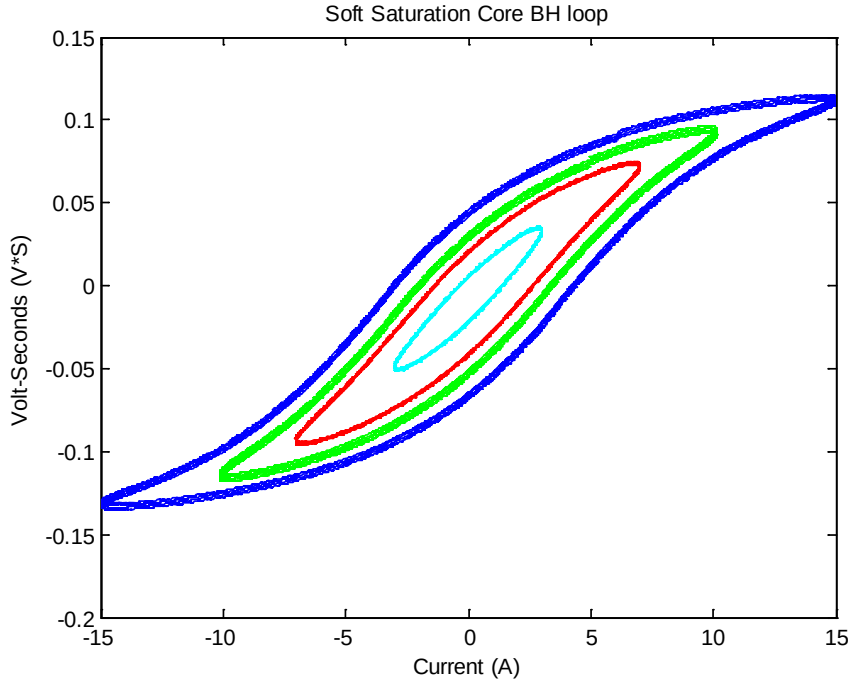


Figure 3.1: Size comparison of hard saturation core (left) and soft saturation core (right). The hard saturation core is 43 mm deep. Soft saturation core is 33 mm in diameter.

Figure 3.2 shows the BH loops for the hard saturation core operating in the non-saturating region and the soft saturation core BH-loop [36], [37]. Inductance is the slope of the curve at a given current. During one cycle, the operating point circulates counter-clockwise around the BH-loop. The different loop colors correspond to different peak currents. Measurements were taken at 1 kHz, in order to accentuate the loop areas. In practical application, the BH-loop areas, which correspond to core losses per cycle, are smaller, as the inductors are run at a higher frequency. Details on the measurement of BH loops using a standard oscilloscope with voltage and current probes is explained in Appendix C.



a)



b)

Figure 3.2:a) Measured BH loop for a hard saturation core. b) Measured BH loop for a soft saturation core.

3.2 Motivation for phase control

The drawback to using a soft saturation core is that the inductor exhibits a widely varying inductance given either a DC bias, or throughout a period of a resonant mode of operation in which the volt-seconds approach or exceed the knee of the BH loop of the particular inductor. For the example of using a resonant ballast, this means resonance for the LC pair varies with volt-seconds, meaning operation near resonance is difficult if only frequency control is employed. In order to insure operation above resonance while inputting a frequency command, thereby operating in the desired zero-voltage switching (ZVS) region, either extensive a priori knowledge of the circuit operation is needed or some external sensing is required. One method to mitigate this requirement is to input a phase command rather than a frequency command. Figure 3.3 shows an LC_SC_P converter schematic, along with its input-to-output transfer function Bode plot in Figure 3.4. The input-to-output is defined as $\frac{v_{load}}{v_{switch}}$.

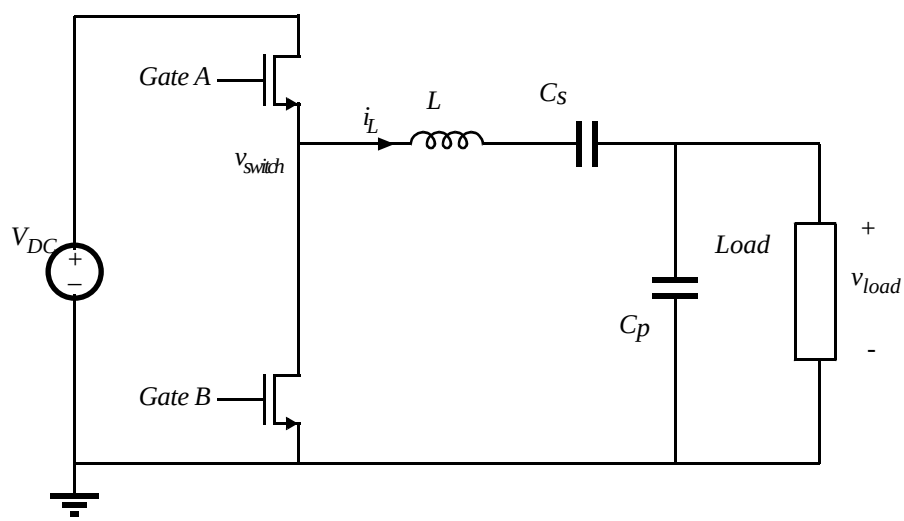


Figure 3.3: LC_SC_P converter schematic

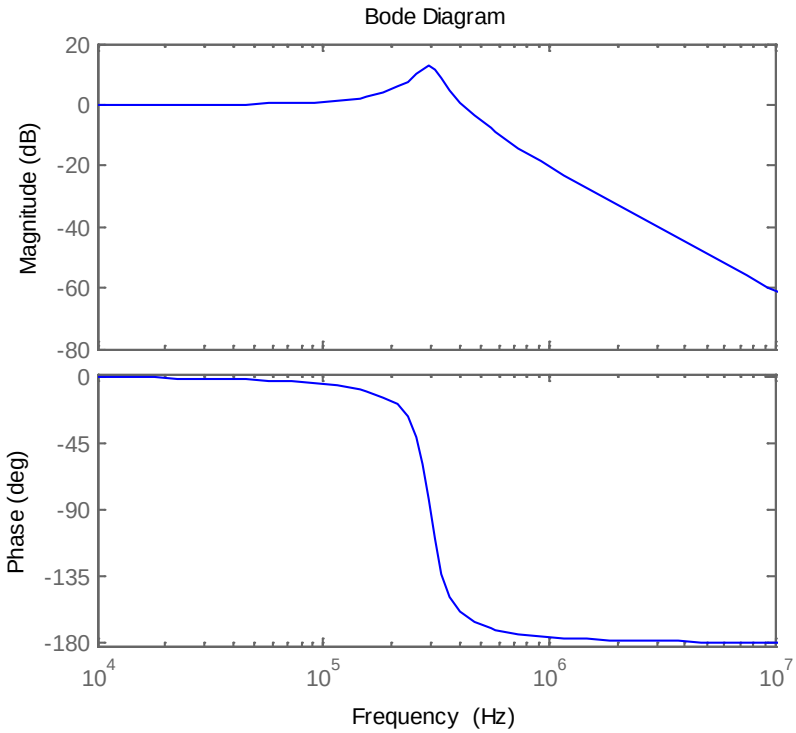


Figure 3.4: Typical pre-ignition input-to-output transfer function bode

A typical ignition with this type of ballast could be performed by sweeping the frequency from well above resonance, towards resonance until enough voltage gain is obtained to ignite the lamp. With a hard saturation core, knowledge of the resonant frequency can be used to set a lower limit on the frequency sweep, thereby insuring operation above resonance, but with a soft saturation core, the inductance varies throughout operation. Figure 3.5 shows different inductance values obtained from varying the incident current on the inductor, showing that with a varying inductance, setting a lower frequency limit can still create a non-ZVS situation.

One thing to note is that although the resonance changes with respect to frequency, the phase angle follows the resonance. This means that if a phase command is given, the phase can be limited to a range that guarantees ZVS operation.

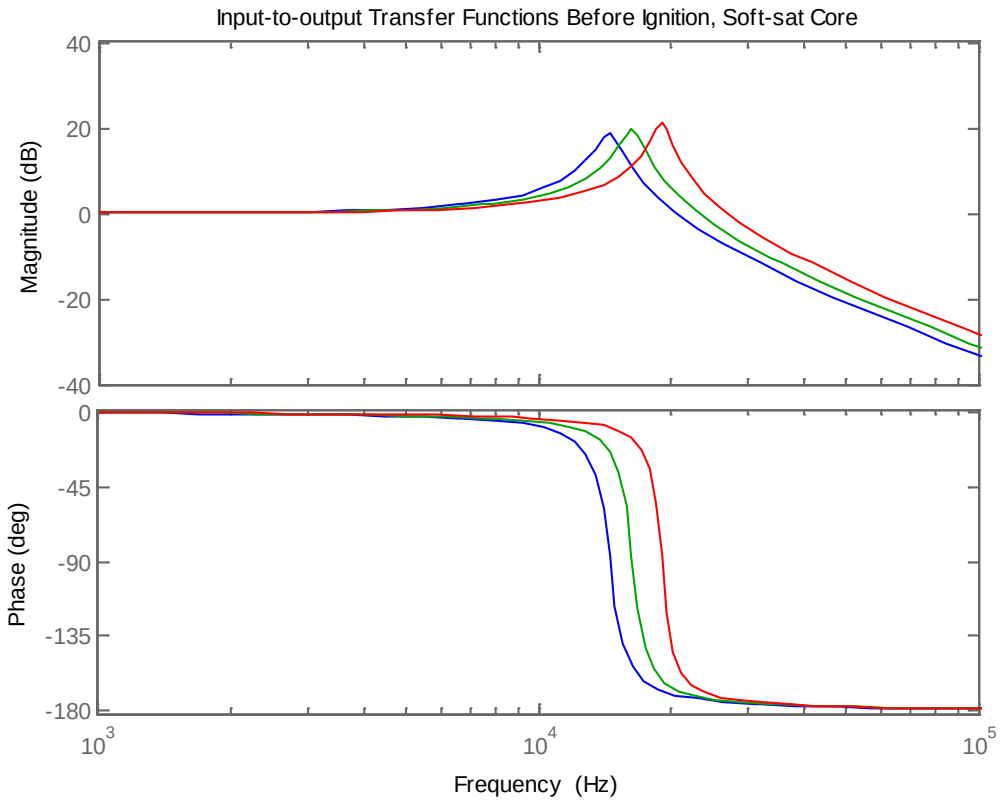


Figure 3.5: Resonant pair with varying inductance by ±50%. Larger inductance creates lower resonance

An added benefit of phase control over frequency control in resonant circuits with hard or soft saturation cores is that near resonance, resolution of a change in operation point is preserved with the phase control, while small changes in frequency near resonance results in exponentially larger reactions in voltage gain. A plot of pre-ignition input-to-output transfer function versus phase is shown in Figure 3.6, showing the smoother action a phase sweep provides.

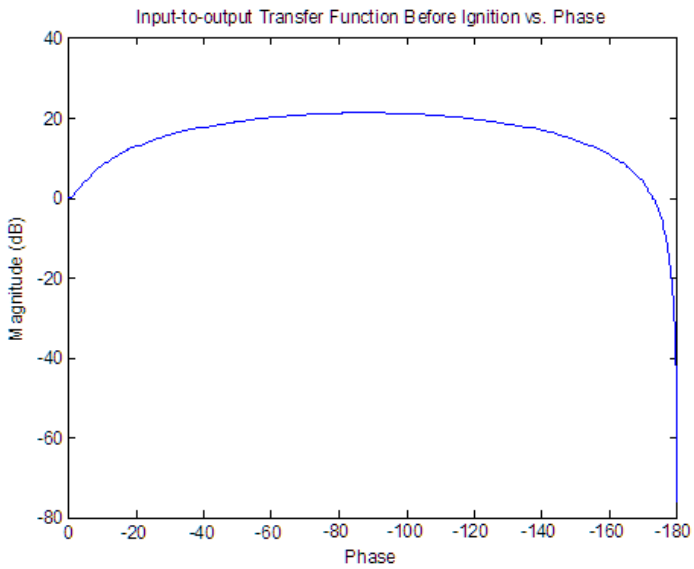


Figure 3.6: Pre-ignition input-to-output magnitude versus phase

3.3 Ignition Implementation

In order to demonstrate a soft saturation core HID ballast with resonant phase controlled ignition, a full bridge LC topology was selected in order to arrive at an acoustic resonance free steady-state operation as will be detailed in the next chapter. For the purpose of this chapter, the circuit shown in Figure 3.7 is operated in a resonant mode in order to achieve ignition of the lamp.

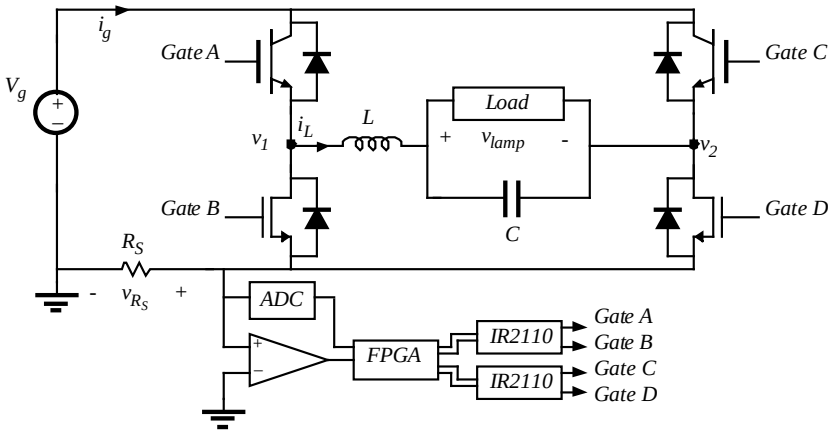


Figure 3.7: Full bridge LC lamp ballast schematic

In order to avoid building a DC bias, and operate the circuit in a resonant mode, a 50% duty cycle gate drive with suitable dead-time as seen in Figure 3.8 is used.

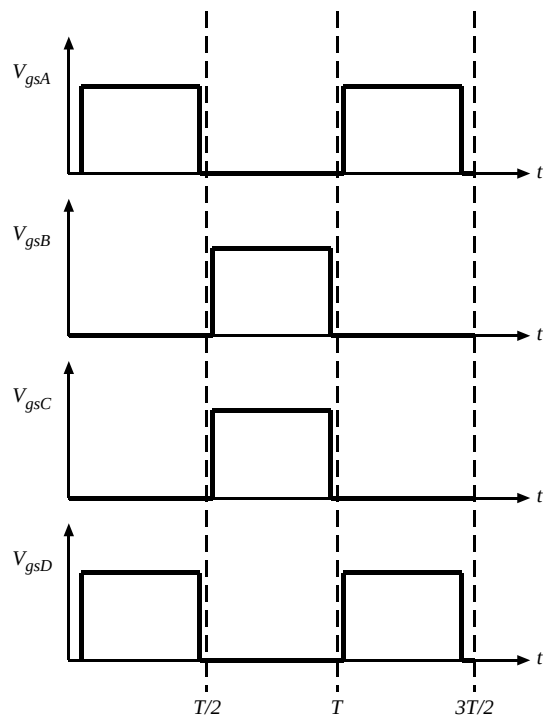


Figure 3.8. Gate signal waveforms for resonant operation

Basic circuit operation follows with the input-to-output transfer function of the LC resonant tank being:

$$G(s) = \frac{1}{s^2 LC + s\frac{L}{R} + 1}, \tag{3.1}$$

where R is the large signal lamp resistance. Using the fundamental approximation assuming a large Q factor and operating near resonance, the magnitude of the voltage incident on the lamp is

$$V_{lamp} = \frac{8}{\pi} V_{bus} \frac{1}{\sqrt{\omega^4 L^2 C^2 + (\frac{L^2}{R^2} - 2)\omega^2 + 1}}, \tag{3.2}$$

where ω is frequency in radians/sec. The resonant frequency in Hertz is

$$f_o = \frac{1}{2\pi\sqrt{LC}}, \tag{3.3}$$

and the corresponding Q factor is

$$Q = \frac{R}{2\pi \cdot f_0 \cdot L}. \tag{3.4}$$

The inductor used is 177 turns on a toroidal Kool Mu 77071 soft saturation core. The inductance at zero dc bias is 1.9 mH. The capacitor is a 63 nF ceramic capacitor that can withstand 1.6 kV.

As a design example [36], [37], an inductor that maintains 1.3 mH with a 1.4 A dc bias is designed using cores available from Magnetics®.

Step 1. Calculate the number of turns required to obtain inductance at zero dc bias using the estimated inductance per turns squared value. In this example, this is 146 turns.

Step 2. Calculate LI^2 in order to find an appropriately sized core, where L is the desired inductance in mH at the bias level I in amps. In this case, LI^2=2.55 mH-A^2. Using the Kool Mu Core Selection table [38], a suitable core above this level is found. For this example, core 77071 was chosen.

Step 3. The nominal permeability for this core is given as 61 nH/turn^2. This permeability will lessen due to the dc bias on the core. Calculate the magnetic field in Amp-Turns/cm using

$$H = \frac{NI}{le}, \tag{3.5}$$

where N is the number of turns in the initial inductor design of step 1, I is the bias current in Amperes, and le=8.14 cm is the magnetic path length of the selected core in cm. For this example, the result is 25.1 Amp-Turns/cm. Using the Permeability vs. dc Bias table [8] for the 77071 material, it is seen that the permeability is 82.5% of nominal at this bias.

Step 4. Increase the amount of turns in the core by dividing the turns found in step 1 by the permeability percentage. In this design, the new core number of turns is 177.

Step 5. Check the design by performing the permeability check once again. The new magnetic field is found to be 30.44 Amp-Turns/cm. This is found to have 76% of nominal permeability at the dc bias level. The new inductance at 1.4A dc bias is found to be 1.5 mH, which is above what is needed. The inductance with no dc bias is 1.9 mH.

For the designed inductor, with a 63 nF capacitor, the approximate pre and post ignition RLC tank impedances are shown in figure 3.8.

For a standard ignition, the phase command for the phase between the inductor current and the switching signals is swept from close to 90º towards resonance corresponding to 0º. In actual practice, ignition is obtained well before 0º as enough voltage gain is obtained prior to resonance in order to ignite the lamp. Once ignition occurs, the lamp impedance goes from around 1500 Ω to anywhere from 10-150 Ω. This drastic change in lamp resistance alters the transfer function, and

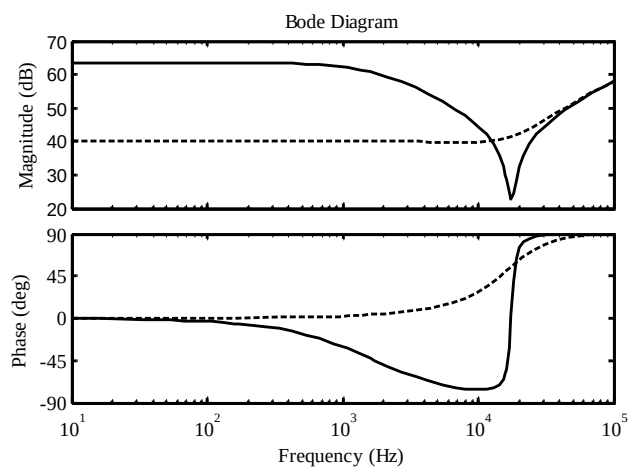


Figure 3.9: Impedance of the RLC resonant tank before (solid) and after (dashed) ignition

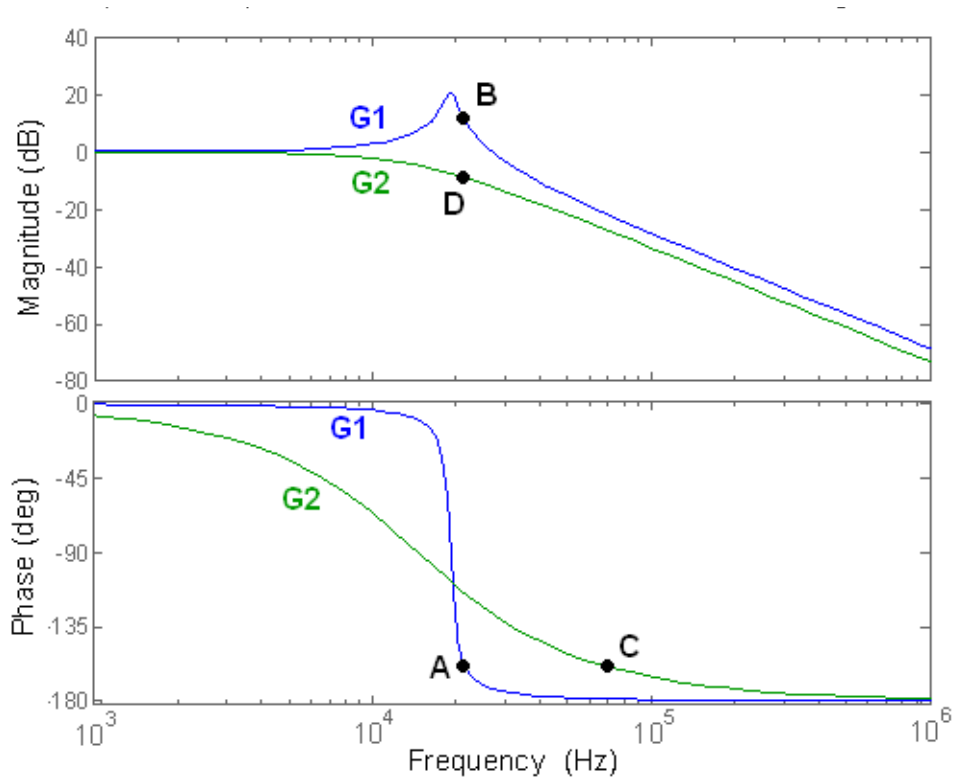


Figure 3.10: Control-to-output transfer functions before (G1, blue) and after (G2, green) ignition

provides a situation where hard switching no longer exists, as the lamp impedance overcomes the capacitance impedance.

For the case of the circuit in Figure 3.6, the pre and post ignition *Q* factors vary greatly, allowing for a situation where the operation point produces an operating frequency higher after ignition with a given phase command. If this change in frequency is too great, lamp extinguishment can occur due to the lamp not being driven with enough current to sustain the arc.

As an example, Figure 3.10 demonstrates a possible pre and post ignition control-to-output voltage transfer function assuming the pre ignition lamp impedance is around 1500 Ω, and the post ignition resistance is 100 Ω, and this example includes a soft saturation core inductor that changes effective value due to RMS current. The control signal is the

operating frequency, while the output is the load voltage. G1 represents the control-to-output of the pre ignition circuit, while G2 represents the post ignition transfer function. A typical phase sweep to ignition as presented in this chapter would consist of sweeping the phase of the inductor current to switching waveforms from around 90º towards 0º. Due to the high *Q* factor of G1, voltage multiplication can occur, allowing the circuit to create peak lamp voltages above the input DC voltage of the ballast. For this particular example, it is assumed that ignition occurs at point $B\angle A$, which is 22 kHz, and an inductor phase of 72º. This corresponds to a magnitude of 10 dB, or a voltage multiplication of 10. If the controller were to follow phase exactly, at the moment the lamp ignited, the operating point would transition to point C, possibly causing lamp extinguishment due to the drop in drive power.

One possible solution to this is to maintain the lowest frequency seen, which would lead to operation at point D, driving the lamp harder than operating point C. An additional benefit of this operation is that lamp ignition detection can be performed by monitoring this lamp impedance change [39]. If the current operating frequency is lower than the requested frequency due to phase control by a factor that is above possible noise, it can be said that the lamp impedance has been lowered, suggesting that the lamp has ignited. This can possibly save the designer from adding an additional sensing point of either lamp voltage or lamp current. During an ignition attempt, the resonant current in the circuit at the sense point for inductor current displays only the inductor current. Example waveforms for an ignition detection are shown in Figure 3.11. A fast ignition is with a constant frequency constraint is implemented as when

$$T_{phase}[n-1] > T_{phase}[n] + buffer, \tag{3.6}$$

then,

$$T_{delay}[n] = T_{delay}[n-1] + T_{phase}[n-1] - T_{phase}[n] \quad , \tag{3.7}$$

where *buffer* is a designed value that is small enough to detect the frequency shift from pre to post ignition lamp impedances, but large enough to overcome noise in the circuit.

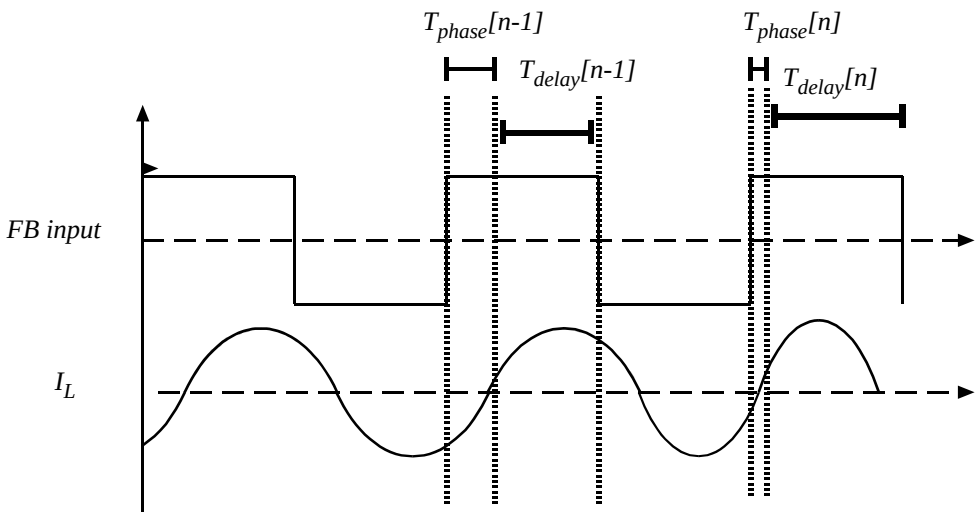


Figure 3.11: Ignition detection waveforms

When the lamp impedance is high (around 1500 Ω), the majority of the current going through the inductor is going across the capacitor that is in parallel with the lamp. Once ignition occurs, the lamp impedance drops below the capacitor impedance, allowing more current to go through the lamp. Another solution would be to create a current sensing point somewhere on the lamp, but this costs an additional sensing point. Alternatively, one could monitor the RMS current in the inductor, and watch for a drop in RMS current. This requires a priori knowledge of the lamp impedance, which decreases the universal nature of utilizing phase control for the ignition. A voltage sense on the lamp could also detect lamp ignition, but once again it is an additional sense point, as well as being a sense point that requires high voltage protection, and allows for suitable resolution in post ignition voltage levels which can be a factor of 100 less than the peak ignition voltages.

3.4 Digital Phase Control Implementation

Implementation of the phase control is performed by monitoring the zero crossing of the inductor current. This is performed with a comparator at the sensing resistor of the return leg outside of the full bridge. It should be noted that at this point, the positive zero crossing of the sense resistor voltage represents both the positive and negative zero crossing of the inductor current as it is defined in Figure 3.7. As such, a simple AND function with one of the gate signals can decipher which positive zero crossing is the correct one to measure for phase control. Figure 3.12 shows ideal waveforms for pre-ignition phase control. Control of the actual phase is performed by measuring the quantity demarked T_{phase} and controlling the quantity demarked T_{delay} [24]. Specifically, where $T_{percent}$ is the percentage of phase desired from 0-100% of 0 to 90º, *T[n-1]* is the period before *T[n]*, and m is the number of bits in the phase command,

$$T_{delay}[n] = \frac{T_{percent} \cdot T_S[n-1]}{4 \cdot 2^m} . \tag{3.8}$$

A simplified block diagram of the controller is shown in Figure 3.13. The state diagram can be seen in Figure 3.14. A frequency known to be well above resonance is first input by frequency control. This results in a very small voltage ripple on the lamp. Once an ignition is requested, phase control is initiated with a phase near 90º, which is swept towards resonance. Post ignition is maintained by a properly designed ballast.

The inductor designed is capable of operating the ballast in a resonant mode with the lamp ignited in order to achieve warm-up. Warm-up would continue for a specified time under a current envelope control before the ballast could switch to a Low-Frequency Square-Wave operation. An example of the ballast operation is shown in Figure 3.15.

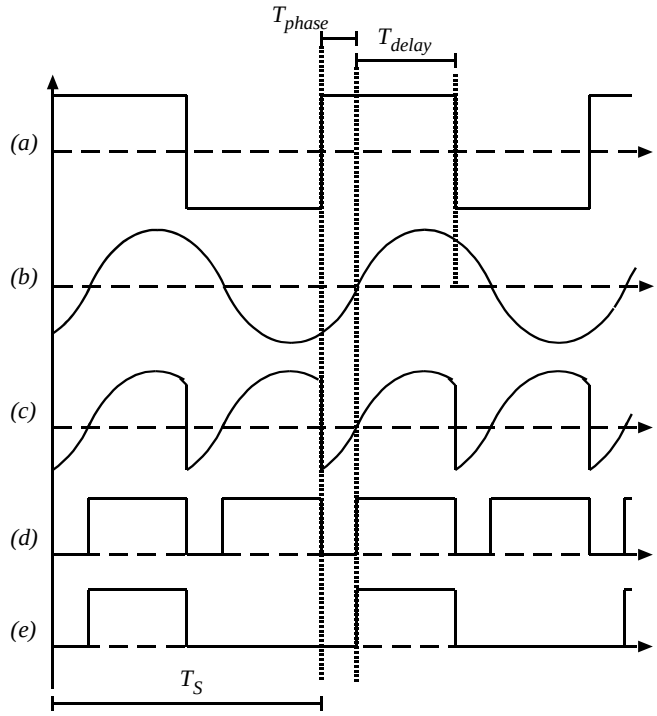


Figure 3.12: Example waveforms of interest. (a) Voltage incident on tank, v_1-v_2; (b) Inductor current, i_L; (c) Sensed voltage, v_{RS}; (d) Comparator output; (e) ANDed comparator output

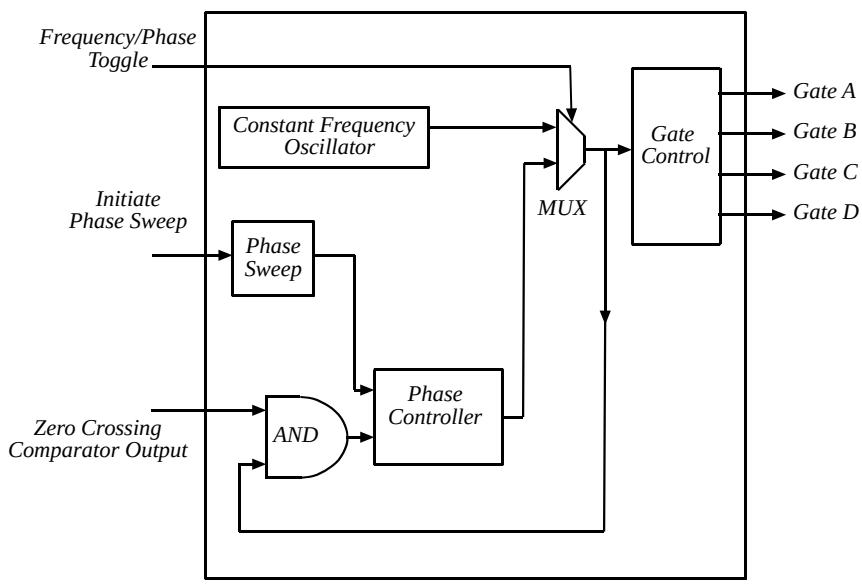


Figure 3.13: Simplified block diagram of the controller

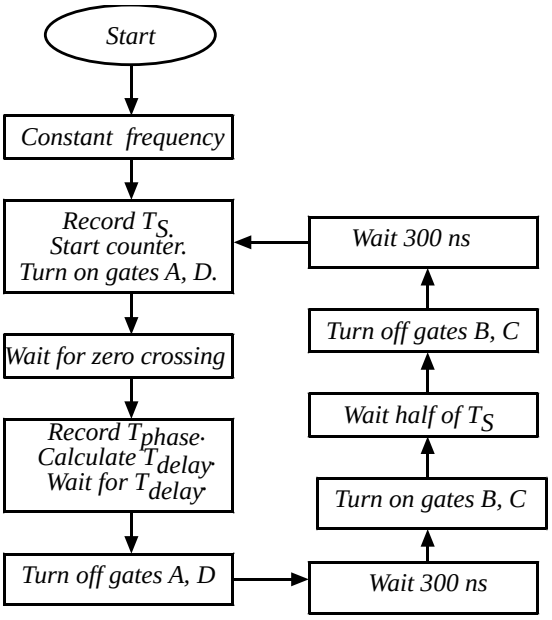


Figure 3.14: State diagram for phase control operation

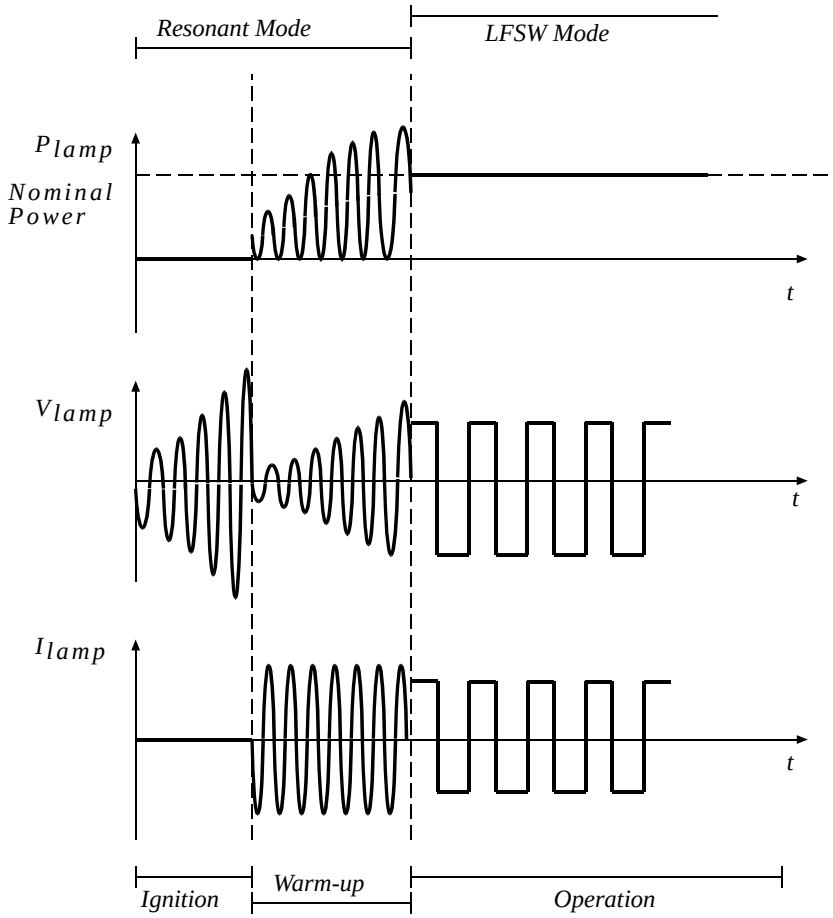


Figure 3.15: Resonant ignition and warm-up with LFSW steady-state

Resonant warm-up with a soft-saturation core inductor is susceptible to acoustic resonance if the operating frequency coincides with a vulnerable frequency of the lamp being driven. Additionally, the soft-saturation core may exhibit higher losses the further into saturation the core is allowed to go during operation. This necessitates the design of a larger core in some cases.

3.5 Summary

In this chapter, the ignition of HID lamps was explored. Examples of LC_SC_P ballasts and ballasts capable of resonant ignition as well as LFSW operation were presented. It has been shown that utilization of a soft saturation core material can provide a means of reducing overall converter weight and size, while allowing for operation of a converter in greatly different volt-second magnitudes. This presented itself in the design of the LFSW capable circuit with resonant ignition. A comparison of a hard saturation core designed to not saturate during lamp ignition was made to a soft saturation core inductor capable of ignition and steady-state operation.

A possible method of ignition detection was presented. This detection was an additional benefit to a control method that doesn’t allow the operating frequency to increase during a phase control sweep. The immediate benefit of this detection scheme is that an additional sense point is not required. Other ignition detection schemes using the preexisting sense points require a priori knowledge of the circuit operating conditions.

4 Warm-up and Low-Frequency Square Wave

Once a high-intensity discharge lamp has been ignited, the large-signal lamp impedance varies in value both in the short and long term time frame. At the moment of ignition, the bulb generally exhibits a resistance that is lower than the steady-state value. The bulb must go through a warm-up phase where the resistance changes and settles to the final value. For bulbs in the 150 W to 400 W range, this takes approximately five minutes to complete. On top of this, for a given bulb, the steady-state operation resistance that is finally reached can easily vary by a factor of three across the lamps lifetime. For a given power level of a group of bulbs, the variance can be even larger. In this chapter, warm-up and operation of Metal Halide (MH) and High Pressure Sodium (HPS) lamps in the 150 W power range are investigated. From empirical testing and reported values, it has been established that the expected resistances for the lamps are in the range of 10-150 Ω.

4.1 Circuit Topology

Considering full power in the lamp, using Ohm's Law, one can find the range of operational currents and voltages expected:

$$P_{lamp} = I_{lamp}{}^2 R_{lamp} = \frac{V_{lamp}{}^2}{R_{lamp}}, \tag{4.1}$$

The expected range of lamp voltage is

$$38.73\ V \le V_{lamp} \le 150\ V. \tag{4.2}$$

The expected range of lamp current is

$$1\ A \le I_{lamp} \le 3.87\ A. \tag{4.3}$$

One of the main obstacles in operating HID lamps is avoidance of acoustic resonance. The method that will be detailed in this chapter is the Low-Frequency Square-Wave (LFSW) operation. The basic idea is to avoid exciting acoustic resonances in the lamp by injecting low harmonic power content into the lamp. Ideally, a power signal of a DC nature would provide a clean signal with no harmonic content, but due to cataphoretic phenomenon, this is not feasible as the bulb would exhibit ionic separation, leading to excessive electrode degradation, uneven lamp ion density, Faraday dark spots, and uneven color distribution to name a few detrimental effects of a constant DC drive. The method chosen the avoid this issue is to operate with lamp voltage and current as in phase square waves, allowing for the power to ideally by constant, as shown in Figure 4.1.

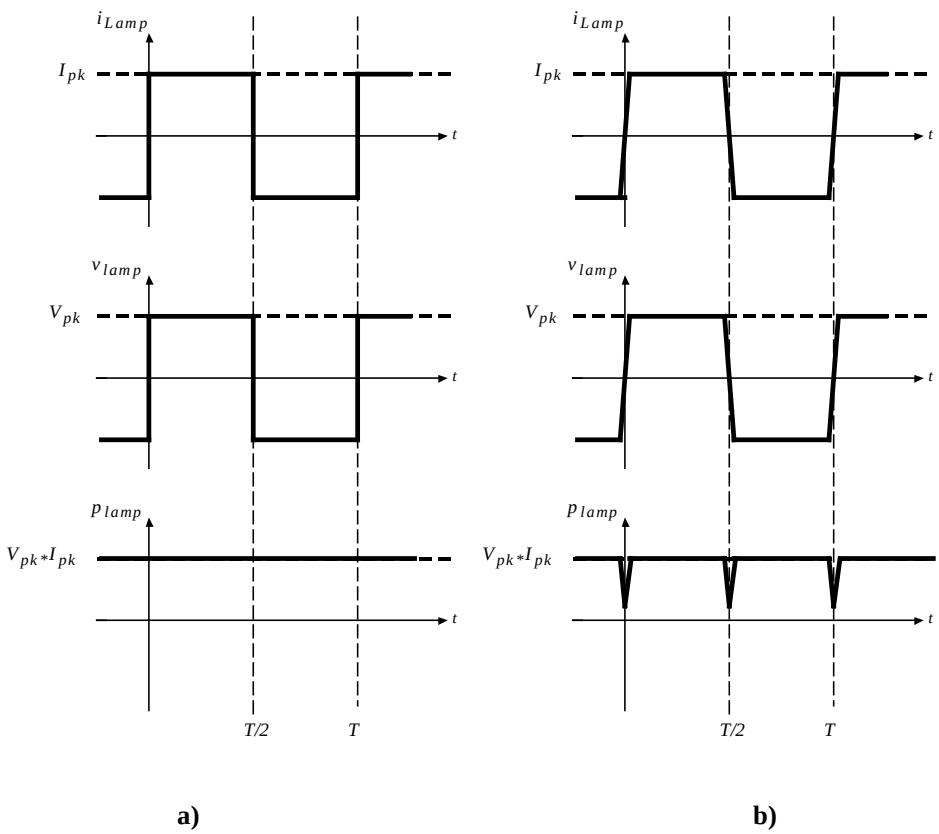


Figure 4.1: a) Ideal and b) Non-Ideal LFSW Waveforms Lamp Current (top), Lamp Voltage (middle), Lamp Power (bottom)

In actual implementation, the transition edges from a positive to negative mode cannot have infinite slope, and thus will exhibit harmonics in the lamp power, as demonstrated in Figure 4.1.b. It has been found that if the harmonic power is less than 5% of the total power, acoustic resonance is not observable by humans [32]. This suppression of harmonics in the power is the main design criterion for the ballast in steady-state operation. The topology chosen to obtain LFSW operation is the same as Chapter 3, but with a slight change to switching operation. The circuit is shown in Figure 4.2, along with the steady-state gate waveforms shown in Figure 4.3.

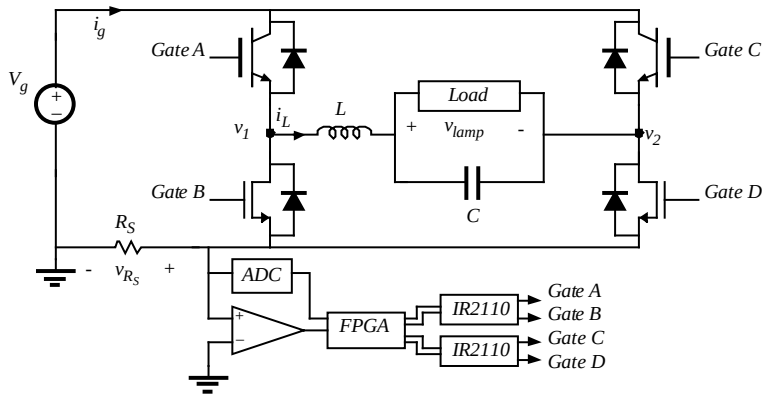


Figure 4.2: Ballast circuit capable of resonant ignition and LFSW operation

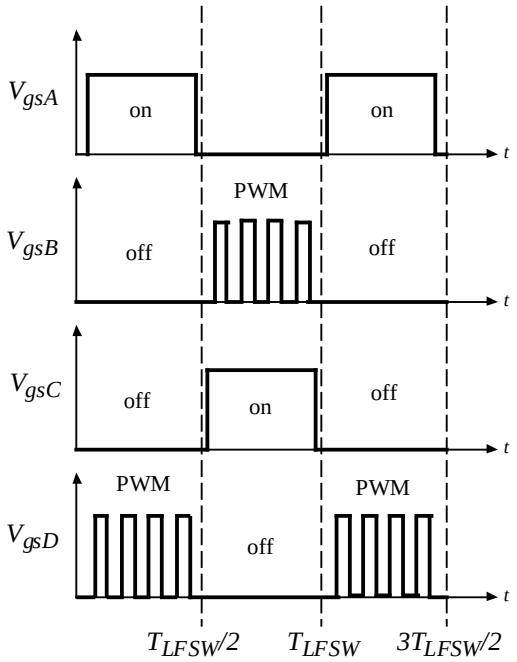


Figure 4.3: LFSW switch patterns

The basic steady-state operation of the converter is a hard-switched positive and negative buck converter. The inductor and capacitor can be thought of as a low-pass filter. The LSFW positive and negative buck mode current waveforms of the inductor and the input current are shown in Figure 4.4.

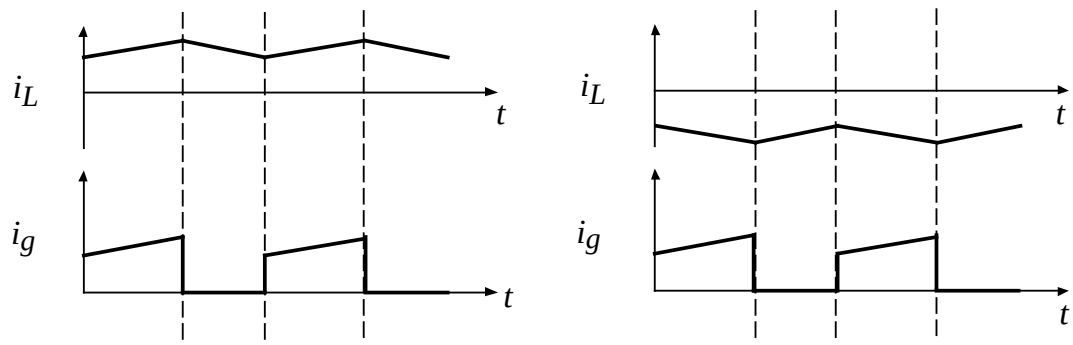


Figure 4.4: LFSW inductor current (top) and input current (bottom) or positive buck mode (left) and negative buck mode (right)

As an example of circuit operation, consider the positive buck mode. The current path during the on time of the PWM goes from the voltage source through switch A, through the buck filter, and through switch *D*, as shown in the Figure 4.5. In the off time, current circulates from the inductor through switch A and the anti-parallel diode of *C*, assuming constant current mode (CCM) operation. The diode in switch *C* is required, and since in this configuration, switch *C* is an IGBT, a diode must be added to the circuit. The IGBTs on the high side were selected for the higher breakdown voltages, and MOSFETs would not be able to handle to reverse current through their body diodes [40], [41]. Since there is no body diode in an IGBT, a more suitable anti-parallel diode can be selected for buck mode off time conduction. The low side MOSFETs were selected in order to allow for lower losses during the PWM action.

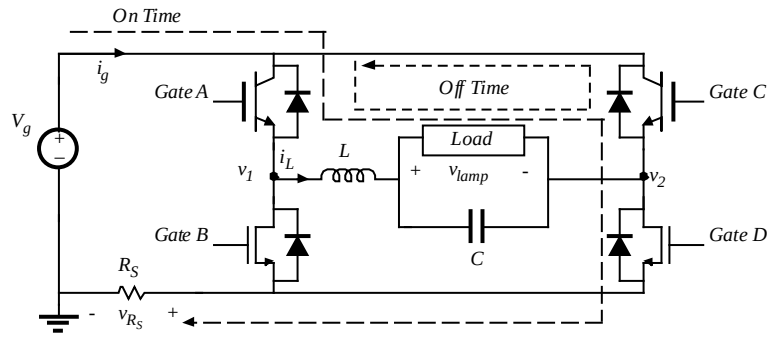


Figure 4.5: Positive buck mode current paths

Assuming CCM operation, the inductor gains a positive current, as defined in Figure 4.5, since in both the on and off times, the inductor has positive current. During the transition from positive to negative buck mode, this current in the inductor must reverse direction. While the current is positive, and the LFSW mode transitions to a negative buck mode operation, the current path in the converter is shown in Figure 4.6.

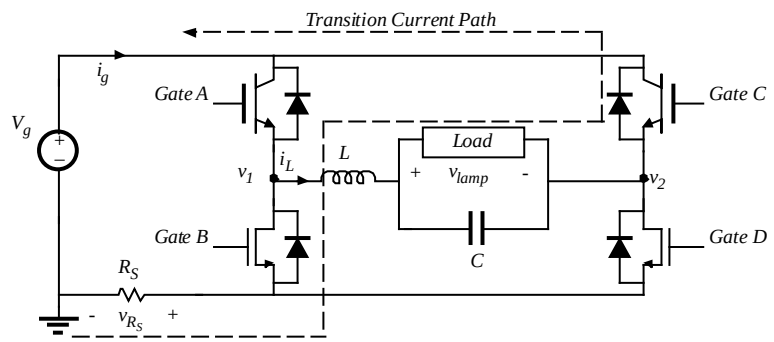


Figure 4.6: Current path during positive to negative buck mode transition

In this case, the anti-parallel diode of switch *C* is maintained forward biased until the current in the inductor reaches zero. Once this occurs, the converter can continue to operate as a negative buck converter.

4.2 Fast Buck Mode Transition

As can be seen in Figure 4.6, during a transition from positive to negative buck mode, the change in inductor current is at the maximum possible for a given input voltage while the body

and anti-parallel diodes of switches B and C are conducting. Alternatively, switches B and C can also be turned on instead of allowing the diodes to conduct. In either case, an effective duty cycle of 100% is seen on the negative buck converter configuration for this time regardless of the switch states of switches B and C. Effectively, the transition from positive to zero current in the inductor as defined in Figure 4.6 is the fastest it can be. Once the inductor current reaches zero and the diodes stop conducting, the transition from zero current to the negative current requested is controlled by the duty cycle the converter is operating at during that time. The transition time from zero to negative is controlled by the natural frequency of the buck converter, and the amount of overshoot or lack thereof is controlled by the *Q* factor of the buck filter response $\|G(jf_{sw})\|$,

$$\|G(jf_{sw})\| = \frac{1}{\sqrt{\left(1-\left(\frac{f_{sw}}{f_0}\right)^2\right)^2 + \frac{1}{Q^2}\left(\frac{f_{sw}}{f_0}\right)^2}} . \tag{4.4}$$

The *Q* factor is defined as:

$$Q = \frac{R_{load}}{L\omega_0} . \tag{4.5}$$

The faster the natural frequency, ω_0, the faster the transition, and a *Q* factor closer to 0.7 provides the least amount of overshoot or over-damping.

If the buck converter were operating in open loop, and the body diodes were not to conduct as explained earlier in this section, the transition would be wholly dependent on the *Q* factor and natural frequency. If the faster transition from the diodes is included, the transition is faster assuming the converter is not already operating at 100% duty cycle. With this is mind, it is a conservative design to design the converter to meet any transition speed requirements without

taking into consideration the diode action. In addition to the faster transition from positive current to zero current due to the diodes conducting, one can easily extend this to having a near optimal transition time by extending the conduction of current through switches B and C. This fast transition time can be obtained by monitoring the time it takes the current in the inductor to go from positive to zero, and copying this time to produce a similar current magnitude change from zero current to the steady-state negative current. This action is demonstrated in Figure 4.7 with the solid line showing the fast transition from positive to negative buck mode, while the dashed line shows a possible transition if switch B is not turned on for time T_{tran}. Switches B and C have the option of being turned on any time between the moment of the start of the transition and the zero crossing of the inductor current. In order to reduce stress on the body diode of the MOSFET and the external diode on the IGBT, and to reduce overall losses, it is elected to have the switches on rather than allow the diodes to conduct. There will still be a small amount of time the diodes conduct during the dead-time between the high and low-side switches of each leg of the full bridge.

It should be noted that this type of transition assumes the load resistance does not change during the transition. Additionally, it is assumed the inductance of the converter remains constant during the transition, which will become important if a soft saturation material is used.

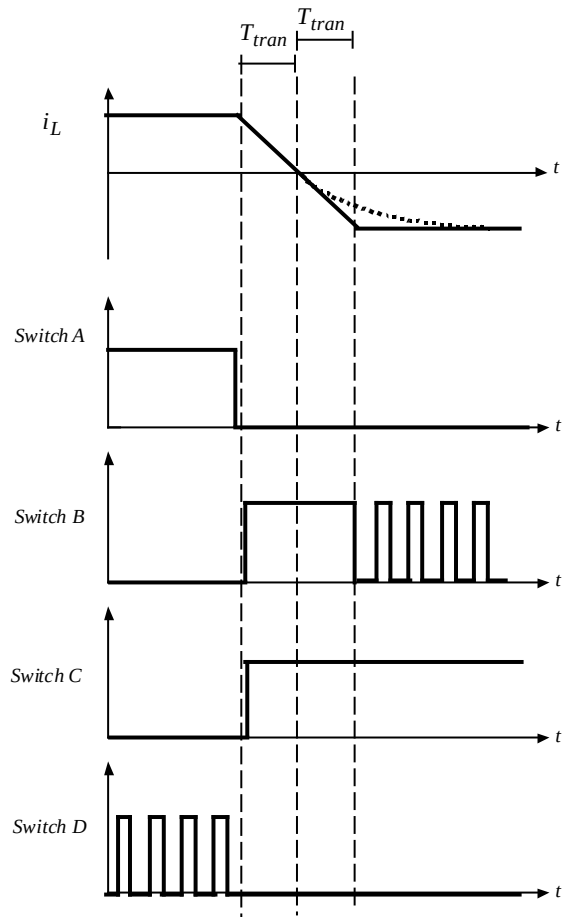


Figure 4.7. Near optimal transition from positive to negative buck mode.

4.3 Soft Saturation Core Inductor Concerns

As mentioned earlier, it is desired to design the circuit so that with LFSW operation, the harmonic power of any given frequency does not exceed 5% [32]. During operation, the buck converter produces an ac component at the switching frequency composed of:

$$V_{fsw} = \frac{4Vg}{\pi}\sin(D\pi) \quad . \tag{4.6}$$

If the fundamental approximation is assumed, the amplitude of the power due to this switching can be written as:

$$p_{lamp} = \frac{\left(DV_g + V_{fsw} \sin(\omega_{sw} t) \frac{1}{\sqrt{\left(1 - \left(\frac{\omega_{sw}}{\omega_0}\right)^2\right)^2 + \frac{1}{Q^2}\left(\frac{\omega_{sw}}{\omega_0}\right)^2}} \right)^2}{R_{load}} . \tag{4.7}$$

Looking at the ac component of the power, one obtains:

$$p_{fsw} = \frac{2DV_g V_{fsw}}{R_{load}\sqrt{\left(1 - \left(\frac{\omega_{sw}}{\omega_0}\right)^2\right)^2 + \frac{1}{Q^2}\left(\frac{\omega_{sw}}{\omega_0}\right)^2}} . \tag{4.8}$$

Using the assumption in [32] that if the magnitude of a power harmonic is less than 5%, the constraint

$$0.05 p_{lamp} \geq p_{fsw} . \tag{4.9}$$

Putting (4.7) and (4.8) into the inequality, one obtains

$$0.05 \frac{\left(DV_g + V_{fsw} \sin(\omega_{sw} t) \frac{1}{\sqrt{\left(1 - \left(\frac{\omega_{sw}}{\omega_0}\right)^2\right)^2 + \frac{1}{Q^2}\left(\frac{\omega_{sw}}{\omega_0}\right)^2}} \right)^2}{R_{load}} \geq \frac{2DV_g V_{fsw}}{R_{load}\sqrt{\left(1 - \left(\frac{\omega_{sw}}{\omega_0}\right)^2\right)^2 + \frac{1}{Q^2}\left(\frac{\omega_{sw}}{\omega_0}\right)^2}} . \tag{4.10}$$

The term

$$\left(\frac{V_{fsw}}{\sqrt{\left(1 - \left(\frac{\omega_{sw}}{\omega_0}\right)^2\right)^2 + \frac{1}{Q^2}\left(\frac{\omega_{sw}}{\omega_0}\right)^2}} \right)^2 \tag{4.11}$$

is considered small and is ignored, and the inequality results in

$$0.05\left(DV_g\right)^2 \geq \frac{2DV_gV_{fsw}}{\sqrt{\left(1-\left(\frac{\omega_{sw}}{\omega_0}\right)^2\right)^2+\frac{1}{Q^2}\left(\frac{\omega_{sw}}{\omega_0}\right)^2}}. \tag{4.12}$$

Redefining with (4.4)

$$\frac{0.05DV_g}{4V_{fsw}} \geq \frac{1}{\sqrt{\left(1-\left(\frac{\omega_{sw}}{\omega_0}\right)^2\right)^2+\frac{1}{Q^2}\left(\frac{\omega_{sw}}{\omega_0}\right)^2}}, \tag{4.13}$$

and substituting in (4.6),

$$\frac{0.05\pi D}{8\sin\left(D\pi\right)} \geq \frac{1}{\sqrt{\left(1-\left(\frac{\omega_{sw}}{\omega_0}\right)^2\right)^2+\frac{1}{Q^2}\left(\frac{\omega_{sw}}{\omega_0}\right)^2}}. \tag{4.14}$$

The next constraint to impose on the system is a maximum Q factor. By imposing a maximum Q factor, the amount of overshoot in transients can be limited, reducing the overall harmonic power introduced into the lamp. If a constant inductance is assumed, the Q factor follows (4.5). As in chapter 3, a soft saturation core inductor will be used in this converter, so a constant inductance cannot be assumed. Additionally, it is desired to keep the Q factor around 0.7 as previously mentioned, and given the large load variations allowed in this design example (10-150 Ω), the Q factor would vary by a factor of

$$\frac{Q_{\min}}{Q_{\max}} = \frac{\frac{R_{\min}}{L\omega_0}}{\frac{R_{\max}}{L\omega_0}} = \frac{R_{\min}}{R_{\max}} \quad . \tag{4.15}$$

In this design example, that would translate to a range of Q factor from 1.2 to 0.08. The 0.08 is very over-damped, and would cause too much harmonic power during transitions between buck modes in the LFSW operation. A benefit of the varying inductance of the soft saturation core material is that as the load resistance is larger, the current to obtain the same power must be lower, obtaining a higher inductance, resulting in a stabilizing effect on the range of Q factors across load changes.

Rewriting (4.15) with varying inductance in mind assuming a constant capacitance, one obtains

$$\frac{Q_{\min}}{Q_{\max}} = \frac{\frac{R_{\min}\sqrt{L_{\min}C}}{L_{\min}}}{\frac{R_{\max}\sqrt{L_{\max}C}}{L_{\max}}} = \frac{\frac{R_{\min}\sqrt{L_{\min}}}{L_{\min}}}{\frac{R_{\max}\sqrt{L_{\max}}}{L_{\max}}} = \frac{\frac{R_{\min}}{\sqrt{L_{\min}}}}{\frac{R_{\max}}{\sqrt{L_{\max}}}} \quad . \tag{4.16}$$

With a given soft saturation core, the relative permeability is decreased as the current times turns increases. An example of a specific core (Kool Mu 077356A7) is shown in Figure 4.7.

The equation the curve fits as supplied by the manufacturer [38] follows:

$$\mu_r = A + B \cdot H + C \cdot H^2 + D \cdot H^3 + E \cdot H^4 , \tag{4.1}$$

where A = 1, B = -2.8x10^{-3}, C = -3.0x10^{-5}, D = 2.0x10^{-7}, and E = -3.0x10^{-10}. Equation (4.16) is valid from $H = \{1 - 150\}$, where H is the DC magnetizing force in ampere turns per cm.

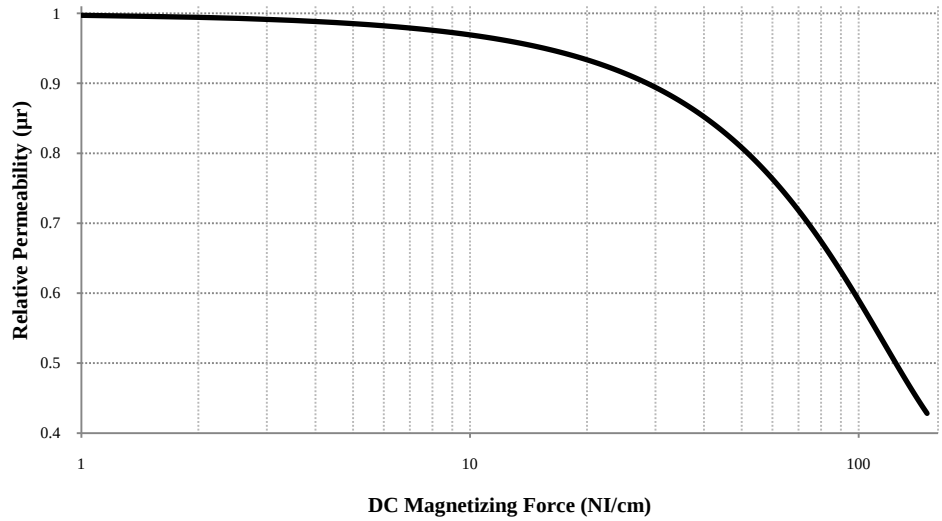


Figure 4.7: Relative Permeability vs. DC magnetizing force of Kool Mu 077356A7 core

For an initial design check, it can be seen that the relative permeability change allowed for the information available is a permeability of 45% to 100%. This assumes the design of the inductor utilizes the full range of reported permeability. Using (4.16), the smallest change in *Q* factor allowed is

$$\frac{Q_{\min}}{Q_{\max}} = \frac{\dfrac{R_{\min}}{\sqrt{L_{\min}}}}{\dfrac{R_{\max}}{\sqrt{L_{\max}}}} = \frac{\dfrac{10}{\sqrt{0.45}}}{\dfrac{150}{\sqrt{1}}} = 0.0994 \quad (4.2)$$

.

This translates to a *Q* factor change in the order of 10 times, which is much better than the 15 times required by the constant inductor. It should be reiterated that this is the maximum *Q* factor change suppression this core allows for the information given by the manufacturer. If the DC magnetizing force to relative permeability of a core is known to even lower percentages, the amount of *Q* factor range suppression can be arbitrarily good. For example, if the minimum permeability percentage were allowed to go to 5% of the nominal permeability which is

reasonable to expect, a Q factor spread of a factor of only 3.35 can be achieved. In order to generalize the design method more, one can see that

$$\frac{Q_{\min}}{Q_{\max}} = \frac{\dfrac{R_{\min}}{\sqrt{L \cdot \mu_{\min}}}}{\dfrac{R_{\max}}{\sqrt{L \cdot \mu_{\max}}}} = \frac{\dfrac{R_{\min}}{\sqrt{\mu_{\min}}}}{\dfrac{R_{\max}}{\sqrt{\mu_{\max}}}} . \tag{4.3}$$

Solving for the ratio of permeability range,

$$\frac{\mu_{\min}}{\mu_{\max}} = \left(\frac{Q_{\min}}{Q_{\max}} \frac{R_{\max}}{R_{\min}} \right)^2 . \tag{4.4}$$

From (4.19) and (4.20), a first pass can be made to decide on core material requirements for the inductor core. It should be kept in mind that this merely checks the minimum and maximum values, and since the permeability curve is not linear across the values used, values between the minimum and maximum load resistances can be outside these values. It is recommended to do a full parametric study once the initial core is decided upon. Linear regression lends itself nicely to finding the best suitable core if given a choice between many specified cores.

4.4 Converter LC design example with soft saturation Core

As a design example, a large-signal lamp impedance of 10-150 Ω is assumed for HID lamps with a 150 W power rating. The input voltage for this design is $V_g = 200V$. A switching frequency of 200 kHz is chosen as it is in the upper limit of commercially available hard-switching converters with today's technology. This is due to the fact that higher frequencies generally lead to less of a benefit and lower efficiency due to switching losses. Using (4.14), the

buck filter response required to obtain less than 5% harmonic power due to the switching is found to be -27 dB for the upper limit of (4.14). A conservative solution is to assert

$$\|G(jf_{sw})\| < -40\ dB \quad (4.5)$$

Imposing (4.21) on (4.14) arrives at

$$\omega_{sw} = 10\omega_0, \quad (4.6)$$

with

$$\omega_{sw} = 2\pi \cdot 200krad/s, \quad (4.7)$$

the maximum corner frequency considering the variable inductance due to the soft saturation core is 20 kHz from (4.22).

Using (4.5), and a maximum desired Q factor of 1.2, a first iteration design of inductance places it at around 1 mH. Using

$$\omega_0 = \frac{1}{\sqrt{LC}}, \quad (4.8)$$

one obtains $C = 63nF$. As discussed earlier, with a hard saturation core inductor, the design process would be over, albeit with a very large range of Q factors. The next step in the design process involves balancing the relative permeability vs. DC magnetizing force of various cores in order to find a fit that reduces the variance of the Q factor. The first step is to choose the core material. This involves obtaining the relative permeability vs. DC magnetizing force equations for various materials supplied by a manufacturer, and setting constraints on the desired cores. For the manufacturer chosen in this study, the online data was trustable to around 45% of relative permeability, translating to a Q factor range change of around 33% as compared to a hard

saturation core material. This was deemed acceptable, although with data going to lower relative permeabilities, the *Q* factor suppression could be improved even more as described in the earlier sections. For this design, the most linear region (as based on a linear regression curve fit to the data available) for the approximate DC magnetizing force to be used on the inductor was found to be the Kool Mu 40µ material. Figure 4.8 demonstrates the linearity of the inductance versus current through the inductor. The linear regression on the linear curve fit was 0.9968 showing a very strong linearity of this region.

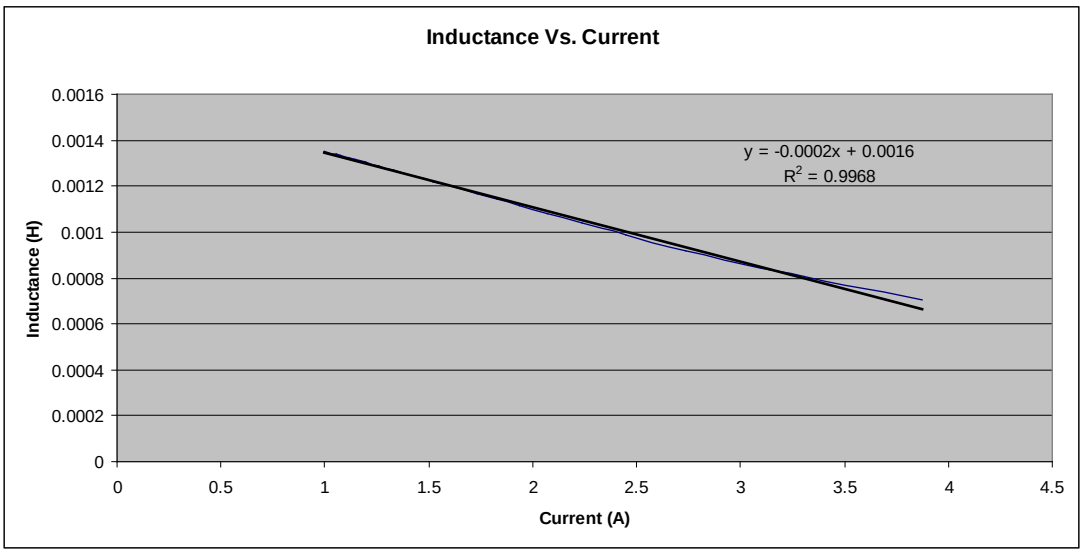


Figure 4.8: Inductance vs. Current on the designed Kool Mu 077356A7 toroidal inductor

With the core material selected, a parametric design search was performed on available cores of that material. The search was programmed to look for the combination of turns and magnetic path length that produced a Q_{max} of 1.2 across all operating loads, a DC magnetizing force that was less than the range the equation supplied by the manufacturer is valid until (150 Ampere turns per cm), and was set to minimize the spread of *Q* factors for all operating conditions. In the parametric search, the maximum inductance and capacitance was allowed a 20% tolerance while keeping the constraint of a natural frequency max of 20 kHz. Having a

lower natural frequency slows the transition between buck modes, but improves the power harmonic ripple due to the switching action of the buck converter.

From the parametric design search, it was found that a Kool Mu 0077356A7 core, which is a toroidal 40μ core from Magnetics Inc. was suitable for the design with a 5.88 cm magnetic path length. A capacitance of 57 nF was also found to be suitable for this application. The inductor consisted of 214 turns. The inductor designed produced a 1.35 mH inductance with a 1 A DC bias, which is important as this is the operating condition with maximum load resistance, or 150 Ω. When the lamp resistance is at its minimum of 10 Ω, the current through the inductor is 3.87 A, resulting in an inductance of 0.7 mH. The *Q* factor exhibits a spread of 10.8, which is close to the theoretical design minimum with the data available. This is compared to the factor of 15 that would be present if a hard saturation core was used. The newly designed inductor with soft saturation core material was 30 g total weight. A comparable hard saturation core inductor designed to not saturate during lamp ignition, and have similar DC resistance was found to be 300 g, resulting in a weight improvement of 90% reduction in weight.

4.5 Compensator Design

A two loop design is employed in order to obtain a fast inner loop current regulation for arc stabilization, while a slow outer power loop regulates the power in the lamp. The inner loop provides a fast current regulation intended to account for the lamp's negative incremental resistance at lower frequencies, thereby providing in essence, large signal impedance stabilization. The target crossover frequency for the inner loop is around 10 kHz, which was chosen to be above the negative incremental impedance of most HID lamps in the 150 W power level. The inner loop topology is a PI compensator, chosen because the integral action removes

all steady-state error, which is important during warm-up, as it is intended that the lamp be driven at the maximum current allowable during this time. As such, the current reference will be railed at its maximum which will be near the converter maximum in certain operating points, and any steady-state error could lead to undesirable operation or even lamp failure. An example operation of an HID ballast driven in DC is shown in Figure 4.9. This example ignores LFSW mode changes, and assumes all current is in one direction. It demonstrates current limiting during warm-up and power control during the end of warm-up and throughout operation.

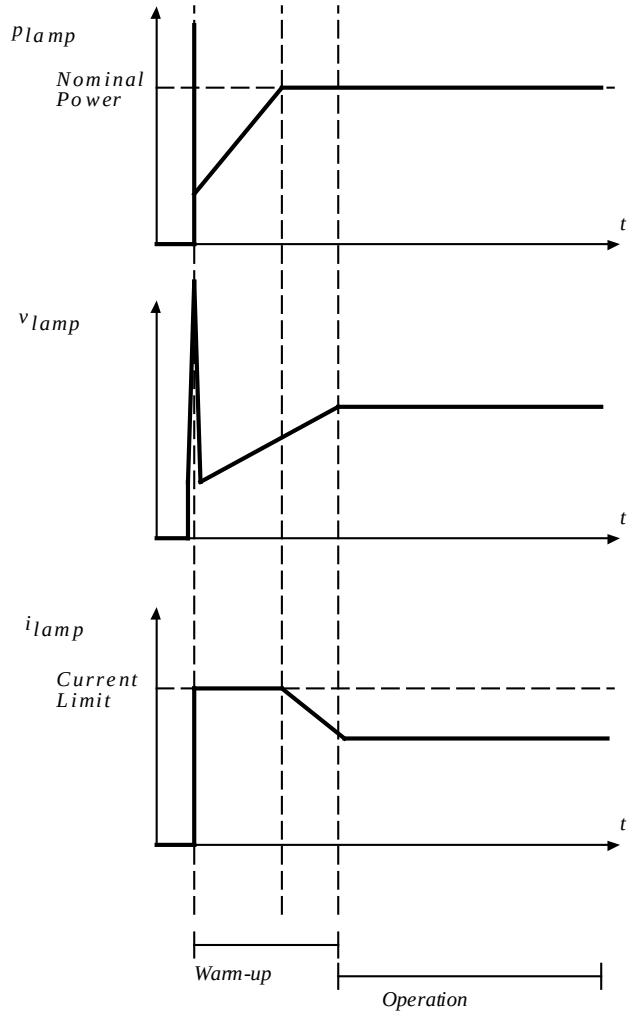


Figure 4.9: Operation modes of a DC lamp ballast

The outer loop is a slow integrator compensator designed to control the input power of the ballasting circuit. The outer loop is used to account for variations in the lamp resistance due to lamp aging and variations between lamp brands and types, as well as possible variations in the input voltage to the ballast (ie the output voltage of the PFC). The bandwidth of the outer loop is constrained to be at least a factor of 10 slower than the inner loop in order to avoid interference, and must be faster than the frequency in which the lamp resistance changes, which is in the order of minutes. During transition between buck modes, the converter operates in open loop with whatever duty cycle was last used before the transition, in order to simplify the transition. The open loop time was programmed to be 3 time constants of the lowest natural frequency the converter will operate with, considering the varying inductance.

The controller was designed assuming the buck operated in one mode (positive for simplicity) as shown in Figure 4.10.

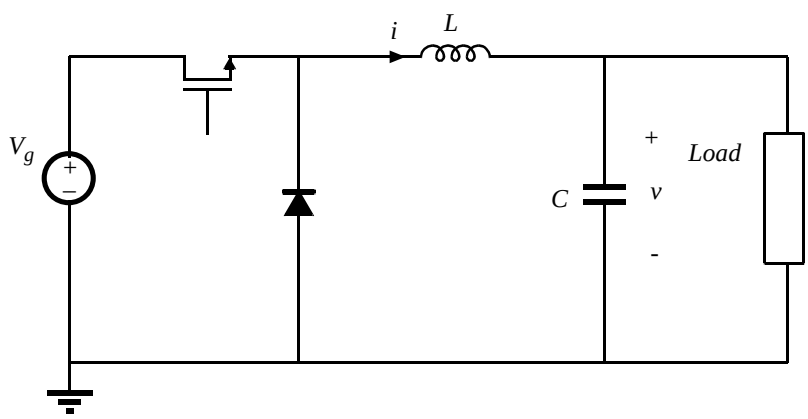


Figure 4.10: Standard buck converter

The discrete time model of the converter was created using the methods in [42]. Using the state-space description

$$\begin{aligned} \dot{x} &= A_i x + b_i Vg \\ y &= C_i x + e_i Vg, \quad i = \{1,2\} \end{aligned}, \tag{4.1}$$

where x is the converter state vector as defined

$$x = \begin{bmatrix} i \\ v \end{bmatrix}. \tag{4.2}$$

Ignoring capacitor ESR and assuming the indictor resistance is small, the converter is defined as:

$$A \approx \begin{bmatrix} 0 & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{CR} \end{bmatrix} \tag{4.3}$$

$$b = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \tag{4.4}$$

$$C \approx \begin{bmatrix} 1 & 0 \end{bmatrix} \tag{4.5}$$

$$e = \begin{bmatrix} 0 \end{bmatrix} \tag{4.6}$$

$$y = i_{out} \tag{4.7}$$

$$\hat{x}[n] = \Phi \hat{x}[n-1] + \gamma \hat{d}[n-1] \tag{4.8}$$

Where

$$\Phi = e^{AT_s} \tag{4.9}$$

$$\gamma = e^{A(T_s - t_d)} b V_g T_s, \; 0 \le t_d \le T_s, \tag{4.10}$$

where

$$t_d = D \cdot T_s + t_{d1} + t_c + t_g, \tag{4.11}$$

where t_{d1} is the delay of the ADC, t_g is the gate switching delay, t_c is the computation delay, and $D \cdot T_s$ is the actual sampling time occurrence. Additionally

$$\hat{y}[n] = C\hat{x}[n]. \tag{4.12}$$

From this, the control-to-output in terms of current in the discrete case is given as

$$G_{id}(z) = \frac{\hat{i}_{out}}{\hat{d}}. \tag{4.13}$$

A comparison between the Laplace transform method and the discrete small signal model is shown in Figure 4.11 and Figure 4.12. The continuous time model is similar to the discrete time model except for the phase. This is as expected, and affects the design of the compensator by altering the crossover frequency slightly. The control-to-output transfer function for the continuous case is found from the small signal model of the buck converter. The continuous control-to-output transfer function from duty cycle to voltage is

$$G_{vd}(s) = \frac{\hat{v}_{out}}{\hat{d}} = V_g \frac{1}{1 + s\frac{L}{R} + s^2 LC}. \tag{4.14}$$

Since the measurement occurs at the sense resistor, the capacitor must be included in the calculation for output current, as seen by the controller. In this case, the control-to-output function in terms of output power related to duty cycle for the system in the continuous time domain is

$$G_{id}(s) = \frac{\hat{i}_{out}}{\hat{d}} = V_g \frac{1 + sCR}{1 + s\frac{L}{R} + s^2 LC}. \tag{4.15}$$

More details can be found in Appendix B.

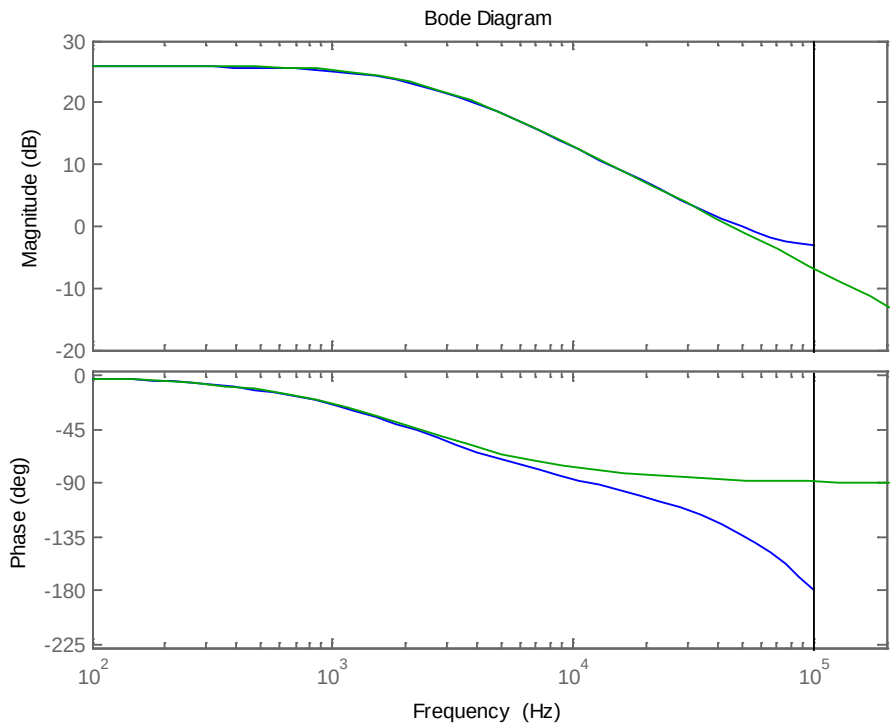


Figure 4.11: Continuous small signal mode (green) and Discrete small signal model (blue) of control-to-output current for R=10 Ω

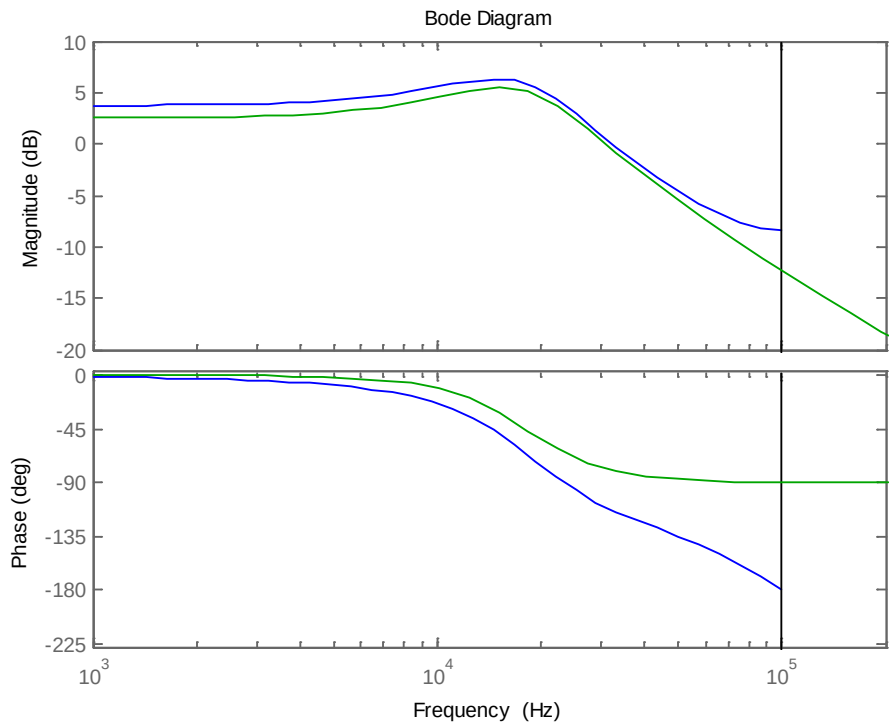


Figure 4.12: Continuous small signal mode (green) and Discrete small signal model (blue) of control-to-output current for R=150 Ω

The models for the lamp impedance do not include the low frequency effects, and therefore are not valid below the frequency where the lamps incremental impedance is negative. The transfer functions presented are only valid where the small signal lamp impedance is coincidental with the large signal lamp impedance, and a constant resistance is a suitable model for the lamp.

Once the discrete time small signal model was created with a sampling time equal to the switching frequency of 200 kHz, design of the controller was performed in MATLAB's SISOTOOL. The design consisted of creating a controller that had a crossover frequency in the target range of around 10 kHz for the load resistance of 10 Ω, and then check if the controller met design specifications for 150 Ω. The initial compensator was designed with its zero placed so that converter dynamics were compensated for in the 10 Ω case. The block diagram of the current loop is shown in Figure 4.13. The loop gain bode plots are shown in Figure 4.14 and Figure 4.15 for both the 10 Ω and 150 Ω cases.

The controller designed was with a sampling frequency of 200 kHz:

$$C_i = K\frac{z - Z_{z1}}{z - 1}, \tag{4.16}$$

where $K = 0.36259$, and $Z_{z1} = 0.7711$.

In this section, where input voltage variations are not considered, the outer power loop was

$$C_p = K_p\frac{1}{z - 1}, \tag{4.17}$$

where $K_p = 1.91x10^{-4}$.

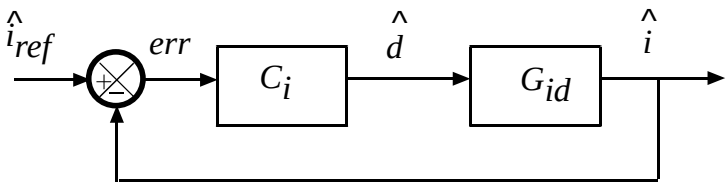


Figure 4.13: Block diagram for control loop design of inner current loop

Since the ballast is able to operate in LFSW mode across the entire range of lamp high frequency impedances, it becomes possible to transition from lamp ignition to LFSW mode for lamp warm-up. Figure 4.16 shows theoretical waveforms possible with a wide load range LFSW ballast with a fast ignition detection scheme. A short time of resonant operation is shown after ignition in order to allow for rectification effects in the lamp to settle. These effects can come from the lamp electrodes heating up unevenly, and the LFSW controller could possibly go unstable during this time.

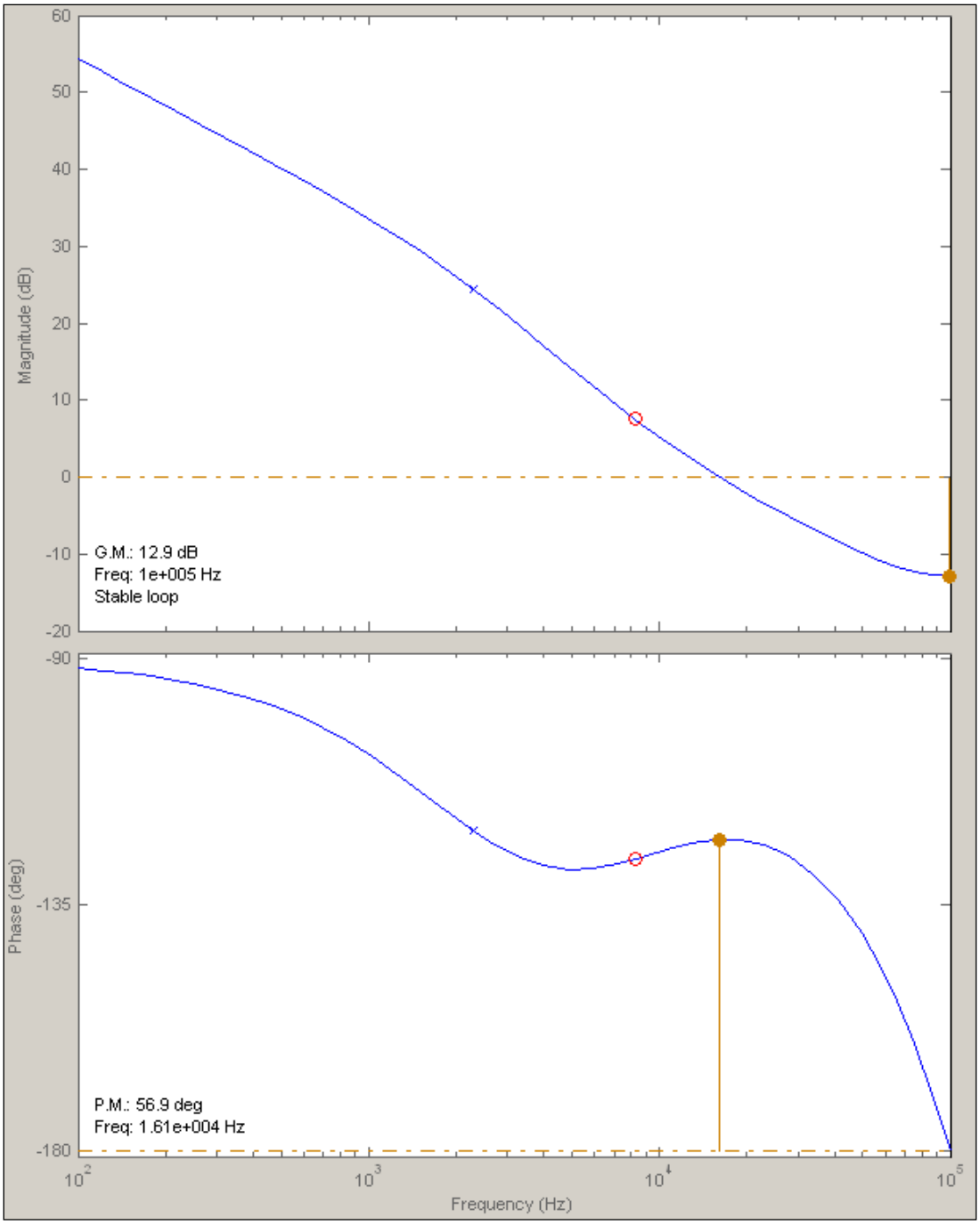


Figure 4.14: Loop gains of the current control loop for 10 Ω case

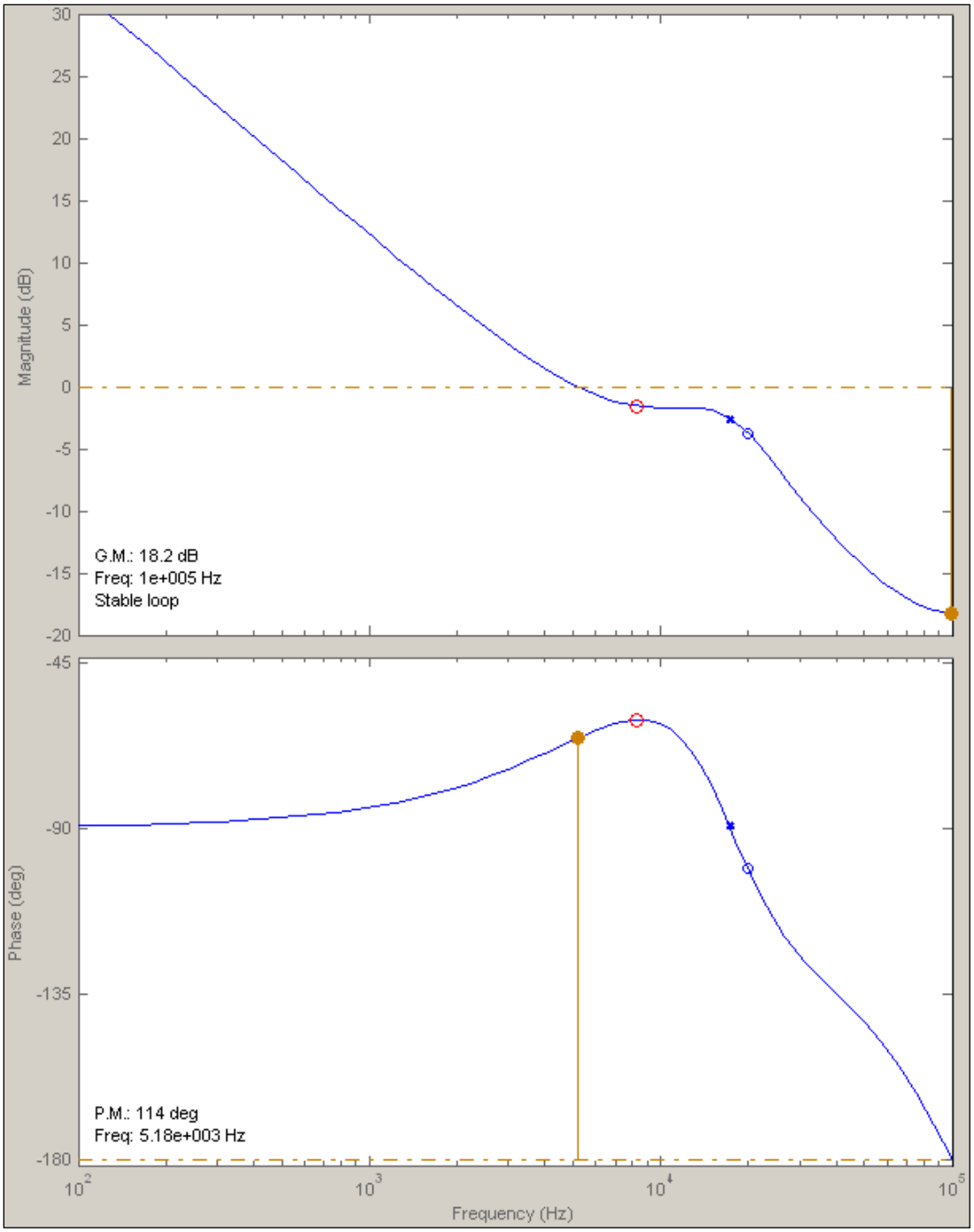


Figure 4.15: Loop gains of the current control loop for 150 Ω case

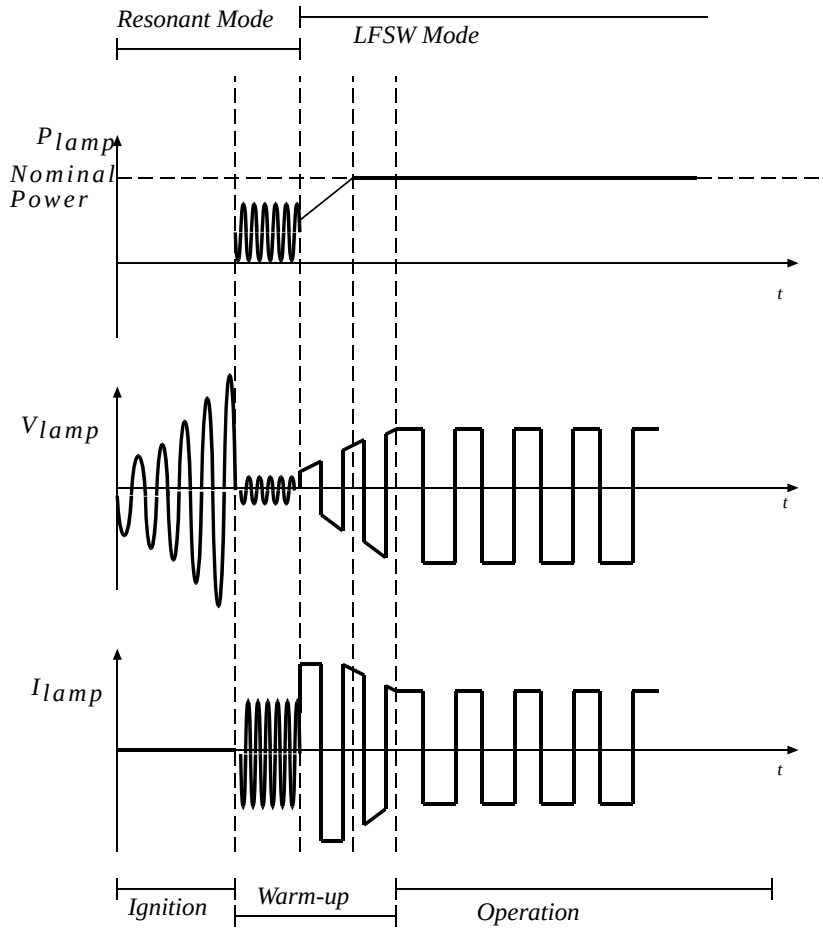


Figure 4.16: Resonant ignition with LFSW warm-up and steady-state

4.6 Summary

This chapter demonstrated the design and benefit of utilizing a soft saturation core inductor. The design was focused primarily on reduction or harmonic power introduced into the lamp by constraining the buck filter response to meet specific criteria. This was complicated further by the large expected load values allowed, as well as the fact that the buck filter response *Q* factor had to remain around critically damped. Design guidelines were given describing how a designer can choose what core material to use, with limited core data. Theoretical maximums of *Q* factor spread suppression were given, allowing the designer to create a buck converter with a

small spread factor, if given an exact relative permeability vs. DC magnetizing force data on a specific core.

A fast transition between buck modes of the converter was obtained through monitoring the zero crossing of the inductor current, and mirroring that time to create a fast inductor slope to the opposite polarity with the same magnitude. This facilitated the *Q* factor design criteria and ultimately led to a converter that met the specifications of the harmonic power threshold.

5 Input Power Control and PFC Ripple Rejection

The previous chapters discussed analysis of the second stage of a two-stage ballast. It was assumed that a DC power supply fed the ballasting circuit, and an assumption of no voltage ripple on the input allowed for simplistic design. In this chapter, the design and validation of allowance of input voltage ripple from the first stage, presumably a power factor corrector (PFC) is explored. The importance of input voltage variation rejection is in the fact that the voltage ripple from a PFC is directly controlled by the size of the output capacitor. The larger the output capacitor is, the smaller the output voltage ripple is. If a larger voltage ripple is allowed, the size of the output capacitor can be decreased. This is desirable because often the first element in switching power converters to fail is the electrolytic capacitors. Additionally, electrolytic capacitors are bulky, and add greatly to the overall size of the HID circuitry. If the capacitance is small enough, alternate capacitor types could be used, increasing the lifetime of the circuit.

In order to design the control system to reject input voltage variations, it is important to have working models of the system as a whole. In this section, two methods of modeling are presented, along with considerations for soft saturation core inductor use. The effect of the inductor variance is examined, and whether the effect of the varying inductance affects the modeling is explored.

5.1 Transient Switch Model

The first step to creating a switch level model of the system is to decompose the system into its linear parts. The first order linear model of the states of the system can be made using the well-known first order differential equations for capacitor and inductor voltage and current:

$$i_L = L\frac{dv_L}{dt} \tag{5.1}$$

$$v_C = C\frac{di_C}{dt} \tag{5.2}$$

Mathematical modeling software such as MATLAB can then create a model of the system. Previous work on models can be found in [43]-[52].Figure 5.1 shows a SIMULINK model of a buck converter that can be operated in both resonant and regular buck mode which is the circuit shown in Figure 5.2.

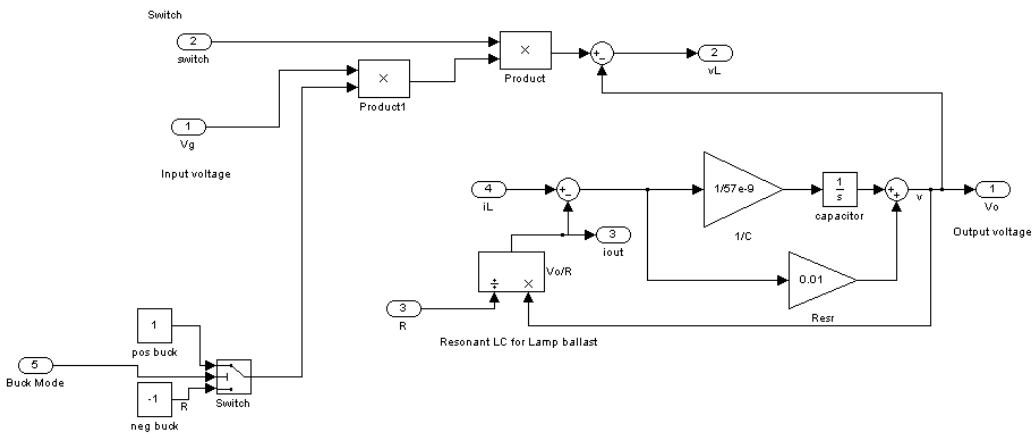


Figure 5.1: Buck Converter Simulation Model in SIMULINK minus inductor

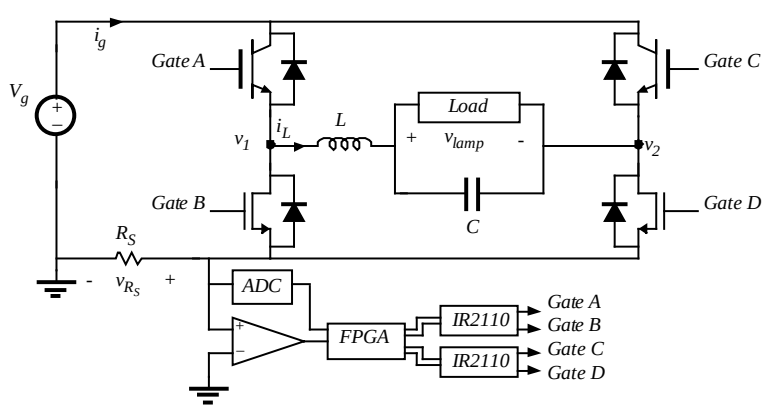


Figure 5.2: Ballast circuit capable of resonant ignition and LFSW operation

The model in Figure 5.1 accepts a value for load resistance, as well as has ports to connect the inductor model to the circuit. This is necessary to model a linear inductance as well as the soft saturation core inductance. The inductance can be modeled as Figure 5.3 if a constant inductance is assumed.

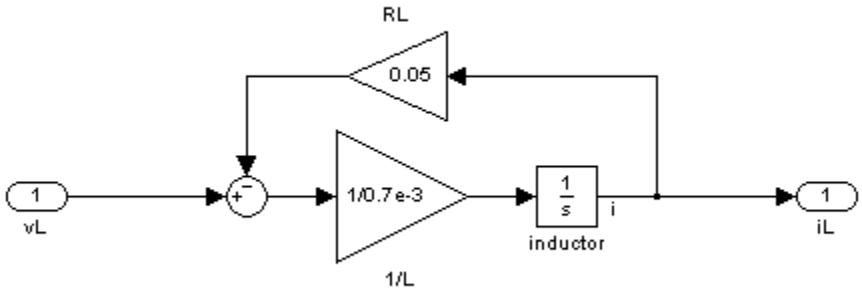


Figure 5.3: Linear inductance model in SIMULINK

In modeling the soft saturation core inductor, the question of linearization arises. One of the most well-known models of nonlinear inductance is found in [53]. This includes hysteresis, but for simplification, a simple relative permeability vs. DC magnetizing force model will be employed. The question is whether the small signal model will be affected by inclusion of the nonlinear inductance. [54] suggests a method for modeling the nonlinear inductance as a nonhysteretic function of current through the inductor. In this model, frequency response of the inductor is neglected, and the model is presented as a simplistic first cut model.

Using the manufacturer provided relative permeability vs. magnetizing force model, a nonlinear inductor was constructed in SIMULINK as shown in Figure 5.4.

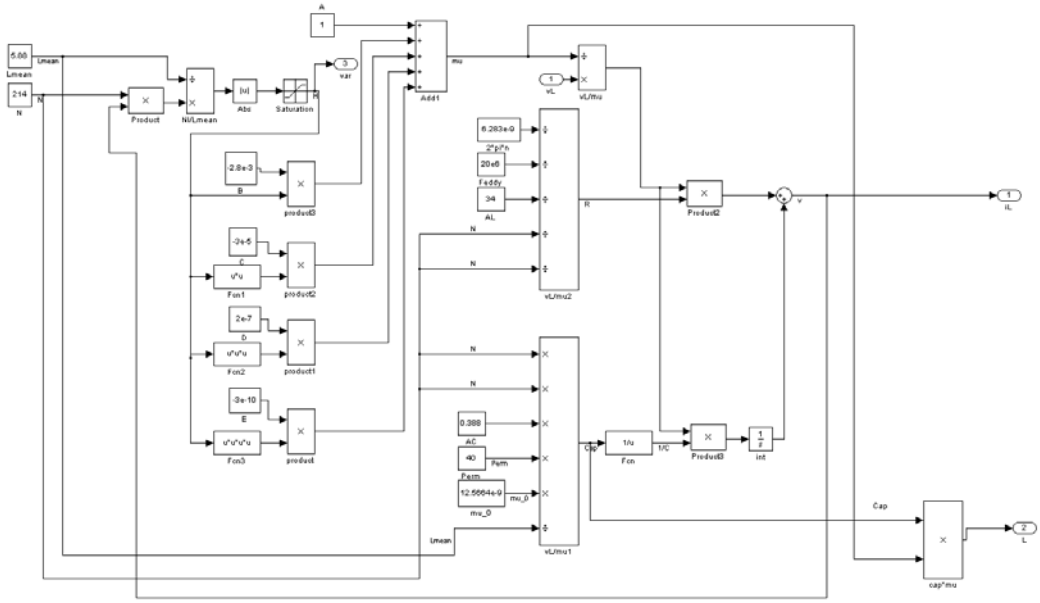


Figure 5.4: Nonlinear inductance model in SIMULINK

The linearity of the relative permeability vs. DC magnetizing force for the range of currents used in this converter is displayed in Figure 5.5 in terms of inductance vs. current in the inductor. This model assumes that the BH loop is approximated by the permeability vs. DC magnetizing force function, and that the area in the BH loop is small. This approximation is valid as when the converter is operating in steady-state, the current exhibits a small ripple, and the small ripple approximation can be applied.

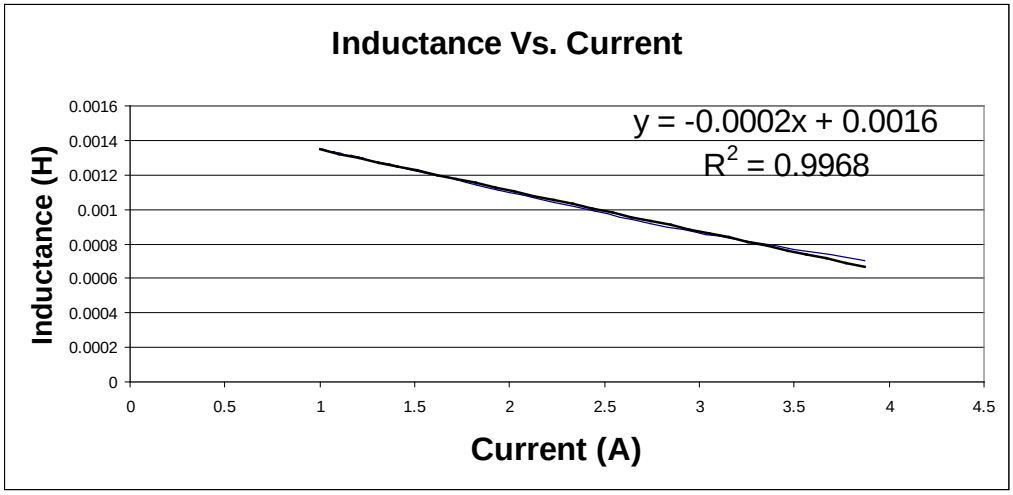


Figure 5.5: Inductance vs. Current of the soft saturation core inductor

The linear regression shows a very tight fit (R^2=0.9968), and the slope of the correlation is -0.0002. Stated another way, the inductance changes 0.2 mH for every Ampere change. This correlates to a very small change in the linearization, and for small signal approximations, the change in inductance can be ignored.

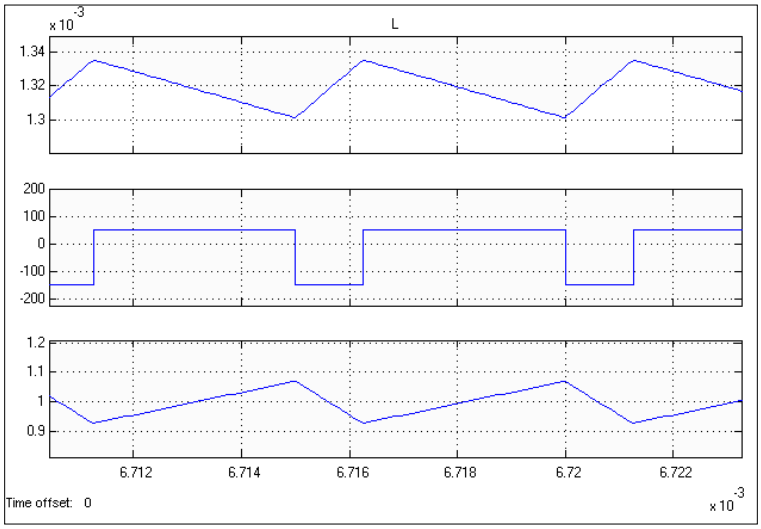


Figure 5.6: Nonlinear Inductor a) inductance, b) voltage across inductor, c) inductor current, across three switching cycles with a 150 Ω load resistance

The approximation is shown in the switch model in Figure 5.6 showing the effective inductance remains approximately constant during a switching cycle (within 1%). The end result of the transient switched model initial investigation is that for the small signal modeling of the converter dynamics, the inductance can be modeled as a constant inductance for a given operating point. Multiple operating points must be considered, each with a different inductance due to the soft saturation core material, but within a given operation point, an approximation of a linear inductor is sufficient.

With the soft saturation inductor model in simulation, it is easy to demonstrate the benefit of phase control for resonant ignition with the soft saturation core. Figure 5.7 shows an ignition performed with a linear inductor using a frequency sweep towards resonance. The simulation

was set to mimic ignition when the peak voltage of the load reached 1 kV, changing the load resistance from 1500 Ω to 50 Ω. Figure 5.8 is the same ignition simulation, except a soft saturation core inductor is used. It can be seen that using frequency control, the fluting on the lamp voltage of the soft saturation case becomes more extreme as resonance is approached. This is caused by the resonance of the tank shifting up in frequency, moving towards the operation point. Phase control slows the fluting down, allowing for a smoother approach to resonance.

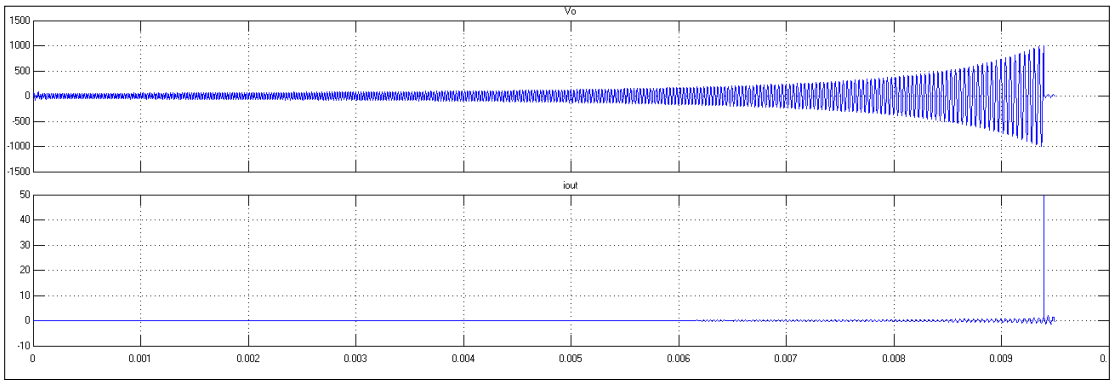


Figure 5.7: Frequency sweep ignition simulation using hard saturation core inductor

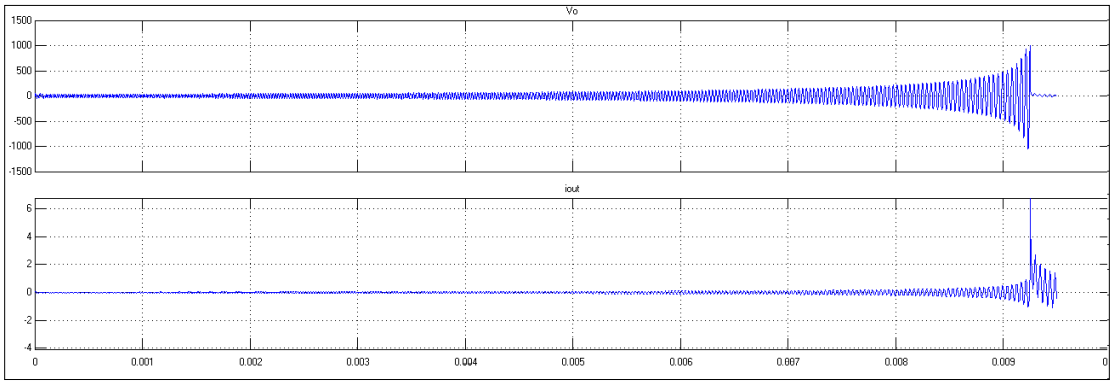


Figure 5.8: Frequency sweep ignition simulation using soft saturation core inductor

5.2 Small Signal Control Loop Modeling

As previously shown, the use of a constant impedance at a given operating point is assumed. Modeling the control-to-output transfer functions of the converter at different operating points was demonstrated in chapter 4. In order to design the inner and outer control loops to

compensate for input voltage variations in the second stage of the system shown in Figure 5.2, it is necessary to decide what measurements are available to sense. Given that the sense point of input current is already available, it is assumed that will be used. With a small ripple assumption in inductor current, it can be said that the inductor current is also available, which in steady state effectively equals the output current in the lamp. For the case of a DC converter, if lamp voltage were known, the output power could be found by:

$$\langle p_{out} \rangle_{T_s} \approx \langle i_{out} \rangle_{T_s} \langle v_{out} \rangle_{T_s} . \tag{5.3}$$

Perturbing by defining:

$$\langle p_{out} \rangle_{T_s} = P_{out} + \hat{p}_{out} \tag{5.4}$$

$$\langle i_{out} \rangle_{T_s} = I_{out} + \hat{i}_{out} \tag{5.5}$$

$$\langle v_{out} \rangle_{T_s} = V_{out} + \hat{v}_{out} , \tag{5.6}$$

and then linearizing by keeping only first order terms,

$$\begin{aligned} P_{out} + \hat{p}_{out} &= \left(I_{out} + \hat{i}_{out}\right)\left(V_{out} + \hat{v}_{out}\right) \\ &= I_{out}V_{out} + I_{out}\hat{v}_{out} + V_{out}\hat{i}_{out} + \hat{i}_{out}\hat{v}_{out} \end{aligned} \tag{5.7}$$

$$\hat{p}_{out} \approx I_{out}\hat{v}_{out} + V_{out}\hat{i}_{out} \tag{5.8}$$

With (5.8), the control topology can be created. As shown in earlier chapters, current control is desired in order to stabilize the arc. A perfect current controller creates an infinite output impedance, which is desired with the possibility of negative incremental resistance in the lamp. In reality, a perfect controller cannot be realized due to sampling effects, and general non-idealities. If a two loop design with an inner loop that controls the lamp current, and an outer loop that controls the lamp power is used, with (5.8) it can be seen that the controller block

diagram for a system monitoring output current and output voltage in order to control output power then becomes:

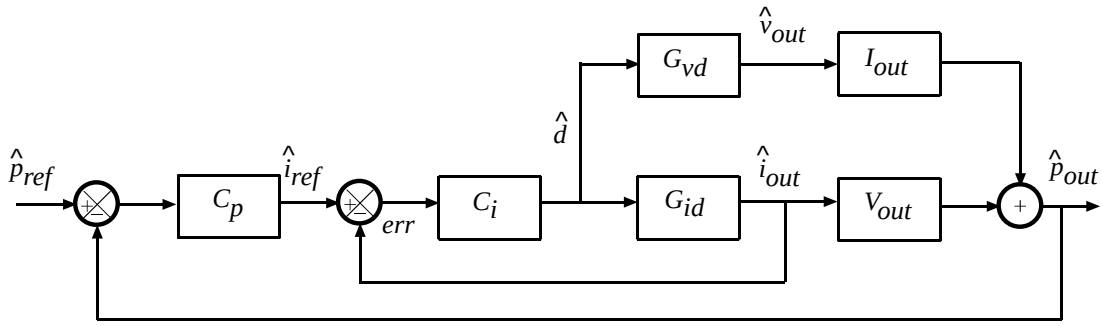


Figure 5.9: Block diagram for output current and output voltage sensing power control

With the control topology as presented in Figure 5.9, the controller C_p directly attempts to control the error of the output power, p_{out}, to the power reference, p_{ref}. If output power perturbations below a certain frequency are desired to be controlled, the bandwidth of both the inner and outer loop must be larger than said perturbation.

Power sensing requires at least two variables of Ohm's law in order for power to be calculated. This can be accomplished by having a known impedance, and monitoring either voltage or current. The lamp impedance is not known in the case at hand, and is by definition variable throughout lamp age and warm-up condition. It would therefore be necessary to monitor both lamp current and voltage simultaneously. Due to the full bridge topology, it is difficult to monitor output voltage with one sense point.

Input voltage can be monitored by a single sense point, and inductor current is already measured in order to achieve current regulation from the inner current loop. The block diagram of the two loop control featuring an outer input power loop with an inner current loop is shown in Figure 6.8.

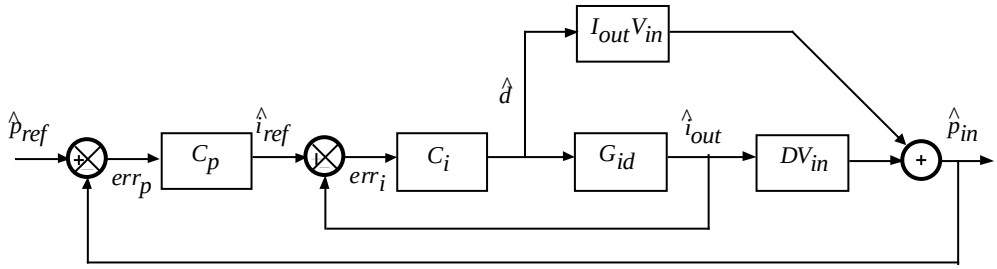


Figure 5.10: Block diagram of input power loop with inner current loop

Perturbing and linearizing, the dependence of output current in terms of input voltage can be derived. The block diagram is shown in Figure 5.11.

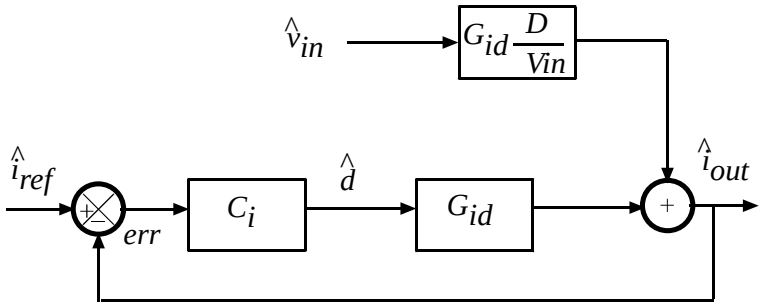


Figure 5.11: Block diagram of current controller

The input voltage rejection of the current loop controller, $\frac{\hat{i}_{out}}{\hat{v}_{in}}$, is shown in Figure 5.12. It can be seen that the crossover frequency constraint for the current loop compensator is much more stringent than a 120 Hz perturbation, and a current loop alone is enough to compensate the input voltage ripple.

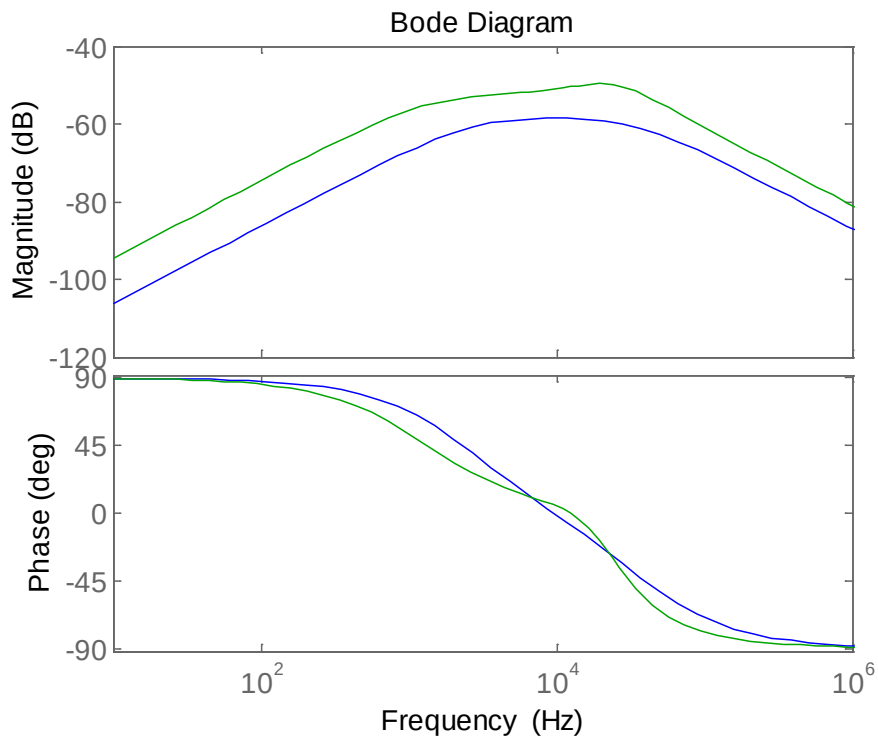


Figure 5.12: Input voltage ripple attenuation for 10 Ω load (blue) and 150 Ω load (green)

5.3 Input Power vs. Output Power Sensing

It can be seen from Figure 5.10 that output power is not directly controlled. As such, it is important to understand the connection between input power and output power. In a steady-state sense, it is trivial to show that the average values of the input and output powers in the absence of perturbations are related by:

$$\langle p_{out} \rangle_{T_s} = \eta \langle p_{in} \rangle_{T_s}, \tag{5.9}$$

where η is the efficiency of the converter.

If the integrator on the power controller has a bandwidth slower than the input voltage perturbation, the perturbation is attenuated at the current control reference, and the current error signal sees less of the perturbation. Since the current reference is not modified, and it is assumed that in this small amount of time, the lamp resistance does not change, the output power remains

constant, as constant current translates to constant power with constant resistance. The speed of the current compensator has already been discussed, and since its bandwidth is designed to be around 3-10 kHz, the 120 Hz ripple perturbation is easily compensated.

If in this case a slower integral power loop compensator is desired in order to not interfere with the inner current loop compensator, what reason holds the designer from making the compensator as slow as possible, as in a gain of 0? If that strikes the reader as a hyperbolic argument, the question is what lower bounds exist for the compensator bandwidth. The arguments for using the power loop compensator were to account for possible PFC output voltage errors, and account for the lamp changing impedance during operation and over its lifetime. It is within these time constants that a lower bound can be found.

If the first stage of this HID ballast were to have a constant error, an integrator would be needed to cancel this out. The constant error could come from a PFC run with a proportional controller among other things. In most cases, this error would essentially be DC as it would not fluctuate during operation, or from turn on to turn on.

The lamp resistance changes throughout bulb life, but this change is measured in terms of days of use. As such, this limit does not provide a very stringent lower bound of the controller bandwidth.

The warm-up of the lamp provides another possible lower limit for the input power loop bandwidth. If the input power loop were to be slower than the linearized change in resistance during warm-up, the power loop would not be able to begin controlling power once the lamp passed into the constant power region. This could lead to an overshoot of power as the system transitions from current control to power control. The warm-up process for most MH and HPS

lamps commercially available are said to take in the range of 3 to 4 minutes in order to reach a steady-state resistance. During this time, the lamp resistance typically varies linearly [55].

In order to provide a conservative limit, it will be assumed that the lamp will exhibit the full range of resistances allowed in the design constraints, even though this is highly unlikely during operation. Also, a faster bound of warm-up occurring in 2 minutes will be assumed. In order to find a suitable bandwidth for the system, the model of lamp resistance changing in a triangular waveform will be assumed. This model is suitable as once the first peak of the triangular waveform is reached, the system would go into power regulation, so the extra frequency data is a conservative over designing. A variation in the load resistance translates to a proportional variance in the output power, since current is controlled as long as the change in resistance happens slower than the current loop. The exact bandwidth required can be seen by looking again at the triangle waveform. Looking at the Fourier series of the example conservative resistance model,

$$y_{triangle} = magnitude \frac{8}{\pi^2} \sum_{k=0}^{\infty} (-1)^k \frac{\sin((2k+1)\omega_{triangle} t)}{(2k+1)^2}, \tag{5.10}$$

where $\omega_{triangle}$ in this case is

$$\omega_{triangle} = 2\pi \frac{1}{2\min} = 2\pi \frac{1}{2 \cdot 60} = 2\pi \cdot 0.0084 rad/s. \tag{5.11}$$

Looking at the roll off of the harmonic frequencies of the triangle waveform, it can be seen that harmonics past 1 are less than 5% of the original magnitude each. As such, having a bandwidth that includes the first harmonic should be sufficient to track the fastest resistance change ramp one should encounter. This translates to a required bandwidth of $2 \cdot \omega_{triangle}$, or 16.8 mHz in this particular case.

5.4 PFC Output Capacitor Sizing

For a standard boost type PFC, the minimum output capacitance is usually given in terms of allowable output ripple in terms of output power [56] as shown in (5.19).

$$Cout\_\min = \frac{2P_{out\_PFC}\Delta t}{V_{out\_PFC}^{\ 2} - V_{out\min\_PFC}^{\ 2}}. \tag{5.12}$$

The Δt represents the holdup time from one rectified AC peak to the next peak. If the system is assumed to be operated in the United States, and the PFC output voltage is the designed 200 VDC, the only variable left in order to define the minimum output capacitance is the minimum voltage allowed. Another way to define this design constraint is to find the maximum allowable voltage ripple on the output of the PFC.

The constraints on the output voltage ripple come from the ability of the power loop controller to reject the 120 Hz perturbation to below the 5% threshold allowed for harmonic power on the lamp output, and the system's steady-state operation. During LFSW, the converter acts as a buck, allowing for voltages at and below the input voltage of the second stage, modified by the converters efficiency, η, in that for the second stage of the HID ballast neglecting switching loss:

$$V_{lamp} = V_{out\_PFC} \cdot \eta \cdot D. \tag{5.13}$$

It is important now to look at the converter efficiency. Conduction losses are found to be:

$$P_{loss} = I_{out} \cdot V_{ce\_sat} + I_{out}^{\ 2} \cdot R_L + D \cdot I_{out}^{\ 2} \cdot R_{on} + D' \cdot I_{out} \cdot V_f, \tag{5.14}$$

where the HGTP12N60A4D IGBTs, $V_{ce\_sat} = 1.6V$ and the forward voltage of the ant-parallel diode is $V_f = 2$. For the IRFP340 MOSFETs the $R_{on} = 0.55\Omega$, and the series resistance of the inductor is $R_L = 0.1\Omega$. Figure 5.12 shows the efficiency across the available lamp resistances.

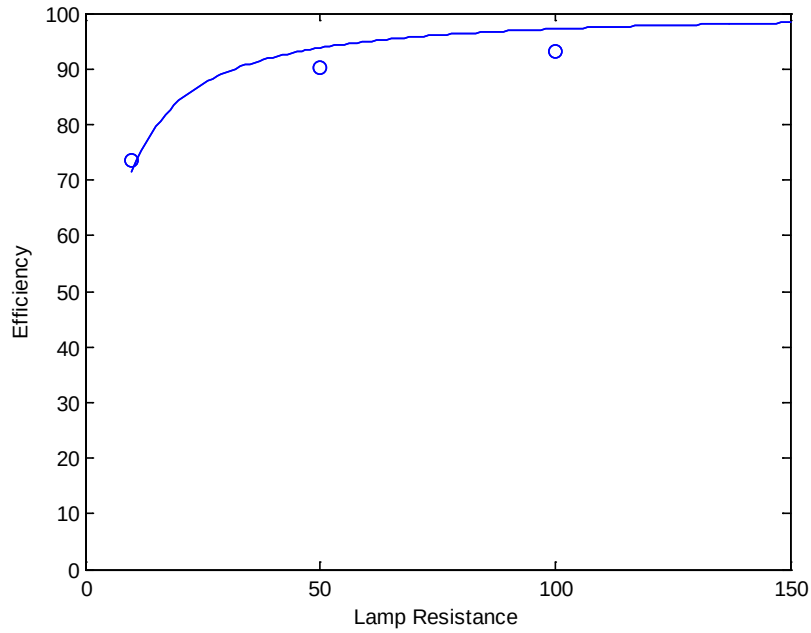


Figure 5.12. Efficiency vs. lamp resistance. Circles are measured results. Line is theoretical ignoring switching and core loss.

From this, one can find the minimum output voltage of the PFC, which is defined by the maximum voltage the lamp would require to operate at full power. This occurs when the lamp resistance is at its maximum, or 150 Ω. The maximum steady-state voltage the lamp would require is

$$V_{out\_\max} = \sqrt{P_{out} \cdot R_{\max}} = \sqrt{150 \cdot 150} = 150V \quad (5.15)$$

Combining (5.20) and (5.22), and assuming a maximum duty cycle of 95% is employed,

$$V_{out\_PFC} = \frac{V_{lamp\_\max}}{\eta \cdot D} = \frac{150}{0.98 \cdot 0.95} = 161.1V \quad (5.16)$$

For a PFC nominal output voltage, this translates to

$$V_{ripple\_PFC} = \pm 38.9V \quad (5.17)$$

The absolute minimum output capacitor is found using (5.19) to be 178 μF. In actual implementation, this would be increased, possibly by as much as a factor of 1.5.

With the minimum PFC output capacitor defined, the final design of the power loop can be completed. Using a standard PFC, such as a boost configuration, the PFC definition translates to allowing a voltage ripple of $\pm V_{ripple\_PFC}$ to occur at the input of the second stage of the ballast. This means that the power loop must be designed so that this ripple does not propagate to the output.

As shown in the previous section, a slower integrator compensator translated to better input voltage ripple attenuation in terms of output lamp power. A lower bound was defined using the lamp warm-up resistance change characteristic as the defining criterion. An upper bound can now be defined by the magnitude of the 120 Hz ripple due to the PFC.

It has been shown that the current loop is capable of attenuating the input voltage ripple to a suitable level. The speed of the power loop compensator must be above the expected speed in which the lamp resistance will change during warm-up, but below where it may interfere with the operation of the current loop. A bandwidth of $3\,\text{Hz}$ was chosen, and the resulting compensator was found to be

$$C_P = K_P \frac{1}{z-1}, \tag{5.18}$$

where $K_p = 1.91 \times 10^{-4}$.

5.5 Summary

The design and implementation of an input voltage and output current sensing control of output lamp power has been investigated. A new control strategy has been proposed comprised of a two loop design in which the inner loop provided current control of the lamp. The inner loop was designed to be very fast relative to the outer loop. The outer loop consisted of an integral

controller which provided input power control. It was found that having a faster outer loop coupled more input voltage disturbance than a slower loop. This was due to the relation between input and output power disturbance rejection.

An upper and lower bound on the bandwidth of the power integrator was found. The lower bound was dictated by the possible speed of the lamp resistance varying during warm-up and steady-state operation. The upper bound on the bandwidth of the power loop was defined by a desire to not interact with the inner current loop. The upper limit was constrained by the amount of suppression the controller would give to the 120 Hz voltage ripple as seen from the output of a first stage PFC. A design method for defining how small the output capacitor of a standard PFC was also presented.

6 HID Lamp Ballast Experimental Results

An experimental test bed was constructed in order to verify the design methodology presented in previous chapters. The simplified block diagram of the system is shown in Figure 6.1. The input voltage V_g was 200 Vdc, in order to simulate the output of a possible first stage PFC. Switches A and C were implemented using HGTP12N60A4D IGBTs with internal anti-parallel diodes which are used in the LFSW buck mode as the passive switch. The MOSFETs on the low-side were IRFP340 in order to allow for lower losses during PWM action in the buck modes. The high-side low-side drivers were IR2110 ICs [57], [58]. The controller was implemented in VHDL (refer to Appendix A) on a Spartan 3E development board with a clock frequency of 50 MHz. For sensing the zero crossing of the inductor current, an LT1016 comparator was used on the current sensing resistor which was 0.25 Ω. Also on the current sensing resistor was a half-flash AD7822 8-bit ADC. A photograph of the experimental setup is shown in Figure 6.2.

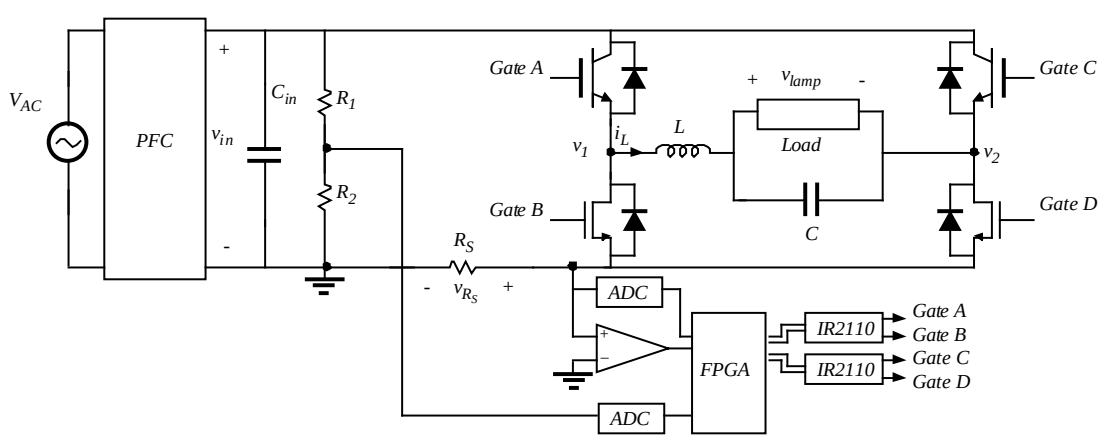


Figure 6.1: Experimental setup block diagram

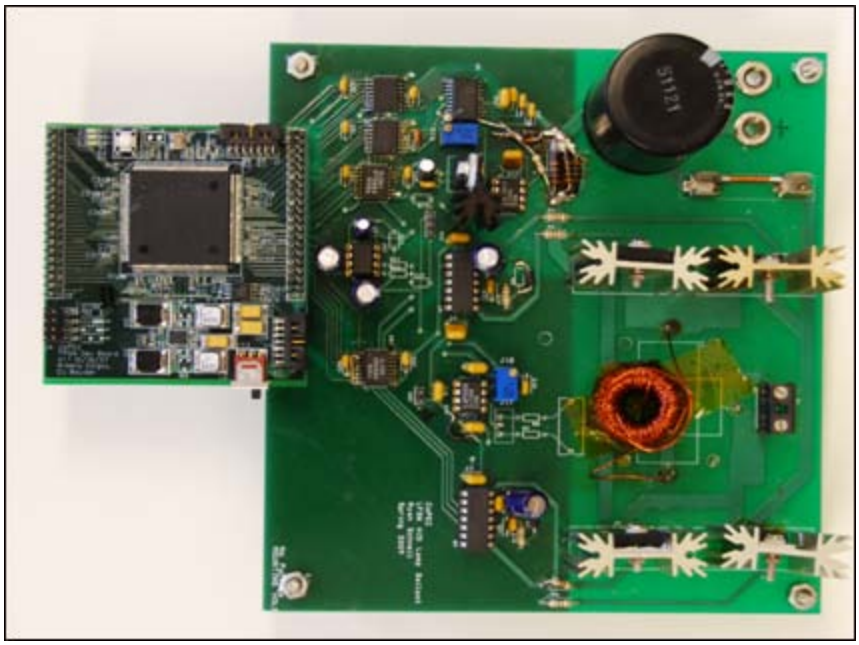


Figure 6.2: Photograph of experimental test setup

6.1 Resonant Ignition with Resonant Warm-up Experimentation

The experimental test bed was edited to include a 63 nF tank capacitor while the inductor, *L*, was designed using a 77071A7 Kool Mu soft saturation core according to the design example in Section III with a nominal inductance of 1.9 mH at zero dc bias. The inductor required 177 turns of 23 AWG wire. IR2110 high-side gate drive ICs were used to drive the switches with a 300 ns dead time and gates A and D complimentary from gates B and C. Based on the tank design, the nominal switching frequency was expected to be between 15-80 kHz at a 50% duty cycle in the resonant mode. The lamps used were metal halide Sylvania HIS-TD 150W/WDL and high pressure sodium GE Lucalox LU 150/100/T/40 lamps.

Successful ignition of a MH is shown in Figure 6.3. A substantial rectification period post ignition can be seen once the lamp voltage collapses. Ignition of a HPS lamp is shown in Figure 6.4. It can be seen that the lamp ignition voltage is well below the manufacture's recommended ignition voltages, specifically, in the case of the metal halide lamp, a single impulse of 3.5 kV is

requested by the manufacturer for ignition, while in testing the lamp was able to ignite regularly under 900 V with a phase sweep. Both lamps were ignited using the same controller, demonstrating the wide ranging capabilities of phase control.

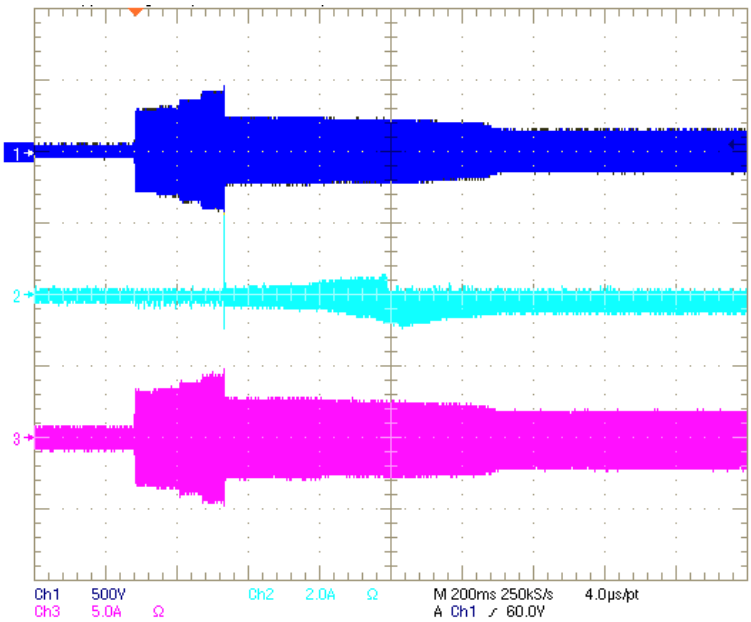


Figure 6.3: Ignition waveforms for metal halide lamp using phase sweep. Upper: lamp voltage (Ch1), middle: lamp current (Ch2), lower: inductor current (Ch3)

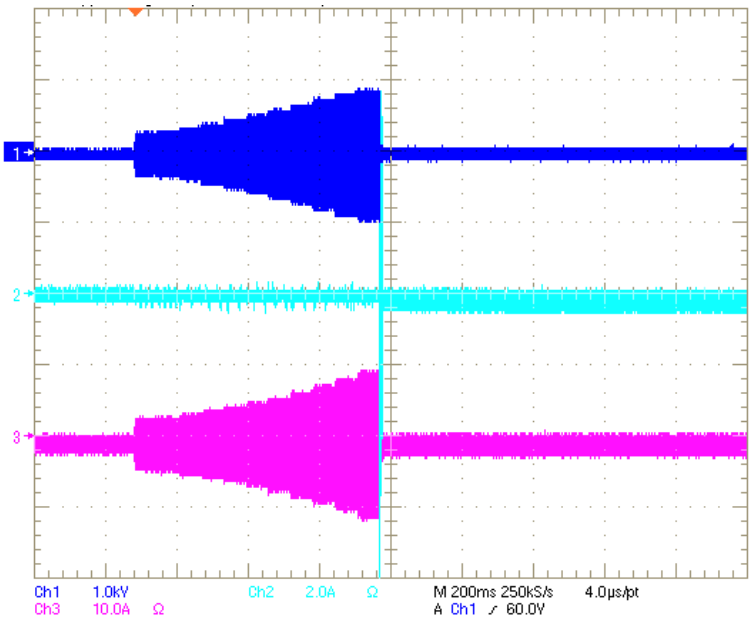


Figure 6.4: Ignition waveforms for high pressure sodium lamp using phase sweep. Upper: lamp voltage (Ch1), middle: lamp current (Ch2), lower: inductor current (Ch3)

Figure 6.5 and Figure 6.6 show oscilloscope waveforms around ignition, showing immediate change of the operating frequency, and successful lamp ignition. It can be noted that the lamp current waveform is triangular due to both the facts that operation is far from resonance, and the soft saturation core helps to add a triangular wave shape to the current.

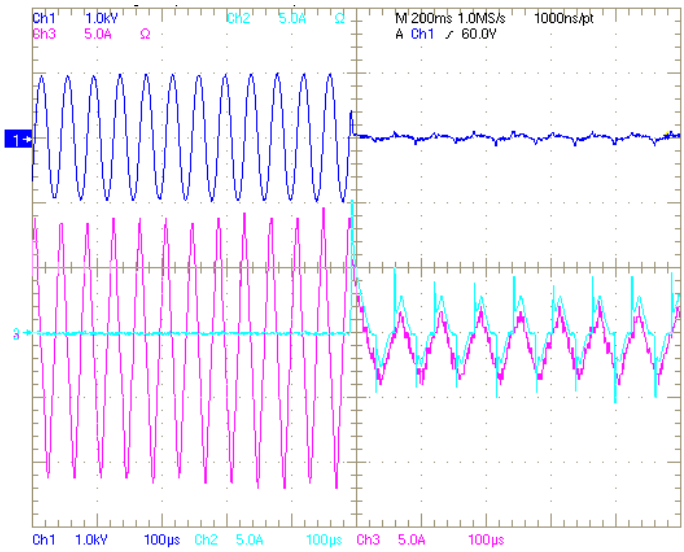


Figure 6.5: Ignition waveforms for a high pressure sodium lamp using a soft saturation core inductor. Upper: lamp voltage (Ch1), middle: lamp current (Ch2), lower: inductor current (Ch3)

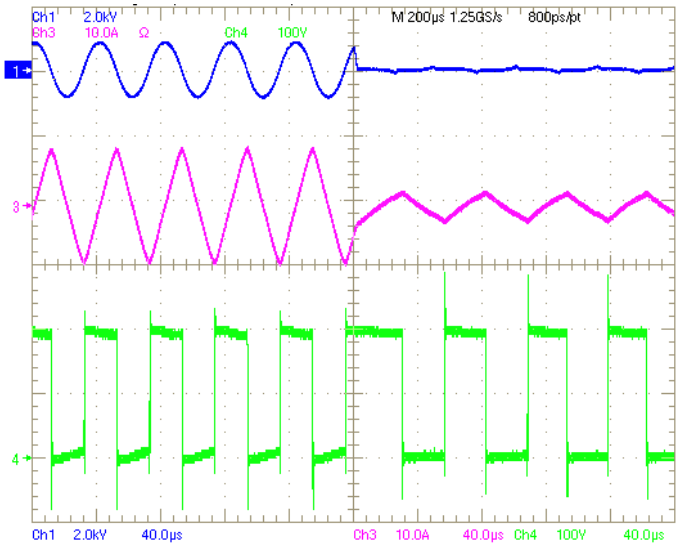


Figure 6.6: Ignition waveforms for a high pressure sodium lamp using a soft saturation core inductor. Upper: lamp voltage (Ch1), middle: lamp current (Ch3), lower: voltage on one leg of the full bridge (Ch4)

It can be seen in Figure 6.5 and Figure 6.6 that the operating frequency directly after ignition went down in both cases. This is not always a guaranteed case, as the operating point for

ignition can vary from lamp to lamp, and ballast design to ballast design. For the case of an LC_SC_P converter, the resonance before and after ignition have relatively high *Q* factors as compared to the post ignition *Q* factor of the buck converter fed with a resonant full bridge. In the case of an LC_SC_P converter, the converter can be designed with a soft saturation core inductor to ensure the post-ignition operating frequency is at least as low as the pre ignition frequency, meaning the lamp is being driven at least as hard as it was before the lamp ignited.

The inductor in this experimental setup was designed to reduce the overall system size and weight, but allow for acceptable losses during warm-up operating in a resonant mode. Warm-up performed in a resonant mode is a typical method for electronic ballasts, but as has been mentioned, such operation is vulnerable to acoustic resonance if not designed properly. In the next section, experimentation with an inductor designed for LFSW mode warm-up is presented. Operation in the LFSW mode allows for lower losses due to the operation in a small BH loop region, and therefore a smaller area of the BH loop. Additionally, LFSW operation reduces the chances of acoustic resonance by reducing the harmonic content in the lamp power.

6.2 LFSW Mode Warm-up Experimentation

Experimentation in this section covers lamp ignition with fast ignition detection through phase control on a ballast with a soft saturation core inductor. This allows for near immediate transition to LFSW mode for the warm-up of the lamp. Warm-up in the LFSW mode also has the benefit of operating the inductor in a smaller BH loop region, reducing core losses. Additionally, by allowing the inductor to go far into saturation, the size of the inductor can be greatly reduced. Figure 6.7 demonstrates the size benefit of this inductor design as compared to a hard saturation inductor designed not to saturate during ignition.

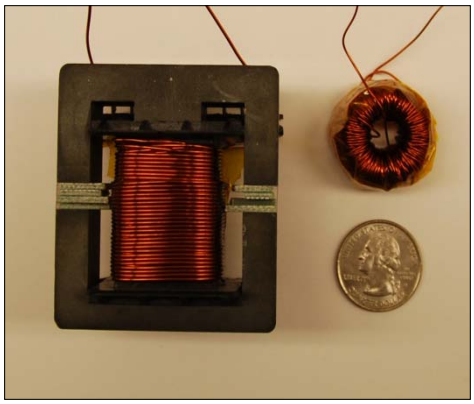


Figure 6.7: Hard saturation core inductor (left), soft saturation core inductor designed for LFSW warm-up (top right), US quarter for size (bottom right)

The experimental test bed tank capacitance was changed 57 nF in order to accommodate the inductor designed in Chapter 5. The inductor was constructed using a toroidal Kool Mu 0077356A7 core with 214 turns of 23 AWG copper wire. A 300 ns dead time was used for the transition between the buck modes. Figure 6.8 shows a successful ignition waveform. The controller was programmed to remain in resonant mode for 1.1 s after ignition was detected. The transition to warm-up mode in LFSW is very fast compared to previous works. The benefit of this fast transition to LFSW mode is greater control of the warm-up current, without having to use either a priori knowledge of the circuit tank elements and load resistance, or using a resonant current sensing element.

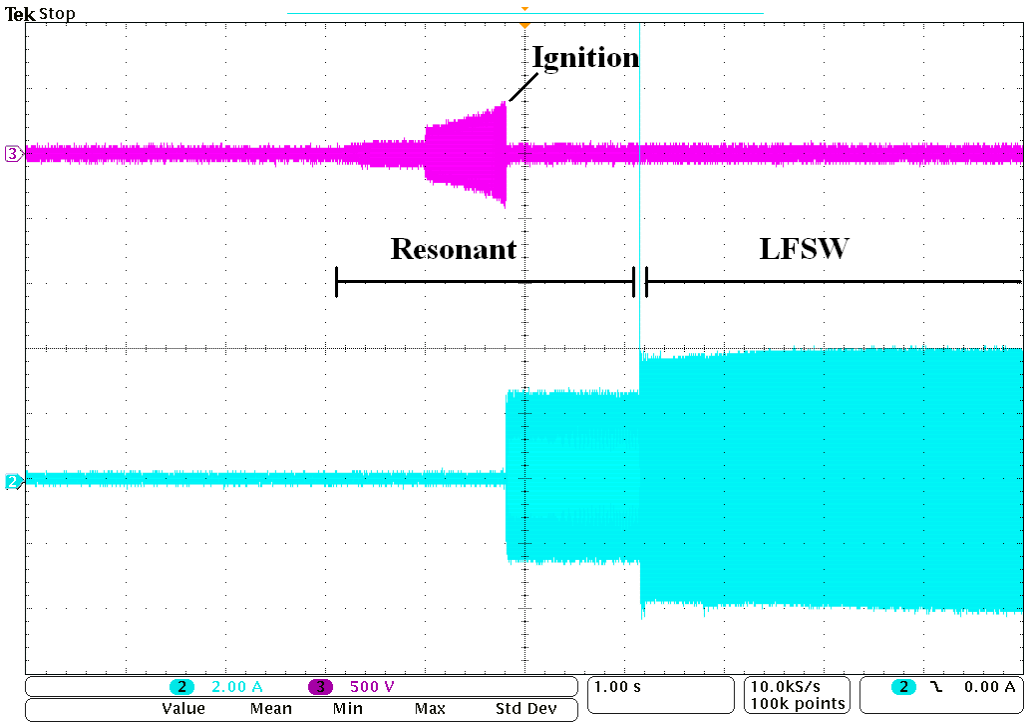


Figure 6.8: Ignition of an HPS lamp. Lamp current (CH2, 2 A/div), Lamp Voltage (CH3, 500 V/div). LFSW begins 1.1 s after ignition.

Steady-state operation of the lamp is shown in Figure 6.9. The Tektronix DPO2014 oscilloscope MATH channel displays the lamp power, showing the characteristic spikes as expected at twice the LFSW switching frequency. The fast Fourier transform was used to decompose the power signal, and it was found that this operation met the 5% threshold given in the design specifications with a 80 µs sampling period. Additionally, no flickering was noticed by the experimenters during operation.

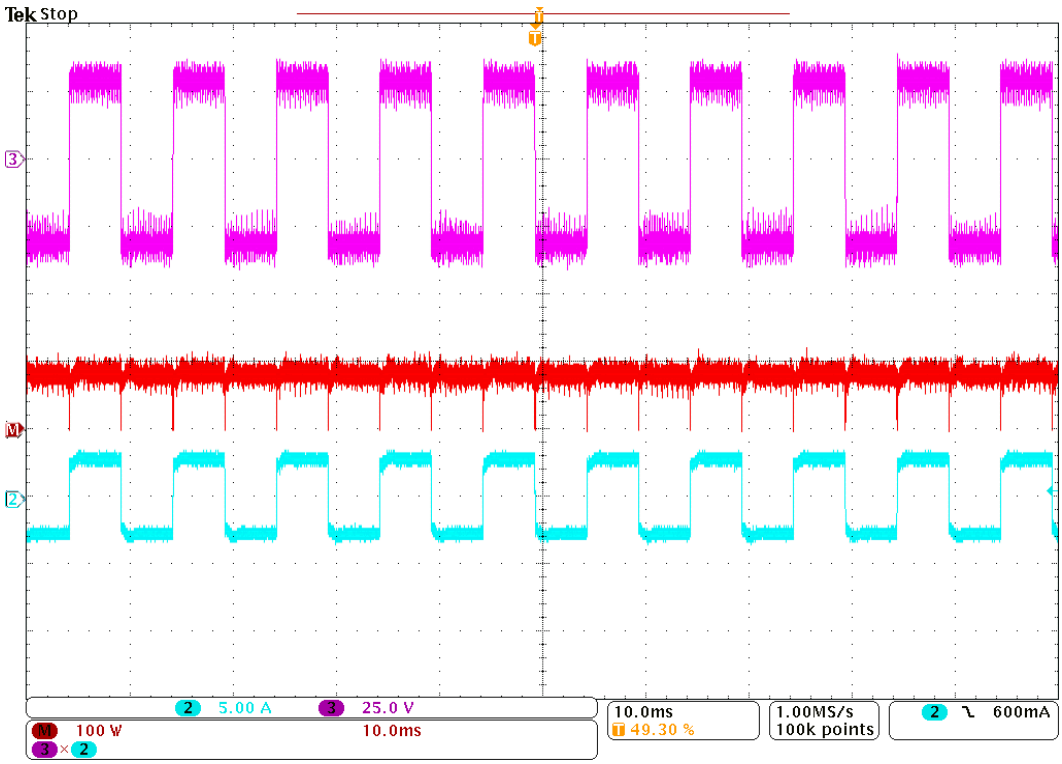
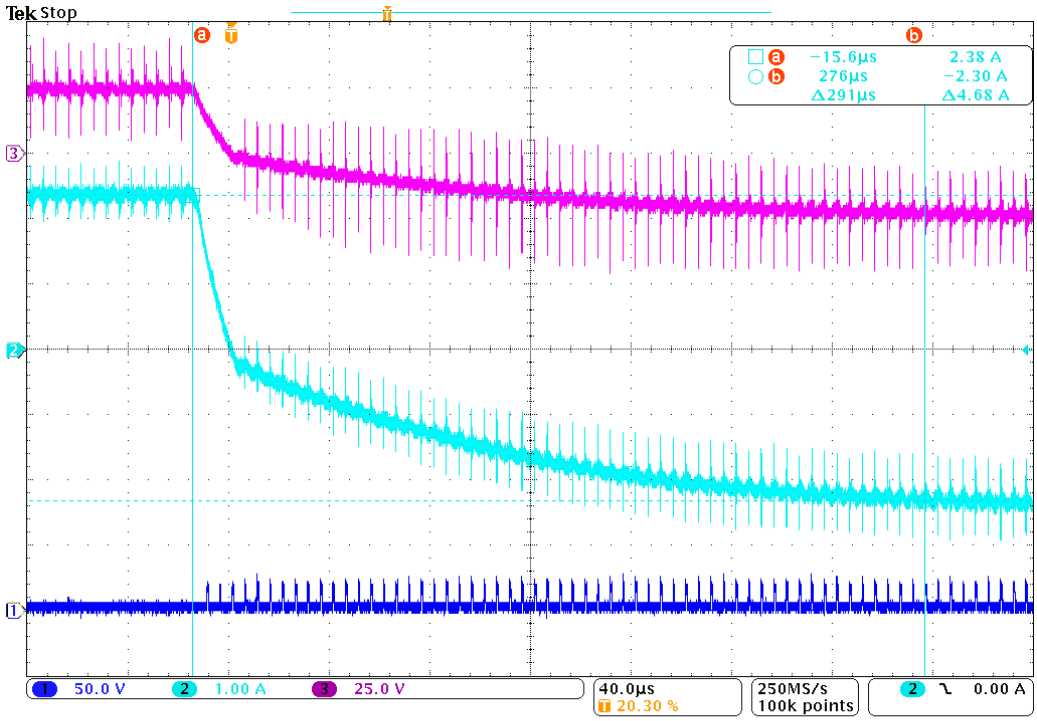
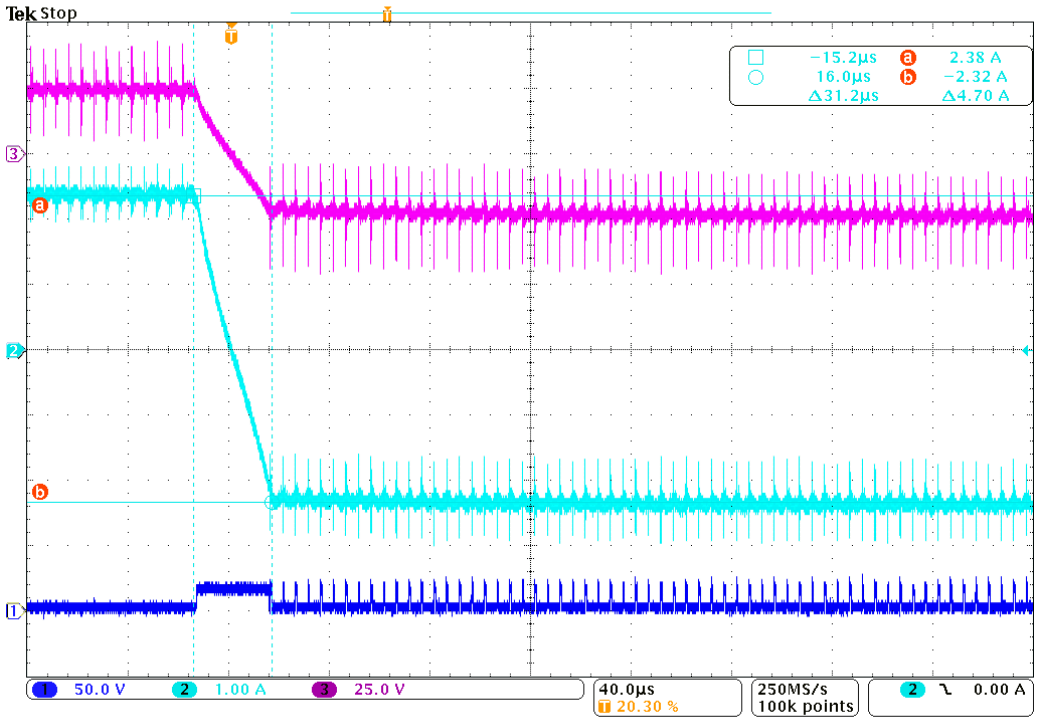


Figure 6.9: Warm-up operation in LFSW. Lamp current (CH2, 5 A/div), Lamp voltage (CH3, 25 V/div), Lamp power (MATH, 100 W/div)

A comparison between operation with and without the fast transition discussed in section 4.2 was made, and it was found that with the lowest *Q* factor case, the 5% threshold was not met without the fast transition switch timing. The highest peak for a 10 Ω resistor load was 10.17% of total power without the fast transition timing. With the fast transition timing, this was brought down to 4.67%, meeting the specification. The comparison between the two transitions is shown in Figure 6.10.



(a)



(b)

Figure 6.10: Steady-state operation transition from positive to negative buck in LFSW a) without time-optimal control; b) with time-optimal control: Gate B signal (CH1 50 V/div), Lamp current (CH2 1 A/div), Lamp voltage (CH3 25 V/div)

It should be noted that no acoustic resonance was observed for the non-fast transition operation as well. The 5% threshold is a conservative measurement, and even meeting it approximately could lead to acoustic resonance free operation. Also, the largest peak of the power harmonic will be at twice the LFSW frequency, which is below where the usual acoustic resonance hot spots occur. As such, this threshold is very conservative, but nonetheless was met.

The resolution of the digital timer that controls the T_{tran} timing was 20 ns, or the clock frequency of the FPGA. Faster transitions were shown to reduce the harmonic power in the lamp, reducing chances of acoustic resonance issues, as well as reducing the chance of re-ignition of the lamp.

It can be seen that successful ignition and warm-up were performed with a smaller inductor. Harmonic power within the lamp was kept below the 5% threshold, and no acoustic resonance was observed. The next section shows experimental results of testing to reject input voltage ripple coming from the PFC.

6.3 Input Voltage Ripple Rejection Experimentation

Using the same secondary stage as previous chapters, but applying an AC input with a 200 V DC bias, the design of the integral power loop was tested. Testing consisted of applying the input voltage while in LFSW mode to a resistor load in order to test the various operating points. Figure 6.11 shows operation with a 50 Ω load and a 20% input voltage ripple. It can be seen that the output power waveform has very little disturbance from the 120 Hz ripple. The Fourier analysis of the waveforms confirmed that the 5% threshold was met for power harmonics.

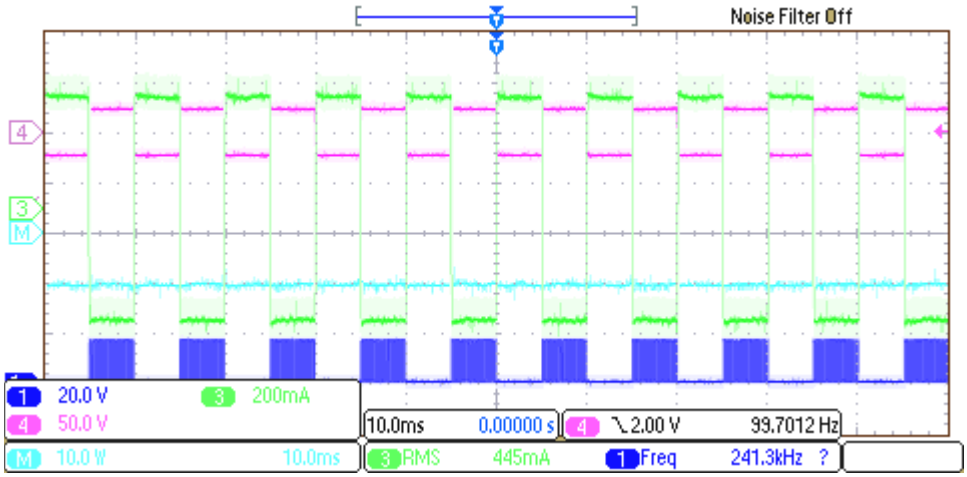


Figure 6.11: Steady-state operation of 50 Ω load. Gate B waveform (CH1), Lamp Current (CH3), Lamp Voltage (CH4), Lamp power (MATH)

Figure 6.12 shows a 50 Ω load on the second stage fed with a ±20 V 120 Hz ripple with a 200 V DC bias. The waveform shows little disturbance to the 10% ripple, as expected. Figure 6.13 shows the same load setup with a ±40 V 120 Hz ripple with a 200 V DC bias.

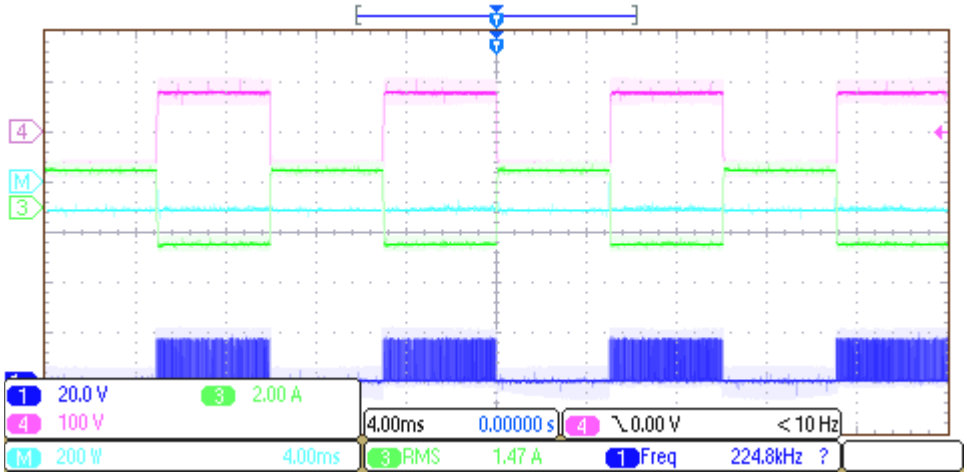


Figure 6.12: Steady-state operation of 50 Ω load. Vg = 200 VDC ±20 V 120 Hz. Gate B waveform (CH1), Lamp Current (CH3), Lamp Voltage (CH4), Lamp power (MATH)

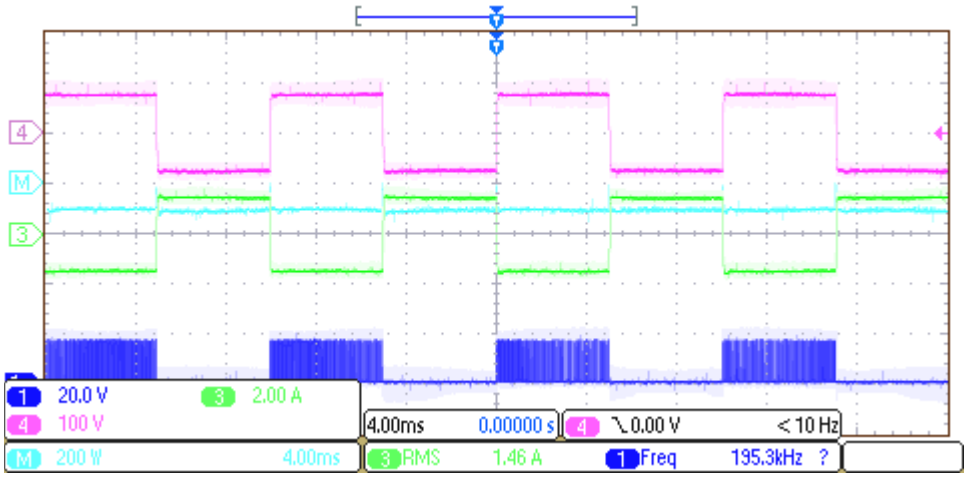


Figure 6.13: Steady-state operation of 50 Ω load. Vg = 200 VDC ±40 V 120 Hz. Gate B waveform (CH1), Lamp Current (CH3), Lamp Voltage (CH4), Lamp power (MATH)

Figure 6.14 shows a 50 Ω load on the second stage fed with a ±10 V 120 Hz and a DC bias of 110 V. This was chosen to demonstrate what happens when the control saturates. In this case, a maximum duty cycle of 80% was imposed on the FPGA in order to allow duty cycle saturation, and at the lowest peaks of the input voltage, more than 80% is required to obtain the requested power. It can be seen that during these times, the controller is unable to regulate the current, leading to propagation of the input ripple. This saturation limit was one of the driving criterion in designing the maximum allowable voltage swing in the PFC output.

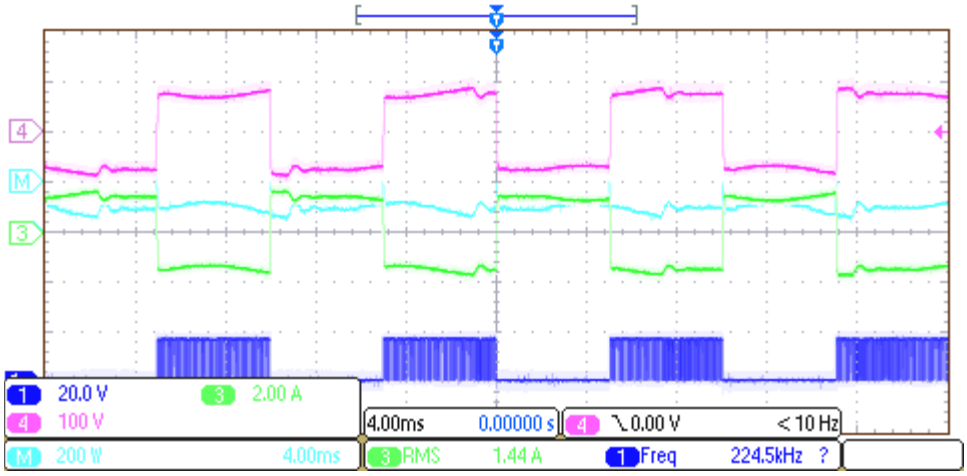


Figure 6.14: Steady-state operation of 50 Ω load. Vg = 110 VDC ±10 V 120 Hz. Gate B waveform (CH1), Lamp Current (CH3), Lamp Voltage (CH4), Lamp power (MATH)

Figure 6.15 shows a 10 Ω load on the second stage fed with a ±20 V 120 Hz ripple with a 120 V DC bias. The duty cycle is not varying much, as the input voltage is at the peak of an AC ripple, so the voltage is relatively constant. The duty cycle in Figure 6.16 is varying in order to compensate for a changing input voltage from the PFC. The two waveform captures demonstrate the controller modifying the duty cycle in order to cancel out the 120 Hz ripple.

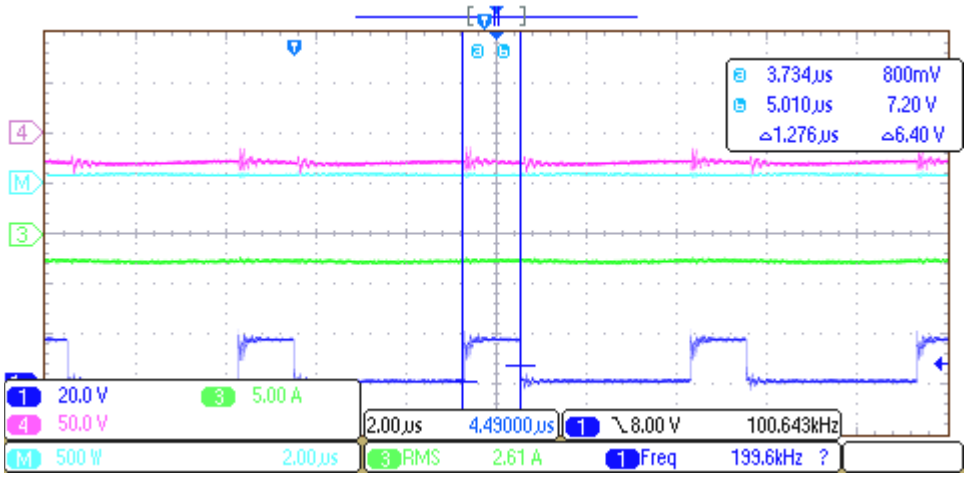


Figure 6.15: Steady-state operation of 10 Ω load. Vg = 120 VDC ±20 V 120 Hz. Peak of AC signal. Gate B waveform (CH1), Lamp Current (CH3), Lamp Voltage (CH4), Lamp power (MATH)

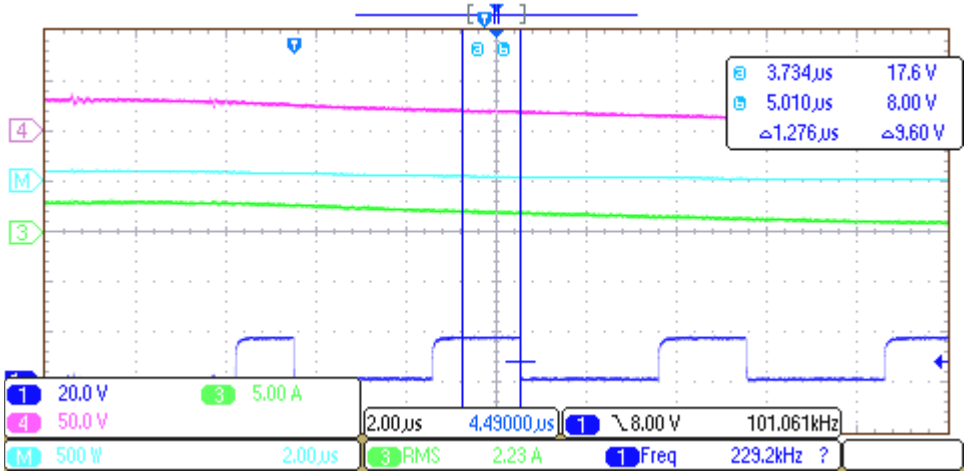


Figure 6.16: Steady-state operation of 10 Ω load. Vg = 120 VDC ±20 V 120 Hz. Gate B waveform (CH1), Lamp Current (CH3), Lamp Voltage (CH4), Lamp power (MATH)

Six periods of LFSW operation were taken on a Tektronix DPO2014 scope with an 80 µs sampling period. Harmonic power was calculated from the lamp voltage and lamp current waveforms using the Fast Fourier Transform, and the largest harmonic at 200 Hz was found to

be 4.7% of the total lamp power, meeting the 5% criterion found in [32]. The resulting single sided Fast Fourier Transform (FFT) of the lamp power is shown in Figure 6.17. The peaks of the FFT correspond to 200 Hz, which is the LFSW mode transition frequency. At the resonant frequency of the buck circuit (around 20 kHz), there is a small peak that is well below the 5% threshold.

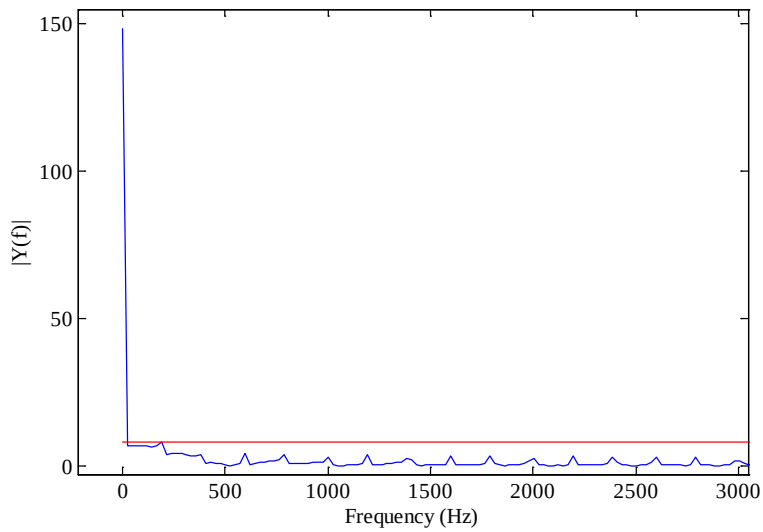


Figure 6.17: Single-sided FFT of lamp power (blue), 5% threshold (red)

It has been empirically shown that the input ripple is rejected by the system, and that the lamp operates without acoustic resonance. This suggests that the current loop is fast enough to compensate for the regions of the HID lamp that can exhibit a negative incremental impedance, and that the power loop is able to stabilize the lamp power, and does not interact negatively with the inner current loop. An experimental setup was constructed in order to verify loop gain of the system, thereby validating the small signal models presented in earlier chapters. The simplified block diagram of the test setup is shown in Figure 6.18. The perturbation injection was achieved by placing a 50 Ω resistor, R_i, in series with the high impedance node of the ADC voltage input. A voltage was induced across the resistor through an isolation transformer that was constructed

out of a Tektronix P6021 AC current probe. The probe has an internal 125 turns as a primary, and 35 turns of 26 AWG insulated copper wire was used as the secondary.

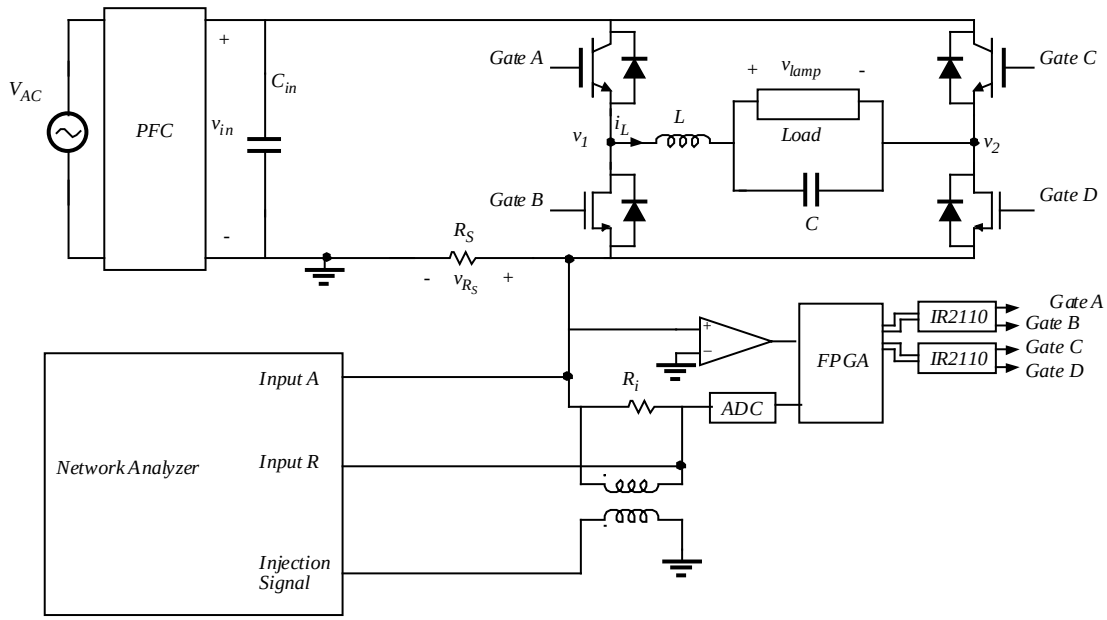


Figure 6.18: Test setup for loop gain measurement

The results of the magnitude plot of $\frac{A}{R}$ for the system running in a constant positive buck mode with a 50 Ω load is shown in Figure 6.19. It is suspected that data below 1 kHz may not be trustable, as the system in question is a PI, causing lower frequency measurements to be somewhat more difficult to obtain. The input injection was manually reduced for lower frequency measurement in order to counteract the integral action of the controller, but the exact amount that would produce the optimal plots was not studied in detail. Additionally, the transfer function characteristics of the isolation transformer built from a current probe is not well-known. The important characteristic of the magnitude plot is the crossover frequency, which is just above 3 kHz. Comparing this to the results of the models shown in previous chapters, this is close to the designed values, and my represent a possible mismatch between theory and implementation of approximately 5-10 dB.

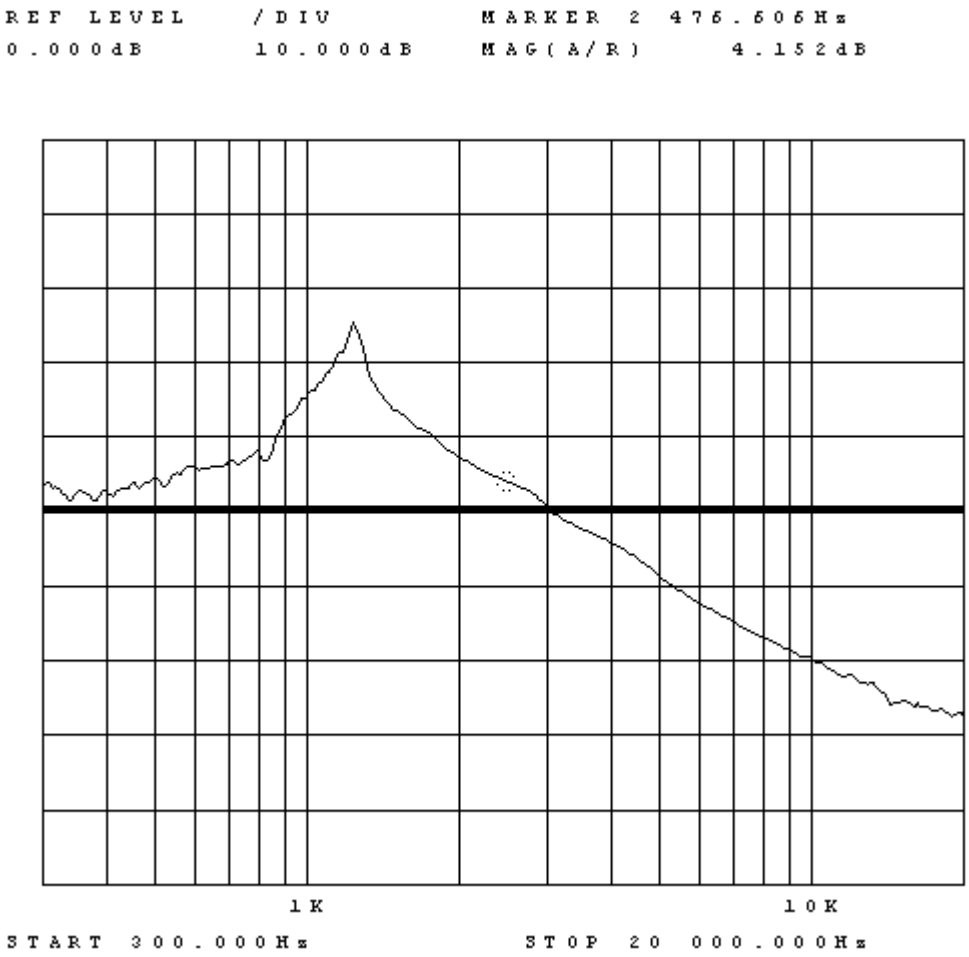


Figure 6.19: Magnitude plot of current controlled loop gain with 50 Ω load

6.4 Summary

Through experimentation, it has been shown that the ballasts designed in previous chapters are capable of utilizing soft saturation core materials in order to reduce size and weight of the total ballast solution. Ignition voltages were reduced from the manufacturer rated specifications through use of a slow voltage ramp accomplished by a phase sweep towards resonance. Ignition was detected using a phase surveillance method, and two warm-up designs were experimentally verified. The resonant ignition and resonant warm-up ballast design featured a slightly larger inductor when compared to the LFSW warm-up design. The LFSW

warm-up and steady state ballast was shown to be capable of acoustic resonance free operation, through use of an inner current loop. Experimental verification of the loop gain was performed. Power loop experimentation showed power levels of the lamp were regulated. A large input voltage ripple perturbation was introduced to the system, and acoustic resonance free operation was observed.

7 Possible Extensions and Conclusions

7.1 Conclusions

The work proposes novel analysis and design criteria for HID ballasts. Design of an HID ballast in the 150 W range has been carried out in order to validate the proposed design methodology. The background information covers the difficulties of HID lamp operation including acoustic resonance avoidance, cataphoretic phenomenon, ignition concerns, electrode sputtering, and lamp stability.

Considering these constraints, a resonant mode ignition is selected in order to minimize parts, and to allow for the large voltage increase required for ignition. For the steady-state operation, a LFSW topology was used in order to account for the possibility of acoustic resonance within the lamp. The constraints for good LFSW operation included fast transitions between positive and negative buck modes in order to reduce the chance of re-ignitions as well as reduce the harmonic power to below a specified 5% threshold of DC power. The LFSW operation is also tasked with being able to control warm-up of the lamp as well as regular operation. During the warm-up, the lamp large signal impedance is continuously increasing until it reaches a steady-state value. During this transition, a 150W lamp could have resistances that vary between 10-150 Ω. A two loop control approach contains a fast inner loop that controls lamp current, thereby stabilizing the arc, and a slower outer loop that controls input power controls total lamp power.

7.1.1 Soft saturation core for ignition

One contribution of the work is the use of a soft saturation material in order to reduce the core size of the inductor. A hard saturation inductor required to be oversized due to the large volt-seconds seen on the inductor during ignition. The soft saturation core inductor allowed for a smoother saturation with a smaller core at the cost of having a variable inductance. Since the effective inductance of the inductor with a soft saturation core is variable, the resonance of the system is also variable. This motivated the use and analysis of phase control for the ignition. A design method is presented in how to select a core, and design the inductor in order to achieve resonant ignition while still having proper inductance for steady-state operation.

7.1.2 Fast transition to LFSW warm-up

Another contribution is the fast transition from ignition to warm-up. Previously, solutions to HID lamp warm-up included operating the lamp in a resonant mode for a given amount of time in order to warm up the lamp. Operation in a resonant mode can lead to acoustic resonance if the lamp dynamics are not known, and the operating frequency of the ballast falls within an acoustic resonance prone frequency band. With a transition from resonant ignition to LFSW operation before the lamp has time to warm-up increases the range of possible lamp impedances the LFSW mode will encounter. With the LFSW topology, the transition times between positive and negative modes require an acceptable natural frequency and Q factor of the buck filter response. As previously mentioned, fast transitions are crucial to maintaining correct lamp operation. Experimentation shows that the designed system is able to sustain LFSW operation much sooner than previous LFSW circuits with resonant ignition have achieved. This

reduces the chance of acoustic resonance during warm-up, and allows for greater flexibility in the current envelope of the warm-up of the lamp.

7.1.3 Fast mode transition switching method

The switching times from positive to negative buck modes and vice versa were increased using an inductor zero crossing method. This provided a faster transition between modes at a rate that could be considered the fastest possible with a given input voltage. With the full bridge topology selected, transitions between LFSW modes began with conduction of current through a body diode and an anti-parallel diode in the circuit. This continued until the diodes were reverse biased, as the current in the inductor was able to change polarity. By measuring the time it took the inductor to reach 0 current, it was found that repeating this time in a 100% duty cycle fashion allowed for a fast transition to the opposite current polarity of the same magnitude. This analysis assumes the load resistance remains constant during the transition. Limitations of this fast transition mode include a possibility of error if the lamp is operating in a rectifying mode, as this could cause under or overshoot during a transition.

7.1.4 *Q* factor control from soft saturation core

With the increased range of lamp impedance values expected, this translated to a large range of variation in *Q* factor for designs using a linear inductor. Use of the soft saturation core inductor allowed for the tuning of this range, and analysis was presented on how to design the inductor to obtain desired *Q* factor range suppression.

7.1.5 Analysis of output power control from input power sensing

The control of the system was chosen to allow for output current sensing and input voltage sensing, as these sense points would already be present an LFSW system. A design constraint of reducing power harmonics seen at the output of the system to below 5% of the total power was imposed in order to reduce the chance of acoustic resonances. Analysis is presented on the control of the output power by sensing the input power. The inner power loop controlling lamp current was designed with a crossover frequency of around 3-10 kHz in order to account for lamp arc stability. The outer loop was designed in order to be fast enough to allow for the lamp resistance change during warm-up, and slow enough to not interact with the current loop which was responsible for attenuation of the 120 Hz ripple from a first stage PFC below the 5% threshold.

7.1.6 Analysis of constraints of LFSW operation

Constraints for the correct operation of LFSW mode were analyzed and presented. A test methodology for assuring the harmonic power was below a given threshold was researched. Empirically, the 5% threshold was met, and the presence of acoustic resonance was not seen.

7.1.7 New constraint for PFC output capacitor sizing

From this control analysis, design constraints on the output capacitor of a PFC were presented. A lower bound on the bandwidth of the input power control loop was found by analyzing possible lamp resistance changes during operation. With an allowable reduction in output capacitance, system lifetime could possibly be improved. High capacitance values are typically obtained by using electrolytic capacitors which are bulky, but more are usually one of the first components to fail in a power system. By allowing for a lower capacitance, either a

different capacitor technology could be employed, or a greater allowance of capacitance derating during the lifetime of electrolytic capacitors could be acceptable. This results directly to improved robustness of a lighting system, and can lead to commercial benefits.

7.2 Possible Extensions

7.2.1 Extension of soft saturation core model validity

The information from the manufacturer about the soft saturation core material relative permeability vs. DC magnetizing force was presented as a fourth order polynomial as well as a graphic in a data sheet. Using the fourth order polynomial function, a close fit to the graphic was seen until upper regions of the DC magnetizing force. Figure 6.1 demonstrates this mismatch, as well as a proposed sigmoid based curve fit.

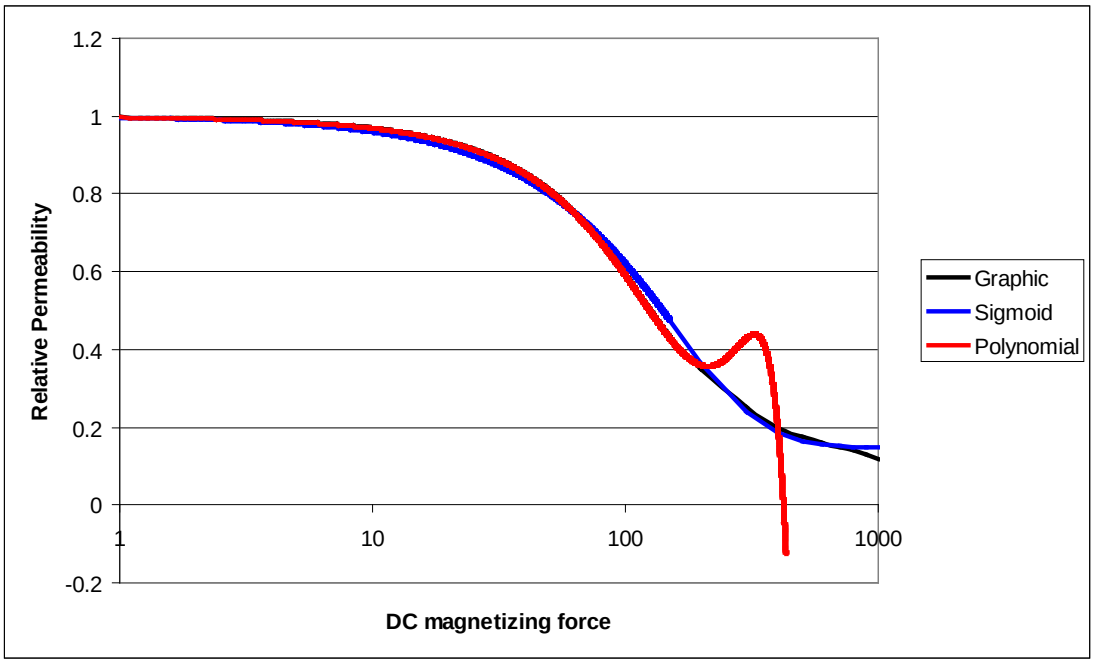


Figure 7.1. Comparison of provided model and proposed sigmoid to provided graph of relative permeability to DC magnetizing force.

The equation for the sigmoid fit was found to be:

$$\frac{A_1}{1+e^{B_1\frac{H}{Lm\cdot turns}}}+C_1 \quad , \tag{7.1}$$

where $Lm = 5.88$ is the magnetic path length in cm, H is the DC magnetizing force in Ampere turns/cm, and $A_1 = 1.7$, $B_1 = 0.15$, $C_1 = 0.35$ are the curve fit parameters.

It can be seen that the provided polynomial curve fit does not follow the provided graphic data past a DC magnetizing force of around 150. By extending the possible relative permeability range to lower levels, it has been shown in earlier sections that the variance in quality factor for the buck filter response can be further suppressed. In this study, by trusting the model up until the point mentioned, a relatively linear region of inductance to DC magnetizing force could be found, thus making finding the maximum and minimum *Q* factors simple, in that they coincided with the maximum and minimum currents through the inductor. With the extension of the model range, the extremes of quality factor could occur somewhere near the lower knee of the sigmoid. This would complicate core selection. This work would require communication with the core manufacturer to verify models.

7.2.2 Modification of ballast to accept High Brightness LED loads

Since the ballast is essentially a current source that tunes the current reference to obtain a certain power, the circuit could theoretically control High Brightness LED (HBLED) circuits. Current control is the control method of choice for HBLEDs due to their exponential response to voltage variations past the knee of the IV curve. In this work, time constant comparisons would have to be made, and a decision of whether LFSW operation could benefit the system.

One potential benefit of this system could be parallel operation of HBLED and HID lamps. The HBLEDs could provide faster turn on at the users request, avoiding such issues as hot-restrike and warm-up, while the HID lamp could provide higher overall efficacy and better color temperature.

Operation of HBLEDs would release the requirement of acoustic resonance avoidance, but add in a more stringent constraint of reduction of perturbations in the human visible frequency range around 10 Hz due to their faster time constants.

7.2.3 Empirical testing of ignition voltages and hot-restrike

In this study, lower than manufacturer suggested ignition voltages were observed due to slow ramping of lamp voltage prior to ignition. This has been observed in other studies [2], [8], but has not been fully quantified. In order to study this and possibly describe what is happening at the lamp level would take many lamps and many ignition attempts in a controlled environment. Possible factors affecting this low voltage ignition include electrode temperature, tube pressure, rate of voltage ramp increase, etc.

Additionally, this study did not address hot-restrike conditions, in which the user requests a lamp ignition shortly after the lamp has come up to full power, and then been powered down again. Manufacturer specifications suggest hot-restrike can require in the order of 30 kV. A study on cool down periods for various lamps could be performed. Also, since the electrode temperature would affect the lamp large signal impedance, it may be possible to detect the lamp impedance using phase control below resonance. By monitoring the requested phase and comparing the magnitude of the output voltage, the Q factor may be able to be found, thus allowing the state of the lamp to be known.

7.2.4 Lamp dimming with soft saturation core material

An assumption of full power was present for the steady-state operation of the HID lamps in this study. Addition of the possibility of lamp dimming complicates the design [59] as this modifies the Q factor suppression shown in chapter 5. One possibility to allow for dimming could be to shape the BH loop of the inductor to account for the different current levels to be encountered by the inductor. The shaping of the BH loop could be performed by a design procedure that would allow for a set parametric variance. Another method could include adaptively changing the core magnetizing force by running a second winding through the core with the purpose of introducing a DC current bias to the core. The secondary winding could comprise of many turns, and feed a very low resistance in order to reduce power loss.

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Appendix A – Selected VHDL Modules

This appendix presents example key VHDL modules for operation of the full HID ballast including resonant ignition and LFSW steady state operation.

Each module includes:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_acoustic resonanceITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
```

A.1 Top Level Module

```
entity main is
port(clock:         in    std_logic;         --Clock: 50MHz
     HB_Current:    in    std_logic;         --If high, goto kill switch
          zero_cross:    in    std_logic;     --zero cross
          Gate_out:      inout std_logic;     --Driver signal. NI-logic
          Gate_1_hi_o:   out   std_logic;     --Driver signal. NI-logic
          Gate_1_lo_o:   out   std_logic;     --Driver signal. NI-logic
          Gate_2_hi_o:   out   std_logic;     --Driver signal. NI-logic
          Gate_2_lo_o:   out   std_logic;     --Driver signal. NI-logic
          Gate_out2:     out   std_logic;     --Driver signal. NI-logic
          sd_1:          out   std_logic;
          sd_2:          out   std_logic;

-----Chipscope inputs
--        Reset:         in    std_logic;                     --Reset button
--        chooser:       in    std_logic;                     --choose button
--        phase_cmd:     in    std_logic_vector(3 downto 0);
--Requested PHASE from toggle switches.
--        phase_add_1:   in    std_logic;
--        phase_add_2:   in    std_logic;
--        phase_add_3:   in    std_logic;
--        freq2_choose:  in    std_logic;

-----Chipscope outputs
          choice_out:    out   std_logic;                     --choice signal
          stater:        out   std_logic_vector(2 downto 0);
          out_count:     out   std_logic_vector(8 downto 0);
          T_delay_read:  out   std_logic_vector(8 downto 0);
          bits_in:       in    std_logic_vector(7 downto 0);
          EOC:           in    std_logic;
          RD:            out   std_logic;
          CS:            out   std_logic;
          CONVST:        out   std_logic;
          bits_inV:       in    std_logic_vector(7 downto 0);
          EOCV:           in    std_logic;
          RDV:            out   std_logic;
          CSV:            out   std_logic;
          CONVSTV:        out   std_logic;
          zero_cross_anded_o: out std_logic
          );
end main;

-------------------------------------------------------
architecture Behavioral of main is

constant Start  : std_logic_vector(2 downto 0) := "000";
```

```
constant Low1   : std_logic_vector(2 downto 0) := "001";
constant High   : std_logic_vector(2 downto 0) := "011";
constant High2  : std_logic_vector(2 downto 0) := "010";
constant Low2   : std_logic_vector(2 downto 0) := "100";
constant Frozen : std_logic_vector(2 downto 0) := "111";
-------------------------------------------------------

  ------------------------------------------------------------------
  ------------------------------------------------------------------
  --  ICON core component declaration
  ------------------------------------------------------------------
  component icon
    port
    (
      control0    :   out std_logic_vector(35 downto 0);
      control1    :   out std_logic_vector(35 downto 0)
    );
  end component;
  ------------------------------------------------------------------
  --  VIO core component declaration
  ------------------------------------------------------------------
  component vio
    port
    (
      control     : in    std_logic_vector(35 downto 0);
      async_in    : in    std_logic_vector(31 downto 0);
      async_out   :   out std_logic_vector(31 downto 0)
    );
  end component;
  ------------------------------------------------------------------
  --  ILA core component declaration
  ------------------------------------------------------------------
  component ila
    port
    (
      control     : in    std_logic_vector(35 downto 0);
      clk         : in    std_logic;
      data        : in    std_logic_vector(15 downto 0);
      trig0       : in    std_logic_vector(0 downto 0)
    );
  end component;
  ------------------------------------------------------------------
  ------------------------------------------------------------------

-------------------------------------------------------
component state_logic is
port(current_state:           in  std_logic_vector( 2 downto 0);
       count:                 in  std_logic_vector(12 downto 0);
       count2:                in  std_logic_vector(13 downto 0);
       T_delay:               in  std_logic_vector(23 downto 0);
       Ts:                    in  std_logic_vector(12 downto 0);
       next_state:            out std_logic_vector( 2 downto 0);
       Gate_out:              out std_logic
         );
end component;
-------------------------------------------------------

-------------------------------------------------------
component state_registers is
port(   reset:             in  std_logic;
       next_state:         in  std_logic_vector(2 downto 0);
       T_delay_hold:       in  std_logic_vector(23 downto 0);
       clock:              in  std_logic;
       HB_current:         in  std_logic;
       zero_cross:         in  std_logic;
       current_state:      out std_logic_vector(2 downto 0);
       count:              inout std_logic_vector(12 downto 0);
       count2:             inout std_logic_vector(13 downto 0);
       lamp_detect:        out std_logic;
```

```
        out_count:         out std_logic_vector(8 downto 0);
        T_delay:           out std_logic_vector(23 downto 0);
        T_delay_read:      out std_logic_vector(8 downto 0);
        Ts:                out std_logic_vector(12 downto 0)
          );
end component;
-------------------------------------------------------

-----------------------------------------------------
component debounce is
port( debounce_in:            in  std_logic;
        clock:                in  std_logic;
        debounce_out:         out std_logic
          );
end component;
-----------------------------------------------------

-----------------------------------------------------
component debounce2 is
port( debounce_in:            in  std_logic;
        clock:                in  std_logic;
        debounce_out:         out std_logic
          );
end component;
-----------------------------------------------------

-----------------------------------------------------
component debounce3 is
port( debounce_in:            in  std_logic;
        clock:                        in  std_logic;
        debounce_out:         out std_logic
          );
end component;
-----------------------------------------------------

-----------------------------------------------------
component debounce4 is
port( debounce_in:            in  std_logic;
        clock:                in  std_logic;
        debounce_out:         out std_logic
          );
end component;
-----------------------------------------------------

-----------------------------------------------------
component freq is
port(clock:                   in std_logic;
        HB_Current:           in std_logic;
        Reset:                in std_logic;
        Gate_out:             out std_logic;
        freq2_choose:         in std_logic;
        period_in:            in std_logic_vector (12 downto 0);
        count:                inout std_logic_vector(12 downto 0)
          );
end component;
-----------------------------------------------------

-----------------------------------------------------
component Phase_Control is
port(lamp_on  : in  STD_LOGIC;
     clk      : in  STD_LOGIC;
     reset    : in  STD_LOGIC;
     on_phase : out  STD_LOGIC_vector (7 downto 0)
          );
end component;
-----------------------------------------------------

-----------------------------------------------------
component gate_control is
```

```
port( clock:           in  std_logic;
        gate_master:   in  std_logic;
        Gate_1_hi:     out std_logic;
        Gate_1_lo:     out std_logic;
        Gate_2_hi:     out std_logic;
        Gate_2_lo:     out std_logic;
        filter:        out std_logic;
        current_state: in  std_logic_vector (2 downto 0)
          );
end component;
-------------------------------------------------------

-------------------------------------------------------
component gate_cntrl_LFSW is
port( clock:           in  std_logic;
        chooser:       in  std_logic;
        duty:          in  std_logic_vector (8 downto 0);
        zero_cross:    in  std_logic;
        open_loop_sig: out std_logic;
        LFSW_mode_out: out std_logic;
        Gate_1_hi:     out std_logic;
        Gate_1_lo:     out std_logic;
        Gate_2_hi:     out std_logic;
        Gate_2_lo:     out std_logic;
        trigger:       out std_logic;
        gate_sig:      out std_logic
          );
end component;
-------------------------------------------------------

-------------------------------------------------------
component ADC_cntrl is
port( clock:           in  std_logic;
read_request:  in  std_logic;
EOC:           in  std_logic;
CONVST:        out std_logic;
CS:            out std_logic;
RD:            out std_logic;
bits_in:       in  std_logic_vector (7 downto 0);
bits_out:      out std_logic_vector (7 downto 0)
          );
end component;
-------------------------------------------------------

-------------------------------------------------------
component PID_cntrl is
port( clock:           in  std_logic;
switch_detect: in  std_logic;
ADC_in:        in  std_logic_vector (7 downto 0);
ref_in:        in  std_logic_vector (5 downto 0);
open_loop_sig: in  std_logic;
LFSW_mode_out: in  std_logic;
chooser:       in  std_logic;
duty_out:      out std_logic_vector (8 downto 0)
          );
end component;
-------------------------------------------------------

-------------------------------------------------------
component power_integ_cntrl is
port( clock:           in  std_logic;
trigger:       in  std_logic;
gate_sig:      in  std_logic;
ADC_in:        in  std_logic_vector (7 downto 0);
v_in:          in  std_logic_vector (7 downto 0);
duty_in:       in  std_logic_vector (8 downto 0);
chooser:       in  std_logic;
open_loop_sig: in  std_logic;
error_out:     out std_logic_vector (15 downto 0);
```

```
ref_out:       out std_logic_vector (5 downto 0)
               );
end component;
-----------------------------------------------------


-----------------------------------------------------
       COMPONENT clock_doubler
       PORT(
CLKIN_IN :     IN std_logic;
               RST_IN :          IN std_logic;
               CLKIN_IBUFG_OUT : OUT std_logic;
               CLK0_OUT :        OUT std_logic;
               CLK2X_OUT :       OUT std_logic
               );
       END COMPONENT;
-----------------------------------------------------

    -- define the states of FSM model
    signal next_state:       std_logic_vector(2 downto 0);
         signal current_state:    std_logic_vector(2 downto 0);
         signal lamp_detect:      std_logic;
         signal count:            std_logic_vector(12 downto 0);
         signal count2:           std_logic_vector(13 downto 0);
         signal Ts:               std_logic_vector(12 downto 0);
         signal T_delay:          std_logic_vector(23 downto 0);
         signal T_delay_hold:     std_logic_vector(23 downto 0);
         signal zero_cross_db:    std_logic;
         signal zero_cross_db2:   std_logic;
         signal zero_cross_anded: std_logic;
         signal phase_gate:       std_logic;
         signal freq_gate:        std_logic;
         signal freq_count:       std_logic_vector(12 downto 0);
         signal on_phase:         std_logic_vector(7 downto 0);
--       signal gate_out:         std_logic;
         signal OC_check:         std_logic;
         signal Gate_1_hi:        std_logic;
         signal Gate_1_lo:        std_logic;
         signal Gate_2_hi:        std_logic;
         signal Gate_2_lo:        std_logic;
         signal filter:           std_logic;
         signal Gate_1_hi_LFSW:   std_logic;
         signal Gate_1_lo_LFSW:   std_logic;
         signal Gate_2_hi_LFSW:   std_logic;
         signal Gate_2_lo_LFSW:   std_logic;
         signal trigger:          std_logic;
         signal gate_sig:         std_logic;
         signal duty:             std_logic_vector(5 downto 0);
         signal choice:           std_logic;
         signal freq2_choose:     std_logic;
         signal reset:            std_logic;
         signal chooser:          std_logic;
         signal phase_cmd:        std_logic_vector(3 downto 0);
         signal phase_add_1:      std_logic;
         signal phase_add_2:      std_logic;
         signal phase_add_3:      std_logic;
         signal period_in:        std_logic_vector(12 downto 0);
         signal phase_choose:     std_logic;
         signal lamp_sweep:       std_logic;
         signal duty_out:         std_logic_vector(8 downto 0);
         signal open_loop_sig:    std_logic;
--       signal ADC_in:           std_logic_vector(7 downto 0);
--       signal switch_detect:    std_logic;
--       signal bits_in:          std_logic_vector(7 downto 0);
         signal bits_out:         std_logic_vector(7 downto 0);
         signal bits_outV:        std_logic_vector(7 downto 0);
--       signal EOC:              std_logic;
--       signal RD:               std_logic;
--       signal CS:               std_logic;
```

```
--      signal CONVST:           std_logic;
        signal ref_in:           std_logic_vector(5 downto 0);
        signal HB_current_db:    std_logic;
        signal chooser_db:       std_logic;
        signal eoc_out:          std_logic;
        signal clock_ibuf:       std_logic;
        signal CLK2X_OUT:        std_logic;
        signal LFSW_mode_out:    std_logic;
        signal error_out:        std_logic_vector (15 downto 0);
        signal ref_out:          std_logic_vector(5 downto 0);



  ------------------------------------------------------------------
  --  ICON core signal declarations
  ------------------------------------------------------------------
  signal control0       : std_logic_vector(35 downto 0);
  signal control1       : std_logic_vector(35 downto 0);
  ------------------------------------------------------------------
  --  VIO core signal declarations
  ------------------------------------------------------------------
  --signal control   : std_logic_vector(35 downto 0);
  signal async_in    : std_logic_vector(31 downto 0);
  signal async_out   : std_logic_vector(31 downto 0);
  ------------------------------------------------------------------
  --  ILA core signal declarations
  ------------------------------------------------------------------
  --signal control   : std_logic_vector(35 downto 0);
  signal clk        : std_logic;
  signal data       : std_logic_vector(15 downto 0);
  signal trig0      : std_logic_vector(0 downto 0);
  ------------------------------------------------------------------

begin
--  RD     <= '0';
--  CS     <= '0';
--  Convst <= '0';
  sd_1   <= '0';         --enable for gate drive 1
  sd_2   <= '0';         --enable for gate drive 2
  eoc_out <= eoc;

-- these bits are used to troubleshoot modes and output bits
--  stater <= current_state(2 downto 0);   --show state on LEDs
  stater <= (lamp_detect & OC_check & current_state(1));  --show if the circuit thinks the lamp
is on w/ LEDs
  zero_cross_anded <= (zero_cross) and filter;
  zero_cross_anded_o <= zero_cross_anded;

-------------------------------------------------------------
--chipscope assignments
--outputs

  trig0(0) <= LFSW_mode_out;
  data(10 downto 3) <= bits_out(7 downto 0);
  data(15) <= Gate_1_lo_LFSW or Gate_2_lo_LFSW;
  data(14) <= Gate_1_hi_LFSW;
  data(13) <= Gate_1_lo_LFSW;
  data(12) <= Gate_2_hi_LFSW;
  data(11) <= Gate_2_lo_LFSW;

--inputs
  freq2_choose <= async_out(0);
  Reset <= async_out(1);
  --chooser <= async_out(2);
  chooser <= lamp_detect and not(lamp_sweep);  -- for automatic transition

  phase_cmd <= async_out(6 downto 3);
  phase_add_1 <= async_out(7);
  phase_add_2 <= async_out(8);
```

```
  phase_add_3 <= async_out(9);
  period_in <= async_out(22 downto 10);
  phase_choose <= async_out(23);
  choice <= async_out(24);
  lamp_sweep <= async_out(25);
  ref_in <= async_out(31 downto 26);

-------------------------------------------------------------

  --Combinational for T_delay - Voltage sense
--  T_delay_hold <= ("00" & phase_add_3 & phase_add_2 & phase_add_1 & on_phase(5 downto 0)) * Ts;
-- & '0'

 process(on_phase, phase_add_3, phase_add_2, phase_add_1, phase_choose, Ts)
   begin
               if (phase_choose = '0') then
                 T_delay_hold <= ("000" & on_phase(7 downto 0)) * Ts; --& '0'
-- purely done by phase_control module
               else
                 T_delay_hold <= ("00" & phase_add_3 & phase_add_2 & phase_add_1 & phase_cmd(3
downto 0)) * Ts;
               end if;
        end process;

--  T_delay_hold <= ("000" & on_phase(7 downto 0)) * Ts; --& '0'
-- purely done by phase_control module
--  T_delay_hold <= ("000000" & phase_cmd ) * Ts;

  process(choice, phase_gate, freq_gate)
    begin
          if ((choice = '1') ) then
                  Gate_out  <= phase_gate;
                  Gate_out2 <= freq_gate;
                  choice_out <= '1';
     elsif ((choice = '0') ) then
                  Gate_out  <= freq_gate;
                  Gate_out2 <= phase_gate;
                  choice_out <= '0';
          end if;
         end process;

-- check if overcurrent, if not, assign gates either resonant or LFSW gate signals
  process(OC_check, Gate_1_hi, Gate_1_lo, Gate_2_hi, Gate_2_lo)
    begin
          if (OC_check = '1') then
--             Gate_1_hi_o <= '0';
--             Gate_1_lo_o <= '1';
--             Gate_2_hi_o <= '0';
--             Gate_2_lo_o <= '1';
               Gate_1_hi_o <= Gate_1_hi;
               Gate_1_lo_o <= Gate_1_lo;
               Gate_2_hi_o <= Gate_2_hi;
               Gate_2_lo_o <= Gate_2_lo;


     else
             if (chooser_db = '0') then
                       Gate_1_hi_o <= Gate_1_hi;
                       Gate_1_lo_o <= Gate_1_lo;
                       Gate_2_hi_o <= Gate_2_hi;
                       Gate_2_lo_o <= Gate_2_lo;
                  else
                       Gate_1_hi_o <= Gate_1_hi_LFSW;
                       Gate_1_lo_o <= Gate_1_lo_LFSW;
                       Gate_2_hi_o <= Gate_2_hi_LFSW;
                       Gate_2_lo_o <= Gate_2_lo_LFSW;
                  end if;
          end if;
    end process;
```

```
  process(reset, HB_current_db)
    begin
if (reset = '1') then
        OC_check <= '0';
elsif (HB_current_db = '1') then
        OC_check <= '1';
end if;
end process;

  U0: state_logic     port map(       current_state => current_state,
                                      count         => count,
                                      count2        => count2,
                                      T_delay       => T_delay,
                                      Ts            => Ts,
                                      next_state    => next_state,
                                      Gate_out      => phase_gate);

  U1: state_registers port map(       reset         => reset,
                                      next_state    => next_state,
                                      T_delay_hold  => T_delay_hold,
                                      clock         => clock_ibuf,
                                      HB_current    => HB_current,
                                      zero_cross    => zero_cross_db,
                                      current_state => current_state,
                                      count         => count,
                                      count2        => count2,
                                      lamp_detect   => lamp_detect,
                                      out_count     => out_count,
                                      T_delay       => T_delay,

                       T_delay_read  => T_delay_read,
                                      Ts            => Ts);

  U2: debounce        port map(       debounce_in   => zero_cross_anded,
                                      clock         => clock_ibuf,
                                      debounce_out  => zero_cross_db);

  U25: debounce2      port map(       debounce_in   => HB_current,
                                      clock         => clock_ibuf,
                                      debounce_out  => HB_current_db);

  U26: debounce3      port map(       debounce_in   => chooser,
                                      clock         => clock_ibuf,
                                      debounce_out  => chooser_db);

  U27: debounce4       port map(      debounce_in   => zero_cross,
                                      clock         => clock_ibuf,
                                      debounce_out  => zero_cross_db2);

  U3: freq            port map(       clock         => clock_ibuf,
                                      HB_Current    => HB_current_db,
                                      Reset         => Reset,
                                      Gate_out      => freq_gate,

                       freq2_choose  => freq2_choose,
period_in     => period_in,
count         => freq_count);

  U4: Phase_Control   port map(       lamp_on       => lamp_sweep,
                                      clk           => clock_ibuf,
                                      reset         => lamp_sweep,
                                      on_phase      => on_phase);

  U5: gate_control    port map(       clock         => clock_ibuf,
                                      gate_master   => gate_out,
                                      Gate_1_hi     => Gate_1_hi,
                                      Gate_1_lo     => Gate_1_lo,
                                      Gate_2_hi     => Gate_2_hi,
```

```
                                    Gate_2_lo     => Gate_2_lo,
                                    filter        => filter,
                                    current_state => current_state);

  U6: gate_cntrl_LFSW port map(     clock         => CLK2X_OUT,
                                    chooser       => chooser_db,
                                    duty          => duty_out,
zero_cross    => zero_cross_db2,
                                    open_loop_sig => open_loop_sig,
                                    LFSW_mode_out => LFSW_mode_out,
                                    Gate_1_hi     => Gate_1_hi_LFSW,
                                    Gate_1_lo     => Gate_1_lo_LFSW,
                                    Gate_2_hi     => Gate_2_hi_LFSW,
                                    Gate_2_lo     => Gate_2_lo_LFSW,
                                    trigger       => trigger,
                                    gate_sig      => gate_sig);

  U7: ADC_cntrl       port map(     clock         => clock_ibuf,
                                    read_request  => gate_sig,
                                    EOC           => EOC,
                                    CONVST        => CONVST,
                                    CS            => CS,
                                    RD            => RD,
                                    bits_in       => bits_in,
                                    bits_out      => bits_out);

  U75: ADC_cntrl      port map(     clock         => clock_ibuf,
                                    read_request  => gate_sig,
                                    EOC           => EOCV,
                                    CONVST        => CONVSTV,
                                    CS            => CSV,
                                    RD            => RDV,
                                    bits_in       => bits_inV,
                                    bits_out      => bits_outV);

  U8: PID_cntrl       port map(     clock         => clock_ibuf,
                                    switch_detect => gate_sig,
--gate_sig  with falling_edge --eoc with rising_edge
                                    ADC_in        => bits_out,
ref_in        => ref_out,
-- ref_out 010110 for 50 ohm
--ref_out, -- 101010 for 100W w/ 10 ohm
--ref_out for power, ref_in for current
                              open_loop_sig  => open_loop_sig,
                              LFSW_mode_out  => LFSW_mode_out,
                              chooser        => chooser_db,
                                    duty_out       => duty_out);

  U85: power_integ_cntrl port map(  clock          => clock_ibuf,
                                    trigger        => trigger,
                                    gate_sig       => gate_sig,
                                    ADC_in         => bits_out,
                              v_in   => bits_outV,
                              duty_in => duty_out,
                              chooser => chooser_db,
open_loop_sig  => open_loop_sig,
                              error_out      => error_out,
ref_out        => ref_out);
  U9: clock_doubler   PORT MAP(     CLKIN_IN        => clock,
                       RST_IN          => reset,
                              CLKIN_IBUFG_OUT => clock_ibuf,
                              CLK0_OUT        => open,
                              CLK2X_OUT       => CLK2X_OUT);

  ------------------------------------------------------------------
  --  ICON core instance
  ------------------------------------------------------------------
  i_icon : icon
    port map
```

```
    (
      control0    => control0,
      control1    => control1
    );
  -----------------------------------------------------------------
  --  VIO core instance
  -----------------------------------------------------------------
  i_vio : vio
    port map
    (
      control   => control0,
      async_in  => async_in,
      async_out => async_out
    );
  -----------------------------------------------------------------
  --  ILA core instance
  -----------------------------------------------------------------
  i_ila : ila
    port map
    (
      control   => control1,
      clk       => clock_ibuf,
      data      => data,
      trig0     => trig0
    );
  -----------------------------------------------------------------
end Behavioral;
```

A.2 Phase Control Combinational Logic

```
entity state_logic is
port(current_state:           in  std_logic_vector(2 downto 0);
       count:         in  std_logic_vector(12 downto 0);
       count2:        in  std_logic_vector(13 downto 0);
       T_delay:                      in  std_logic_vector(23 downto 0);
       Ts:                           in  std_logic_vector(12 downto 0);
       next_state:           out std_logic_vector(2 downto 0);
       Gate_out:             out std_logic
         );
end state_logic;

architecture Behavioral of state_logic is

constant Start   : std_logic_vector(2 downto 0) := "000";
constant Low1    : std_logic_vector(2 downto 0) := "001";
constant High    : std_logic_vector(2 downto 0) := "011";
constant High2   : std_logic_vector(2 downto 0) := "010";
constant Low2    : std_logic_vector(2 downto 0) := "100";
constant Frozen  : std_logic_vector(2 downto 0) := "111";

signal T_delay_shifted: std_logic_vector(11 downto 0);
signal trans_01: std_logic_vector(12 downto 0);
signal trans_02: std_logic_vector(13 downto 0);

begin


-------------------------------------------------------------------------
         comb_logic1: process(T_delay, Ts)
    begin
                trans_01 <= (T_delay(22 downto 10)) ...
+ ("00" & Ts(12 downto 2)) - "0000000011101";

         end process;
-------------------------------------------------------------------------

-------------------------------------------------------------------------
```

```
        comb_logic2: process(T_delay, Ts)
    begin
                trans_02 <= ('0' & trans_01) ...
+ ("00" & Ts(12 downto 1)) - "0000000000000";
        end process;
-----------------------------------------------------------------------

    comb_logic: process(current_state, count, T_delay, Ts)
    begin

case current_state is

when Start =>  Gate_out <= '0';
       next_state <= Low1;

when Low1 =>   Gate_out <= '0';
               if (count = "0000000000000") then
                      next_state <= Low2;
               elsif (count2 >= trans_02) then
                      next_state <= High2;
               else
                      next_state <= Low1;
               end if;

       when Low2 =>   Gate_out <= '0';
               if (count2 >= trans_02) then
                      next_state <= High;
               else
                      next_state <= Low2;
               end if;
       when High =>   Gate_out <= '1';
               if ((count >= trans_01)) then
                      next_state <= Low1;
               else
                      next_state <= High;
               end if;

       when High2 =>  Gate_out <= '1';
               if ((count <= "0000000000000") or (('0' & count) < count2)) then
                      next_state <= High;
               else
                      next_state <= High2;
               end if;

       when Frozen => Gate_out <= '0';
               next_state <= Frozen;

       when others => Gate_out <= '0';
               next_state <= Frozen;
       end case;
    end process;
end Behavioral;
```

A.3 Phase Control Sequential Logic

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_acoustic resonanceITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

-------------------------------------------------------
entity state_registers is
port(reset:            in  std_logic;
       next_state:     in  std_logic_vector(2 downto 0);
       T_delay_hold:   in  std_logic_vector(23 downto 0);
       clock:          in  std_logic;
```

```
        HB_current:    in  std_logic;
        zero_cross:    in  std_logic;
        current_state: inout std_logic_vector(2 downto 0);
        count:         inout std_logic_vector(12 downto 0);
        count2:        inout std_logic_vector(13 downto 0);
        lamp_detect:   out std_logic;
        out_count:     out std_logic_vector(8 downto 0);
        T_delay:       out std_logic_vector(23 downto 0);
        T_delay_read:  out std_logic_vector(8 downto 0);
        Ts:            out std_logic_vector(12 downto 0)
          );
end state_registers;
-------------------------------------------------------

-------------------------------------------------------
architecture Behavioral of state_registers is

constant Start  : std_logic_vector(2 downto 0) := "000";
constant Low1   : std_logic_vector(2 downto 0) := "001";
constant High   : std_logic_vector(2 downto 0) := "011";
constant High2  : std_logic_vector(2 downto 0) := "010";
constant Low2   : std_logic_vector(2 downto 0) := "100";
constant Frozen : std_logic_vector(2 downto 0) := "111";

signal zero_detect:   std_logic;
signal old_Ts:        std_logic_vector(12 downto 0);

-------------------------------------------------------
begin
    state_reg: process(clock, reset, HB_Current, zero_cross)
    begin

        if (HB_Current='1') then
                current_state <= Frozen; --Freeze if over current
        elsif (reset='1') then
                T_delay <= "000000000000000000000001";
                T_delay_read <= "000000001";
                count <= (others => '0');
                count2 <= (others => '0');
                current_state <= Start;
                zero_detect <='0';
                Ts <= "0000010001110";
                old_Ts <= "0000010001110";
                lamp_detect <= '0';
        elsif (clock'event and clock='1') then    --On posedge(clock)
                if ((zero_detect = '0') and (zero_cross = '1')) then
                        if (count >= "0000000000000") then
                                zero_detect <= '1';
                                if (count >= "0000010001110") then
                                        if (count <= old_Ts - "0000010001110") then
                                                lamp_detect <= '1';
end if;
if ((count >= old_Ts) ...
and (count <= "0110100000101")) then
-- count <= max period
--15k 0110100000101
--18k 0101011011010
--22k 0100011100000
                                        if (count <= old_Ts + "0000000100000") then
                                                Ts <= count;
                                                old_Ts <= count;
                                                T_delay <= T_delay_hold;
                                        else
                                                Ts <= old_Ts + "0000000100000";
                                                old_Ts <= old_Ts + "0000000100000";
                                                T_delay <= T_delay_hold;
                        end if;
                                end if;
                        else
```

```
                        end if;


                        count <= (others => '0');
                end if;
                out_count <= count(8 downto 0);
        else
                if ((zero_detect = '1') and (zero_cross = '0')) then
                        if (count >= "0000000000000") then
                                zero_detect <= '0';
                                count2 <= '0' & count;
end if;
                end if;
                count <= count + 1;

                if (next_state = Low1) then
                        count2 <= ('0' & count) + 1;
                else
                        count2 <= count2 + 1;
                end if;

                        current_state <= next_state;
                        out_count <= count(8 downto 0);
                end if;
        end if;
    end process;
end Behavioral;
```

A.4 Gate controller

```
--accepts a single gate master signal and breaks it into 4 channels

entity gate_control is
port( clock:          in  std_logic;
        gate_master:   in  std_logic;
        Gate_1_hi:     out std_logic;
        Gate_1_lo:     out std_logic;
        Gate_2_hi:     out std_logic;
        Gate_2_lo:     out std_logic;
        filter:         out std_logic;
        current_state:  in  std_logic_vector(2 downto 0) );
end gate_control;

architecture Behavioral of gate_control is
signal count_1:  std_logic_vector(4 downto 0);
signal count_2:  std_logic_vector(4 downto 0);
signal count_f:  std_logic_vector(6 downto 0);
signal gate_1_h: std_logic;
signal gate_2_h: std_logic;
signal filter_h:   std_logic;
constant dead_time  : std_logic_vector(4 downto 0) := "10111";
constant hold_time  : std_logic_vector(6 downto 0) := "1100000";

begin
process (clock)
        begin

        if (clock'event and clock='1') then

-- gate 1
                if (gate_master = '0') then
                        gate_1_h <= '0';
                        count_1 <= (others => '0');
                else
                        if (count_1 < dead_time) then
                                count_1 <= count_1 + 1;
```

```
                        else
                                gate_1_h <= '1';
                        end if;
                end if;

-- gate 2
                if (gate_master = '1') then
                        gate_2_h <= '0';
                        count_2 <= (others => '0');
                else
                        if (count_2 < dead_time) then
                                count_2 <= count_2 + 1;
                        else
                                gate_2_h <= '1';
                        end if;
                end if;

-- filter logic
                if (gate_master = '0') then
                        filter_h <= '0';
                        count_f <= (others => '0');
                else
                        if (count_f < hold_time) then
                                count_f <= count_f + 1;
                        else
                                filter_h <= '1';
                        end if;
                end if;

        end if;

        filter <=  filter_h;

        if (current_state = "111") then
                Gate_2_lo <= '1';
                Gate_1_lo <= '1';
                Gate_1_hi <= '0';
                Gate_2_hi <= '0';
        else
                Gate_1_hi <= gate_1_h;
                Gate_2_lo <= gate_1_h;

                Gate_1_lo <= gate_2_h;
                Gate_2_hi <= gate_2_h;
        end if;
end process;
end Behavioral;
```

A.5 LFSW Gate controller

```
--controls gate under LFSW conditions. Different from Gate Controller
--because different switches are on, and PWM mode exists

entity gate_cntrl_LFSW is
port( clock:                    in  std_logic;  --doubled  (100 MHz, 10 ns period)
        chooser:                in  std_logic;
        duty:                   in  std_logic_vector(8 downto 0);
        zero_cross:             in  std_logic;
        open_loop_sig:          out std_logic;
        LFSW_mode_out:          out std_logic;
        Gate_1_hi:              out std_logic;
        Gate_1_lo:              out std_logic;
        Gate_2_hi:              out std_logic;
        Gate_2_lo:              out std_logic;
        trigger:                out std_logic;
        gate_sig:               out std_logic);
```

```
end gate_cntrl_LFSW;

architecture Behavioral of gate_cntrl_LFSW is

signal f_sw_count:     std_logic_vector( 9 downto 0);
signal LFSW_count:     std_logic_vector(12 downto 0);
signal fsw:            std_logic;
signal LFSW_mode:      std_logic;
signal LFSW_gate:      std_logic;
signal per_duty:       std_logic_vector( 8 downto 0);
signal TOC_counter:    std_logic_vector(12 downto 0);
signal count_up:       std_logic;
signal TOC_on_sig:     std_logic;
signal old_LFSW_mode:  std_logic;
signal open_loop_sign: std_logic;

begin

LFSW_mode_out <= LFSW_mode;
open_loop_sig <= open_loop_sign; --TOC_on_sig;  --open_loop_sign;

process(chooser,clock)
begin
if chooser = '0' then
f_sw_count <= "0000000000";
else
if(clock'event and clock='1') then
               if(f_sw_count>="0111110100")then
--  011111010 111110100  PWM period in clock cycles
                       f_sw_count <= "0000000000";
                       per_duty <= duty;
               else
                       f_sw_count <= f_sw_count+1;
               end if;
       end if;
end if;
end process;

process (clock, chooser, f_sw_count)
 begin
if chooser = '0' then
fsw  <= '0';
else
       if ((f_sw_count <= "0011111010"  )) then
--makes a 50% duty cycle to key off of for LFSW
               fsw  <= '1';
       else
               fsw  <= '0';
       end if;
end if;
end process;

process(fsw, chooser)
begin
if chooser = '0' then
LFSW_mode <= '0';
LFSW_count <= "0000000000000";
else
       if(fsw'event and fsw='1') then
               if(LFSW_count<="0000000100000")then
       --number of periods of PWM switch frequency for open loop
                       open_loop_sign <= '1';
               else
                       open_loop_sign <= '0';
               end if;

               if(LFSW_count>="0001111101000")then
               --0110010000 0011001000 LFSW switch period in PWM cycles
                       LFSW_count <= "0000000000000";
```

```
                        LFSW_mode<=not(LFSW_mode);
                else
                        LFSW_count <= LFSW_count+1;
                end if;

                if(LFSW_count>="0001111100110")then -- LFSW switch periods minus 2
                                --1111101000      50hz
                                --0011111010     200hz
                        trigger <= '1';
                else
                        trigger <= '0';
                end if;
        end if;
end if;
end process;

process (per_duty, clock, chooser, f_sw_count)
begin
if chooser = '0' then
        LFSW_gate  <= '0';
else
        if ((f_sw_count <= (per_duty) + "0000001010"  ) ...
        and (f_sw_count <= "0101110100")) then  --sets max duty, or trips on duty
                LFSW_gate  <= '1';
        else
                LFSW_gate  <= '0';
        end if;

        if ((f_sw_count <= (per_duty) ) and (f_sw_count <= "0101101010")) then
                --sets max duty, or trips on duty
                gate_sig  <= '1';
        else
                gate_sig  <= '0';
        end if;
end if;
end process;

process(clock, LFSW_mode)     -- TOC transient signal
begin
if chooser = '0' then
TOC_counter <= "0000000000000";
old_LFSW_mode <= LFSW_mode;
else
if(clock'event and clock='1') then
if (TOC_counter > "0000000000000") then
                        TOC_on_sig <= '1';
                else
                        TOC_on_sig <= '0';
                end if;
                if(old_LFSW_mode /= LFSW_mode) then
                        TOC_counter <= (OTHERS=>'0');
                        old_LFSW_mode <= LFSW_mode;
                        count_up <= '1';
                else
                        if ((count_up = '1') and (zero_cross ='0'))then
                                if (TOC_counter <= "0111110100000") then
--  0111110100000  =4000 clocks of 100 MHz
                                        TOC_counter <= TOC_counter + "000000000001";
                                else
                                        count_up <= '0';
                                end if;
                        else  --count_up = '0' or zero_cross = '1'
                                count_up <= '0';
                                if (TOC_counter > "0000000000000") then
                                        TOC_counter <= TOC_counter - "000000000001";
                                end if;
                        end if;
                end if;
end if;
```

```
end if;
end process;

process (LFSW_count, LFSW_gate, LFSW_mode, f_sw_count)
begin
if (LFSW_count<"0000000000001" and (f_sw_count <= "0001000000")) then
-- add in dead time as two cycle of Fsw --and (f_sw_count <= "00000010")
        Gate_1_hi <= '0';
        Gate_1_lo <= '0';
        Gate_2_hi <= '0';
        Gate_2_lo <= '0';
else
if (LFSW_mode = '0') then
                Gate_1_hi <= '1';
                Gate_1_lo <= '0';
                Gate_2_hi <= '0';
                Gate_2_lo <= LFSW_gate or TOC_on_sig;
--              Gate_2_lo <= LFSW_gate;
else
                Gate_1_hi <= '0';
                Gate_1_lo <= LFSW_gate or TOC_on_sig;
--              Gate_1_lo <= LFSW_gate;
                Gate_2_hi <= '1';
                Gate_2_lo <= '0';
        end if;
end if;
end process;
end Behavioral;
```

A.6 Current Loop Controller

```
--Named PID, Actually a PI controller
-- fixed point is 1/2^13 = 0.00012207,  divide everything by this

entity PID_cntrl is
port( clock:                  in  std_logic;
        switch_detect:        in  std_logic;
        ADC_in:               in  unsigned (7 downto 0);
        ref_in:               in  unsigned (5 downto 0);
        open_loop_sig:        in  std_logic;
        LFSW_mode_out:        in  std_logic;
        chooser:              in  std_logic;
      duty_out:               out signed (8 downto 0));
end PID_cntrl;

architecture Behavioral of PID_cntrl is
signal integrator_count:  signed (10 downto 0);
signal error:             signed ( 9 downto 0);
signal error_int:         signed (31 downto 0);
signal big_out:           signed (38 downto 0);
signal Kp:                signed (13 downto 0);
signal Ki:                signed (13 downto 0);

begin
Kp<="01100010001001";  --factor 1/2^13
Ki<="00000100110101";  --factor 1/2^13

process(LFSW_mode_out, big_out)
begin
     duty_out <= big_out(25 downto 17);
end process;

process(chooser, ref_in, ADC_in)
begin
if (chooser = '1') then
        error   <= signed('0' & ref_in & "000") - signed('0' & ADC_in & '0');
        --accounts for H
```

```
else
        error <= (OTHERS=>'0');
end if;
end process;

process(ADC_in, switch_detect, integrator_count, LFSW_mode_out)

begin

if falling_edge(switch_detect) then  --falling_edge(switch_detect)
        if (chooser = '0') then
                error_int        <= (OTHERS=>'0');
                big_out          <= "00000000000000001110010000000000000000";
        else
                if (open_loop_sig = '0') then
                        if ((error_int + Ki*(error)) ...
                        >= "0000000000010011000000000000000") then
                                error_int <= "0000000000010011000000000000000";
                        if ((big_out + "0000000000010011000000000000000" ...
                + Kp*(error)) >= "00000000000001011111000000000000000000") then
                                big_out <= "00000000000001011111000000000000000000";
                        elsif ((big_out + "0000000000010011000000000000000" + ...
                        Kp*(error)) <= "0000000000000000000000000000000000000") then
                                big_out <= "0000000000000000000000000000000000000";
                        elsif (true) then
                                big_out <= (big_out + ...
                                "0000000000010011000000000000000" + Kp*(error));
                        end if;



                        elsif ((error_int + Ki*(error)) <= ...
                        "1111111111101101000000000000000") then
                                error_int <= "1111111111101101000000000000000";
                                if ((big_out + "1111111111101101000000000000000" +...
                         Kp*(error)) >= "00000000000001011111000000000000000000") then
                                big_out <= "00000000000001011111000000000000000000";
                              elsif ((big_out + "1111111111101101000000000000000" +
        Kp*(error)) <= "0000000000000000000000000000000000000") then
                                     big_out <= ...
                                       "0000000000000000000000000000000000000";
                        elsif (true) then
                                big_out <= (big_out + ...
                                "1111111111101101000000000000000" + Kp*(error));
                        end if;

                        elsif (true) then
                                 error_int <= error_int + Ki*(error);
                                if ((big_out + error_int + Ki*(error) + Kp*(error)) ...
                                >= "00000000000001011111000000000000000000") then
                                  big_out <= "00000000000001011111000000000000000000";
                              elsif ((big_out + error_int + Ki*(error) + Kp*(error))...
                                <= "0000000000000000000000000000000000000") then
                                  big_out <= "0000000000000000000000000000000000000";
                        elsif (true) then
                         big_out <= (big_out + error_int + Ki*(error) + Kp*(error));
                end if;
             end if;
          end if;
        end if;
end if;
end process;
end Behavioral;
```

A.7 Power Loop Controller

```
--Controls current ref into current controller.
```

```
entity power_integ_cntrl is
port( clock:          in  std_logic;
        trigger:      in  std_logic;
        gate_sig:     in  std_logic;
        ADC_in:       in  std_logic_vector (7 downto 0);
        v_in:         in  std_logic_vector (7 downto 0);
        duty_in:      in  std_logic_vector (8 downto 0);
        chooser:      in  std_logic;
        open_loop_sig: in  std_logic;
        error_out:    out signed (15 downto 0);
        ref_out:      out signed (5 downto 0)
                );
end power_integ_cntrl;

architecture Behavioral of power_integ_cntrl is
signal error:             signed (16 downto 0);
signal big_out:           signed (28 downto 0);
signal error_chunk:       signed (16 downto 0);
begin
process(error)
begin
        error_chunk <= (error(16 downto 0));
        error_out   <= (error(15 downto 0));
end process;

process(big_out)
begin
        ref_out <= big_out(26 downto 21);
end process;

process(chooser, duty_in, ADC_in)
begin
        if (chooser = '1') then
                if ((signed('0' & ADC_in) * signed('0' & duty_in)) >= ...
                "01111111111111110") then  --bigger than twice
                        error <= "10000000000000010";  --makes one negative saturation
        else
                error <= ("00111111111111111") - (signed('0' & ADC_in) * ...
                signed('0' & duty_in)  ); --0100001111100000 for 150W with vin = 200VDC
        end if;
        else
      error <= (OTHERS=>'0');
   end if;
end process;
process(error_chunk, trigger)
begin
    if falling_edge(gate_sig) then  --falling_edge(switch_detect)
     --if (trigger = '1') then
          if (chooser = '0') then
                 big_out <= "00000111110000000000000000000";
                else

                 if (open_loop_sig = '0') then
                if ((big_out + error_chunk) >= "00110000000000000000000000000") then
--max of 4A 00111111000000000000000000000   max 3 00101111010000000000000000000
                     big_out <= "00110000000000000000000000000";
                 elsif ((big_out + error_chunk) <= "00000000000000000000000000000") then  --
negative reference protection
                          big_out <= "00000000000000000000000000000";
        elsif (true) then
                          big_out <= (big_out + error_chunk);
        end if;
      end if;
   end if;
end if;
end process;
end Behavioral;
```

A.8 Phase Sweep Controller

```
--controls sweep towards resonance
entity Phase_Control is
    Port     ( lamp_on  : in  STD_LOGIC;
               clk      : in  STD_LOGIC;
               reset    : in  STD_LOGIC;
               on_phase : out STD_LOGIC_vector (7 downto 0));
end Phase_Control;

architecture Behavioral of Phase_Control is

signal counter      : std_logic_vector (25 downto 0); -- 10 11111010 11110000 10000000
signal count        : std_logic_vector (7 downto 0);
signal ready_sweep  : std_logic;

begin
        phase_control: process (clk, reset)
        begin
        if (reset = '1')then
                on_phase    <= "00000001";      --01000000
                counter     <= (others => '0');
                count       <= (others => '0');
                ready_sweep <= '1';
        elsif (clk = '1' and clk'event) then
                if ((lamp_on = '0') and (ready_sweep = '1'))then
                        if (counter >= "00001011111010111100001000") then
                                count <= count + 1;
                                counter <= (others => '0');
                        else
                                counter <= counter + 1;
                                if ((count = "10101111") or (lamp_on = '1')) then
                                        ready_sweep <= '0';
                                end if;
                        end if;
                end if;
                on_phase <= count;
        end if;
end process;
end Behavioral;
```

A.9 ADC Controller

```
--Useful for controlling AD7822 half flash ADC
entity ADC_cntrl is
port( clock:           in  std_logic;
        read_request:  in  std_logic;
        EOC:           in  std_logic;
        CONVST:        out std_logic;
        CS:            out std_logic;
        RD:            out std_logic;
        bits_in:       in  STD_LOGIC_vector (7 downto 0);
        bits_out:      out STD_LOGIC_vector (7 downto 0));
end ADC_cntrl;

architecture Behavioral of ADC_cntrl is
signal CONVST_cnt: std_logic_vector(1 downto 0);
signal mst_count:  std_logic_vector(9 downto 0);
signal CS_reg:     std_logic;
signal RD_reg:     std_logic;

begin
CS       <= CS_reg;
RD       <= RD_reg;
process(read_request, clock, EOC)
begin
```

```
    if (rising_edge(EOC)) then
        bits_out <= bits_in;
    end if;
    if read_request='1' then
            mst_count<="0000000000";
        elsif rising_edge(clock) then
            if (mst_count<"0000000111") then
                    CONVST <= '0';
                else
                    CONVST <= '1';
                end if;
            if (EOC='0') then
                    CS_reg <= '0';
                else
                    CS_reg <= '1';
                end if;
            if (EOC='0' and CS_reg='0' and mst_count<"0001111111") then
                    RD_reg <= '0';
                else
                    RD_reg <= '1';
                end if;
            if (mst_count<"1111111111") then
                    mst_count <= mst_count+1;
                end if;
        end if;
end process;
end Behavioral;
```

Appendix B – Discrete and Continuous control-to-output

The following MATLAB code can be used to plot the discrete and continuous small signal models of a buck converter. The discrete small signal model is heavily dependent on the sampling frequency and delays in measurement. Further details can be found in [42].

```
%Discrete model of lamp ballast

%%%%%%%%%%%%%%data
P = 150;
R = 150;  %change to lamp resistance

%L calc for soft sat core
winds = 214;
Lm=5.88;
Al=34;
T=abs(sqrt(P/R))*winds/Lm;
perm = 1-2.8e-3*T-3e-5*T^2+2e-7*T^3-3e-10*T^4;
L=Al*winds^2*perm*1e-9
%%%%%%%%%%%%%%%%%%%

C = 57e-9;
Vg = 200;
Ts = 5e-6;
Duty = abs(sqrt(P*R/(Vg^2)))
tc = 10e-9;
td1 = 80e-9;
tg = 10e-9;
td = tc + td1 + Duty*Ts + tg;

%State matrices
A = [0 -1/L ; 1/C -1/(C*R)];
B1 = [1/L ; 0];
C1 = [1 0]; %current
D = [0]; % ; 0];

C2 = [0 1];  %voltage

%discrete system matrices
phi = expm(A*Ts);
gamma = expm(A*(Ts-td))*B1*Vg*Ts;

%transfer functions
discsys = ss(phi, gamma, C1, D, Ts);
G_disc = tf (discsys);

discsysV = ss(phi, gamma, C2, D, Ts);
G_discV = tf (discsysV);

figure(1)
bode (G_disc, 'b');
hold on;
%continuous time
s=tf('s');
G_cont=1/(s^2*L*C*R+s*L+R)/(1/(s*C*R+1))*Vg
%figure(2)
bode(G_cont, 'g')
```

Appendix C – Measurement of BH Loops

Within power electronics, there is often a need to design an inductor to utilize space efficiently while maintaining correct operation and low losses in the system. This issue is often left to the designer of the inductor, and more often than not, the solution is to calculate a B_{max}, and call the design done. Verification can sometimes be performed in circuit by looking for waveforms that show significant distortion. Figure C.2 shows waveforms of the circuit in Figure C.1 operating in a resonant mode. It can be seen that the inductor current is being fed by essentially a constant voltage, and from

$$i_L = L\frac{dv_L}{dt} \tag{C.1}$$

$$v_C = C\frac{di_C}{dt}, \tag{C.2}$$

it can be seen that the current should be increasing linearly.

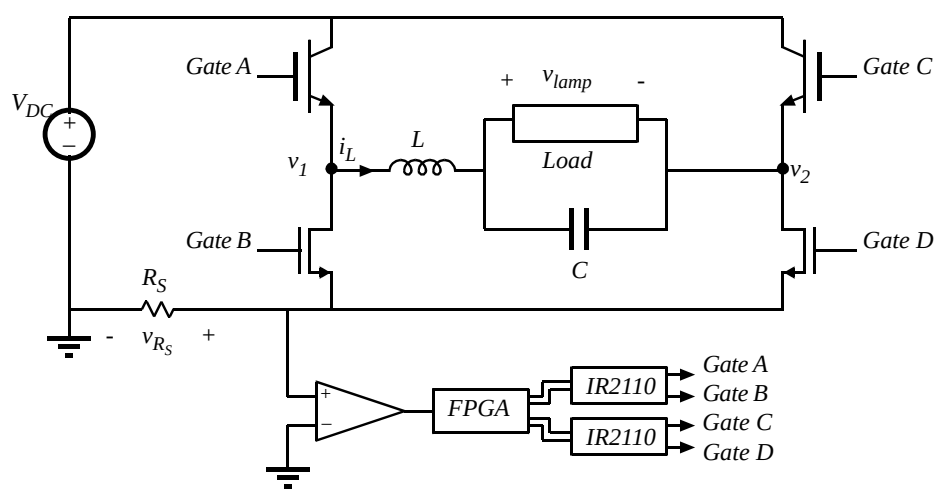

Figure C.1: Resonant ballast circuit

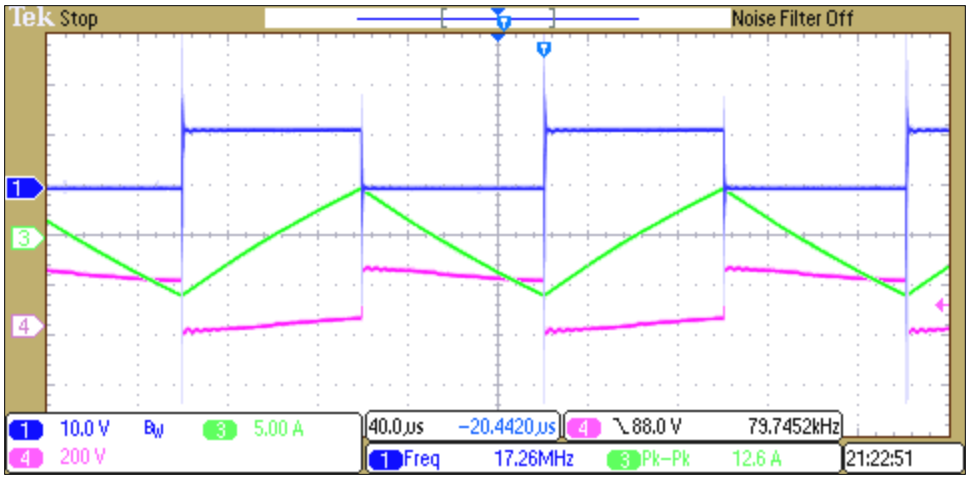

Figure C.2: Hard saturation core inductor operation. Gate B waveform (CH1), Inductor Current (CH3), v_1 (CH4)

Figure C.3 shows similar operation of the circuit, except the inductor is now a soft saturation inductor that is allowed to go into saturation. It can be observed that the peaks of the inductor current waveforms are bent slightly, suggesting the inductance has shifted, as the incident voltage has not changed.

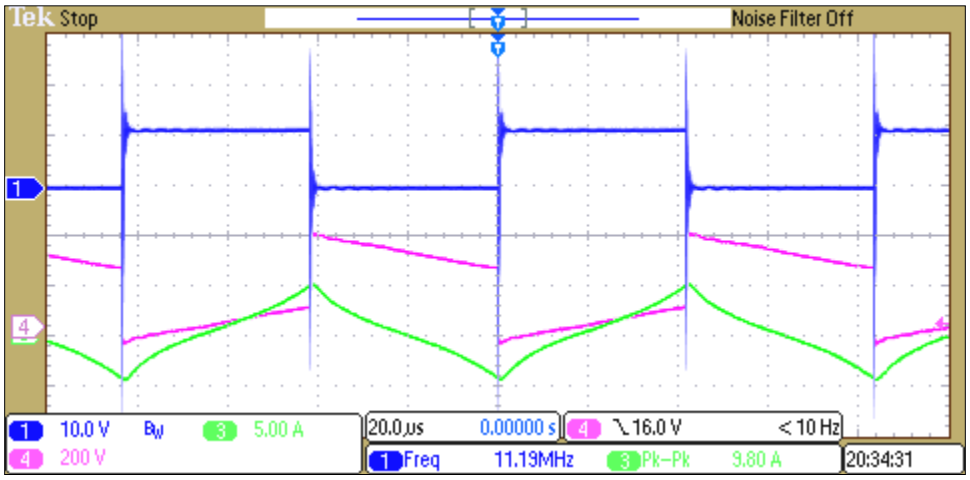

Figure C.3: Soft saturation core inductor operation. Gate B waveform (CH1), Inductor Current (CH3), v1 (CH4)

Such visual inspection methods may suffice for determining if a particular core is reaching saturation, but a more quantitative method is desired. The magnetic field strength, *H*, is proportional to current through the inductor. The magnetic flux density, *B*, is proportional to the

integral of the volts applied across the inductor. A simple test setup is to introduce a sinusoidal voltage or current to the inductor, and measure both the voltage and current seen on and through the inductor. By integrating the voltage across a period, and plotting against current, a qualitative BH loop can be obtained. Care must be taken that the integration of the voltage waveform either begins at a zero crossing, or the area previous to the start of the waveform is known, and introduced as an offset. The flux density measurement is very susceptible to DC offset of the measurement device as well, as there is an integration occurring. For most cases, a simple Riemann sum will suffice in order to produce an acceptable BH loop plot.

If exact quantities are required, the magnetic field strength is related to the current by

$$H = \frac{Ni_L}{le}, \tag{C.3}$$

where N is the turns on the inductor, *le*, is the magnetic length, and I_L is the current through the inductor. The flux density is related by Faradays law:

$$v_L = N\frac{d\Phi}{dt}, \tag{C.4}$$

where Φ is the magnetic flux. Integrating both sides, and relating flux density to flux from

$$B = \frac{\Phi}{A_C}, \tag{C.5}$$

where A_C is the cross sectional area of the core,

$$\int V_L dt = BA_C N. \tag{C.6}$$

From this the relationship of the integral of voltage on the inductor is proportional to the flux density is shown.

If the waveforms of the voltage and current are numerically available, the following MATLAB script will plot the BH loop. There are provision in the code to account for offset within the waveforms, and attempt to remove and DC bias seen in the measurements.

```
start_index = 0;  % set to zero crossing of voltage
stop_index = 50e6; % set to a full integer period of voltage

voltage = voltage_raw(start_index:stop_index);
current = current_raw(start_index:stop_index);

voltage = voltage - mean(voltage);
current = current - mean(current);

offset = -0.8183;  %accounts for offset in probe measurement
v_int = 3e-4;      %accounts for offset in voltage probe

for n = 2:length(voltage)
   v_int = v_int + (data(n,1)-data(n-1,1))*(voltage(n)-offset);
                       %performs integration by Riemann sum
   bh_y(n) = v_int;
end

figure(1)

plot(current,bh_y)

clear bh_y;
```

If all goes well, the result will be a BH loop. If the offsets are not properly set, the result will look like a spring, and the offsets need to be altered. It is suggested to perform the BH loop analysis on at least two periods of the injected sinusoid, in order to more easily determine if the offset is set correctly.